BT236X-800G

4Q Triac

Rev.01 - 25 April 2018 Product data sheet

1. General description

Planar passivated four quadrant triac in a SOT186A (TO-220F) plastic package intended for use in general purpose bidirectional switching and phase control applications.

2. Features and benefits

- High blocking voltage capability
- Planar passivated for voltage ruggedness and reliability
- Least sensitive gate for highest noise immunity
- Triggering in all four quadrants
- Isolated package

3. Applications

- General purpose motor control
- General purpose switching

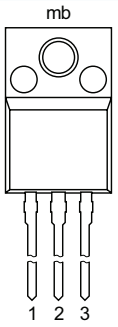
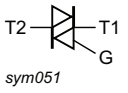
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Values				Unit
Absolute maximum rating							
V_{DRM}	repetitive peak off-state voltage		800				V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_h \leq 88$ °C; Fig. 1; Fig. 2; Fig. 3	6				A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25$ °C; $t_p = 20$ ms; Fig. 4; Fig. 5	65				A
Symbol	**Parameter**	**Conditions**		**Min**	**Typ**	**Max**	**Unit**
Static characteristics							
I_{GT}	gate trigger current	$V_D = 12$ V; $I_T = 0.1$ A; T2+ G+; $T_j = 25$ °C; Fig. 7		-	5	50	mA
		$V_D = 12$ V; $I_T = 0.1$ A; T2+ G-; $T_j = 25$ °C; Fig. 7		-	8	50	mA
		$V_D = 12$ V; $I_T = 0.1$ A; T2- G-; $T_j = 25$ °C; Fig. 7		-	11	50	mA
		$V_D = 12$ V; $I_T = 0.1$ A; T2- G+; $T_j = 25$ °C; Fig. 7		-	30	100	mA

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T1	main terminal 1		
2	T2	main terminal 2		
3	G	gate		
mb	n.c.	mounting base; isolated		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BT236X-800G	TO-220F	plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack"	SOT186A

7. Marking

Table 4. Marking codes

Type number	Marking codes
BT236X-800G	BT236X-800G

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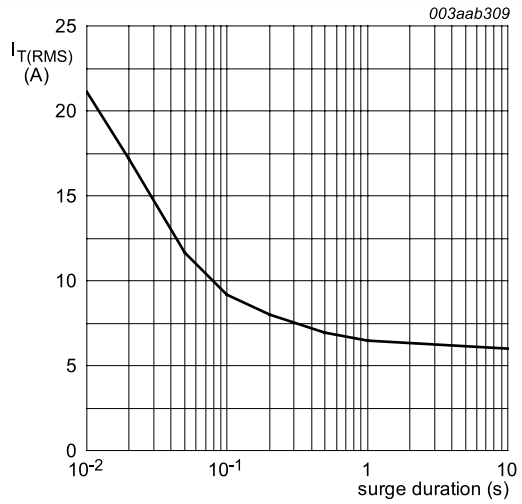
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8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Values	Unit
V_{DRM}	repetitive peak off-state voltage		800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_h \leq 88$ °C; Fig 1; Fig 2; Fig 3	6	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25$ °C; $t_p = 20$ ms; Fig 4; Fig 5	65	A
		full sine wave; $T_{j(init)} = 25$ °C; $t_p = 16.7$ ms	71	A
I^2t	I^2t for fusing	$t_p = 10$ ms; SIN	21	A^2s
dI_T/dt	rate of rise of on-state current	$I_G = 100$ mA; T2+ G+	50	A/µs
		$I_G = 100$ mA; T2+ G-	50	A/µs
		$I_G = 100$ mA; T2- G-	50	A/µs
		$I_G = 200$ mA; T2- G+	10	A/µs
I_{GM}	peak gate current		2	A
P_{GM}	peak gate power		5	W
$P_{G(AV)}$	average gate power	over any 20 ms period	0.5	W
T_{stg}	storage temperature		-40 to 150	°C
T_j	junction temperature		125	°C



f = 50 Hz; T_h = 88 °C

Fig. 1. RMS on-state current as a function of surge duration; maximum values

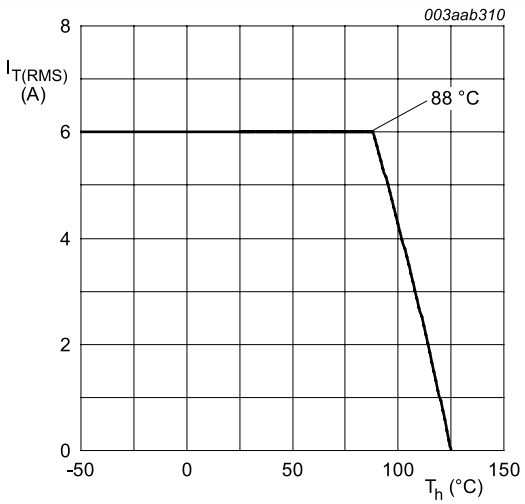
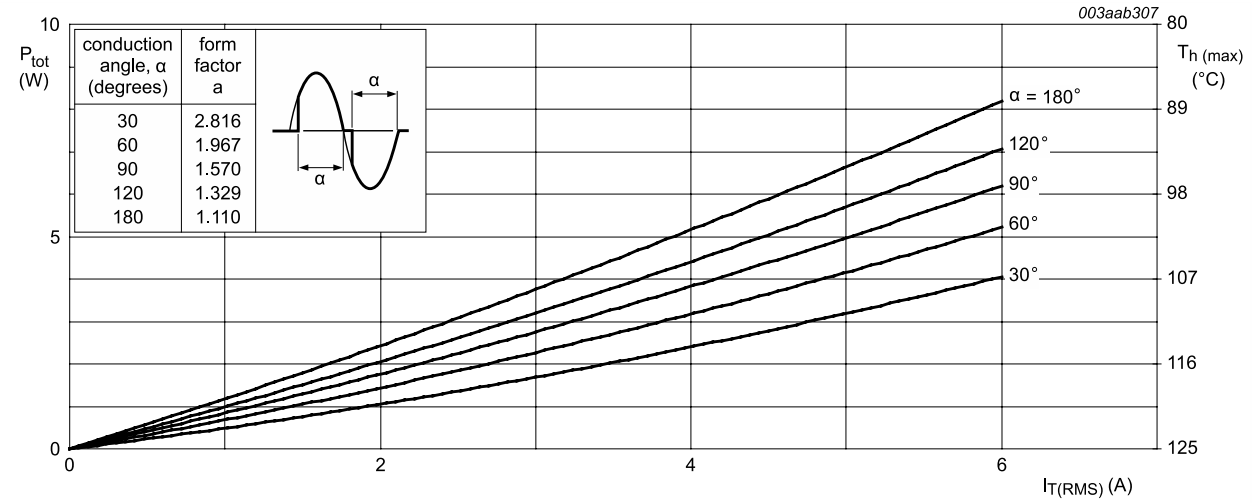


Fig. 2. RMS on-state current as a function of heatsink temperature; maximum values

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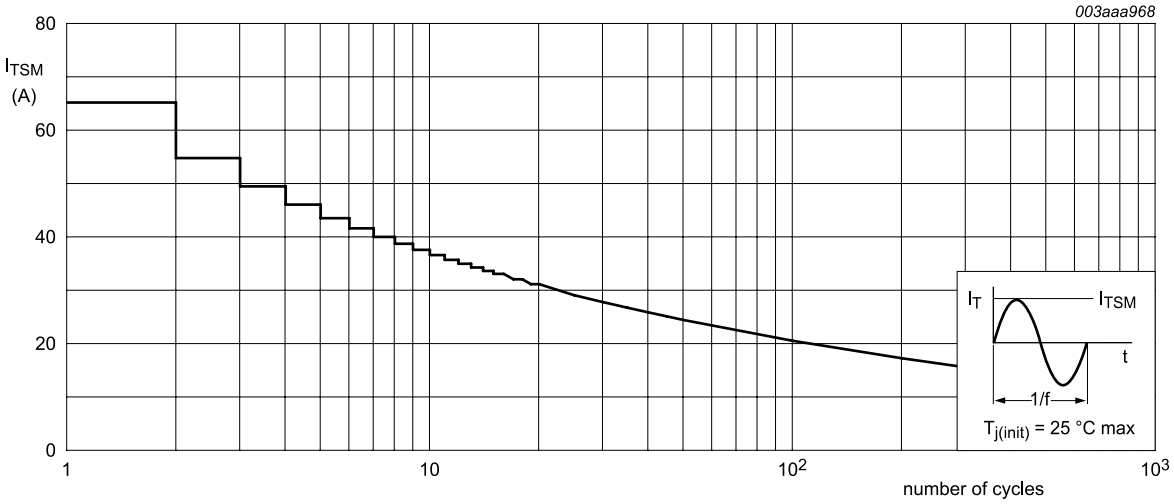
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α = conduction angle

a = form factor = $I_{T(RMS)}$ / $I_{T(AV)}$

Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

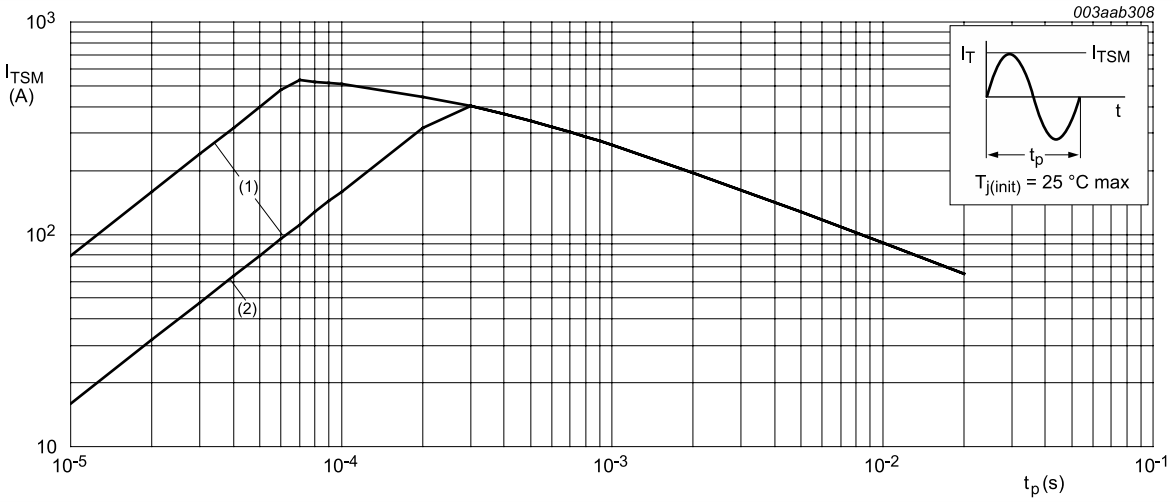


f = 50 Hz

Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

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$t_p \leq 20$ ms
(1) dI_T/dt limit
(2) T2- G+ quadrant limit

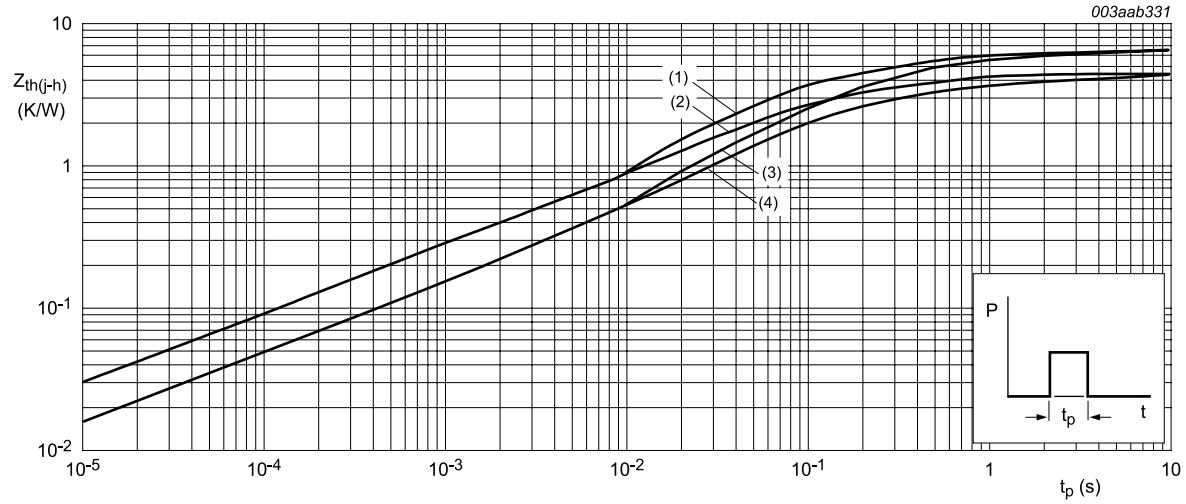
Fig. 5. Non-repetitive peak on-state current as a function of pulse width; maximum values

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9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-h)}$	thermal resistance from junction to heatsink	full or half cycle; with heatsink compound; Fig 6		-	-	4.5	K/W
		full or half cycle; without heatsink compound; Fig 6		-	-	6.5	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air		-	55	-	K/W



(1) Unidirectional (half cycle) without heatsink compound
(2) Unidirectional (half cycle) with heatsink compound
(3) Bidirectional (full cycle) without heatsink compound
(4) Bidirectional (full cycle) with heatsink compound

Fig. 6. Transient thermal impedance from junction to heatsink as a function of pulse width

10. Isolation characteristics

Table 7. Isolation characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{isol(RMS)}$	RMS isolation voltage	from all terminals to external heatsink; sinusoidal waveform; clean and dust free; 50 Hz ≤ f ≤ 60 Hz; RH ≤ 65 %; T_h = 25 °C		-	-	2500	V
C_{isol}	isolation capacitance	from main terminal 2 to external heatsink; f = 1 MHz; T_h = 25 °C		-	10	-	pF

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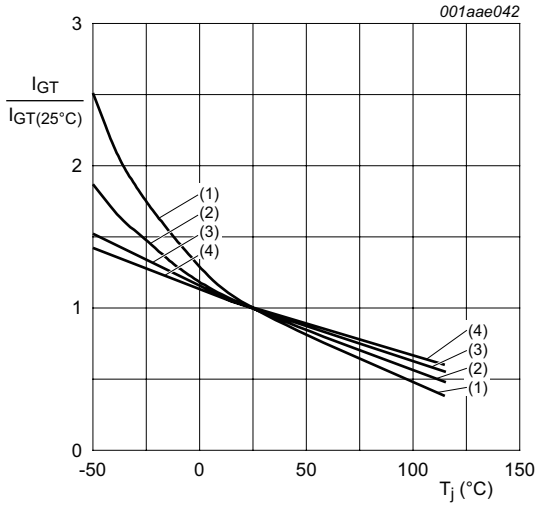
11. Characteristics

Table 8. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 0.1 A; T2+ G+; T_j = 25 °C; Fig. 7		-	5	50	mA
		V_D = 12 V; I_T = 0.1 A; T2+ G-; T_j = 25 °C; Fig. 7		-	8	50	mA
		V_D = 12 V; I_T = 0.1 A; T2- G-; T_j = 25 °C; Fig. 7		-	11	50	mA
		V_D = 12 V; I_T = 0.1 A; T2- G+; T_j = 25 °C; Fig. 7		-	30	100	mA
I_L	latching current	V_D = 12 V; I_G = 0.1 A; T2+ G+; T_j = 25 °C; Fig. 8		-	7	45	mA
		V_D = 12 V; I_G = 0.1 A; T2+ G-; T_j = 25 °C; Fig. 8		-	16	60	mA
		V_D = 12 V; I_G = 0.1 A; T2- G-; T_j = 25 °C; Fig. 8		-	5	45	mA
		V_D = 12 V; I_G = 0.1 A; T2- G+; T_j = 25 °C; Fig. 8		-	7	60	mA
I_H	holding current	V_D = 12 V; T_j = 25 °C; Fig. 9		-	5	40	mA
V_T	on-state voltage	I_T = 10 A; T_j = 25 °C; Fig. 10		-	1.3	1.65	V
V_{GT}	gate trigger voltage	V_D = 12 V; I_T = 0.1 A; T_j = 25 °C; Fig. 11		-	0.7	1	V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 °C; Fig. 11		0.25	0.4	-	V
I_D	off-state current	V_D = 800 V; T_j = 125 °C		-	0.1	0.5	mA
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 536 V; T_j = 125 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit		200	250	-	V/µs
dV_{com}/dt	rate of change of commutating voltage	V_D = 400 V; T_j = 95 °C; I_T = 6 A; dI_{com}/dt = 3.6 A/ms; gate open circuit		10	20	-	V/µs
t_{gt}	gate-controlled turn-on time	V_D = 800 V; I_{TM} = 12 A; I_G = 0.1 A; dI_G/dt = 5 A/µs		-	2	-	µs

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(1) T2- G+
(2) T2- G-
(3) T2+ G-
(4) T2+ G+

Fig. 7. Normalized gate trigger current as a function of junction temperature

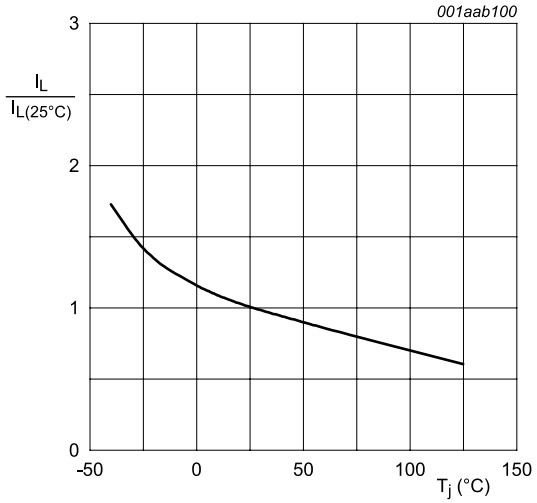


Fig. 8. Normalized latching current as a function of junction temperature

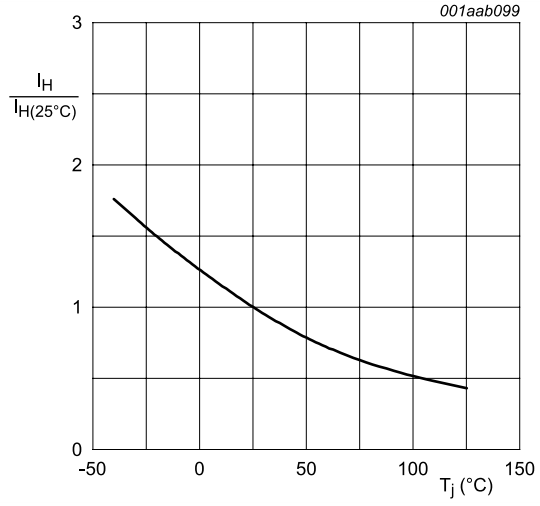
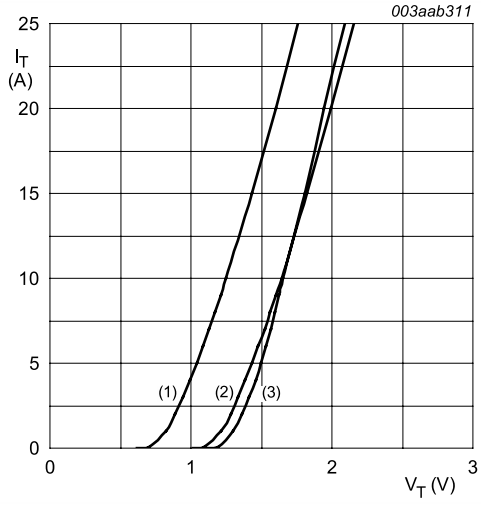


Fig. 9. Normalized holding current as a function of junction temperature



V_o = 1.26 V; R_s = 0.0378 Ω
(1) T_j = 125 °C; typical values
(2) T_j = 125 °C; maximum values
(3) T_j = 25 °C; maximum values

Fig. 10. On-state current as a function of on-state voltage

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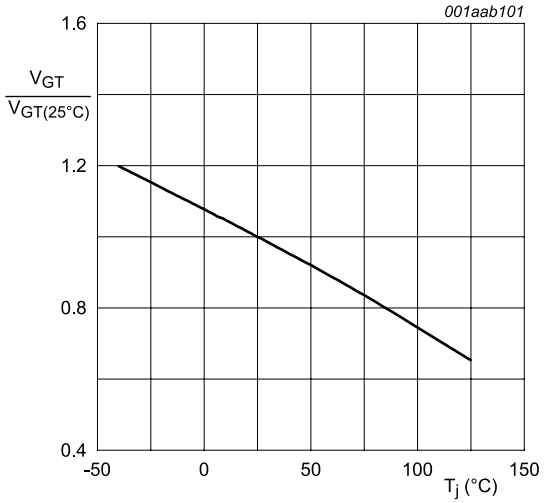


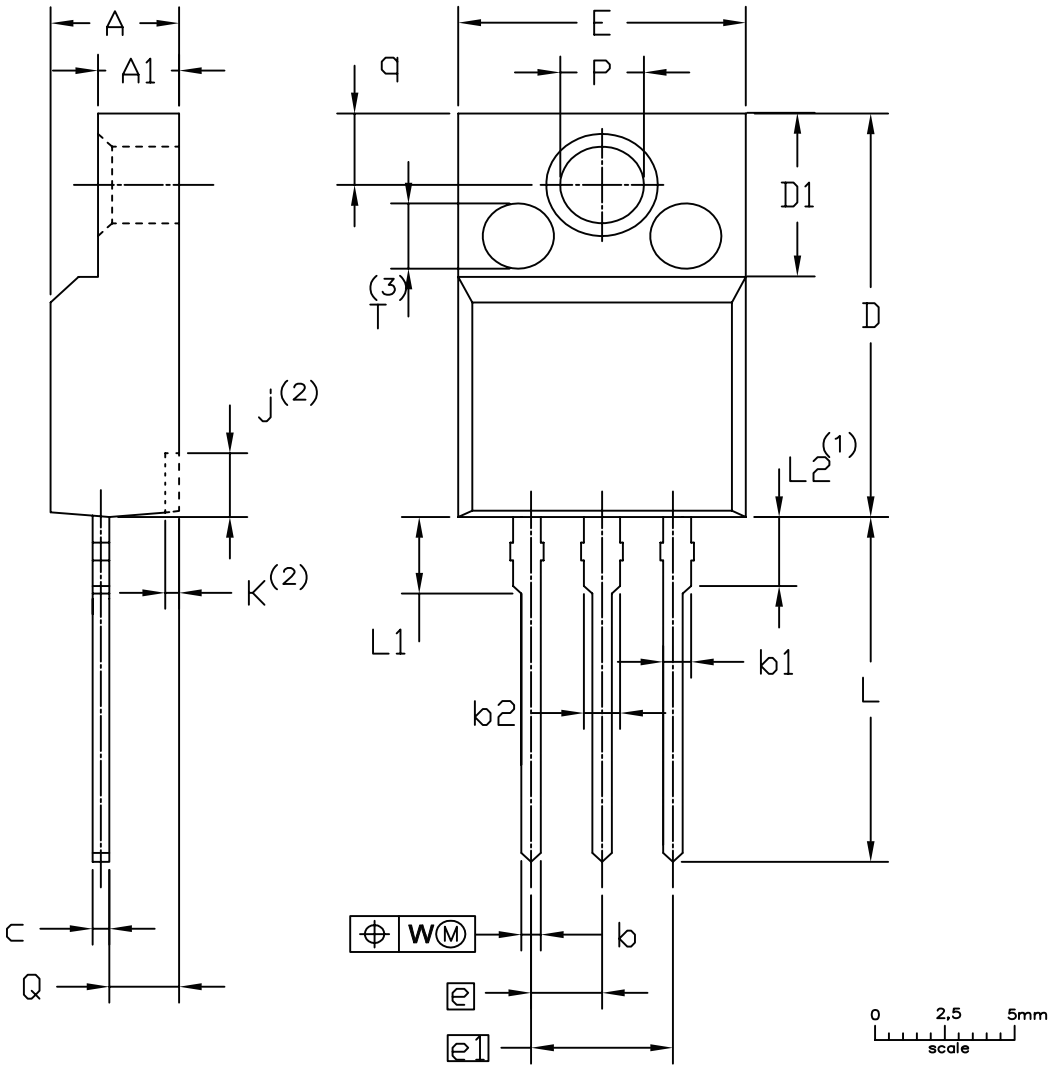
Fig. 11. Normalized gate trigger voltage as a function of junction temperature

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12. Package outline

Plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack" SOT186A



UNIT	A	A_1	b	b_1	b_2	c	D	D_1	E	e	e_1	$j^{(2)}$	$K^{(2)}$	L	L_1	$L_2^{(1)}$ max.	P	Q	q	W	$T^{(3)}$
mm	4.6	2.9	0.9	1.1	1.4	0.7	15.8	6.5	10.3	2.54	5.08	2.7	0.6	14.4	3.30	3	3.2	2.6	3.0	0.4	2.5
	4.0	2.5	0.7	0.9	1.0	0.4	15.2	6.3	9.7			1.7	0.4	13.5	2.79		3.0	2.3	2.6		

Notes
1. Terminal dimensions within this zone are uncotrolled
2. Dot lines area designs may vary
3. Eject pin mark is for reference only

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT186A		3 LEADS TO220F				2013-11-14

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14. Contents

1. General description 1
2. Features and benefits 1
3. Applications 1
4. Quick reference data 1
5. Pinning information 2
6. Ordering information 2
7. Marking 2
8. Limiting values 3
9. Thermal characteristics 6
10. Isolation Characteristics 6
11. Characteristics 7
12. Package outline 10
13. Legal information 11
14. Contents 13

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