BTA312X-600E

3Q Hi-Com Triac

Rev.02 - 25 September 2024 Product data sheet

1. General description

Planar passivated high commutation three quadrant triac in a SOT186A (TO-220F) "full pack" plastic package. This "series E" triac balances the requirements of commutation performance and gate sensitivity and is intended for interfacing with low power drivers including microcontrollers.

2. Features and benefits

- 3Q technology for improved noise immunity
- Direct interfacing with low power drivers and microcontrollers
- Good immunity to false turn-on by dV/dt
- High commutation capability with sensitive gate
- High voltage capability
- Isolated mounting base package
- Planar passivated for voltage ruggedness and reliability
- Sensitive gate for easy logic level triggering
- Triggering in three quadrants only

3. Applications

- Electronic thermostats (heating and cooling)
- High power motor controls e.g. washing machines and vacuum cleaners

4. Quick reference data

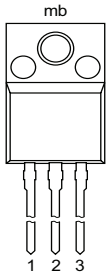
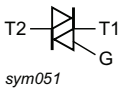
Table 1. Quick reference data

Symbol	Parameter	Conditions	Notes	Values			Unit
V_{DRM}	repetitive peak off-state voltage			600			V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_h \leq 59$ °C; Fig. 1; Fig. 2; Fig. 3		12			A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25$ °C; $t_p = 20$ ms; Fig. 4; Fig. 5		100			A
		full sine wave; $T_{j(init)} = 25$ °C; $t_p = 16.7$ ms		110			A
T_j	junction temperature			125			°C
Symbol	**Parameter**	**Conditions**	**Notes**	**Min**	**Typ**	**Max**	**Unit**
Static characteristics							
I_{GT}	gate trigger current	$V_D = 12$ V; $I_T = 0.1$ A; T2+ G+; $T_j = 25$ °C; Fig. 7		-	-	10	mA
		$V_D = 12$ V; $I_T = 0.1$ A; T2+ G-; $T_j = 25$ °C; Fig. 7		-	-	10	mA
		$V_D = 12$ V; $I_T = 0.1$ A; T2- G-; $T_j = 25$ °C; Fig. 7		-	-	10	mA
I_H	holding current	$V_D = 12$ V; $T_j = 25$ °C; Fig. 9		-	-	15	mA
V_T	on-state voltage	$I_T = 15$ A; $T_j = 25$ °C; Fig. 10		-	1.3	1.6	V

Symbol	Parameter	Conditions	Notes	Min	Typ	Max	Unit
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 402 V; T_j = 125 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit		50	-	-	V/µs
dI_{com}/dt	rate of change of commutating current	V_D = 400 V; T_j = 125 °C; $I_{T(RMS)}$ = 12 A; dV_{com}/dt = 20 V/µs; (snubberless condition); gate open circuit		3	-	-	A/ms
		V_D = 400 V; T_j = 125 °C; $I_{T(RMS)}$ = 12 A; dV_{com}/dt = 10 V/µs; gate open circuit		6		-	A/ms
		V_D = 400 V; T_j = 125 °C; $I_{T(RMS)}$ = 12 A; dV_{com}/dt = 1 V/µs; gate open circuit		10		-	A/ms

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T1	main terminal 1		
2	T2	main terminal 2		
3	G	gate		
mb	n.c	mounting base; isolated		

6. Ordering information

Table 3. Ordering information

Type number	Package Name	Orderable part number	Packing method	Small packing quantity	Package version	Package issue date
BTA312X-600E	TO220F	BTA312X-600E,127	Tube	50	SOT186A	14-Nov-2013
BTA312X-600E/DG		BTA312X-600E/DGQ	Tube	50	SOT186A (Halogen free)	14-Nov-2013

7. Marking

Table 4. Marking codes

Type number	Marking codes	
	Assembly factory: d	Assembly factory: A
BTA312X-600E	BTA312X 600E PJdxxxx xx	BTA312X 600E PJAxxxx xx
BTA312X-600E/DG	BTA312X 600EDG PJdxxxx xx	BTA312X 600EDG PJAxxxx xx

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8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Notes	Values	Unit
V_{DRM}	repetitive peak off-state voltage			600	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_h \leq 59$ °C; Fig. 1; Fig. 2; Fig. 3		12	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25$ °C; $t_p = 20$ ms; Fig 4; Fig 5		100	A
		full sine wave; $T_{j(init)} = 25$ °C; $t_p = 16.7$ ms		110	A
I^2t	I^2t for fusing	$t_p = 10$ ms; SIN		50	A^2s
dI_T/dt	rate of rise of on-state current	$I_G = 0.2$ A		100	A/µs
I_{GM}	peak gate current			2	A
P_{GM}	peak gate power			5	W
$P_{G(AV)}$	average gate power	over any 20 ms period		0.5	W
T_{stg}	storage temperature			-40 to 150	°C
T_j	junction temperature			125	°C

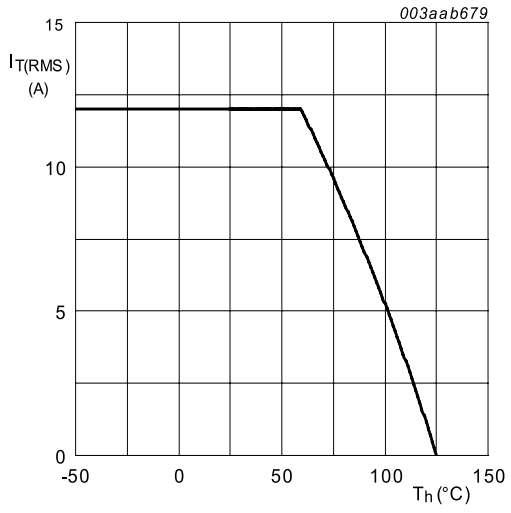
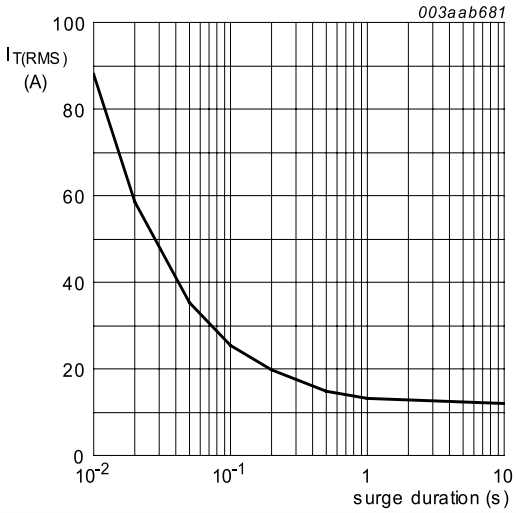


Fig. 1. RMS on-state current as a function of mounting base temperature; maximum values

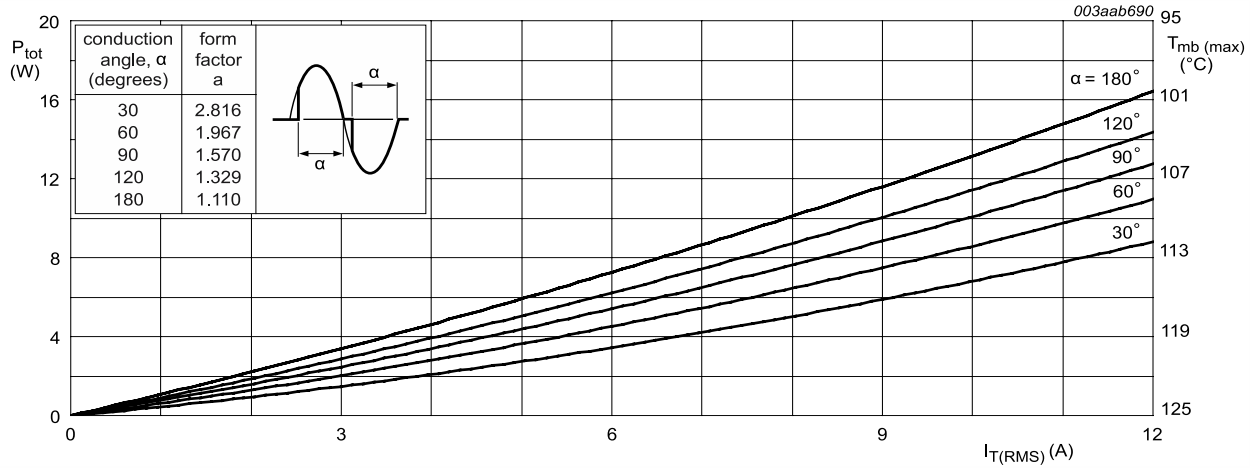


f = 50 Hz; $T_{mb} = 59$ °C

Fig. 2. RMS on-state current as a function of surge duration; maximum values

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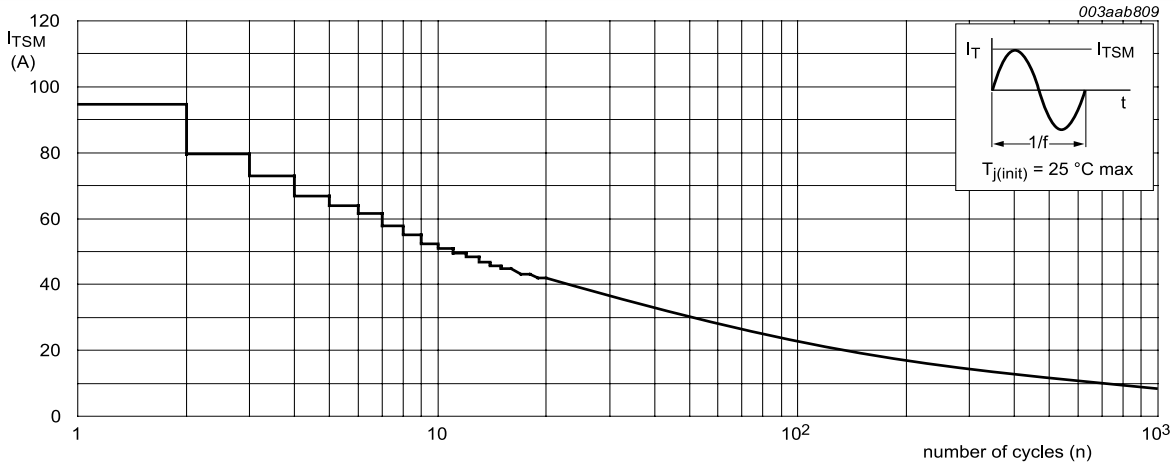
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α = conduction angle

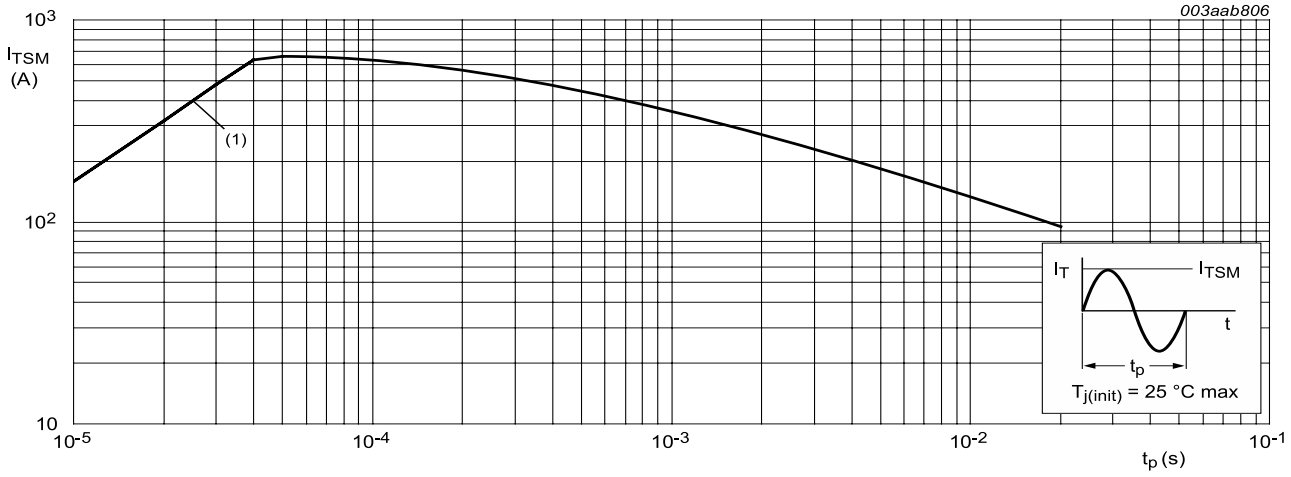
a = form factor = $I_{T(RMS)}$ / $I_{T(AV)}$

Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values



f = 50 Hz

Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



$t_p \leq 20$ ms

(1) dI_T/dt limit

Fig. 5. Non-repetitive peak on-state current as a function of pulse width; maximum values

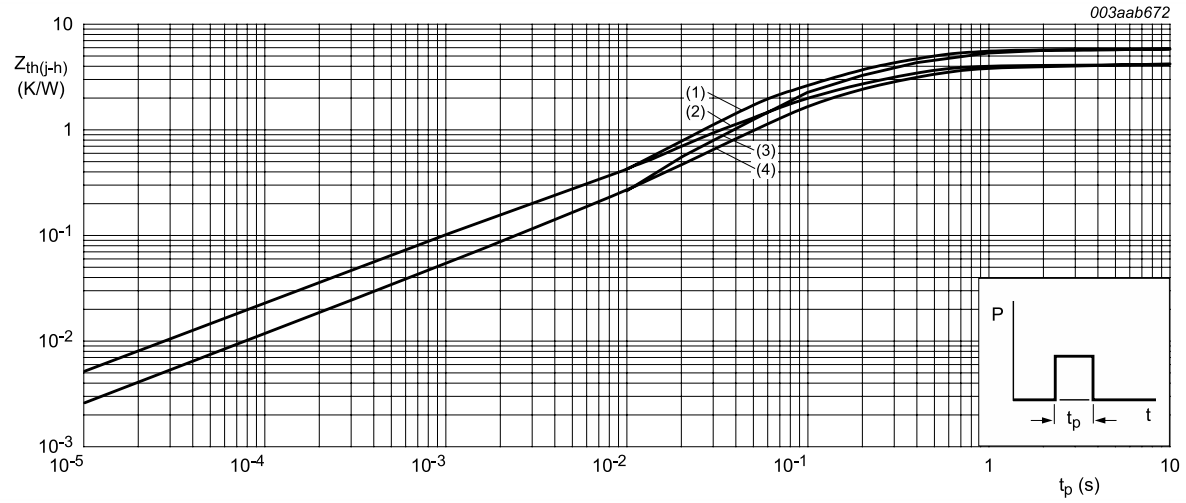
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9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Notes	Min	Typ	Max	Unit
$R_{th(j-h)}$	thermal resistance from junction to heatsink	full cycle or half cycle; with heatsink compound; Fig. 6		-	-	4	K/W
		full cycle or half cycle; without heatsink compound; Fig. 6		-	-	5.5	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air		-	55	-	K/W



(1) Unidirectional (half cycle) without heatsink compound
(2) Unidirectional (half cycle) with heatsink compound
(3) Bidirectional (full cycle) without heatsink compound
(4) Bidirectional (full cycle) with heatsink compound

Fig. 6. Transient thermal impedance from junction to heatsink as a function of pulse duration

10. Isolation characteristics

Table 7. Isolation characteristics

Symbol	Parameter	Conditions	Notes	Min	Typ	Max	Unit
$V_{isol(RMS)}$	RMS isolation voltage	from all pins to external heatsink; sinusoidal waveform; clean and dust free; 50 Hz ≤ f ≤ 60 Hz; RH ≤ 65 %; T_h = 25 °C		-	-	2500	V
C_{isol}	isolation capacitance	from main terminal 2 to external heatsink; f = 1 MHz; T_h = 25 °C		-	10	-	pF

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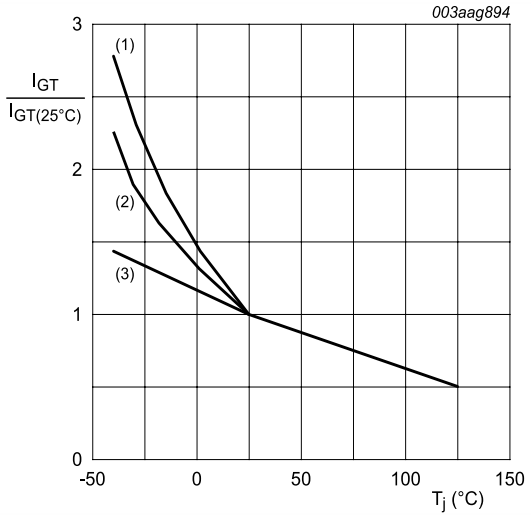
11. Characteristics

Table 8. Characteristics

Symbol	Parameter	Conditions	Notes	Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 0.1 A; T2+ G+; T_j = 25 °C; Fig. 7		-	-	10	mA
		V_D = 12 V; I_T = 0.1 A; T2+ G-; T_j = 25 °C; Fig. 7		-	-	10	mA
		V_D = 12 V; I_T = 0.1 A; T2- G-; T_j = 25 °C; Fig. 7		-	-	10	mA
I_L	latching current	V_D = 12 V; I_G = 0.1 A; T2+ G+; T_j = 25 °C; Fig. 8		-	-	25	mA
		V_D = 12 V; I_G = 0.1 A; T2+ G-; T_j = 25 °C; Fig. 8		-	-	30	mA
		V_D = 12 V; I_G = 0.1 A; T2- G-; T_j = 25 °C; Fig. 8		-	-	25	mA
I_H	holding current	V_D = 12 V; T_j = 25 °C; Fig. 9		-	-	15	mA
V_T	on-state voltage	I_T = 15 A; T_j = 25 °C; Fig. 10		-	1.3	1.6	V
V_{GT}	gate trigger voltage	V_D = 12 V; I_T = 0.1 A; T_j = 25 °C; Fig. 11		-	0.7	1	V
		V_D = 400 V; I_T = 0.1 A; T_j = 150 °C		0.25	0.4	-	V
I_D	off-state current	V_D = 600 V; T_j = 125 °C		-	0.1	0.5	mA
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 402 V; T_j = 125 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit		50	-	-	V/µs
dI_{com}/dt	rate of change of commutating current	V_D = 400 V; T_j = 125 °C; $I_{T(RMS)}$ = 12 A; dV_{com}/dt = 20 V/µs; (snubberless condition); gate open circuit		3	-	-	A/ms
		V_D = 400 V; T_j = 125 °C; $I_{T(RMS)}$ = 12 A; dV_{com}/dt = 10 V/µs; gate open circuit		6		-	A/ms
		V_D = 400 V; T_j = 125 °C; $I_{T(RMS)}$ = 12 A; dV_{com}/dt = 1 V/µs; gate open circuit		10		-	A/ms

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(1) T2- G-
(2) T2+ G-
(3) T2+ G+

Fig. 7. Normalized gate trigger current as a function of junction temperature

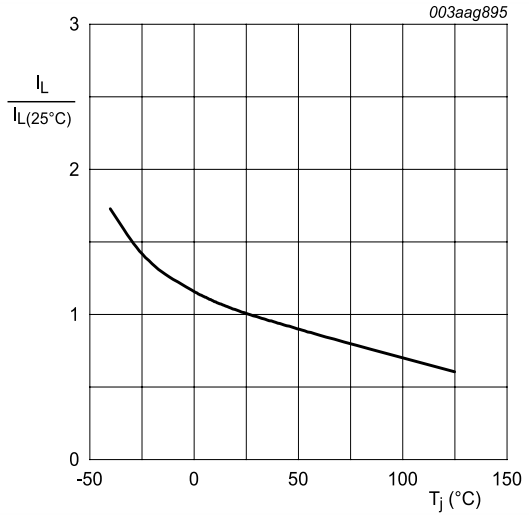


Fig. 8. Normalized latching current as a function of junction temperature

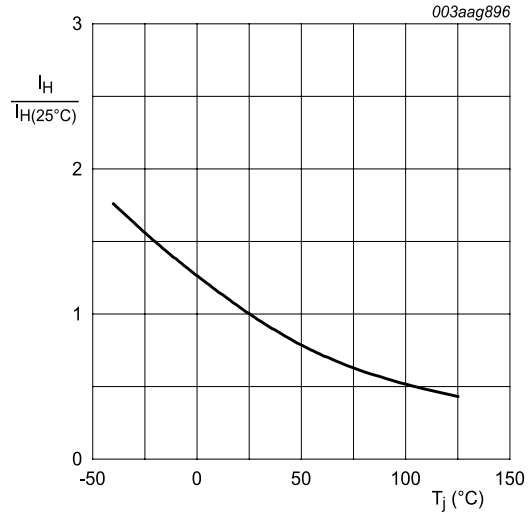
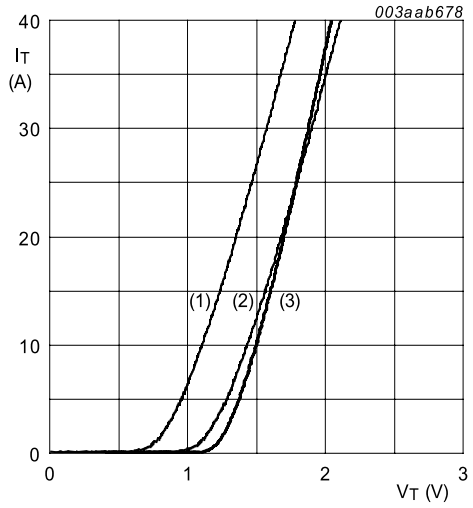


Fig. 9. Normalized holding current as a function of junction temperature



V_o = 1.164 V; R_s = 0.027 Ω
(1) T_j = 125 °C; typical values
(2) T_j = 125 °C; maximum values
(3) T_j = 25 °C; maximum values

Fig. 10. On-state current as a function of on-state voltage

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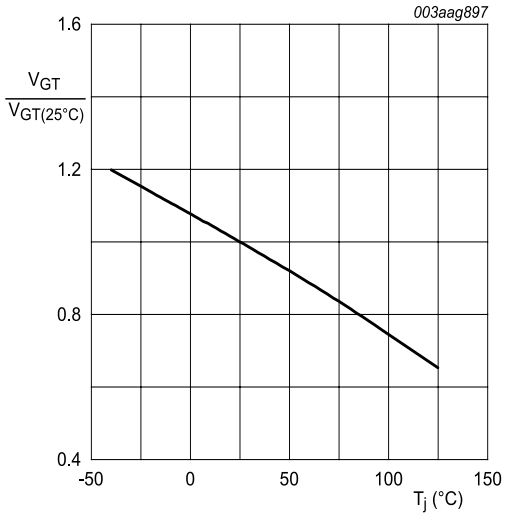


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

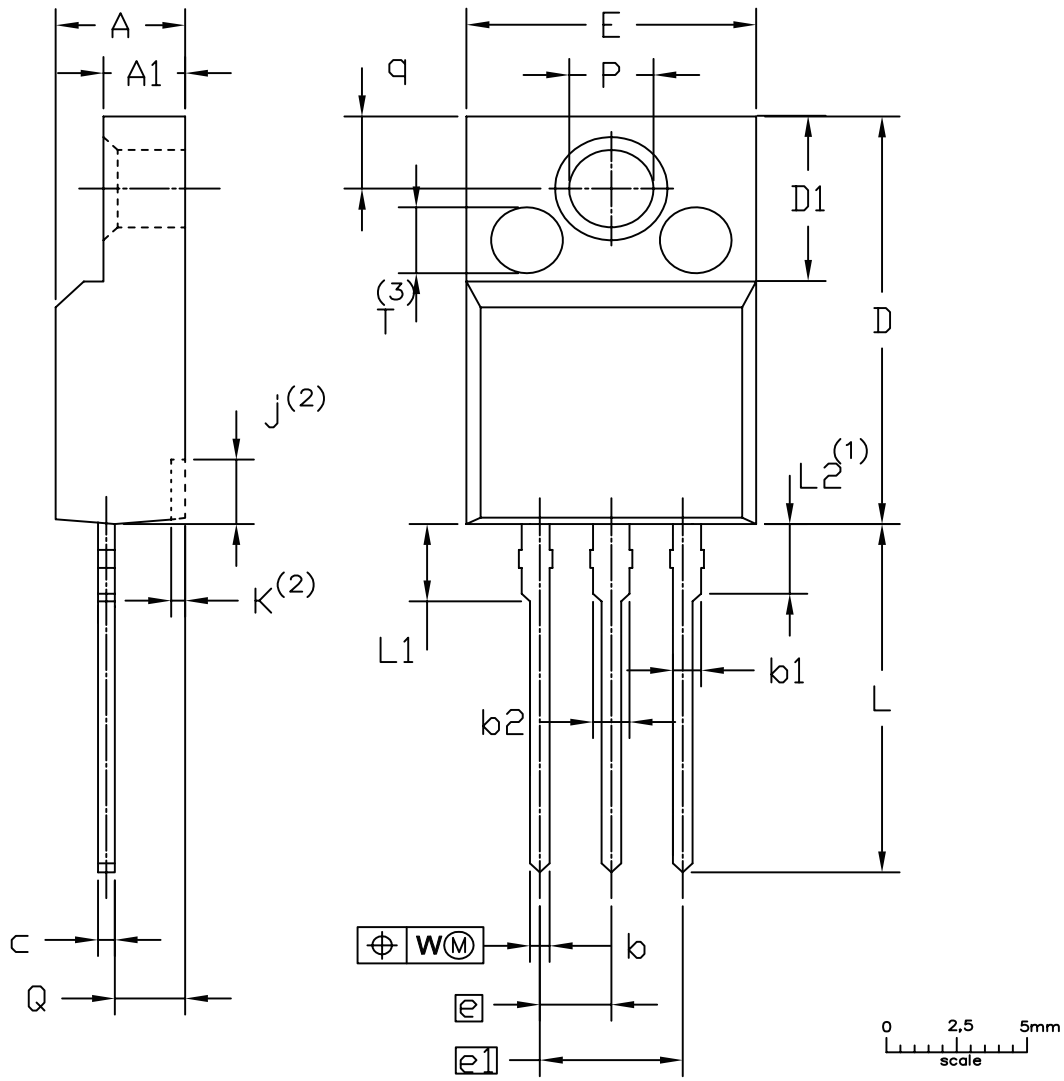
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12. Package outline

Assembly factory: d & A

Plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack" SOT186A



UNIT	A	A_1	b	b_1	b_2	c	D	D_1	E	e	e_1	$j^{(2)}$	$k^{(2)}$	L	L_1	$L_2^{(1)}$ max.	P	Q	q	W	$T^{(3)}$
mm	4.6	2.9	0.9	1.1	1.4	0.7	15.8	6.5	10.3	2.54	5.08	2.7	0.6	14.4	3.30	3	3.2	2.6	3.0	0.4	2.5
	4.0	2.5	0.7	0.9	1.0	0.4	15.2	6.3	9.7			1.7	0.4	13.5	2.79		3.0	2.3	2.6		

Notes
1. Terminal dimensions within this zone are uncotrolled
2. Dot lines area designs may vary
3. Eject pin mark is for reference only

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT186A		3 LEADS TO220F				2013-11-14

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Date of release: 25 September 2024