CC2400
2.4 GHz Low-Power RF Transceiver

Applications

- *2.4 GHz MHz ISM/SRD band systems*
- *Game controllers*
- *Sports and leisure equipment*
- *Wireless audio*
- *PC peripherals*
- *Advanced toys*

Product Description

The ***CC2400*** is a true single-chip 2.4 GHz RF transceiver designed for low-power and low-voltage wireless applications. The RF transceiver is integrated with a baseband modem supporting data rates up to 1 Mbps.

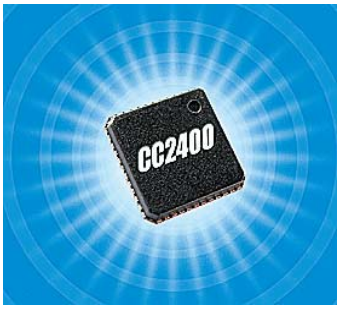
The ***CC2400*** is a low-cost, highly integrated solution enabling robust wireless communication in the 2.4 - 2.4835 GHz unlicensed ISM band. It is intended for systems compliant with world-wide regulations covered by EN 300 440 (Europe), CFR47 Part 15 (US) and ARIB STD-T66 (Japan).

Targeting a wide range of applications at 2.4 GHz, the ***CC2400*** supports over-the-air data rates of 10 kbps, 250 kbps and 1 Mbps without requiring any modifications to the hardware.

The ***CC2400*** provides extensive hardware support for packet handling, data buffering, burst transmissions, data coding and error detection reducing the workload on the host microcontroller.

The main operating parameters of ***CC2400*** can be programmed via an SPI-bus. In a typical system ***CC2400*** will be used together with a microcontroller and a few external, passive components.

CC2400 is based on Chipcon's SmartRF®-03 technology in 0.18 μm CMOS.



Key Features

- True single-chip 2.4 GHz RF transceiver with baseband modem
- 10 kbps, 250 kbps and 1 Mbps over-the-air data rates
- Low current consumption (RX: 24 mA)
- Low core supply voltage (1.8 V)
- Programmable output power
- No external RF switch / filter needed
- I/Q low-IF receiver
- I/Q direct up-conversion transmitter
- Few external components
- FIFO allows bursting of data
- Packet handling hardware
- Data buffering
- Digital RSSI output
- Small size (QFN 48 package), 7x7 mm
- Reference design complies with EN 300 328, EN 300 440, FCC CFR47 part 15 and ARIB STD-T66
- Powerful and flexible development tools available
- Easy-to-use software for generating the ***CC2400*** configuration data

This document contains information on a pre-production product. Specifications and information herein are subject to change without notice.

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1 Abbreviations

ACP	Adjacent Channel Power
ACR	Adjacent Channel Rejection
ADC	Analog-to-Digital Converter
AFC	Automatic Frequency Correction
AGC	Automatic Gain Control
BER	Bit Error Rate
BOM	Bill Of Materials
bps	bits per second
BT	Bandwidth-Time product (for GFSK)
CRC	Cyclic Redundancy Check
CSMA	Carrier Sense Multiple Access
CSMA / CA	Carrier Sense Multiple Access / Collision Avoidance
DAC	Digital-to-Analog Converter
ESR	Equivalent Series Resistance
FH	Frequency Hopping
FHSS	Frequency Hopping Spread Spectrum
FIFO	First In First Out (queue)
FS	Frequency Synthesizer
FSK	Frequency Shift Keying
GFSK	Gaussian Frequency Shift Keying
IF	Intermediate Frequency
ISM	Industrial Scientific Medical
kbps	kilo bits per second
LNA	Low Noise Amplifier
Mbps	Mega bits per second
MCU	Micro Controller Unit
NRZ	Non Return to Zero
PA	Power Amplifier
PD	Phase Detector
PCB	Printed Circuit Board
PN9	Pseudo-random Bit Sequence (9-bit)
PLL	Phase Locked Loop
PRN	Pseudo Random Number
PRNG	Pseudo Random Number Generator
RF	Radio Frequency
RSSI	Received Signal Strength Indicator
RX	Receive (mode)
SPI	Serial Peripheral Interface
SRD	Short Range Device
TBD	To Be Decided/Defined
TDMA	Time Division Multiple Access
TX	Transmit (mode)
VCO	Voltage Controlled Oscillator
VGA	Variable Gain Amplifier

2 Features

- 2400 – 2483 MHz RF transceiver
  - GFSK and FSK modulation
  - Very low current consumption (RX: 24 mA)
  - Over-the-air data rates of 10 kbps, 250 kbps and 1 Mbps
  - High sensitivity (-87 dBm @ 1Mbps, BER=10^{-3})
  - Agile frequency synthesizer (40 us settling time)
  - On-chip VCO, LNA and PA
  - Low core supply voltage (1.6-2.0 V)
  - Flexible I/O supply voltage (1.6–3.6 V) to match the signal levels of the interfacing microcontroller
  - Programmable output power
  - I/Q low-IF receiver
  - I/Q direct up-conversion transmitter
- Few external components
  - Only reference crystal and a few passives needed
  - No external filters needed
- Programmable baseband modem
  - 4-wire SPI interface
  - Serial clock up to 20 MHz
  - Digital RSSI output
- Packet handling hardware support
  - Preamble generator with programmable length
  - Programmable synchronization word insertion/detection
  - CRC computation over the data field
  - 8B/10B line coding option
- Data buffering
  - 32 byte FIFO
  - Provides for flexible communication with the host controller.
  - Burst transmission reduces the average power consumption.
- Powerful and flexible development tools available
  - Fully equipped development kit
  - Demonstration board reference design with microcontroller code
  - Easy-to-use SmartRF Studio software for generating the ***CC2400*** configuration data
- Small size (QFN 48 package) 7 x 7 mm
- Reference design complies with EN 300 328, EN 300 440, FCC CFR47 part 15 and ARIB STD-T66

3 Absolute Maximum Ratings

Parameter	Min.	Max.	Units	Condition
Supply voltage, chip core, AVDD/DVDD1.8=VDD	−0.3	2.0	V	
Supply voltage (DVDD3.3=VDDIO), digital I/O	−0.3	3.6	V	
Voltage on any pin, core	−0.3	VDD+0.3, max 2.0	V	
Voltage on any pin, digital I/O (pin no. 27-35)	−0.3	VDDIO+0.3, max 3.6	V	
Input RF level		10	dBm	
Storage temperature range	−50	150	°C	
Reflow solder temperature		260	°C	T = 10 s

NOTE:

The supply voltage to the chip core (AVDD/DVDD1.8) should not be switched off when the digital IO (DVDD3.3) supply voltage is still applied to the chip. If this is done, a large current will flow inside the ***CC2400*** and the chip may be damaged as a result.

If the core supply needs to be switched off to lower the power consumption, please see page 17 for a suggested solution.

The absolute maximum ratings given above should under no circumstances be violated. Stress exceeding one or more of the limiting values may cause permanent damage to the device.



Caution! *ESD sensitive device. Precaution should be used when handling the device in order to prevent permanent damage.*

4 Operating Conditions

Parameter	Min.	Typ.	Max.	Unit	Condition
Supply voltage, chip core, AVDD/DVDD1.8	1.6		2.0	V	
Supply voltage (DVDD3.3), digital I/O, VDDIO	1.6		3.6	V	The digital I/O voltage (DVDD3.3 pin) must match the interfacing circuit.
Recommended supply voltage, chip core, AVDD/DVDD1.8		1.8V			
Recommended supply voltage (DVDD3.3), digital I/O		1.8V/ 3.3V			
Operating ambient temperature range	−40		85	°C	

5 Electrical Specifications

Parameter	Min.	Typ.	Max.	Unit	Condition / Note
Current Consumption, Power Down mode (OFF)		1.5	5	μA	Oscillator core off
Current Consumption, Idle mode (IDLE)		1.2		mA	
Current Consumption, Frequency synthesizer (FS_ON)		6.3		mA	
Current Consumption, Receive mode		24		mA	
Current Consumption, Transmit mode:					
P=−25 dBm		11		mA	The output power is delivered differentially to a 50Ω single-ended load through a balun, see also p. 50.
P=−5 dBm		15		mA	
P=0 dBm		19		mA	
Current Consumption, crystal oscillator core		38		μA	16 MHz, 16 pF load crystal

Table 1 Electrical specifications

6 General Characteristics

Tc = 25°C, AVDD/DVDD1.8 = 1.8 V, DVDD3.3 = 3.3V (digital I/O) if nothing else stated. Measured on Chipcon's CC2400EM reference design.

Parameter	Min.	Typ.	Max.	Unit	Condition / Note
RF Frequency Range	2400		2483	MHz	Programmable in 1 MHz channel steps.
Data rate		10 250 1		kbps kbps Mbps	Data rate is programmable/selectable, see page 40

Table 2 General characteristics

7 RF Transmit section

Tc = 25°C, AVDD/DVDD1.8 = 1.8 V, DVDD3.3 = 3.3V (digital I/O) if nothing else stated. Measured on Chipcon's CC2400EM reference design.

Parameter	Min.	Typ.	Max.	Unit	Condition / Note
Binary FSK frequency deviation	0	250	500	±kHz	The frequency corresponding to the digital "0" is denoted f_0, while f_1 corresponds to a digital "1". The frequency deviation is given by $f_d=\pm(f_1-f_0)/2$. The RF carrier frequency, f_c, is then given by $f_c=(f_0+f_1)/2$.
Nominal output power		0		dBm	Default settings. Power delivered to a 50 Ω single-ended load through a balun. The output power is programmable in 8 steps.
Programmable output power range		25		dB	
20 dB bandwidth FSK GFSK		 1.2 1.0		 MHz MHz	Maximum output power. Modulation is 1 Mbps, NRZ data, ± 250 kHz frequency deviation.
Adjacent Channel Power (ACP) FSK GFSK		 -30 -43		 dBc dBc	Maximum output power. Modulation is 1 Mbps, NRZ data, ± 250 kHz frequency deviation. Measured at 2 MHz offset.
Harmonics 2nd order harmonic 3rd order harmonic		 -41 -54		 dBm dBm	At max output power delivered to 50 Ω single-ended load through a balun. Carrier modulated with pseudo-random data. See p.50.
Spurious emission 30 - 1000 MHz 1– 12.75 GHz 1.8 – 1.9 GHz 5.15 – 5.3 GHz		 -65 -41 -69 -65	 -36 -30 -47 -47	 dBm dBm dBm dBm	Maximum output power. Modulation is 1 Mbps FSK, NRZ data, ±250 kHz frequency deviation. Complying with EN 300 440, CFR47 Part 15 and ARIB STD-T66
Optimum load impedance		110 + j130		Ω	Differential impedance as seen from the RF-port (RF_P and RF_N) towards the antenna. For matching details see "Input/ output matching" page 50 as well as the application circuit description on page 17.

Table 3 Transmit characteristics

8 RF Receive section

Tc = 25°C, AVDD/DVDD1.8 = 1.8 V, DVDD3.3 = 3.3V (digital I/O) if nothing else stated. Measured on Chipcon's CC2400EM reference design.

Parameter	Min.	Typ.	Max.	Unit	Condition / Note
Receiver Sensitivity at BER = 10^{-3}					Measured in a 50 Ohm single-ended load through a balun. FSK, NRZ mode used.
1 Mbps, 1 MHz channel BW		-87		dBm	±250 kHz frequency deviation
250 kbps, 1 MHz channel BW		-91		dBm	±250 kHz frequency deviation
10 kbps, 500 kHz channel BW		-101		dBm	±125 kHz frequency deviation
Saturation (maximum input level)		3		dBm	Maximum gain in LNA. NRZ coded data, BER = 10^{-3}
Co-channel rejection		-10		dB	1 Mbps wanted signal 10 dB above the sensitivity level, interferer modulated like signal (pseudo-random FSK, ± 250 kHz deviation), interferer at operating frequency, BER = 10^{-3}
Adjacent channel rejection (ACR)					FSK wanted signal 10 dB above the sensitivity level, 1 MHz channel spacing, interferer modulated like signal (pseudo-random FSK, ± 250 kHz deviation) at adjacent channel, BER = 10^{-3}
1 Mbps		0		dB	
250 kbps		12		dB	
Image channel rejection					FSK wanted signal 10 dB above the sensitivity level, interferer modulated like signal (pseudo-random FSK, ± 250 kHz deviation) at image frequency, BER = 10^{-3}. The image channel is centered 2MHz below the center frequency of the desired channel.
1 Mbps		21		dB	
250 kbps		39		dB	
Selectivity (C/I) (In-band channel rejection)					
+ 2MHz		20		dB	1Mbps FSK wanted signal at 2441 MHz, 3 dB above the sensitivity level (except + 2 MHz, which is 10 dB above the sensitivity limit), jammer modulated like signal (pseudo-random, ± 250 kHz deviation) at ± 2-39 MHz in 1 MHz steps offset, BER = 10^{-3}. Adjacent channels and image channel are excluded.
± 3MHz		41		dB	
± 4MHz		50		dB	
± 5MHz		52		dB	
± 10MHz		55		dB	
± 20 MHz		56		dB	
± 50MHz		59		dB	
+ 2 MHz		48		dB	250 kbps FSK wanted signal at 2441 MHz, 3 dB above the sensitivity level (except + 2 MHz, which is 10 dB above the sensitivity limit), jammer modulated like signal (pseudo-random, ± 250 kHz deviation) at ± 2-39 MHz in 1 MHz steps offset, BER = 10^{-3}. Adjacent channels and image channel are excluded.
± 3 MHz		50		dB	
± 4 MHz		55		dB	
± 5 MHz		56		dB	
± 10 MHz		59		dB	
± 20 MHz		60		dB	
± 50 MHz		64		dB	

Parameter	Min.	Typ.	Max.	Unit	Condition / Note
Blocking / Desensitization* (*out-of-band spurious response rejection) 0.3 – 2.0 GHz 2.0 – 2.399 GHz 2.498 – 3.0 GHz 3 – 12.75 GHz		 71 50 49 76		 dB dB dB dB	 1 Mbps FSK wanted signal 3 dB above the sensitivity level, sine-wave interfering signal, BER = 10^{-3}.
Input IIP3 Out of band In band		 -5 -17		 dBm dBm	 Measured directly by applying two tones and measuring the resulting difference tone amplitude.
Image frequency suppression		56		dB	Ratio between sensitivity for a signal at the image frequency and the sensitivity in the wanted channel with an inverted signal. The image frequency is centered -2 MHz from the center of the wanted channel. The signal source is 1Mbps, NRZ coded data, ±250 kHz frequency deviation, signal level for BER = 10^{-3}
Spurious reception		80		dB	Ratio between the sensitivity for an unwanted frequency and the sensitivity in the wanted channel. The signal source is a 1 Mbps, NRZ coded data, ±250 kHz frequency deviation, swept over all frequencies 2400 – 2483.5 MHz. Signal level for BER = 10^{-3} Adjacent channels and image channel are excluded.
Spurious emission < 1 GHz 1 – 12.75 GHz		 −70 −56	 -57 -47	 dBm dBm	Complying with EN 300 440, CFR47 Part 15 and ARIB STD-T66

Table 4 RF Receive characteristics

9 AFC section

Parameter	Min.	Typ.	Max.	Unit	Condition / Note
					For 1Mbps and 1 MHz channel width, AFC_SETTLING=4.
AFC range		± 500		kHz	Measured using an unmodulated carrier.
AFC accuracy		5		kHz	

Table 5 AFC characteristics

10 RSSI / Carrier Sense section

Parameter	Min.	Typ.	Max.	Unit	Condition / Note
RSSI range / Carrier sense range		80		dB	For 1Mbps and 1 MHz channel width. (The range is from –100 dBm to –20 dBm typically)
RSSI settling time		20		µs	
RSSI accuracy		± 4		dB	See page 44 for details

Table 6 RSSI / Carrier sense characteristics

11 IF section

Parameter	Min.	Typ.	Max.	Unit	Condition / Note
Intermediate frequency (IF)		1		MHz	
Digital channel filter bandwidth	125		1000	kHz	The digital channel filter 6dB-bandwidth is programmable in steps: 125, 250, 500 and 1000 kHz. See page 39 for details.

Table 7 IF characteristics

12 Frequency Synthesizer section

Parameter	Min.	Typ.	Max.	Unit	Condition / Note
Crystal oscillator frequency		16		MHz	See page 49 for details.
Crystal frequency accuracy requirement			20	±ppm	The total crystal frequency accuracy, i.e. initial tolerance plus aging and temperature dependency, will determine the frequency accuracy of the transmitted signal. 1 Mbps FSK, 250 kHz deviation.
Crystal operation		Parallel			C4 and C5 are loading capacitors, see page 49
Crystal load capacitance	12	16	20	pF	16 pF recommended
Crystal ESR			60	Ω	
Crystal oscillator start-up time		1.13		ms	16 pF load Note: This time can be reduced to 15 µs by enabling the XOSC core in power-down using the MANAND register.
Phase noise		-108 -114 -114		dBc/Hz dBc/Hz dBc/Hz	Unmodulated carrier At ±1 MHz offset from carrier At ±2 MHz offset from carrier At ±5 MHz offset from carrier
PLL loop bandwidth		50		kHz	

Parameter	Min.	Typ.	Max.	Unit	Condition / Note
PLL lock time (RX / TX turn-on time)		40		μs	Until within ± 10 kHz Step size is 1MHz, no calibration. Note: Calibration should be performed for frequency changes > 8 MHz.
PLL turn-on time from IDLE mode, crystal oscillator on		100		μs	Crystal oscillator running. Calibration time included.

Table 8 Frequency synthesizer characteristics

13 Digital Inputs/Outputs

Parameter	Min.	Typ.	Max.	Unit	Condition / Note
Logic "0" input voltage	0		0.3* DVDD	V	Signal levels are referred to the voltage level at the pin DVDD3.3.
Logic "1" input voltage	0.7* DVDD		DVDD	V	
Logic "0" output voltage	0		0.4	V	Output current −8 mA, 3.3 V supply voltage
Logic "1" output voltage	2.5		DVDD	V	Output current 8 mA, 3.3 V supply voltage
Logic "0" input current	NA		−1	μA	Input signal equals GND
Logic "1" input current	NA		1	μA	Input signal equals DVDD
DIO setup time	20			ns	TX un-buffered mode, minimum time DIO must be ready before the positive edge of DCLK
DIO hold time	10			ns	TX un-buffered mode, minimum time DIO must be held after the positive edge of DCLK
Serial interface (SCLK, SI, SO and CSn) timing specification					See Table 12 page 22

Table 9 Digital input/output characteristics

14 Pin Assignment

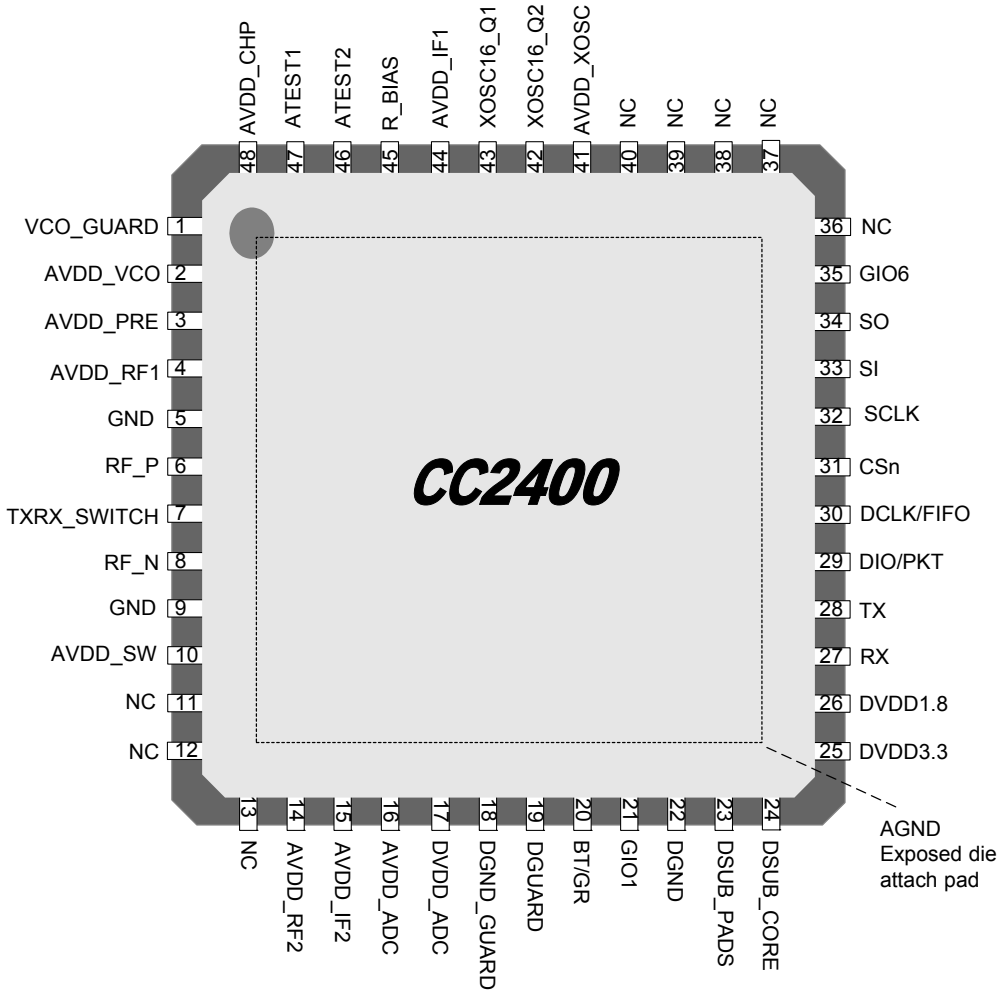


Figure 1 *CC2400* Top View

Pin no.	Pin name	Pin type	Description
-	AGND	Ground (analog)	Exposed die attach pad. **Must** be connected to solid ground plane
1	VCO_GUARD	Power (Analog)	Connection of guard ring for VCO shielding
2	AVDD_VCO	Power (Analog)	Power supply for VCO
3	AVDD_PRE	Power (Analog)	Power supply for Prescaler
4	AVDD_RF1	Power (Analog)	Power supply for RF front-end
5	GND	Ground (Analog)	Grounded pin for RF shielding
6	RF_P	RF I/O	Positive RF input/output signal to LNA/from PA in receive/transmit mode
7	TXRX_SWITCH	Power (Analog)	Common supply connection for RF front-end. Must be connected to RF_P and RF_N externally through a DC path.
8	RF_N	RF I/O	Negative RF input/output signal to LNA/from PA in receive/transmit mode
9	GND	Ground (Analog)	Grounded pin for RF shielding
10	AVDD_SW	Power (Analog)	Power supply connection

Pin no.	Pin name	Pin type	Description
11	NC	---	No Connect
12	NC	---	No Connect
13	NC	---	No Connect
14	AVDD_RF2	Power (Analog)	Power supply for receive and transmit mixers
15	AVDD_IF2	Power (Analog)	Power supply for transmit IF chain
16	AVDD_ADC	Power (Analog)	Power supply connection of ADCs and DACs
17	DVDD_ADC	Power (Digital)	Power supply for digital part of receive ADCs
18	DGND_GUARD	Ground (Digital)	Ground connection for digital noise isolation
19	DGUARD	Power (Digital)	Power supply connection for digital noise isolation
20	BT/GR	Digital Input	Selection of Built-in-Test or Generic Radio (normal operation). Connect to ground for normal operation (NOTE: For Chipcon internal use only.)
21	GIO1	Digital I/O	General digital I/O pin. Configure as output when not used. See Table 18
22	DGND	Ground (Digital)	Ground connection for digital modules
23	DSUB_PADS	Ground (Digital)	Substrate connection for digital I/O's
24	DSUB_CORE	Ground (Digital)	Substrate connection for digital modules
25	DVDD3.3	Power (Digital)	Power supply for digital I/O's
26	DVDD1.8	Power (Digital)	Power supply for digital modules
27	RX	Digital Input	Strobe signal for RX mode. Connect to ground when not used.
28	TX	Digital I/O	Strobe signal for TX mode. Connect to ground when not used.
29	DIO/PKT	Digital I/O	Data input/output in un-buffered mode or packet handling control signal. Configure as output when not used.
30	DCLK/FIFO	Digital Output	Data clock output signal in un-buffered mode or FIFO control signal. Leave open when not used.
31	CSn	Digital Input	SPI: Chip Select
32	SCLK	Digital Input	SPI: Serial data clock
33	SI	Digital Input	SPI: Slave Input
34	SO	Digital Output	SPI: Slave Output
35	GIO6	Digital Output	General digital output pin. See Table 18
36	NC	---	No Connect
37	NC	---	No Connect
38	NC	---	No Connect
39	NC	---	No Connect
40	NC	---	No Connect
41	AVDD_XOSC	Power (Analog)	Power supply for 16 MHz crystal oscillator
42	XOSC16_Q2	Analog output	16 MHz crystal oscillator
43	XOSC16_Q1	Analog input	16 MHz crystal oscillator or external clock input
44	AVDD_IF1	Power (Analog)	Power supply connection of receive IF chain
45	R_BIAS	Analog Output	Connection for external precision bias resistor
46	ATEST2	Analog I/O	Analog test I/O for prototype and production testing. Leave not connected when not used.
47	ATEST1	Analog I/O	Analog test I/O for prototype and production testing. Leave not connected when not used.
48	AVDD_CHP	Power (Analog)	Power supply for phase detector and charge pump

NOTES:

The exposed die attach pad **must** be connected to a solid ground plane as this is the main ground connection for the chip.

The digital inputs SCLK, SI and CSn are high-impedance inputs (no internal pull-up) and should have external pull-ups if not driven. RX and TX should have external pull-down if not driven (to prevent the state machine from being trigged). SO is high-impedance when CSn is high. External pull-up should be used at SO to prevent floating input at the microcontroller.

15 Circuit Description

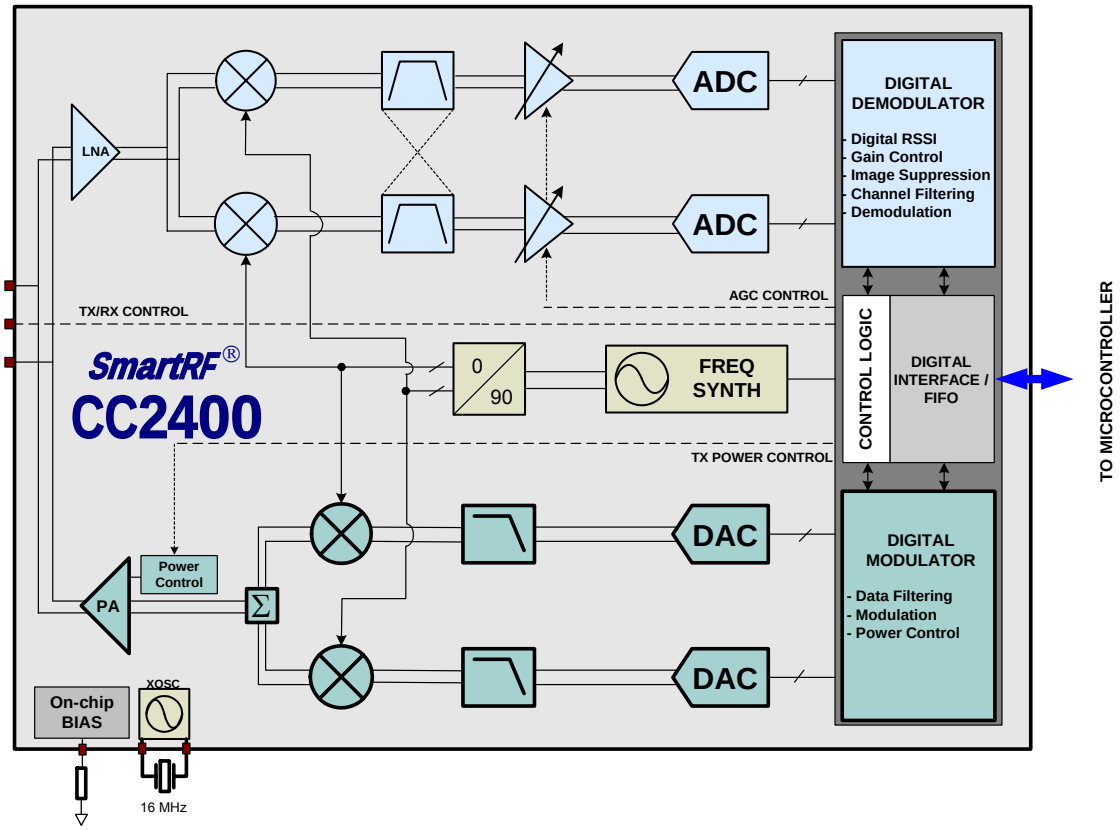


Figure 2. *CC2400* simplified block diagram

A simplified block diagram of ***CC2400*** is shown in Figure 2.

CC2400 features a low-IF receiver. The received RF signal is amplified by the low-noise amplifier (LNA) and down-converted in quadrature (I and Q) to the intermediate frequency (IF). At IF (1 MHz), the I/Q signal is filtered and amplified, and then digitized by the ADCs. Automatic gain control, final channel filtering, demodulation and bit synchronization is performed digitally.

CC2400 outputs (in un-buffered mode only) the digital demodulated data on the DIO pin. A synchronized data clock is then available at the DCLK pin. In buffered mode the demodulated data is sent to a FIFO and is accessible through the SPI interface. RSSI is available in digital format and can be read via the serial interface. The RSSI also features a programmable carrier sense indicator with output on either GIO1 or GIO6.

In transmit mode the baseband signal is directly up-converted quadrature (I and Q) and then fed to the power amplifier (PA).

The TX IF signal is frequency shift keyed (FSK). Optionally Gaussian filtering can be used enabling GFSK. The BT of the Gaussian filter is 0.5 for a datarate of 1 Mbps.

The internal T/R switch circuitry simplifies the antenna interface and matching. The antenna connection is differential. The biasing of the PA and LNA is done by connecting TXRX_SWITCH to RF_P and RF_N through an external DC path.

The frequency synthesizer includes a completely on-chip LC VCO and a 90 degrees phase splitter for generating the

LO_I and LO_Q signals to the down-conversion mixers in receive mode and up-conversion mixers in transmit mode. The VCO operates in the frequency range 4800 – 4966 MHz, and the frequency is divided by two when split in I and Q.

A crystal must be connected to XOSC16_Q1 and XOSC16_Q2 and generates the reference frequency for the synthesizer. A PLL lock signal is available via the GIO pins.

The digital baseband includes support for packet handling and data buffering.

The 4-wire SPI serial interface is used for configuration (and data interface in buffered mode). A few digital I/O lines can be configured for use with packet handling strobe and interrupt signals.

16 Application Circuit

Few external components are required for the operation of ***CC2400***. A typical application circuit is shown in Figure 3. A description of the external components referring to Figure 3 are described in Table 10. The bill of materials (BOM) is given in Table 11.

Good PCB layout is vital for proper operation, please see the section on PCB Layout Recommendations on page 56 for more details.

16.1 Input / output matching

The RF input/output is high impedance and differential. The optimum differential load for the RF port is listed on page 8.

When using an unbalanced antenna like a monopole, a balun should be used in order to get optimum performance. The balun can be implemented using low-cost discrete inductors and capacitors. The balun consists of C61, C62, C71, C81, L61, L62 and L72, and will match the RF input/output to 50 Ω, see Figure 3. L61 and L62 also provide DC biasing of the LNA/PA input/output. L71 is used to isolate the TXRX_SWITCH pin. An internal T/R switch circuit is used to switch between the LNA and the PA. See "Input/output matching" on page 50 for more details.

If a balanced antenna, like a folded dipole, is used, the balun can be omitted. If the antenna also provides a DC path from the TXRX_SWITCH pin to the RF pins, inductors are not needed for DC biasing. The L71 isolation inductor should still be used to avoid antenna reflections. Figure 4 shows a typical application circuit with differential antenna. The dipole has a virtual ground point, hence bias is provided without degradation in antenna performance. Please note that a differential antenna is generally larger than an equivalent single-ended antenna.

16.2 Bias resistor

The bias resistor R451 is used to set an accurate bias current for the chip.

16.3 Crystal

An external crystal with input and output loading capacitors (C421 and C431) is used for the crystal oscillator. See page 49 for details.

16.4 Digital I/O

The supply voltage for the digital I/O must match the interfacing microcontroller. The digital I/Os of ***CC2400*** can interface microcontrollers with supply voltages in the range 1.6 – 3.6 V.

16.5 Power supply decoupling and filtering

Proper power supply decoupling must be used for optimum performance. The placement and size of the decoupling capacitors and the power supply filtering are very important to achieve the best performance in an application. Chipcon provides a compact reference design that should be followed very closely.

16.6 Power supply switching

As described in a note in the Absolute Maximum Ratings section, the voltage supply to the chip core should not be switched off separately from the I/O supply voltage.

If it is necessary to switch the core power supply off, for instance to save the power dissipated in the 1.8V regulator, the I/O supply should be turned off as well. This can be done quite easily by running the I/O supply from a microcontroller I/O pin. Current drawn on the I/O supply is just a few milliamps, so an ordinary I/O pin should have no problems in sourcing this current. Power sequencing should be performed so that both supplies are turned on and off simultaneously.

Ref	Description
C71	Front-end bias decoupling and match, see page 50
C61	Discrete balun and match, see page 50
C81	Discrete balun and match, see page 50
C62	DC block to antenna and match
C421	16MHz crystal load capacitor, see page 49
C431	16MHz crystal load capacitor, see page 49
L61	DC bias and match, see page 50
L62	DC bias and match, see page 50
L71	RF blocking inductor, see page 50
L81	Discrete balun and match, see page 50
R451	Precision resistor for current reference generator
XTAL	16MHz crystal, see page 49

Table 10. Overview and description of external components for an unbalanced antenna (balun implemented with low cost discrete components)

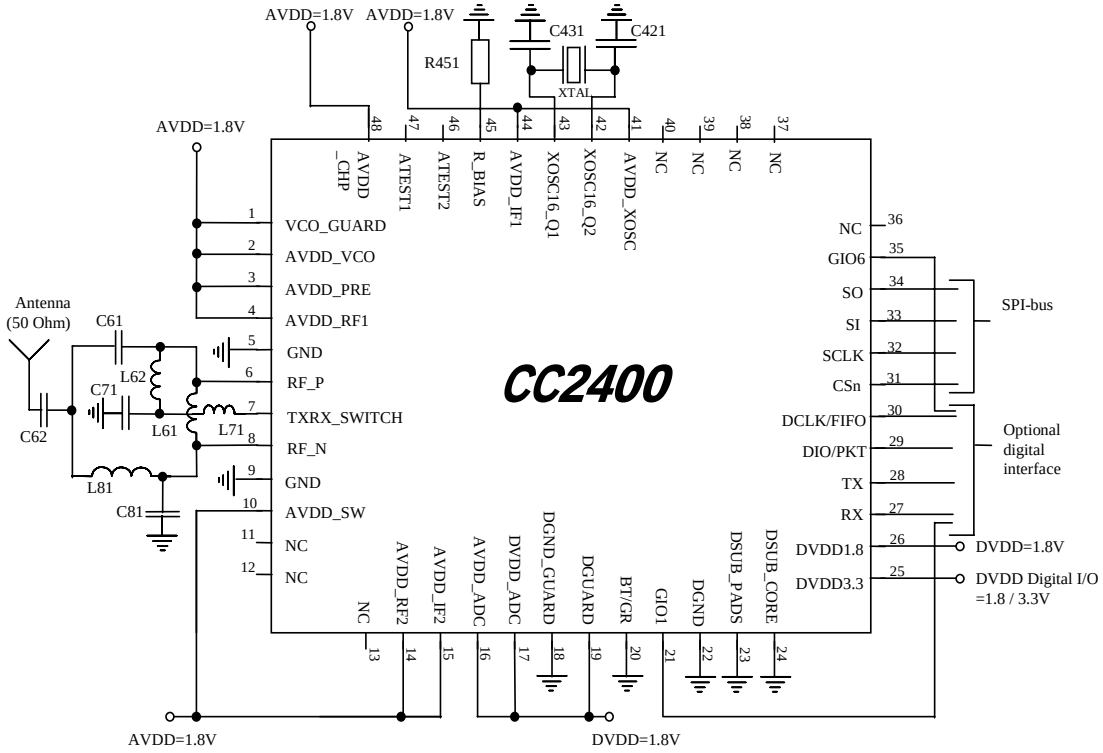


Figure 3 Typical application circuit with discrete balun for interfacing single-ended antenna

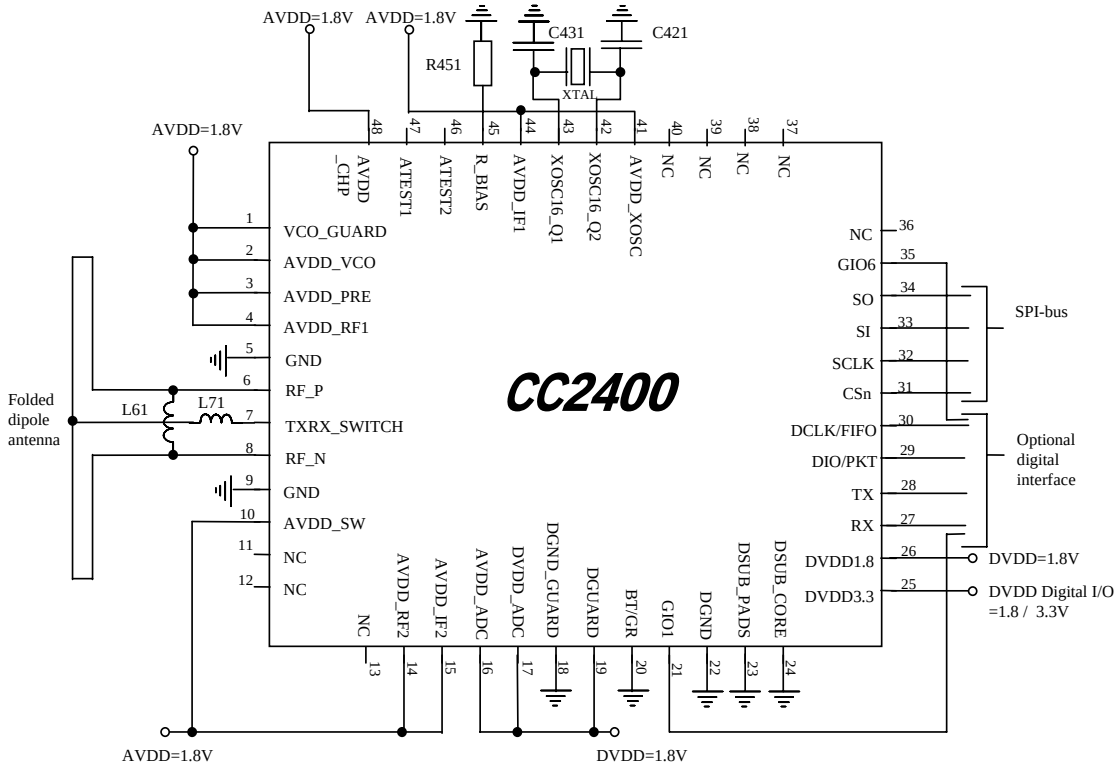


Figure 4 Typical application circuit with differential antenna (folded dipole)

Item	Single ended output, discrete balun	Differential antenna
C62	5.6 pF, +/- 0.25pF, NP0, 0402	Not used
C61	0.5 pF, +/- 0.25pF, NP0, 0402	Not used
C81	0.5 pF, +/- 0.25pF, NP0, 0402	Not used
C71	100 nF, 10%, X5R, 0402	100 nF, 10%, X5R, 0402
C421	18 pF, 5%, NP0, 0402	18 pF, 5%, NP0, 0402
C431	18 pF, 5%, NP0, 0402	18 pF, 5%, NP0, 0402
L61	7.5 nH, 5%, Monolithic/multilayer, 0402	27 nH, 5%, Monolithic/multilayer, 0402
L62	5.6 nH, 5%, Monolithic/multilayer, 0402	Not used
L71	27 nH, 5%, Monolithic/multilayer, 0402	27 nH, 5%, Monolithic/multilayer, 0402
L81	7.5 nH, 5%, Monolithic/multilayer, 0402	Not used
R451	43 kΩ, 1%, 0402	43 kΩ, 1%, 0402
XTAL	16 MHz crystal, 16 pF load (C_L)	16 MHz crystal, 16 pF load (C_L)

NOTE: Decoupling components are not included.

Table 11. Bill of materials for the application circuits

17 Configuration Overview

CC2400 can be configured to achieve optimum performance for different applications. Through the programmable configuration registers the following key parameters can be programmed:

- Receive / transmit mode
- RF frequency
- RF output power
- FSK frequency deviation
- Power-down / power-up mode
- Crystal oscillator power-up / power down
- Data rate and line coding (NRZ, 8B/10B coding)
- Synthesizer lock indicator mode
- Digital RSSI
- FSK / GFSK modulation
- Data buffering
- Packet handling hardware support

18 Configuration Software

Chipcon provides users of ***CC2400*** with a software program, SmartRF® Studio (Windows interface) that generates all necessary ***CC2400*** configuration data, based on the user's selections of various parameters. These hexadecimal numbers will then be the necessary input to the microcontroller for the configuration of ***CC2400***.

Figure 5 shows the user interface of the ***CC2400*** configuration software.

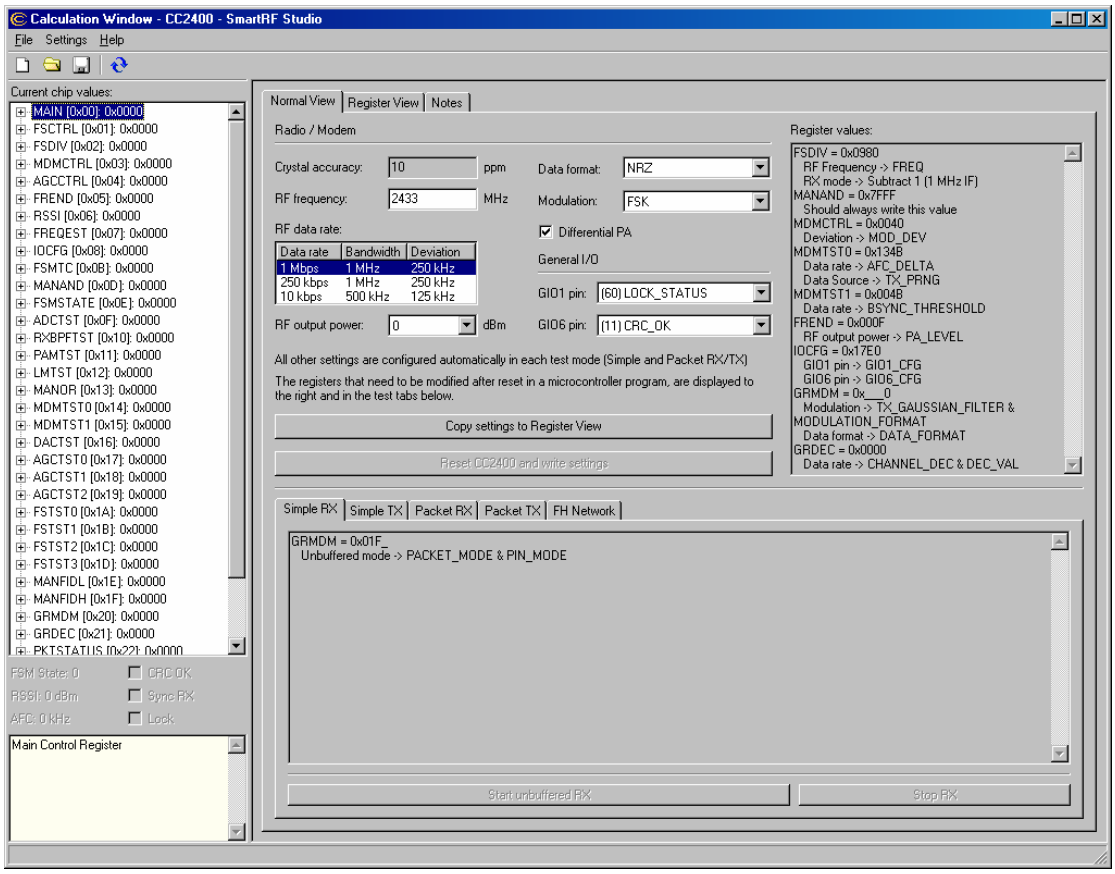


Figure 5. SmartRF® Studio user interface

19 4-wire Serial Configuration Interface

CC2400 is configured via a simple 4-wire SPI-compatible interface (SI, SO, SCLK and CSn) where ***CC2400*** is the slave. This interface is also used as data interface in buffered mode (see page 27).

There are 44 16-bit configuration registers, 9 Command Strobe Registers, and one register to access the FIFO. Each register has a 7-bit address. The FIFO (32 bytes) is 8 bits wide. A Read/Write bit indicates a read or a write operation and forms the 8-bit address field together with the 7-bit address.

Some registers are termed Command Strobe Registers. By addressing a Command Strobe register internal sequences will be started. These commands can be used to quickly change from RX mode to TX mode, for example.

A full configuration of ***CC2400*** requires sending 44 data frames of 24 bits each (7 address bits, R/W bit and 16 data bits). The time needed for a full configuration depend on the SCLK frequency. With a SCLK frequency of 20 MHz the full configuration is done in less than 5 μs. Setting the device in power down mode requires addressing one command strobe register only, and will in this case take less than 0.4 μs. All registers except the strobe registers are also readable.

In each write-cycle, 24 bits are sent on the SI-line. The bit to be sent first is the R/W bit (0 for write, 1 for read). The next seven bits are the address-bits (*A6:0)*. *A6* is the MSB (Most Significant Bit) of the address and is sent first. The 16 data-bits are then transferred (*D15:0*). During address and data transfer the CSn (Chip Select, active low) must be kept low. See Figure 6.

The timing for the programming is shown in Figure 6 with reference to Table 12. The clocking of the data on SI into the ***CC2400*** is performed on the positive edge of SCLK.

The data word is loaded into the internal configuration register, when the last bit, *D0*, of the 16 data bits has been written.

The configuration data will be retained during a programmed power-down mode, but not when the power-supply is turned off. The registers can be programmed in any order.

The configuration registers can also be read by the microcontroller via the same configuration interface. The R/W bit must be set high to initiate the data read-back, then the seven address bits are sent. ***CC2400*** then returns the data from the addressed register. SO is used as the data output and must be configured as an input by the microcontroller.

The command strobe register is accessed in the same way as for a write operation, but no data is transferred. That is, only the R/W bit and the seven address bits are written before CSn should be set high.

Figure 7 shows a summary of read and write operations. A register read/write can be terminated after one byte if only the most significant byte is required. A register can also be accessed repeatedly without writing the address again. The buffer FIFO (8 bit wide, 32 bytes) can be written continuously by simply writing new bytes over and over. The internal data pointer is then updated for every written byte. The session is terminated when the CSn is set high.

Please note that a longer hold time, t_{ps}, is needed before setting CSn high when accessing the FIFO in buffered mode.

During the transfer of the address, the ***CC2400*** returns a status byte on the SO line containing some important flags. This is shown in Table 13.

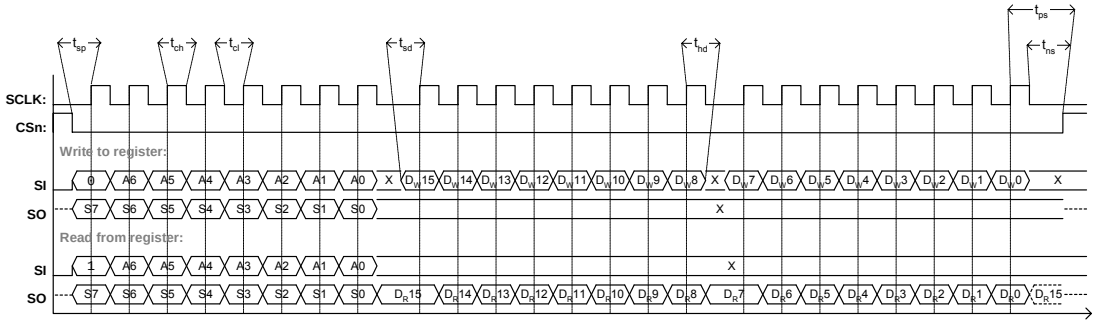


Figure 6. SPI timing diagram

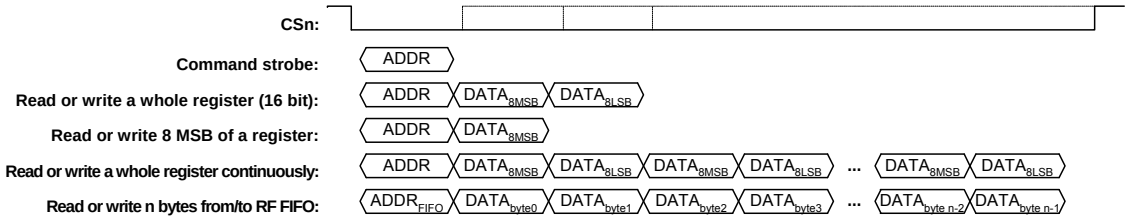


Figure 7. Configuration registers write and read operations via SPI

Parameter	Symbol	Min	Max	Units	Conditions
SCLK, clock frequency	f_{SCLK}		20	MHz	
SCLK low pulse duration	$t_{cl,min}$	25		ns	The minimum time SCLK must be low.
SCLK high pulse duration	$t_{ch,min}$	25		ns	The minimum time SCLK must be high.
CSn setup time	t_{sp}	25		ns	The minimum time CSn must be low before *positive* edge of SCLK.
CSn hold time 1	t_{ns}	25		ns	The minimum time CSn must be held low after the last *negative* edge of SCLK.
CSn hold time 2	t_{ps}	300		ns	In buffered mode: The minimum time CSn must be held low after the last *positive* edge of SCLK. This only applies to FIFO accesses.
SI setup time	t_{sd}	25		ns	The minimum time data on SI must be ready before the *positive* edge of SCLK.
SI hold time	t_{hd}	25		ns	The minimum time data must be held at SI, after the *positive* edge of SCLK.
Rise time	t_{rise}		100	ns	The maximum rise time for SCLK and CSN
Fall time	t_{fall}		100	ns	The maximum fall time for SCLK and CSn

Note: The set-up- and hold-times refer to 50% of VDD.

Table 12. SPI timing specification

Bit #	Name	Description
7	-	Reserved, ignore value
6	XOSC16M_STABLE	Indicates whether the 16 MHz oscillator is running ('1') or not
5	RESERVED	Reserved
4	SYNC_RECEIVED	Indicates whether a sync word has been received or not so far in the RX operation
3	CRC_OK	Indicates whether the next two bytes in the FIFO will make the CRC calculation successful or not: 0: CRC not OK or CRC off 1: CRC OK
2	FS_LOCK	Indicates whether the frequency synthesiser is in lock ('1') or not.
1:0	RESERVED[1:0]	Reserved

Table 13. Status byte returned during address transfer

20 Overview of Configurations and Hardware Support

The ***CC2400*** can be configured for different data interfaces, coding schemes and packet handling hardware support.

Table 14 below gives a summary of the possibilities.

Data interface	Data coding	Packet handling support
Buffered (32 byte FIFO accessed through the SPI interface)	NRZ	TX: • Preamble generation • Sync word insertion • CRC computation and insertion RX: • Sync Word detection • CRC computation and check
	8/10 code	
	Manchester	
Un-buffered (DIO and DCLK synchronous interface)	NRZ	RX: • Sync Word detection
	Manchester	

Table 14. Configurations and hardware support

21 Microcontroller Interface and Pin Configuration

Used in a typical system, ***CC2400*** will interface to a microcontroller. This microcontroller must be able to:

- Program ***CC2400*** into different modes and read back status information via the 4-wire SPI-bus configuration interface (SI, SO, SCLK and CSn). In buffered mode the data signal is also transmitted through the SPI-bus
- Interface to the bi-directional synchronous data signal interface (DIO and DCLK) if un-buffered data transmission is to be used
- Optionally interface to the general control and status pins (RX, TX, FIFO, PKT, GIO1 and GIO6) if the hardware supported packet handling functions are to be used
- Optionally the microcontroller can monitor the general I/O pins (GIO1, GIO6) for frequency lock status, carrier sense status, or other status information
- Optionally, the microcontroller can read back digital RSSI value and other status information via the 4-wire SPI interface

21.1 Configuration interface

The microcontroller interface is shown in Figure 8. The microcontroller uses a minimum of 4 I/O pins for the SPI configuration interface (SI, SO, SCLK and CSn). All other pins are optional. SO should be connected to an input at the microcontroller. SI, SCLK and CSn must be microcontroller outputs.

The microcontroller pins connected to SI, SO and SCLK can be shared with other SPI-interface devices. SO is a high impedance output as long as CSn is not activated (active low).

CSn should have an external pull-up resistor or be set to a high level during power down mode in order to prevent the input from floating. SI and SCLK should be set to a defined level to prevent the input from floating.

21.2 Signal interface in un-buffered mode

A bi-directional pin (DIO) is used for data to be transmitted and received. DCLK providing the data timing should be connected to a microcontroller input.

The data is clocked in/out at the positive edge of DCLK.

21.3 General control and status pins

Optionally, in buffered mode, the FIFO pin can be used to interrupt the microcontroller at full/empty FIFO. This pin should then be connected to a microcontroller interrupt pin.

Optionally, using the packet handling support, the PKT pin can be used in buffered mode to interrupt the microcontroller when a sync word is detected (RX mode) and packet is transmitted (TX mode). This pin should then be connected to a microcontroller interrupt pin.

The polarity of FIFO and PKT can be controlled by the INT register (address 0x23).

Optionally, the RX and TX pins can be used to change the operating mode of ***CC2400*** as an alternative to using the SPI interface strobe commands. These pins should then be connected to microcontroller output pins. If the RX and TX pins are not used, they should be grounded in order to prevent accidental change of mode.

Optionally, the GIO1 and GIO6 can be used to monitor several status signals as selected by the `IOCFG` register. The GIO6 pin should be connected to a microcontroller input pin. See Table 18 for available signals.

Table 15 gives a summary of the possible pin configurations in the different operation modes.

Pin name	SCLK	SI	SO	CSn	DIO/ PKT	DCLK/ FIFO	RX	TX	GIO1*	GIO6*
Pin number	32	33	34	31	29	30	27	28	21	35
Direction	I	I	O	I	I/O	O	I	I	O	O
Buffered mode	SCLK	SI	SO	CSn	-	FIFO	(RX)	(TX)	(GIO1)	(GIO6)
Buffered mode with Packet handling	SCLK	SI	SO	CSn	PKT	FIFO	(RX)	(TX)	(GIO1)	(GIO6)
Un-buffered mode	SCLK	SI	SO	CSn	DIO	DCLK	(RX)	(TX)	(GIO1)	(GIO6)

NOTE: Pin functions in parentheses are optional

* The use of GIO1 and GIO6 are selected in register `IOCFG` (address 0x08)

Table 15. Pin configuration

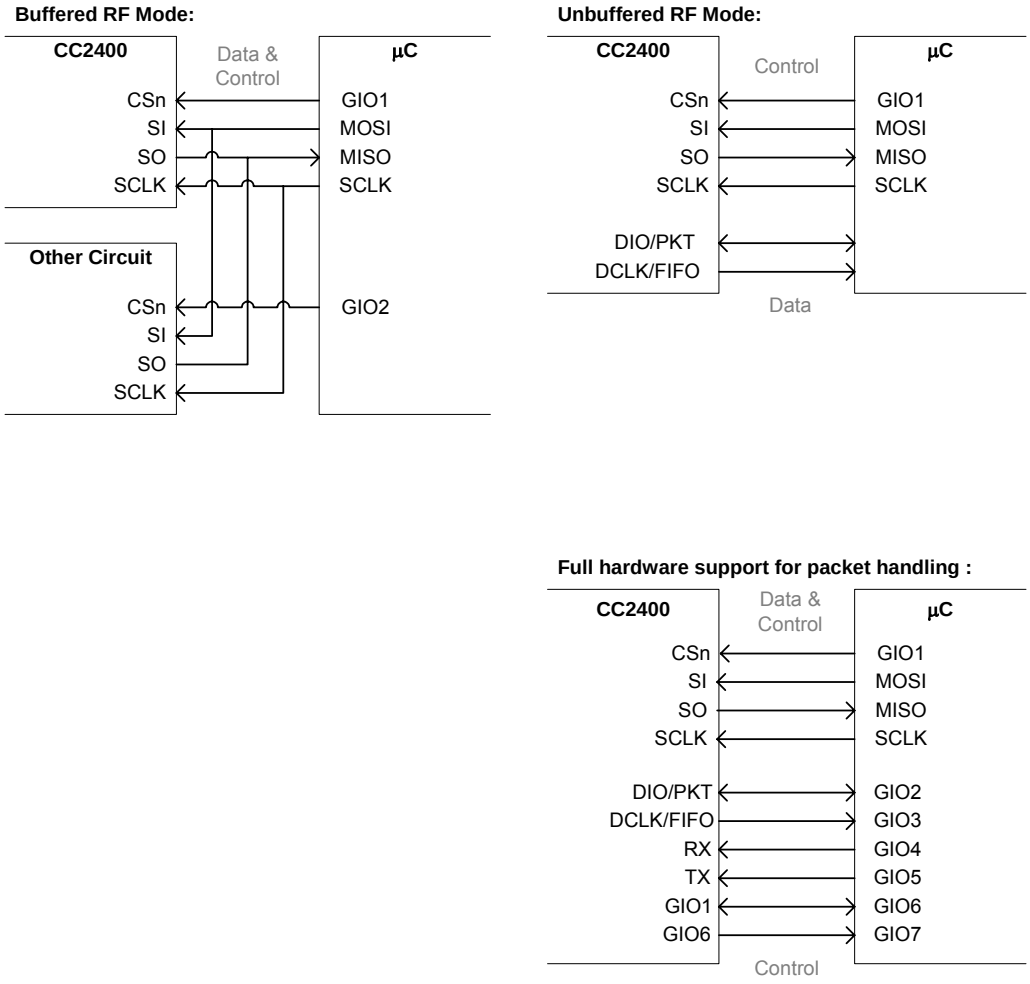


Figure 8. Microcontroller interface

22 Data Buffering

The ***CC2400*** can be used with a buffered or un-buffered data interface. The data buffering mode is controlled by the GRMDM.PIN_MODE[1:0] bits (register address 0x20).

In un-buffered mode a synchronous data clock is provided by ***CC2400*** at the DCLK pin, and the DIO pin is used as data input/output (see Figure 8).

22.1 Buffered mode

In the buffered mode a 32-byte First-in First-Out (FIFO) register block is used for data to be transmitted and data received. The FIFO is accessed through the FIFOREG register (address 0x70) using the SPI interface. Multiple bytes can be written to the FIFO without repeating the address if the CSn line is held low.

The crystal oscillator must be running when accessing the FIFO.

By using the FIFO buffer the data can be transmitted in bursts. The buffered mode will therefore offload the host controller keeping the SPI data rate much lower than the data rate on the air. This gives also a great advantage in reducing the current consumption as the transmitter and receiver are enabled only in short periods. It also allows the SPI to operate faster than the data rate, providing more time for the MCU to work between data transfers.

More than 32 bytes can be received if the FIFO is read during reception. In the same way more than 32 bytes can be transmitted if new data is written into the FIFO during transmission. Figure 9 shows the ways the FIFO can be used during transmission.

22.2 Buffered mode hardware support

In the buffered mode the FIFO pin can be used as an interrupt output to assist the microcontroller in supervising the FIFO.

The FIFO pin can be programmed to give an interrupt when the FIFO is nearly empty in TX mode, and nearly full in RX mode. The threshold (FIFO_THRESHOLD) is set in INT.FIFO_THRESHOLD[4:0].

In receive mode there will be an interrupt when the number of received bytes in the FIFO reaches FIFO_THRESHOLD. The default value is 30, giving an interrupt when 30 bytes are received. If the FIFO becomes full (32 bytes) before it is read, the reception will be terminated (goes to the FS_ON state).

In transmit mode there will be an interrupt when the number of bytes left in the FIFO reaches 32 - FIFO_THRESHOLD. For the default value this will happen when there are 2 bytes left. The transmission is terminated when the FIFO runs empty (goes to the FS_ON state). Note that in order for the FIFO pin to give an interrupt in transmit mode the number of bytes must first exceed 32 - FIFO_THRESHOLD.

The FIFO pin activity is illustrated in Figure 10.

The INT.FIFO_POLARITY bit sets the polarity of the interrupt signal.

In TX mode, the FIFO pin goes low when a transmission starts and the preamble is sent. It will stay low as long as the FIFO is empty. When data is written to the FIFO, it will go high. If the number of bytes in the FIFO goes below the FIFO_THRESHOLD, the FIFO pin will go low again. If the FIFO pin goes low, it will stay low until the CRC has been transmitted.

FIFO_FULL and FIFO_EMPTY signals are available on the general-purpose I/O pins. These two signals are affected by FIFO_THRESHOLD.

In transmit mode, FIFO_EMPTY is low if the number of bytes in the FIFO is more than 32-FIFO_THRESHOLD. In receive mode, FIFO_EMPTY goes low when there is more than 1 byte in the FIFO.

FIFO_FULL is high if the number of bytes in the FIFO is greater or equal to FIFO_THRESHOLD.

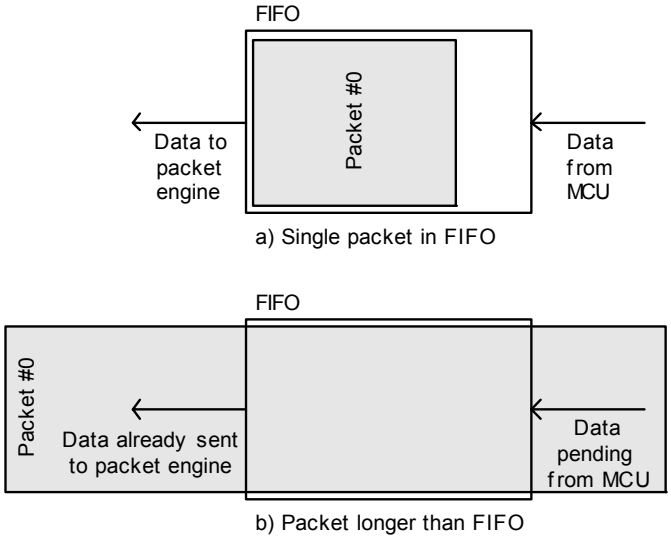


Figure 9. Ways in which the FIFO can be used during transmit mode

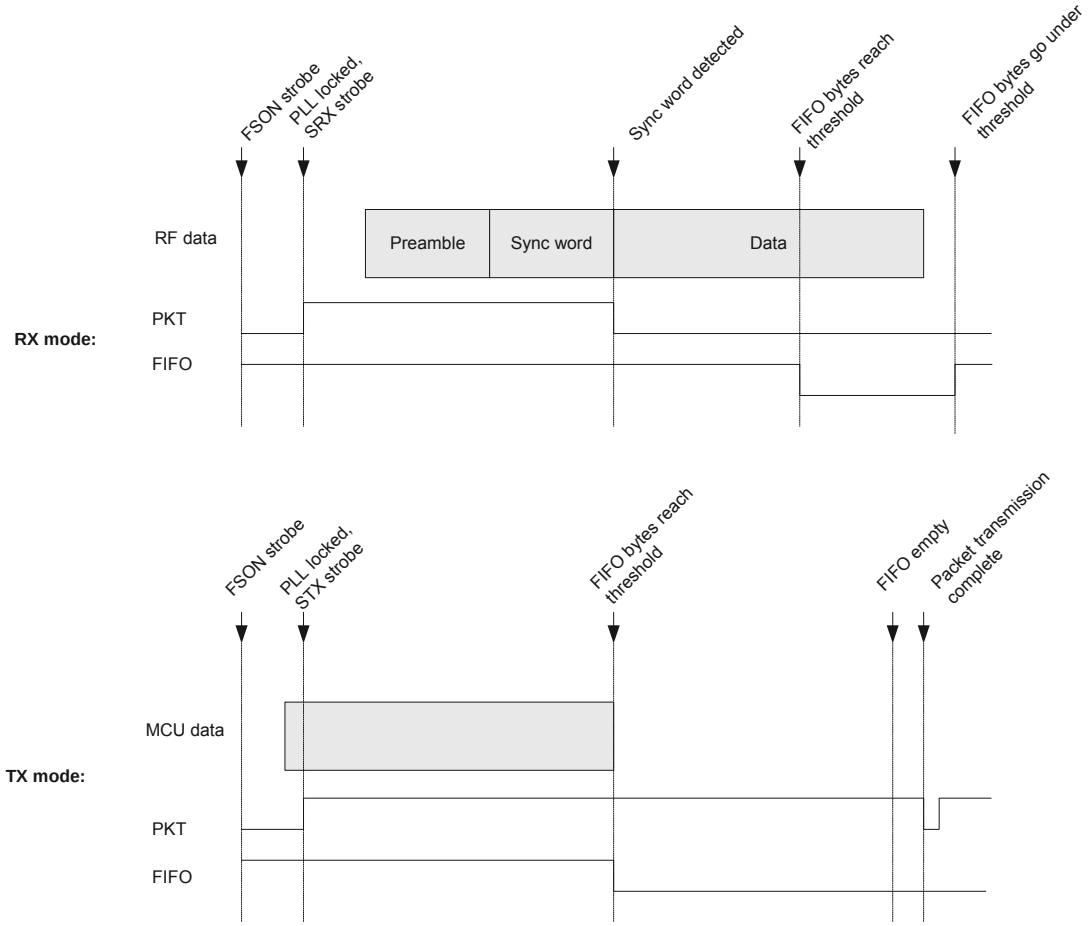


Figure 10. FIFO and PKT timing diagram

23 Packet Handling Hardware Support

The *CC2400* has built-in hardware support for packet oriented radio protocols.

The buffered mode packet handling support can in transmit mode be used to construct the data packet:

- Add a programmable number of preamble bytes
- Add a synchronization word
- Compute and add a CRC computed over the data field

In receive mode the packet handling support can be used to de-construct the data packet:

- Synchronization word detection
- Compute and check the received CRC

The packet handling support can be combined with the 8/10 line-encoding scheme. The 8/10 coding will apply to the data field (FIFO data) of the packet only (and CRC).

In un-buffered mode the synchronization word detection can be used to mute DCLK until a valid sync word is received.

23.1 Data packet format

The format of the data packet can be configured, and can consist of the following items:

- Preamble
- Synchronization word
- Data
- CRC

See Table 16 and Figure 11 for details.

The preamble pattern is '(0)101010…'. The first bit in the preamble is always the same as the first bit in the synchronization word. The length of the preamble is programmable. The default and recommended length is 4 bytes.

When using GFSK modulation at 1 Mbps, Chipcon recommends using a preamble length of 32 bytes in order to avoid a high level of bit errors. If low packet overhead is required, Chipcon recommends that FSK be used at 1 Mbps instead of GFSK.

GRMDM.PRE_BYTES[2:0]	Number of bytes (8 bits)
000	0*
001	1
010	2
011	4
100	8
101	16
110	32
111	Infinitely until TX GRMDM.PRE_BYTES [2:0] is set to 000

* Should not be used if packet reception is to be used. Use to terminate infinite transmission (111).

The length of the synchronization word is programmable as shown below.

GRMDM.SYNC_WORD_SIZE[1:0]	Number of bits
00	8
01	16
10	24
11	32

The synchronization word is programmable in the SYNCL and SYNCH registers. The default (and recommended) synchronization word length is 32 bits, which gives high immunity against false synchronization word indication. If lower immunity can be accepted, one can reduce the length to 16 bits. (However, using 8 bits will typically give too many false synchronization word indications.)

A threshold on the number of bits in error when receiving the synchronization word can be programmed in GRMDM.SYNC_ERRBITS_ALLOWED[1:0] in the range 0 – 3. (A threshold of 0 is default.)

23.2 Error detection

When the CRC is enabled it will be calculated based on the data field of the packet, i.e. not including the preamble or the synchronization word. When transmitting the packet the CRC is appended after the last data byte in the data field, i.e. when the FIFO becomes empty.

When a packet is being received the CRC is calculated as the data is read out of the

FIFO. When all data is read, the next two bytes in the FIFO are the CRC.

If the reception of the packet is error free, the PKTSTATUS.CRC_OK flag is set (also available on the GIO1 and GIO6 pins).

The CRC polynomial is:

$$x^{16} + x^{15} + x^2 + 1$$

Packet field	Preamble	Synchronisation word	Data field	CRC
Use	Mandatory	Mandatory	Mandatory	Optional
Length	≥ 1 byte	1, 2, 3 or 4 bytes	≥ 1 byte	2 bytes
GRMDM register configuration bits	PRE_BYTES[2:0]	SYNC_WORD_SIZE[1:0]		CRC_ON

Table 16. Data packet format

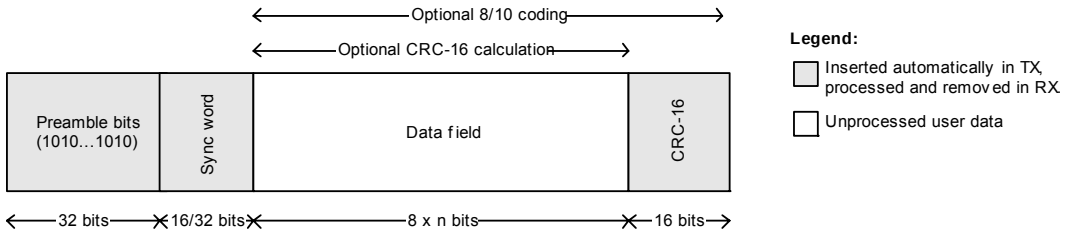


Figure 11. Packet format details (with recommended lengths of preamble and synchronization word)

23.3 Hardware interface

In the buffered mode the PKT pin can be used as an interrupt output to assist the microcontroller in supervising the transmission and reception of data packets.

The PKT pin can be programmed to give an interrupt when the synthesizer has locked and is ready to receive / transmit a data packet. Receive mode or transmit mode can then be activated.

In receive mode there will be an interrupt when the synchronization word is found. Incoming data will then be written to the FIFO.

In transmit mode there will be an interrupt when the FIFO has run empty, the two CRC bytes have been transmitted and the transmitter has been turned off.

Outside of the TX and RX modes, the PKT pin provides an indication of whether the PLL is in lock or not. For example, in the FSON state, the PKT pin will be high if the PLL is in lock.

The PKT pin activity is illustrated in Figure 10.

The polarity of the interrupt signal is set by the `INT.PKT_POLARITY` bit.

In transmit mode, the PKT pin will go low for a short while when the transmission is completely over (the CRC has been sent).

In receive mode, the PKT pin will go low when a sync word is found. It will stay low for the period of time it would take to receive 32 bytes, no matter how long the received packet is (the ***CC2400*** does not know how long incoming packets are).

24 Data / Line Encoding

The ***CC2400*** can operate with the following line-encoding formats:

- NRZ (Non-Return-to-Zero)
- Manchester coding (also known as bi-phase-level)
- 8/10 coding

The data format is controlled by the `GRMDM.DATA_FORMAT[1:0]` bits. Manchester coding and 8/10 coding reduce the effective bit rate but are in some applications used for spectral properties and error detection.

Manchester coding means coding each bit into two chips of opposite polarity. The Manchester code is based on transitions; a “0” is encoded as a low-to-high transition, a “1” is encoded as a high-to-low transition. See Figure 14. The Manchester code ensures that the signal has a constant DC component, which is necessary in some FSK demodulators. This is not required by the ***CC2400*** demodulator, but the coding option is included for compatibility reasons. The effective bit rate is half the baud rate using Manchester coding.

8/10 coding means that 8 bits are coded into 10 chips using the original IBM 8B/10B-coding scheme. The effective bit rate is 80 % of the baud rate using 8/10 coding and is therefore more efficient that the Manchester coding.

The benefit of the Manchester coding and 8/10 coding is the whitening of the transmission spectrum even when rows of equal bits are to be transmitted, improved clock recovery properties and DC balance.

Setting the `MDMTST0.INVERT_DATA` bit the data is inverted before transmission in TX mode and inverted after reception in RX mode.

24.1 Data encoding in buffered mode

In the buffered mode, using the internal FIFO, all three line-encoding schemes can be used.

The encoding/decoding takes place as the data is sent from the FIFO to the modulator, and from the demodulator to the FIFO. The line encoding is therefore invisible to the user.

If 8/10 coding is selected when using the packet mode support, it should be noted that the preamble and the sync words are not encoded.

24.2 Data encoding in un-buffered mode

When data buffering is not used, but the DIO/DCLK interface, the ***CC2400*** can be configured for two different data formats:

Synchronous NRZ mode. In transmit mode ***CC2400*** provides the data clock at DCLK, and DIO is used as data input. Data is clocked into ***CC2400*** at the rising edge of DCLK. The data is modulated at RF without encoding. In receive mode ***CC2400*** does the synchronization and provides received data clock at DCLK and data at DIO. The data should be clocked into the interfacing circuit at the rising edge of DCLK. See Figure 12.

Synchronous Manchester encoded mode. In transmit mode ***CC2400*** provides the data clock at DCLK, and DIO is used as data input. Data is clocked into ***CC2400*** at the rising edge of DCLK and should be in NRZ format. The data is modulated at RF with Manchester code. The encoding is done by ***CC2400***. In this mode the effective bit rate is half the baud rate due to the coding. This limits the maximum bit rate to 500 kbps. In receive mode ***CC2400*** does the synchronization and provides received data clock at DCLK and data at DIO. ***CC2400*** does the decoding and NRZ data is presented at DIO. The data should be clocked into the interfacing circuit at the rising edge of DCLK. See Figure 13.

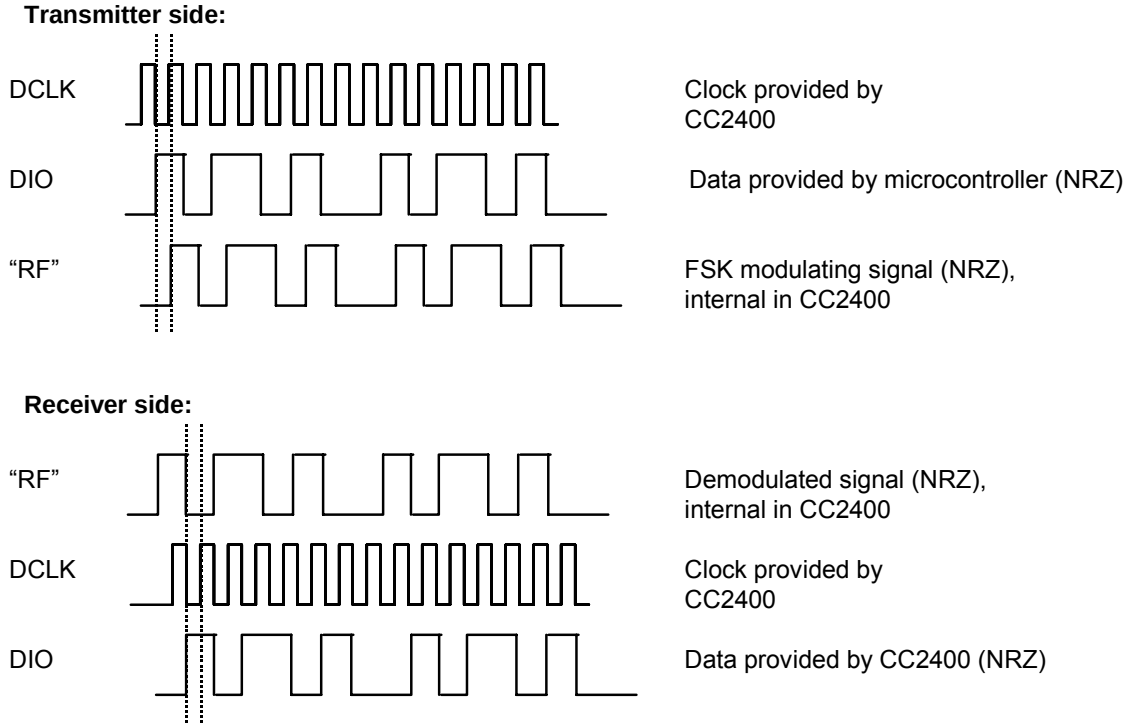


Figure 12. Synchronous NRZ mode

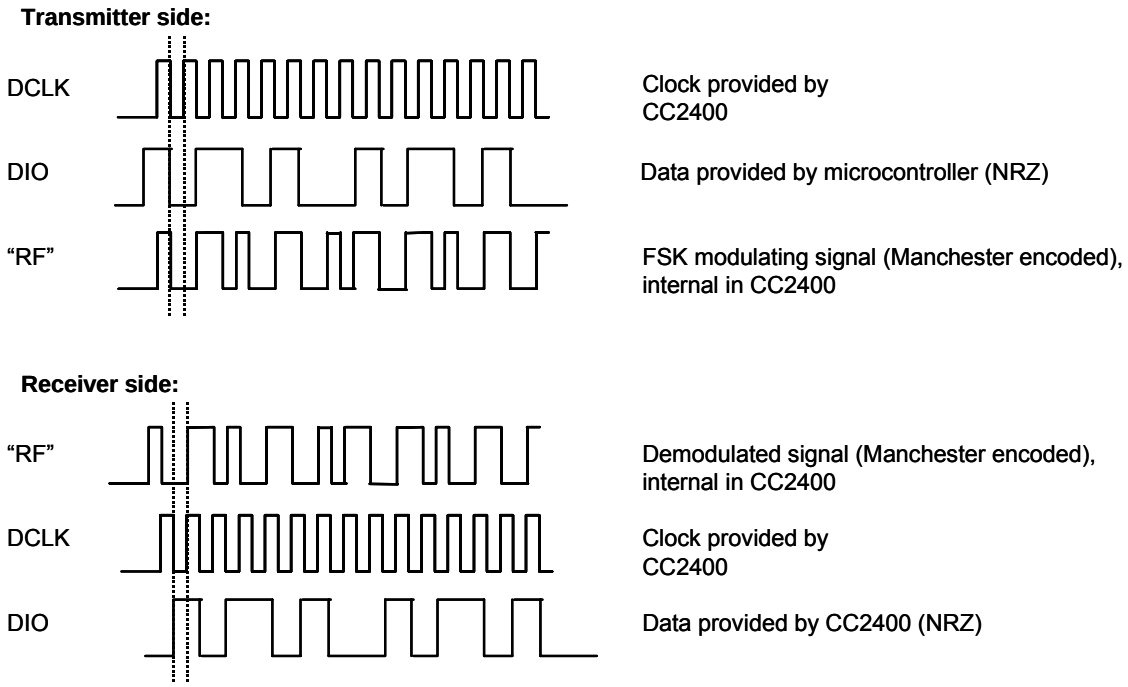


Figure 13. Synchronous Manchester encoded mode

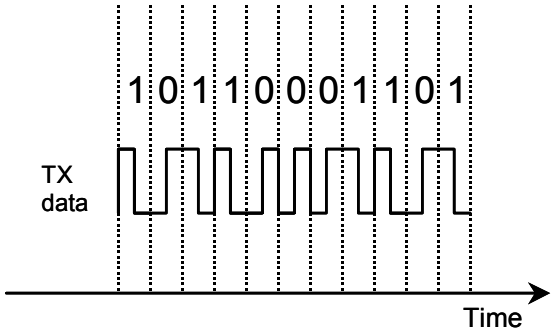


Figure 14. Manchester encoding

25 Radio control state machine

CC2400 has a built-in state machine that is used to switch between different operation states (modes). The change of state is done either by writing to command strobe registers, or using dedicated pins.

Before using the radio in either RX or TX mode, the main crystal oscillator must be turned on and become stable. The crystal oscillator has a start-up time given in Table 8, during which its output is gated internally to avoid timing problems stemming from too narrow clock pulses. The crystal oscillator is controlled by accessing the SXOSCON/SXOSCOFF command strobe registers. The XOSC16M_STABLE bit in the status register returned during address transfer indicates whether the oscillator is running and stable or not (See Table 13). This status register can be polled when waiting for the oscillator to start.

The frequency synthesizer (FS) can be started by either accessing the command strobe register SFSON or by using the RX and TX control pins. The FS will then enter its self-calibration mode. After the calibration is performed, the FS needs to lock onto the right LO frequency. The calibration and lock acquisition time is given in Table 8.

When the FS is in lock it is possible to go into RX or TX mode. That can be done either by accessing the SRX/STX command strobe registers, or by using the RX and TX control pins. It is possible to change quickly between TX and RX by way of the FS On state.

Turning off RF can be accomplished by either accessing the command strobe register SRFOFF or by using the RX and TX control pins. When using the RX and TX pins to go from the FS On to Radio Off it is important that TX is set to 0 before RX is set to 0.

The state transitions using the RX and TX pins are illustrated in Figure 15.

Note that to switch between RX and TX, the FSDIV register must be updated. This is because direct conversion is used in TX mode, while an IF frequency of 1 MHz is used in RX mode. Please see page 47 for more information about frequency programming.

Also note that the FSDIV register should only be changed when the radio is in IDLE mode, otherwise the PLL can go out of lock.

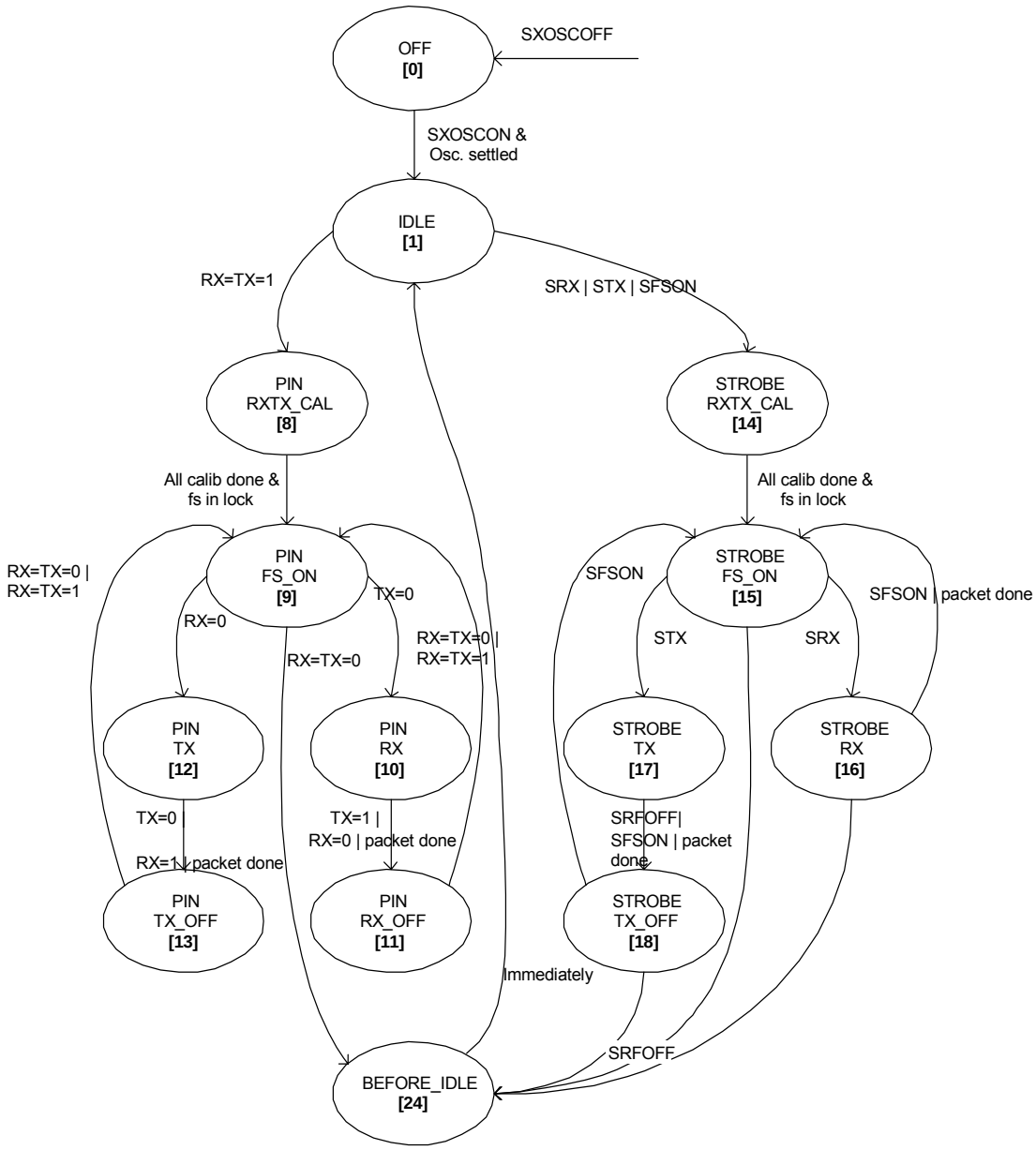


Figure 15. Radio control state diagram (`FSMSTATE.FSM_CUR_STATE[4:0]` value in brackets)

Figure 15 shows a state transition diagram for the radio control state machine. This figure shows the possibilities that exist for changing between states. Note for example that it is not possible to go from IDLE mode back to OFF. This diagram can be very useful for debugging what is happening within the ***CC2400*** by reading `FSMSTATE.FSM_CUR_STATE[4:0]`.

If invalid parameters are used during development or testing, the PLL may not lock after calibration. If this happens, the ***CC2400*** will get stuck in the STROBE_RXTX_CAL state. The chip must then be reset to exit this state. This should never happen in an actual application as long as recommended register settings are used.

Also note that the frequency register `FSDIV` should only be modified when the ***CC2400*** is in IDLE mode, otherwise the PLL may go out of lock since calibration is only performed when exiting the IDLE state

26 Power Management Flow Chart

CC2400 offers great flexibility for power management in order to meet strict power consumption requirements in battery-operated applications.

After reset the ***CC2400*** is in Power Down mode. All configuration registers can then be programmed in order to make the chip ready to operate at the correct frequency, data rate and mode. Due to the very fast start-up time, the ***CC2400*** can remain in Power Down until a transmission session is requested.

Figure 16 shows a typical power-on and initializing sequence. After this initializing sequence the chip is in Power Down mode with very low power consumption and the crystal oscillator is not running.

Figure 17 shows the sequence for entering RX or TX mode. The flow chart illustrates the simplest way to send a data packet using the strobe command registers. After one or more data packets are transmitted or received, the chip is again set to Power Down mode.

During chip initialization a few registers need to be programmed to other values than their reset values. SmartRF® Studio should be used to find/generate the required configuration data for these registers.

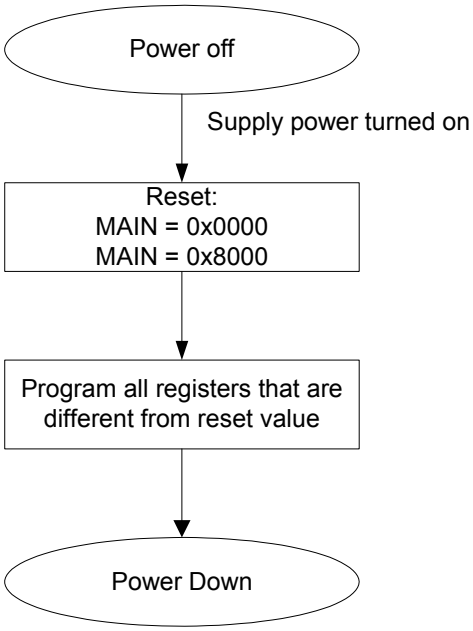


Figure 16. Initializing sequence

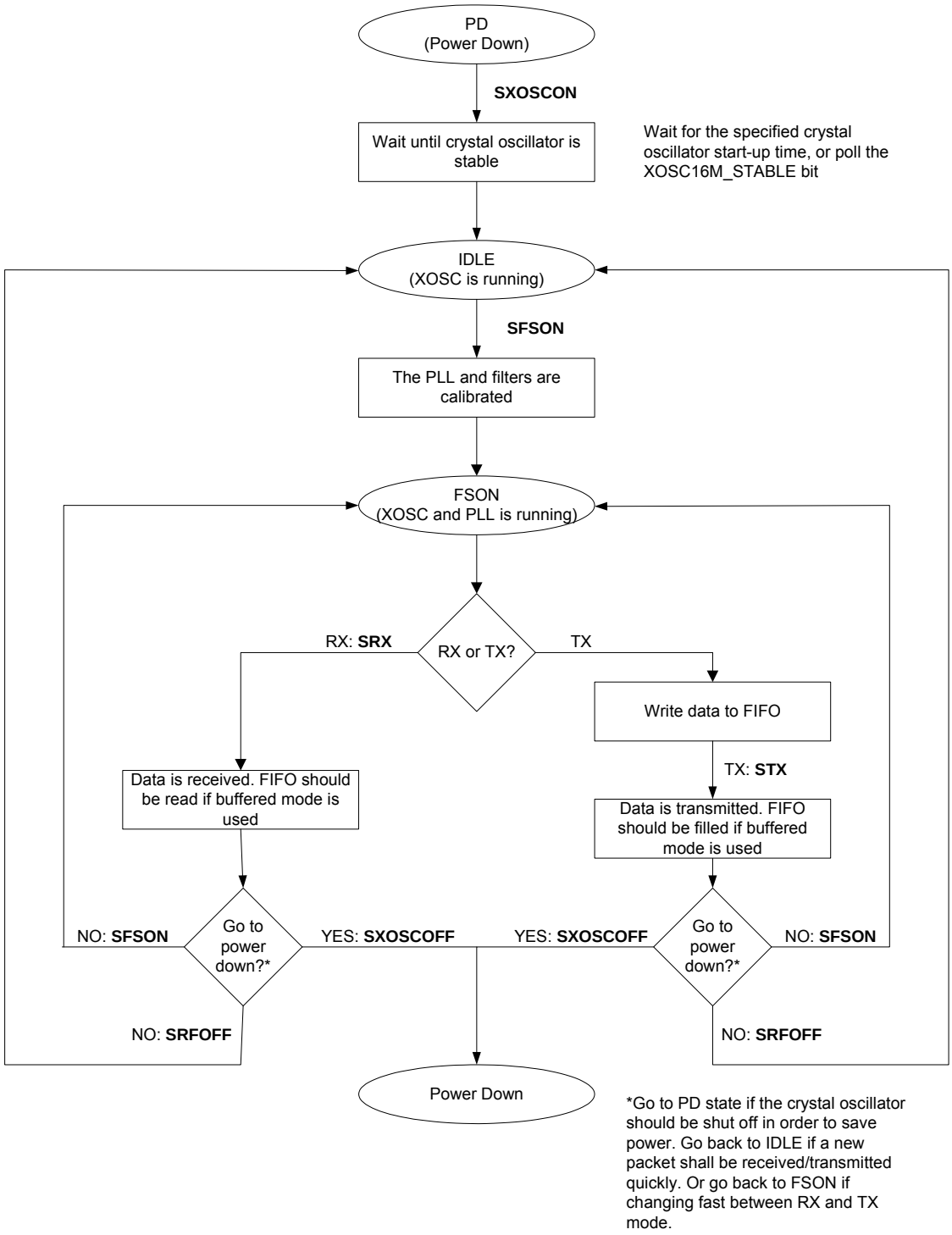


Figure 17. Sequence for activating RX or TX mode

27 FSK Modulation Formats

The data modulator can modulate 2FSK, which is two level FSK, and GFSK, which is a Gaussian filtered FSK with BT=0.5 at 1 Mbps (for lower data rates BT will be higher).

The purpose of the GFSK is to make a more bandwidth efficient system. The modulation and the Gaussian filtering is performed internally. The `GRMDM.TX_GAUSSIAN_FILTER` bit enables the GFSK.

However, if GFSK modulation is used together with a data rate of 1 Mbps, it is recommended to use a preamble length of 32 bytes as otherwise packet error performance can be affected.

Figure 18 shows a plot of the spectrum for FSK and GFSK modulation. Input data was a PN9 sequence. The plot was captured using a spectrum analyzer set to 5 MHz span and 300 kHz RBW.

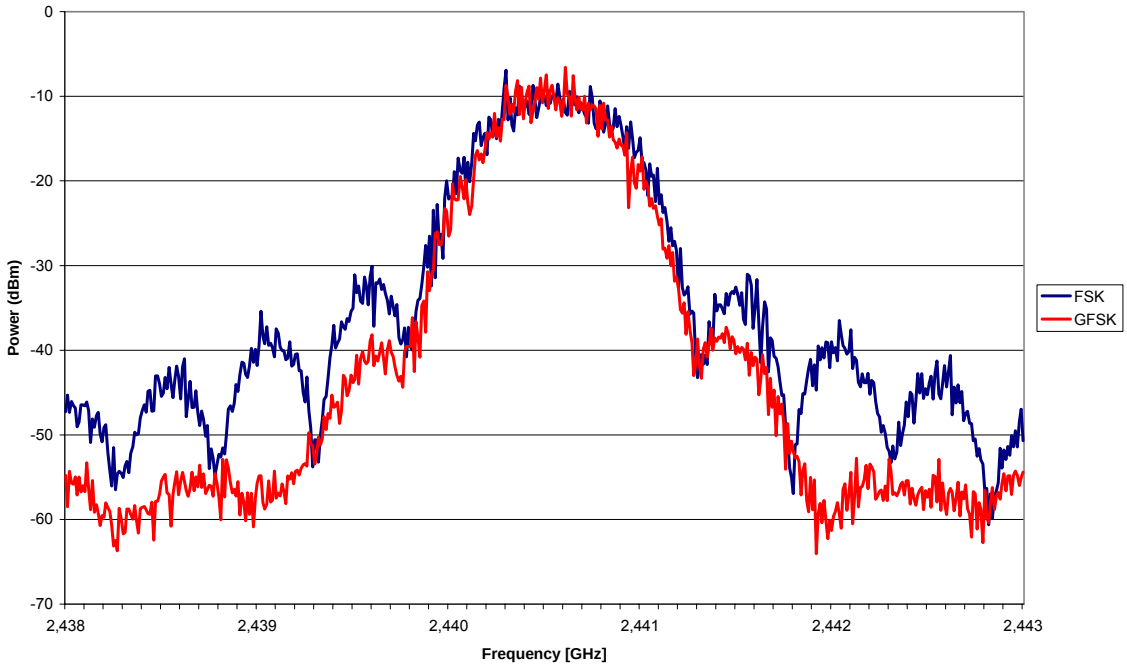


Figure 18. Modulated spectrum

28 Built-in Test Pattern Generator

The ***CC2400*** has a built-in test pattern generator that can generate a PN9 pseudo random sequence. The `MDMTST0.TX_PRNG` bit enables the PN9 generator.

The PN9 pseudo random sequence is defined by the polynomial $x^9 + x^5 + 1$.

The PN9 generator can be used for transmission of 'real-life' data when measuring modulation bandwidth or occupied bandwidth.

29 Receiver Channel Bandwidth

In order to meet different channel width and channel spacing requirements, the receiver's digital channel filter bandwidth is programmable. It can be programmed from 125 to 1000 kHz.

The `GRDEC.CHANNEL_DEC[1:0]` register bits control the bandwidth.

The table below summarizes the selectable channel bandwidths.

Channel filter bandwidth [kHz]	GRDEC.CHANNEL_DEC[1:0] [binary]
1000	00
500	01
250	10
125	11

There is a tradeoff between selectivity and accepted frequency tolerance. In applications where larger frequency drift is expected (depends on the accuracy of the crystal), the filter bandwidth should be increased, at the expense of reduced adjacent channel rejection (ACR).

It is strongly recommended to use one of the three settings for over-the-air data rates and channel bandwidths as described in the section "Data Rate Programming" on page 40.

30 Data Rate Programming

The supported over-the-air data rates are 1Mbps, 250kbps and 10kbps. The data rate is programmable via the GRDEC register.

Supported channel filter bandwidths and data rates are shown in the following table.

Figure 19 shows how sensitivity varies as a function of frequency offset between the transmitter and the receiver for various data rates. It is possible to tolerate even larger offsets by making use of the AFC feature; please see page 42 for further details.

CHANNEL_DEC [binary]	BW [kHz]	DEC_VAL [decimal]	Data rate [kbps]
00	1000	0	1000
00	1000	3	250
01	500	49	10

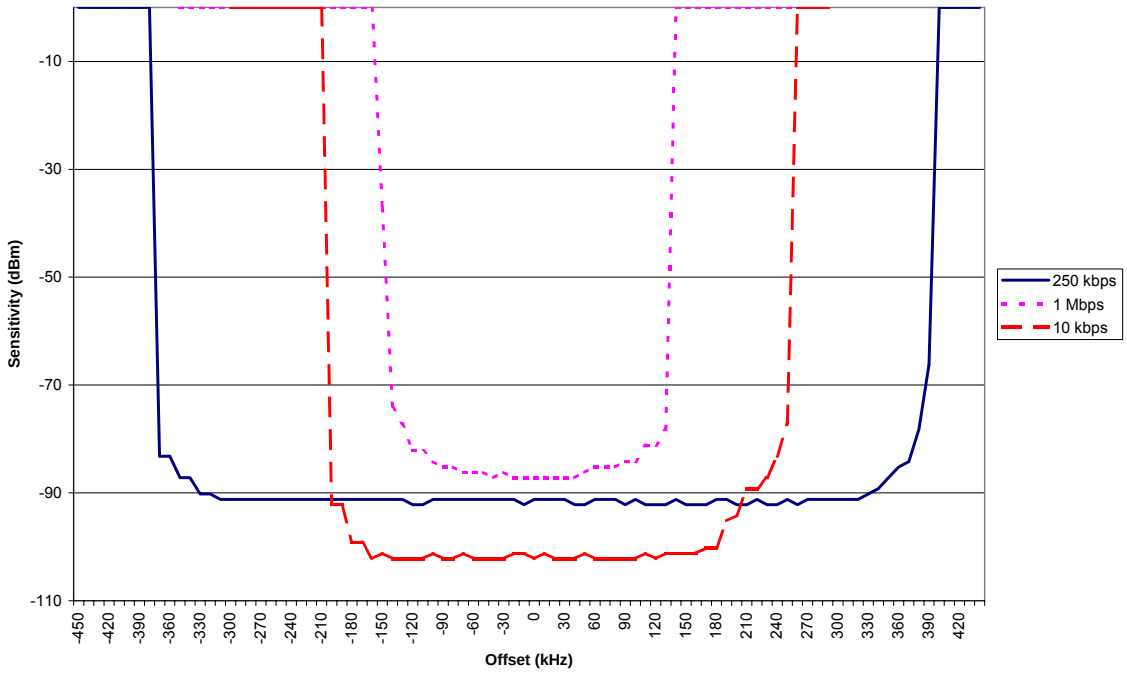


Figure 19. Sensitivity as a function of frequency offset

31 Demodulator, Bit Synchronizer and Data Decision

The block diagram for the demodulator, data slicer and bit synchronizer is shown in Figure 20. The built-in bit synchronizer extracts the data rate and performs data decision. The data decision is done using over-sampling and digital filtering of the incoming signal. This improves the reliability of the data transmission and provides a synchronous clock in the un-buffered mode. Using the buffered mode simplifies the data interface further, as data can be written and read byte-for-byte in bursts from the FIFO.

The suggested preamble is a 32 bit '(0)10101…' bit pattern, the same as used by the packet handling support, see page 29. This is necessary for the bit synchronizer to synchronize with the coding correctly.

The data slicer performs the bit decision. Ideally the two received FSK frequencies are placed symmetrically around the IF frequency. However, if there is some frequency error between the transmitter and the receiver, the bit decision level should be adjusted accordingly. In ***CC2400*** this is done automatically by measuring the two frequencies and by using the average value as the decision level.

The digital data slicer in ***CC2400*** uses an average value of the minimum and maximum frequency deviation detected as the comparison level. The `MDMTST0.AFC_DELTA` register is used to set the expected deviation of the incoming signal. Once a shift in the received frequency larger than half the expected separation is detected, a bit transition is recorded and the average value to be used by the data slicer is calculated.

The actual number of samples used to find the averaging value can be programmed and set higher for better data decision accuracy. This is controlled by the `AFC_SETTLING[1:0]` bits. If RX data is present in the channel when the RX chain is turned on, then the data slicing estimate will usually give correct results after 4 bits. The data slicing accuracy will increase after this, depending on the `AFC_SETTLING[1:0]` bits. If the start of a transmission occurs after the RX chain is turned on, the minimum number of bit transitions (or preamble bits) before correct data slicing will depend on the `AFC_SETTLING[1:0]` bits, as shown in Table 17. The recommended setting is 11b, requiring 16 data bits of preamble to fill the averaging filter completely.

The internally calculated average FSK frequency value gives a measure for the frequency offset of the receiver compared to the transmitter. The frequency offset can be read from `RSSI.RX_FREQ_OFFSET[7:0]`. This information can also be used for an automatic frequency control, as described at page 43.

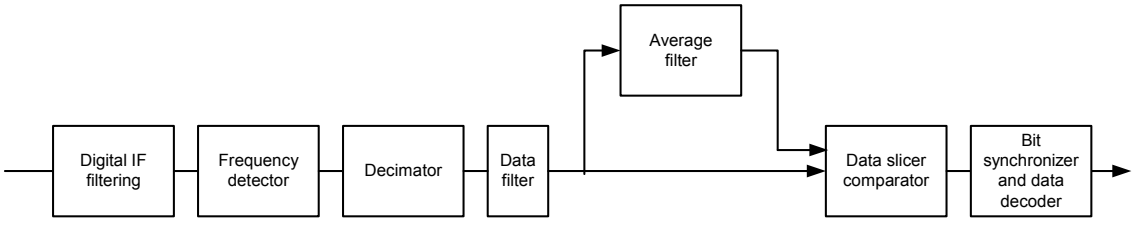


Figure 20. Demodulator block diagram

AFC settling time MDMTST0.AFC_SETTLING[1:0]	# Bits
00	2
01	4
10	8
11	16

Table 17. Minimum number of bits for the averaging filter

32 Automatic Frequency Control

CC2400 has a built-in optional feature called AFC (Automatic Frequency Control). This feature can be used to measure and compensate for frequency drift.

The average frequency offset of the received signal (from the nominal IF) can be read from the FREQEST.RX_FREQ_OFFSET[7:0] register. This is a signed (2's-complement) 8-bit value that can be used to compensate for frequency offset between an external transmitter and the receiving device. The frequency offset is given by:

$$\Delta F = \text{RX_FREQ_OFFSET} \times 5.2 \quad [\text{kHz}]$$

The receiver can be calibrated against an external transmitter (another ***CC2400*** or an external test signal) by changing the operating frequency according to the measured offset. The new frequency must be calculated by the microcontroller and written to the MDMCTRL.MOD_OFFSET[5:0] register. After this compensation the center frequency of the received signal will better match the digital channel filter bandwidth. The compensation, as described above, also automatically compensates the transmitter, i.e. the transmitted signal will match the 'external' transmitter's signal. However, compensating the transmitter signal may cause additional spurs in the TX spectrum. Chipcon therefore recommends only compensating in RX mode.

This feature reduces the requirement on the crystal accuracy, which is important when using the narrower channel bandwidths. For a further description of this feature please refer to page 53 (Crystal drift compensation).

Figure 21 shows how the value of the FREQEST.RX_FREQ_OFFSET[7:0] register varies as a function of frequency offset for different values of MDMTST0.AFC_SETTLING[1:0]. Chipcon recommends using a value of 4.

The following procedure should be followed when using the AFC to compensate for a frequency offset between transmitter and receiver:

1. Read the FREQEST.RX_FREQ_OFFSET[7:0] register. This is a signed 2's-complement value.
2. Use the equation on this page to calculate the frequency offset in kHz.
3. The microcontroller then needs to calculate the equivalent value to write to the MDMCTRL.MOD_OFFSET[5:0] register.

For example:

The value read from the FREQEST.RX_FREQ_OFFSET[7:0] register is 0xE0. This equals –32 since the register value is in signed 2's complement. This corresponds to –32 x 5.2 = -166.4 kHz.

The MOD_OFFSET register should therefore be set to –166.4 kHz / 15.625 kHz = -10.6496 ≈ -11. –11 equals 0x35 in hexadecimal.

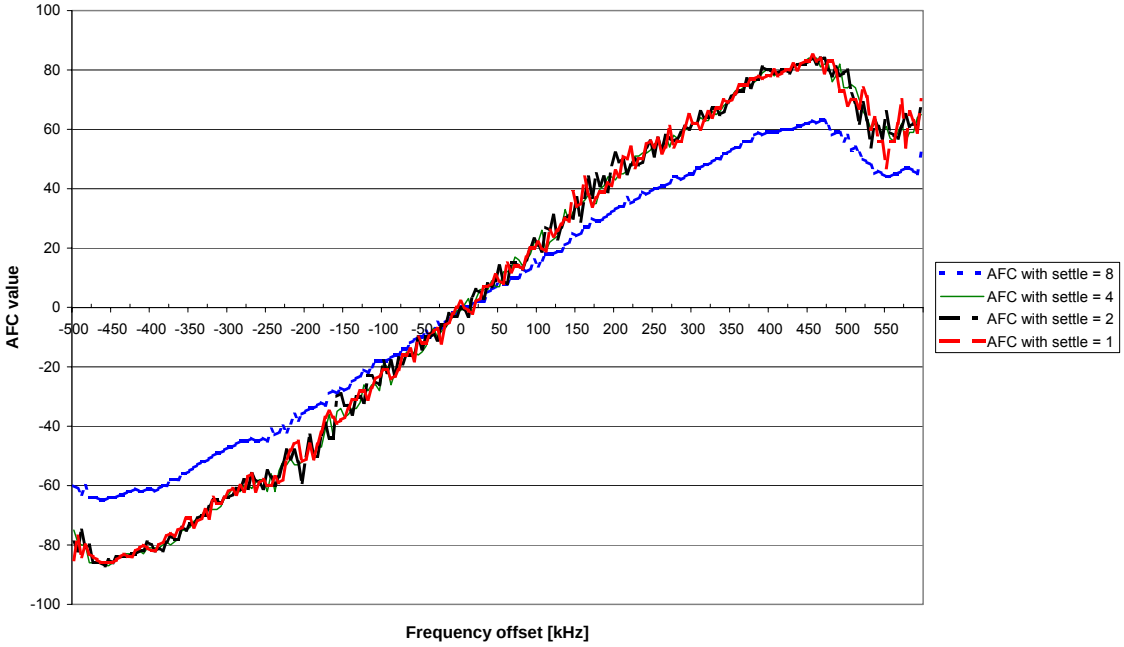


Figure 21. AFC value vs. frequency offset

33 Linear IF and AGC Settings

CC2400 is based on a linear IF chain where the signal amplification is done in an analog VGA (variable gain amplifier). The gain of the VGA is controlled by the digital part of the IF-chain after the ADC (Analog Digital Converter).

The AGC (Automatic Gain Control) loop ensures that the ADC operates inside its dynamic range by using an analog/digital feedback loop.

The AGC characteristics are set through the AGCCTRL, AGCTST0, AGCTST1 and AGCTST2 registers.

Note that the RSSI function does not take AGC settings into consideration if the AGC settings are overridden.

34 RSSI

CC2400 has a built-in RSSI (Received Signal Strength Indicator) giving a digital value that can be read form the RSSI.RSSI_VAL[7:0] register.

The RSSI reading provides a measure of the signal power entering the RF input. The scale is logarithmic, so that RSSI_VAL provides a value in dB.

The number of samples that are used to calculate the average signal amplitude is controlled by the RSSI.RSSI_FILT[1:0] register. The RSSI filter length (averaging) can be done over up to 8 symbols. This will determine the response time of the RSSI.

The RSSI measurement can be referred to the power at the RF input pins by using the following equation:

$$P = RSSI_VAL + RSSI_OFFSET \text{ [dBm]}$$

where the nominal value of RSSI_OFFSET is –54dB. (If the gain in the LNA/Mixer is changed from the default settings, the offset is changed.)

A typical plot of the RSSI_VAL reading as function of input power is shown in Figure 22 (for 1Mbps).

Note that the RSSI function does not take AGC settings into consideration if the AGC settings are overridden.

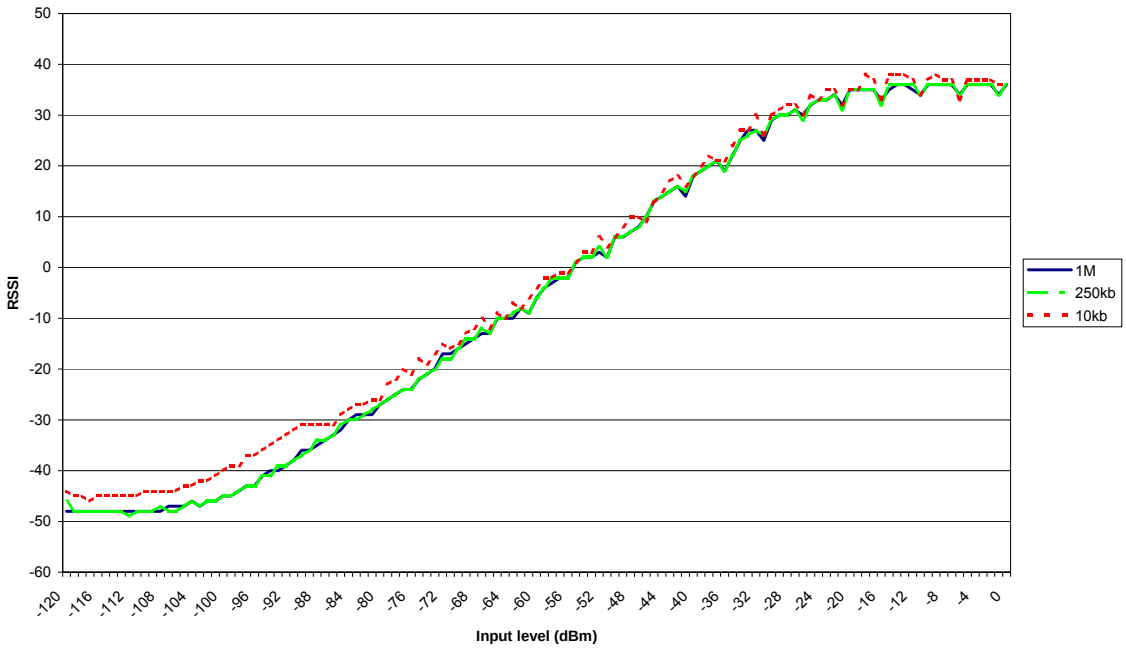


Figure 22. Typical RSSI value vs. input power

35 Carrier Sense

The carrier sense signal is based on the measured RSSI value and a programmable threshold. The carrier-sense function can be used to simplify the implementation of a CSMA (Carrier Sense Multiple Access) medium access protocol.

Carrier sense threshold level is programmed by `RSSI.RSSI_CS_THRES[5:0]`. The value of this register can be calculated in the same way as described for `RSSI.RSSI_VAL` in the previous section, except that the unit is 4 dB instead of 1 dB. The default level (0x3C) corresponds to a threshold of –70 dBm. A threshold of 0x09 corresponds to –18 dBm, and a threshold of 0x37 corresponds to –90 dBm.

The carrier sense signal can be multiplexed to the GIO1/GIO6 pin. The CARRIER_SENSE_N signal is enabled by setting `IOCFG.GIO1_CFG[5:0] = 01010B` (see Table 18).

36 Interfacing an External LNA or PA

CC2400 has two digital output pins, GIO1 and GIO6, which can be used to control an external LNA or PA. The functionality of these pins are controlled through the `IOCFG` register.

The PA_EN, PA_EN_N, RX_PD, TX_PD signals can be multiplexed to the GIO1/GIO6 pin and used for controlling the PA / LNA and one or more T/R switches.

These two pins can also be used as two general control signals, see Table 18.

For further information on attaching a PA, please see page 54.

37 General Purpose / Test Output Control Pins

The two digital output pins, GIO1 and GIO6, can be used as two general control signals by writing to `IOCFG.GIO1_CFG[5:0]` and `IOCFG.GIO6_CFG[5:0]`.

`GIO1_CFG = 61` sets the pin low, and `GIO1_CFG = 62` sets the pin high.

This feature can be used to save I/O pins on the microcontroller when the other functions associated with these pins are not used.

These two pins can also be used as a test pin to monitor a lot of internal signals. This is summarized in Table 18.

`GIO1_CFG / GIO6_CFG` **[decimal]**	**Signal**	**I/O**	**Description**
0	Reserved	O	Reserved
1	Reserved	O	Reserved
2	Reserved	O	Reserved
3	PA_EN	O	Active high PA enable signal
4	PA_EN_N	O	Active low PA enable signal
5	SYNC_RECEIVED	O	Set if a valid sync word has been received since last time RX was turned on
6	PKT	O	Packet status signal See Figure 10, page 28.
7	Reserved	I	Reserved
8	Reserved	O	Reserved
9	Reserved	O	Reserved
10	CARRIER_SENSE_N	O	Carrier sense output (RSSI above threshold)

11	CRC_OK	O	CRC check OK after last byte read from FIFO
12	AGC_EN	O	AGC enable signal
13	FS_PD	O	Frequency synthesiser power down
14	RX_PD	O	RX power down
15	TX_PD	O	TX power down
16	Reserved	O	Reserved
17	Reserved	O	Reserved
18	Reserved	O	Reserved
19	Reserved	O	Reserved
20	Reserved	O	Reserved
21	Reserved	O	Reserved
22	PKT_ACTIVE	O	Packet reception active
23	MDM_TX_DIN	O	The TX data sent to modem
24	MDM_TX_DCLK	O	The TX clock used by modem
26	MDM_RX_DOUT	O	The RX data received by modem
26	MDM_RX_DCLK	O	The RX clock recovered by modem
27	MDM_RX_BIT_RAW	O	The un-synchronized RX data received by modem
28	Reserved	O	Reserved
29	MDM_BACKEND_EN	O	The Backend enable signal used by modem in RX
30	MDM_DEC_OVRFLW	O	Modem decimation overflow
31	AGC_CHANGE	O	Signal that toggles whenever AGC changes gain.
32	VGA_RESET_N	O	The VGA peak detectors' reset signal
33	CAL_RUNNING	O	VCO calibration in progress
34	SETTLING_RUNNING	O	Stepping CHP current after calibration
35	RXBPF_CAL_RUNNING	O	RX band-pass filter calibration running
36	VCO_CAL_START	O	VCO calibration start signal
37	RXBPF_CAL_START	O	RX band-pass filter start signal
38	FIFO_EMPTY	O	FIFO empty signal
39	FIFO_FULL	O	FIFO full signal
40	CLKEN_FS_DIG	O	Clock enable Frequency Synthesiser
41	CLKEN_RXBPF_CAL	O	Clock enable RX band-pass filter calibration
42	CLKEN_GR	O	Clock enable generic radio
43	XOSC16M_STABLE	O	Indicates that the Main crystal oscillator is stable
44	XOSC_16M_EN	O	16 MHz XOSC enable signal
45	XOSC_16M	O	16 MHz XOSC output from analog part
46	CLK_16M	O	16 MHz clock from main clock tree
47	CLK_16M_MOD	O	16 MHz modulator clock tree
48	CLK_8M16M_FSDIG	O	8/16 MHz clock tree for fs_dig module
49	CLK_8M	O	8 MHz clock tree derived from XOSC_16M
50	CLK_8M_DEMOD_AGC	O	8 MHz clock tree for demodulator/AGC
51	Reserved	O	Reserved
52	Reserved	O	Reserved
53	FREF	O	Reference clock (4 MHz)
54	FPLL	O	Output clock of A/M-counter (4 MHz)
55	PD_F_COMP	O	Phase detector comparator output
56	WINDOW	O	Window signal to PD (Phase Detector)
57	LOCK_INSTANT	O	Window signal latched in PD (Phase Detector) by the FREF clock
58	RESET_N_SYSTEM	O	Chip wide reset (except registers)
59	FIFO_FLUSH	O	FIFO flush signal
60	LOCK_STATUS	O	The top-level FS in lock status signal
61	ZERO	O	Output logic zero
62	ONE	O	Output logic one
63	HIGH_Z	-	Pin set as high-impedance output

Table 18. GIO1 / GIO6 signal select table

38 Frequency Programming

The operating frequency is set by programming the frequency word in the FSDIV configuration register.

The frequency word is 12 bits and is located in FSDIV.FREQ[11:0]. Writing/reading FSDIV[11:0] will give the frequency directly in MHz. (The bits FSDIV.FREQ[11:10] are hardwired to '10' giving a fixed offset of 2048.)

FSDIV should only be modified while the ***CC2400*** is in IDLE mode. Otherwise the PLL may go out of lock as a calibration is only performed when exiting IDLE mode.

38.1 Transmit mode

In transmit mode an I/Q direct upconversion scheme is used (i.e. no intermediate frequency for the modulated baseband signal). MDMTST0.TX_1MHZ_OFFSET_N=1 must therefore be set during the chip initialization sequence (ref. Figure 16).

When MDMTST0.TX_1MHZ_OFFSET_N=1 the transmit channel center frequency (carrier frequency), f_c, in MHz is given directly by:

$$f_c = \mathrm{FREQ}[11:0] = 2048 + \mathrm{FREQ}[9:0]$$

The two FSK modulation frequencies are given by:

$$f_0 = f_c - f_{dev}$$
$$f_1 = f_c + f_{dev}$$

where f_{dev} is the FSK frequency deviation. f_{dev} is programmed with MDMCTRL.MOD_DEV[6:0] and given by (in kHz):

$$f_{dev} = \pm 3.9062 \cdot MOD_DEV[6:0]$$

The default value is MOD_DEV = 64 giving 250 kHz deviation.

The TX_GAUSSIAN_FILTER bit in the GRMDM register controls the Gaussian shaping of the modulation signal. See also page 38.

38.2 Receive mode

Low side LO injection is used, hence:

$$f_{LO} = f_{RF} - f_{IF}$$

where, f_{RF} is the center frequency of the channel and f_{IF} = 1 MHz.

Thus, in receive mode the frequency generated by the frequency synthesizer, f_c, must be programmed to be the LO frequency.

39 Alternate TX IF setting

It is possible to configure ***CC2400*** to operate with an intermediate frequency of 1 MHz in transmit mode. It is not generally recommended to do this, as the TX spectrum will have higher spur content than when using the direct up conversion mode. Using an intermediate frequency of 1 MHz in TX has the advantage of much lower RX/TX switching time because the VCO operates at the same frequency in RX and TX.

1 MHz IF in TX mode is enabled by setting MDMTST0.TX_1MHZ_OFFSET_N=0.

40 VCO

The VCO is completely integrated and operates at 4800 – 4966 MHz. The VCO frequency is divided by 2 to generate frequencies in the desired band (2400-2483 MHz).

The VCO frequency is related to FSDIV.FREQ[9:0] as follows:

$$f_{VCO} = 2 \cdot (2047 + FREQ[9:0])$$

41 VCO Self-Calibration

The characteristics of the VCO will vary with temperature, changes in supply voltages, and the desired operating frequency. In order to ensure reliable operation the bias current and tuning range of the VCO are automatically calibrated every time the RX mode or TX mode is enabled.

42 Output Power Programming

The RF output power from the device is programmable and is controlled by the FREND.PA_LEVEL[2:0] register. Table 19 shows the relationship between the register value, output power and current consumption.

PA_LEVEL[2:0] [binary]	RF frequency 2.45 GHz	
	Output power [dBm]	Current consumption, typ. [mA]
000	-25	11
001	-15	12
010	-10	13
011	-7	14
100	-4.6	16
101	-2.8	17
110	-1.3	18
111	0	19

Table 19. Output power settings and typical current consumption

43 Crystal Oscillator

An external clock signal or the internal crystal oscillator can be used as main frequency reference. The reference frequency must be 16 MHz. Because the crystal frequency is used as reference for the data rate as well as other internal signal processing functions, other frequencies cannot be used.

If an external clock signal is used this should be connected to XOSC16_Q1, while XOSC16_Q2 should be left open. If rail-to-rail (1.8V) square-wave signal is used, the `MAIN.XOSC16M_BYPASS` bit must be set. It is also possible to use a sine-wave input. A voltage swing of 200 mV peak-to-peak is recommended in this case.

Using the internal crystal oscillator, the crystal must be connected between the XOSC16_Q1 and XOSC16_Q2 pins. The oscillator is designed for parallel mode operation of the crystal. In addition, loading capacitors (C5 and C6) for the crystal are required. The loading capacitor values depend on the total load capacitance, C_L, specified for the crystal. The total load capacitance seen between the crystal terminals should equal C_L for the crystal to oscillate at the specified frequency.

$$C_L = \frac{1}{\frac{1}{C421}+\frac{1}{C431}} + C_{parasitic}$$

The parasitic capacitance is constituted by pin input capacitance and PCB stray capacitance. The total parasitic capacitance is typically 5 pF.

The crystal oscillator circuit is shown in Figure 23. Typical component values for different values of C_L are given in Table 20. Note that these values will depend on the PCB layout and the crystal used. Determination of the values should be done by measuring RF frequency on several boards and adjusting the values of the loading capacitors accordingly.

The crystal oscillator is amplitude regulated. This means that a high current is used to start up the oscillations. When the amplitude builds up, the current is reduced to what is necessary to maintain a stable oscillation. This ensures a fast start-up and keeps the drive level to a minimum. The ESR of the crystal should be within the specification in order to ensure a reliable start-up (see the Electrical Specifications section).

A small SMD crystal is used in the reference design; note that the crystal package strongly influences the price. In a low-cost design, it may be preferable to use a larger crystal package.

The required accuracy of the crystal is determined by the receive filtering. Figure 19 shows how sensitivity varies with the frequency offset between the transmitter and the receiver. It is important to take the total tolerance of the crystal into consideration; this consists of the initial tolerance, drift due to temperature and aging.

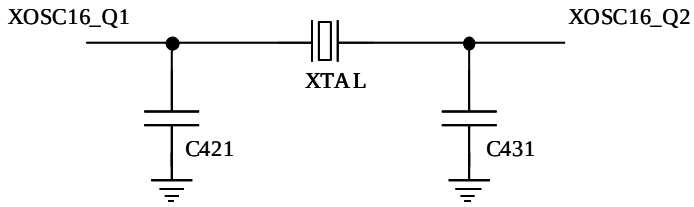


Figure 23. Crystal oscillator circuit

Item	C_L= 16 pF
C421	22 pF
C431	22 pF

Table 20. 16MHz crystal oscillator component values for C_L=16pF

44 Input / Output Matching

The RF input / output is differential (RF_N and RF_P). In addition there is supply switch output pin (TXRX_SWITCH) that must have an external DC path to RF_N and RF_P.

In RX mode the TXRX_SWITCH pin is at ground and will bias the LNA. In TX mode the TXRX_SWITCH pin is at supply rail voltage and will properly bias the internal PA.

The RF output and DC bias can be achieved using different topologies. Application circuits are shown in Figure 3 and Figure 4. Component values are given in Table 11.

If a single ended output is required (for a single ended connector or a single ended antenna), a balun should be used. The balun can be realized using discrete inductors and capacitors.

Using a differential antenna, no balun is required.

45 Typical performance graphs

The following graphs show how some important parameters vary with temperature. These graphs show typical performance as a function of temperature, and should be used as design guidance only.

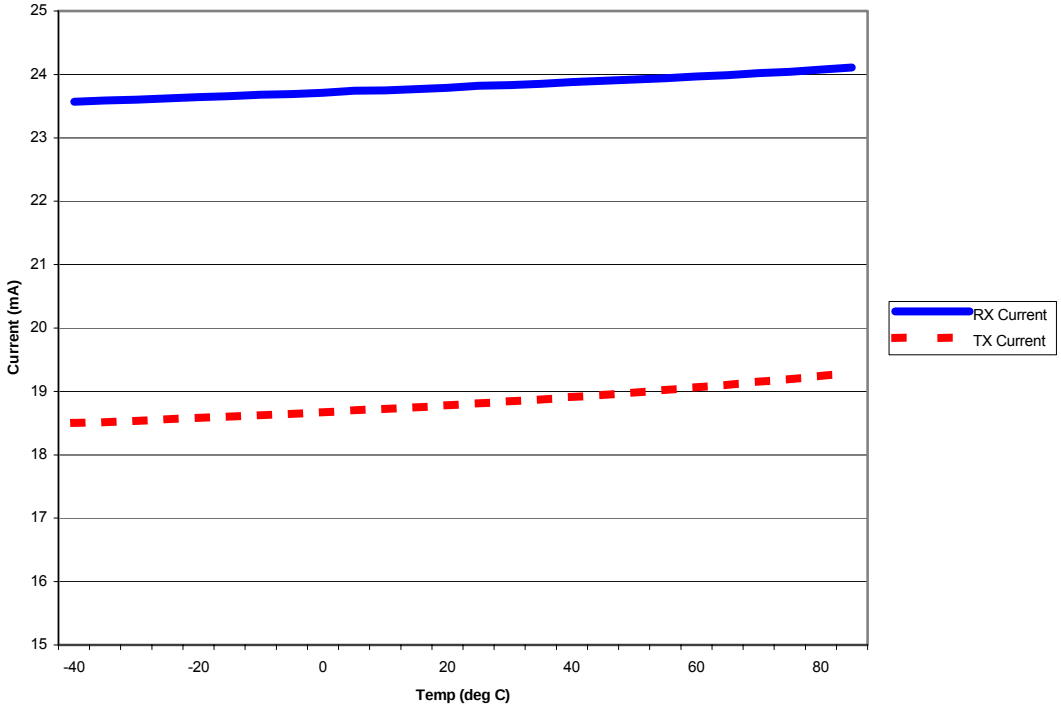


Figure 24 Typical RX and TX current vs. temperature

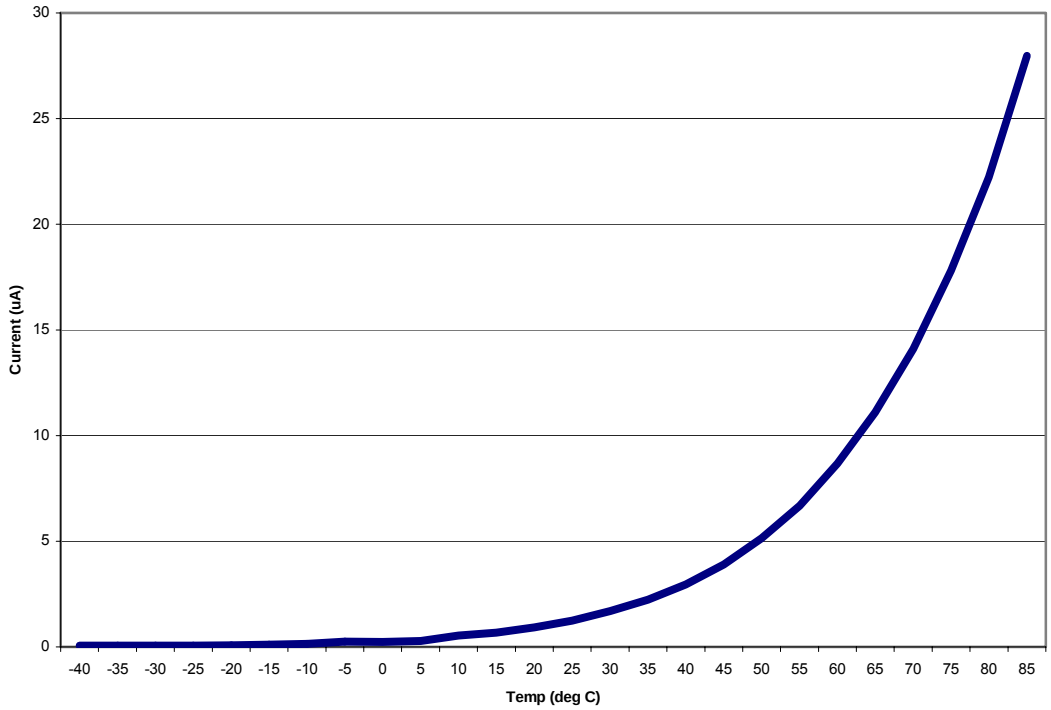


Figure 25 Typical power-down current vs. temperature

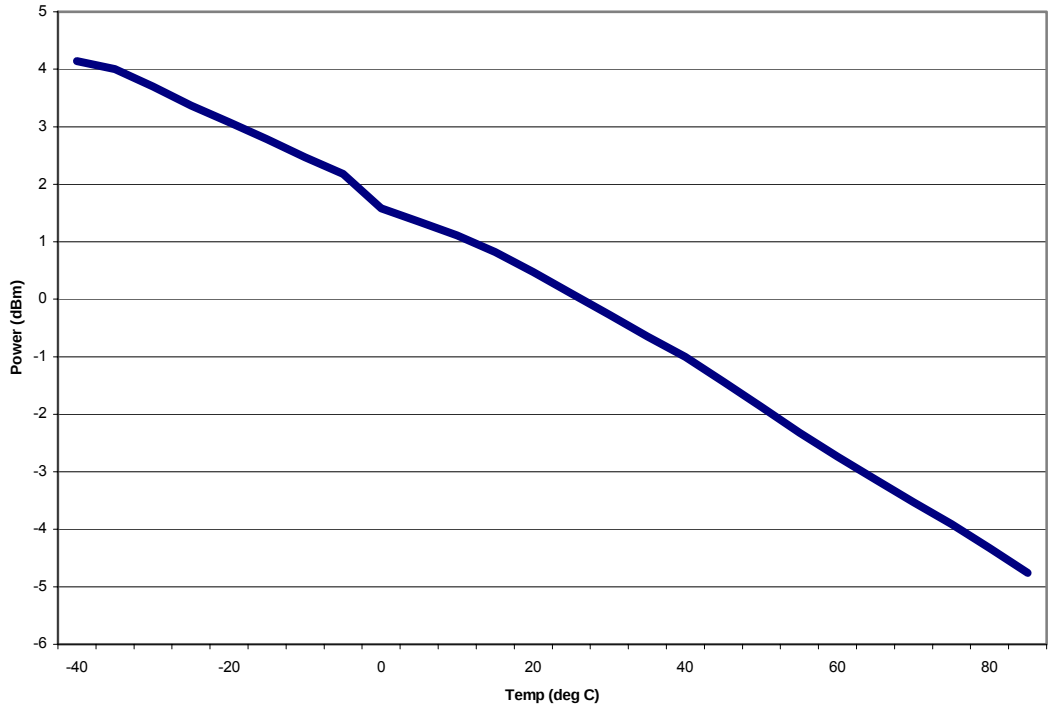


Figure 26 Typical output power vs. temperature

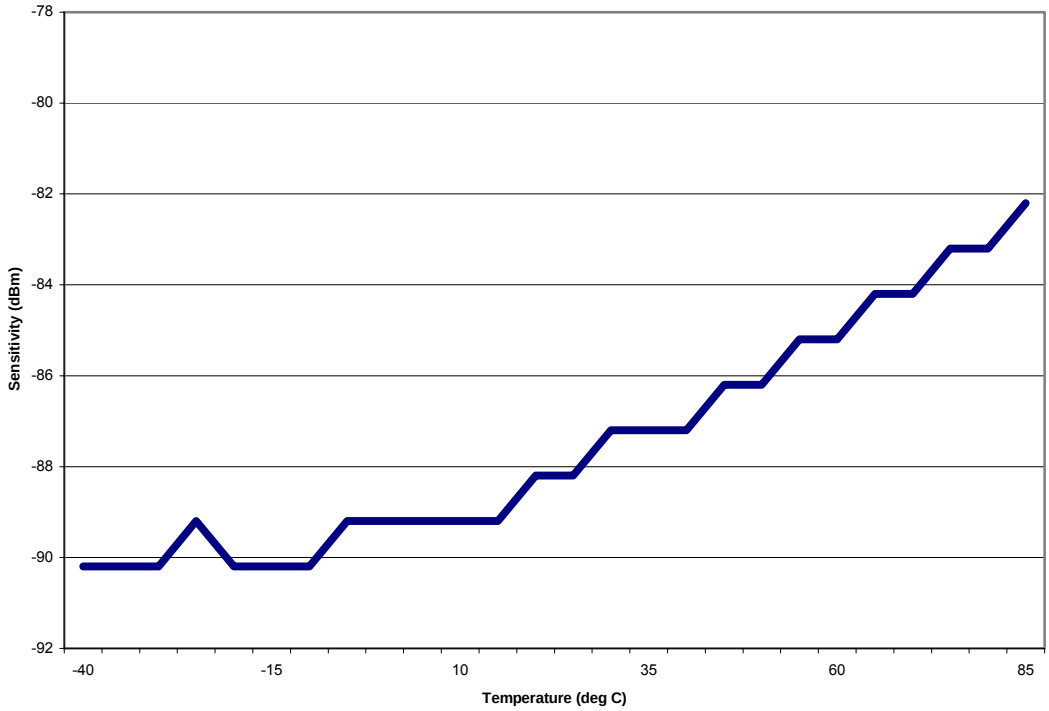


Figure 27 Typical 1 Mbps sensitivity vs. temperature

46 System Considerations and Guidelines

46.1 SRD regulations

International regulations and national laws regulate the use of radio receivers and transmitters. SRDs (Short Range Devices) for license free operation are allowed to operate in the 2.45 GHz bands worldwide. The most important regulations are EN 300 440 and EN 300 328 (Europe), FCC CFR47 part 15.247 and 15.249 (USA), and ARIB STD-T66 (Japan).

The CC2400EM reference design complies with EN 300 440. If frequency hopping is to be used at 1 Mbps data rate, GFSK should be selected to keep the bandwidth below 1 MHz. The ***CC2400*** complies with EN 300 440 class 2 if the band spacing is 2 MHz or more. It complies with EN 300 440 class 1 if the channel and band spacing is 10 MHz or more.

Please note that compliance with regulations is dependent on complete system performance. It is the customer's responsibility to ensure that the system complies with regulations.

46.2 Frequency hopping and multi-channel systems

The 2.400 – 2.4835 GHz band is shared by many systems both in industrial, office and home environment. It is therefore recommended to use frequency hopping spread spectrum (FHSS) or a multi-channel protocol because the frequency diversity makes the system more robust with respect to interference from other systems operating in the same frequency band.

CC2400 is highly suited for FHSS or multi-channel systems due to its agile frequency synthesizer and effective communication interface. Using the packet handling support and data buffering is also beneficial in such systems as these features will significantly offload the host controller.

Due to the low-IF I/Q receiver and the on-chip complex filtering, the image channel will be significantly rejected. This is important for all 2.4GHz systems.

46.3 Data burst transmissions

The high maximum data rate of ***CC2400*** opens up for burst transmissions. A low average data rate link (say 10 kbps), can be realized using a higher over-the-air data rate. Buffering the data and transmitting in bursts at high data rate (say 1 Mbps) will reduce the time in active mode, and hence also reduce the average current consumption significantly.

46.4 Continuous transmissions

In data streaming applications the ***CC2400*** opens up for continuous transmissions at 1 Mbps effective data rate. A typical application is digital audio systems. As the modulation is done with an I/Q up-converter with LO I/Q-signals coming from a closed loop PLL, there is no limitation in the length of a transmission. (Open loop modulation used in some transceivers often prevents this kind of continuous data streaming and reduces the effective data rate.)

46.5 Crystal drift compensation

A unique feature in ***CC2400*** is the very fine frequency resolution using the `MDMCTRL.MOD_OFFSET[5:0]`. This feature can be used to compensate for frequency offset and drift. The compensation affects both the receiver and the transmitter of the device being compensated. I.e. the received signal of the device will match the receiver's channel filter better. In the same way the center frequency of the transmitted signal will match the 'external' transmitter's signal.

Initial adjustment can be done using this frequency programmability. This eliminates the need for an expensive TCXO and trimming in some applications. The frequency offset between an 'external' transmitter and the receiver is measured in the ***CC2400*** and can be read back from an internal register (`FREQEST.RX_FREQ_OFFSET[7:0]`).
The measured frequency offset can thus

be used to calibrate the frequency using the 'external' transmitter as the reference. See also page 42 (Automatic Frequency Control). Figure 28 shows the improvement that can be achieved.

This feature can also be used for temperature compensation of the crystal if the temperature drift curve is known and a temperature sensor is included in the system.

In less demanding applications, a crystal with low temperature drift and low aging could be used without further compensation.

46.6 Spectrum efficient modulation

CC2400 also has the possibility to use Gaussian shaped FSK (GFSK). This spectrum-shaping feature improves adjacent channel power (ACP) and occupied bandwidth. In 'true' FSK systems with abrupt frequency shifting, the spectrum is inherently broad. By making the frequency shift 'softer', the spectrum can be made significantly narrower. Thus, higher data rates can be transmitted in the same bandwidth using GFSK.

46.7 Low latency systems

CC2400 is ideal for applications where latency is critical. Unbuffered mode should be used for lowest latency, since it takes time to fill the FIFO buffer. The total latency over the RF link in unbuffered mode is around 8 µs. ***CC2400*** can also provide very low RX-TX switching time, as described on page 47.

46.8 Low cost systems

As the ***CC2400*** provides 1 Mbps multi-channel performance without any external filters, a very low cost system can be made.

A differential antenna will eliminate the need for a balun, and the DC biasing can be achieved in the antenna topology, see Figure 4.

A small SMD crystal is used in the reference design; note that the crystal package strongly influences the price. In a low-cost design, it may be preferable to use a larger crystal package.

46.9 Battery operated systems

In low power applications, the power down mode should be used when not active. Depending on the start-up time requirement, the crystal oscillator core can be powered during power down. See page 36 for information on how effective power management can be implemented.

46.10 Increasing output power

In some applications it may be necessary to extend the link range. Adding an external power amplifier is the most effective way of doing this.

The power amplifier should be inserted between the antenna and the balun, and two T/R switches are needed to disconnect the PA in RX mode. See Figure 29.

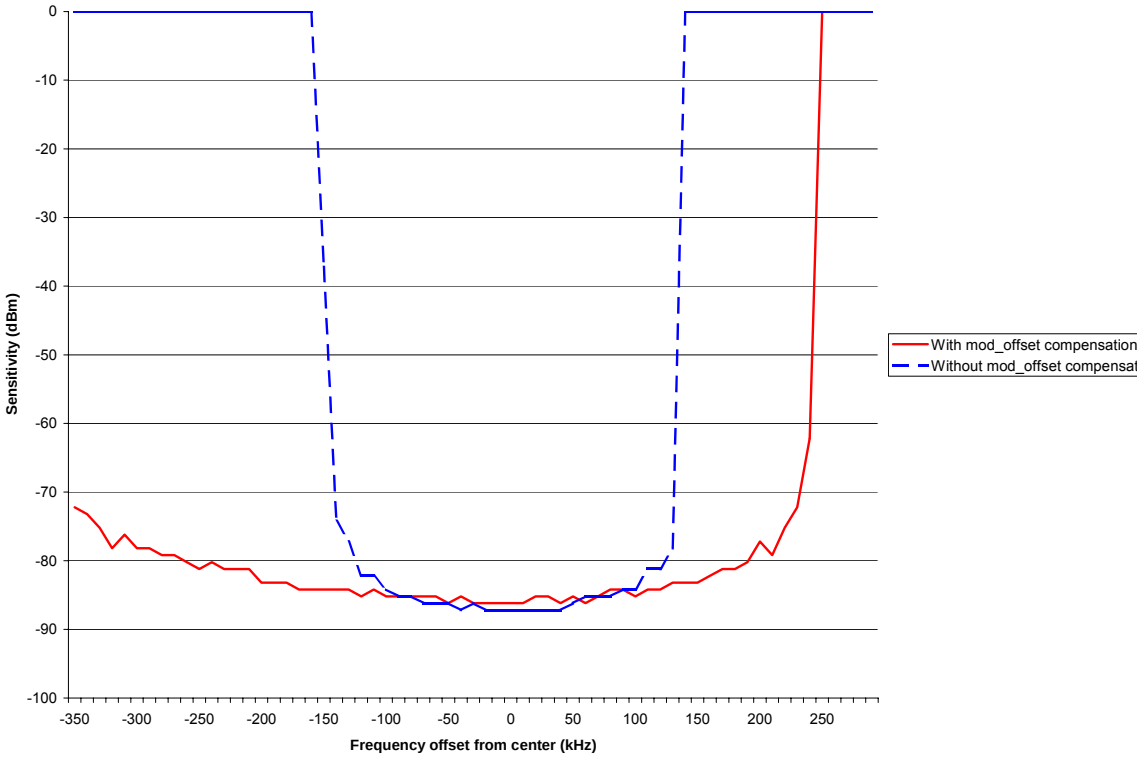


Figure 28. Sensitivity vs. frequency offset with and without AFC

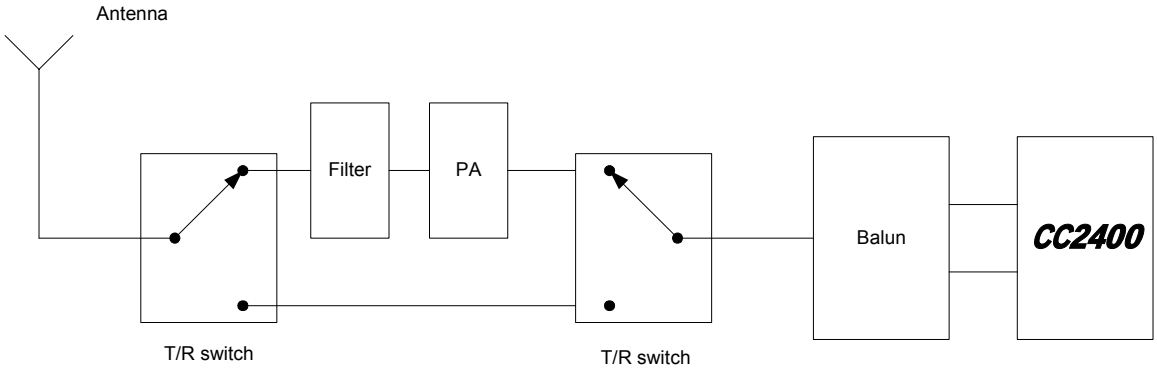


Figure 29. Block diagram of *CC2400* usage with external power amplifier

47 PCB Layout Recommendations

A four layer PCB is highly recommended. The second layer of the PCB should be the “ground-layer”.

The top layer should be used for signal routing, and the open areas should be filled with metallization connected to ground using several vias.

The area under the chip is used for grounding and must be connected closely to the ground plane with several vias.

The ground pins should be connected to ground as close as possible to the package pin using individual vias. The de-coupling capacitors should also be placed as close as possible to the supply pins and connected to the ground plane by separate vias. Supply power filtering is very important.

The external components should be as small as possible (0402 is recommended) and surface mount devices must be used. Please note that components smaller than those specified may have differing characteristics.

Caution should be used when placing the microcontroller in order to avoid interference with the RF circuitry.

A Development Kit with a fully assembled Evaluation Module is available. It is strongly advised that this reference layout is followed very closely in order to achieve the best performance.

The schematic, BOM and layout Gerber files for the reference designs are all available from the Chipcon website.

48 Antenna Considerations

CC2400 can be used together with various types of antennas. A differential antenna like a dipole would be the easiest to interface not needing a balun (balanced to un-balanced transformation network).

The length of the λ/2-dipole antenna is given by:

$$L = 14250 / f$$

where f is in MHz, giving the length in cm. An antenna for 2450 MHz should be 5.8 cm. Each arm is therefore 2.9 cm.

Other commonly used antennas for short-range communication are monopole, helical and loop antennas. The single-ended monopole and helical would require a balun network between the differential output and the antenna.

Monopole antennas are resonant antennas with a length corresponding to one quarter of the electrical wavelength (λ/4). They are very easy to design and can be implemented simply as a “piece of wire” or even integrated into the PCB.

The length of the λ/4-monopole antenna is given by:

$$L = 7125 / f$$

where f is in MHz, giving the length in cm. An antenna for 2450 MHz should be 2.9 cm.

Non-resonant monopole antennas shorter than λ/4 can also be used, but at the expense of range. In size and cost critical applications such an antenna may very well be integrated into the PCB.

Enclosing the antenna in high dielectric constant material reduces the overall size of the antenna. Many vendors offer such antennas intended for PCB mounting.

Helical antennas can be thought of as a combination of a monopole and a loop antenna. They are a good compromise in size critical applications. But helical antennas tend to be more difficult to optimize than the simple monopole.

Loop antennas are easy to integrate into the PCB, but are less effective due to difficult impedance matching because of their very low radiation resistance.

For low power applications the differential antenna is recommended giving the best range and because of its simplicity.

The antenna should be connected as close as possible to the IC. If the antenna is located away from the RF pins the antenna should be matched to the feeding transmission line (50 Ω).

49 Configuration Registers

The configuration of *CC2400* is done by programming the 16-bit configuration registers. The configuration data based on selected system parameters are most easily found by using the SmartRF® Studio software. Complete descriptions of the registers are given in the following tables. After a RESET is programmed, all the registers have default values as shown in the tables.

Some registers are Strobe Command Registers. Accessing these registers will initiate the change of an internal state or mode.

The FIFO is accessed as an 8-bit register.

Some registers contain signed values. These are in two's complement format. I.e. for a 4-bit value, 0000 is 0, 1111 is –1, 1110 is –2, 1000 is -8 and 0111 is 7.

During the address transfer a status byte is returned. This status byte is described in Table 13 at page 23.

Overview of *CC2400*'s control registers

Address	Register name	Register Type[1]	Description
0x00	MAIN	R/W	Main control register
0x01	FSCTRL	R/W	Frequency synthesiser main control and status
0x02	FSDIV	R/W	Frequency synthesiser frequency division control
0x03	MDMCTRL	R/W	Modem main control and status
0x04	AGCCTRL	R/W	AGC main control and status
0x05	FREND	R/W	Analog front-end control
0x06	RSSI	R/W	RSSI information
0x07	FREQEST	R/W	Received signal frequency offset estimation
0x08	IOCFG	R/W	I/O configuration register
0x09			Unused
0x0A			Unused
0x0B	FSMTC	R/W	Finite state machine time constants
0x0C	RESERVED	R/W	Reserved register containing spare control and status bits
0x0D	MANAND	R/W	Manual signal AND-override register
0x0E	FSMSTATE	R/W	Finite state machine information and breakpoint
0x0F	ADCTST	R/W	ADC test register
0x10	RXBPFTST	R/W	Receiver bandpass filters test register
0x11	PAMTST	R/W	PA and transmit mixers test register
0x12	LMTST	R/W	LNA and receive mixers test register
0x13	MANOR	R/W	Manual signal OR-override register
0x14	MDMTST0	R/W	Modem test register 0
0x15	MDMTST1	R/W	Modem test register 1
0x16	DACTST	R/W	DAC test register
0x17	AGCTST0	R/W	AGC test register: various control and status.
0x18	AGCTST1	R/W	AGC test register: AGC timeout.
0x19	AGCTST2	R/W	AGC test register: AGC various parameters.
0x1A	FSTST0	R/W	Test register: VCO array results and override.
0x1B	FSTST1	R/W	Test register: VC DAC manual control. VCO current constant.
0x1C	FSTST2	R/W	Test register:VCO current result and override.
0x1D	FSTST3	R/W	Test register: Charge pump current etc.
0x1E	MANFIDL	R	Manufacturer ID, lower 16 bit
0x1F	MANFIDH	R	Manufacturer ID, upper 16 bit
0x20	GRMDM	R/W	Generic radio modem control
0x21	GRDEC	R/W	Generic radio decimation control and status
0x22	PKTSTATUS	R	Packet mode status

[1] R/W - Read/write (control/status), R - Status only, S – Strobe command register (perform action upon access)

Address	Register name	Register Type[1]	Description
0x23	INT	R/W	Interrupt register
0x24	Reserved	R/W	
0x25	Reserved	R/W	
0x26	Reserved	R/W	
0x27	Reserved	R/W	
0x28	Reserved	R/W	
0x29	Reserved	R/W	
0x2A	Reserved	R/W	
0x2B	Reserved	R/W	
0x2C	SYNCL	R/W	Synchronisation word, lower 16 bit.
0x2D	SYNCH	R/W	Synchronisation word, upper 16 bit.
...			
0x60	SXOSCON	S	Command strobe register: Turn on XOSC.
0x61	SFSON	S	Command strobe register: Start and calibrate FS and go from RX/TX to a wait mode where the FS is running.
0x62	SRX	S	Command strobe register: Start RX.
0x63	STX	S	Command strobe register: Start TX (turn on PA).
0x64	SRFOFF	S	Command strobe register: Turn off RX/TX and FS.
0x65	SXOSCOFF	S	Command strobe register: Turn off XOSC.
0x66	Reserved	S	
0x67	Reserved	S	
0x68	Reserved	S	
0x69	Reserved	S	
0x6A	Reserved	S	
0x6B	Reserved	S	
0x6C	Reserved	S	
0x6D	Reserved	S	
0x6E	Reserved	S	
0x6F	Reserved	S	
0x70	FIFOREG	Special	Used to write data to and read data from the 8-bit wide 32 bytes FIFO used to buffer outgoing TX data and incoming RX data in buffered RF mode.

MAIN (0x00) - Main Control Register

Bit	Field Name	Reset	R/W	Description
15	RESETN	-	R/W	Active low reset of entire circuit. Should be applied before doing anything else.
14:10	-	0	W0	Reserved, write as 0.
9	FS_FORCE_EN	0	R/W	Forces the frequency synthesiser on (starts with a calibration). The synthesiser can also be turned on in a number of other ways.
8	RXN_TX	0	R/W	Selects whether RX operation ('0') or TX operation ('1') is desired when FS_FORCE_EN is used. RX or TX mode is usually selected using the SRX and STX strobe commands (or RX and TX pins).
7:4	-	0	W0	Reserved, write as 0.
3	-	0	R/W	Reserved, write as 0.
2	-	0	R/W	Reserved, write as 0.
1	XOSC16M_BYPASS	0	R/W	Bypasses the 16 MHz main crystal oscillator and uses a buffered version of the signal on Q1 directly. Used for external clock only.
0	XOSC16M_EN	0	R/W	Forces the 16 MHz main crystal oscillator and the global bias on. These modules can also be turned on in other ways.

FSCTRL (0x01) - Frequency Synthesiser Control and Status

Bit	Field Name	Reset	R/W	Description
15:6	-	0	W0	Reserved, write as 0.
5:4	LOCK_THRESHOLD[1:0]	1	R/W	Number of consecutive reference clock periods with successful sync windows required to indicate lock: 0: 64 1: 128 2: 256 3: 512
3	CAL_DONE	0	R	Calibration has been performed since the last time the FS was turned on.
2	CAL_RUNNING	0	R	Calibration status, '1' when calibration in progress.
1	LOCK_LENGTH	0	R/W	LOCK_WINDOW pulse width: 0: 2 CLK_PRE periods 1: 4 CLK_PRE periods
0	LOCK_STATUS	0	R	'1' when PLL is in lock, otherwise '0'.

FSDIV (0x02) - Frequency Synthesiser Frequency Division Control

Bit	Field Name	Reset	R/W	Description
15:12	-	0	W0	Reserved, write as 0.
11:10	FREQ[11:10]	2	R	Read only. Directly gives the right frequency in MHz when reading/writing FREQ[11:0].
9:0	FREQ[9:0]	353	R/W	Frequency control word. $f_c = FREQ[11:0] = 2048 + FREQ[9:0]$ [MHz] where f_c is the channel centre frequency. See page 47 for a description of how to program the channel for tansmit and receive modes respectively. Reading/writing FREQ[11:0] gives the right frequency in MHz. The default value corresponds to f_c=2401MHz.

MDMCTRL (0x03) - Modem Control and Status

Bit	Field Name	Reset	R/W	Description
15:13	-	0	W0	Reserved, write as 0.
12:7	MOD_OFFSET[5:0]	0	R/W	Modulator/Demodulator centre frequency in 15.625 kHz steps (for the receiver the steps are relative to 1 MHz, for the transmitter the steps are relative to 0MHz when MDMTST0.TX_1MHZ_OFFSET_N=1). Two's complement signed value. I.e. MOD_OFFSET=0x1F ➔ centre frequency=1.48 MHz; MOD_OFFSET=0x20 ➔ centre frequency=0.50 MHz.
6:0	MOD_DEV[6:0]	64	R/W	Modulator frequency deviation in 3.9062 kHz steps (0-500 kHz). Unsigned value. Reset value gives a deviation of 250 kHz.

AGCCTRL (0x04) - AGC Control and Status

Bit	Field Name	Reset	R/W	Description
15:8	VGA_GAIN [7:0]	0XF7	R/W	When written, VGA manual gain override value; when read, the currently used VGA gain setting.
7:4	-	0	W0	Reserved, write as 0.
3	AGC_LOCKED	0	R	AGC lock status
2	AGC_LOCK	0	R/W	Lock gain after maximum number of attempts.
1	AGC_SYNC_LOCK	0	R/W	Lock gain after sync word received and maximum number of attempts. (As configured in AGCTST0.AGC_ATTEMPTS. Attempts may be 0)
0	VGA_GAIN_OE	0	R/W	Use the VGA_GAIN value during RX instead of the AGC value.

FREND (0x05) – Front-end Control Register

Bit	Field Name	Reset	R/W	Description
15:4	-	0	W0	Reserved, write as 0.
3	-	1	W1	Reserved, write as 1.
2:0	PA_LEVEL[2:0]	7	R/W	PA output power level.

RSSI (0x06) - RSSI Status and Control Register

Bit	Field Name	Reset	R/W	Description
15:8	RSSI_VAL[7:0]	-	R	Averaged RSSI estimate on a logarithmic scale in signed two's complement format. Unit is 1 dB. Offset= -54dB, see also page 44.
7:2	RSSI_CS_THRES[5:0]	0X3C	R/W	Carrier sense signal threshold value in signed two's complement format. Unit is 4 dB. The CS_ABOVE_THRESHOLD_N signal goes low when the received signal is above this value. The CS_ABOVE_THRESHOLD_N signal is available on the GIO1 pin or in the status word returned during SPI address byte. The reset value corresponds to a threshold of approx. -69 dBm.
1:0	RSSI_FILT[1:0]	2	R/W	RSSI averaging filter length: 0: 0 bits (no filtering) 1: 1 bit 2: 4 bits 3: 8 bits

FREQEST (0x07) - Received frequency offset estimation

Bit	Field Name	Reset	R/W	Description
15:8	RX_FREQ_OFFSET[7:0]	-	R	Estimate of the received signals centre frequency comparison to the ideal 1 MHz centre frequency. Two's complement signed value. See page 42.
7:0	-	0	W0	Reserved, write as 0.

IOCFG (0x08) - I/O configuration register

Bit	Field Name	Reset	R/W	Description
15	-	0	W0	Reserved, write as 0.
14:9	GIO6_CFG[5:0]	11	R/W	Configuration of the GIO6 pin. See page 45 for options. The reset value outputs the signal CRC_OK on pin GIO6.
8:3	GIO1_CFG[5:0]	60	R/W	How to use the GIO1 pin. See page 45 for options. The reset value outputs the signal LOCK_STATUS on pin GIO1.
2:0	HSSD_SRC[2:0]	0	R/W	For test purposes only. The HSSD (High Speed Serial Data) test module is used as follows: 0: Off. 1: Output AGC status (gain setting / peak detector status / accumulator value) 2: Output ADC I and Q values. 3: Output I/Q after digital down-mixing and channel filtering. 4: Output RX signal magnitude / frequency unfiltered (from demodulator). 5: Output RX signal magnitude / frequency filtered (from demodulator). 6: Output RSSI / RX frequency offset estimation 7: Input DAC values. The HSSD test module requires that the FS is up and running as it uses CLK_PRE (~150 MHZ) to produce its ~37.5 MHz data clock and serialize its output words. Also, in order for HSSD to function properly GRMDM.PIN_MODE must be set for HSSD.

FSMTC (0x0B) - Finite state machine time constants

Bit	Field Name	Reset	R/W	Description
15:13	TC_RXON2AGCEN[2:0]	3	R/W	The time in 5 µs steps from RX is turned on until the AGC is enabled. This time constant must be large enough to allow the RX chain to settle so that the AGC algorithm starts working on a proper signal. The default value corresponds to 15 us.
12:10	TC_PAON2SWITCH[2:0]	6	R/W	The time in µs from TX is started until the TX/RX switch allows the TX signal to pass.
9:6	RES[9:6]	10	R/W	Reserved
5:3	TC_TXEND2SWITCH[2:0]	2	R/W	The time in µs from TX is stopped (for instance the last bit of the packet is sent) until the RX/TX switch breaks the TX output and the PKT signal is set.

Bit	Field Name	Reset	R/W	Description
2:0	TC_TXEND2PAOFF[2:0]	4	R/W	The time in µs from TX is stopped until the TX chain is turned off and the state machine goes to the next state. The PKT signal will then go low. This value must be greater than TC_TXEND2SWITCH[2:0].

RESERVED (0x0C) - Reserved register containing spare control and status bits

Bit	Field Name	Reset	R/W	Description
15:5	RES[15:5]	0	R/W	Reserved
4:0	RES[4:0]	0	R/W	Reserved

MANAND (0x0D) - Manual signal AND override register[2]

Bit	Field Name	Reset	R/W	Description
15	VGA_RESET_N	1	R/W	Overrides VGA_RESET_N used to reset the peak detectors in the VGA in the RX chain. Must be set to 0 during chip initialization.
14	LOCK_STATUS	1	R/W	Overrides the LOCK_STATUS top-level signal that indicates whether VCO lock is achieved or not.
13	BALUN_CTRL	1	R/W	Overrides the BALUN_CTRL signal that controls whether the PA should receive its required external biasing (1) or not (0) by controlling the RX/TX output switch.
12	RXTX	1	R/W	Overrides the RXTX signal that controls whether the LO buffers (0) or PA buffers (1) should be used.
11	PRE_PD	1	R/W	Power down of prescaler.
10	PA_N_PD	1	R/W	Power down of PA (negative path).
9	PA_P_PD	1	R/W	Power down of PA (positive path). When PA_N_PD=1 and PA_P_PD=1 the up-conversion mixers are in powerdown.
8	DAC_LPF_PD	1	R/W	Power down of TX DACs.
7	BIAS_PD	1	R/W	Power down control of global bias generator + XOSC clock buffer.
6	XOSC16M_PD	1	R/W	Power down control of 16 MHz XOSC core.
5	CHP_PD	1	R/W	Power down control of charge pump.
4	FS_PD	1	R/W	Power down control of VCO, I/Q generator, LO buffers.

[2] For some important signals the value can be overridden manually by the MANAND and MANOVR registers. This is done as follows for the hypothetical important signal IS:

```
IS_USED = (IS * IS_AND_MASK) + IS_OR_MASK,
```

using Boolean notation.

The AND-mask and OR-mask for the important signals listed resides in the MANAND and MANOR registers, respectively.

Examples:

- Writing 0xFFFE to MANAND and 0x0000 to MANOR will force LNAMIX_PD=0 whereas all other signals will be unaffected.
- Writing 0xFFFF to MANAND and 0x0001 to MANOVR will force LNAMIX_PD=1 whereas all other signals will be unaffected.

Bit	Field Name	Reset	R/W	Description
3	ADC_PD	1	R/W	Power down control of the ADCs.
2	VGA_PD	1	R/W	Power down control of the VGA.
1	RXBPF_PD	1	R/W	Power down control of the band-pass receive filter.
0	LNAMIX_PD	1	R/W	Power down control of the LNA, down-conversion mixers and front-end bias.

FSMSTATE (0x0E) - Finite state machine information and breakpoint

Bit	Field Name	Reset	R/W	Description
15:13	-	0	W0	Reserved, write as 0.
12:8	FSM_STATE_BKPT[4:0]	0	R/W	FSM breakpoint state. State=0 means that breakpoints are disabled.
7:5	-	0	W0	Reserved, write as 0.
4:0	FSM_CUR_STATE[4:0]	-	R	Gives the current state of the finite state machine.

ADCTST (0x0F) - ADC Test Register

Bit	Field Name	Reset	R/W	Description
15	-	0	W0	Reserved, write as 0.
14:8	ADC_I[6:0]	-	R	Read the current ADC I-branch value.
7	-	0	W0	Reserved, write as 0.
6:0	ADC_Q[6:0]	-	R	Read the current ADC Q-branch value.

RXBPFTST (0x10) - Receiver Band-pass Filters Test Register

Bit	Field Name	Reset	R/W	Description
15	-	0	W0	Reserved, write as 0.
14	RXBPF_CAP_OE	0	R/W	RX band-pass filter capacitance calibration override enable.
13:7	RXBPF_CAP_O[6:0]	0	R/W	RX band-pass filter capacitance calibration override value.
6:0	RXBPF_CAP_RES[6:0]	-	R	RX band-pass filter capacitance calibration result. 0 Minimum capacitance in the feedback. 1: Second smallest capacitance setting. … 127: Maximum capacitance in the feedback.

PAMTST (0x11) - PA and Transmit Mixers Test Register

Bit	Field Name	Reset	R/W	Description
15:13	-	0	W0	Reserved, write as 0.
12	VC_IN_TEST_EN	0	R/W	When ATESTMOD_MODE=7 this controls whether the ATEST1 in is used to output the VC node voltage (0) or to control the VC node voltage (1).
11	ATESTMOD_PD	1	W	Power down of the analog test module.
10:8	ATESTMOD_MODE[2:0]	0	R/W	When ATESTMOD_PD=0, the function of the analog test module is as follows: 0: Outputs "I" (ATEST2) and "Q" (ATEST1) from RxMIX. 1: Inputs "I" (ATEST2) and "Q" (ATEST1) to BPF. 2: Outputs "I" (ATEST2) and "Q" (ATEST1) from VGA. 3: Inputs "I" (ATEST2) and "Q" (ATEST1) to ADC. 4: Outputs "I" (ATEST2) and "Q" (ATEST1) from LPF. 5: Inputs "I" (ATEST2) and "Q" (ATEST1) to TxMIX. 6: Outputs "P" (ATEST2) and "N" (ATEST1) from Prescaler. 7: Connects TX IF to RX IF and simultaneously the ATEST1 pin to the internal VC node (see VC_IN_TEST_EN).
7	-	0	W0	Reserved, write as 0.
6:5	TXMIX_CAP_ARRAY[1:0]	0	R/W	Selects varactor array settings in the transmit mixers.
4:3	TXMIX_CURRENT[1:0]	0	R/W	Transmit mixers current: 0: 1.72 mA 1: 1.88 mA 2: 2.05 mA 3 2.21 mA
2:0	PA_CURRENT[2:0]	3	R/W	Programming of the PA current 0: -3 current adjustment 1: -2 current adjustment 2: -1 current adjustment 3: Nominal setting 4: +1 current adjustment 5: +2 current adjustment 6: +3 current adjustment 7: +4 current adjustment

LMTST (0x12) - LNA and receive mixers test register

Bit	Field Name	Reset	R/W	Description
15:14	-	0	W0	Reserved, write as 0.
13	RXMIX_HGM	1	R/W	Receiver mixers high gain mode enable.
12:11	RXMIX_TAIL[1:0]	1	R/W	Control of the receiver mixers output current. 0: 12 µA 1: 16 µA (Nominal) 2: 20 µA 3:24 µA
10:9	RXMIX_VCM[1:0]	1	R/W	Controls VCM level in the mixer feedback loop 0: 8 µA mixer current 1: 12 µA mixer current (Nominal) 2: 16 µA mixer current 3: 20 µA mixer current Must be set to 0 during chip initialisation.
8:7	RXMIX_CURRENT[1:0]	2	R/W	Controls current in the mixer 0: 360 µA mixer current (x2) 1: 720 µA mixer current (x2) 2: 900 µA mixer current (x2) (Nominal) 3: 1260 µA mixer current (x2)
6:5	LNA_CAP_ARRAY[1:0]	1	R/W	Selects varactor array setting in the LNA 0: OFF 1: 0.1pF (x2) (Nominal) 2: 0.2pF (x2) 3: 0.3pF (x2)
4	LNA_LOWGAIN	0	R/W	Selects low gain mode of the LNA 0: 19 dB (Nominal) 1: 7 dB
3:2	LNA_GAIN[1:0]	0	R/W	Controls current in the LNA gain compensation branch 0: OFF (Nominal) 1: 100 µA LNA current 2: 300 µA LNA current 3: 1000 µA LNA current
1:0	LNA_CURRENT[1:0]	2	R/W	Controls main current in the LNA 0: 240 µA LNA current (x2) 1: 480 µA LNA current (x2) 2: 640 µA LNA current (x2) (Nominal) 3: 1280 µA LNA current (x2)

MANOR (0x13) - Manual signal OR override register[3]

Bit	Field Name	Reset	R/W	Description
15	VGA_RESET_N	0	R/W	Overrides VGA_RESET_N used to reset the peak detectors in the VGA in the RX chain.
14	LOCK_STATUS	0	R/W	Overrides the LOCK_STATUS top-level signal that indicates whether VCO lock is achieved or not.
13	BALUN_CTRL	0	R/W	Overrides the BALUN_CTRL signal that controls whether the PA should receive its required external biasing (1) or not (0) by controlling the RX/TX output switch.
12	RXTX	0	R/W	Overrides the RXTX signal that controls whether the LO buffers (0) or PA buffers (1) should be used.
11	PRE_PD	0	R/W	Power down of prescaler.
10	PA_N_PD	0	R/W	Power down of PA (negative path).
9	PA_P_PD	0	R/W	Power down of PA (positive path). When PA_N_PD=1 and PA_P_PD=1 the up-conversion mixers are in power down.
8	DAC_LPF_PD	0	R/W	Power down of TX DACs.
7	BIAS_PD	0	R/W	Power down control of global bias generator + XOSC clock buffer.
6	XOSC16M_PD	0	R/W	Power down control of 16 MHz XOSC core.
5	CHP_PD	0	R/W	Power down control of charge pump.
4	FS_PD	0	R/W	Power down control of VCO, I/Q generator, LO buffers.
3	ADC_PD	0	R/W	Power down control of the ADCs.
2	VGA_PD	0	R/W	Power down control of the VGA.
1	RXBPF_PD	0	R/W	Power down control of complex band-pass receive filter.
0	LNAMIX_PD	0	R/W	Power down control of LNA, down-conversion mixers and front-end bias.

MDMTST0 (0x14) - Modem Test Register 0

Bit	Field Name	Reset	R/W	Description
15:14	-	0	W0	Reserved, write as 0.
13	TX_PRNG	0	R/W	When set, the transmitted data is taken from a 10-bit PRNG instead of from the DIO pin in un-buffered mode or from the FIFO in buffered mode.
12	TX_1MHZ_OFFSET_N	0	R/W	Determines TX IF frequency: 0: 1 MHz (Not used) 1: 0 MHz (During initialization this bit must be set to a logical '1'.)
11	INVERT_DATA	0	R/W	When this bit is set the data are inverted (internally) before transmission, and inverted after reception.
10	AFC_ADJUST_ON_PACKET	0	R/W	When this bit is set to '1', modem parameters are adjusted for slow tracking of the received signal as opposed to quick acquisition when a packet is received in RX.

- [3] See footnote for MANAND register (address 0x0D) for description of the use of this register.

Bit	Field Name	Reset	R/W	Description
9:8	AFC_SETTLING[1:0]	3	R/W	Controls how many max-min pairs that are used to compute the output. 00: 1 pair 01: 2 pairs 10: 4 pairs 11: 8 pairs
7:0	AFC_DELTA[7:0]	75	R/W	Programmable level used in AFC-algorithm that indicates the expected frequency deviation of the received signal. See page 42 for further details.

MDMTST1 (0x15) - Modem Test Register 1

Bit	Field Name	Reset	R/W	Description
15:7	-	0	W0	Reserved, write as 0.
6:0	BSYNC_THRESHOLD[6:0]	75	R/W	Threshold value used in clock recovery algorithm. Sets the level for when re-synchronization takes place.

DACTST (0x16) - DAC Test Register

Bit	Field Name	Reset	R/W	Description
15	-	0	W0	Reserved, write as 0.
14:12	DAC_SRC[2:0]	0	R/W	The TX DACs data source is selected by DAC_SRC according to: 0: Normal operation (from modulator). 1: The DAC_I_O and DAC_Q_O override values below. 2: From ADC 3: I/Q after digital down-mixing and channel filtering. 4: Full-spectrum White Noise (from PRNG.) 5: RX signal magnitude / frequency filtered (from demodulator). 6: RSSI / RX frequency offset estimation. 7: HSSD module. This feature will often require the DACs to be manually turned on in MANOVR and PAMTST.ATESTMOD_MODE=4.
11:6	DAC_I_O[5:0]	0	R/W	I-branch DAC override value.
5:0	DAC_Q_O[5:0]	0	R/W	Q-branch DAC override value.

AGCTST0 (0x17) - AGC Test Register 0

Bit	Field Name	Reset	R/W	Description
15:13	AGC_SETTLE_BLANK_DN[2:0]	4	R/W	AGC blanking enable/limit for negative gain changes. 0: Disabled 1-7: Duration of blanking signal in 8 MHz clock cycles.
12:11	AGC_WIN_SIZE[1:0]	2	R/W	AGC window size.
10:7	AGC_SETTLE_PEAK[3:0]	2	R/W	AGC peak detectors settling period.
6:3	AGC_SETTLE_ADC[3:0]	2	R/W	AGC ADC settling period.
2:0	AGC_ATTEMPTS[2:0]	0	R/W	The maximum number of attempts to set the gain.

AGCTST1 (0x18) - AGC Test Register 1

Bit	Field Name	Reset	R/W	Description
15	-	0	W0	Reserved, write as 0.
14	AGC_VAR_GAIN_SAT	1	R/W	Chooses the gain reduction upon saturation of the variable gain stage: 0: -1/-3 gain steps 1: -3/-5 gain steps
13:11	AGC_SETTLE_BLANK_UP[2:0]	0	R/W	AGC blanking enable/limit for positive gain changes. 0: Disabled 1-7: Duration of blanking signal in 8 MHz clock cycles.
10	PEAKDET_CUR_BOOST	0	R/W	Doubles the bias current in the peak-detectors in-between the VGA stages when set.
9:6	AGC_MULT_SLOW[3:0]	0	R/W	AGC timing multiplier, slow mode.
5:2	AGC_SETTLE_FIXED[3:0]	4	R/W	AGC settling period, fixed gain step.
1:0	AGC_SETTLE_VAR[1:0]	0	R/W	AGC settling period, variable gain step.

AGCTST2 (0x19) - AGC Test Register 1

Bit	Field Name	Reset	R/W	Description
15:14	-	0	W0	Reserved, write as 0.
13:12	AGC_BACKEND_BLANKING[1:0]	0	R/W	AGC blanking makes sure that the modem locks its bit synchronization and centre frequency estimator when the AGC changes the gain. 0: Disabled 1-3: Fixed/variable enable
11:9	AGC_ADJUST_M3DB[2:0]	0	R/W	AGC parameter -3 dB.
8:6	AGC_ADJUST_M1DB[2:0]	0	R/W	AGC parameter -1 dB.
5:3	AGC_ADJUST_P3DB[2:0]	0	R/W	AGC parameter +3 dB.
2:0	AGC_ADJUST_P1DB[2:0]	0	R/W	AGC parameter +1 dB.

FSTST0 (0x1A) - Frequency Synthesiser Test Register 0

Bit	Field Name	Reset	R/W	Description
15:14	RXMIXBUF_CUR[1:0]	2	R/W	RX mixer buffer bias current. 0: 690uA 1: 980uA 2: 1.16mA (nominal) 3: 1.44mA
13:12	TXMIXBUF_CUR[1:0]	2	R/W	TX mixer buffer bias current. 0: 690uA 1: 980uA 2: 1.16mA (nominal) 3: 1.44mA
11	VCO_ARRAY_SETTLE_LONG	0	R/W	When '1' this control bit doubles the time allowed for VCO settling during FS calibration.
10	VCO_ARRAY_OE	0	R/W	VCO array manual override enable.
9:5	VCO_ARRAY_O[4:0]	16	R/W	VCO array override value.
4:0	VCO_ARRAY_RES[4:0]	-	R	The resulting VCO array setting from the last calibration.

FSTST1 (0x1B) - Frequency Synthesiser Test Register 1

Bit	Field Name	Reset	R/W	Description
15	RXBPF_LOCUR	0	R/W	Controls reference bias current to RX band-pass filters: 0: 4 uA (nominal) 1: 3 uA
14	RXBPF_MIDCUR	0	R/W	Controls reference bias current to RX band-pass filters: 0: 4 uA (nominal) 1: 3.5 uA
13:10	VCO_CURRENT_REF[3:0]	4	R/W	The value of the reference current calibrated against during VCO calibration.
9:4	VCO_CURRENT_K[5:0]	0	R/W	VCO current calibration constant (override value current B when FSTST2.VCO_CURRENT_OE=1).
3	VC_DAC_EN	0	R/W	Controls the source of the VCO control voltage in normal operation (PAMTST.VC_IN_TEST_EN=0): 0: Loop filter (closed loop PLL) 1: VC DAC (open loop PLL)
2:0	VC_DAC_VAL[2:0]	2	R/W	VC DAC output value. (The value of the reference voltage used during VCO calibration.)

FSTST2 (0x1C) - Frequency Synthesiser Test Register 2

Bit	Field Name	Reset	R/W	Description
15	-	0	W0	Reserved, write as 0.
14:13	VCO_CURCAL_SPEED[1:0]	0	R/W	VCO current calibration speed: 0: Normal 1: Undefined 2: Half speed 3: Undefined.
12	VCO_CURRENT_OE	0	R/W	VCO current manual override enable.
11:6	VCO_CURRENT_O[5:0]	24	R/W	VCO current override value (current A).
5:0	VCO_CURRENT_RES[5:0]	-	R	The resulting VCO current setting from last calibration.

FSTST3 (0x1D) - Frequency Synthesiser Test Register 3

Bit	Field Name	Reset	R/W	Description
15:14	-	0	W0	Reserved, write as 0.
13	CHP_TEST_UP	0	R/W	When CHP_DISABLE=1 forces the CHP to output "up" current.
12	CHP_TEST_DN	0	R/W	When CHP_DISABLE=1 forces the CHP to output "down" current.
11	CHP_DISABLE	0	R/W	Set to disable charge pump during VCO calibration.
10	PD_DELAY	0	R/W	Selects short or long reset delay in phase detector: 0: Short reset delay 1: Long reset delay
9:8	CHP_STEP_PERIOD[1:0]	2	R/W	The charge pump current value step period: 0: 0.25 us 1: 0.5 us 2: 1 us 3: 4 us
7:4	STOP_CHP_CURRENT[3:0]	13	R/W	The charge pump current to stop at after the current is stepped down from START_CHP_CURRENT after VCO calibration is complete. The current is stepped down periodically with intervals as defined in CHP_STEP_PERIOD.
3:0	START_CHP_CURRENT [3:0]	13	R/W	The charge pump current to start with after VCO calibration is complete. The current is then stepped down periodically to the value STOP_CHP_CURRENT with intervals as defined in CHP_STEP_PERIOD.

MANFIDL (0x1E) - Manufacturer ID, Lower 16 Bit

Bit	Field Name	Reset	R/W	Description
15:12	PARTNUM[3:0]	1	R	The device part number. ***CC2400*** has part number 0x001.
11:0	MANFID[11:0]	0X33D	R	Gives the JEDEC manufacturer ID. The actual manufacturer ID can be found in MANIFID[7:1], the number of continuation bytes in MANFID[11:8] and MANFID[0]=1. Chipcon's JEDEC manufacturer ID is 0x7F 0x7F 0x7F 0x9E (0x9E preceded by three continuation bytes.)

MANFIDH (0x1F) - Manufacturer ID, Upper 16 Bit

Bit	Field Name	Reset	R/W	Description
15:12	VERSION[3:0]	0	R	Chip version number.
11:0	PARTNUM[15:4]	0	R	The device part number. ***CC2400*** has part number 0x001.

GRMDM (0x20) - Generic Radio Modem Control and Status

Bit	Field Name	Reset	R/W	Description
15	-	0	W0	Reserved, write as 0.
14:13	SYNC_ERRBITS_ALLOWED [1:0]	0	R/W	Sync word detection occurs when the number of bits in the sync word correlator different from that specified by the SYNC registers is equal to or lower than SYNC_ERRBITS_ALLOWED.
12:11	PIN_MODE[1:0]	1	R/W	Selects between un-buffered mode, buffered mode or test mode. The pin configuration is set according to Table 15. 0: Un-buffered mode 1: Buffered mode 2: HSSD test mode 3: Unused
10	PACKET_MODE	1	R/W	When this bit is set the packet mode is enabled. The pin configuration is set according to Table 15. In TX, this enables preamble generation, sync word, and CRC appending (if enabled by CRC_ON) in the buffered mode. In RX, this enables sync word detection in buffered *and* un-buffered modes, and CRC verification (if enabled by CRC_ON) in buffered mode.
9:7	PRE_BYTES[2:0]	3	R/W	The number of preamble bytes ("01010101") to be sent in packet mode: 000: 0 001: 1 010: 2 011: 4 100: 8 101: 16 110: 32 111: Infinitely on
6:5	SYNC_WORD_SIZE[1:0]	3	R/W	The size of the packet mode sync word sent in TX and correlated against in RX: 00: The 8 MSB bits of SYNC_WORD. 01: The 16 MSB bits of SYNC_WORD. 10: The 24 MSB bits of SYNC_WORD. 11: The 32 MSB bits of SYNC_WORD.
4	CRC_ON	1	R/W	In packet mode a CRC is calculated and is transmitted after the data in TX, and a CRC is calculated during reception in RX.

Bit	Field Name	Reset	R/W	Description
3:2	DATA_FORMAT[1:0]	0	R/W	Selects line-coding format used during RX and TX operations. 00: NRZ 01: Manchester 10: 8/10 line-coding (Not applied to preambles or sync words) 11: Reserved
1	MODULATION_FORMAT	0	R/W	Modulation format of modem: 0: FSK/GFSK 1: Reserved
0	TX_GAUSSIAN_FILTER	1	R/W	When this bit is set the data sent in TX is Gaussian filtered before transmission enabling GFSK

GRDEC (0x21) - Generic Radio Decimation Control and Status

Bit	Field Name	Reset	R/W	Description
15:13	-	0	W0	Reserved, write as 0.
12	IND_SATURATION	-	R	Signal indicates whether the accumulate-and-dump decimation filters have saturated at some point since the last read. If saturation occurs the DEC_SHIFT can be adjusted. The status flag is cleared when reading the GRDEC register.
11:10	DEC_SHIFT[1:0]	0	R/W	Controls extra shifts in decimation, for extra precision. Decimation shift value: 2: -2 3: -1 0: 0 1: 1
9:8	CHANNEL_DEC[1:0]	0	R/W	Selects channel filter bandwidth. 00: 1 MHz (used for 1Mbps and 250 kbps datarates) 01: 500 kHz (used for 10 kbps data rate) 01: 250 kHz 11: 125 kHz
7:0	DEC_VAL[7:0]	0	R/W	In combination with CHANNEL_DEC[1:0], DEC_VAL[7:0] is used to program the data rate. See page 40 for a description.

PKTSTATUS (0x22) - Packet Mode Status

Bit	Field Name	Reset	R/W	Description
15:11	-	0	W0	Reserved, write as 0.
10	SYNC_WORD_RECEIVED	0	R	Indicates that the currently configured sync word has been received since RX was turned on.
9	CRC_OK	-	R	Indicates that the two next bytes available to be read from the FIFO equal the CRC16 calculated over the bytes already read from the FIFO.
8	-	0	R	Reserved for future use.
7:0	-	-	R	Reserved for future use.

INT (0x23) - Interrupt Register

Bit	Field Name	Reset	R/W	Description
15:8	-	0	W0	Reserved, write as 0.
7	-	0	R/W	Reserved.
6	PKT_POLARITY	0	R/W	Polarity of the PKT signal.
5	FIFO_POLARITY	0	R/W	Polarity of the FIFO signal. See Figure 10 for details.
4:0	FIFO_THRESHOLD[4:0]	30	R/W	The FIFO pin signals that the 32 bytes data FIFO is near empty in TX or near full in RX. The threshold is used as follows: # bytes in FIFO >= FIFO_THRESHOLD in RX # bytes in FIFO <= 32 - FIFO_THRESHOLD in TX.

Reserved (0x24) – Reserved regiser

Bit	Field Name	Reset	R/W	Description
15:14	RES[15:14]	0	W0	Reserved for future use.
13:10	RES[13:10]	8	R/W	Reserved for future use.
9:7	RES[9:7]	0	R/W	Reserved for future use.
6:0	RES[6:0]	80	R/W	Reserved for future use.

Reserved (0x25) – Reserved register

Bit	Field Name	Reset	R/W	Description
15:12	RES[15:12]	0	W0	Reserved for future use.
11:0	RES[11:0]	0	R/W	Reserved for future use.

Reserved (0x26) – Reserved register

Bit	Field Name	Reset	R/W	Description
15:10	RES[15:10]	8	R/W	Reserved for future use.
9:0	RES[9:0]	0	R/W	Reserved for future use.

Reserved (0x27) – Reserved register

Bit	Field Name	Reset	R/W	Description
15:8	RES[15:8]	-	R	Reserved for future use.
7:3	RES[7:3]	0	R/W	Reserved for future use.
2:0	RES[2:0]	6	R/W	Reserved for future use.

Reserved (0x28) – Reserved register

Bit	Field Name	Reset	R/W	Description
15	RES[15]	0	R/W	Reserved for future use.
14:13	RES[14:13]	2	R/W	Reserved for future use.
12:7	RES[12:7]	63	R/W	Reserved for future use.
6:0	RES[6:0]	0	R/W	Reserved for future use.

Reserved (0x29) – Reserved Register

Bit	Field Name	Reset	R/W	Description
15:8	RES[15:8]	0	W0	Reserved for future use.
7:3	RES[7:3]	0	R/W	Reserved for future use.
2:0	RES[2:0]	3	R/W	Reserved for future use.

Reserved (0x2A) – Reserved Register

Bit	Field Name	Reset	R/W	Description
15:11	RES[15:11]	0	W0	Reserved for future use.
10	RES[10]	0	R/W	Reserved for future use.
9:0	RES[9:0]	512	R/W	Reserved for future use.

Reserved (0x2B) – Reserved register

Bit	Field Name	Reset	R/W	Description
15:14	RES[15:14]	0	W0	Reserved for future use.
13	RES[13]	-	R/W	Reserved for future use.
12	RES[12]	-	R	Reserved for future use.
11:0	RES[11:0]	1953	R	Reserved for future use.

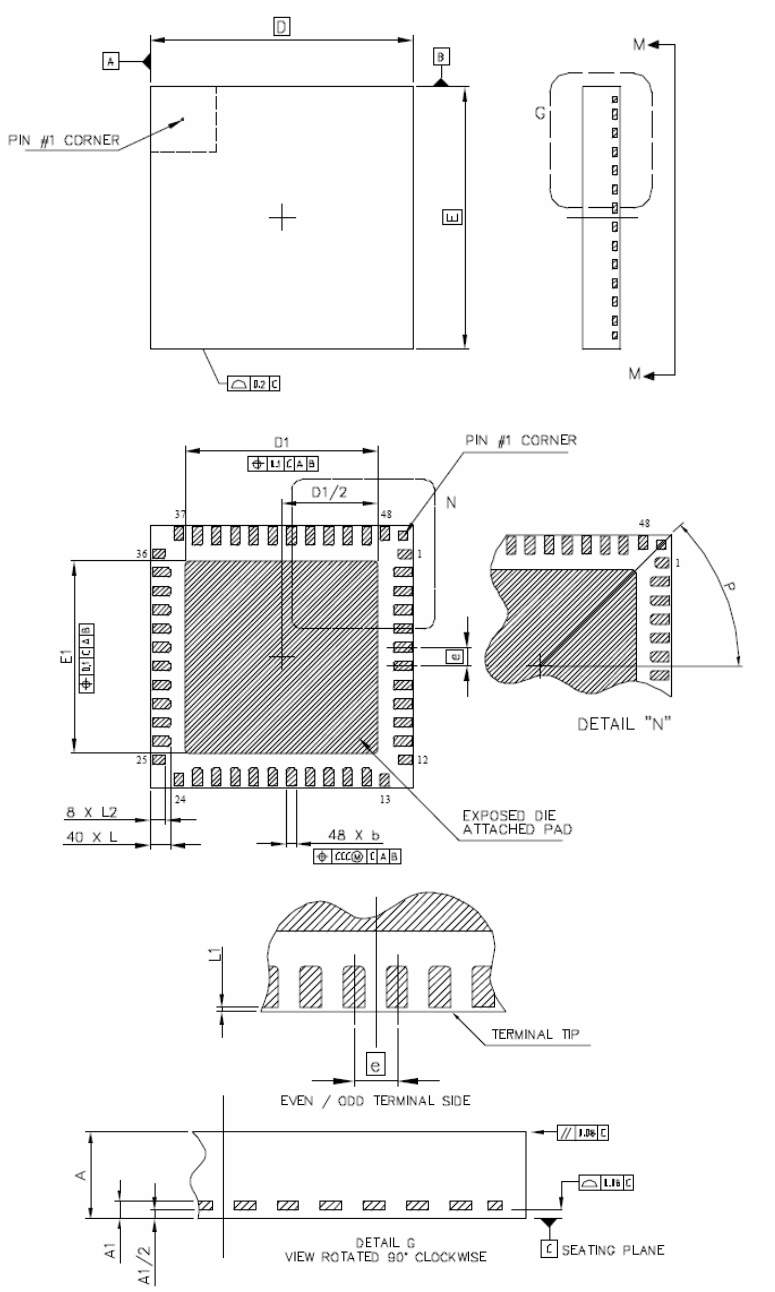
SYNCL (0x2C) - Sync Word, Lower 16 Bit

Bit	Field Name	Reset	R/W	Description
15:0	SYNCWORD[15:0]	0XDA26	R/W	Synchronisation word, lower 16 bit. The default synchronization word of 0XD391DA26 has very good DC, autocorrelation, and bit-run properties for all synchronization word lengths.

SYNCH (0x2D) - Sync Word, Upper 16 Bit

Bit	Field Name	Reset	R/W	Description
15:0	SYNCWORD[31:16]	0XD391	R/W	Synchronisation word, upper 16 bit.

50 Package Description (QFN48)

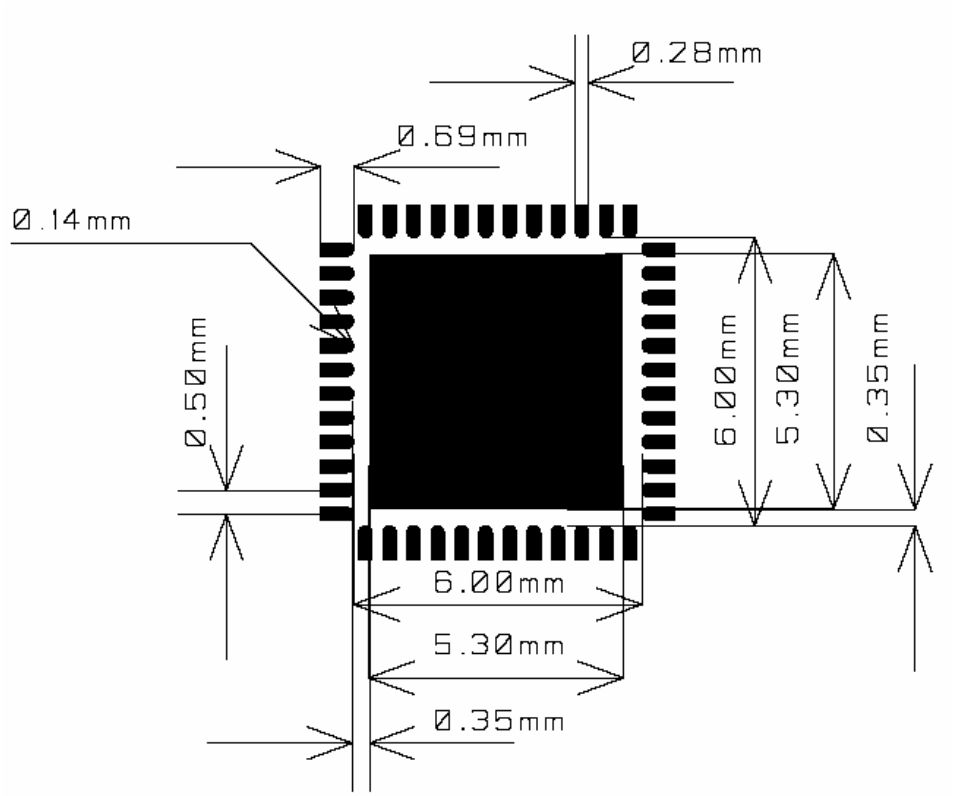


Note: The figure is an illustration only and not to scale.

Quad Flat Pack - No Lead Package (QFN)												
		A	A1	b	D	E	D1	E1	e	L	L1	L2
QFN 48	Min	0.8		0.18			5.04	5.04		0.43		0.30
			0.203	0.25	7.0	7.0			0.5	0.53		0.40
	Max	1.0		0.30			5.24	5.24		0.63	0.1	0.50
The overall package height is 0.9 +/ 0.1 mm. All dimensions in mm												

The package is compliant to JEDEC standard MO-220.

51 Recommended layout for package (QFN48)



Note: The figure is an illustration only and not to scale. There are nine 14 mil diameter via holes distributed symmetrically in the ground pad under the package. See also the CC2400EM reference design.

52 Package Thermal Properties

Thermal resistance	
Air velocity [m/s]	0
Rth,j-a [K/W]	25.6

53 Soldering Information

Recommended soldering profile for both standard leaded packages and Pb-free packages is according to IPC/JEDEC J-STD-020B, July 2002.

54 IC marking

Note: Please submit the entire marking information when contacting Chipcon technical support about chip-related issues, not just the date code.

Example of QFN 48 standard leaded assembly



0440 is assembly year and week no.
XAA is lot code

Example of QFN 48 RoHS compliant Pb-free assembly



A is to identify RoHS compliant Pb-free assembly
4 is to identify year 2004
40 is week no
XAA is lot code

55 Plastic Tube Specification

QFN 7x7 mm antistatic tube.

Tube Specification				
Package	Tube Width	Tube Height	Tube Length	Units per Tube
QFN 48	8.5 ± 0.2 mm	2.2 +0.2/-0.1 mm	315 ± 1.25 mm	43

56 Carrier Tape and Reel Specification

Carrier tape and reel is in accordance with EIA Specification 481.

Tape and Reel Specification					
Package	Tape Width	Component Pitch	Hole Pitch	Reel Diameter	Units per Reel
QFN 48	16 mm	12 mm	4 mm	13 inch	4000

57 Ordering Information

Ordering part number		Description	MOQ
1170	CC2400-STB1	CC2400, QFN48 package, standard leaded assembly, tubes with 43 pcs per tube, 2.4 GHz RF transceiver.	43
1096	CC2400-STR1	CC2400, QFN48 package, standard leaded assembly, T&R with 4000 pcs per reel, 2.4 GHz RF transceiver.	4,000
1139	CC2400-RTB1	CC2400, QFN48 package, RoHS compliant Pb-free assembly, tubes with 43 pcs per tube, 2.4 GHz RF transceiver.	43
1140	CC2400-RTR1	CC2400, QFN48 package, RoHS compliant Pb-free assembly,with 4000/T&R per reel, 2.4 GHz RF transceiver.	4,000
10031	CC2400DK	CC2400DK Development kit	1
10041	CC2400DBK	CC2400DBK, Demonstration Board Kit	1
1097	CC2400SK	**CC2400** QFN48 package, standard leaded assembly, **(5 pcs.)**	1
1162	CC2400SK RoHS	**CC2400 QFN48 package, RoHS compliant Pb-free assembly, 5 pcs.**	1

MOQ = Minimum Order Quantity
T&R = tape and reel

58 General Information

58.1 Document History

Revision	Date	Description/Changes
1.5	2006-03-20	Removed QLP information
1.4	2006-01-16	Address information and ordering information have been updated.
1.3	2004-10-20	Various clarifications. Added recommended PCB footprint. Added package height. Added radio control state diagram with state ID numbers. Added information about EN 300 328 and EN 300 440. Added AFC, RSSI settling time and 20 dB bandwidth to electrical specifications. Electrical specifications updated. Bit 5 of the STATUS register has been set as reserved; see Errata Note 003 for details. RSSI and carrier sense value calculation clarified and corrected. Added graphs showing typical current consumption, sensitivity and output power as function of temperature Clarified packet handling and data buffering sections. Description of the FSMTC register corrected. Added example calculation to AFC description. Updated ordering information with RoHS-compliant Pb-free versions. “CRC-16” replaced with “CRC”. Reorganized electrical specification section. Added chapter numbering. Added QFN 48 package description. Added IC marking description. RSSI value calculation corrected.
1.2	2004-02-05	Various clarifications. Single-ended operation of the chip has been removed. Corrected value of DEC_VAL for 250 kbps data rate. Added information that the core supply cannot be switched off while I/O supply is still on. Electrical specification updated. Selectivity in-band is now measured using a FSK modulated interferer. Added note that choice of crystal package strongly affects price. Added section about low-latency systems. Added graph of sensitivity vs. frequency offset. Added plot of modulated spectrum. Added more information about AFC. Added information about using an external PA. Operating conditions put into separate table.
1.1	2003-10-02	Removed 32 kHz oscillator. Added L71 to application circuit. Modified component names in application circuit to match reference design. Corrected E2 and D2 package dimensions. Minor corrections and editorial changes. Added recommendation on length of preamble when using GFSK. Added Manchester data encoding.
1.0	2003-09-10	Initial release.

58.2 Product Status Definitions

Data Sheet Identification	Product Status	Definition
Advance Information	Planned or Under Development	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	Engineering Samples and First Production	This data sheet contains preliminary data, and supplementary data will be published at a later date. Chipcon reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
No Identification Noted	Full Production	This data sheet contains the final specifications. Chipcon reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Obsolete	Not In Production	This data sheet contains specifications on a product that has been discontinued by Chipcon. The data sheet is printed for reference information only.

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59 Address Information

Web site: http://www.chipcon.com
E-mail: wireless@chipcon.com
Technical Support Email: support@chipcon.com
Technical Support Hotline: +47 22 95 85 45

Headquarters:

Chipcon AS
Gaustadalléen 21
N-0349 Oslo
NORWAY
Tel: +47 22 95 85 44
Fax: +47 22 95 85 46
E-mail: wireless@chipcon.com

US Offices:

Chipcon Inc., Western US Sales Office
1455 Frazee Road, Suite 800
San Diego, CA 92108
USA
Tel: +1 619 542 1200
Fax: +1 619 542 1222
Email: ussales@chipcon.com

Chipcon Inc., Eastern US Sales Office
35 Pinehurst Avenue
Nashua, New Hampshire, 03062
USA
Tel: +1 603 888 1326
Fax: +1 603 888 4239
Email: eastUSsales@chipcon.com

Sales Office Germany:

Chipcon AS
Riedberghof 3
D-74379 Ingersheim
GERMANY
Tel: +49 7142 9156815
Fax: +49 7142 9156818
Email: Germanysales@chipcon.com

Sales Office Asia:

Chipcon AS
Unit 503, 5/F
Silvercord Tower 2, 30 Canton Road
Tsimshatsui
HONG KONG
Tel: +852 3519 6226
Fax: +852 3519 6520
Email:

Asiasales@chipcon.com (China, Hong Kong, Taiwan)

SEAsales@chipcon.com (Korea, South East Asia, India, Australia and New Zealand)

Sales Office Japan

Chipcon AS
#403, Bureau Shinagawa
4-1-6, Konan, Minato-Ku
Tokyo, Zip 108-0075
JAPAN
Tel: +81 3 5783 1082
Fax: +81 3 5783 1083
Email: Japansales@chipcon.com

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