Texas Instruments
Data sheet acquired from Harris Semiconductor
SCHS104C – Revised October 2003

CD40174B Types

CMOS Hex 'D'-Type Flip-Flop

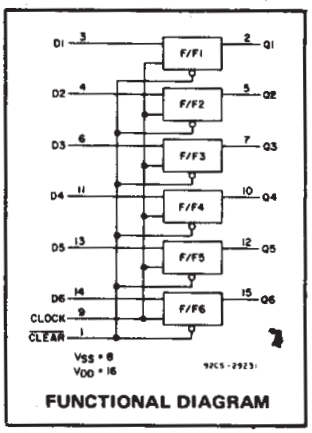
High-Voltage Types (20-Volt Rating)

■ CD40174B consists of six identical 'D'-type flip-flops having independent DATA inputs. The CLOCK and $\overline{\text{CLEAR}}$ inputs are common to all six units. Data is transferred to the Q outputs on the positive-going transition of the clock pulse. All six flip-flops are simultaneously reset by a low level on the $\overline{\text{CLEAR}}$ input.

The CD40174B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, MT, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

Features:

- 5-V, 10-V, and 15-V parametric rating
- Standardized symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package-temperature range): 1 V at V_{DD} = 5 V; 2 V at V_{DD} = 10 V; 2.5 V at V_{DD} = 15 V
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"



FUNCTIONAL DIAGRAM

Applications:

- Shift Registers
- Buffer/Storage Registers
- Pattern Generators

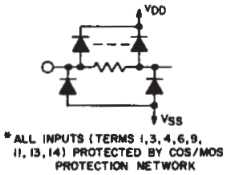
MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
Voltages referenced to V_{SS} Terminal) ..... −0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS ..... −0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −55°C to +100°C 500mW
For T_A = +100°C to +125°C ..... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)..... 100mW
OPERATING-TEMPERATURE RANGE (T_A) .....−55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) .....−65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C

TRUTH TABLE FOR 1 OF 6 FLIP-FLOPS

INPUTS			OUTPUT
CLOCK	DATA	$\overline{\text{CLEAR}}$	Q
⌐⌐	0	1	0
⌐⌐	1	1	1
⌐⌐	X	1	NC
X	X	0	0

1 = High Level X = Don't Care
0 = Low Level NC = No Change



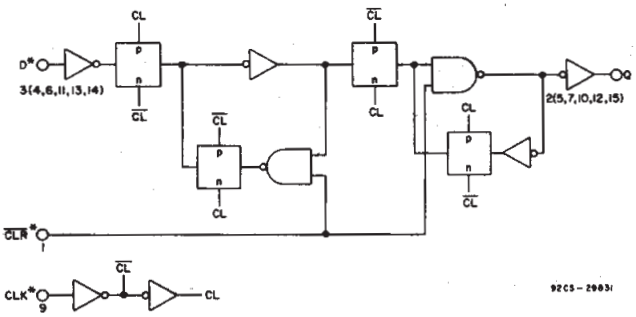


Fig. 1 – Logic diagram (1 of 6 flip-flops).

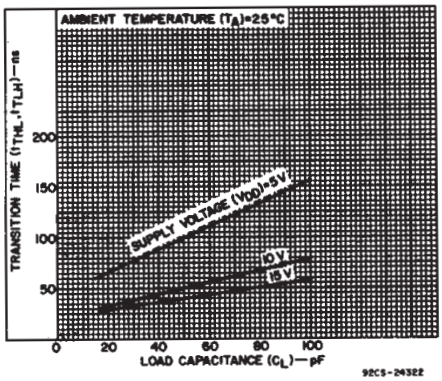
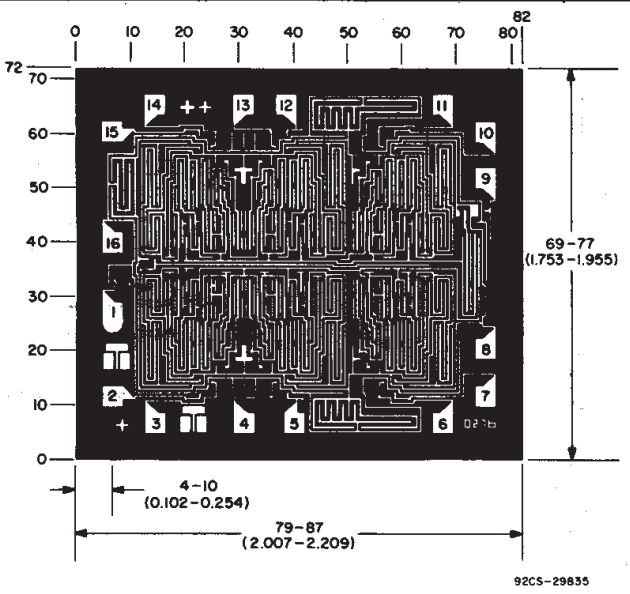


Fig. 2– Typical transition time as a function of load capacitance.

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RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS		UNITS
		Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	–	3	18	V
Data Setup Time, t_{SU}	5	40	–	ns
	10	20	–	
	15	10	–	
Data Hold Time, t_H	5	80	–	ns
	10	40	–	
	15	30	–	
Clock Input Frequency, f_{CL}	5	–	3.5	MHz
	10	dc	6	
	15		8	
Clock Input Rise or Fall Time, t_rCL, t_fCL	5	–	15	μs
	10	–	15	
	15	–	15	
Clock Input Pulse Width, t_{WL}, t_{WH}	5	130	–	ns
	10	60	–	
	15	40	–	
$\overline{\text{Clear}}$ Pulse Width, t_{WL}	5	100	–	ns
	10	50	–	
	15	40	–	
$\overline{\text{Clear}}$ Removal Time, t_{REM}	5	0	–	ns
	10	0	–	
	15	0	–	



Dimensions and pad layout for CD40174BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of −3 mils to +16 mils applicable to the nominal dimensions shown.

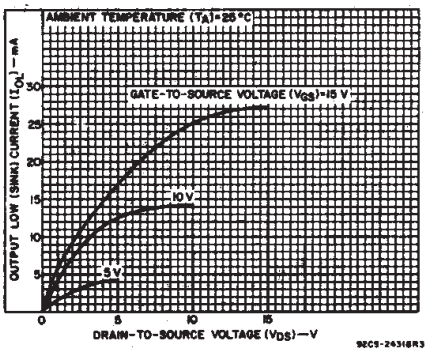


Fig. 3— Typical output low (sink) current characteristics.

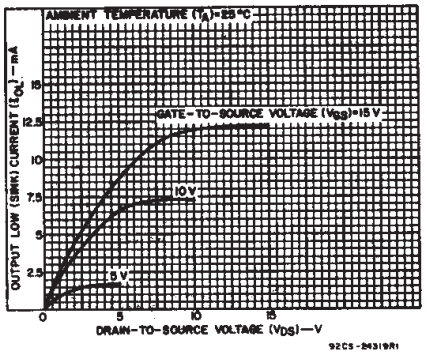


Fig. 4— Minimum output low (sink) current characteristics.

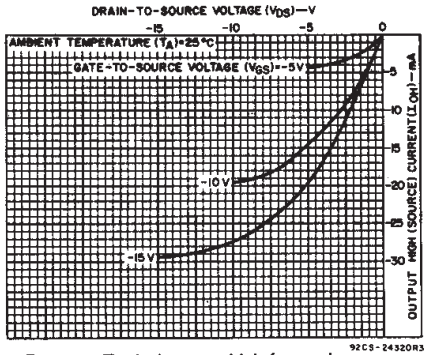


Fig. 5— Typical output high (source) current characteristics.

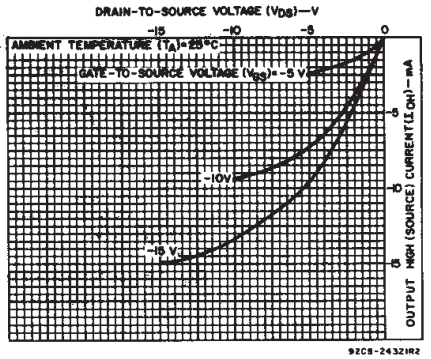


Fig. 6— Minimum output high (source) current characteristics.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	μA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6		
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8		
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–		0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

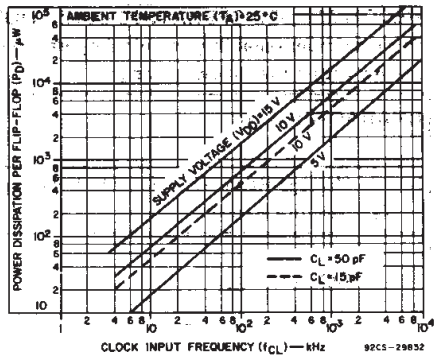


Fig. 7— Typical dynamic power dissipation as a function of CLOCK frequency.

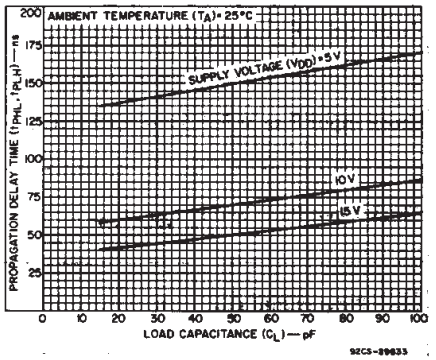


Fig. 8— Typical propagation delay time (CLOCK to OUTPUT) as a function of load capacitance.

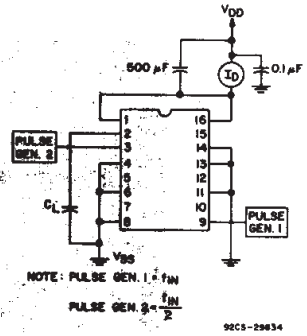


Fig. 9— Dynamic power dissipation test circuit.

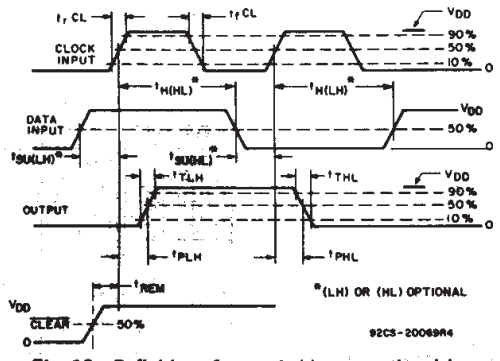


Fig. 10— Definition of setup, hold, propagation delay, and removal times.

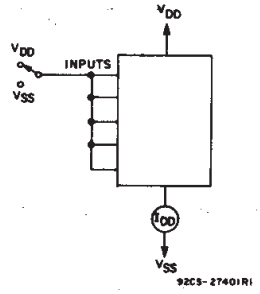


Fig. 11 — Quiescent device current test circuit.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C;
Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS			UNITS
		Min.	Typ.	Max.	
Propagation Delay Time Clock to Output, t_{PHL}, t_{PLH}	5	–	150	300	ns
	10	–	70	140	
	15	–	50	100	
$\overline{\text{Clear}}$ to Output, t_{PHL}	5	–	100	200	ns
	10	–	50	100	
	15	–	40	80	
Transition Time, t_{THL}, t_{TLH}	5	–	100	200	ns
	10	–	50	100	
	15	–	40	80	
Minimum Pulse Width, Clock, t_{WL}, t_{WH}	5	–	65	130	ns
	10	–	30	60	
	15	–	20	40	
$\overline{\text{Clear}}$, t_{WL}	5	–	50	100	ns
	10	–	25	50	
	15	–	20	40	
Minimum Data Setup Time, t_{SU}	5	–	20	40	ns
	10	–	10	20	
	15	–	0	10	
Minimum Data Hold Time, t_H	5	–	40	80	ns
	10	–	20	40	
	15	–	15	30	
Maximum Clock Frequency, f_{CL}	5	3.5	7	–	MHz
	10	6	12	–	
	15	8	16	–	
Maximum Clock Rise or Fall Time, t_rCL, t_fCL	5	15	–	–	μs
	10	15	–	–	
	15	15	–	–	
Input Capacitance, C_{IN} $\overline{\text{Clear}}$	–	–	25	40	pF
All other	–	–	5	7.5	
Minimum $\overline{\text{Clear}}$ Removal Time, t_{REM}	5	–	–40	0	ns
	10	–	–15	0	
	15	–	–10	0	

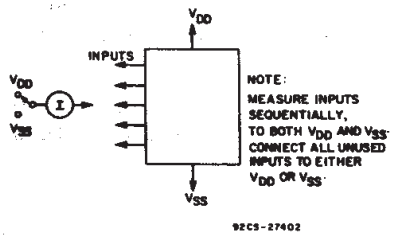


Fig. 12 – Input current test circuit.

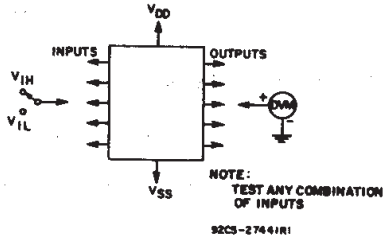
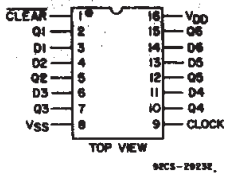


Fig. 13 – Input voltage test circuit.

TERMINAL ASSIGNMENT



PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD40174BE	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD40174BE
CD40174BE.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD40174BE
CD40174BEE4	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD40174BE
CD40174BF	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD40174BF
CD40174BF.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD40174BF
CD40174BF3A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD40174BF3A
CD40174BF3A.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD40174BF3A
CD40174BM	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	CD40174BM
CD40174BM96	NRND	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD40174BM
CD40174BM96.A	NRND	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD40174BM
CD40174BNSR	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD40174B
CD40174BNSR.A	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD40174B
CD40174BPW	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM0174B
CD40174BPW.A	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM0174B

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD40174B, CD40174B-MIL :

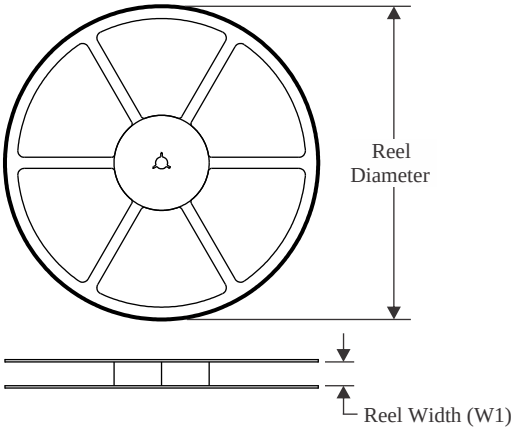
- Catalog : CD40174B
- Military : CD40174B-MIL

NOTE: Qualified Version Definitions:

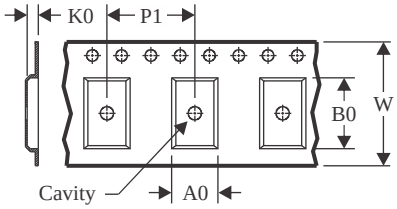
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

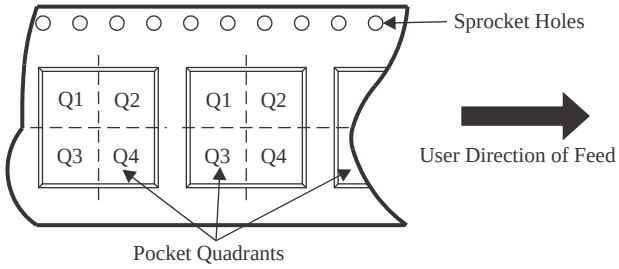


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

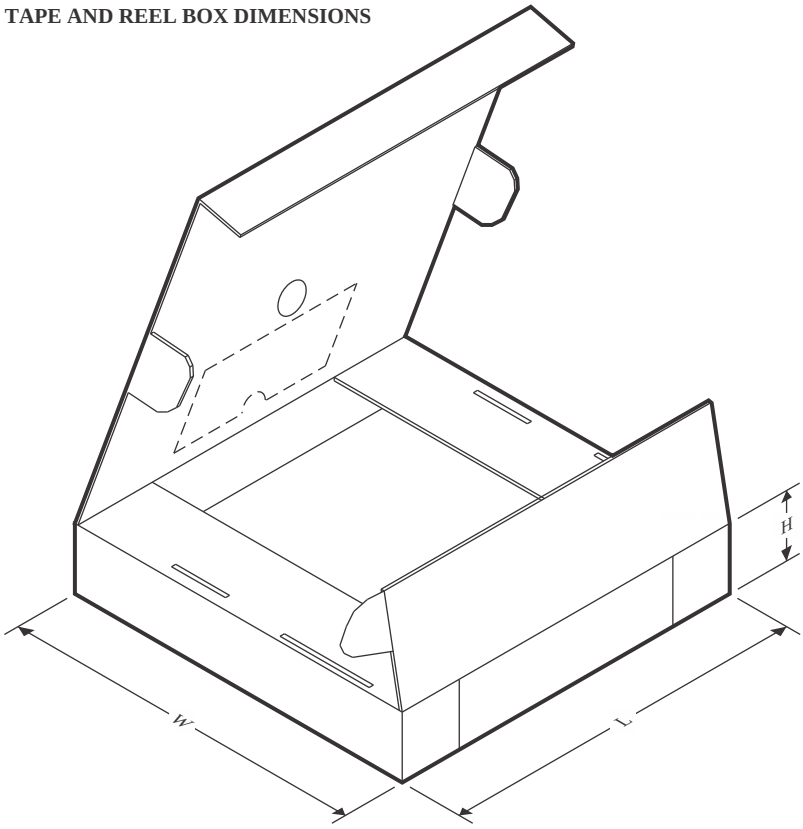
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD40174BM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD40174BNSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1

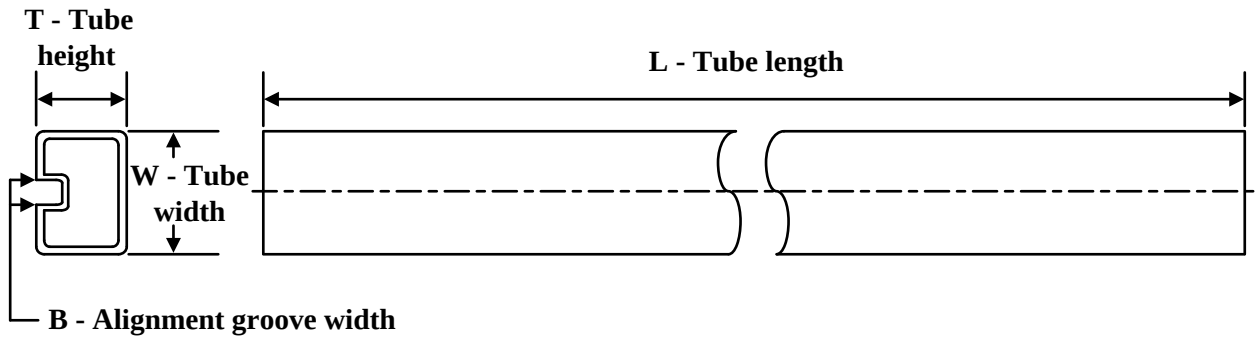
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD40174BM96	SOIC	D	16	2500	353.0	353.0	32.0
CD40174BNSR	SOP	NS	16	2000	353.0	353.0	32.0

TUBE



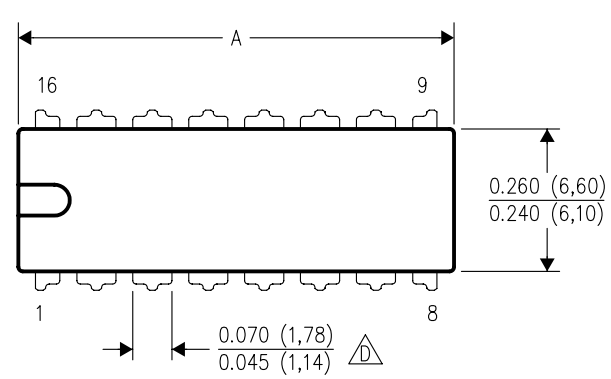
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD40174BE	N	PDIP	16	25	506	13.97	11230	4.32
CD40174BE	N	PDIP	16	25	506	13.97	11230	4.32
CD40174BE.A	N	PDIP	16	25	506	13.97	11230	4.32
CD40174BE.A	N	PDIP	16	25	506	13.97	11230	4.32
CD40174BEE4	N	PDIP	16	25	506	13.97	11230	4.32
CD40174BEE4	N	PDIP	16	25	506	13.97	11230	4.32
CD40174BPW	PW	TSSOP	16	90	530	10.2	3600	3.5
CD40174BPW.A	PW	TSSOP	16	90	530	10.2	3600	3.5

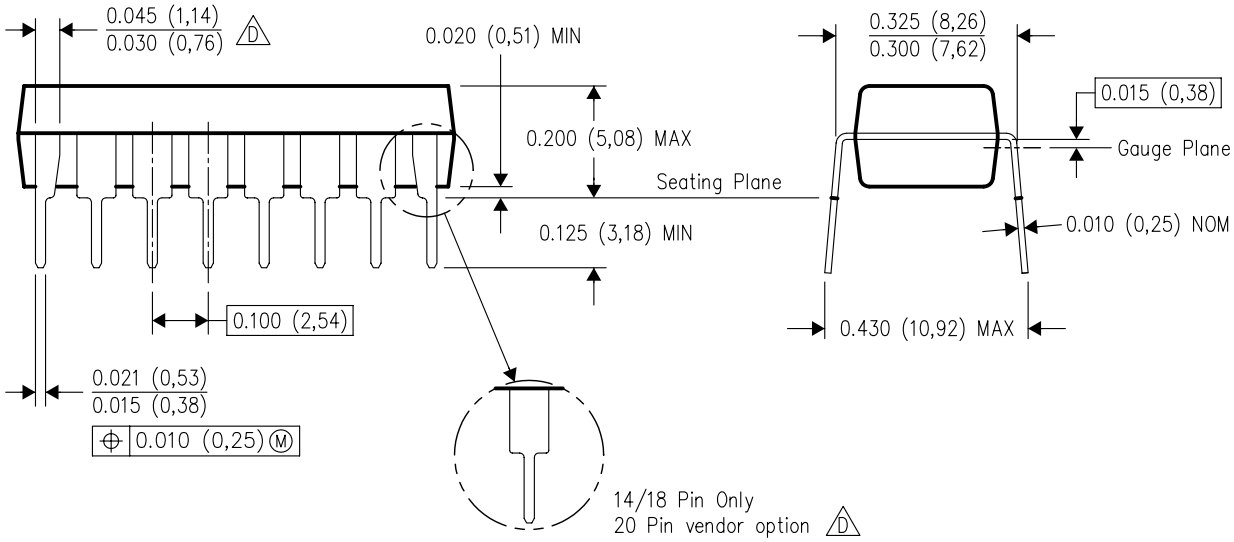
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

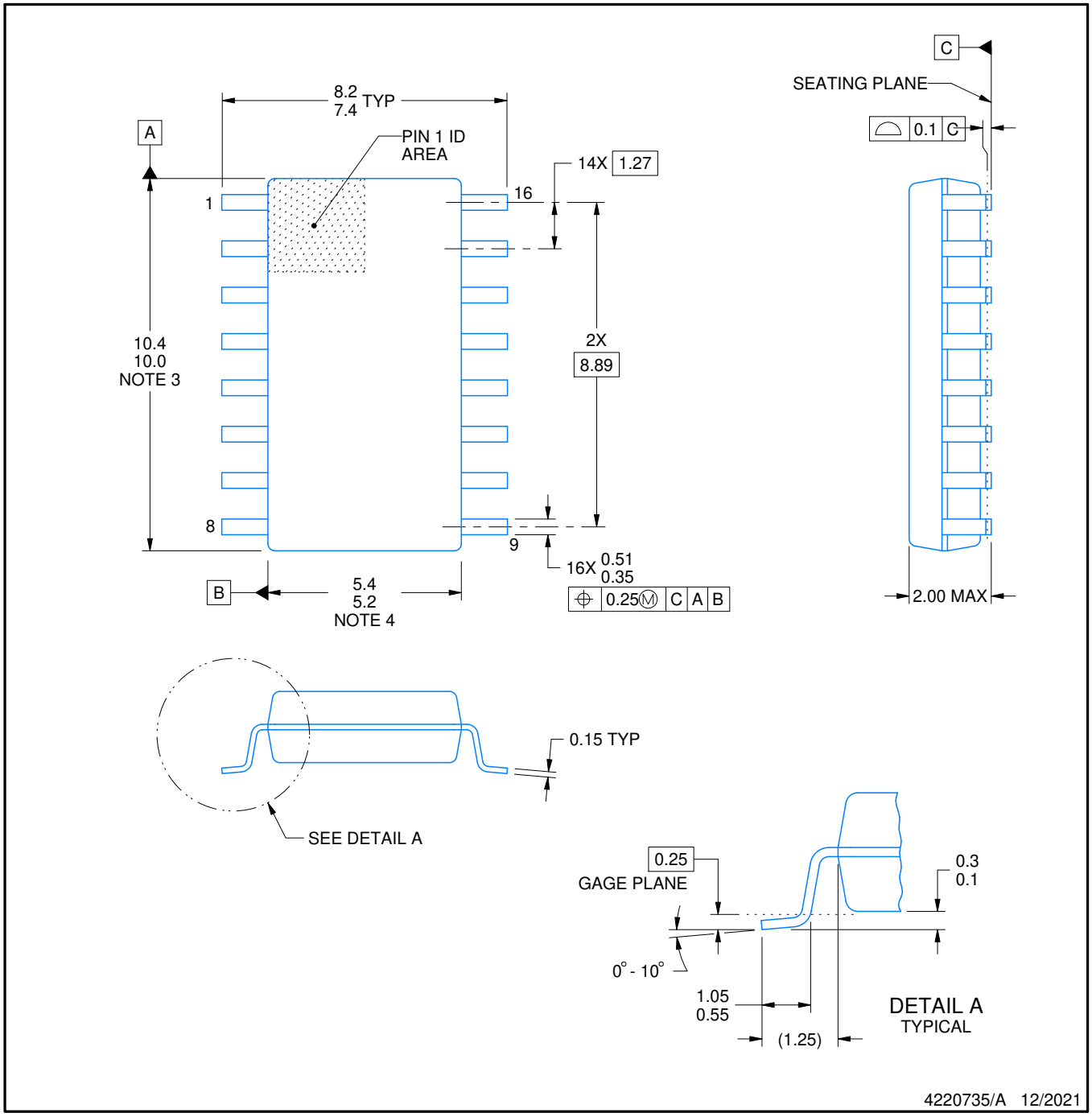


PACKAGE OUTLINE

NS0016A

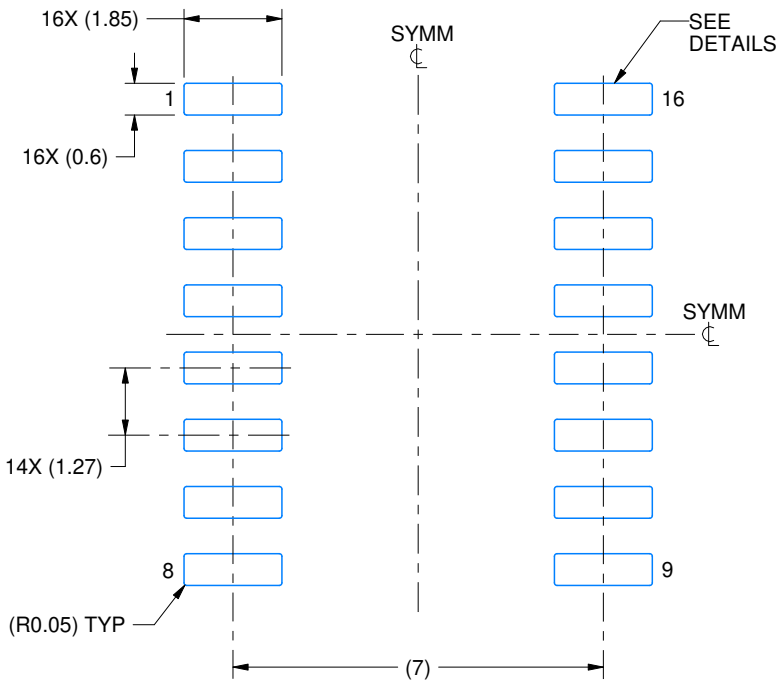
SOP - 2.00 mm max height

SOP

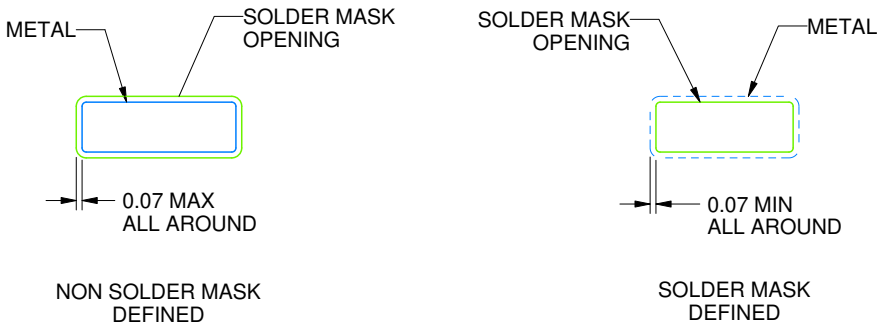


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X

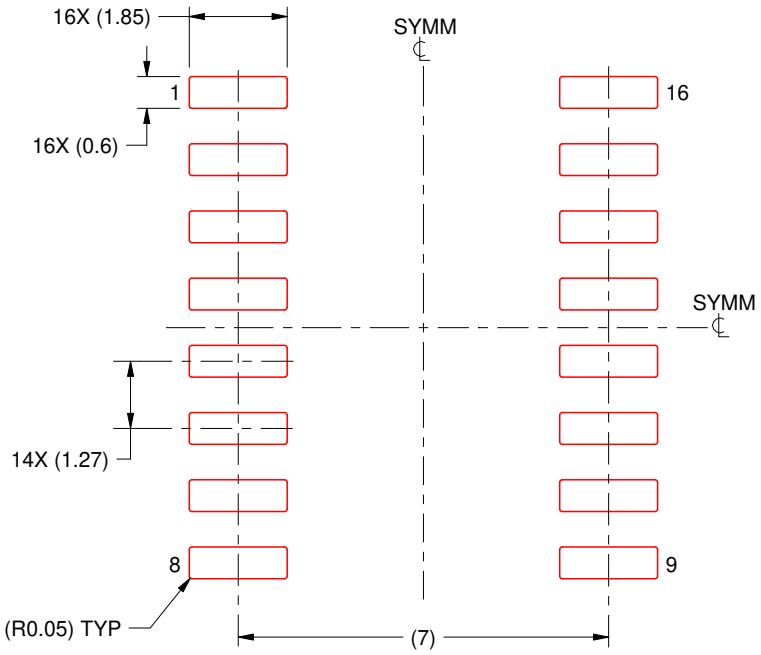


SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



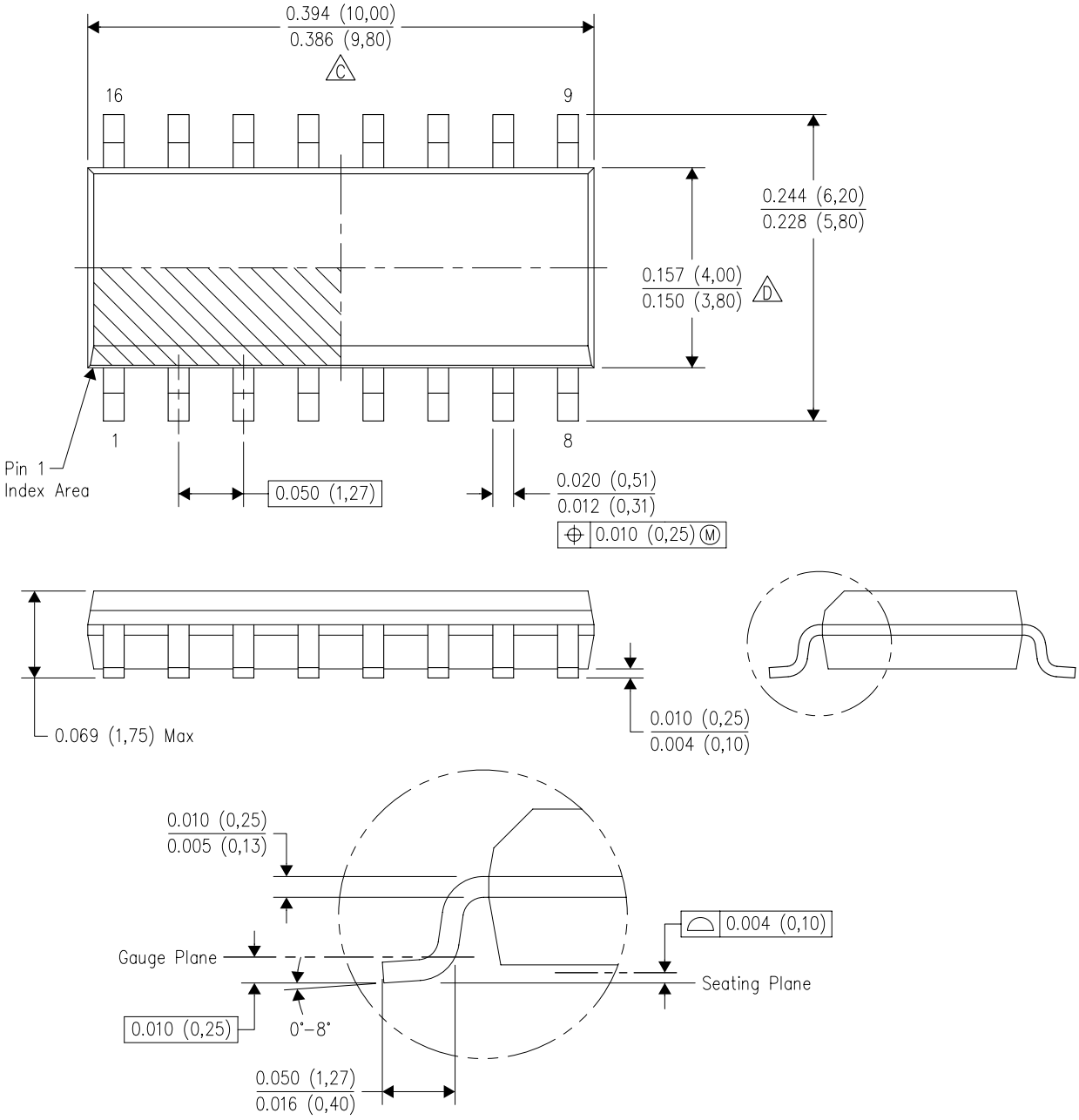
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

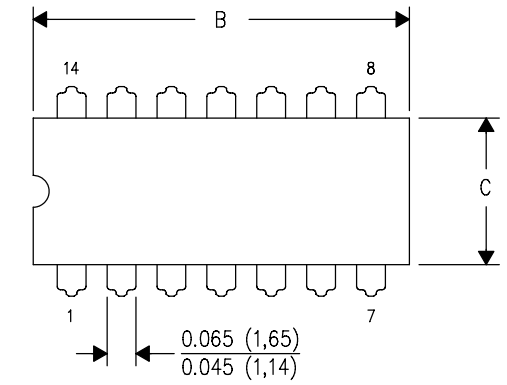


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

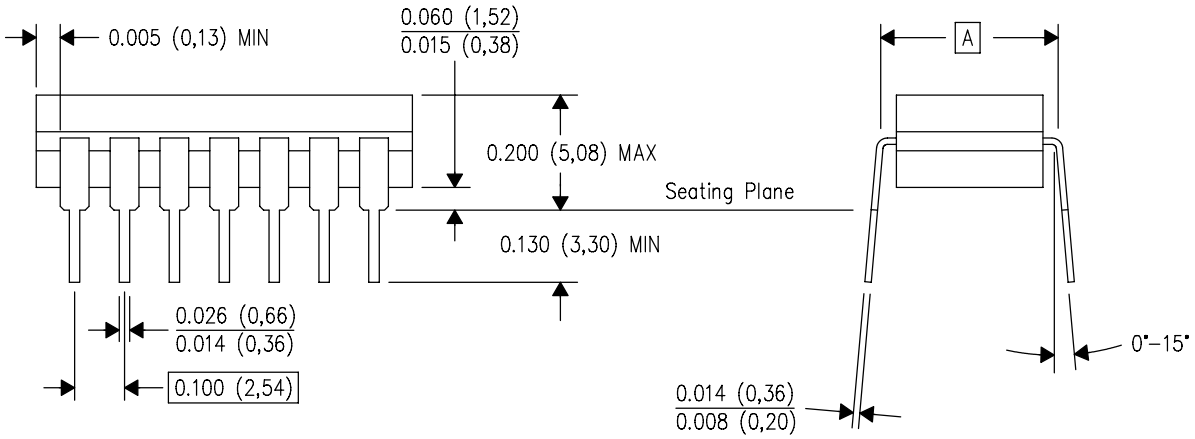
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

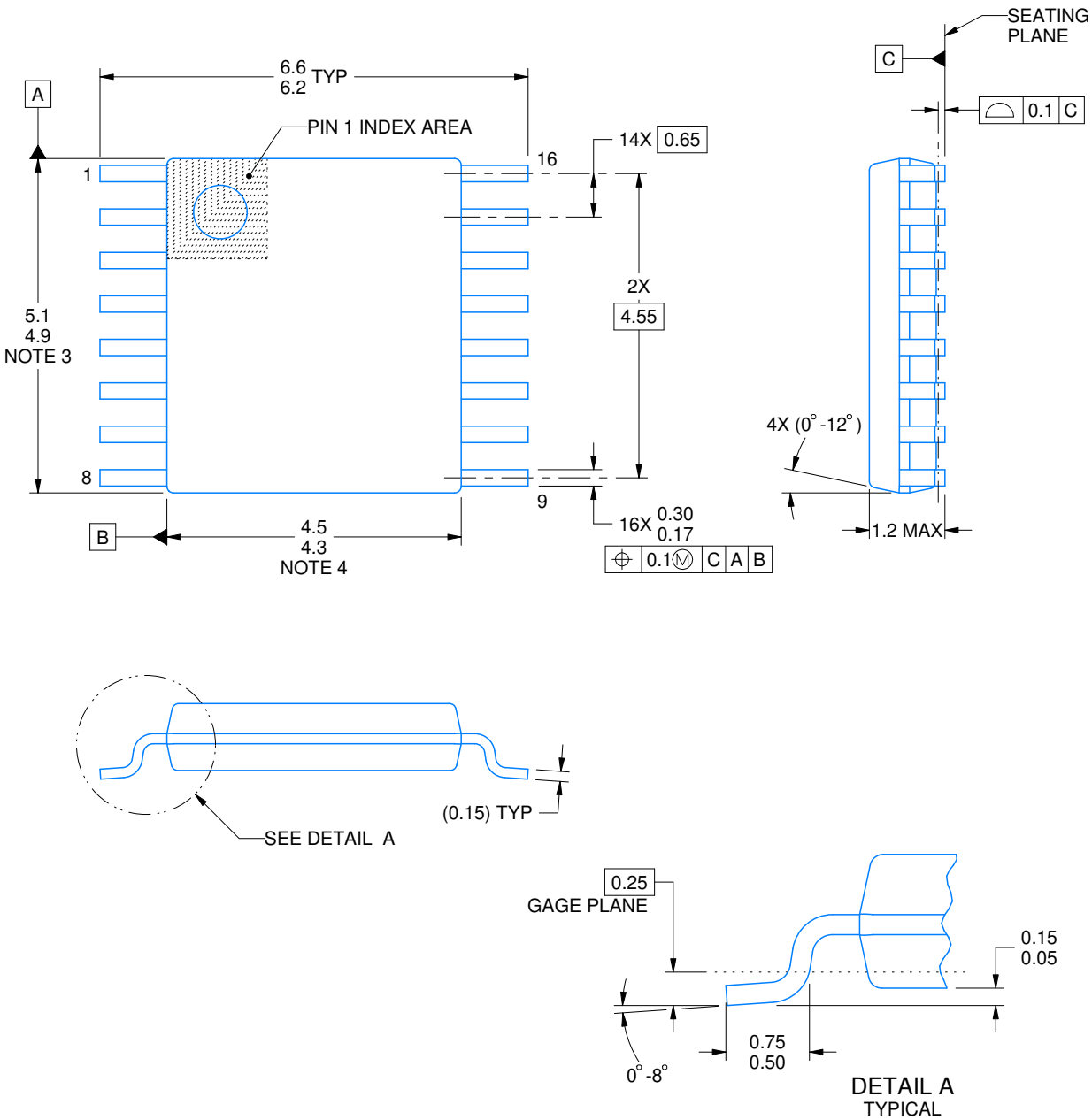
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

PACKAGE OUTLINE

PW0016A

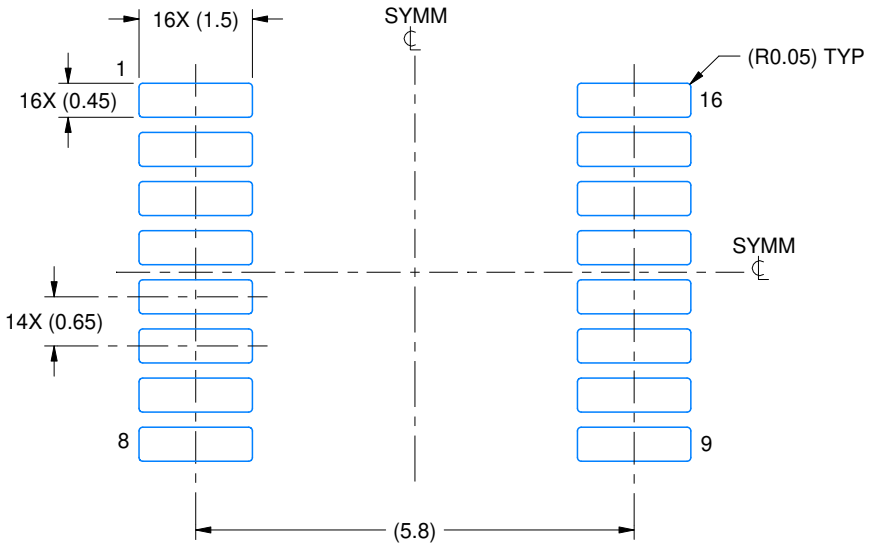
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

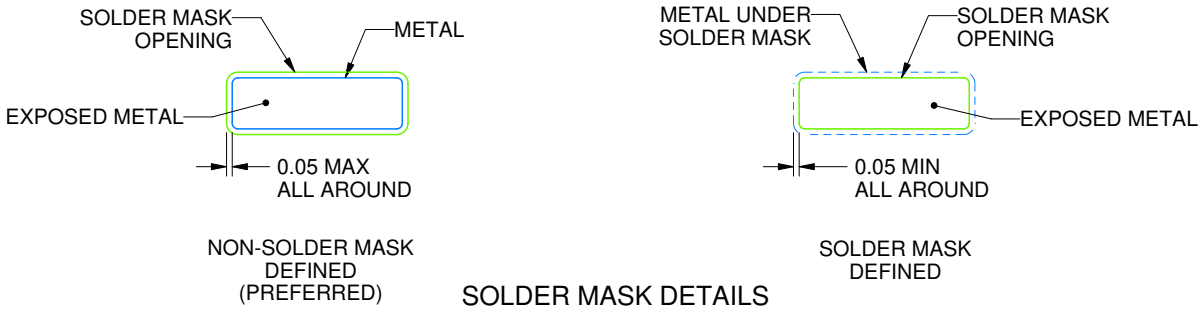


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

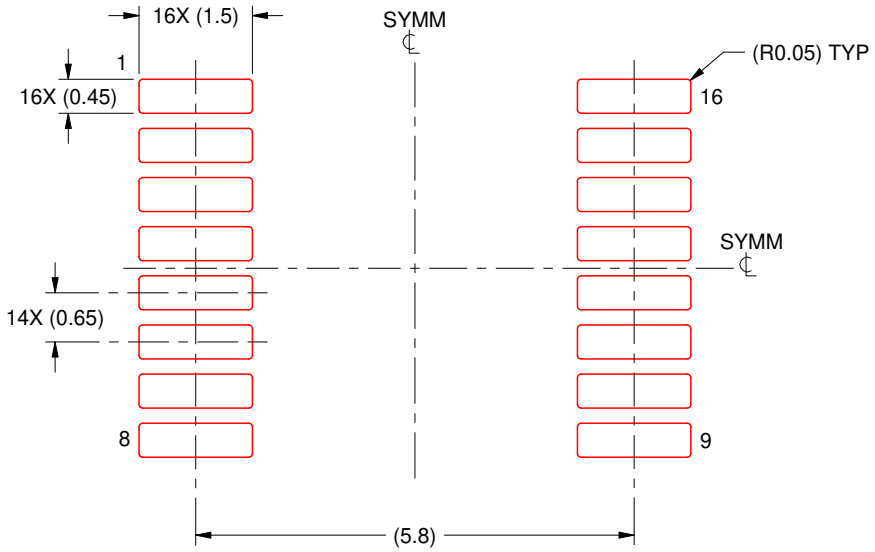


SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025