CD4027B CMOS Dual J-K Flip Flop

1 Features

- Set-reset capability
- Static flip-flop operation – retains state indefinitely with clock level either *high* or *low*
- Medium speed operation – 16 MHz (typical) clock toggle rate at 10 V
- Standardized symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 µA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package-temperature range):
  - 1 V at V_{DD} = 5 V
  - 2 V at V_{DD} = 10 V
  - 2.5 V at V_{DD} = 15 V
- 5 V, 10 V, and 15 V parametric ratings
- Meets all requirements of JEDEC tentative standard No. 138, *standard specifications for description of 'B' series CMOS devices*

2 Applications

- Registers, counters, control circuits

3 Description

CD4027B is a single monolithic chip integrated circuit containing two identical complementary-symmetry J-K flip flops. Each flip-flop has provisions for individual J, K, Set, Reset, and Clock input signals. Buffered Q and $\overline{Q}$ signals are provided as outputs. This input-output arrangement provides for compatibile operation with the RCA-CD4013B dual D-type flip-flop.

The CD4027B is useful in performing control, register, and toggle functions. Logic levels present at the J and K inputs along with internal self-steering control the state of each flip-flop; changes in the flip-flop state are synchronous with the postitive-going transition of the clock pulse. Set and reset functions are independent of the clock and are initiated when a high level signal is present at either the Set or Reset input.

The CD4027B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffice), 16-lead small-outline packages (M, M96, MT, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

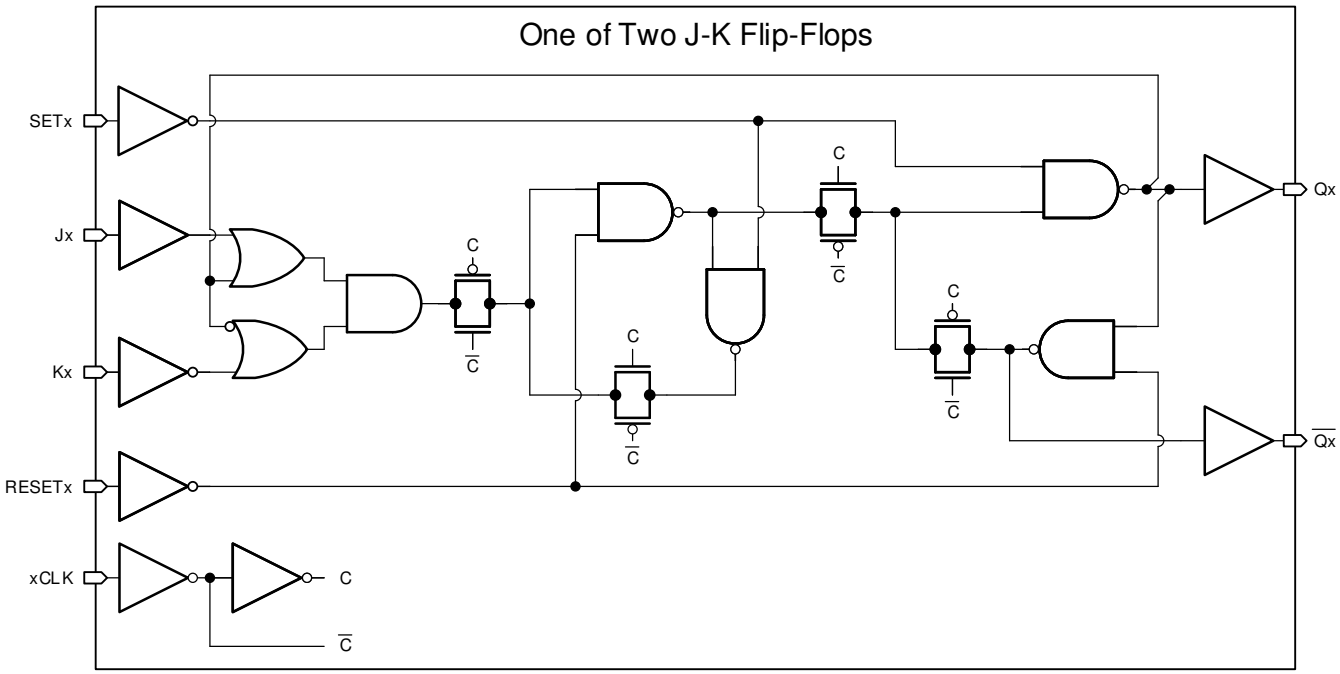


Figure 3-1. Logic Diagram

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (October 2003) to Revision D (July 2021)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1

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5 Pin Configuration and Functions

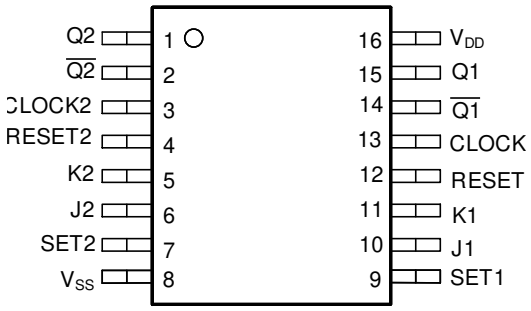


Figure 5-1. Terminal Assignment

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CLOCK1	13	I	Clock input for channel 1
CLOCK2	3	I	Clock input for channel 2
J1	10	I	J input for channel 1
J2	6	I	J input for channel 2
K1	11	I	K input for channel 1
K2	5	I	K input for channel 2
Q1	15	O	Q output for channel 1
$\overline{Q1}$	14	O	Inverted Q output for channel 1
Q2	1	O	Q output for channel 2
$\overline{Q2}$	2	O	Inverted Q output for channel 2
RESET1	12	I	Reset input for channel 1
RESET2	4	I	Reset input for channel 2
SET1	9	I	Set input for channel 1
SET2	7	I	Set input for channel 2
V_{DD}	16	—	Supply
V_{SS}	8	—	Ground

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6 Specifications

6.1 Absolute Maximum Ratings

			MIN	MAX	UNIT
V_{DD}	DC Supply Voltage Range	Voltages referenced to V_{SS} Terminal	–0.5	20	V
All Inputs	Input Voltage Range		–0.5	V_{DD} + 0.5	V
Any One Input	DC Input Current			±10	mA
P_D	Power Dissipation per Package	For T_A = –55°C to + 100°C		500	mW
		For T_A = +100°C to +125°C	12mW/°C	200	mW
	Device Dissipation per Output Transistor	For T_A = Full package-temperature range (all package types)		100	mW
T_A	Operating- Temperature Range		–55	125	°C
T_{stg}	Storage temperature		–65	150	°C
	Lead Temperatur (During Soldering)	At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max		265	°C

6.2 Recommended Operating Conditions

at T_A = 25°C, except as noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC			V_{DD} (V)	LIMITS		UNIT
				ALL PACKAGES		
				MIN	MAX	
	Supply-Voltage Range	For T_A = Full Package Temperature Range		3	18	V
t_S	Data Setup Time		5	200		ns
			10	75		
			15	50		
t_W	Clock Pulse Width		5	140		ns
			10	60		
			15	40		
f_{CL}	Clock Input Frequency (Toggle Mode)		5		3.5	MHz
			10	dc	8	
			15		12	
t_rCL, t_fCL(1)	Clock Rise or Fall Time		5		45	µs
			10		5	
			15		2	
t_W	Set or Reset Pulse Width		5	180		ns
			10	80		
			15	50		

(1) If more than one unite is cascaded in a parallel clocked operation, t_rCL should be made less than or equal to the sum of the fixed propagation delay time at 15 pF and the transitiopn time of the output driving stage for the estimated capacitive load.

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6.3 Static Electrical Characteristics

CHARACTERISTIC	TEST CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNIT
	V_O (V)	V_{IN} (V)	V_{DD} (V)	–55	–40	+85	+125	+25			
								MIN	TYP	MAX	
Quiescent		0, 5	5	1	1	30	30		0.02	1	μa
Device		0, 10	10	2	2	60	60		0.02	2	
Current		0, 15	15	4	4	120	120		0.02	4	
I_{DD} Max.		0, 20	20	20	20	600	600		0.04	20	
Output Low (Sink)	0.4	0, 5	5	0.64	0.61	0.42	0.36	0.51	1		mA
Current	0.5	0, 10	10	1.6	1.5	1.1	0.9	1.3	2.6		
I_{OL} Min.	1.5	0, 15	15	4.2	4	2.8	2.4	3.4	6.8		
Output High	4.6	0, 5	5	–0.64	–0.61	–0.42	–0.36	–0.51	–1		mA
(Source)	2.5	0, 5	5	–2	–1.8	–1.3	–1.15	–1.6	–3.2		
Current	9.5	0, 10	10	–1.6	–1.5	–1.1	–0.9	–1.3	–2.6		
I_{OH} Min.	13.5	0, 15	15	– 4.2	–4	–2.8	–2.4	–3.4	–6.8		
Output Voltage		0, 5	5	0.05					0	0.05	V
Low-Level		0, 10	10	0.05					0	0.05	
V_{OL} Max.		0, 15	15	0.05					0	0.05	
Output Voltage		0, 5	5	4.95				4.95	5		V
High-Level		0, 10	10	9.95				9.95	10		
V_{OH} Min.		0, 15	15	14.95				14.95	15		
Input Low	0,5, 4.5		5	1.5						1.5	V
Voltage	1, 9		10	3						3	
V_{IL} Max.	1.5, 13.5		15	4						4	
Input High	0.5, 4.5		5	3.5				3.5			V
Voltage	1, 9		10	7				7			
V_{IH} Min.	1.5, 13.5		15	11				11			
Input Current, V_{IH} Max.		0, 18	18	±0.1	±0.1	±1	±1		$\pm 10^{-5}$	±0.1	μA

6.4 Dynamic Electrical Characteristics

at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	V_{DD} (V)	LIMITS			UNIT
		ALL PACKAGES			
		MIN	TYP	MAX	
Propagation Delay Time	5		150	300	ns
Clock to Q or $\overline{Q}$ Outputs	10		65	130	
t_{PHL}, t_{PLH}	15		45	90	
Set to Q or Reset to $\overline{Q}$, t_{PLH}	5		150	300	ns
	10		65	130	
	15		45	90	
Set to $\overline{Q}$ or Reset to Q, t_{PHL}	5		200	400	ns
	10		85	170	
	15		60	120	
Transition Time	5		100	200	ns
t_{THL}, t_{TLH}	10		50	100	
	15		40	80	

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6.4 Dynamic Electrical Characteristics (continued)

at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	V_{DD} (V)	LIMITS			UNIT
		ALL PACKAGES			
		MIN	TYP	MAX	
Maximum Clock Input	5	3.5	7		MHz
Frequency (Toggle Mode)(1)	10	8	16		
f_{CL}	15	12	24		
Minimum Clock Pulse Width, t_W	5		70	140	ns
	10		30	60	
	15		20	40	
Minimum Set or Reset Pulse Width, t_W	5		90	180	ns
	10		40	80	
	15		25	50	
Minimum Data Setup Time, t_S	5		100	200	ns
	10		35	75	
	15		25	50	
Clock Input Rise or Fall Time t_{rCL}, t_{fCL}	5			45	µs
	10			5	
	15			2	
Input Capacitance, C_I			5	7.5	pF

(1) Input t_r, t_f = 5 ns

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6.5 Typical Characteristics

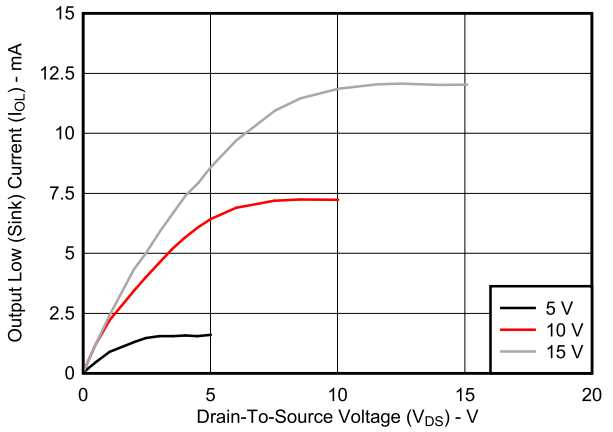


Figure 6-1. Typical Output Low (Sink) Current Characteristics

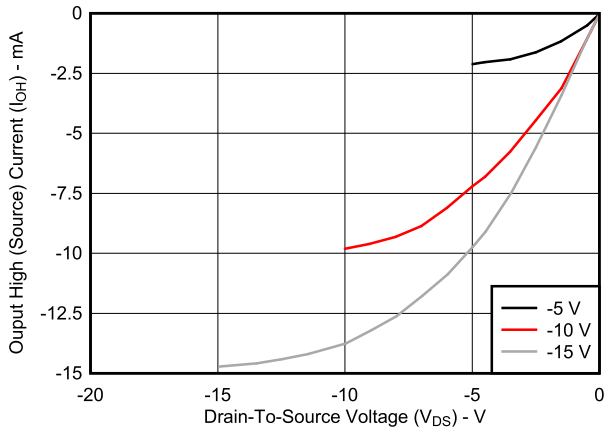


Figure 6-2. Typical Output High (Source) Current Characteristics

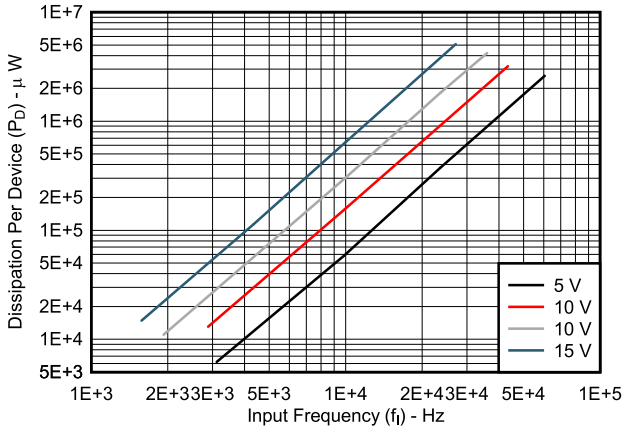


Figure 6-3. Typical Power Dissipation vs Frequency

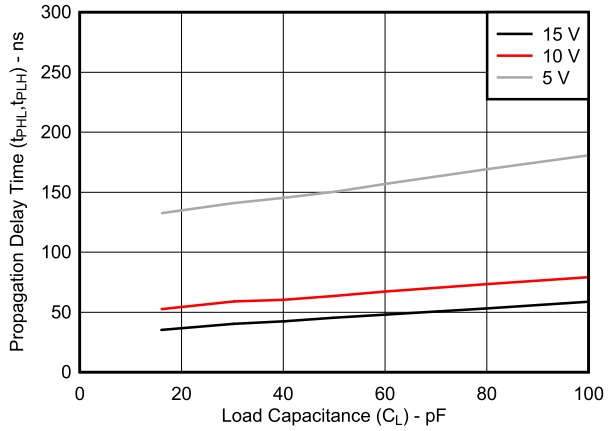


Figure 6-4. Typical Propagation Delay Time vs Load Capacitance (Clock or Set to Q, Clock or Reset to $\overline{Q}$)

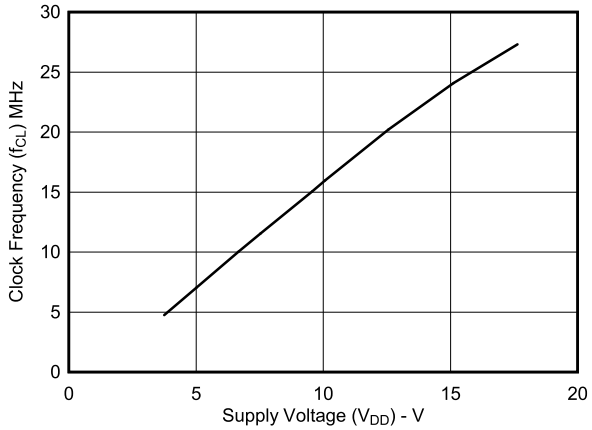


Figure 6-5. Typical Maximum Clock Frequency vs Supply Voltage (Toggle Mode)

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7 Parameter Measurement Information

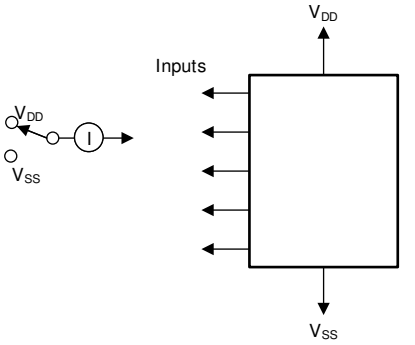


Figure 7-1. Input Current Test Circuit

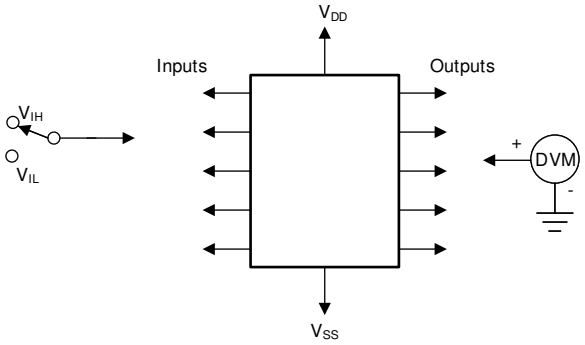


Figure 7-2. Input-Voltage Test Circuit

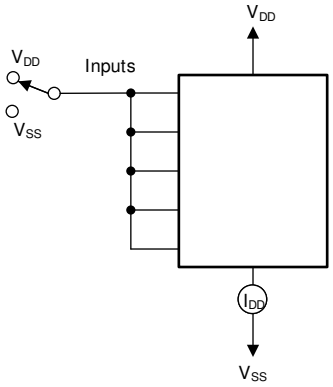
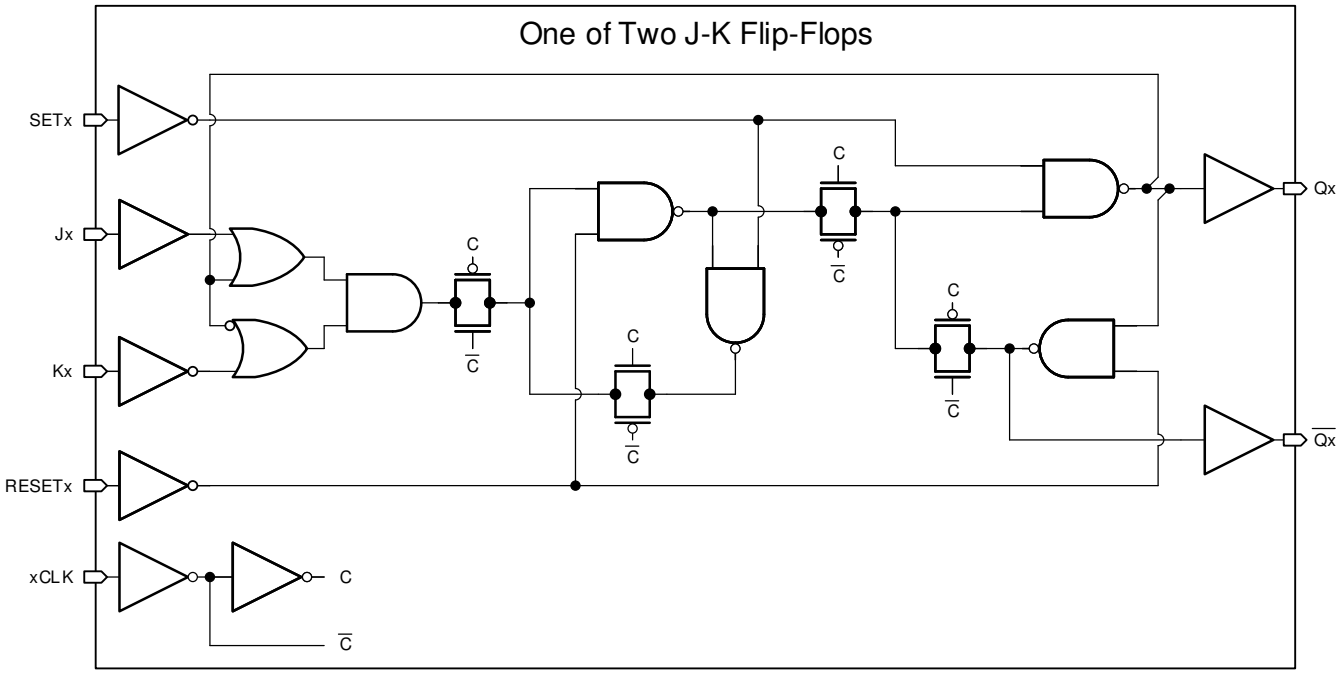


Figure 7-3. Quiescent Device Current Test Circuit

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8 Detailed Description

8.1 Functional Block Diagram



8.2 Device Functional Modes[1]

PRESENT STATE					CL[2]	NEXT STATE	
INPUTS				OUTPUT		OUTPUTS	
J	K	S	R	O	_/‾	O	$\overline{O}$
I	X	O	O	O	_/‾	I	O
X	O	O	O	I	_/‾	I	O
O	X	O	O	O	_/‾	O	I
X	I	O	O	I	_/‾	O	I
X	X	O	O	X	‾_	No change	No change
X	X	I	O	X	X	I	O
X	X	O	I	X	X	O	I
X	X	I	I	X	X	I	I

(1) Logic I = High Level, Logic O = Low Level, X = Do not care
(2) Level change

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9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD4027BE	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4027BE
CD4027BE.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4027BE
CD4027BEE4	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4027BE
CD4027BF	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4027BF
CD4027BF.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4027BF
CD4027BF3A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4027BF3A
CD4027BF3A.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4027BF3A
CD4027BM	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	CD4027BM
CD4027BM96	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4027BM
CD4027BM96.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4027BM
CD4027BM96E4	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4027BM
CD4027BMT	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	CD4027BM
CD4027BNSR	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4027B
CD4027BNSR.A	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4027B
CD4027BPW	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-55 to 125	CM027B
CD4027BPWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM027B
CD4027BPWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM027B
JM38510/05152BEA	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 05152BEA
JM38510/05152BEA.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 05152BEA
M38510/05152BEA	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 05152BEA

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD4027B, CD4027B-MIL :

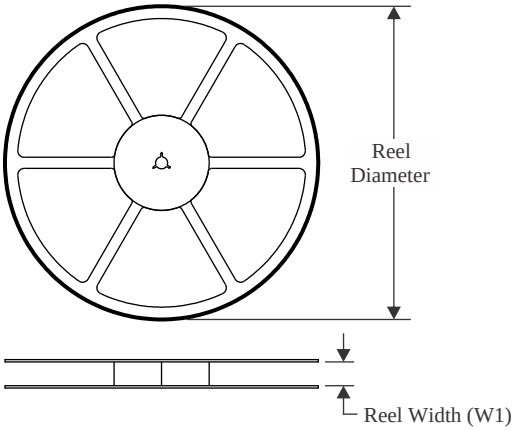
- Catalog : CD4027B
- Military : CD4027B-MIL

NOTE: Qualified Version Definitions:

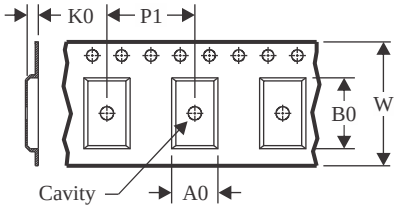
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

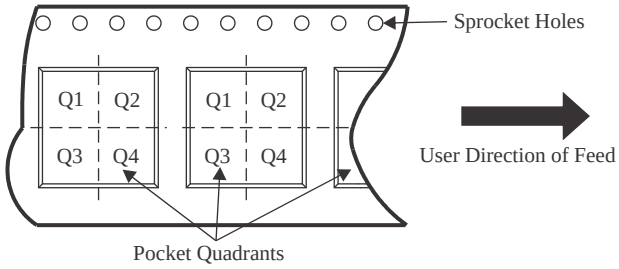


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

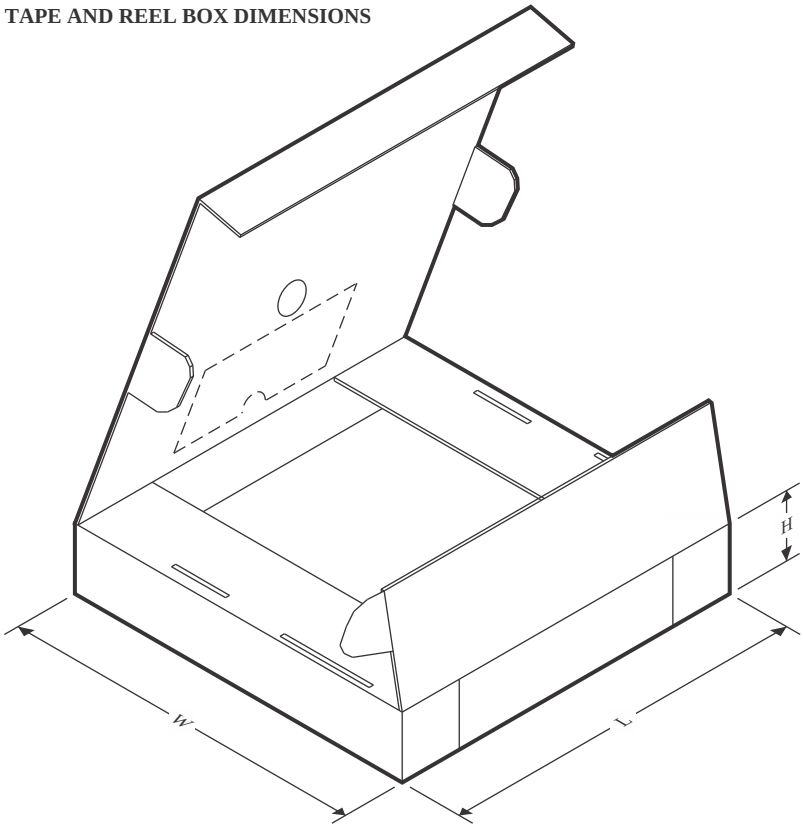
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4027BM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4027BNSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
CD4027BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

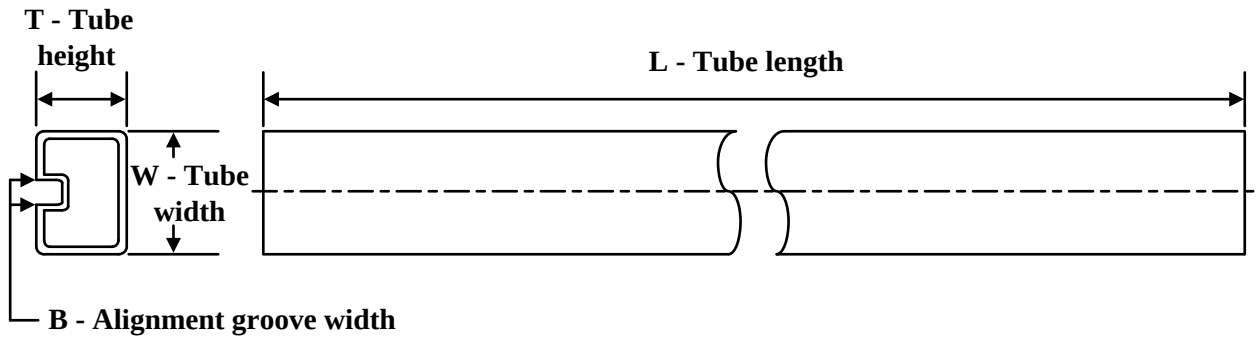
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4027BM96	SOIC	D	16	2500	353.0	353.0	32.0
CD4027BNSR	SOP	NS	16	2000	353.0	353.0	32.0
CD4027BPWR	TSSOP	PW	16	2000	353.0	353.0	32.0

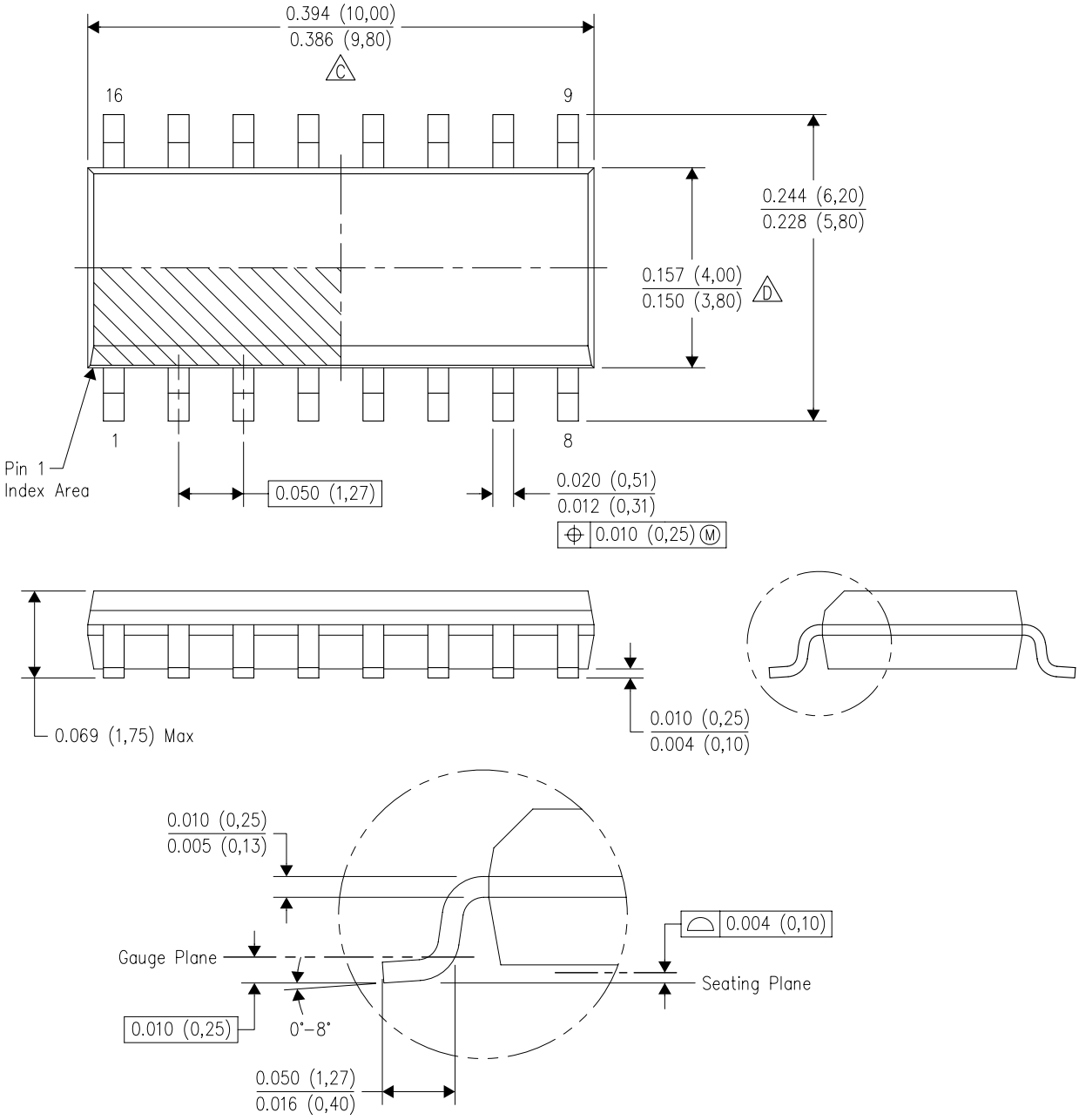
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD4027BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4027BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4027BE.A	N	PDIP	16	25	506	13.97	11230	4.32
CD4027BE.A	N	PDIP	16	25	506	13.97	11230	4.32
CD4027BEE4	N	PDIP	16	25	506	13.97	11230	4.32
CD4027BEE4	N	PDIP	16	25	506	13.97	11230	4.32

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

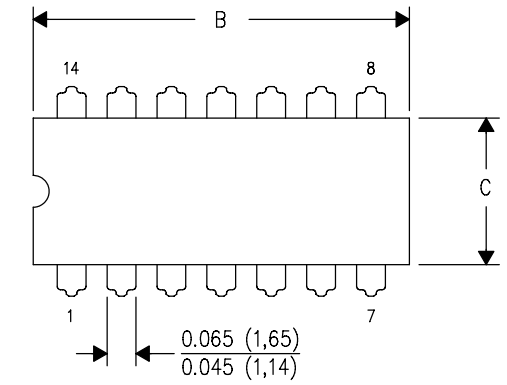


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

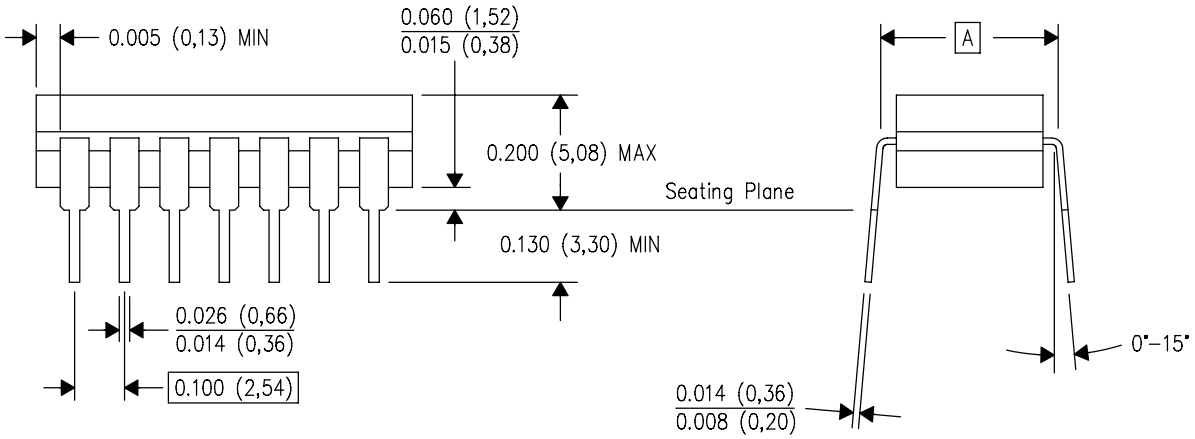
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

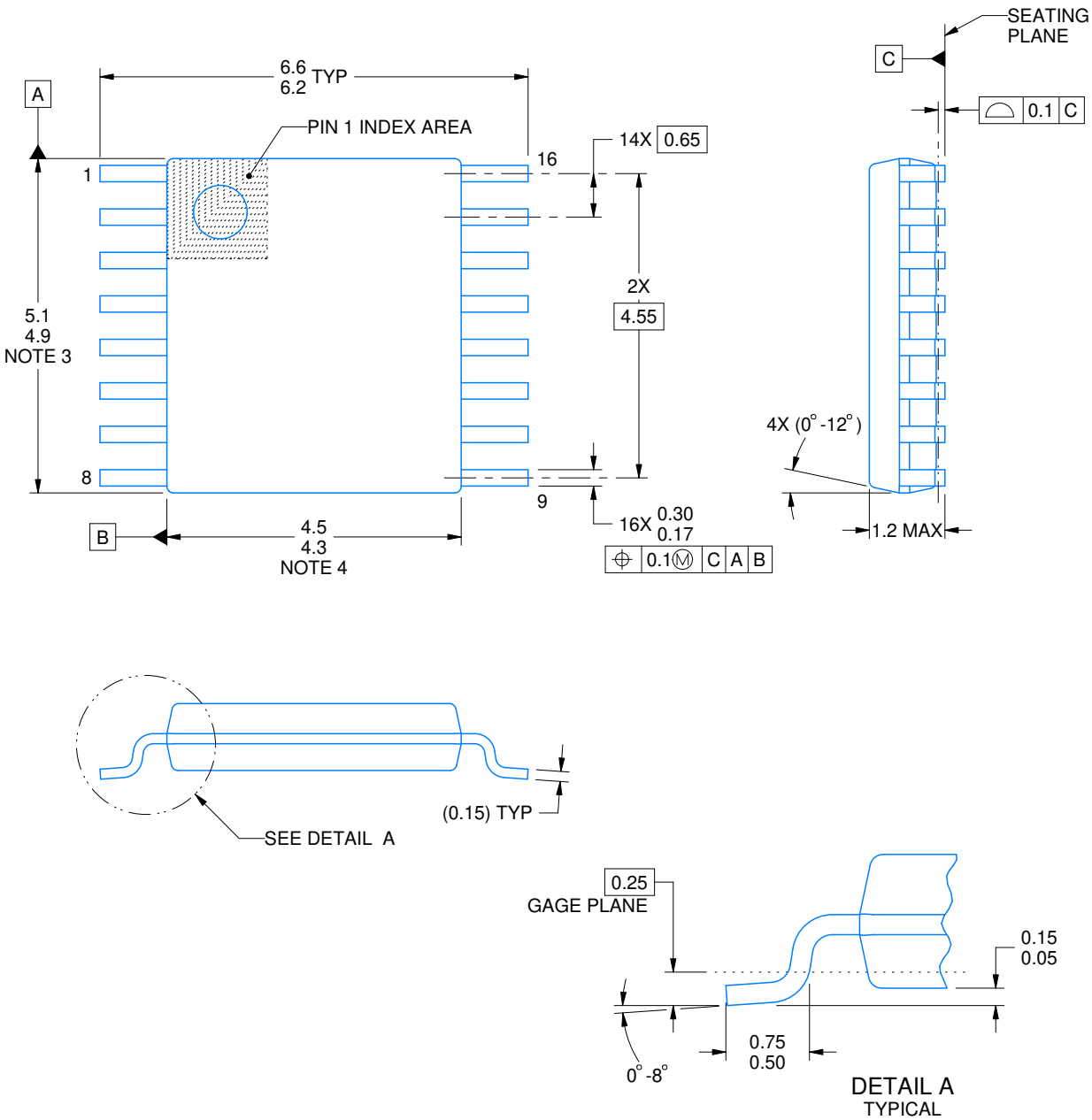
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

PACKAGE OUTLINE

PW0016A

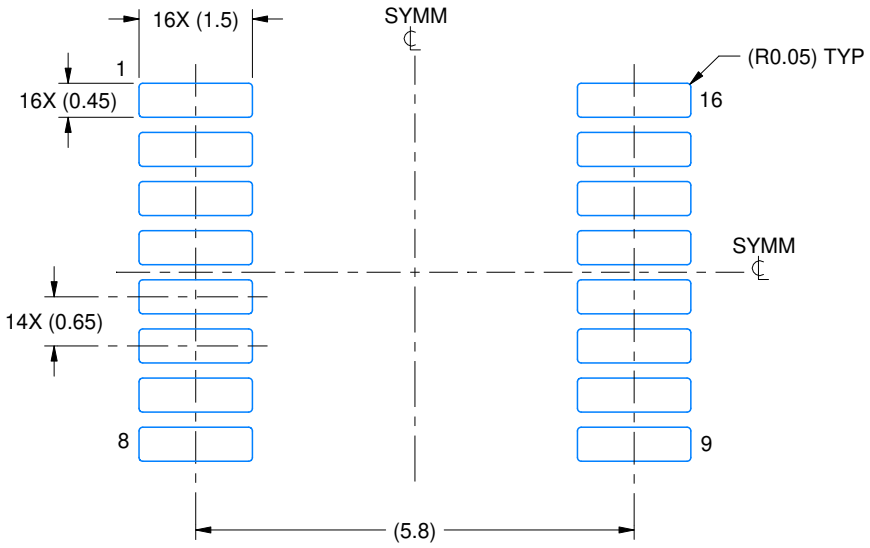
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

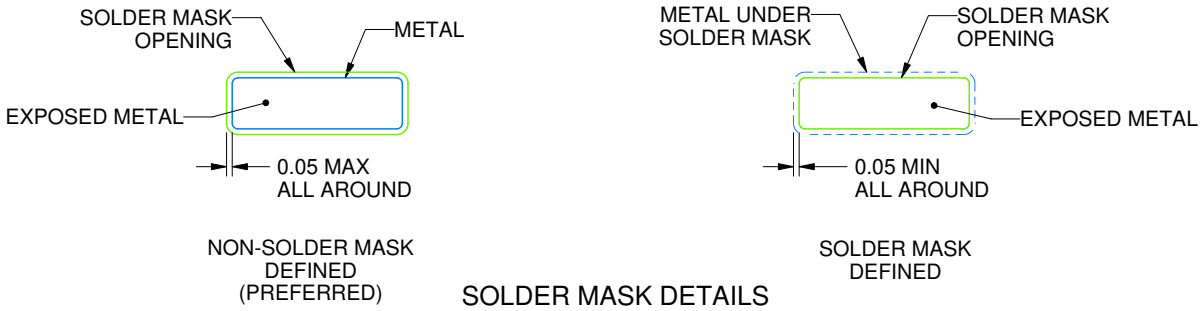


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

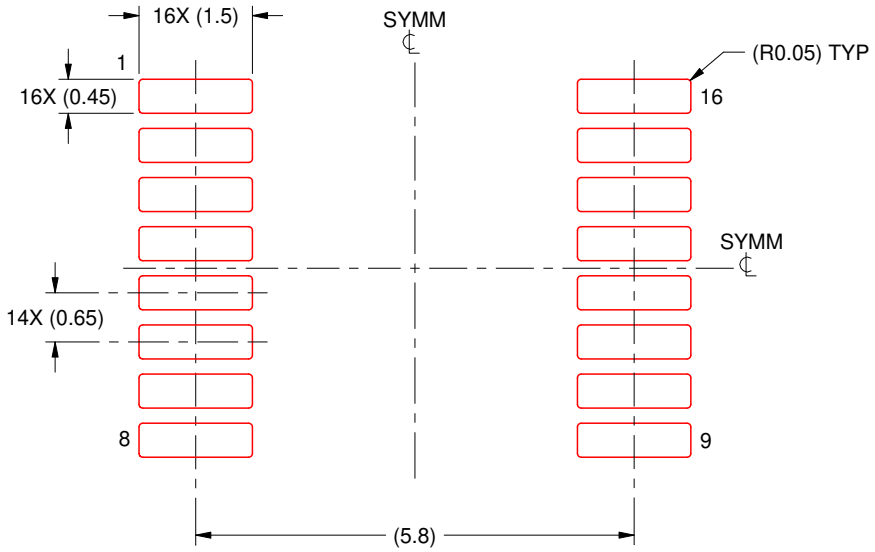


SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

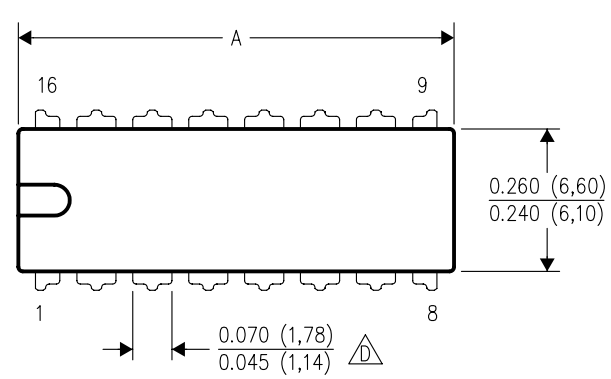
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

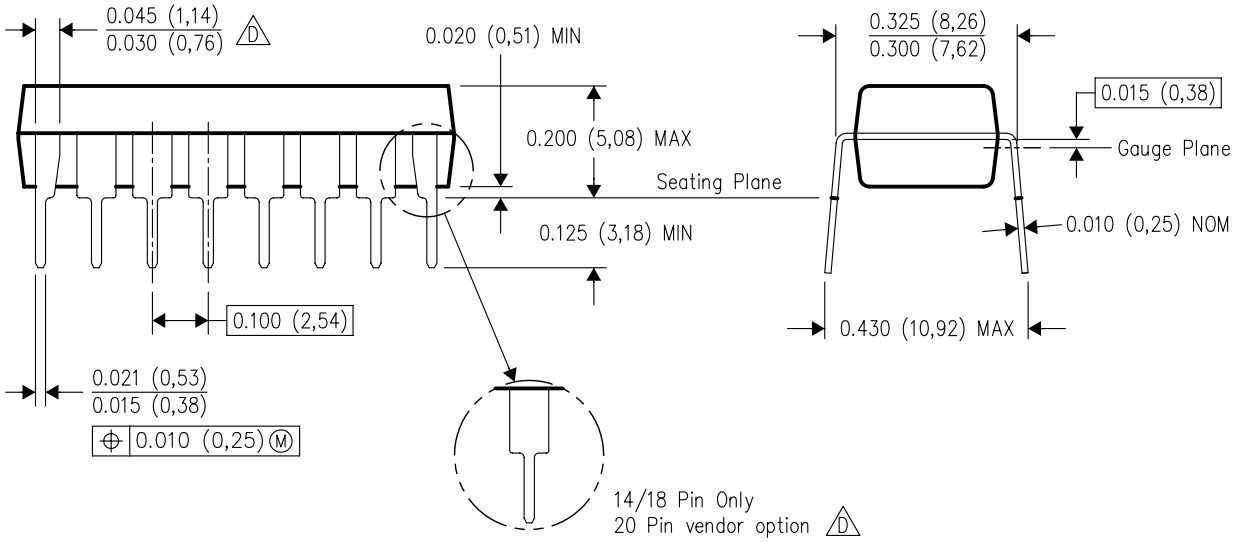
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

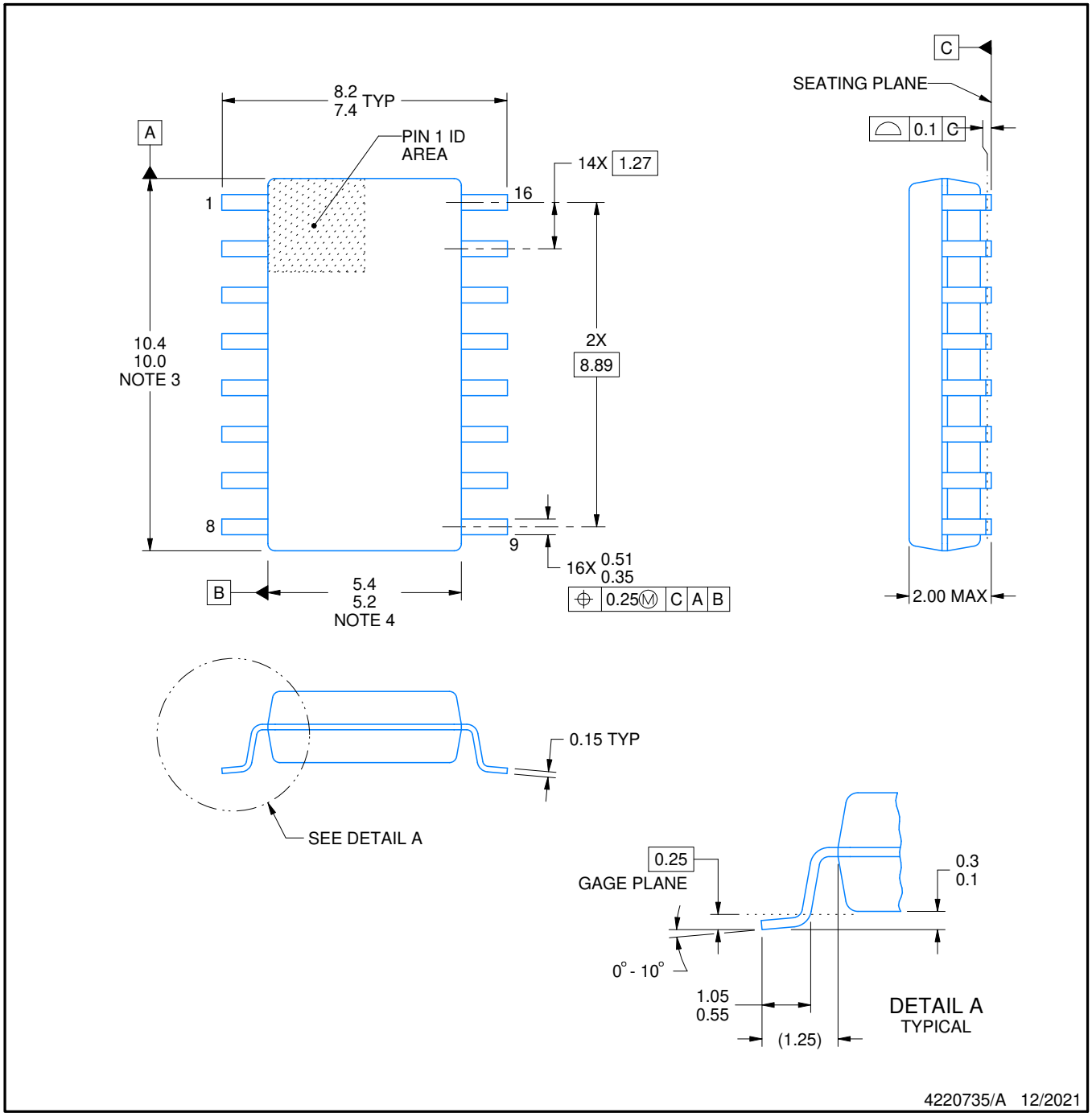


PACKAGE OUTLINE

NS0016A

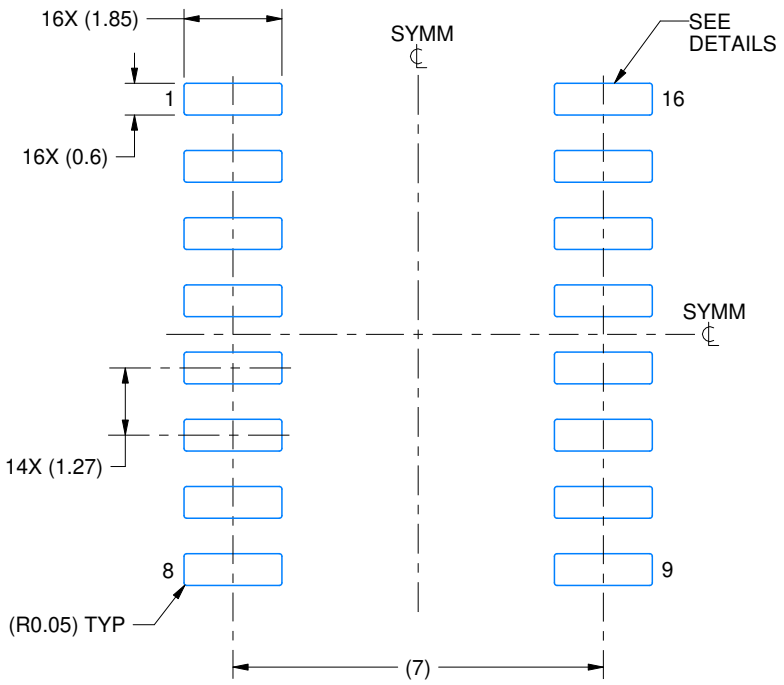
SOP - 2.00 mm max height

SOP

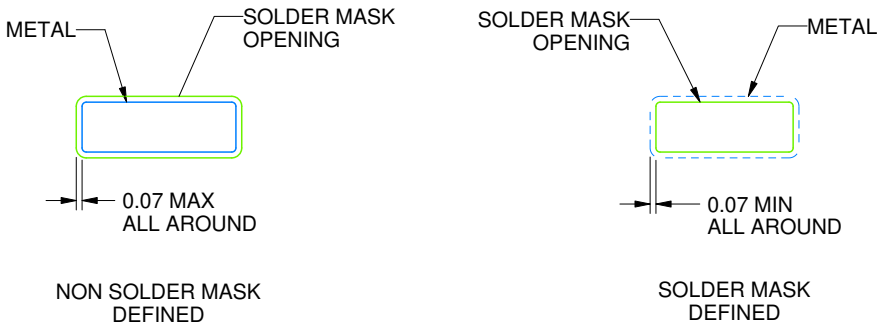


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X

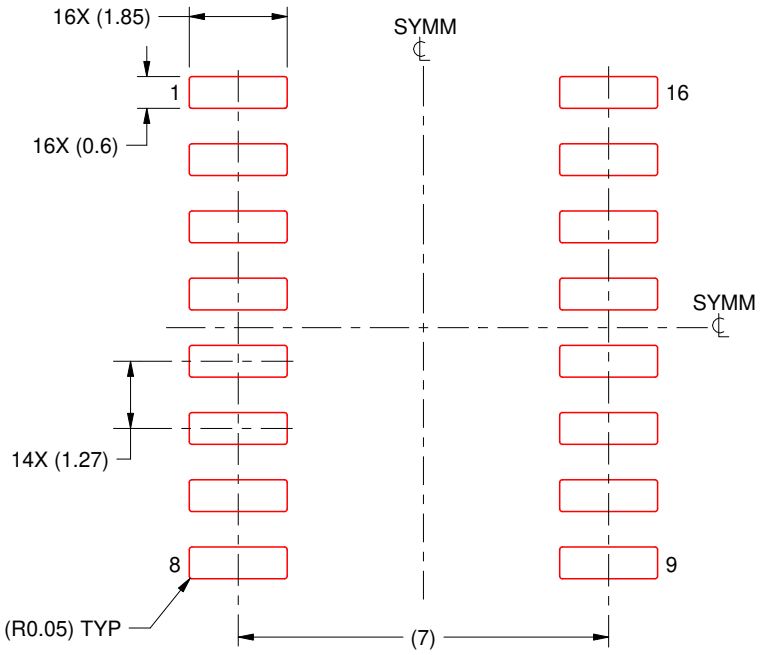


SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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