TEXAS INSTRUMENTS
Data sheet acquired from Harris Semiconductor
SCHS041D – Revised October 2003

CD4043B, CD4044B Types

CMOS Quad 3-State R/S Latches

High-Voltage Types (20-Volt Rating)
Quad NOR R/S Latch – CD4043B
Quad NAND R/S Latch – CD4044B

■CD4043B types are quad cross-coupled 3-state CMOS NOR latches and the CD4044B types are quad cross-coupled 3-state CMOS NAND latches. Each latch has a separate Q output and individual SET and RESET inputs. The Q outputs are controlled by a common ENABLE input. A logic "1" or high on the ENABLE input connects the latch states to the Q outputs. A logic "0" or low on the ENABLE input disconnects the latch states from the Q outputs, resulting in an open circuit condition on the Q outputs. The open circuit feature allows common bus-ing of the outputs.

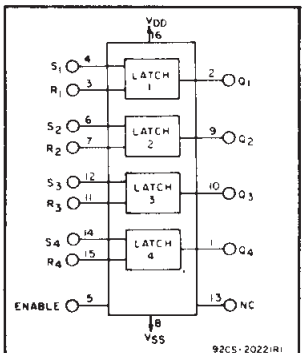
The CD4043B and CD4044B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (D, DR, DT, DW, DWR, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

Features:

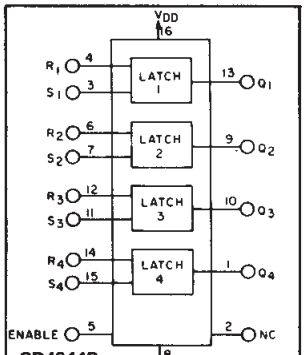
- 3-state outputs with common output ENABLE
- Separate SET and RESET inputs for each latch
- NOR and NAND configurations
- 5-V, 10-V, and 15-V parametric ratings
- Standardized symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range): 1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Holding register in multi-register system
- Four bits of independent storage with output ENABLE
- Strobed register
- General digital logic
- CD4043B for positive logic systems
- CD4044B for negative logic systems



CD4043B FUNCTIONAL DIAGRAM



CD4044B FUNCTIONAL DIAGRAM

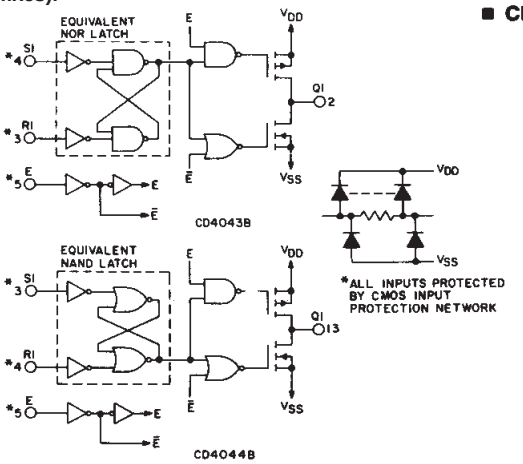
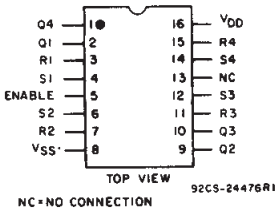
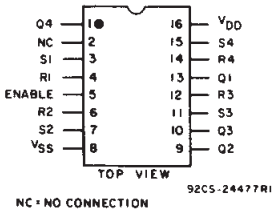


Fig. 1 – Logic diagrams.



NC = NO CONNECTION
CD4043B



NC = NO CONNECTION
CD4044B

TERMINAL ASSIGNMENTS

S	R	E	Q
X	X	0	OC*
0	0	1	NC+
1	0	1	1
0	1	1	0
1	1	1	Δ

*OPEN CIRCUIT
+ NO CHANGE
Δ DOMINATED BY S=1 INPUT

CD4043B

S	R	E	Q
X	X	0	OC*
1	1	1	NC+
0	1	1	1
1	0	1	0
0	0	1	ΔΔ

*OPEN CIRCUIT
+ NO CHANGE
ΔΔ DOMINATED BY R=0 INPUT

CD4044B

TRUTH TABLES

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
Voltages referenced to V_{SS} Terminal) ..... -0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55°C to +100°C 500mW
For T_A = +100°C to +125°C ..... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C

Recommended Operating Conditions T_A=25°C
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	V_{DD} (V)	Min.	Max.	Units
Supply-Voltage Range (T_A = Full Package Temperature Range)	–	3	18	V
SET or RESET Pulse Width, t_W	5	160	–	ns
	10	80	–	
	15	40	–	

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STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	μA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	1.5,13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	—	—	
	1, 9	–	10	7				7	—	—	
	1.5, 3.5	–	15	11				11	—	—	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA
3-State Output Leakage Current I_{OUT} Max.	0,18	0,18	18	±0.4	±0.4	±12	±12	–	$\pm10^{-4}$	±0.4	μA

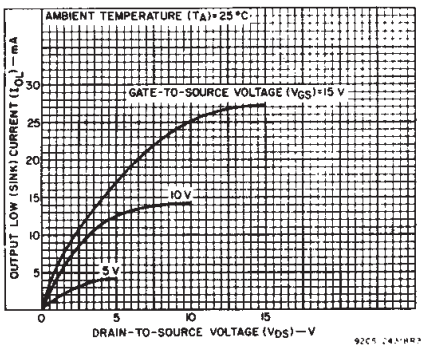


Fig. 2 — Typical output low (sink) current characteristics.

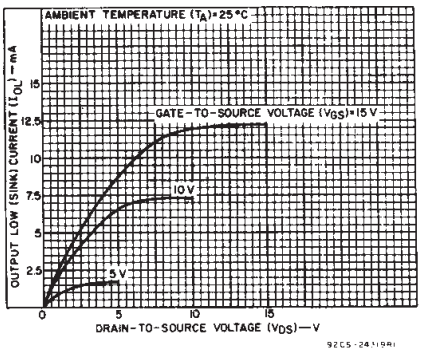


Fig. 3 — Minimum output low (sink) current characteristics.

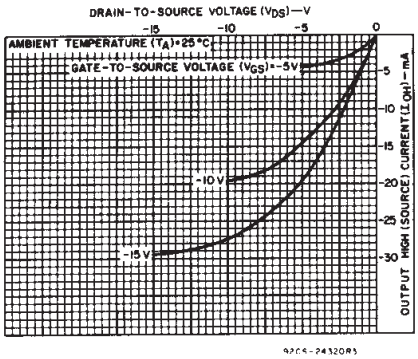


Fig. 4 — Typical output high (source) current characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS *at $T_A = 25°$ C; Input t_r, $t_f = 20$ ns, $C_L = 50$ pF, $R_L = 200$ KΩ*

CHARACTERISTIC	V_{DD} (V)	LIMITS ALL TYPES TYP.	LIMITS ALL TYPES MAX.	UNITS
Propagation Delay Time: t_{PHL}, t_{PLH} SET or RESET to Q	5	150	300	ns
	10	70	140	
	15	50	100	
3-State Propagation Delay Time: ENABLE to Q t_{PHZ}, t_{PZH}	5	115	230	ns
	10	55	110	
	15	40	80	
t_{PLZ}, t_{PZL}	5	90	180	ns
	10	50	100	
	15	35	70	
Transition Time: t_{THL}, t_{TLH}	5	100	200	ns
	10	50	100	
	15	40	80	
Minimum SET or RESET Pulse Width, t_W	5	80	160	ns
	10	40	80	
	15	20	40	
Input Capacitance, (Any Input) C_{IN}	–	5	7.5	pF

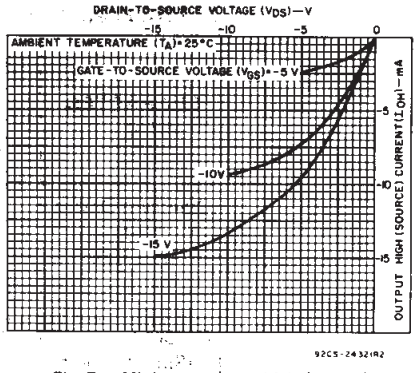


Fig. 5 – Minimum output high (source) current characteristics.

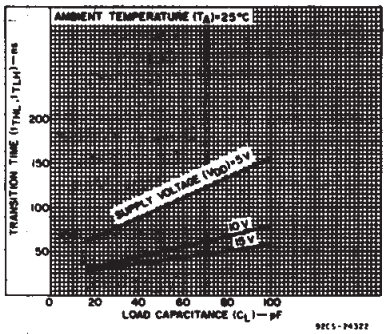


Fig. 6 – Typical transition time vs. load capacitance.

TEST CIRCUITS

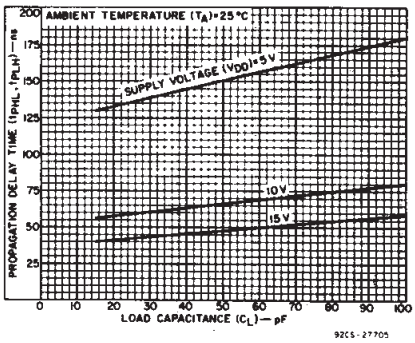


Fig. 7 – Typical propagation delay time vs. load capacitance–SET, RESET to Q, $\bar{Q}$.

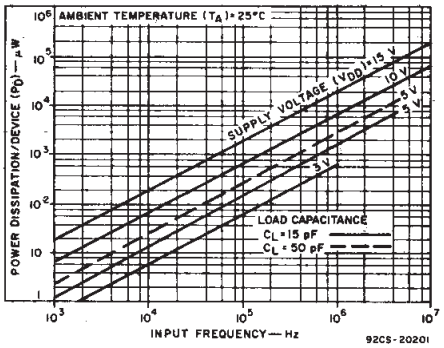


Fig. 8 – Typical power dissipation vs. frequency.

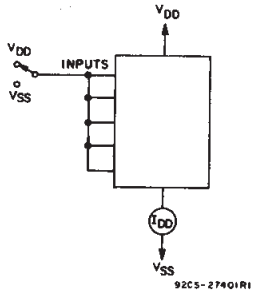


Fig. 9 – Quiescent device current.

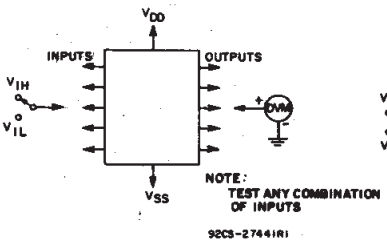


Fig. 10 – Input voltage.

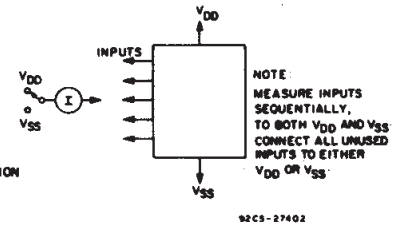


Fig. 11 – Input current.

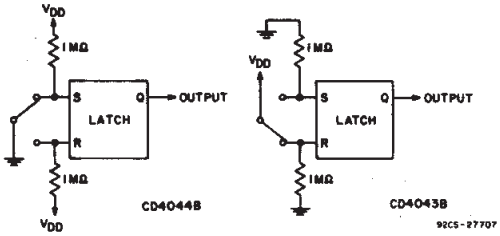


Fig. 12 – Switch bounce eliminator.

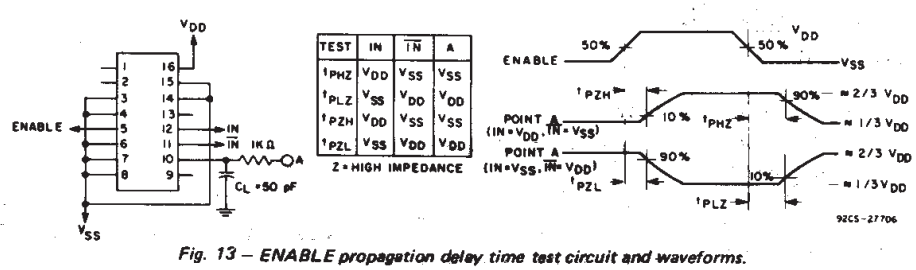
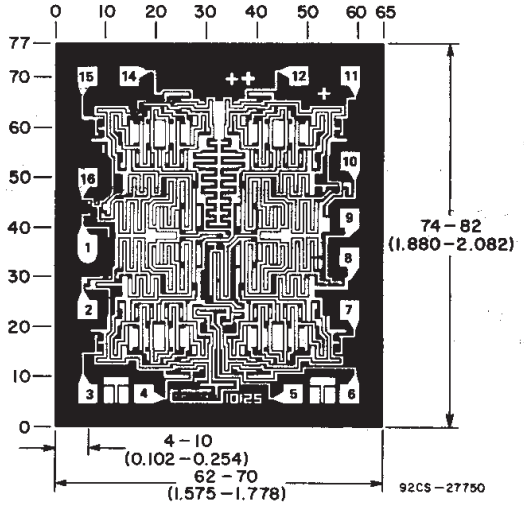
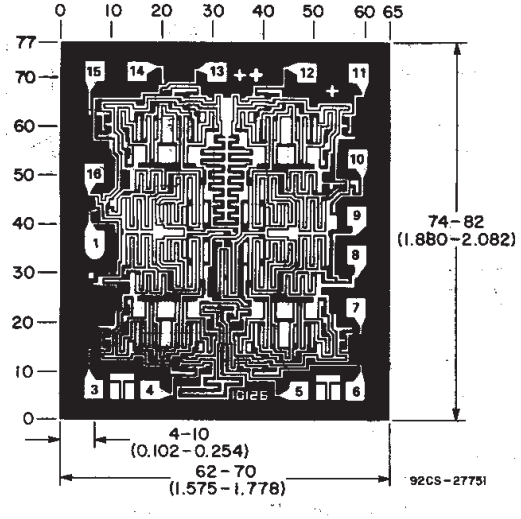


Fig. 13 – ENABLE propagation delay time test circuit and waveforms.

CHIP DIMENSIONS AND PAD LAYOUTS



CD4043BH



CD4044BH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

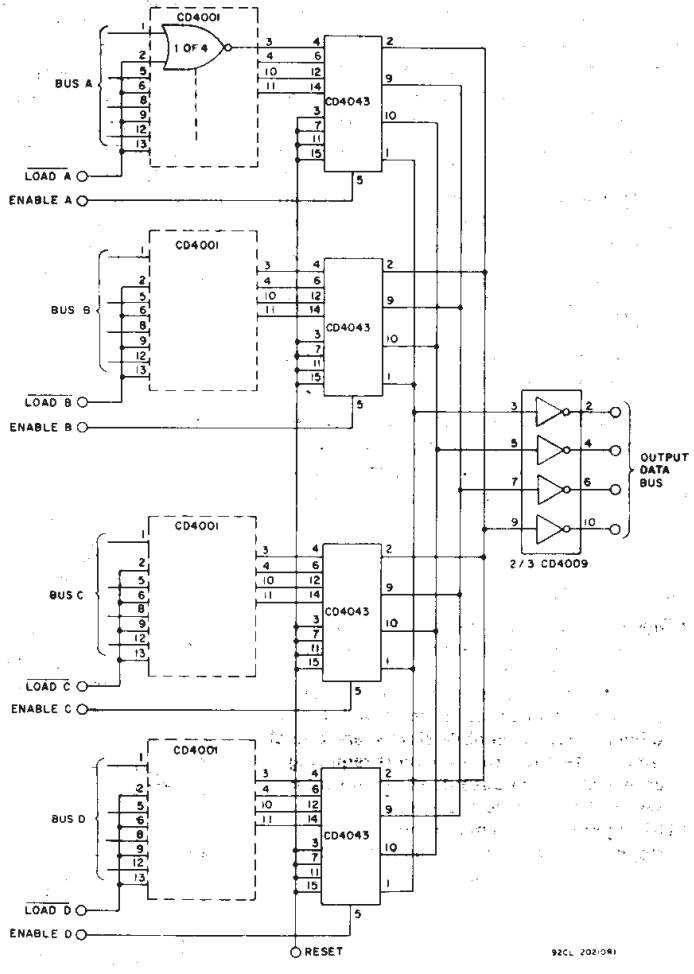


Fig. 14 – Multiple bus storage.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
CD4043BD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4043BDE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4043BDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4043BDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4043BDRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4043BDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4043BDT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4043BDTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4043BDTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4043BDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4043BDWE4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4043BDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4043BDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4043BDWRE4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4043BDWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4043BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4043BEE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4043BF3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type
CD4043BF3AS2534	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
CD4043BM	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI
CD4043BNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4043BNSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4043BNSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4043BPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4043BPWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4043BPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
CD4044BD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4044BDE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4044BDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4044BDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4044BDRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4044BDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4044BDT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4044BDTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4044BDTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4044BDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4044BDWE4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4044BDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4044BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4044BEE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4044BF	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type
CD4044BF3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type
CD4044BF3AS2534	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
CD4044BM	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI
CD4044BNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4044BNSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4044BNSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4044BPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4044BPWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4044BPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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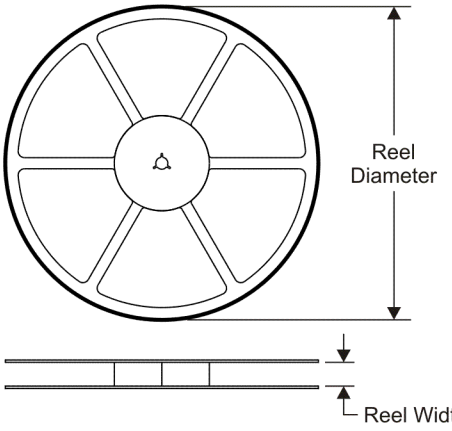
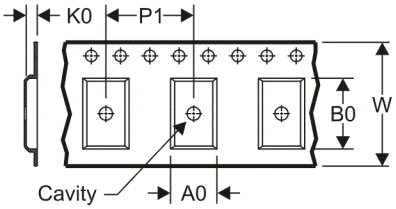
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

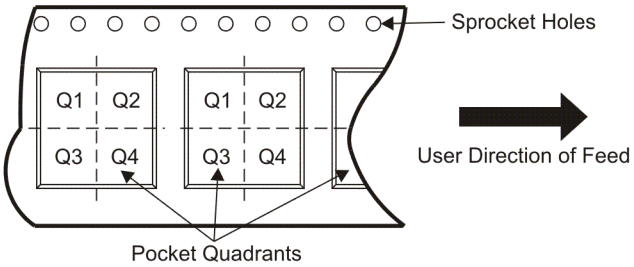


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

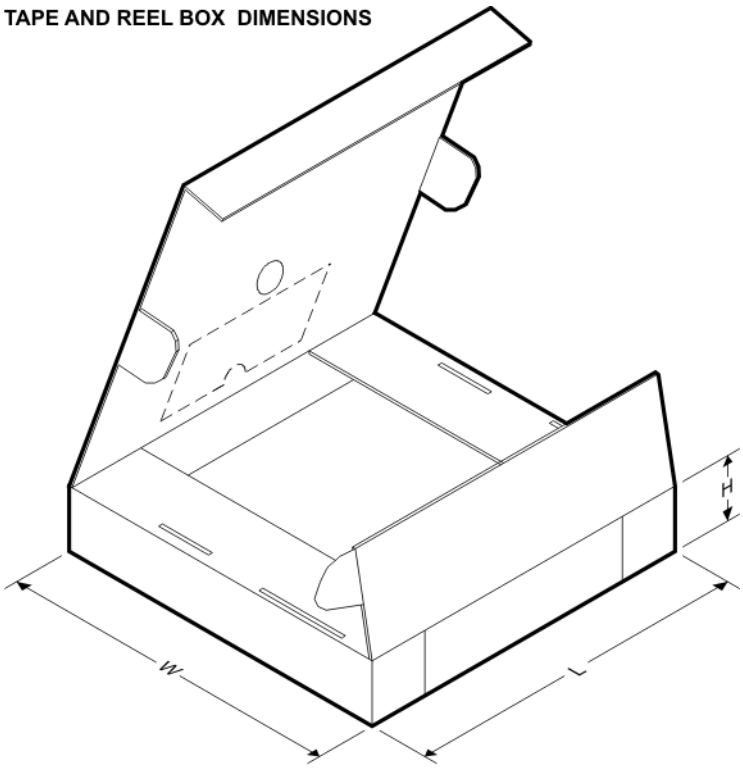
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4043BDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4043BDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
CD4043BNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4043BPWR	TSSOP	PW	16	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1
CD4044BDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4044BNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4044BPWR	TSSOP	PW	16	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

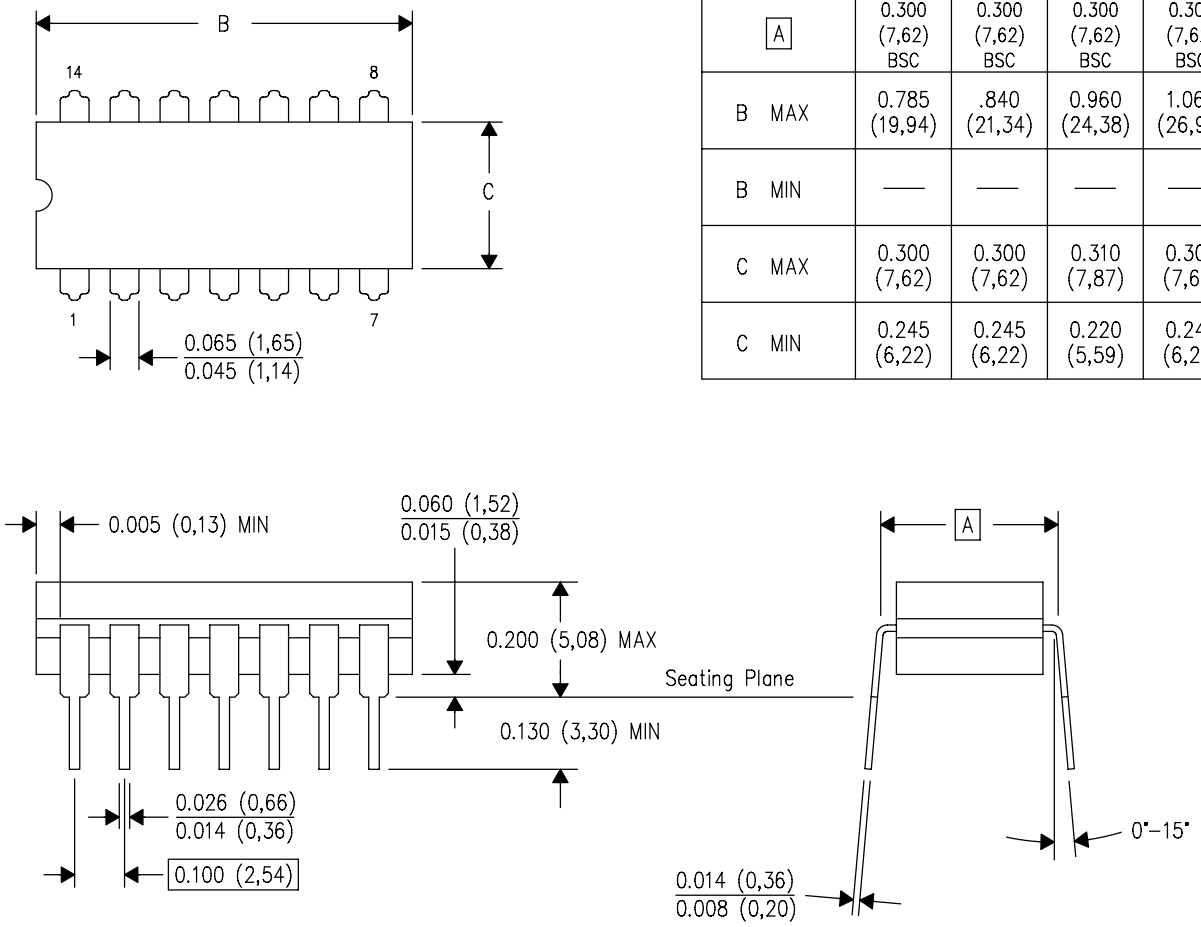


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4043BDR	SOIC	D	16	2500	333.2	345.9	28.6
CD4043BDWR	SOIC	DW	16	2000	346.0	346.0	33.0
CD4043BNSR	SO	NS	16	2000	346.0	346.0	33.0
CD4043BPWR	TSSOP	PW	16	2000	346.0	346.0	29.0
CD4044BDR	SOIC	D	16	2500	333.2	345.9	28.6
CD4044BNSR	SO	NS	16	2000	346.0	346.0	33.0
CD4044BPWR	TSSOP	PW	16	2000	346.0	346.0	29.0

J (R–GDIP–T**) CERAMIC DUAL IN–LINE PACKAGE

14 LEADS SHOWN



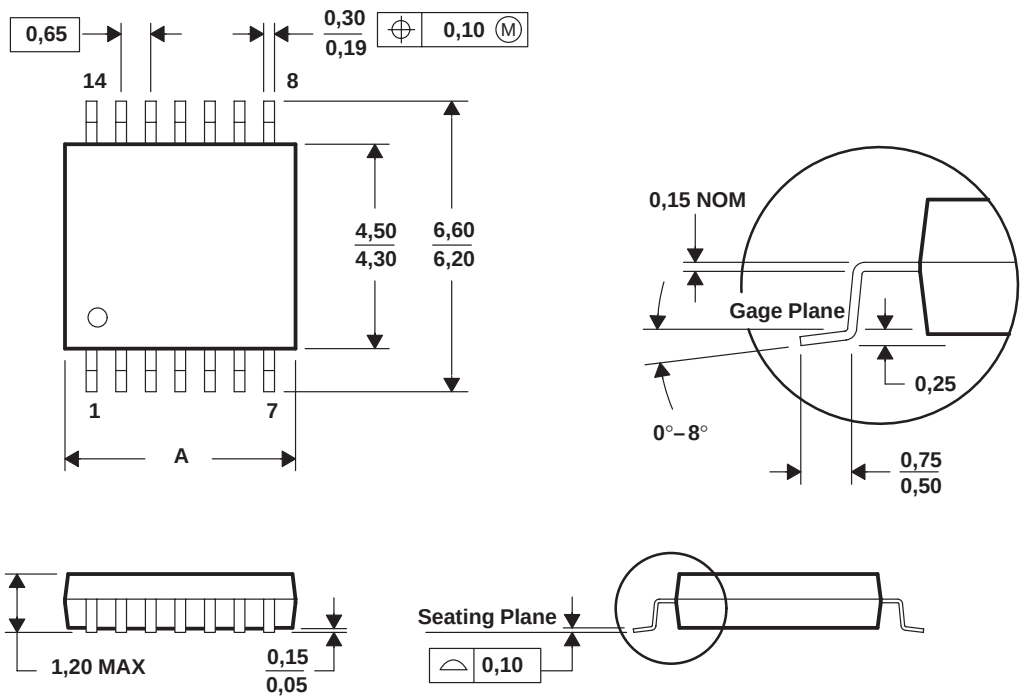
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

4040083/F 03/03

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

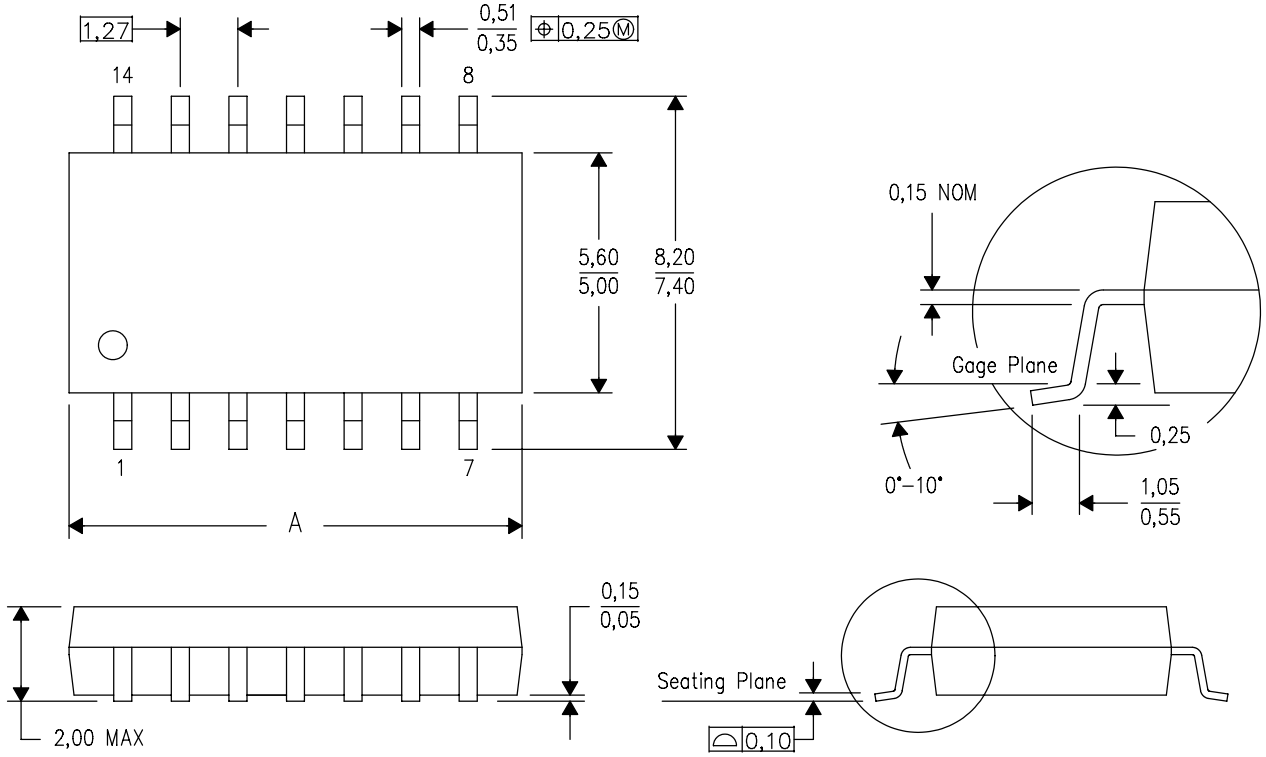
4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

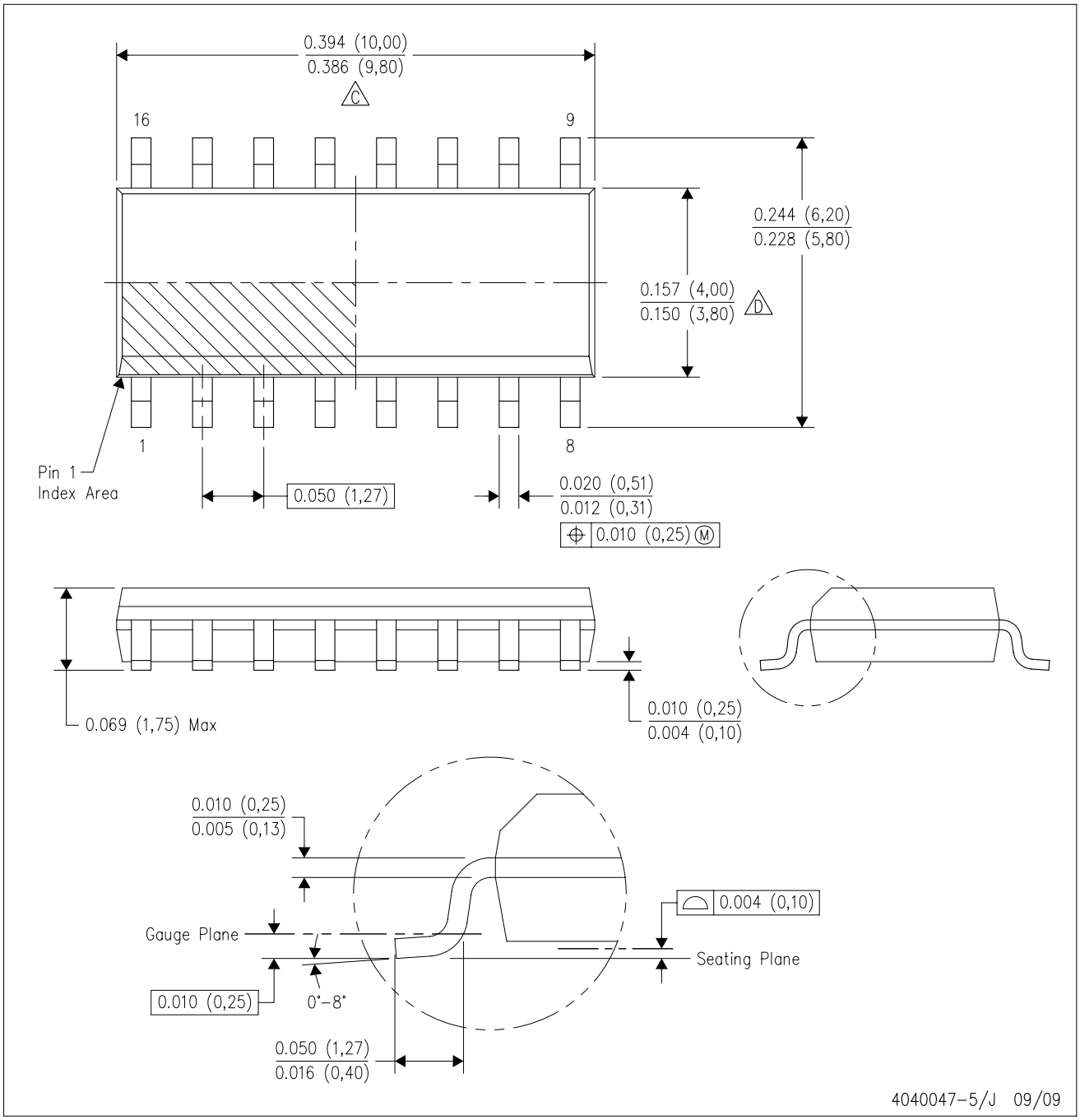


DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

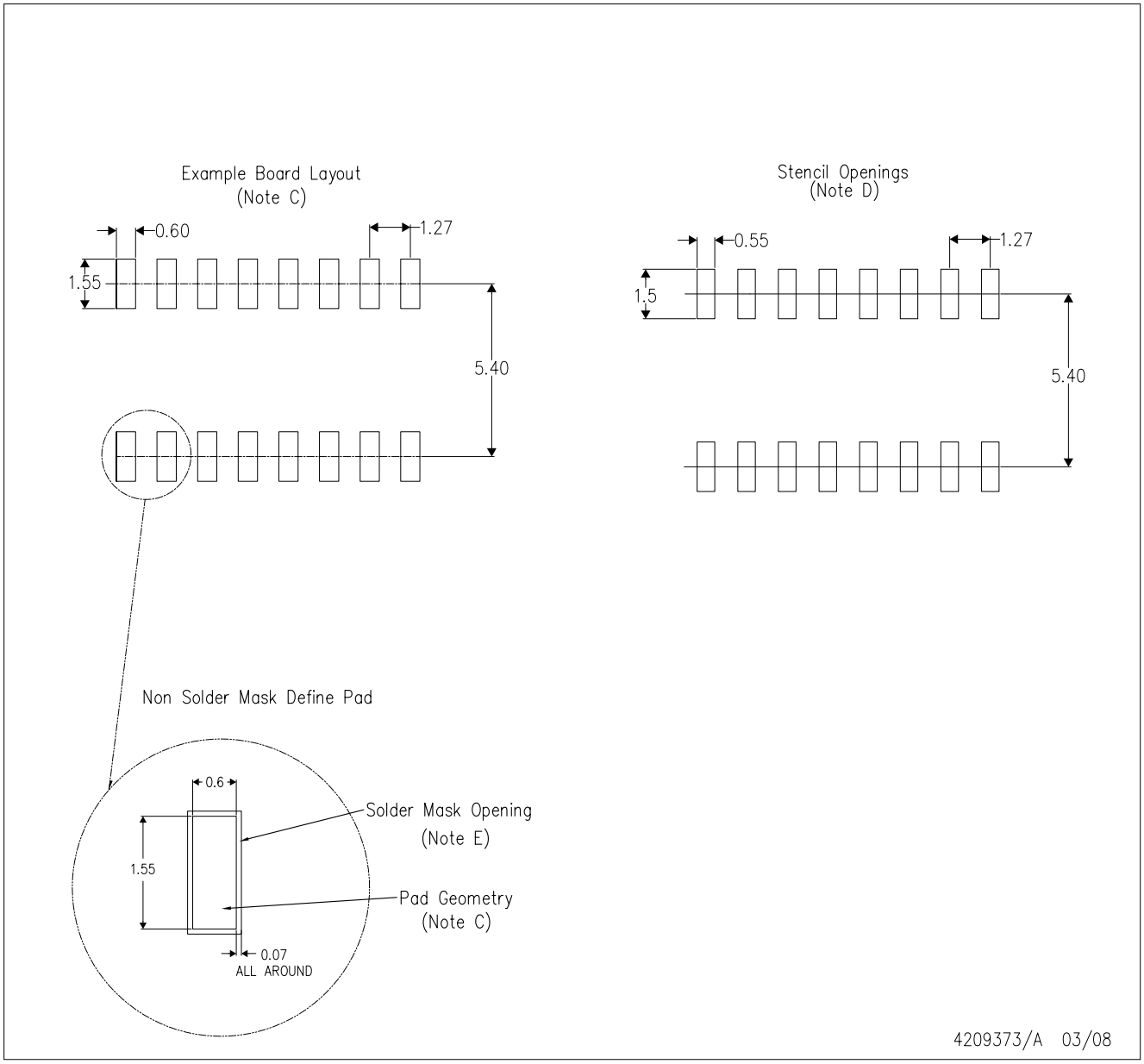
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

D (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE



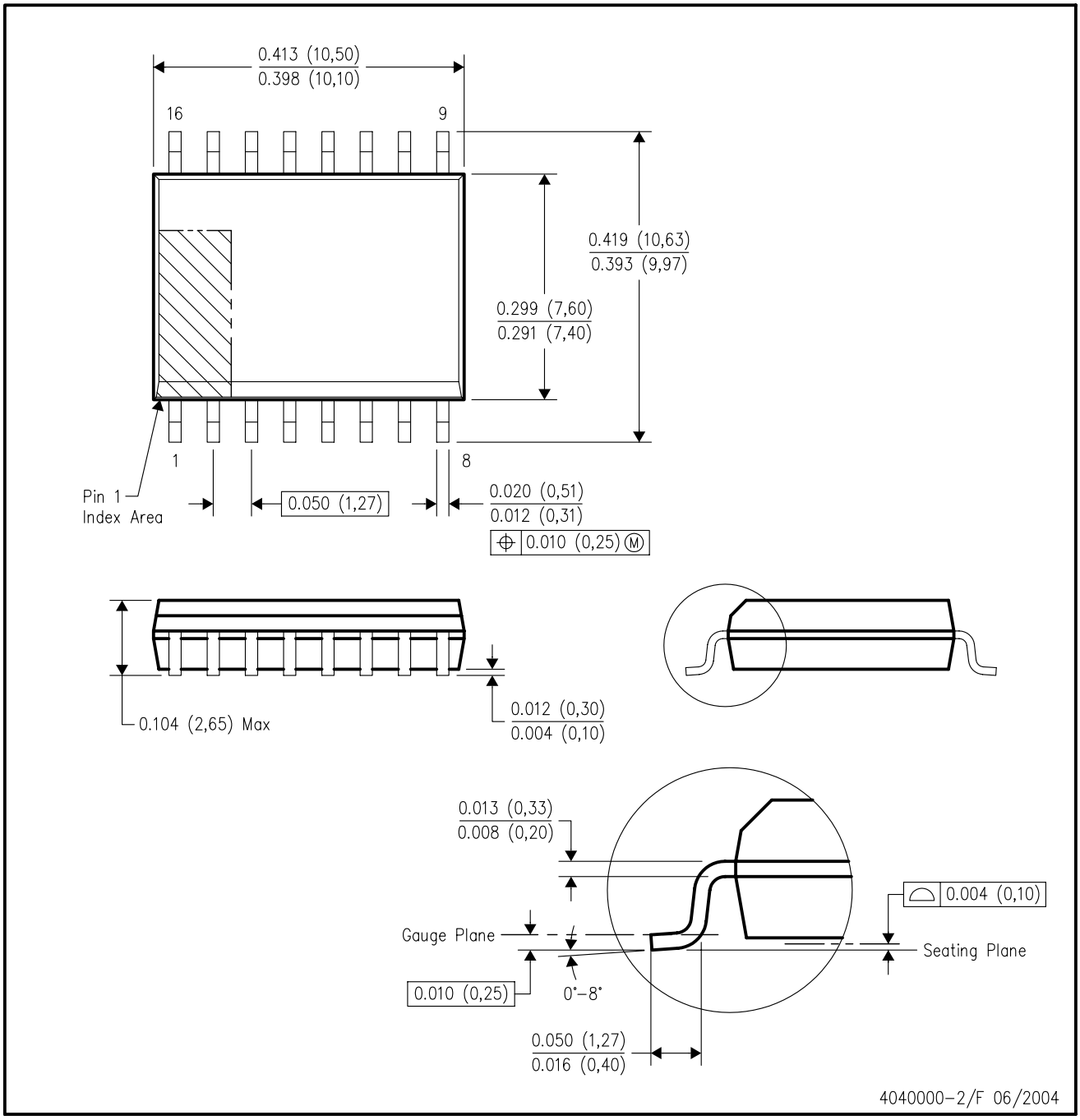
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AC.

D(R–PDSO–G16)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

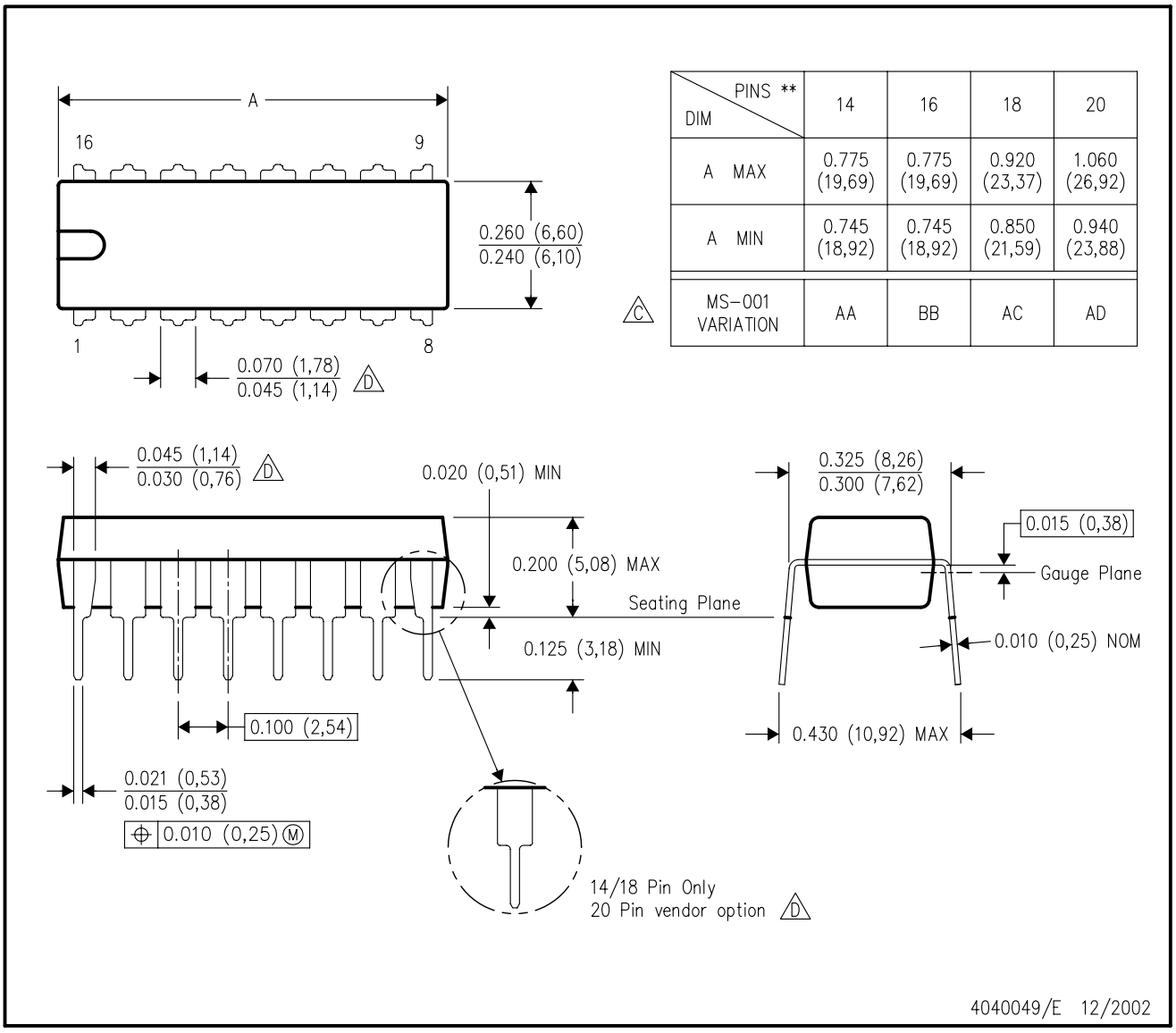
DW (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AA.

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD4043BD	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	CD4043BM
CD4043BDR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4043BM
CD4043BDR.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4043BM
CD4043BDRG4	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4043BM
CD4043BDT	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	CD4043BM
CD4043BDW	Obsolete	Production	SOIC (DW) | 16	-	-	Call TI	Call TI	-55 to 125	CD4043BM
CD4043BDWR	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4043BM
CD4043BDWR.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4043BM
CD4043BE	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4043BE
CD4043BE.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4043BE
CD4043BEE4	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4043BE
CD4043BF3A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4043BF3A
CD4043BF3A.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4043BF3A
CD4043BNSR	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4043B
CD4043BNSR.A	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4043B
CD4043BPWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 125	CM043B
CD4043BPWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM043B
CD4043BPWRG4	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM043B
CD4044BD	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	CD4044BM
CD4044BDR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4044BM
CD4044BDR.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4044BM
CD4044BDT	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	CD4044BM
CD4044BDW	NRND	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4044BM
CD4044BDW.A	NRND	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4044BM
CD4044BE	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4044BE
CD4044BE.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4044BE
CD4044BEE4	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4044BE
CD4044BF	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4044BF
CD4044BF.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4044BF

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD4044BF3A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4044BF3A
CD4044BF3A.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4044BF3A
CD4044BNSR	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4044B
CD4044BNSR.A	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4044B
CD4044BPWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM044B
CD4044BPWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM044B

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF CD4043B, CD4043B-MIL, CD4044B, CD4044B-MIL :

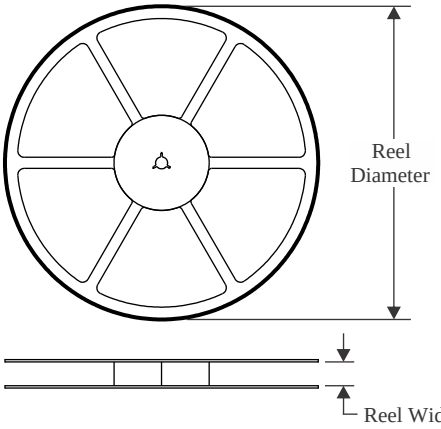
- Catalog : CD4043B, CD4044B
- Military : CD4043B-MIL, CD4044B-MIL

NOTE: Qualified Version Definitions:

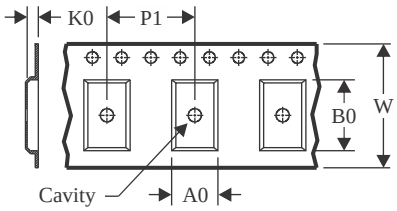
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

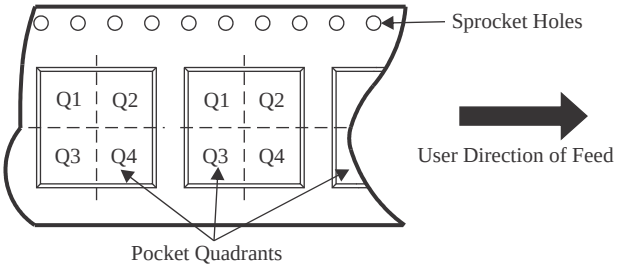


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

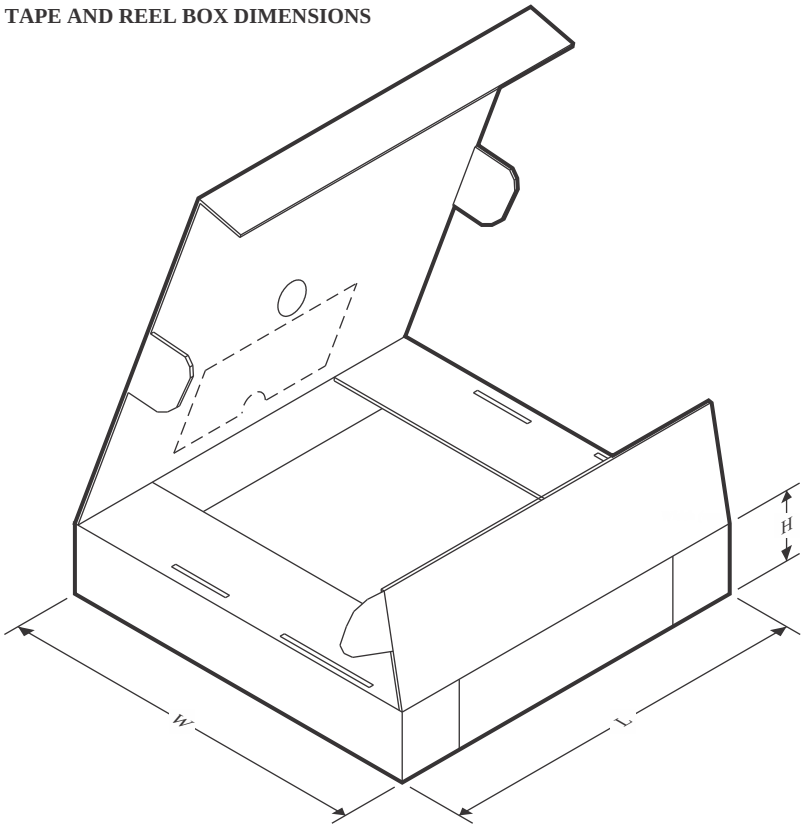
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4043BDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4043BDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
CD4043BNSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
CD4043BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4043BPWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4044BDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4044BNSR	SOP	NS	16	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
CD4044BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

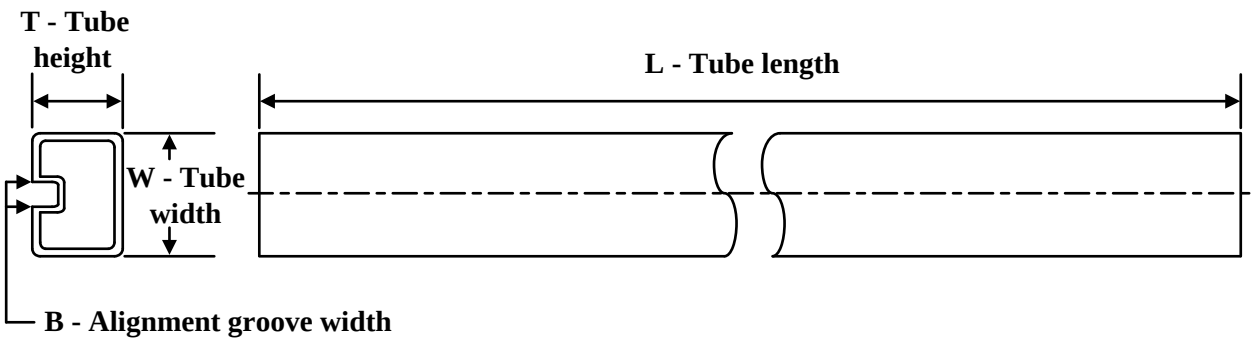
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

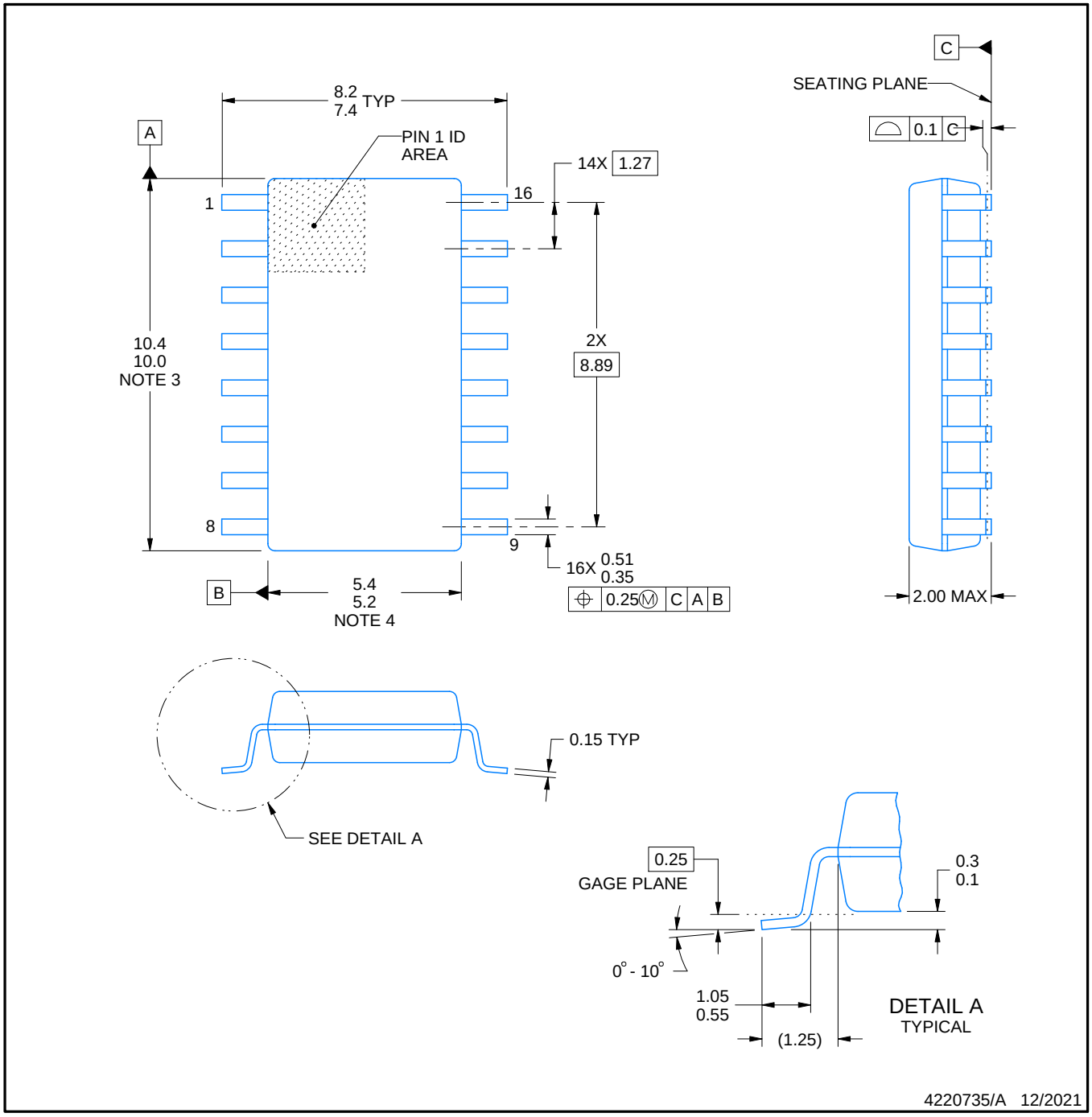
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4043BDR	SOIC	D	16	2500	353.0	353.0	32.0
CD4043BDWR	SOIC	DW	16	2000	350.0	350.0	43.0
CD4043BNSR	SOP	NS	16	2000	353.0	353.0	32.0
CD4043BPWR	TSSOP	PW	16	2000	356.0	356.0	35.0
CD4043BPWRG4	TSSOP	PW	16	2000	356.0	356.0	35.0
CD4044BDR	SOIC	D	16	2500	353.0	353.0	32.0
CD4044BNSR	SOP	NS	16	2000	353.0	353.0	32.0
CD4044BPWR	TSSOP	PW	16	2000	353.0	353.0	32.0

TUBE



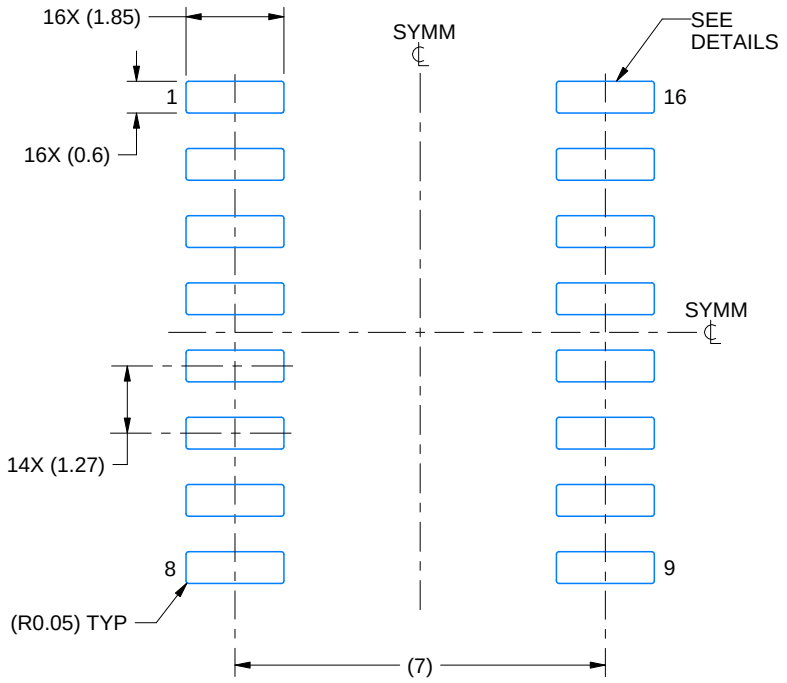
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD4043BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4043BE.A	N	PDIP	16	25	506	13.97	11230	4.32
CD4043BEE4	N	PDIP	16	25	506	13.97	11230	4.32
CD4044BDW	DW	SOIC	16	40	506.98	12.7	4826	6.6
CD4044BDW.A	DW	SOIC	16	40	506.98	12.7	4826	6.6
CD4044BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4044BE.A	N	PDIP	16	25	506	13.97	11230	4.32
CD4044BEE4	N	PDIP	16	25	506	13.97	11230	4.32

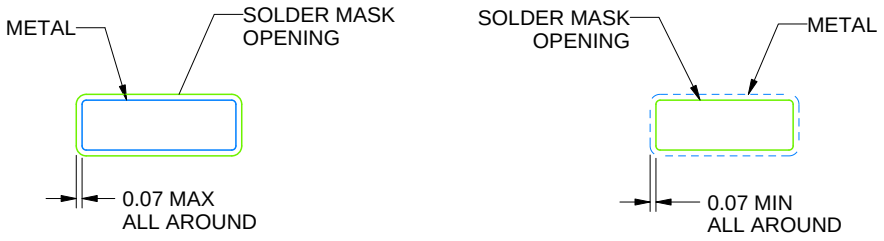


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X



NON SOLDER MASK DEFINED

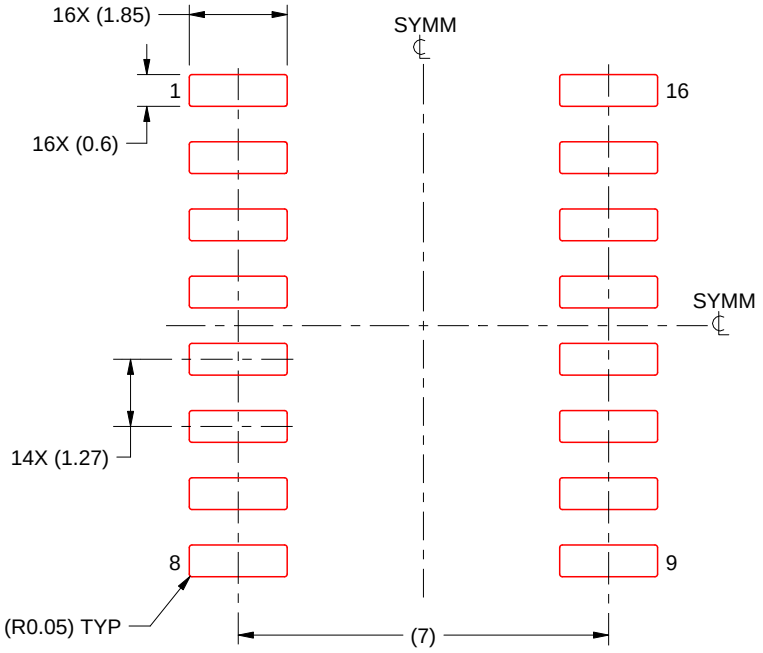
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



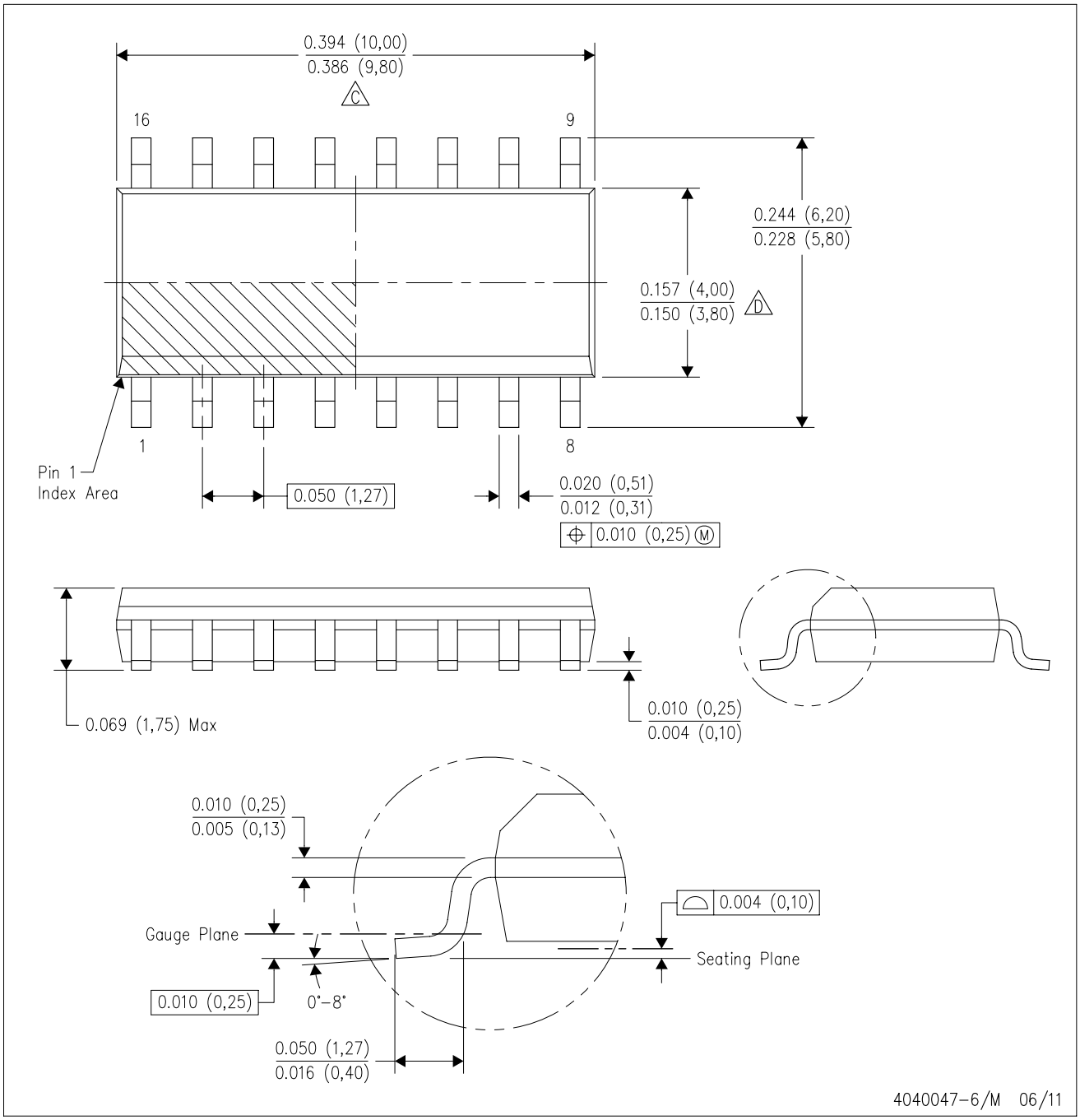
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

GENERIC PACKAGE VIEW

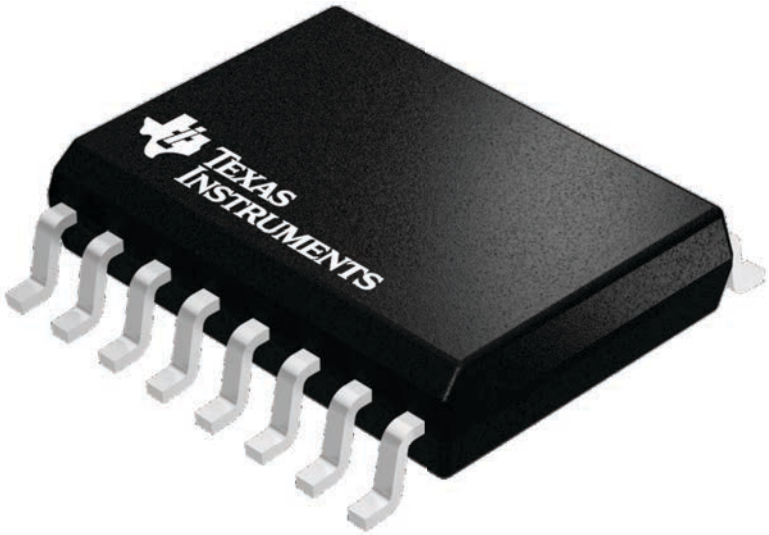
DW 16

SOIC - 2.65 mm max height

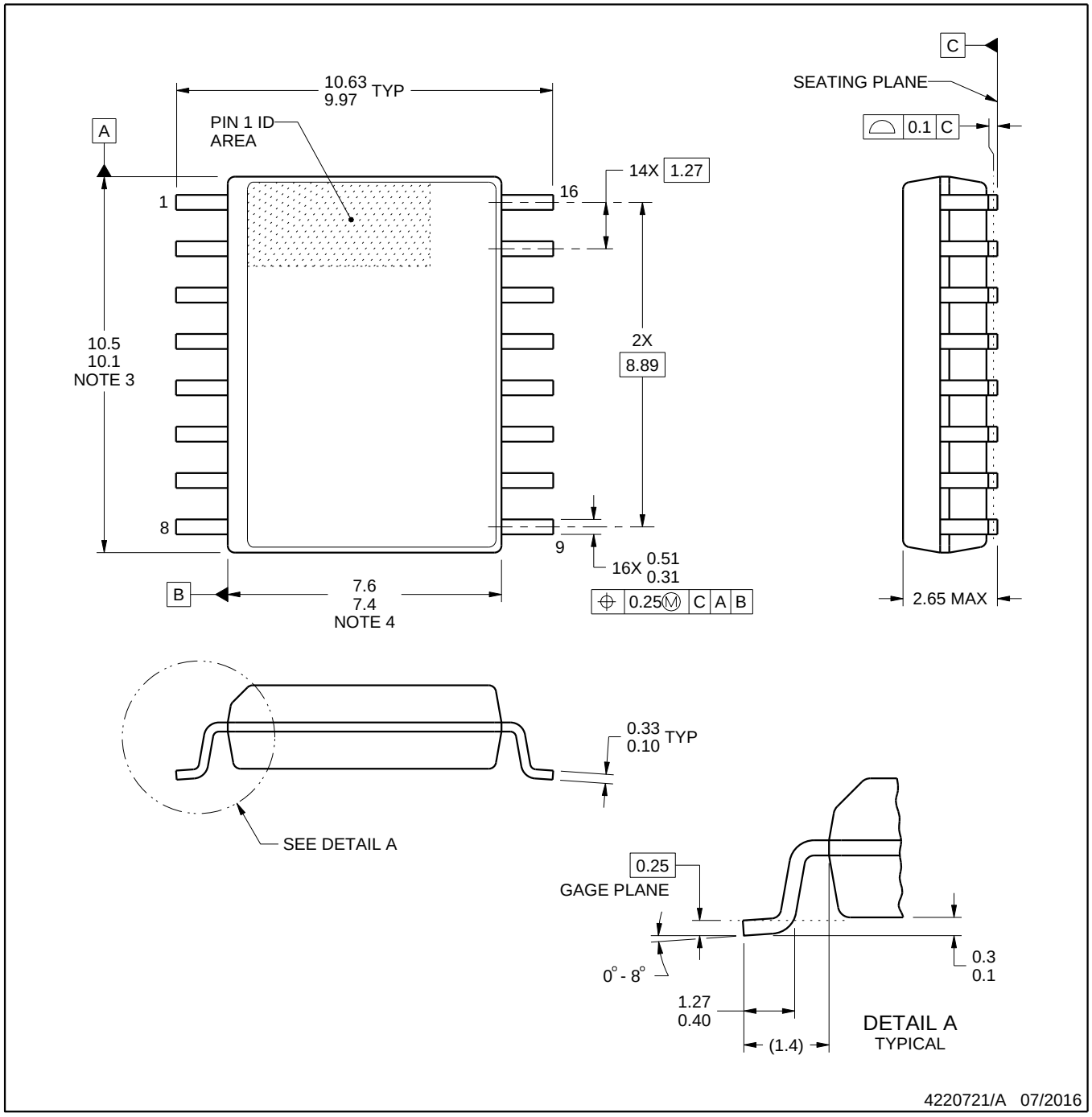
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

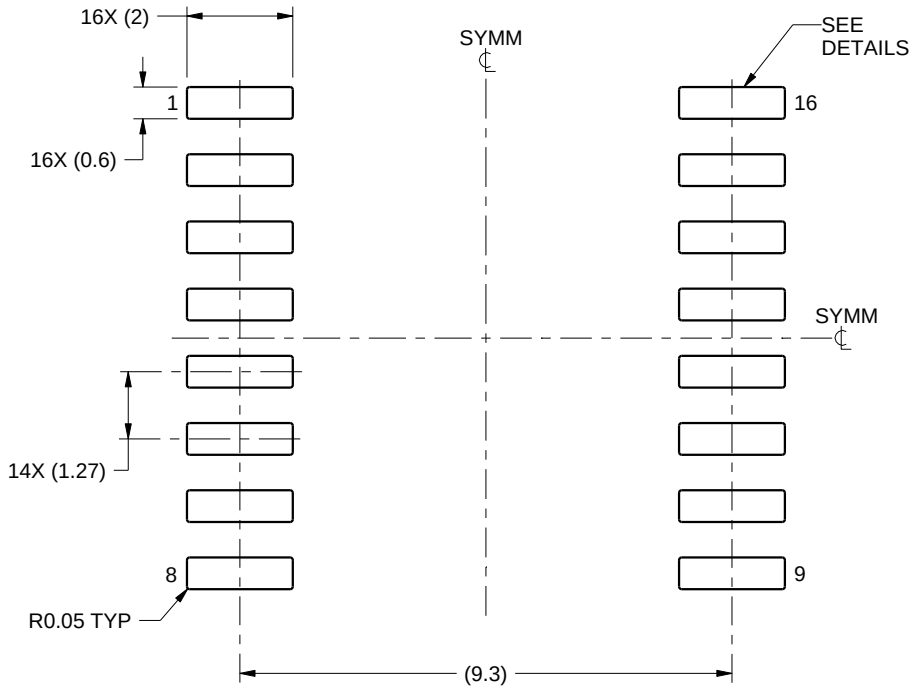


4224780/A

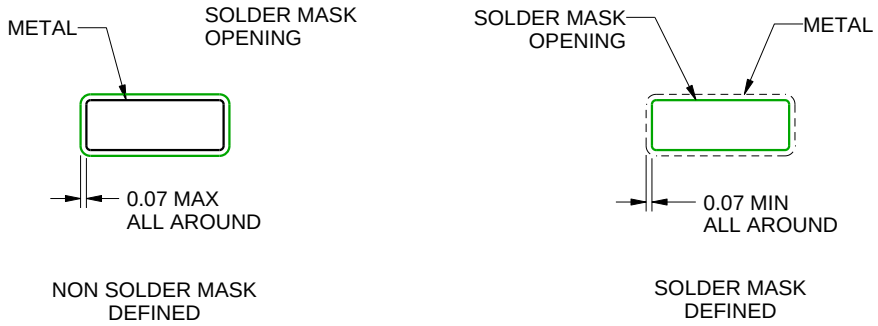


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

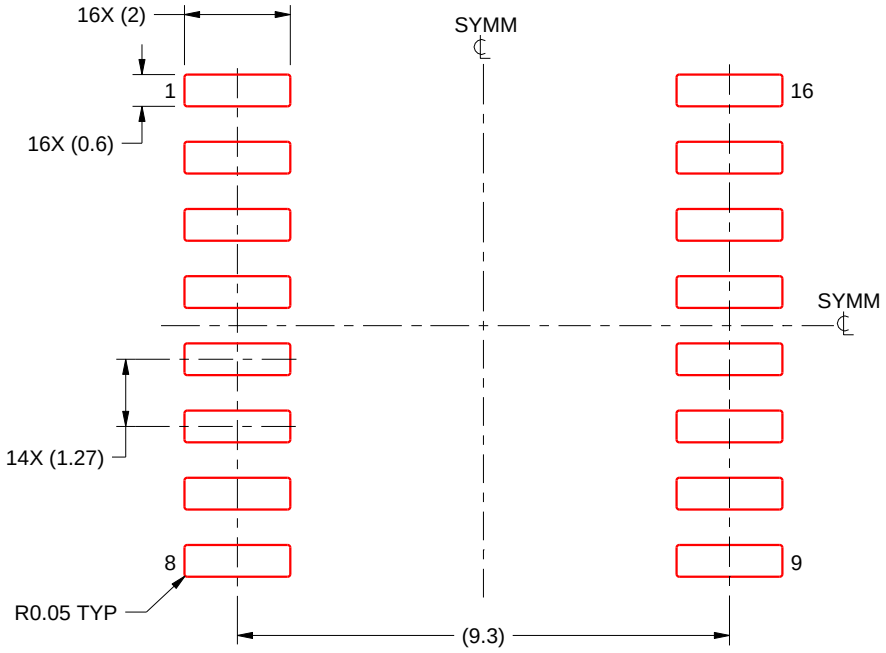


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

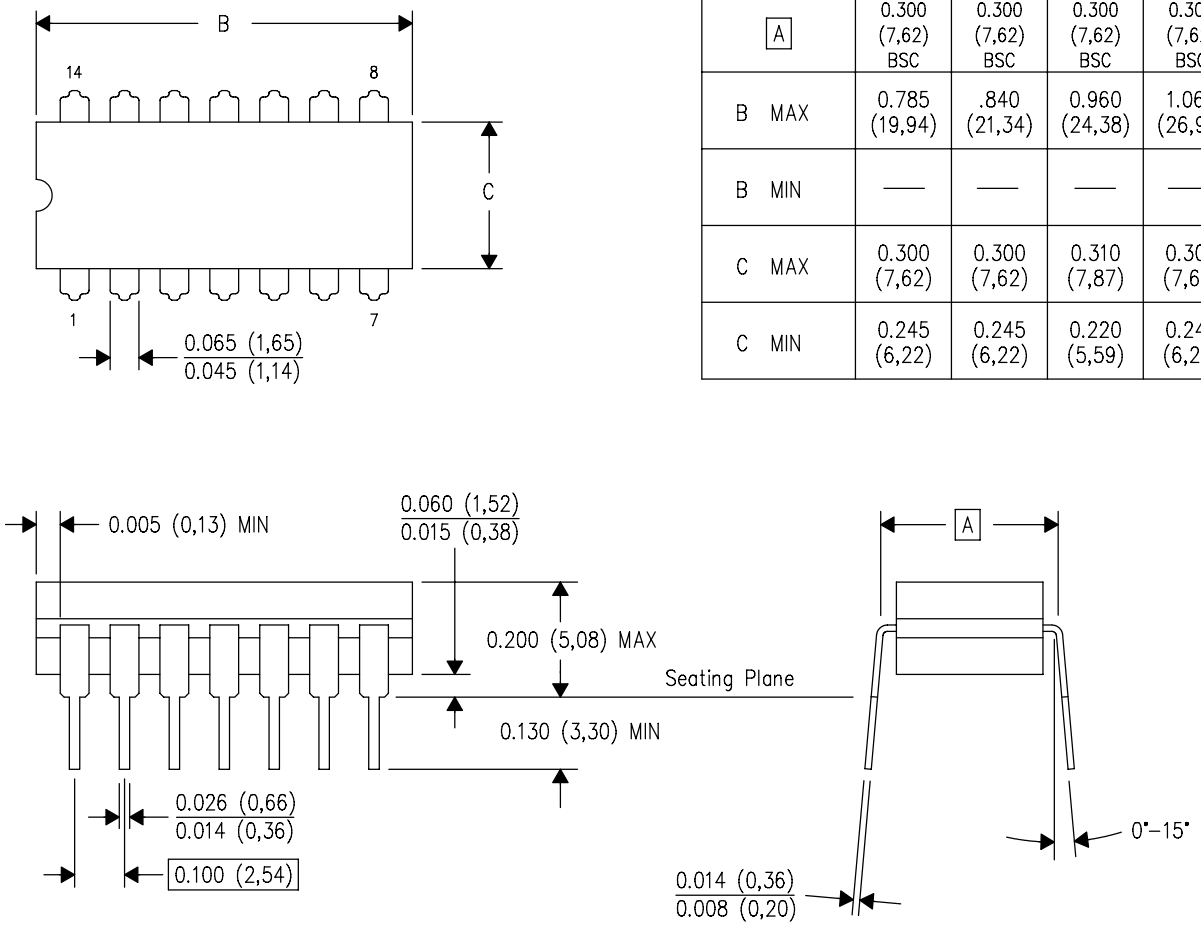
4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

J (R–GDIP–T**) CERAMIC DUAL IN–LINE PACKAGE

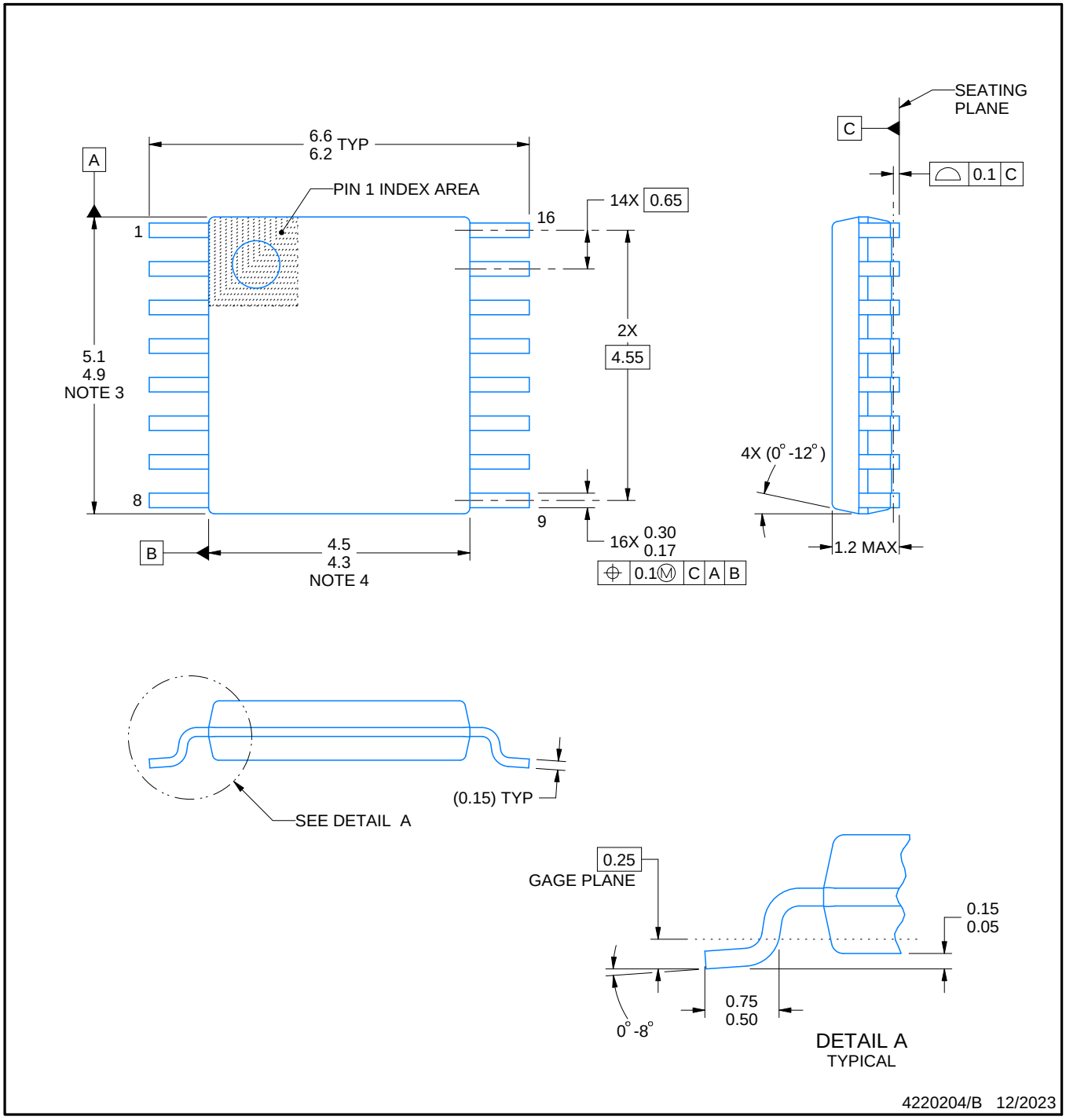
14 LEADS SHOWN



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

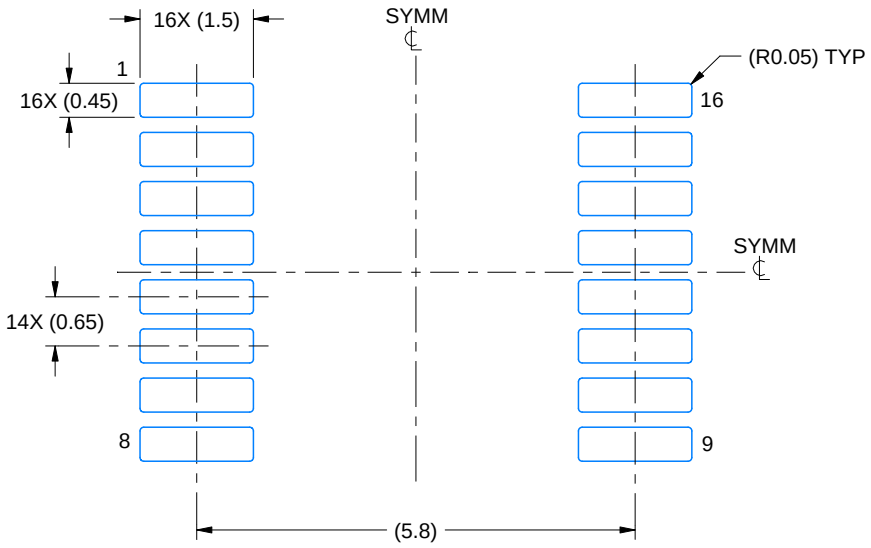
4040083/F 03/03

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

NON-SOLDER MASK DEFINED (PREFERRED)

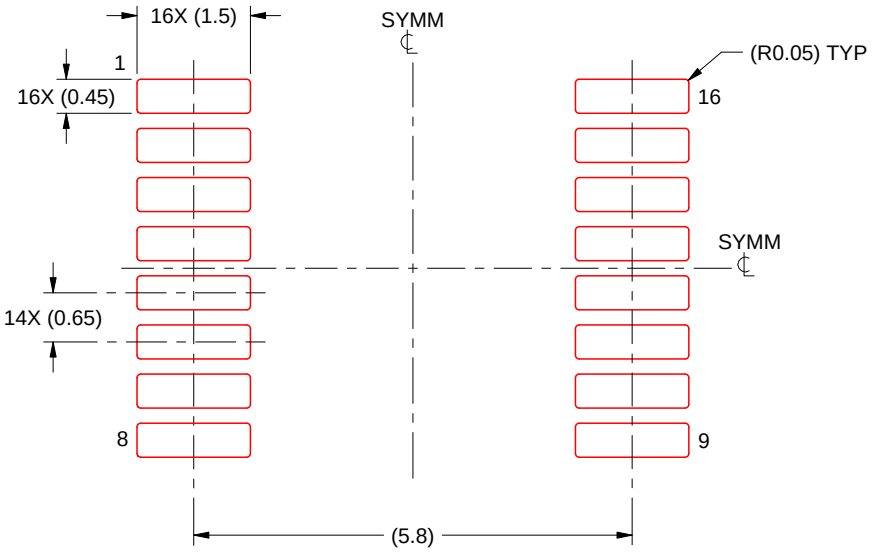
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

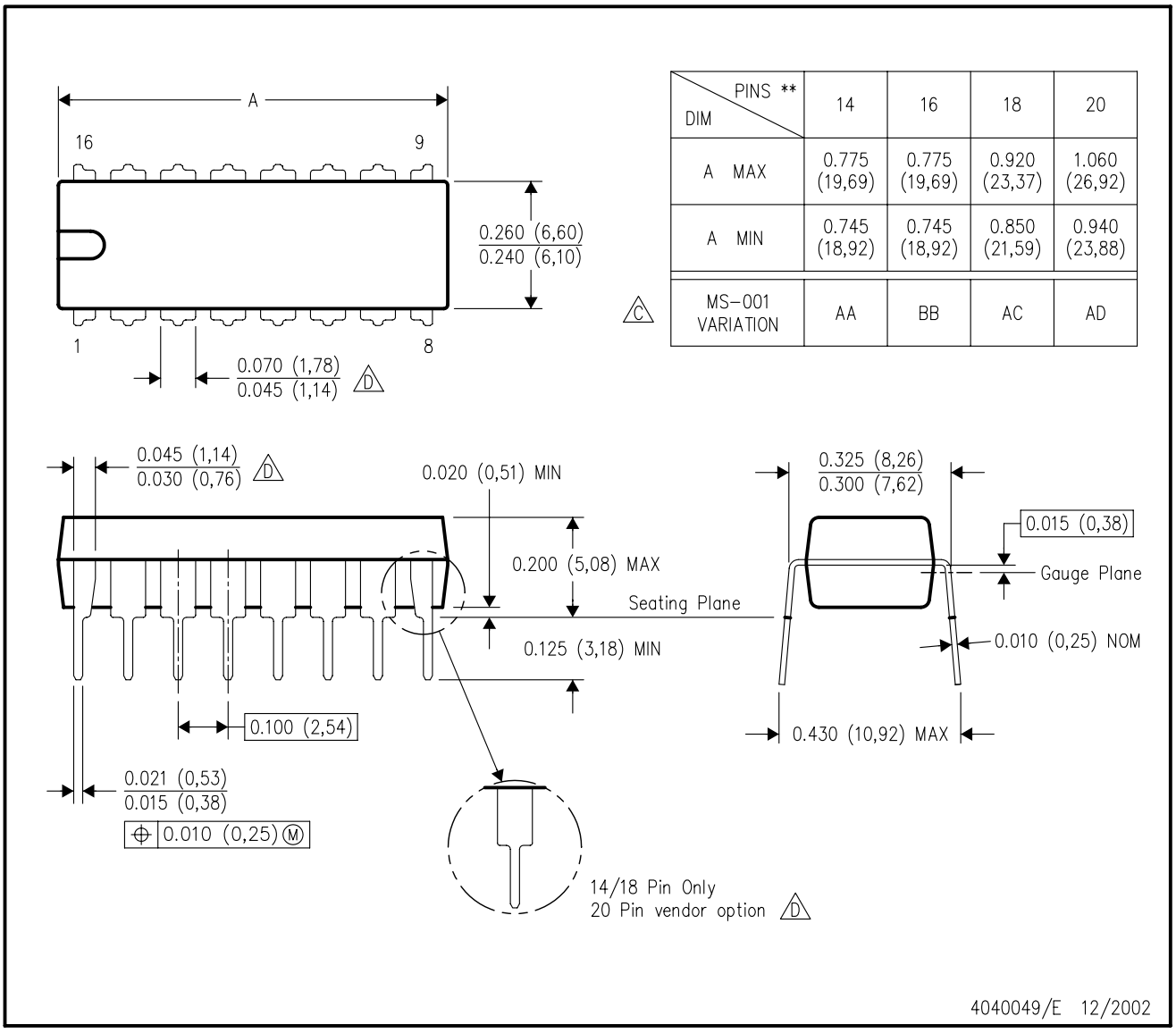
4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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