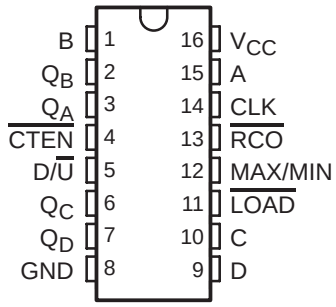
- **2-V to 6-V V_{CC} Operation ('HC190, 191)**
- **4.5-V to 5.5-V V_{CC} Operation ('HCT191)**
- **Wide Operating Temperature Range of −55°C to 125°C**
- **Synchronous Counting and Asynchronous Loading**
- **Two Outputs for n-Bit Cascading**
- **Look-Ahead Carry for High-Speed Counting**
- **Balanced Propagation Delays and Transition Times**
- **Standard Outputs Drive Up To 15 LS-TTL Loads**
- **Significant Power Reduction Compared to LS-TTL Logic ICs**

CD54HC190, 191; CD54HCT191 . . . F PACKAGE
CD74HC190 . . . E, NS, OR PW PACKAGE
CD74HC191, CD74HCT191 . . . E OR M PACKAGE
(TOP VIEW)



description/ordering information

The CD54/74HC190 are asynchronously presettable BCD decade counters, whereas the CD54/74HC191 and CD54/74HCT191 are asynchronously presettable binary counters.

Presetting the counter to the number on preset data inputs (A−D) is accomplished by a low asynchronous parallel load ($\overline{LOAD}$) input. Counting occurs when $\overline{LOAD}$ is high, count enable ($\overline{CTEN}$) is low, and the down/up (D/$\overline{U}$) input is either high for down counting or low for up counting. The counter is decremented or incremented synchronously with the low-to-high transition of the clock.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−55°C to 125°C	PDIP − E	Tube of 25	CD74HC190E	CD74HC190E
			CD74HC191E	CD74HC191E
			CD74HCT191E	CD74HCT191E
	SOIC − M	Tube of 40	CD74HC191M	HC191M
		Reel of 2500	CD74HC191M96	
		Reel of 250	CD74HC191MT	
		Tube of 40	CD74HCT191M	HCT191M
	SOP − NS	Reel of 2000	CD74HC190NSR	HC190M
	TSSOP − PW	Tube of 90	CD74HC190PW	HJ190
		Reel of 2000	CD74HC190PWR	
		Reel of 250	CD74HC190PWT	
	CDIP − F	Tube of 25	CD54HC190F3A	CD54HC190F3A
			CD54HC191F3A	CD54HC191F3A
			CD54HCT191F3A	CD54HCT191F3A

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

description/ordering information (continued)

When an overflow or underflow of the counter occurs, the MAX/MIN output, which is low during counting, goes high and remains high for one clock cycle. This output can be used for look-ahead carry in high-speed cascading (see Figure 1). The MAX/MIN output also initiates the ripple clock ($\overline{RCO}$) output, which normally is high, goes low, and remains low for the low-level portion of the clock pulse. These counters can be cascaded using $\overline{RCO}$ (see Figure 2).

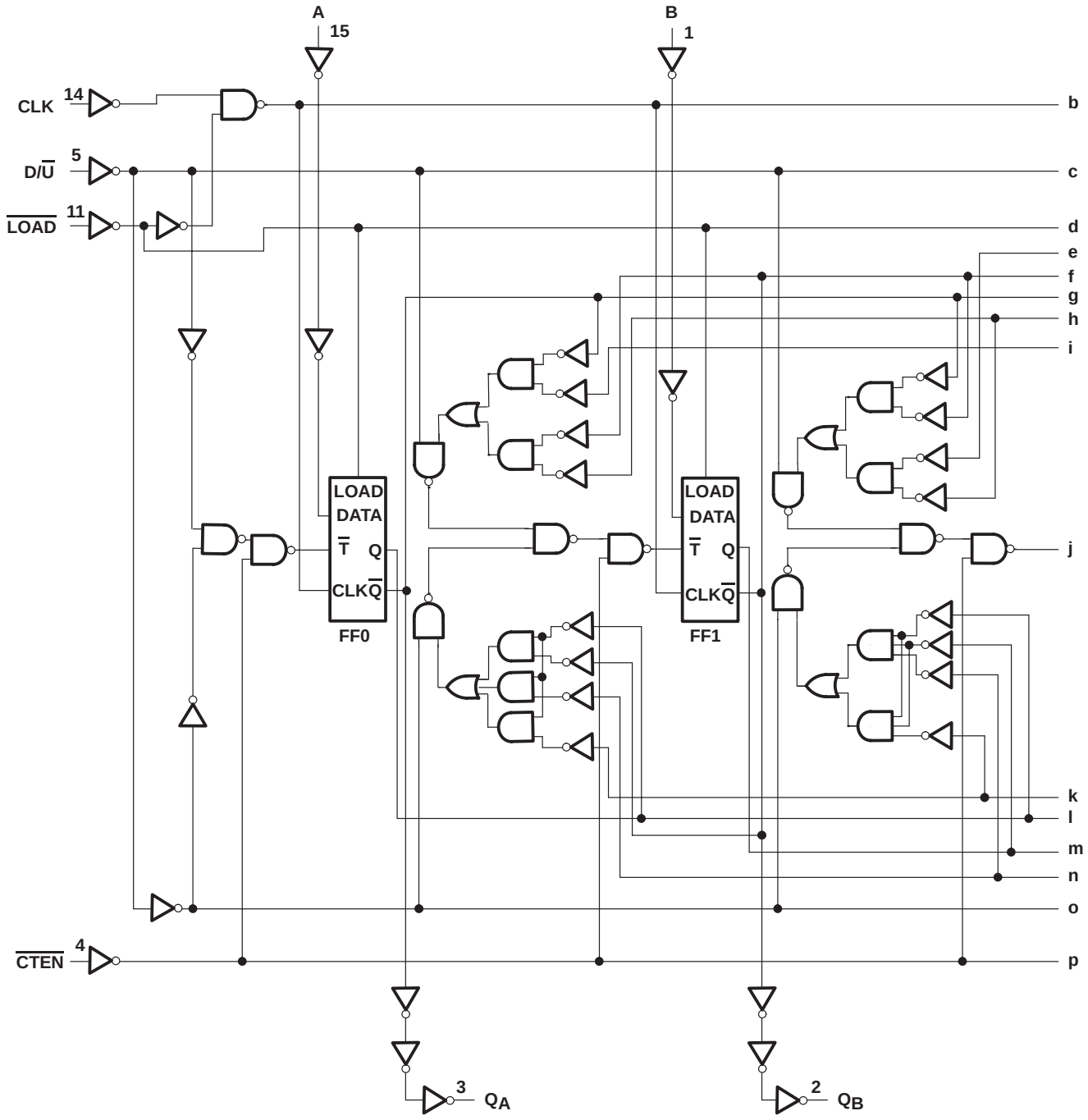
If a decade counter is preset to an illegal state or assumes an illegal state when power is applied, it returns to the normal sequence in one or two counts, as shown in the state diagrams (see Figure 3).

FUNCTION TABLE

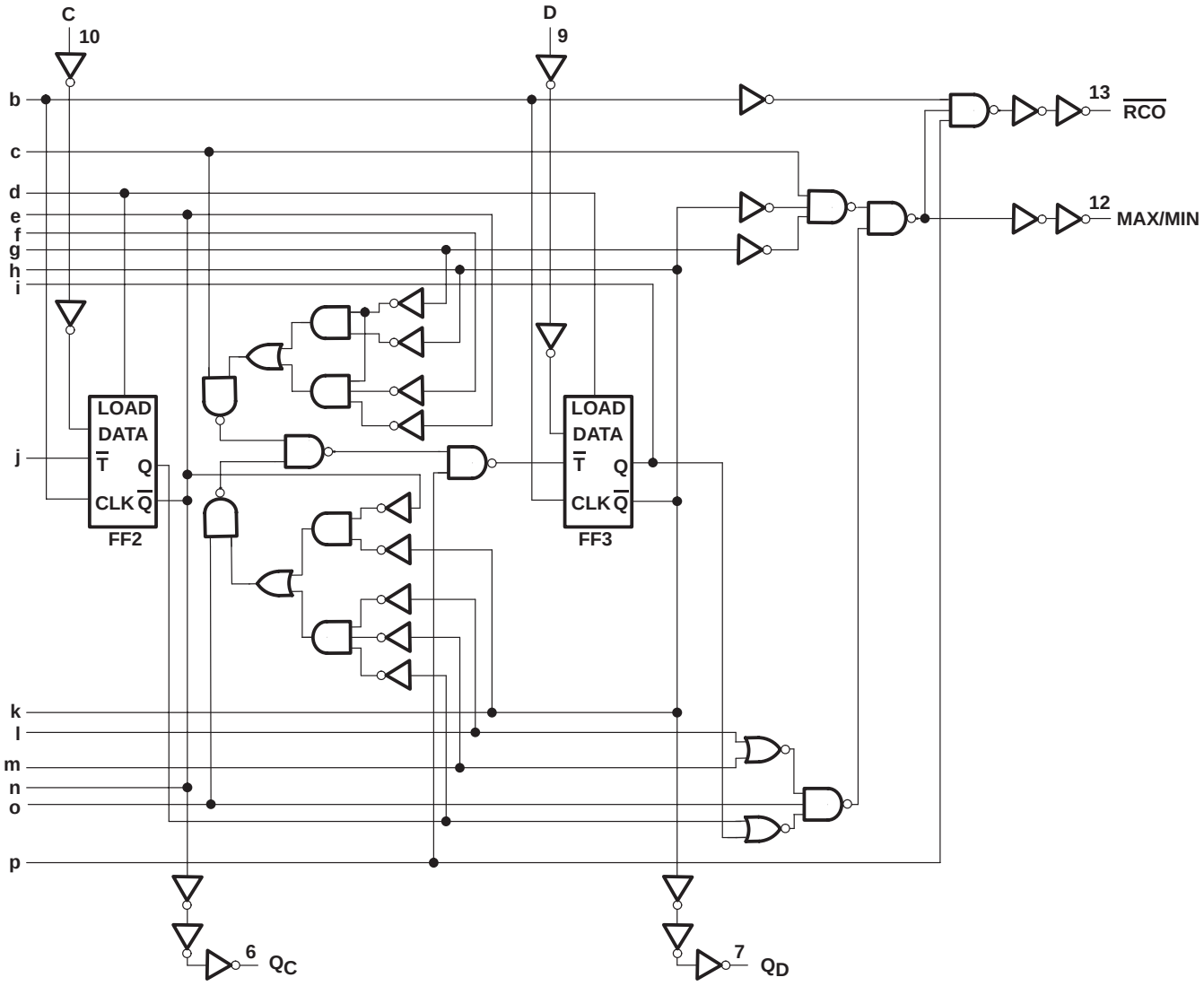
INPUTS				FUNCTION
$\overline{LOAD}$	$\overline{CTEN}$	D/$\overline{U}$	CLK	
H	L	L	⌐	Count up
H	L	H	⌐	Count down
L	X	X	X	Asynchronous preset
H	H	X	X	No change

D/$\overline{U}$ or $\overline{CTEN}$ should be changed only when clock is high.
X = Don't care
⌐ Low-to-high clock transition

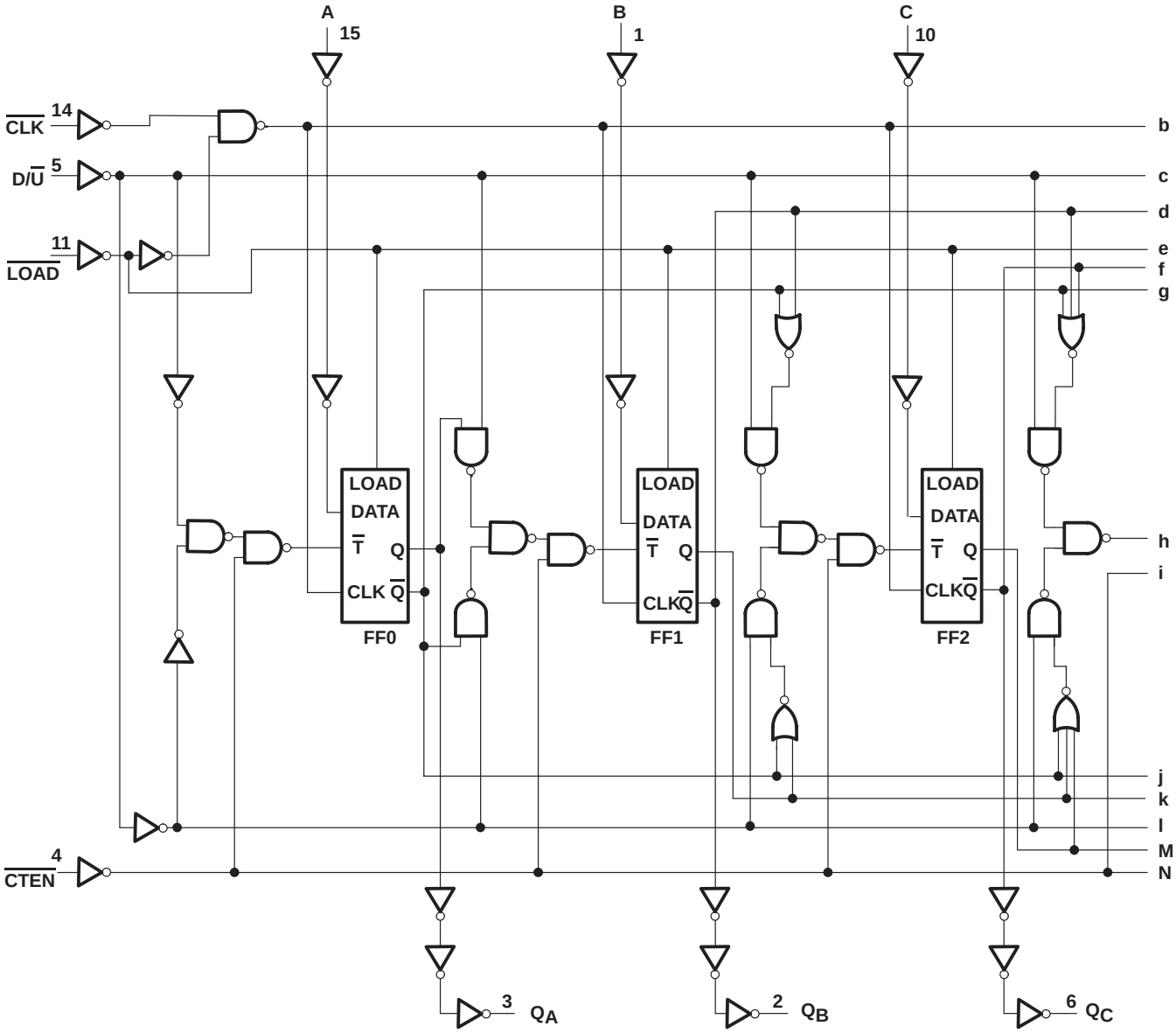
'HC190 logic diagram



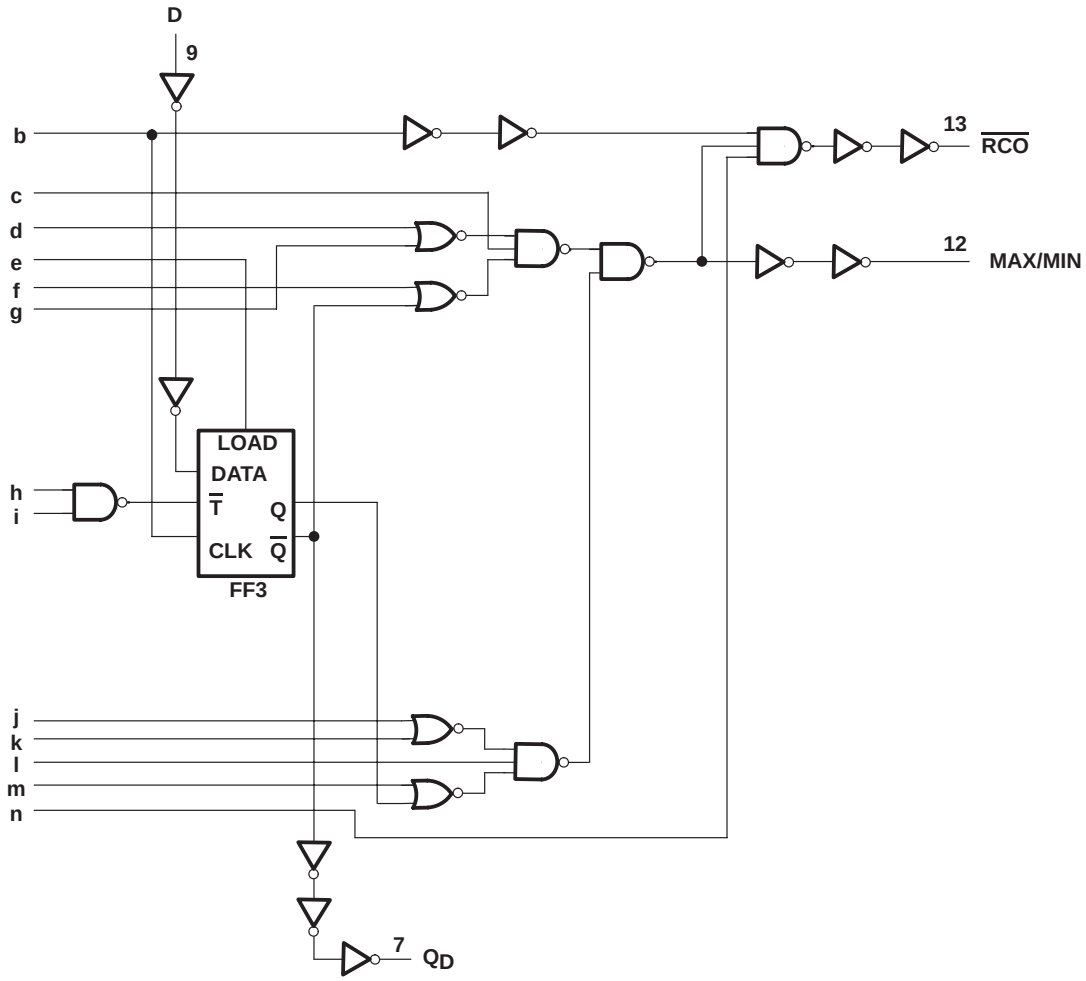
'HC190 logic diagram (continued)



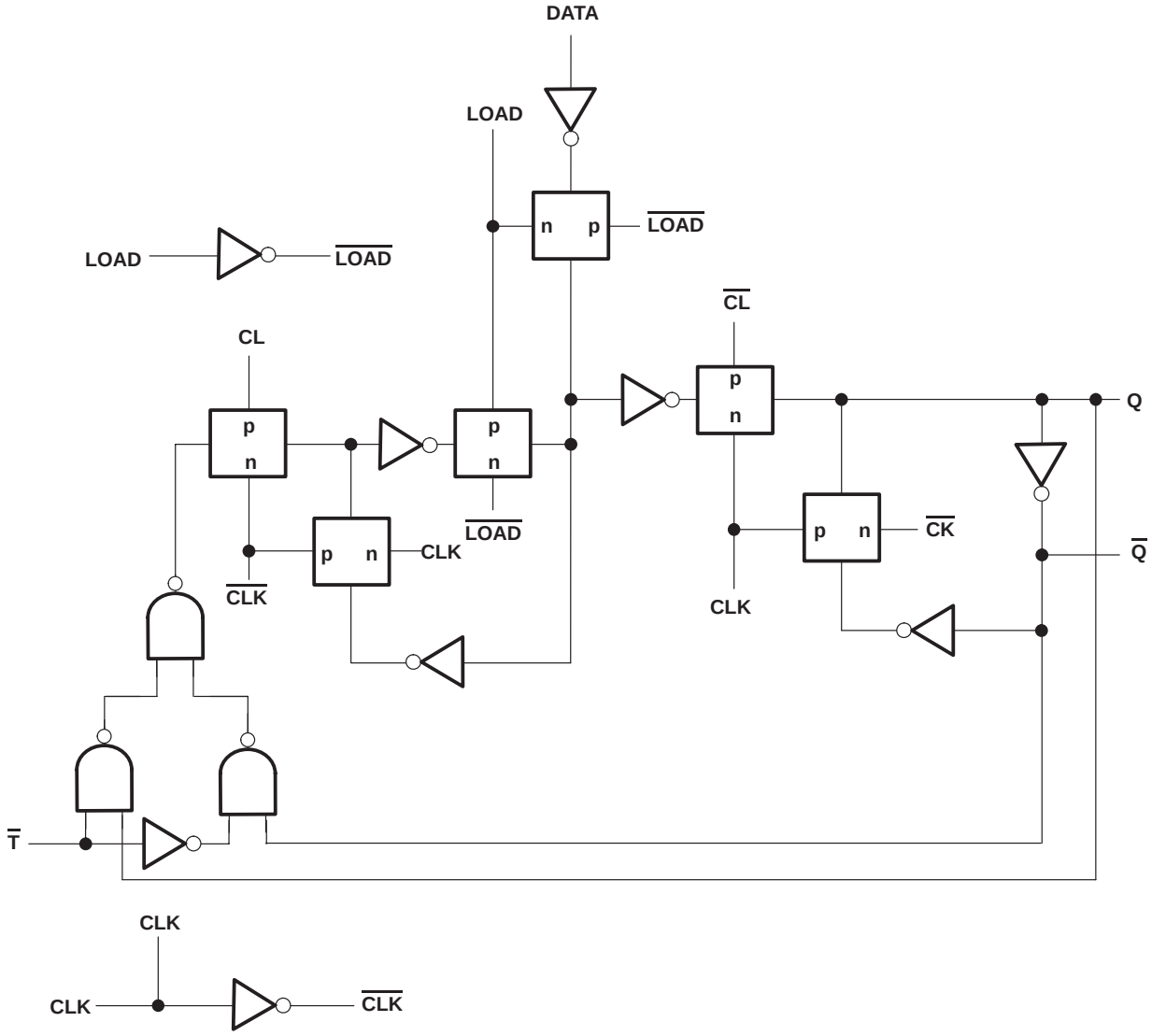
'HC191, 'HCT191 logic diagram



'HC191, 'HCT191 logic diagram (continued)



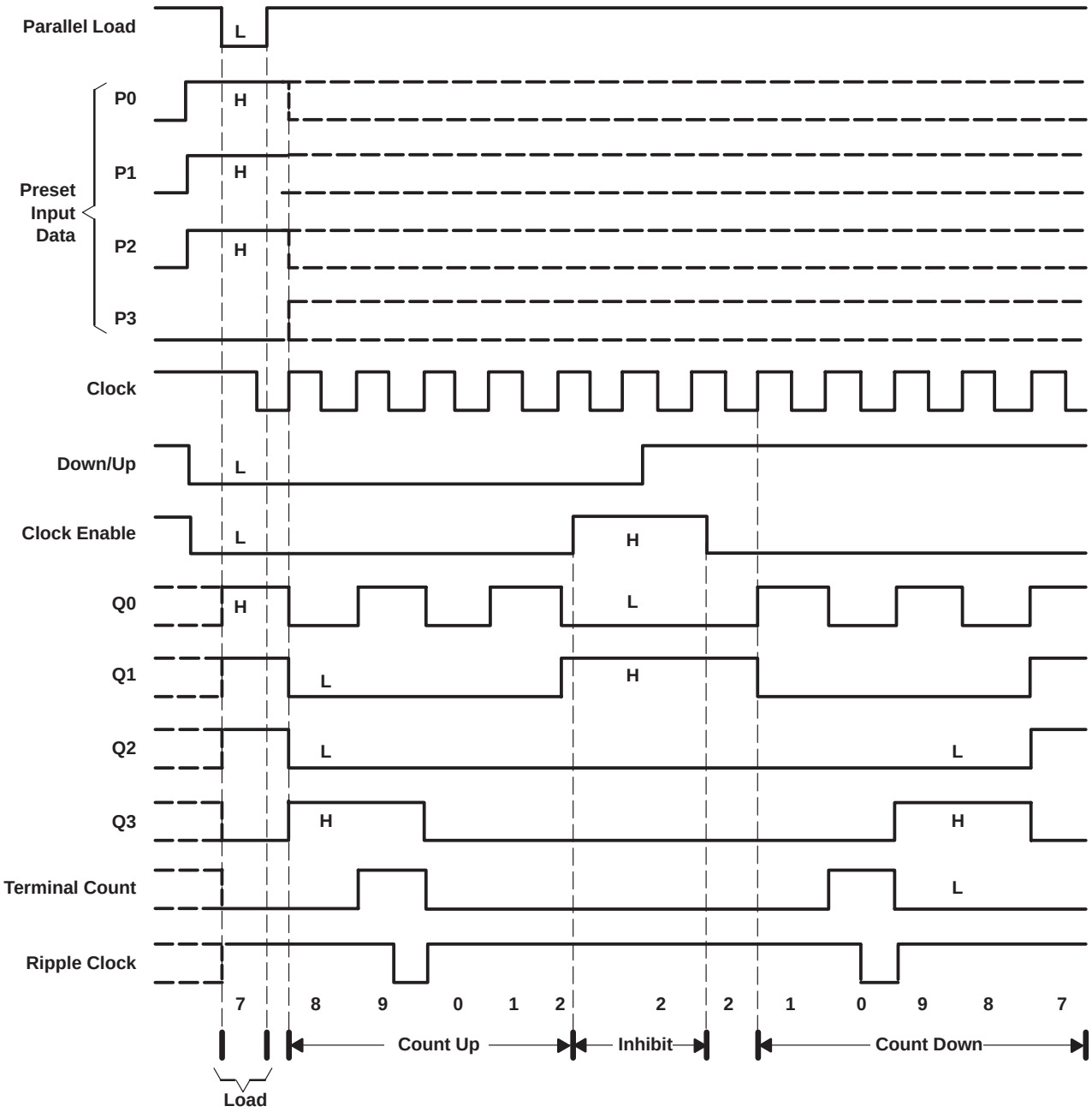
'HC190 and 'HC191/HCT191 flip-flop



typical load, count, and inhibit sequence for ’HC190

The following sequence is illustrated below:

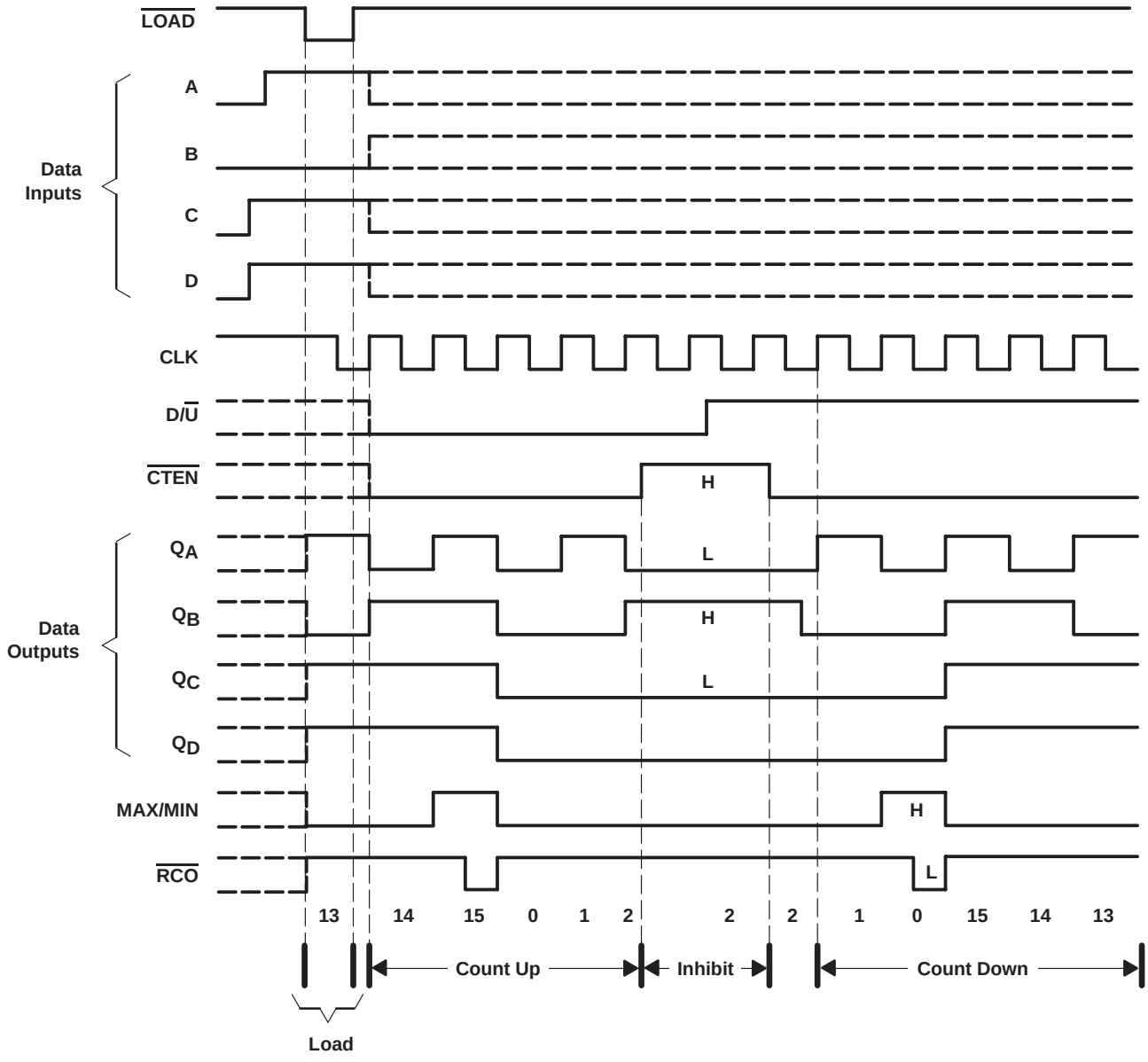
1. Load (preset) to BCD 7
2. Count up to 8, 9 (maximum), 0, 1, and 2
3. Inhibit
4. Count down to 1, 0 (minimum), 9, 8, and 7



typical load, count, and inhibit sequence for ’HC191 and ’HCT191

The following sequence is illustrated below:

1. Load (preset) to binary 13
2. Count up to 14, 15 (maximum), 0, 1, and 2
3. Inhibit
4. Count down to 1, 0 (minimum), 15, 14, and 13



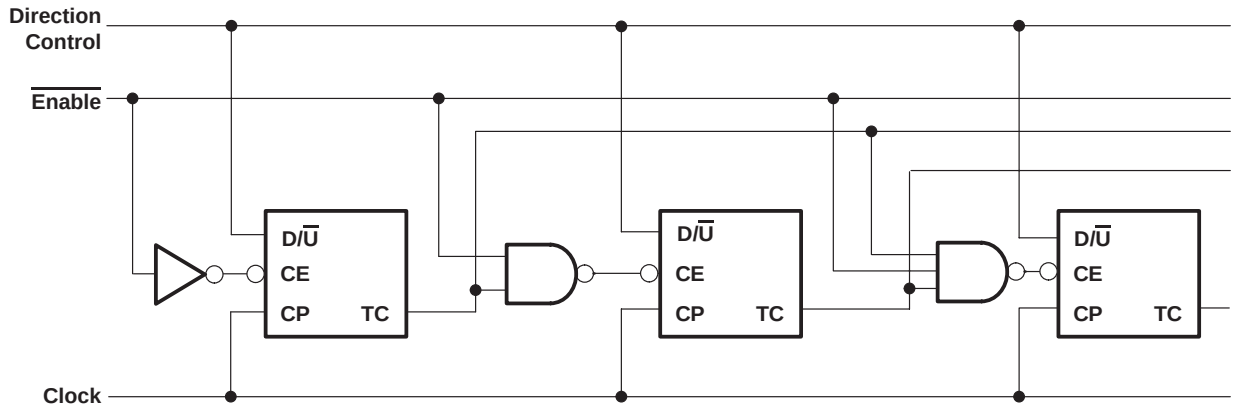


Figure 1. 'HC190 Synchronous n-Stage Counter With Parallel Gated Terminal Count

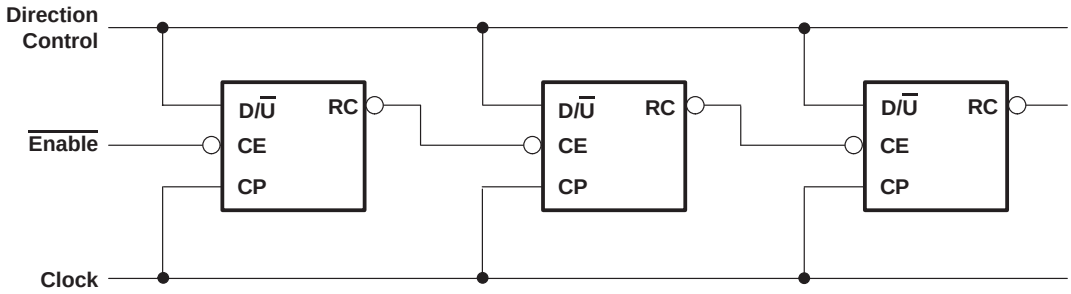
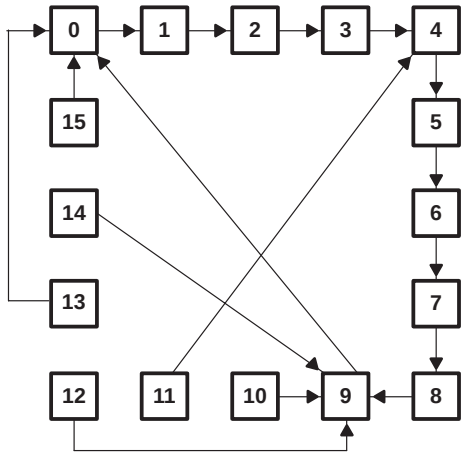
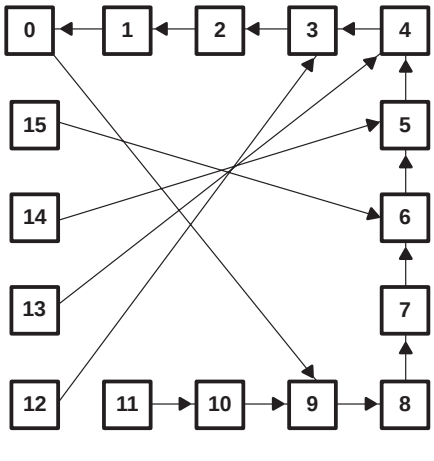


Figure 2. 'HC191, 'HCT191 Synchronous n-Stage Counter With Parallel Gated Terminal Count



Count Up

NOTE: Illegal states in BCD counters corrected in one count



Count Down

NOTE: Illegal states in BCD counters corrected in one or two counts

Figure 3. 'HC190 State Diagram

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) . . . . . ±20 mA
Continuous output drain current per output, I_O ($V_O = 0$ to V_{CC}) . . . . . ±35 mA
Continuous output source or sink current per output, I_O ($V_O = 0$ to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND . . . . . ±50 mA
Package thermal impedance, θ_{JA} (see Note 2): E package . . . . . 67°C/W
M package . . . . . 73°C/W
NS package . . . . . 64°C/W
PW package . . . . . 108°C/W
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions for ’HC190 and ’HC191 (see Note 3)

			T_A = 25°C		T_A = −55°C TO 125°C		T_A = −40°C TO 85°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	6	2	6	2	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		1.5		V
		V_{CC} = 4.5 V	3.15		3.15		3.15		
		V_{CC} = 6 V	4.2		4.2		4.2		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5		0.5	V
		V_{CC} = 4.5 V		1.35		1.35		1.35	
		V_{CC} = 6 V		1.8		1.8		1.8	
V_I	Input voltage		0	V_{CC}	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	0	V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V		1000		1000		1000	ns
		V_{CC} = 4.5 V		500		500		500	
		V_{CC} = 6 V		400		400		400	

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

recommended operating conditions for ’HCT191 (see Note 4)

		T_A = 25°C		T_A = −55°C TO 125°C		T_A = −40°C TO 85°C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		2		V
V_{IL}	Low-level input voltage		0.8		0.8		0.8	V
V_I	Input voltage		V_{CC}		V_{CC}		V_{CC}	V
V_O	Output voltage		V_{CC}		V_{CC}		V_{CC}	V
t_t	Input transition (rise and fall) time		500		500		500	ns

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

'HC190, 'HC191

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C		T_A = −55°C TO 125°C		T_A = −40°C TO 85°C		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = −20 μA	2 V	1.9		1.9		1.9		V
			4.5 V	4.4		4.4		4.4		
			6 V	5.9		5.9		5.9		
		I_{OH} = −4 mA	4.5 V	3.98		3.7		3.84		
		I_{OH} = −5.2 mA	6 V	5.48		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.1		0.1		0.1	V
			4.5 V		0.1		0.1		0.1	
			6 V		0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V		±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or 0, I_O = 0		6 V		8		160		80	μA
C_i					10		10		10	pF

'HCT191

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			T_A = −55°C TO 125°C		T_A = −40°C TO 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = −20 μA	4.5 V	4.4			4.4		4.4		V
		I_{OH} = −4 mA		3.98			3.7		3.84		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	4.5 V			0.1		0.1		0.1	V
		I_{OL} = 4 mA				0.26		0.4		0.33	
I_I	V_I = V_{CC} to GND		5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or 0, I_O = 0		5.5 V			8		160		80	μA
ΔI_{CC}†	One input at V_{CC} − 2.1 V, Other inputs at 0 or V_{CC}		4.5 V to 5.5 V		100	360		490		450	μA
C_i						10		10		10	pF

† Additional quiescent supply current per input pin, TTL inputs high, 1 unit load

HCT INPUT LOADING TABLE

INPUTS	UNIT LOADS
A-D	0.4
CLK	1.5
$\overline{\text{LOAD}}$	1.5
D/$\overline{\text{U}}$	1.2
$\overline{\text{CTEN}}$	1.5

Unit load is ΔI_{CC} limit specified in electrical characteristics table, (e.g., 360 μA max at 25°C).

'HC190, 'HC191 timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 4)

			V_{CC}	T_A = 25°C		T_A = −55°C TO 125°C		T_A = −40°C TO 85°C		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency†		2 V		6		4		5	MHz
			4.5 V		30		20		25	
			6 V		35		23		29	
t_w	Pulse duration	$\overline{LOAD}$ low	2 V	80		120		100		ns
			4.5 V	16		24		20		
			6 V	14		20		17		
		CLK high or low	2 V	100		150		125		
			4.5 V	20		30		25		
			6 V	17		26		21		
t_{su}	Setup time	Data before $\overline{LOAD}$↑	2 V	60		90		75		ns
			4.5 V	12		18		15		
			6 V	10		15		13		
		$\overline{CTEN}$ before CLK↑	2 V	60		90		75		
			4.5 V	12		18		15		
			6 V	10		15		13		
		D/$\overline{U}$ before CLK↑	2 V	90		135		115		
			4.5 V	18		27		23		
			6 V	15		23		20		
t_h	Hold time	Data before $\overline{LOAD}$↑	2 V	2		2		2		ns
			4.5 V	2		2		2		
			6 V	2		2		2		
		$\overline{CTEN}$ before CLK↑	2 V	2		2		2		
			4.5 V	2		2		2		
			6 V	2		2		2		
		D/$\overline{U}$ before CLK↑	2 V	0		0		0		
			4.5 V	0		0		0		
			6 V	0		0		0		
t_{rec}	Recovery time	$\overline{LOAD}$ inactive before CLK↑	2 V	60		90		75		ns
			4.5 V	12		18		15		
			6 V	10		15		13		

† Applies to noncascaded operation only. With cascaded counters, clock-to-terminal count propagation delays, $\overline{CTEN}$-to-clock setup times, and $\overline{CTEN}$-to-clock hold times determine maximum clock frequency. For example, with these HC devices:

$$f_{max}(CLK) = \frac{1}{\text{CLK-to-MAX/MIN propagation delay} + \overline{CTEN}\text{-to-CLK setup time} + \overline{CTEN}\text{-to-CLK hold time}} = \frac{1}{42 + 12 + 2} \approx 18 \text{ MHz}$$

'HC190, 'HC191

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	T_A = 25°C			T_A = −55°C TO 125°C		T_A = −40°C TO 85°C		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}				2 V	6			4		5		MHz
				4.5 V	30			20		25		
				6 V	35			23		29		
t_{pd}	$\overline{LOAD}$	Q	C_L = 50 pF	2 V			195		295		245	ns
				4.5 V			39		59		49	
				6 V			33		50		42	
			C_L = 15 pF	5 V		16						
	A, B, C, or D	Q	C_L = 50 pF	2 V			175		265		220	
				4.5 V			35		53		44	
				6 V			30		45		37	
			C_L = 15 pF	5 V		14						
	CLK	Q	C_L = 50 pF	2 V			170		255		215	
				4.5 V			34		51		43	
				6 V			29		43		37	
			C_L = 15 pF	5 V		14						
	CLK	$\overline{RCO}$	C_L = 50 pF	2 V			125		190		155	
				4.5 V			25		38		31	
				6 V			21		32		26	
			C_L = 15 pF	5 V		10						
	CLK	MAX/MIN	C_L = 50 pF	2 V			210		315		265	
				4.5 V			42		63		53	
				6 V			36		54		45	
			C_L = 15 pF	5 V		18						
	D/$\overline{U}$	$\overline{RCO}$	C_L = 50 pF	2 V			150		225		190	
				4.5 V			30		45		38	
				6 V			26		38		33	
			C_L = 15 pF	5 V		12						
	D/$\overline{U}$	MAX/MIN	C_L = 50 pF	2 V			165		250		205	
				4.5 V			33		50		41	
				6 V			28		43		35	
			C_L = 15 pF	5 V		13						
	$\overline{CTEN}$	$\overline{RCO}$	C_L = 50 pF	2 V			125		190		155	
				4.5 V			25		38		31	
				6 V			21		32		26	
			C_L = 15 pF	5 V		10						
t_t		Any	C_L = 50 pF	2 V			75		110		95	ns
				4.5 V			15		22		19	
				6 V			13		19		16	

'HCT191

timing requirements over recommended operating free-air temperature range V_{CC} = 4.5 V (unless otherwise noted) (see Figure 5)

			T_A = 25°C		T_A = −55°C TO 125°C		T_A = −40°C TO 85°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			30		20		25	MHz
t_w	Pulse duration	$\overline{LOAD}$ low	16		24		20		ns
		CLK high or low	20		30		25		
t_{su}	Setup time	Data before $\overline{LOAD}\uparrow$	12		18		15		ns
		$\overline{CTEN}$ before CLK$\uparrow$	12		18		15		
		D/$\overline{U}$ before CLK$\uparrow$	18		27		23		
t_h	Hold time	Data before $\overline{LOAD}\uparrow$	2		2		2		ns
		$\overline{CTEN}$ before CLK$\uparrow$	2		2		2		
		D/$\overline{U}$ before CLK$\uparrow$	0		0		0		
t_{rec}	Recovery time	$\overline{LOAD}$ inactive before CLK$\uparrow$	12		18		15		ns

'HCT191

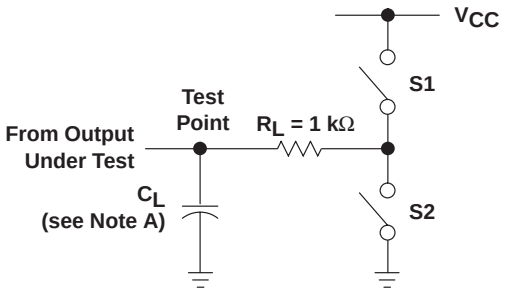
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	T_A = 25°C			T_A = −55°C TO 125°C		T_A = −40°C TO 85°C		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}				4.5 V	30			20		25		MHz
t_{pd}	$\overline{LOAD}$	Q	C_L = 50 pF	4.5 V			40		60		50	ns
			C_L = 15 pF	5 V		17						
	A, B, C, or D	Q	C_L = 50 pF	4.5 V			38		57		48	
			C_L = 15 pF	5 V		16						
	CLK	$\overline{RCO}$	C_L = 50 pF	4.5 V			35		53		44	
			C_L = 15 pF	5 V		14						
	CLK	Q	C_L = 50 pF	4.5 V			27		41		34	
			C_L = 15 pF	5 V		11						
	CLK	MAX/MIN	C_L = 50 pF	4.5 V			42		63		53	
			C_L = 15 pF	5 V		18						
	D/$\overline{U}$	$\overline{RCO}$	C_L = 50 pF	4.5 V			30		45		38	
			C_L = 15 pF	5 V		12						
	D/$\overline{U}$	MAX/MIN	C_L = 50 pF	4.5 V			38		57		48	
			C_L = 15 pF	5 V		16						
	$\overline{CTEN}$	$\overline{RCO}$	C_L = 50 pF	4.5 V			27		41		34	
			C_L = 15 pF	5 V		11						
t_t		Any	C_L = 50 pF	4.5 V			15		22		19	ns

operating characteristics, V_{CC} = 5 V, T_A = 25°C

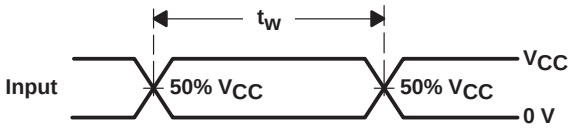
PARAMETER			TYP	UNIT
C_{pd}	Power dissipation capacitance	'HC190	59	pF
		'HC191	55	
		'HCT191	68	

PARAMETER MEASUREMENT INFORMATION − ’HC190, ’HC191

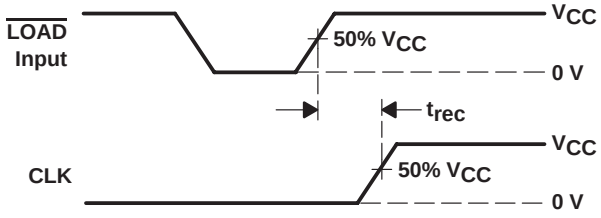


LOAD CIRCUIT

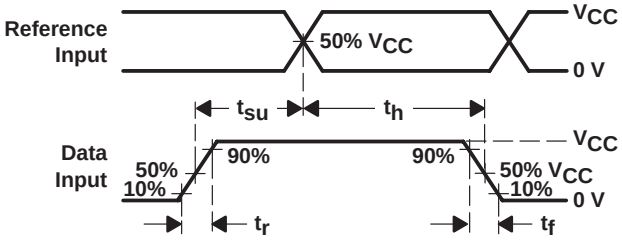
PARAMETER		S1	S2
t_{en}	t_{PZH}	Open	Closed
	t_{PZL}	Closed	Open
t_{dis}	t_{PHZ}	Open	Closed
	t_{PLZ}	Closed	Open
t_{pd} or t_t		Open	Open



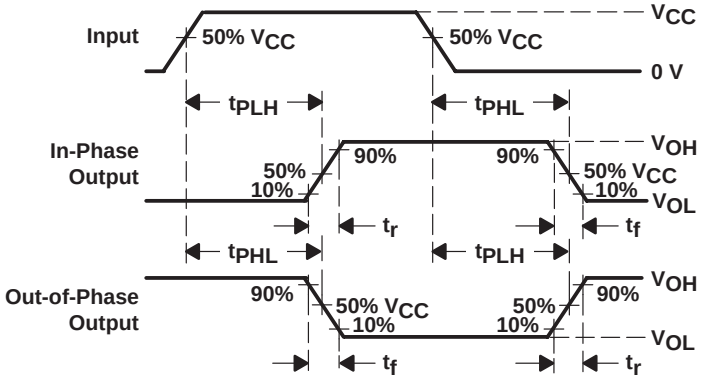
VOLTAGE WAVEFORMS
PULSE DURATION



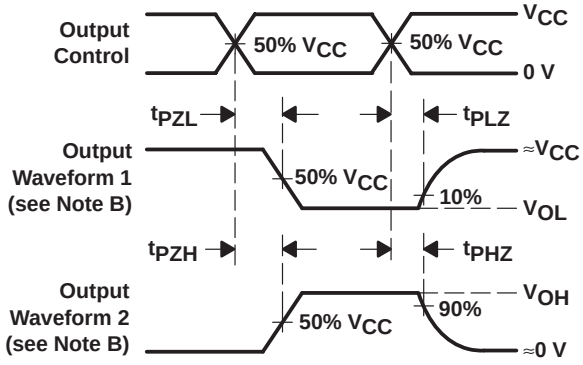
VOLTAGE WAVEFORMS
RECOVERY TIME



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

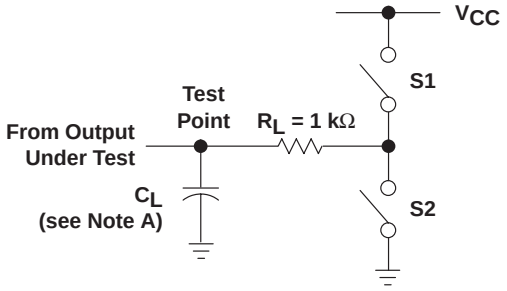


VOLTAGE WAVEFORMS
OUTPUT ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
E. The outputs are measured one at a time with one input transition per measurement.
F. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
G. t_{PZL} and t_{PZH} are the same as t_{en}.
H. t_{PLH} and t_{PHL} are the same as t_{pd}.

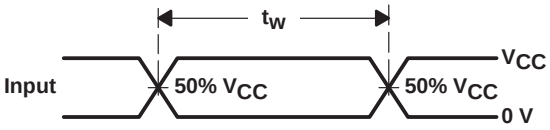
Figure 4. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION − ’HCT191

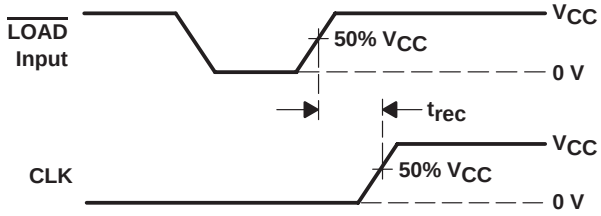


LOAD CIRCUIT

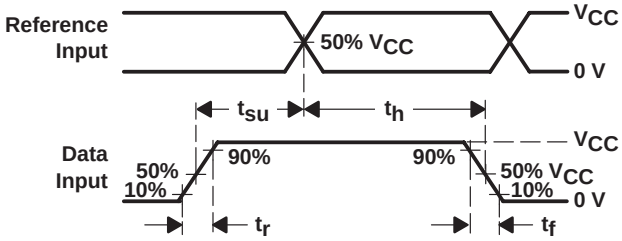
PARAMETER		S1	S2
t_{en}	t_{PZH}	Open	Closed
	t_{PZL}	Closed	Open
t_{dis}	t_{PHZ}	Open	Closed
	t_{PLZ}	Closed	Open
t_{pd} or t_t		Open	Open



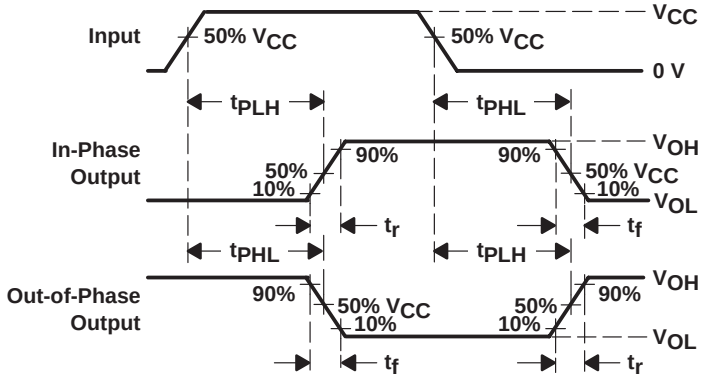
VOLTAGE WAVEFORMS
PULSE DURATION



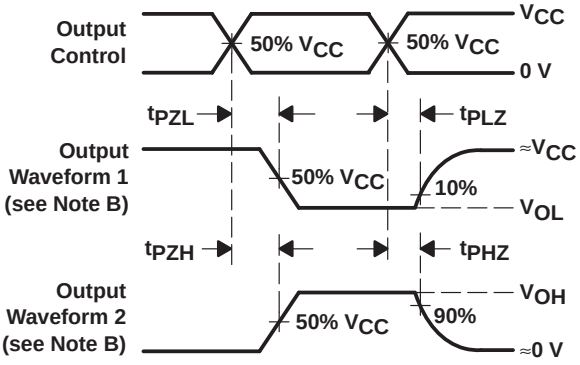
VOLTAGE WAVEFORMS
RECOVERY TIME



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS
OUTPUT ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
E. The outputs are measured one at a time with one input transition per measurement.
F. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
G. t_{PZL} and t_{PZH} are the same as t_{en}.
H. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 5. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-8867101EA	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8867101EA CD54HCT191F3A
5962-8994601EA	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8994601EA CD54HC190F3A
CD54HC190F3A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8994601EA CD54HC190F3A
CD54HC190F3A.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8994601EA CD54HC190F3A
CD54HC191F3A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8689101EA CD54HC191F3A
CD54HC191F3A.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8689101EA CD54HC191F3A
CD54HCT191F3A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8867101EA CD54HCT191F3A
CD54HCT191F3A.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8867101EA CD54HCT191F3A
CD74HC190E	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC190E
CD74HC190E.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC190E
CD74HC190NSR	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC190M
CD74HC190NSR.A	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC190M
CD74HC190PW	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-55 to 125	HJ190
CD74HC190PWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ190
CD74HC190PWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ190
CD74HC191E	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC191E
CD74HC191E.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC191E
CD74HC191M	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	HC191M
CD74HC191M96	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC191M
CD74HC191M96.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC191M
CD74HC191MT	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	HC191M
CD74HCT191E	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT191E
CD74HCT191E.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT191E

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD74HCT191M	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT191M
CD74HCT191M.A	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT191M

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD54HC190, CD54HC191, CD54HCT191, CD74HC190, CD74HC191, CD74HCT191 :

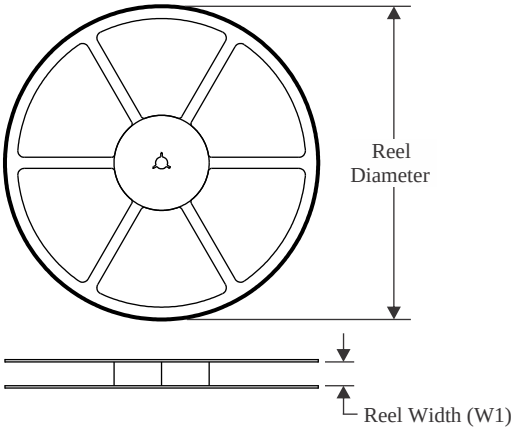
- Catalog : CD74HC190, CD74HC191, CD74HCT191
- Military : CD54HC190, CD54HC191, CD54HCT191

NOTE: Qualified Version Definitions:

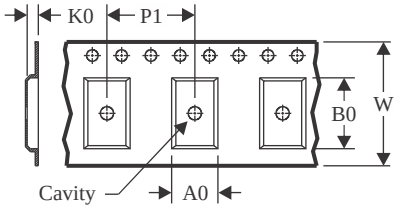
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

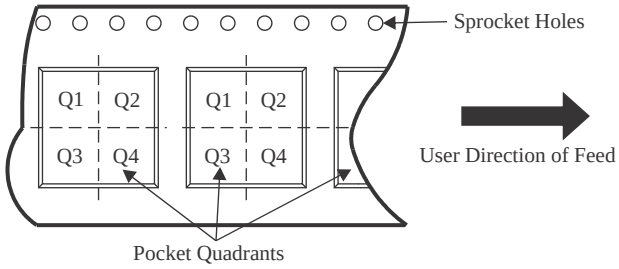


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

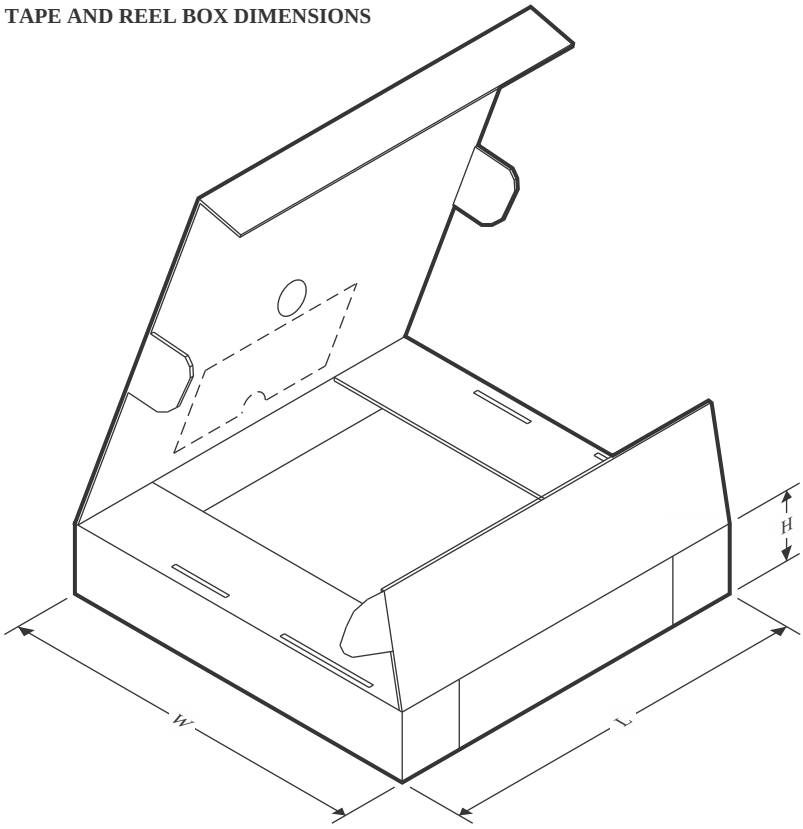
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC190NSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
CD74HC190PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC191M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

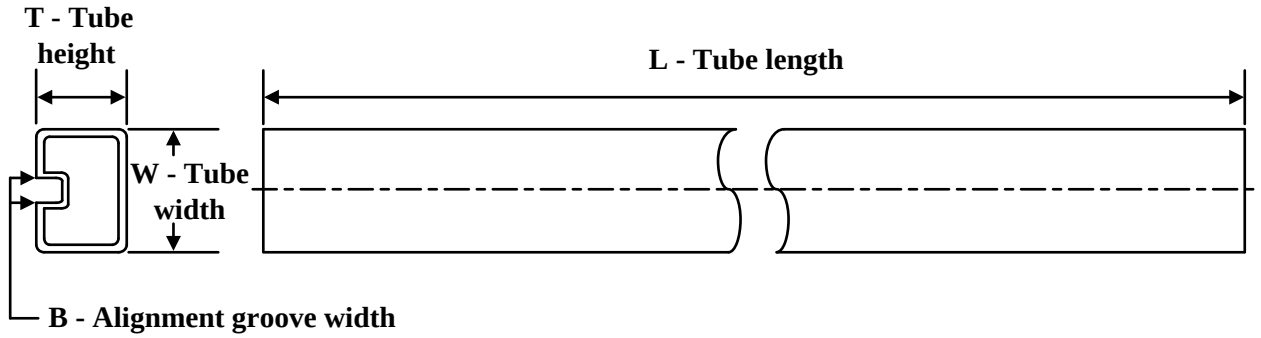
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

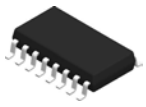
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC190NSR	SOP	NS	16	2000	353.0	353.0	32.0
CD74HC190PWR	TSSOP	PW	16	2000	353.0	353.0	32.0
CD74HC191M96	SOIC	D	16	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74HC190E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC190E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC190E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC190E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC191E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC191E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC191E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC191E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT191E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT191E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT191E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT191E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT191M	D	SOIC	16	40	507	8	3940	4.32
CD74HCT191M.A	D	SOIC	16	40	507	8	3940	4.32

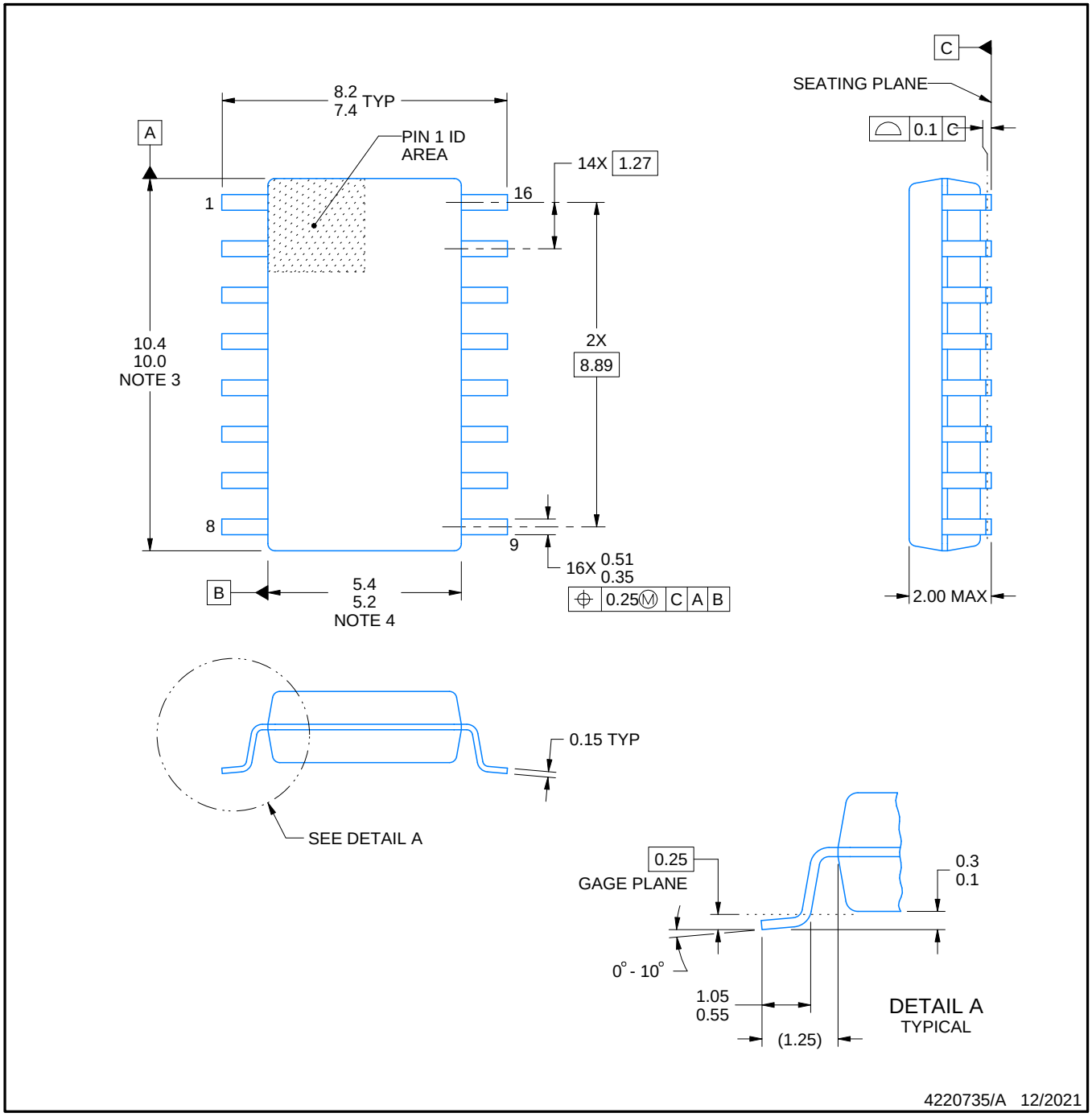


PACKAGE OUTLINE

NS0016A

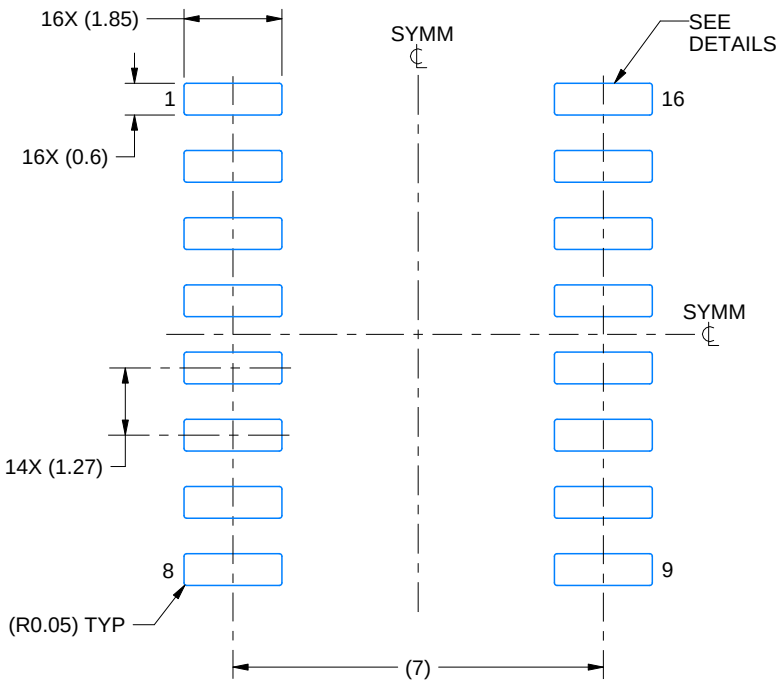
SOP - 2.00 mm max height

SOP

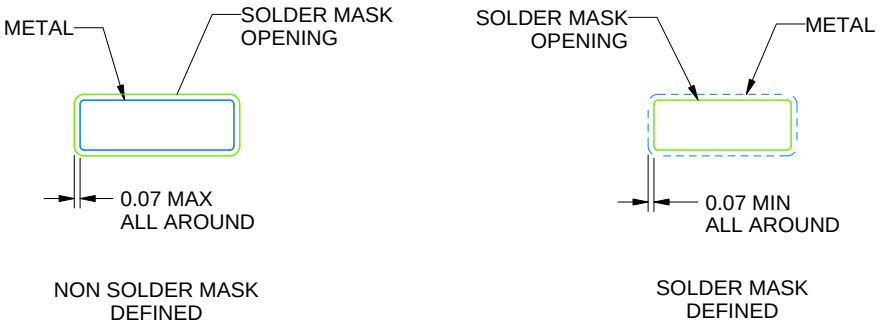


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X



NON SOLDER MASK
DEFINED

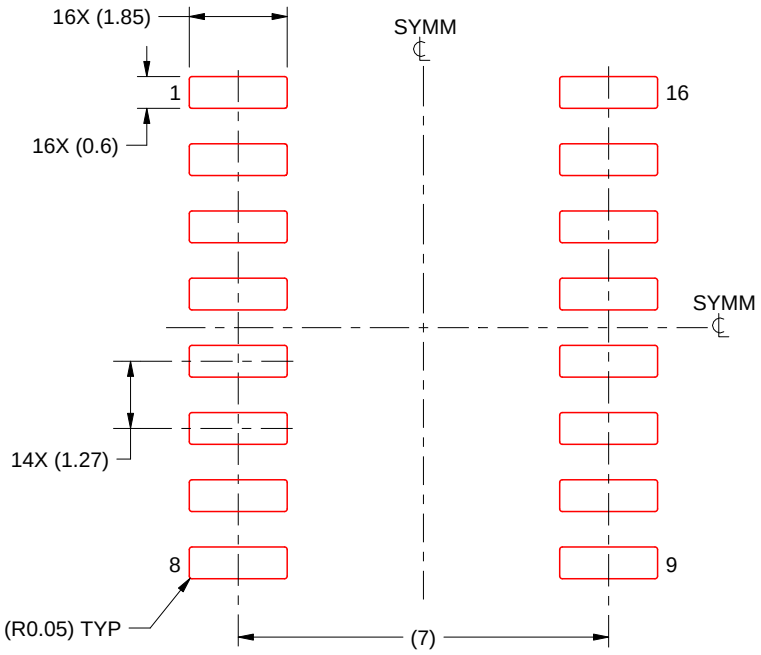
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



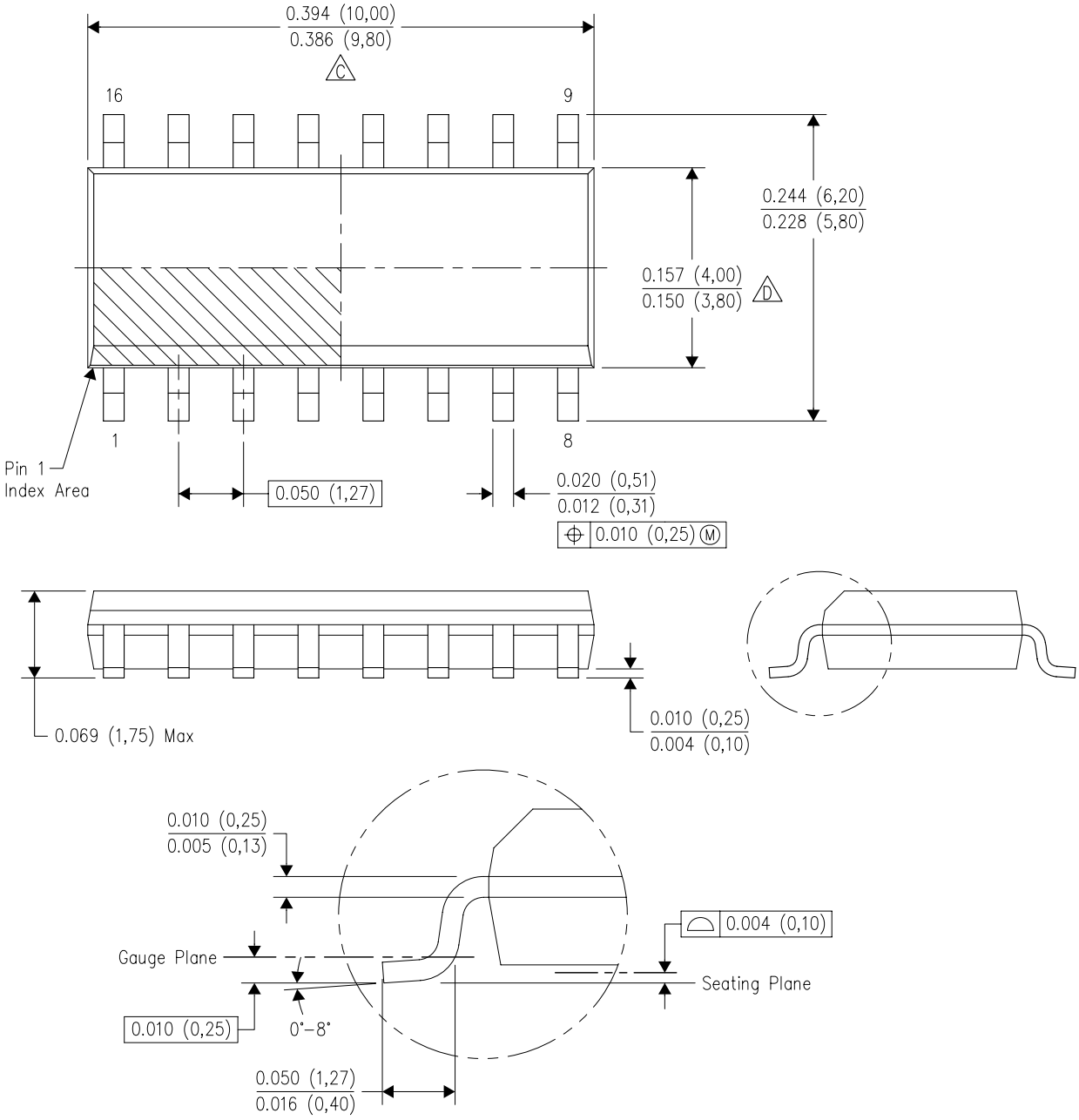
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

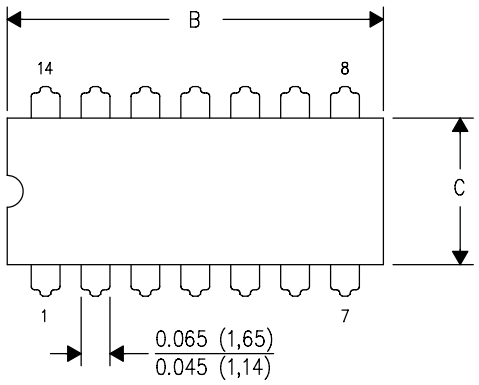


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

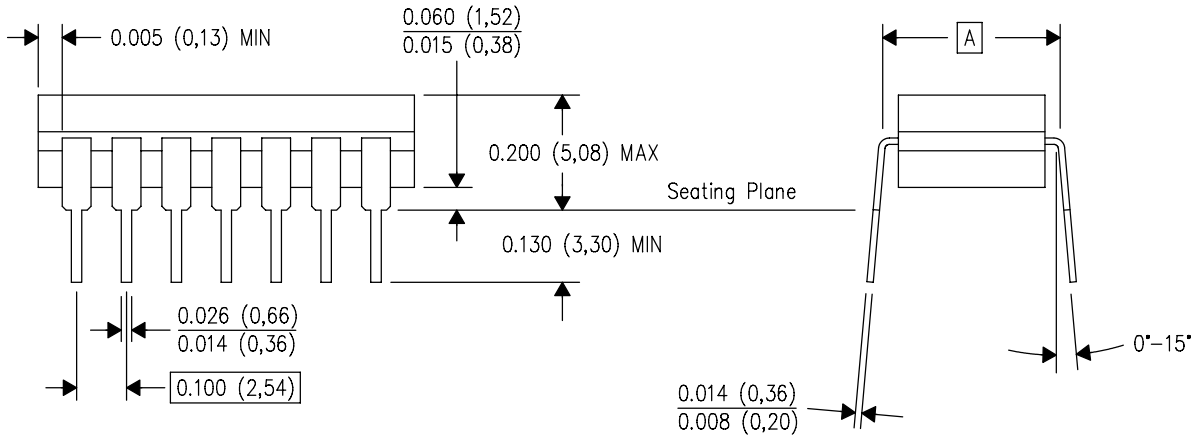
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

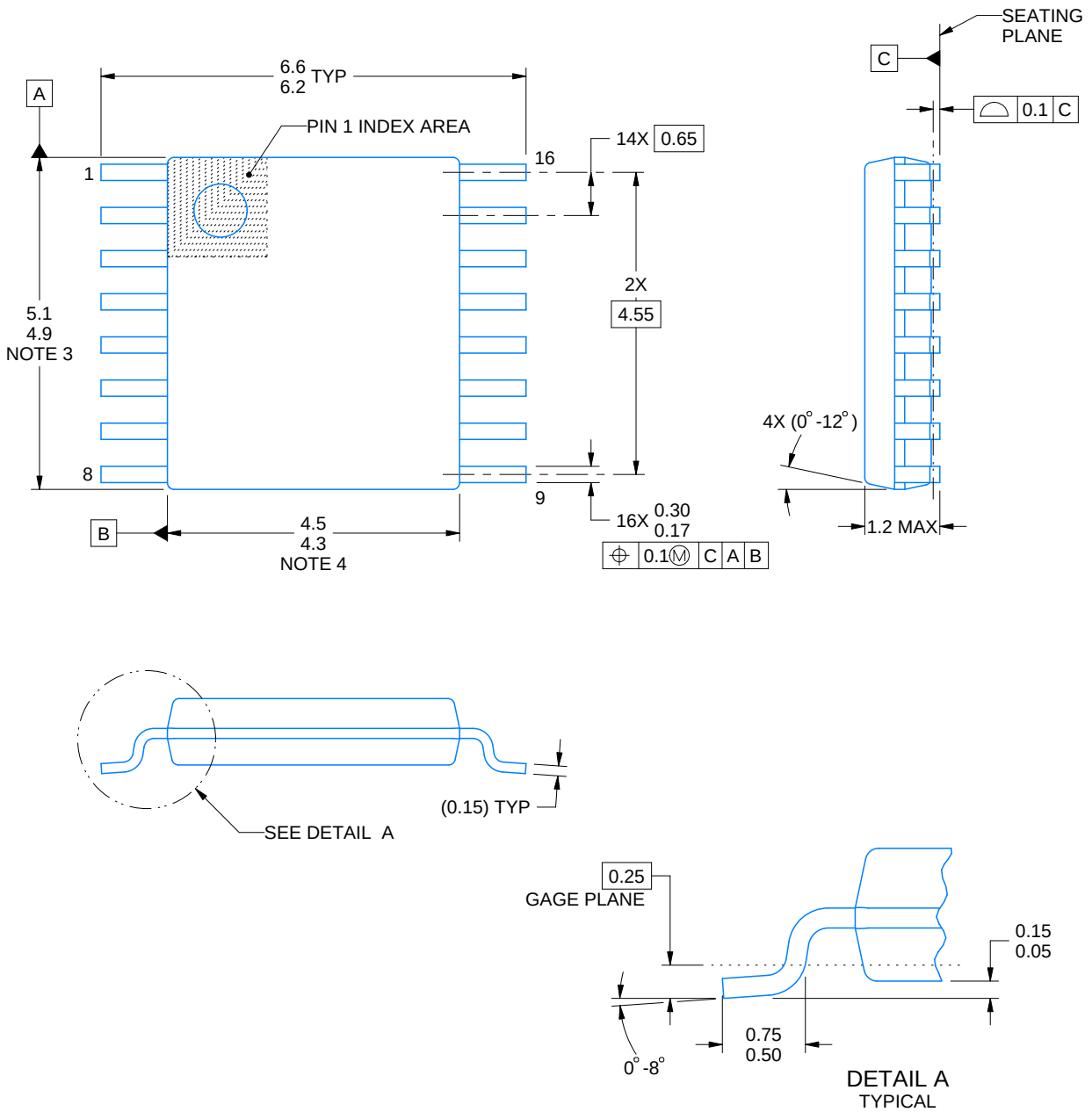
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

PACKAGE OUTLINE

PW0016A

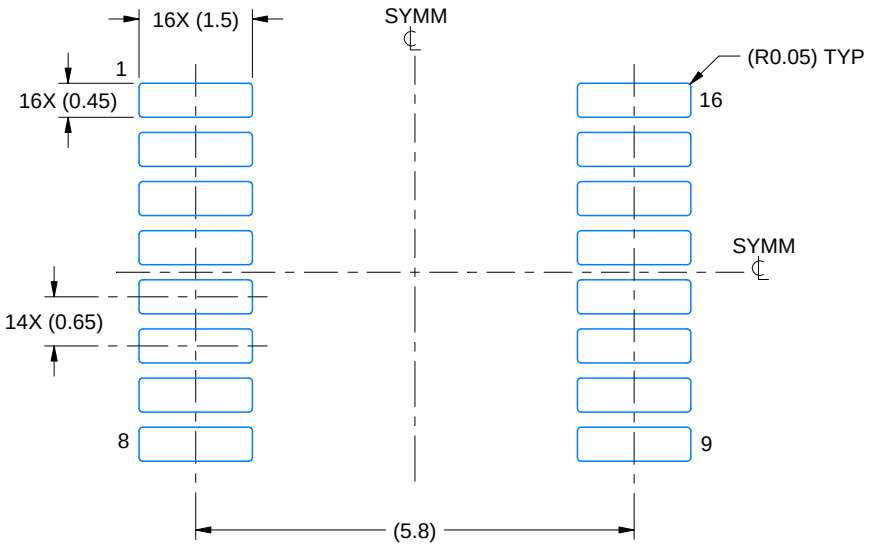
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

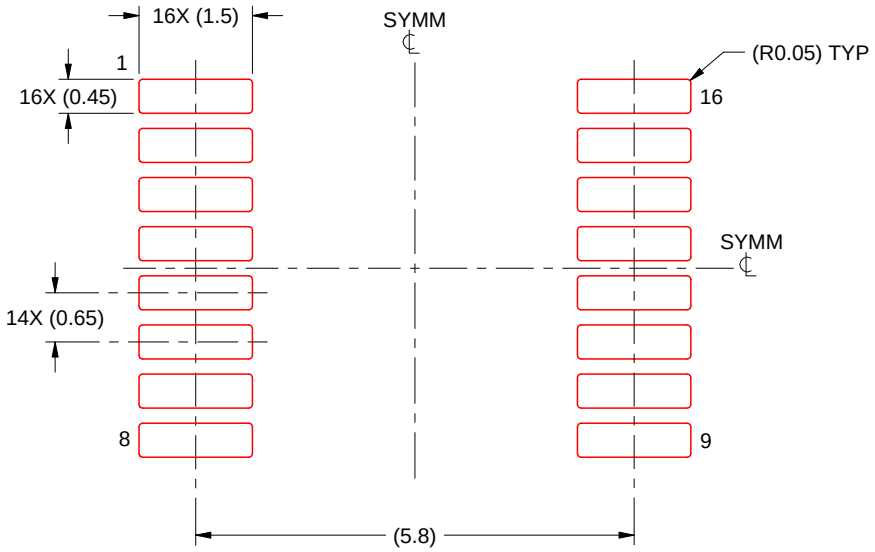


SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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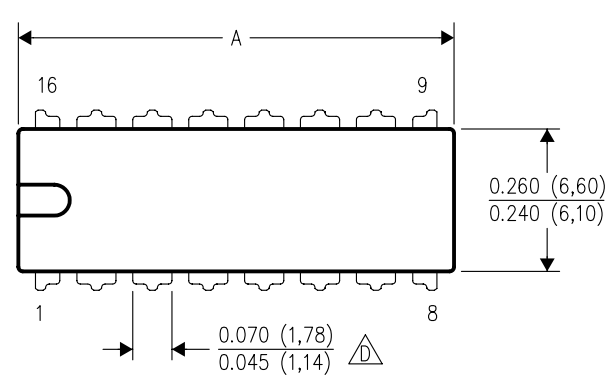
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

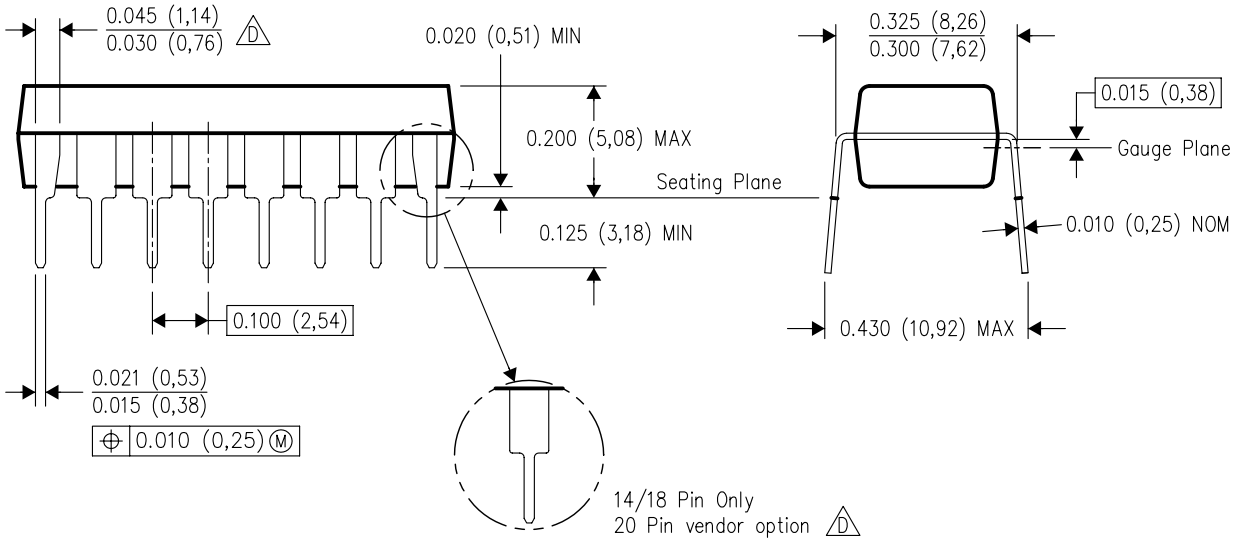
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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