# CDx4HCx4316 High-Speed CMOS Logic Quad Analog Switch with Level Translation

## 1 Features

- Wide analog-input-voltage range:

  $V_{CC}$ - $V_{EE}$: 0V to 10V
- Low ON resistance:
  - 45Ω (typical): $V_{CC}$ = 4.5V
  - 35Ω (typical): $V_{CC}$ = 6V
  - 30Ω (typical): $V_{CC}$ – $V_{EE}$ = 9V
- Fast switching and propagation delay times
- Low OFF leakage current
- Built-in break-before-make switching
- Logic-level translation to enable 5V logic to accommodate ±5 V analog signals
- Wide operating temperature range: -55°C to 125°C
- HC types:
  - 2V to 10V operation
  - High noise immunity: $N_{IL}$ = 30%, $N_{IH}$ = 30% of $V_{CC}$ at $V_{CC}$ = 5V
- HCT types:
  - Direct LSTTL input logic compatibility, $V_{IL}$= 0.8V (maximum), $V_{IH}$ = 2V (minimum)
  - CMOS input compatibility, $I_I \leq 1$ µA at $V_{OL}$, $V_{OH}$

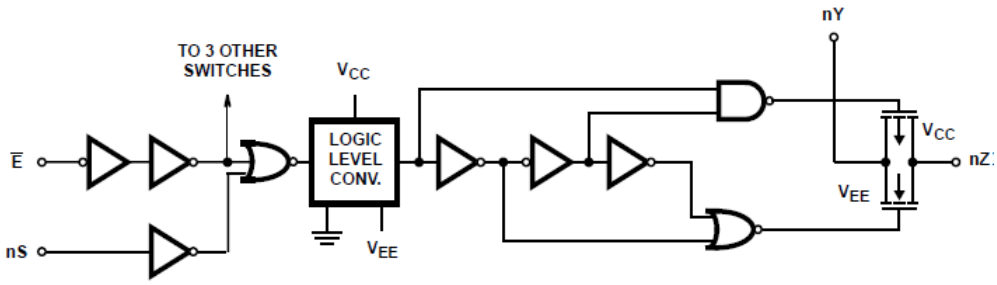
## 2 Description

The ’HC4316 and CD74HCT4316 contain four independent digitally controlled analog switches that use silicon-gate CMOS technology to achieve operating speeds similar to LSTTL with the low power consumption of standard CMOS integrated circuits.

In addition these devices contain logic-level translation circuits that provide for analog signal switching of voltages between ±5V via 5V logic. Each switch is turned on by a high-level voltage on its select input (S) when the common Enable (E) is Low. A High E disables all switches. The digital inputs can swing between $V_{CC}$ and GND; the analog inputs/outputs can swing between $V_{CC}$ as a positive limit and $V_{EE}$ as a negative limit. Voltage ranges are shown in Figure 13-1 and Figure 13-2.

**Device Information**

| Inputs | | Switch |
|---|---|---|
| $\overline{E}$ | S | ON/OFF |
| L | L | OFF |
| L | H | ON |
| H | H | OFF |




**One Switch**

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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# 3 Pin Configurations and Functions

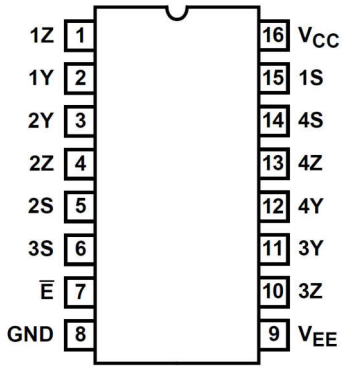



**Figure 3-1. CD74HC4316 (TSSOP)**

**Table 3-1. Pin Functions**

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| 1Z | 1 | I/O | Input/Output for Switch 1 |
| 1Y | 2 | I/O | Input/Output for Switch 1 |
| 2Y | 3 | I/O | Input/Output for Switch 2 |
| 2Z | 4 | I/O | Input/Output for Switch 2 |
| 2S | 5 | I | Control pin for Switch 2 |
| 3S | 6 | I | Control pin for Switch 3 |
| E | 7 | I | Enable Pin |
| GND | 8 | - | Ground Pin |
| $V_{EE}$ | 9 | - | Power Pin |
| 3Z | 10 | I/O | Input/Output for Switch 3 |
| 3Y | 11 | I/O | Input/Output for Switch 3 |
| 4Y | 12 | I/O | Input/Output for Switch 4 |
| 4Z | 13 | I/O | Input/Output for Switch 4 |
| 4S | 14 | I | Control pin for Switch 4 |
| 1S | 15 | I | Control pin for Switch 1 |
| $V_{CC}$ | 16 | - | Power Pin |

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# 4 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC} – V_{EE}$ | DC Supply voltage | | -0.5 | 10.5 | V |
| $V_{CC}$ | | | –0.5 | 7 | V |
| $V_{EE}$ | | | 0.5 | -7 | V |
| $I_{IK}$ | DC input diode current | $V_I < – 0.5$ V or $V_I > V_{CC} + 0.5$ V | –20 | 20 | mA |
| $I_{OK}$ | DC switch diode current | $V_I < V_{EE} – 0.5$ V or $V_I < V_{CC} + 0.5$ V | –25 | 25 | mA |
| $I_{OK}$ | DC Output Diode Current | For $V_O < -0.5$V or $V_O > V_{CC} + 0.5$V | –20 | 20 | mA |
| $I_O$ | DC Output Source or Sink Current per Output Pin | For $V_O > -0.5$V or $V_O < V_{CC} + 0.5$V | –25 | 25 | mA |
| $I_{CC}$ | DC $V_{CC}$ or ground current | | –50 | 50 | mA |
| $T_{JMAX}$ | Maximum junction temperature | | | 150 | °C |
| $T_{LMAX}$ | Maximum lead temperature | Soldering 10 s | | 300 | °C |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.


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## 5 Thermal Information

| THERMAL METRIC (1) | | PW (TSSOP) 16 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 127.9 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 6 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range ($T_A$ = full package temperature range)(2) | CD54 and 74HC types | 2 | | 6 | V |
| | | CD54 and 74HCT types | 4.5 | | 5.5 | |
| $V_{CC} – V_{EE}$ (1) | Supply voltage range ($T_A$ = full package temperature range)(2) | CD54 and 74HC types, CD54 and 74HCT types | 2 | | 10 | V |
| $V_{EE}$ | Supply voltage range ($T_A$ = full package temperature range)(3) | CD54 and 74HC types, CD54 and 74HCT types | 0 | | –6 | V |
| $V_I$ | DC input control voltage | | GND | | $V_{CC}$ | V |
| $V_{IS}$ | Analog switch I/O voltage | | $V_{EE}$ | | $V_{CC}$ | V |
| $T_A$ | Ambient temperature | | –55 | | 125 | °C |
| $t_r$ , $t_f$ | Input rise and fall times | 2 V | 0 | | 1000 | ns |
| | | 4.5 V | 0 | | 500 | |
| | | 6 V | 0 | | 400 | |

(1) $V_{DD}$ and $V_{SS}$ can be any value as long as 3 V ≤ ($V_{DD}$ – $V_{SS}$) ≤ 24 V, and the minimum $V_{DD}$ is met.

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## 7 Electrical Characteristics: HC Devices

Over operating free-air temperature range, $V_{SUPPLY}$ = ±5 V, and $R_L$ = 100 Ω, (unless otherwise noted)(1)

| PARAMETER | TEST CONDITIONS | | | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| **SIGNAL INPUTS ($V_{IS}$) AND OUTPUTS ($V_{OS}$)** | | | | | | | | | |
| | **$V_{IS}$ (V)** | **$V_I$ (V)** | **$V_{EE}$ (V)** | **$V_{CC}$ (V)** | **$T_A$** | | | | |
| Input High Voltage, $V_{IH}$, Min | | | | 2 | 25°C | | | 1.5 | V |
| | | | | | –40°C to +85°C | | | 1.5 | |
| | | | | | –55°C to +125°C | | | 1.5 | |
| | | | | 4.5 | 25°C | | | 3.15 | |
| | | | | | –40°C to +85°C | | | 3.15 | |
| | | | | | –55°C to +125°C | | | 3.15 | |
| | | | | 6 | 25°C | | | 4.2 | |
| | | | | | –40°C to +85°C | | | 4.2 | |
| | | | | | –55°C to +125°C | | | 4.2 | |
| Input Low Voltage, $V_{IL}$, Max | | | | 2 | 25°C | | 0.5 | | V |
| | | | | | –40°C to +85°C | | 0.5 | | |
| | | | | | –55°C to +125°C | | 0.5 | | |
| | | | | 4.5 | 25°C | | 1.35 | | |
| | | | | | –40°C to +85°C | | 1.35 | | |
| | | | | | –55°C to +125°C | | 1.35 | | |
| | | | | 6 | 25°C | | 1.8 | | |
| | | | | | –40°C to +85°C | | 1.8 | | |
| | | | | | –55°C to +125°C | | 1.8 | | |


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Over operating free-air temperature range, $V_{SUPPLY}$ = ±5 V, and $R_L$ = 100 Ω, (unless otherwise noted)(1)

| PARAMETER | TEST CONDITIONS | | | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| $r_{ON}$ ON resistance $I_O$ = 1mA | $V_{CC}$ or $V_{EE}$ | $V_{IH}$ or $V_{IL}$ | 0 | 4.5 | 25°C | | 30 | 180 | Ω |
| | | | | | –40°C to +85°C | | | 225 | |
| | | | | | –55°C to +125°C | | | 270 | |
| | | | 0 | 6 | 25°C | | 35 | 160 | |
| | | | | | –40°C to +85°C | | | 200 | |
| | | | | | –55°C to +125°C | | | 240 | |
| | | | -4.5 | 4.5 | 25°C | | 30 | 135 | |
| | | | | | –40°C to +85°C | | | 170 | |
| | | | | | –55°C to +125°C | | | 205 | |
| | $V_{CC}$ to $V_{EE}$ | | 0 | 4.5 | 25°C | | 40 | 320 | Ω |
| | | | | | –40°C to +85°C | | | 400 | |
| | | | | | –55°C to +125°C | | | 480 | |
| | | | 0 | 6 | 25°C | | 30 | 240 | |
| | | | | | –40°C to +85°C | | | 300 | |
| | | | | | –55°C to +125°C | | | 360 | |
| | | | -4.5 | 4.5 | 25°C | | 35 | 170 | |
| | | | | | –40°C to +85°C | | | 215 | |
| | | | | | –55°C to +125°C | | | 255 | |
| $\Delta r_{ON}$ Maximum ON resistance between any two channels | | | 0 | 4.5 | 25°C | | 10 | | Ω |
| | | | 0 | 6 | 25°C | | 8.5 | | |
| | | | -4.5 | 4.5 | 25°C | | 5 | | |
| $I_{IZ}$ Switch OFF leakage current | $V_{CC}$ - $V_{EE}$ | $V_{IH}$ or $V_{IL}$ $\overline{E}$ = $V_{CC}$ | 0 | 6 | 25°C | | | ±0.1 | µA |
| | | | 0 | 6 | –55°C to 85°C | | | ±1 | |
| | | | 0 | 6 | –55°C to 125°C | | | ±1 | |
| | | | -5 | 5 | 25°C | | | ±0.1 | |
| | | | -5 | 5 | –55°C to 85°C | | | ±1 | |
| | | | -5 | 5 | –55°C to 125°C | | | ±1 | |
| $I_{IL}$ Control input leakage current | | $V_{CC}$ or GND | 0 | 6 | 25°C | | | ±0.1 | µA |
| | | | | | –55°C to 85°C | | | ±1 | |
| | | | | | –55°C to 125°C | | | ±1 | |

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Over operating free-air temperature range, $V_{SUPPLY}$ = ±5 V, and $R_L$ = 100 Ω, (unless otherwise noted)(1)

| PARAMETER | TEST CONDITIONS | | | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| Quiescent Device Current, $I_{DD}$ Max $I_O$ = 1mA | When $V_{IS}$ = $V_{EE}$, $V_{OS}$ = $V_{CC}$ | $V_{CC}$ or GND | 0 | 6 | 25°C | | | 14 | µA |
| | | | | | –55°C to 85°C | | | 80 | |
| | | | | | –55°C to 125°C | | | 160 | |
| | When $V_{IS}$ = $V_{CC}$, $V_{OS}$ = $V_{EE}$ | | -5 | 5 | 25°C | | | 30 | |
| | | | | | –55°C to 85°C | | | 160 | |
| | | | | | –55°C to 125°C | | | 320 | |
| **CONTROL (ADDRESS OR INHIBIT), $V_C$** | | | | | | | | | |

(1) For dual-supply systems theoretical worst case (VI = 2.4V, VCC = 5.5V) specification is 1.8mA


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## 8 Electrical Characteristics: HCT Devices

Over operating free-air temperature range, $V_{SUPPLY}$ = ±5 V, and $R_L$ = 100 Ω, (unless otherwise noted)(1)

| PARAMETER | | TEST CONDITIONS | | | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| **SIGNAL INPUTS ($V_{IS}$) AND OUTPUTS ($V_{OS}$)** | | | | | | | | | | |
| | | **$V_{IS}$ (V)** | **$V_I$ (V)** | **$V_{CC}$ (V)** | **$V_{EE}$ (V)** | **$T_A$** | | | | |
| High Level Input Voltage | $V_{IH}$ | | | 4.5 to 5.5 | | 25°C | 2 | | | V |
| | | | | | | –40°C to +85°C | 2 | | | |
| | | | | | | –55°C to +125°C | 2 | | | |
| Low Level Input Voltage | $V_{IL}$ | | | | | 25°C | | | 0.8 | V |
| | | | | | | –40°C to +85°C | | | 0.8 | |
| | | | | | | –55°C to +125°C | | | 0.8 | |
| "ON" Resistance IO = 1mA | $R_{ON}$ | $V_{CC}$ or $V_{EE}$ | $V_{IH}$ or $V_{IL}$ | 4.5 | 0 | 25°C | | 30 | 180 | Ω |
| | | | | | | –40°C to +85°C | | 45 | 225 | |
| | | | | | | –55°C to +125°C | | | 270 | |
| | | $V_{CC}$ to $V_{EE}$ | | 4.5 | -4.5 | 25°C | | | 135 | |
| | | | | | | –40°C to +85°C | | 30 | 170 | |
| | | | | | | –55°C to +125°C | | | 205 | |
| | | $V_{CC}$ or $V_{EE}$ | | 4.5 | 0 | 25°C | | | 320 | |
| | | | | | | –40°C to +85°C | | 85 | 400 | |
| | | | | | | –55°C to +125°C | | | 480 | |
| | | $V_{CC}$ to $V_{EE}$ | | 4.5 | -4.5 | 25°C | | 35 | 170 | |
| | | | | | | –40°C to +85°C | | | 215 | |
| | | | | | | –55°C to +125°C | | | 255 | |
| "ON" Resistance Between Any Two Switches | $\blacktriangle R_{ON}$ | | VCC | 4.5 | 0 | 25°C | | 10 | | Ω |
| | | | | 4.5 | -4.5 | 25°C | | 5 | | Ω |
| Off-Switch Leakage Current | $I_{IZ}$ | $V_{CC}$ - $V_{EE}$ | $V_{IH}$ or $V_{IL}$ | 6 | 0 | 25°C | | | ±0.1 | µA |
| | | | | | | –55°C to 85°C | | | ±1 | µA |
| | | | | | | –55°C to 125°C | | | ±1 | µA |
| | | | | 5 | -5 | 25°C | | | ±0.1 | µA |
| | | | | | | –55°C to 85°C | | | ±1 | |
| | | | | | | –55°C to 125°C | | | ±1 | |
| Input Leakage Current (Any Control) | $I_{IL}$ | | $V_{CC}$ or GND | 5.5 | 0 | 25°C | | | ±0.1 | µA |
| | | | | | | –55°C to 85°C | | | ±1 | |
| | | | | | | –55°C to 125°C | | | ±1 | |

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Over operating free-air temperature range, $V_{SUPPLY}$ = ±5 V, and $R_L$ = 100 Ω, (unless otherwise noted)(1)

| PARAMETER | | TEST CONDITIONS | | | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| Quiescent Device Current | $I_{CC}$ | When $V_{IS}$ = $V_{EE}$, $V_{OS}$ = $V_{CC}$, When $V_{IS}$ = $V_{CC}$, $V_{OS}$ = $V_{EE}$ | Any voltage between $V_{CC}$ and GND | 5.5 | 0 | 25°C | | | 8 | µA |
| | | | | | | –55°C to 85°C | | | 80 | |
| | | | | | | –55°C to 125°C | | | 160 | |
| | | | | 5.5 | -4.5 | 25°C | | | 16 | |
| | | | | | | –55°C to 85°C | | | 160 | |
| | | | | | | –55°C to 125°C | | | 320 | |
| Additional Quiescent Device Current Per Input Pin: 1 Unit Load | ▲$I_{CC}$ (1) | $V_{CC}$ - 2.1 | | 4.5 to 5.5 | | 25°C | | 100 | 360 | µA |
| | | | | | | –55°C to 85°C | | | 450 | |
| | | | | | | –55°C to 125°C | | | 490 | |
| **CONTROL (ADDRESS OR INHIBIT), $V_C$** | | | | | | | | | | |

(1) For dual-supply systems theoretical worst case (VI = 2.4V, VCC = 5.5V) specification is 1.8mA

## 9 Switching Characteristics HC

over operating free-air temperature range (unless otherwise noted)

| Parameter | | VEE (V) | VCC (V) | Test Conditions | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| Propagation Delay, Switch In to Out | $t_{PLH}$, $t_{PHL}$ | 0 | 2 | 50pF | 25°C | | | 60 | ns |
| | | 0 | 2 | | –40°C to +85°C | | | 75 | |
| | | 0 | 2 | | –55°C to +125°C | | | 90 | |
| | | 0 | 4.5 | | 25°C | | | 12 | |
| | | 0 | 4.5 | | –40°C to +85°C | | | 15 | |
| | | 0 | 4.5 | | –55°C to +125°C | | | 18 | |
| | | 0 | 6 | | 25°C | | | 10 | |
| | | 0 | 6 | | –40°C to +85°C | | | 13 | |
| | | 0 | 6 | | –55°C to +125°C | | | 15 | |
| | | -4.5 | 4.5 | | 25°C | | | 8 | |
| | | -4.5 | 4.5 | | –40°C to +85°C | | | 10 | |
| | | -4.5 | 4.5 | | –55°C to +125°C | | | 12 | |


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over operating free-air temperature range (unless otherwise noted)

| Parameter | | VEE (V) | VCC (V) | Test Conditions | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| Turn "ON" Time !E to Out | tPZH, tPZL | 0 | 2 | 50pF | 25°C | | | 205 | ns |
| | | 0 | 2 | | –40°C to +85°C | | | 255 | |
| | | 0 | 2 | | –55°C to +125°C | | | 310 | |
| | | 0 | 4.5 | | 25°C | | | 41 | |
| | | 0 | 4.5 | | –40°C to +85°C | | | 51 | |
| | | 0 | 4.5 | | –55°C to +125°C | | | 62 | |
| | | 0 | 6 | | 25°C | | | 35 | |
| | | 0 | 6 | | –40°C to +85°C | | | 43 | |
| | | 0 | 6 | | –55°C to +125°C | | | 53 | |
| | | -4.5 | 4.5 | | 25°C | | | 37 | |
| | | -4.5 | 4.5 | | –40°C to +85°C | | | 47 | |
| | | -4.5 | 4.5 | | –55°C to +125°C | | | 56 | |
| | | - | 5 | 15pF | 25°C | | 8 | | |
| Turn "ON" Time nS to Out | $t_{PZH}$, $t_{PZL}$ | 0 | 2 | 50pF | 25°C | | | 175 | ns |
| | | 0 | 2 | | –40°C to +85°C | | | 220 | |
| | | 0 | 2 | | –55°C to +125°C | | | 265 | |
| | | 0 | 4.5 | | 25°C | | | 35 | |
| | | 0 | 4.5 | | –40°C to +85°C | | | 44 | |
| | | 0 | 4.5 | | –55°C to +125°C | | | 53 | |
| | | 0 | 6 | | 25°C | | | 30 | |
| | | 0 | 6 | | –40°C to +85°C | | | 37 | |
| | | 0 | 6 | | –55°C to +125°C | | | 45 | |
| | | -4.5 | 4.5 | | 25°C | | | 34 | |
| | | -4.5 | 4.5 | | –40°C to +85°C | | | 43 | |
| | | -4.5 | 4.5 | | –55°C to +125°C | | | 51 | |
| | | - | 5 | 15pF | 25°C | | 14 | | |

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over operating free-air temperature range (unless otherwise noted)

| Parameter | | VEE (V) | VCC (V) | Test Conditions | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| Turn "OFF" Time !E to Out | $t_{PLZ}$, $t_{PHZ}$ | 0 | 2 | 50pF | 25°C | | | 205 | ns |
| | | 0 | 2 | | –40°C to +85°C | | | 255 | ns |
| | | 0 | 2 | | –55°C to +125°C | | | 310 | ns |
| | | 0 | 4.5 | | 25°C | | | 41 | ns |
| | | 0 | 4.5 | | –40°C to +85°C | | | 51 | ns |
| | | 0 | 4.5 | | –55°C to +125°C | | | 62 | ns |
| | | 0 | 6 | | 25°C | | | 35 | ns |
| | | 0 | 6 | | –40°C to +85°C | | | 43 | ns |
| | | 0 | 6 | | –55°C to +125°C | | | 53 | ns |
| | | -4.5 | 4.5 | | 25°C | | | 37 | ns |
| | | -4.5 | 4.5 | | –40°C to +85°C | | | 47 | ns |
| | | -4.5 | 4.5 | | –55°C to +125°C | | | 56 | ns |
| | | - | 5 | 15pF | 25°C | | 8 | | ns |
| Turn "OFF" Time nS to Out | $t_{PLZ}$, $t_{PHZ}$ | 0 | 2 | 50pF | 25°C | | | 175 | ns |
| | | 0 | 2 | | –40°C to +85°C | | | 220 | |
| | | 0 | 2 | | –55°C to +125°C | | | 265 | |
| | | 0 | 4.5 | | 25°C | | | 35 | |
| | | 0 | 4.5 | | –40°C to +85°C | | | 44 | |
| | | 0 | 4.5 | | –55°C to +125°C | | | 53 | |
| | | 0 | 6 | | 25°C | | | 30 | |
| | | 0 | 6 | | –40°C to +85°C | | | 37 | |
| | | 0 | 6 | | –55°C to +125°C | | | 45 | |
| | | -4.5 | 4.5 | | 25°C | | | 34 | |
| | | -4.5 | 4.5 | | –40°C to +85°C | | | 43 | |
| | | -4.5 | 4.5 | | –55°C to +125°C | | | 51 | |
| | | - | 5 | 15pF | 25°C | | 14 | | |


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over operating free-air temperature range (unless otherwise noted)

| Parameter | | VEE (V) | VCC (V) | Test Conditions | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| Input (Control) Capacitance | $C_I$ | - | - | - | 25°C | | | 10 | pF |
| Input (Control) Capacitance | | - | - | | –40°C to +85°C | | | 10 | |
| Input (Control) Capacitance | | - | - | | –55°C to +125°C | | | 10 | |
| Power dissipation capacitance(1) | $C_{PD}$ | - | 5 | | 25°C | | 42 | | |

## 10 Switching Characteristics HCT

over operating free-air temperature range (unless otherwise noted)

| Parameter | | VEE (V) | VCC (V) | Test Conditions | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| Propagation Delay, Switch In to Out | $t_{PLH}$, $t_{PHL}$ | 0 | 4.5 | 50pF | 25°C | | | 12 | ns |
| | | | | | –40°C to +85°C | | | 15 | |
| | | | | | –55°C to +125°C | | | 18 | |
| | | -4.5 | 4.5 | | 25°C | | | 8 | |
| | | | | | –40°C to +85°C | | | 10 | |
| | | | | | –55°C to +125°C | | | 12 | |
| Turn "ON" Time !E to Out | tPZH, tPZL | 0 | 4.5 | 50pF | 25°C | | | 44 | ns |
| | | | | | –40°C to +85°C | | | 55 | |
| | | | | | –55°C to +125°C | | | 66 | |
| | | -4.5 | 4.5 | | 25°C | | | 42 | |
| | | | | | –40°C to +85°C | | | 53 | |
| | | | | | –55°C to +125°C | | | 63 | |
| | | - | 5 | 15pF | 25°C | | 18 | | |
| | | 0 | 4.5 | 50pF | 25°C | | | 56 | |
| | | | | | –40°C to +85°C | | | 70 | |
| | | | | | –55°C to +125°C | | | 85 | |
| | | -4.5 | 4.5 | | 25°C | | | 42 | |
| | | | | | –40°C to +85°C | | | 53 | |
| | | | | | –55°C to +125°C | | | 63 | |
| | | - | 5 | 15pF | 25°C | | 24 | | |

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over operating free-air temperature range (unless otherwise noted)

| Parameter | | VEE (V) | VCC (V) | Test Conditions | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| Turn "ON" Time nS to Out | $t_{PZH}$, $t_{PZL}$ | 0 | 4.5 | 50pF | 25°C | | | 40 | ns |
| | | | | | –40°C to +85°C | | | 53 | |
| | | | | | –55°C to +125°C | | | 60 | |
| | | -4.5 | 4.5 | | 25°C | | | 34 | |
| | | | | | –40°C to +85°C | | | 43 | |
| | | | | | –55°C to +125°C | | | 51 | |
| | | 0 | 5 | 15pF | 25°C | | 17 | | |
| | | 0 | 4.5 | 50pF | 25°C | | | 50 | |
| | | | | | –40°C to +85°C | | | 63 | |
| | | | | | –55°C to +125°C | | | 75 | |
| | | -4.5 | 4.5 | | 25°C | | | 34 | |
| | | | | | –40°C to +85°C | | | 43 | |
| | | | | | –55°C to +125°C | | | 51 | |
| | | - | 5 | 15pF | 25°C | | 18 | | |
| Turn "OFF" Time !E to Out | $t_{PLZ}$, $t_{PHZ}$ | 0 | 4.5 | 50pF | 25°C | | | 50 | ns |
| | | | | | –40°C to +85°C | | | 63 | |
| | | | | | –55°C to +125°C | | | 75 | |
| | | -4.5 | 4.5 | | 25°C | | | 46 | |
| | | | | | –40°C to +85°C | | | 58 | |
| | | | | | –55°C to +125°C | | | 69 | |
| | | - | 5 | 15pF | 25°C | | 21 | | |
| Turn "OFF" Time nS to Out | $t_{PLZ}$, $t_{PHZ}$ | 0 | 4.5 | 50pF | 25°C | | | 44 | ns |
| | | | | | –40°C to +85°C | | | 55 | |
| | | | | | –55°C to +125°C | | | 66 | |
| | | -4.5 | 4.5 | | 25°C | | | 40 | |
| | | | | | –40°C to +85°C | | | 50 | |
| | | | | | –55°C to +125°C | | | 60 | |
| | | - | 5 | 15pF | 25°C | | 18 | | |


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over operating free-air temperature range (unless otherwise noted)

| Parameter | | VEE (V) | VCC (V) | Test Conditions | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| Input (Control) Capacitance | $C_I$ | - | - | - | 25°C | | | 10 | pF |
| | | - | - | - | –40°C to +85°C | | | 10 | |
| | | - | - | - | –55°C to +125°C | | | 10 | |
| Power dissipation capacitance(1) | $C_{PD}$ | - | 5 | - | 25°C | | 47 | | |

## 11 Analog Channel Specifications

over operating free-air temperature range (unless otherwise noted)

| Parameter | Test Conditions | | HC, HCT TYPES | $V_{CC}$ (V) | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $f_{MAX}$ Minimum switch frequency response at –3 dB | | | HC | 4.5 | | 200 | | MHz |
| | | | HCT | 4.5 | | 200 | | |
| THD Sine-wave distortion | 1kHz, $V_{IS}$ = $4V_{P-P}$ | | HC | 4.5 | | 0.078 | | % |
| | 1kHz, $V_{IS}$ = $8V_{P-P}$ | | | 9 | | 0.018 | | |
| | 1kHz, $V_{IS}$ = $4V_{P-P}$ | | HCT | 4.5 | | 0.078 | | |
| | 1kHz, $V_{IS}$ = $8V_{P-P}$ | | | 9 | | 0.018 | | |
| Switch "OFF" Signal Feedthrough | | | HC | 4.5 | | -62 | | dB |
| | | | HCT | 4.5 | | -62 | | |
| Switch Input Capacitance, $C_S$ | | | HC | - | | 5 | | pF |
| | | | HCT | - | | 5 | | |

## 12 HCT Input Loading Table

| INPUT | UNIT LOADS(1) |
|---|---|
| All | 0.5 |

(1) Unit Load is $\Delta I_{CC}$ limit specified in DC Electrical Table, e.g., 360µA max at 25°C

## 13 Recommended Operating Area as a Function of Supply Voltage

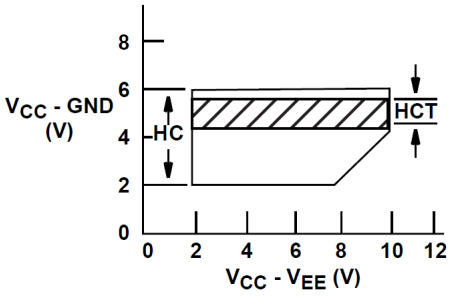



Figure 13-1.

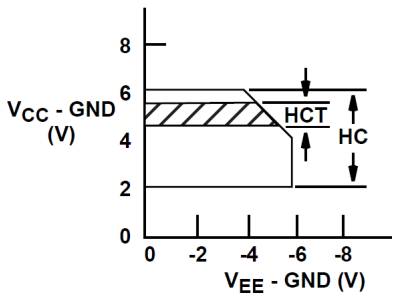



Figure 13-2.

## 14 Typical Performance Curves

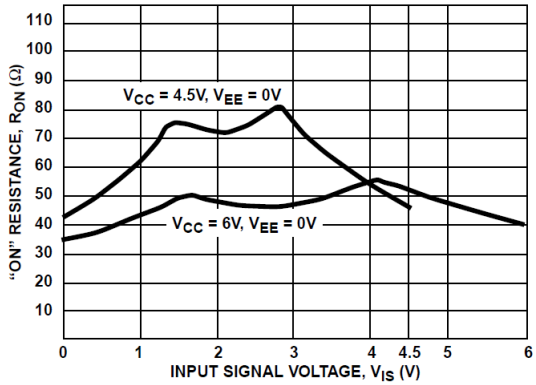



**Figure 14-1. Typical On Resistance vs Input Signal Voltage**

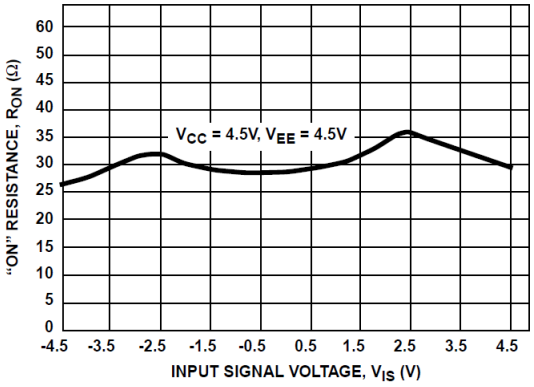



**Figure 14-2. Typical On Resistance vs Input Signal Voltage**

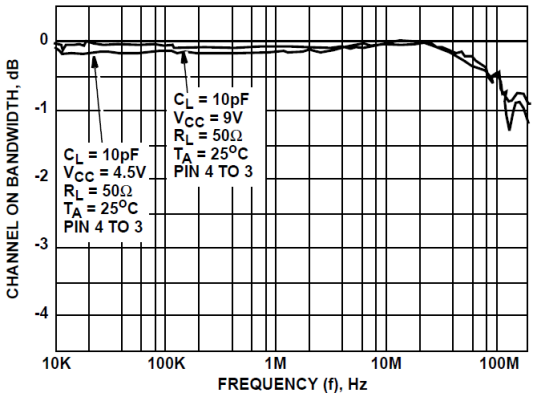



**Figure 14-3. Switch Frequency Response**

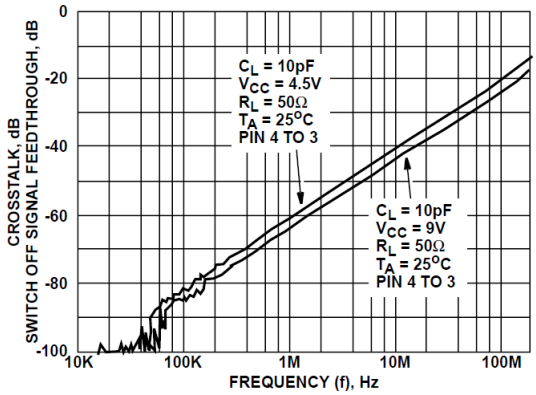



**Figure 14-4. Switch-Off Signal Feedthrough and Crosstalk vs Frequency**


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## 15 Parameter Measurement Information

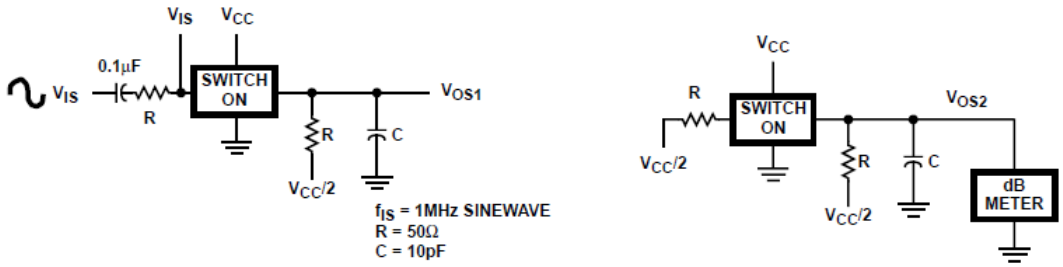



**Figure 15-1. Crosstalk Between Two Switches Test Circuit**

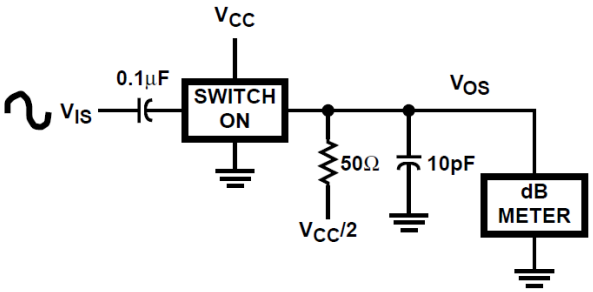



**Figure 15-2. Frequency Response Test Circuit**

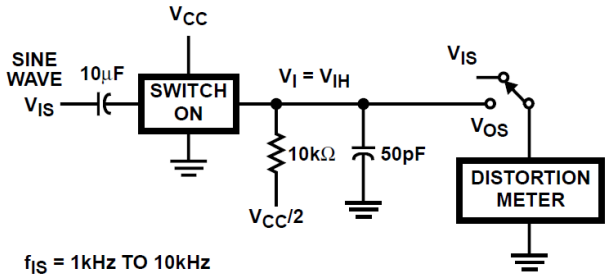



**Figure 15-3. Total Harmonic Distortion Test Circuit**

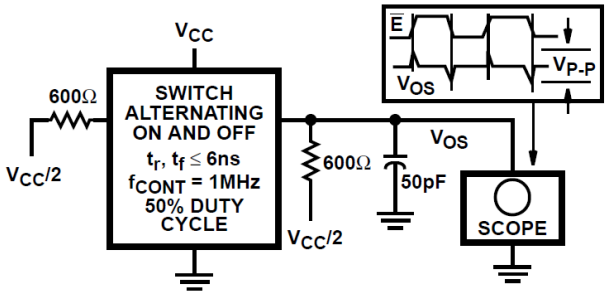



**Figure 15-4. Control-To-Switch Feedthrough Noise Test Circuit**

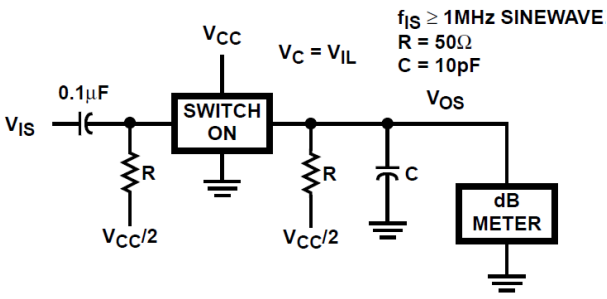



**Figure 15-5. Switch Off Signal Feedthrough**

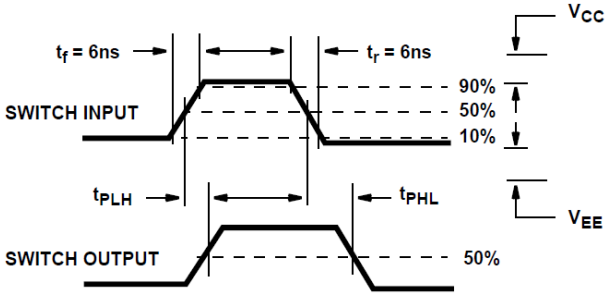



**Figure 15-6. Switch Propagation Delay Times**

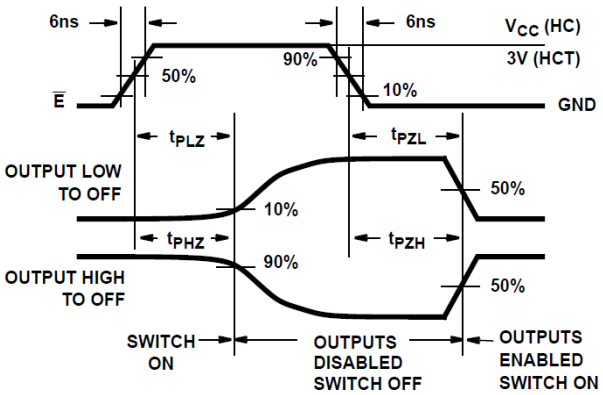
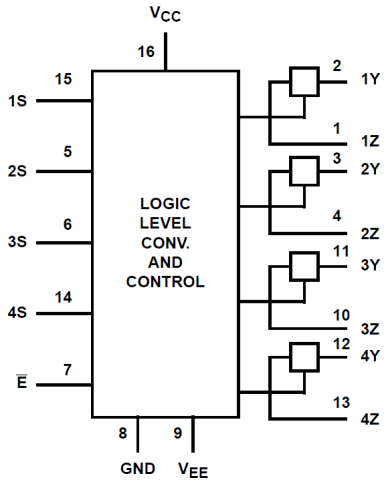



**Figure 15-7. Switch Turn-On and Turn-Off Propagation Delay Times Waveforms**

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# 16 Detailed Description

## 16.1 Functional Block Diagram




## 16.2 Device Functional Modes

**Table 16-1. Truth Table(1)**

| INPUTS | | SWITCH |
|---|---|---|
| E | S | |
| L | L | OFF |
| L | H | ON |
| H | X | OFF |

(1) H = High Level Voltage, L = Low Level Voltage, X = Do not Care


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# 17 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

## 17.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 17.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 17.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 17.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 17.5 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 18 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision D (October 2003) to Revision E (July 2024) | Page |
|---|---|
| • Updated the numbering format for tables, figures, and cross-references throughout the document | 1 |
| • Updated thermal information | 5 |
| • Updated electrical specifications | 6 |
| • Updated switching specifications | 10 |
| • Updated analog channel specifications | 15 |
| • Updated orderable information | 19 |

# 19 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| CD54HC4316F3A | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | CD54HC4316F3A |
| CD54HC4316F3A.A | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | CD54HC4316F3A |
| CD74HC4316E | NRND | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD74HC4316E |
| CD74HC4316E.A | NRND | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD74HC4316E |
| CD74HC4316M | Obsolete | Production | SOIC (D) \| 16 | - | - | Call TI | Call TI | -55 to 125 | HC4316M |
| CD74HC4316M96 | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC4316M |
| CD74HC4316M96.A | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC4316M |
| CD74HC4316NSR | NRND | Production | SOP (NS) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC4316M |
| CD74HC4316NSR.A | NRND | Production | SOP (NS) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC4316M |
| CD74HC4316PW | Obsolete | Production | TSSOP (PW) \| 16 | - | - | Call TI | Call TI | -55 to 125 | HJ4316 |
| CD74HC4316PWR | Active | Production | TSSOP (PW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HJ4316 |
| CD74HC4316PWR.A | Active | Production | TSSOP (PW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HJ4316 |
| CD74HCT4316E | NRND | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD74HCT4316E |
| CD74HCT4316E.A | NRND | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD74HCT4316E |
| CD74HCT4316M | NRND | Production | SOIC (D) \| 16 | 40 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HCT4316M |
| CD74HCT4316M.A | NRND | Production | SOIC (D) \| 16 | 40 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HCT4316M |
| CD74HCT4316M96 | NRND | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HCT4316M |
| CD74HCT4316M96.A | NRND | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HCT4316M |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**(5) MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF CD54HC4316, CD74HC4316 :**

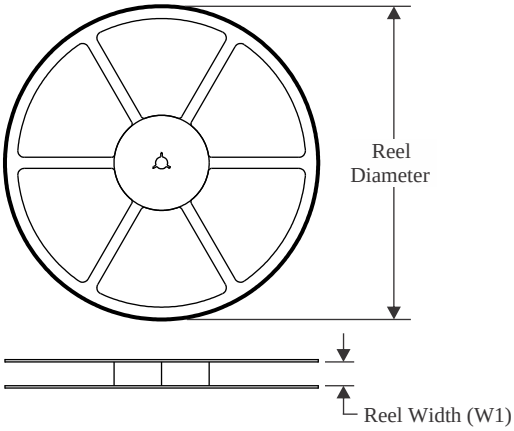
- Catalog : CD74HC4316
- Military : CD54HC4316

NOTE: Qualified Version Definitions:

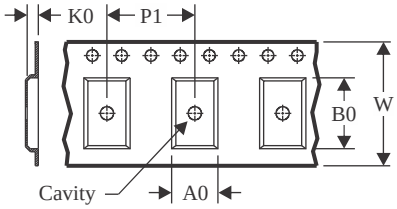
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

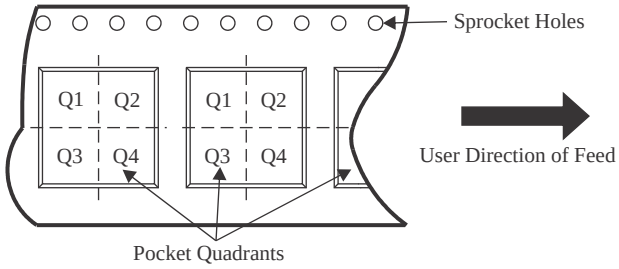



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

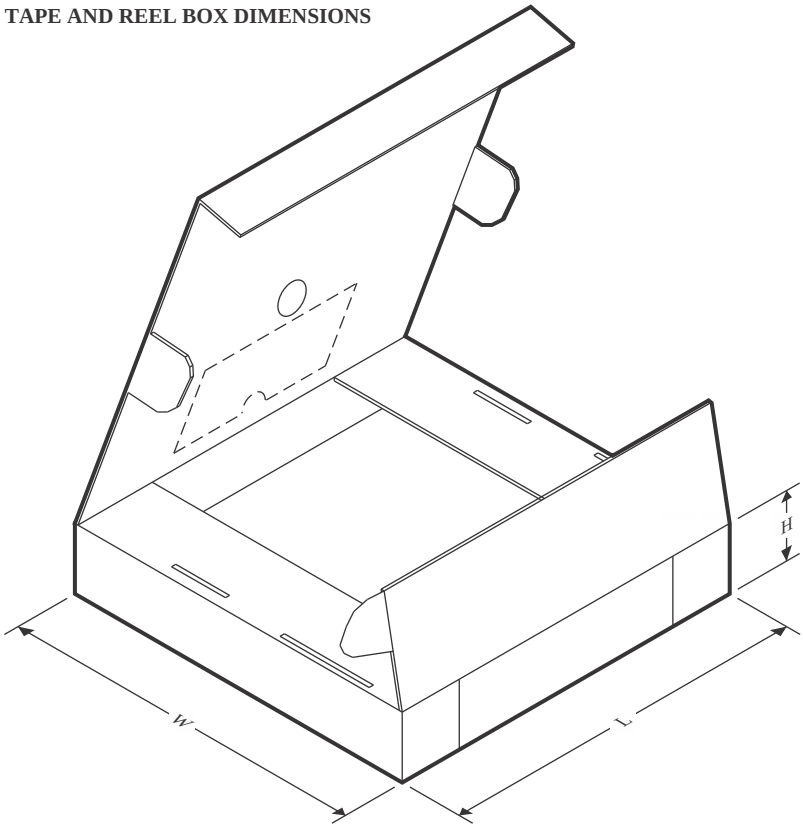
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CD74HC4316M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| CD74HC4316NSR | SOP | NS | 16 | 2000 | 330.0 | 16.4 | 8.1 | 10.4 | 2.5 | 12.0 | 16.0 | Q1 |
| CD74HC4316PWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| CD74HCT4316M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |

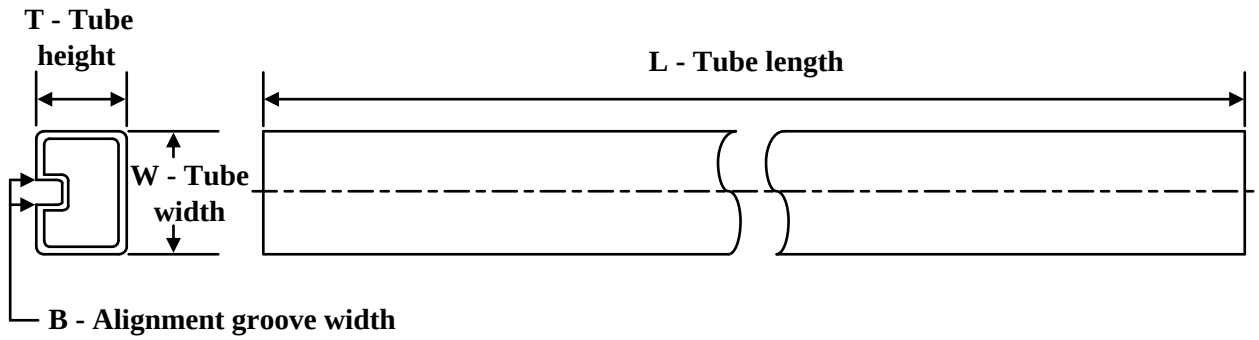
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

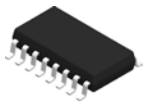
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CD74HC4316M96 | SOIC | D | 16 | 2500 | 353.0 | 353.0 | 32.0 |
| CD74HC4316NSR | SOP | NS | 16 | 2000 | 353.0 | 353.0 | 32.0 |
| CD74HC4316PWR | TSSOP | PW | 16 | 2000 | 353.0 | 353.0 | 32.0 |
| CD74HCT4316M96 | SOIC | D | 16 | 2500 | 340.5 | 336.1 | 32.0 |

## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| CD74HC4316E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HC4316E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HC4316E.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HC4316E.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HCT4316E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HCT4316E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HCT4316E.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HCT4316E.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HCT4316M | D | SOIC | 16 | 40 | 507 | 8 | 3940 | 4.32 |
| CD74HCT4316M.A | D | SOIC | 16 | 40 | 507 | 8 | 3940 | 4.32 |

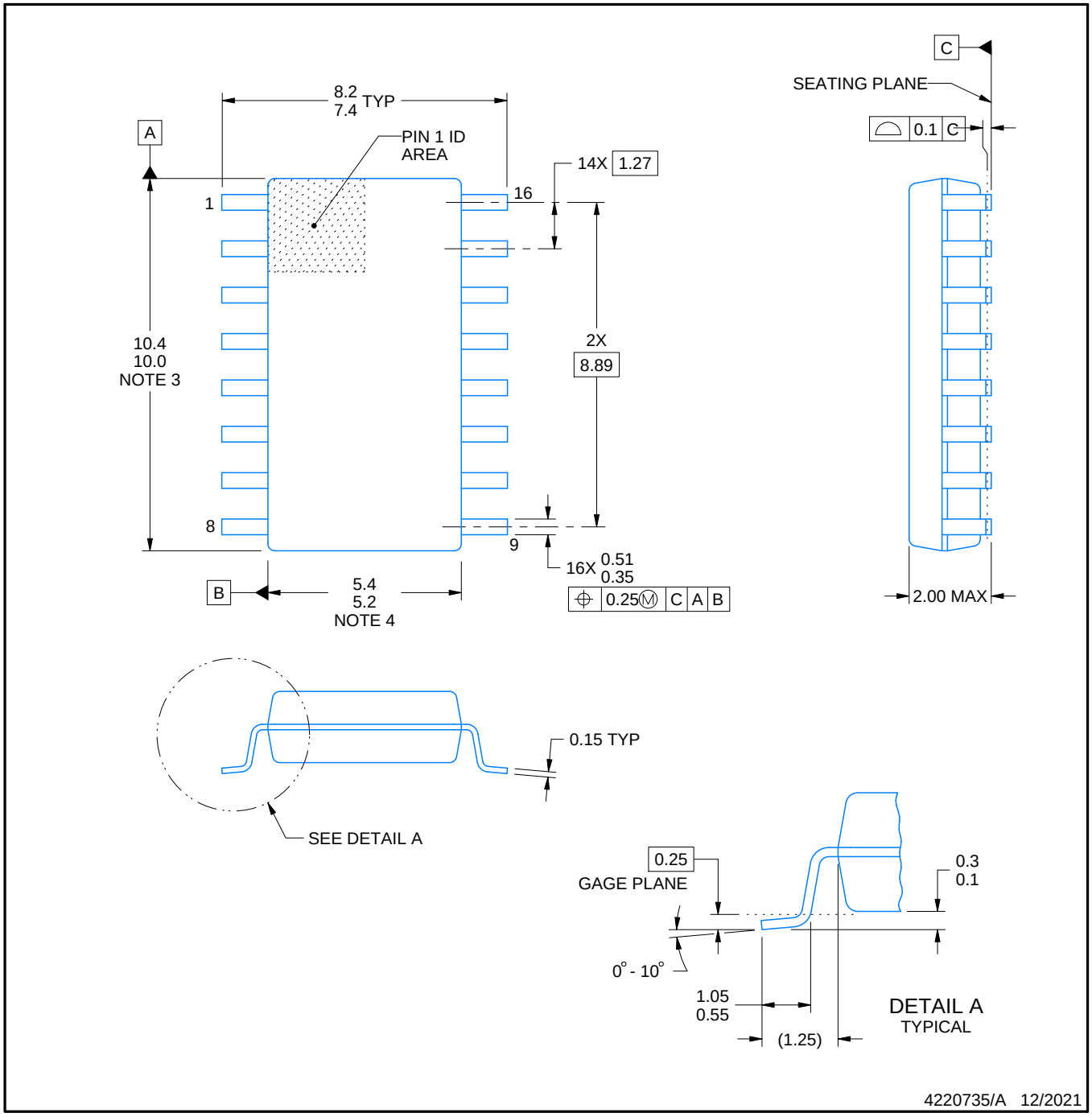


# PACKAGE OUTLINE

## NS0016A

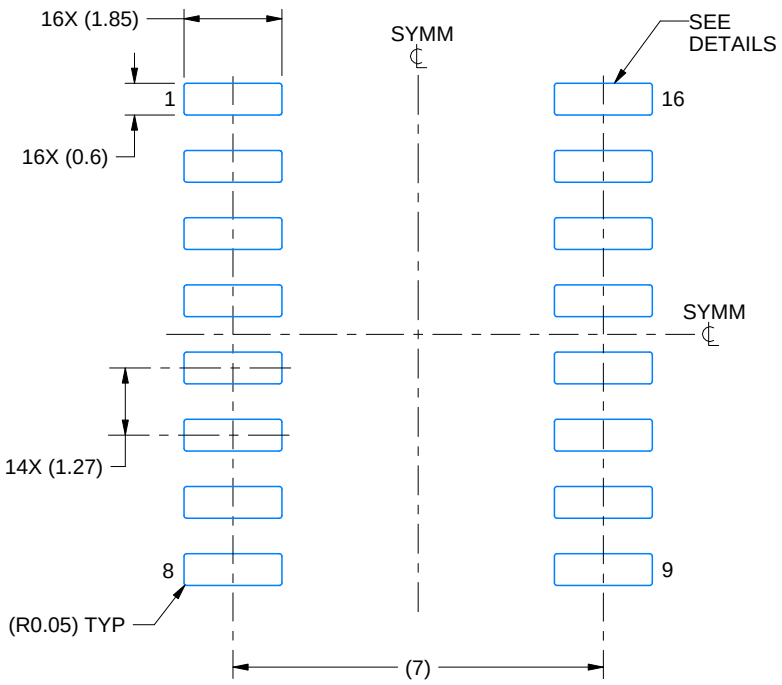
## SOP - 2.00 mm max height

SOP

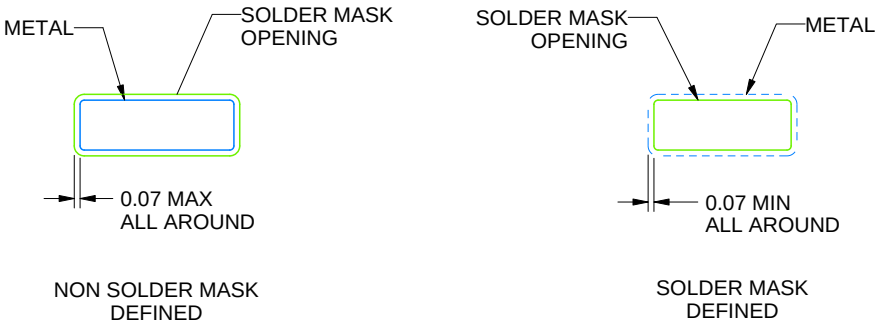



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.




LAND PATTERN EXAMPLE
SCALE:7X




NON SOLDER MASK
DEFINED

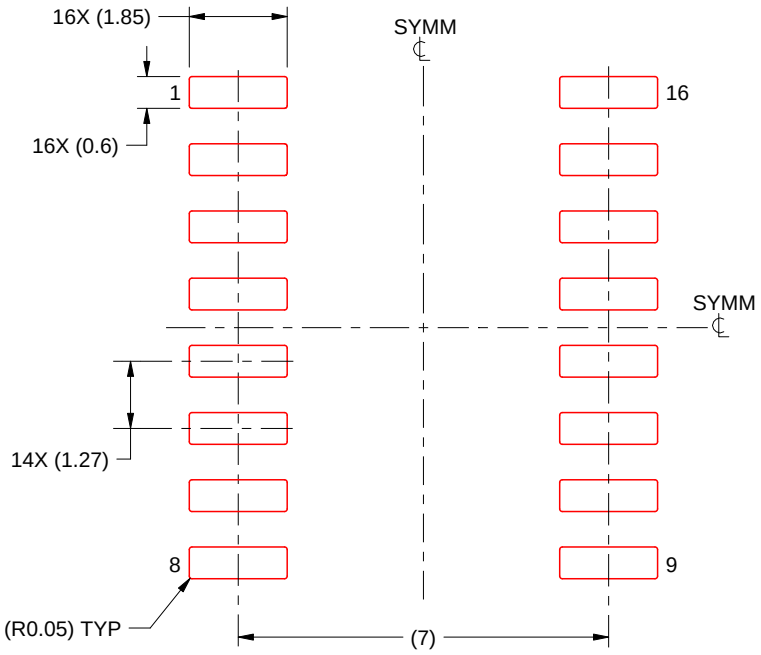
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



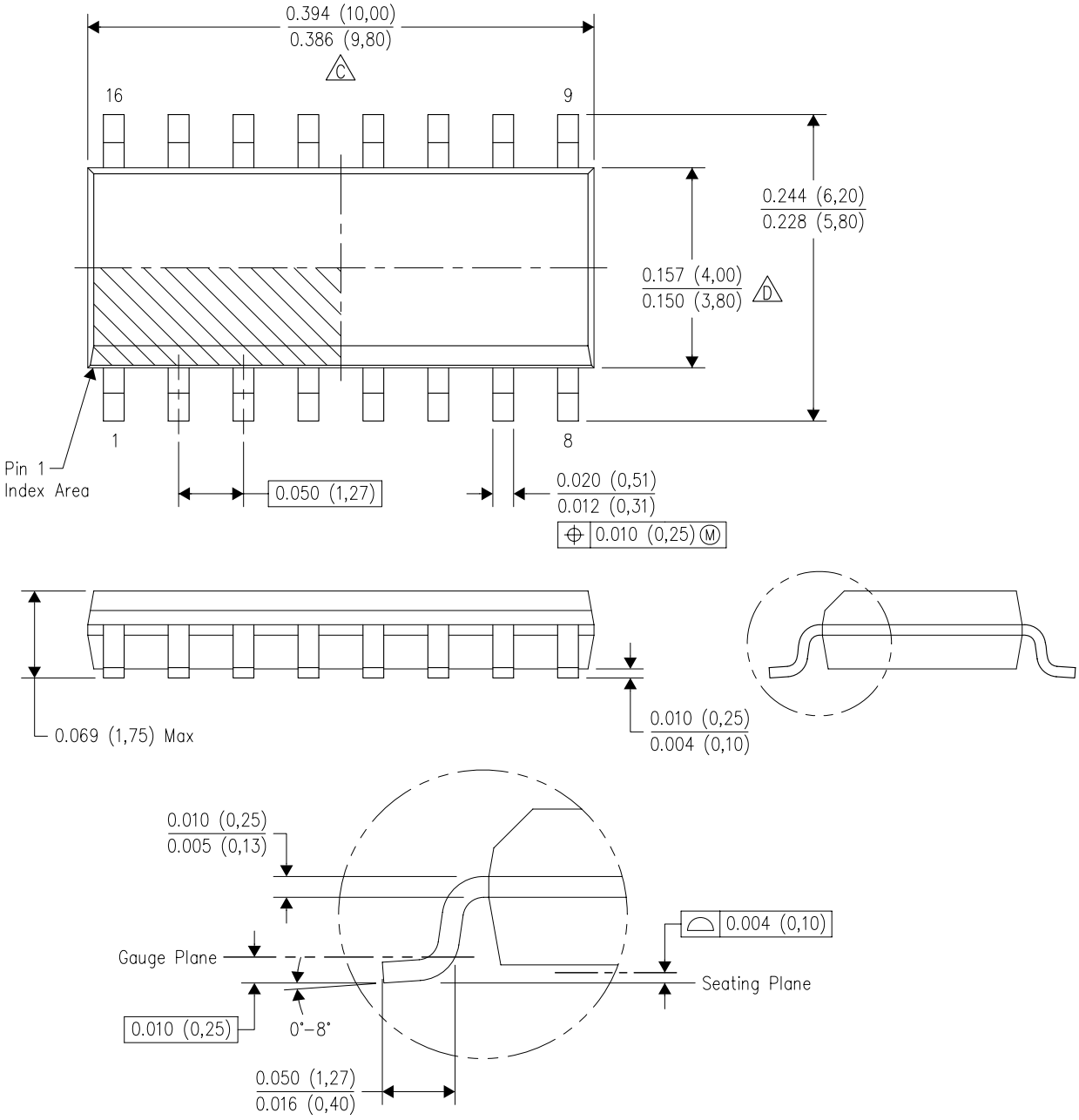

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

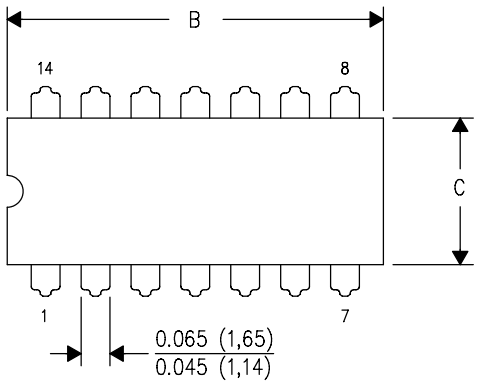



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

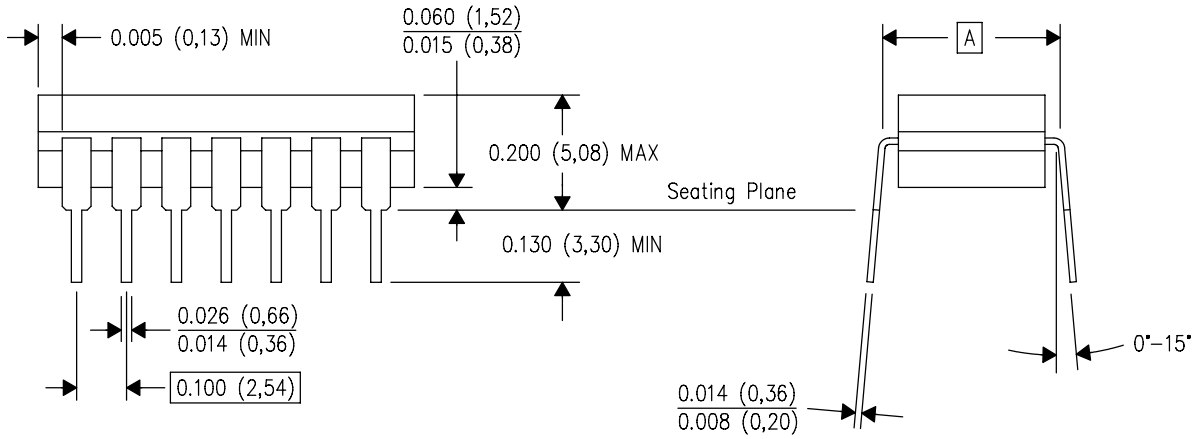
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |




4040083/F 03/03

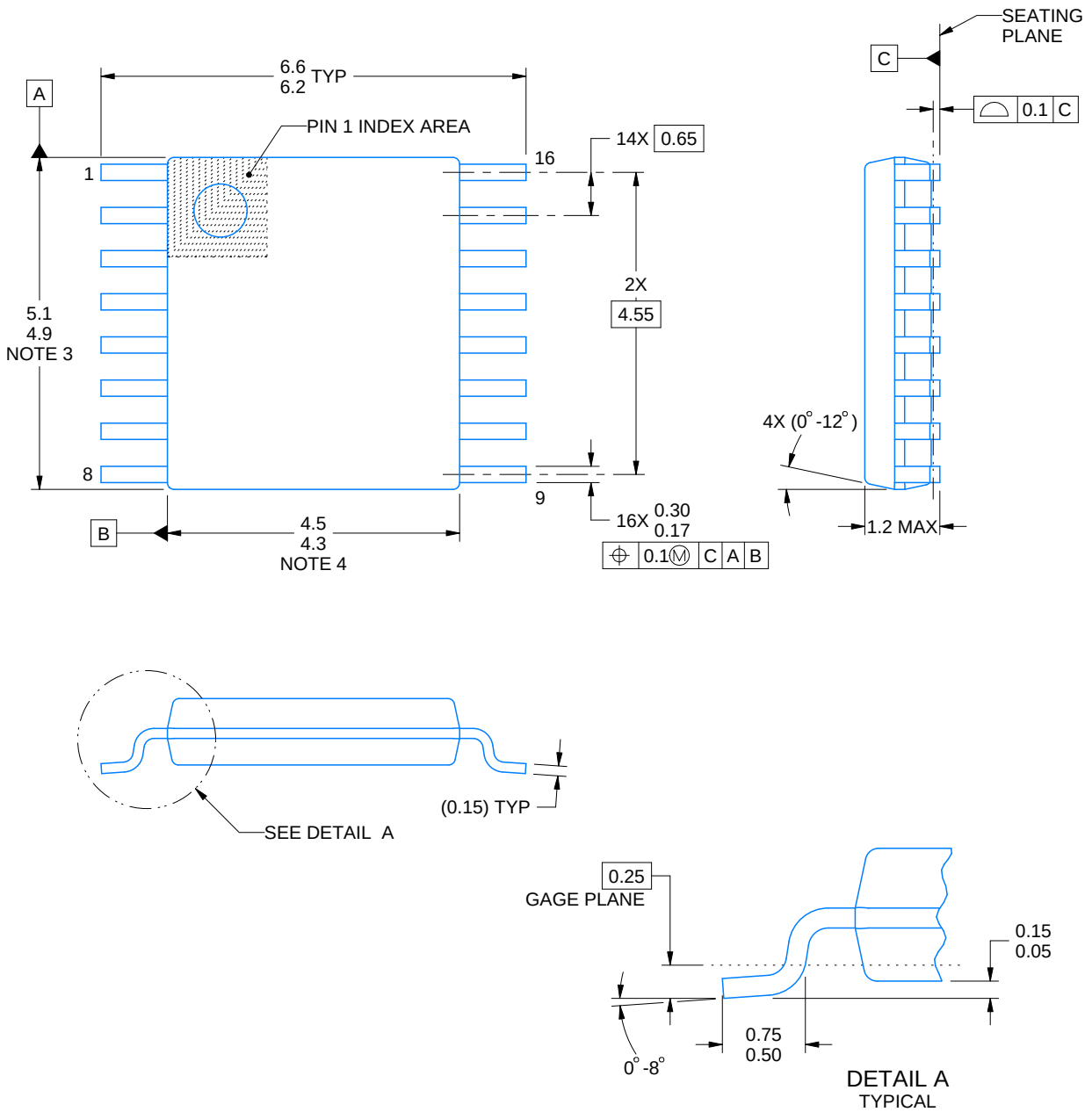
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

# PACKAGE OUTLINE

## PW0016A

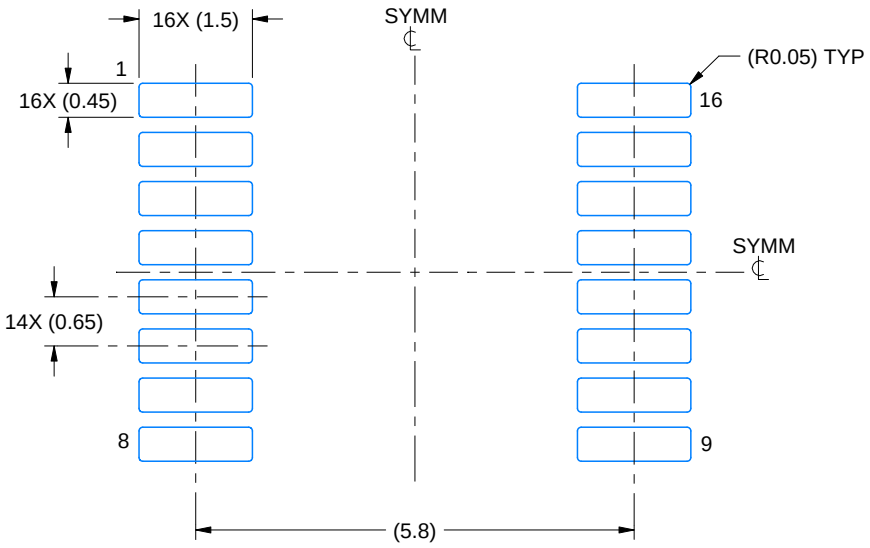
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE




NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

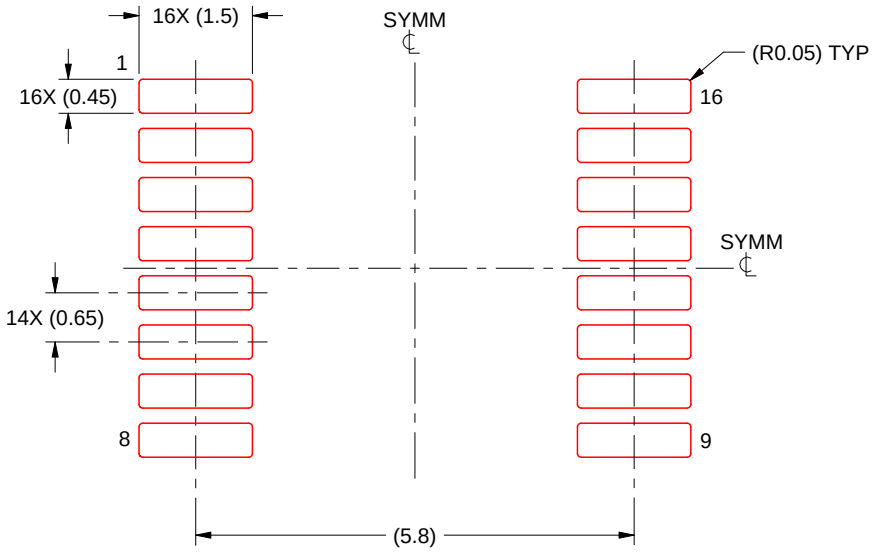



SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

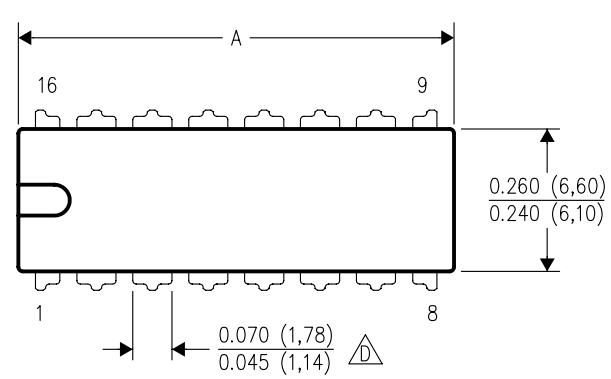
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

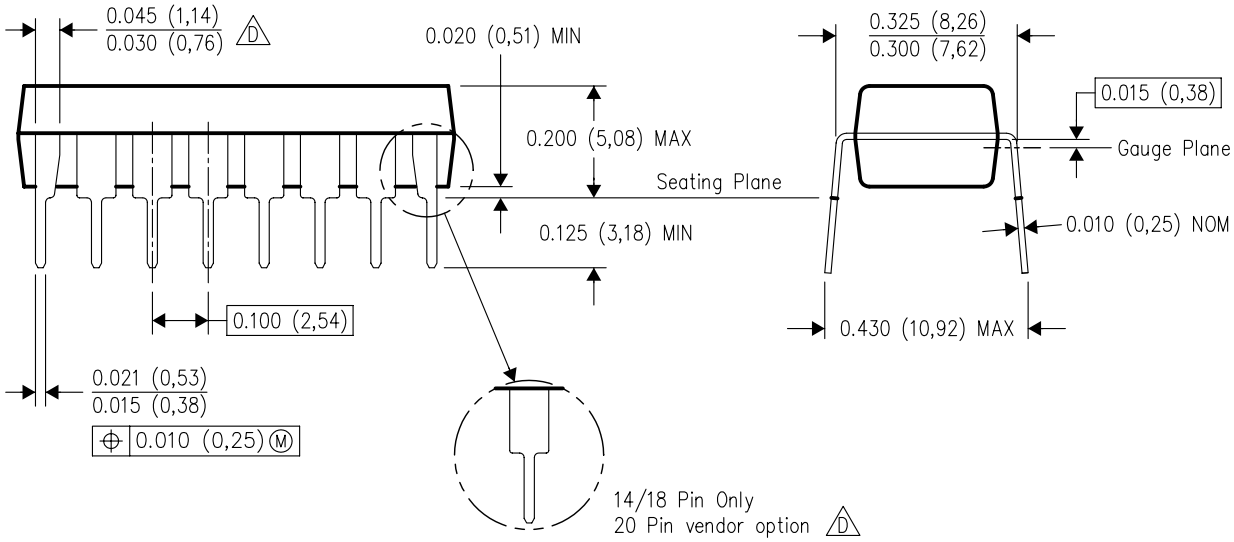
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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