

Memory Products Data Book

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SECTION 1
MICROCHIP TECHNOLOGY INC.
INTRODUCTION

Introduction 1-1

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MICROCHIP MICROCHIP TECHNOLOGY INC.

Section 1 - Introduction

1.0 INTRODUCTION

Microchip Technology Inc. is a leading provider of microcontrollers, analog and interface semiconductors, and serial nonvolatile memory. Based in Chandler, Arizona USA, Microchip owns its wafer fabrication facilities in Tempe, Arizona and Gresham, Oregon, as well as its own assembly and test facility in Thailand. One of the most solid and stable performers in the semiconductor world, Microchip provides a broad product portfolio meeting the needs of the embedded control market, including:

- 8-bit PIC® microcontrollers
- 16-bit PIC® microcontroller and dsPIC® digital signal controllers
- Complete line of Analog products including LDOs, PORs, Voltage refs, ADCs, DACs, op amps, comparators, PGAs, thermal management and power management solutions
- Interface products supporting CAN, IrDA® standard, LIN and serial
- High-performance specialty and standard serial EEPROM devices compatible with all three popular buses: I²C™, Microwire and SPI
- Security devices (KEELOQ® products)

Please request a Microchip Product Line Card for a listing of the entire Microchip product offering. This literature can be obtained from your local sales office or downloaded from Microchip's informative web site at www.microchip.com.

1.1 Manual Overview

Serial EEPROM product requirements are provided in three Family Data Sheets which have been grouped into the specific I²C™, Microwire, and SPI bus types. As of the date of printing, all data sheets are current and represent products that are in full production. Since this information is subject to change without notice, it is recommended that the latest version of the data sheet should be downloaded before finalizing any designs. Please check for the most recent revisions or product availability by contacting your local Microchip sales office, Representative, Distributor or by visiting us online at www.microchip.com/Memory.

All buses are compatible with de facto industry standards, including I²C, Microwire and SPI. In most cases the Microchip device can be used as a drop-in replacement for competitor devices. And for new designs, Microchip's value-added features can provide smaller footprint, lower power consumption, and faster bus rates than many commodity devices.

Two useful sections are provided at the front of the manual:

- Serial EEPROM Selection Guide – every serial EEPROM in the Microchip offering is listed here, along with the most important AC/DC parameters and package options for quick comparison and selection. Full data sheets are provided in this manual for each device listed in the Selection Guide. For the most up-to-date information, be sure to check Microchip's web site at www.microchip.com.
- Competitive Part Numbering Guide – this guide provides the basic part numbering schemes from several serial EEPROM manufacturers without having to search through endless versions of old data sheets for a part description. Since part numbers from each manufacturer contains unique codes for temperature, packaging and voltage, as well as other parameters, a single location with this information should be very useful when determining a Microchip replacement. Once the parameters from a competitive device are known, Microchip's MAPS (Microchip Advanced Parts Selector) tool can be used to determine the correct Microchip device to use. You can download MAPS at www.microchip.com/MAPS.

1.2 Key EEPROM Parameters

I²C EEPROMS from the 24AAXX family of devices now have a wider operating voltage from 1.7V to 5.5V over the entire density range from 128 bits to 1 Mbit. This meets the need for lower operating voltages to support the ever increasing number of battery operated systems. In addition, the higher speed 24FCXX family of devices can also meet the requirements for 400 kHz operation over the voltage range from 1.8V to 2.5V and 1 MHz at voltages of 2.5V and above.

SPI EEPROMs from the 25LCXX family of devices now have higher operating speeds for all densities ranging from 1 Kbit up to 1 Mbit. This includes speeds up to 10 MHz for densities up to 256 Kbits and 20 MHz for the 512 Kbit and 1 Mbit devices. As an added bonus, the 512K and 1 Mbit devices have been released as EEPROM/Flash devices. Designed as a robust EEPROM for high endurance, wide voltage range and byte/page operations, they also respond to standard Flash commands and sector operations.

1.3 Packaging: RoHS Compliant

Microchip serial EEPROMs are packaged at Microchip's own facilities and by authorized subcontractors. After packaging, whether in-house or outside at a subcontractor, every device is 100% tested again in a Microchip facility prior to shipment.

Microchip excels at micro-miniature packaging for serial EEPROMs, including the following:

- 8-lead SOIC – up to 1 Mbit
- 8-lead MSOP – up to 256 Kbits
- 8-lead TSSOP – up to 256 Kbits
- 5-lead SOT23 – up to 16 Kbits
- 6-lead SOT23 – up to 16 Kbits
- 8-lead 5x6 DFN – up to 1 Mbit
- 8-lead 2x3 DFN – up to 64 Kbits
- Die and wafer packaging – all densities

All products use Pb-free plating, and all are RoHS compliant. A rigorous qualification and production environment ensures high-temperature solderability, moisture sensitivity level, absence of whisker growth, and reliability of the new Pb-Free package family.

1.4 Quality

Microchip delivers the highest-quality serial EEPROM products in the world, with world-class line yields, well-designed processes, and rigorous Statistical Process Control (SPC) in each of its continuous-improvement facilities. Outgoing quality level is close to 0 ppm across nearly a billion serial EEPROMs shipped each year.

Each serial EEPROM is tested three times: first at wafer-level, where each individual die on the wafer receives 100% AC/DC testing of all data sheet parameters. At the end of that test, each die is programmed with data in each memory cell and then baked for five hours at 250°C to ensure data retention specs. Following the bake, every die on every wafer is tested again, including AC/DC data sheet parameters and special tests of the data array to verify oxide quality and to limit infant mortality. Finally, after packaging, every device receives a final functional test to screen out any potential assembly-related issues.

After final test, quality samples are taken continuously to monitor reliability. The resulting data is available annually in a formal report available at www.microchip.com.

For Microchip, quality is not a side issue - it is integral to our culture, our systems and our products. It is, in fact, our business model.

1.5 Development Tools

Microchip provides some of the best serial EEPROM tools in the industry, including:

- SEEVAL® 32 Designer's Kit – a feature-rich and easy-to-use programmer/data viewer supporting all Microchip Serial EEPROM products. This inexpensive tool can shorten time-to-market by weeks. Easy to set-up and use right out of the box, it can help solve a week's worth of headaches in an afternoon. See the Development Tools section of this manual for more information.
- Total Endurance™ software – a powerful mathematical model for predicting Erase/Write endurance of your specific serial EEPROM in your specific application. All serial EEPROMs, from all manufacturers, eventually experience bit-failures after some number of erase/write cycles. Microchip's serial EEPROM endurance is among the best in the world, and Total Endurance software is the only tool of its kind for modeling and predicting device lifetime. This can help designers to produce a robust design since trade-off analysis is so fast with this easy-to-use software modeling tool.

  Any discussion of endurance must include the parameters of voltage, temperature, semiconductor process, cell design, array size, bytes per cycle, and cycles per day in order to understand what the endurance number means - and to predict how a given device will perform in a particular application. Total Endurance software accepts your input of each of these parameters and outputs FIT rate or MTBF vs. time or vs. number of cycles. Download it for FREE at www.microchip.com.

1.6 e-Commerce

Microchip serial EEPROMs are available from any Microchip distributor, sales representative or sales office and even from Microchip's own e-commerce site, www.microchipDirect.com. They can also be sampled for free from Microchip's main web site www.microchip.com - and delivered fast. Just click the "Sample" button to order free samples or the "Buy Online" button to purchase serial EEPROMs using a credit card.

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SECTION 2
SERIAL EEPROM
SELECTION GUIDE AND CROSS REFERENCE

Serial EEPROM Selection Guide 2-1
Competitor Part Numbering Guide 2-9

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I²C™ Compatible

Device	Vcc Range	Write Protect	Page Size	Max Clock	Write Cycle	Cascade	Endurance	Temp Grade	Packages	Data Sheet
128-bit I²C compatible										
24AA00	1.8-5.5	No	N/A	400 kHz	4 ms	No	1,000,000	I	P, SN, ST, OT, MC	DS21178
24LC00	2.5-5.5	No	N/A	400 kHz	4 ms	No	1,000,000	I	P, SN, ST, OT, MC	DS21178
24C00	4.5-5.5	No	N/A	400 kHz	4 ms	No	1,000,000	I, E	P, SN, ST, OT, MC	DS21178
1Kbit I²C compatible										
24AA01	1.8-5.5	Yes	8 bytes	400 kHz	5 ms	No	1,000,000	I	P, SN, ST, MS, OT, MC	DS21711
24LC01B	2.5-5.5	Yes	8 bytes	400 kHz	5 ms	No	1,000,000	I, E	P, SN, ST, MS, OT, MC	DS21711
24C01C	4.5-5.5	Yes	16 bytes	400 kHz	1 ms	8	1,000,000	I, E	P, SN, ST, MS, MC	DS21201
24AA014	1.8-5.5	Yes	16 bytes	400 kHz	10 ms	8	1,000,000	I	P, SN, ST, MS, MC	DS21809
24LC014	2.5-5.5	Yes	16 bytes	400 kHz	10 ms	8	1,000,000	I	P, SN, ST, MS, MC	DS21809
24LC21A	2.5-5.5	No	8 bytes	400 kHz	10 ms	No	1,000,000	I	P, SN	DS21160
24LCS21A	2.5-5.5	Yes	8 bytes	400 kHz	10 ms	No	1,000,000	I	P, SN	DS21161
2Kbit I²C compatible										
24AA02	1.8-5.5	Yes	8 bytes	400 kHz	5 ms	No	1,000,000	I	P, SN, ST, MS, OT, MC	DS21709
24LC02B	2.5-5.5	Yes	8 bytes	400 kHz	5 ms	No	1,000,000	I, E	P, SN, ST, MS, OT, MC	DS21709
24LCS22A	2.5-5.5	Yes	8 bytes	400 kHz	10 ms	No	1,000,000	I	P, SN	DS21682
24C02C	4.5-5.5	Yes	16 bytes	400 kHz	1 ms	8	1,000,000	I, E	P, SN, ST, MS, MC	DS21202
24LCS52	2.5-5.5	Yes	16 bytes	400 kHz	5 ms	8	1,000,000	I	P, SN, ST, MS, MC	DS21166
24AA52	1.8-5.5	Yes	16 bytes	400 kHz	5 ms	8	1,000,000	I	P, SN, ST, MS, MC	DS21166
24AA024	1.8-5.5	Yes	16 bytes	400 kHz	10 ms	8	1,000,000	I	P, SN, ST, MS, MC	DS21210
24LC024	2.5-5.5	Yes	16 bytes	400 kHz	10 ms	8	1,000,000	I, E	P, SN, ST, MS, MC	DS21210
24AA025	1.8-5.5	No	16 bytes	400 kHz	10 ms	8	1,000,000	I	P, SN, ST, MS, MC	DS21210
24LC025	2.5-5.5	No	16 bytes	400 kHz	10 ms	8	1,000,000	I, E	P, SN, ST, MS, MC	DS21210

P = 8 PDIP, SN = 150 Mil SOIC, SM = 207 Mil SOIC, ST = 8 TSSOP, MS = 8 MSOP, OT = SOT-23, MF = 6x5 mm DFN, ST14 = 14 TSSOP, MC = 2x3 mm DFN

Most devices also available in die and wafer form. Please contact Microchip sales office.

I²C is a trademark of Philips Corporation.

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I²C Compatible

Device	Vcc Range	Write Protect	Page Size	Max Clock	Write Cycle	Cascade	Endurance	Temp Grade	Packages	Data Sheet
4Kbit I²C compatible										
24AA04	1.8-5.5	Yes	16 bytes	400 kHz	5 ms	No	1,000,000	I	P, SN, ST, MS, OT, MC	DS21708
24LC04B	2.5-5.5	Yes	16 bytes	400 kHz	5 ms	No	1,000,000	I, E	P, SN, ST, MS, OT, MC	DS21708
8Kbit I²C compatible										
24AA08	1.8-5.5	Yes	16 bytes	400 kHz	5 ms	No	1,000,000	I	P, SN, ST, MS, OT, MC	DS21710
24LC08B	2.5-5.5	Yes	16 bytes	400 kHz	5 ms	No	1,000,000	I, E	P, SN, ST, SM, OT, MC	DS21710
16Kbit I²C compatible										
24AA16	1.8-5.5	Yes	16 bytes	400 kHz	5 ms	No	1,000,000	I	P, SN, ST, MS, OT, MC	DS21703
24LC16B	2.5-5.5	Yes	16 bytes	400 kHz	5 ms	No	1,000,000	I, E	P, SN, ST, MS, OT, MC	DS21703
32Kbit I²C compatible										
24AA32A	1.8-5.5	Yes	32 bytes	400 kHz	5 ms	8	1,000,000	I	P, SN, ST, MS, MC	DS21713
24LC32A	2.5-5.5	Yes	32 bytes	400 kHz	5 ms	8	1,000,000	I, E	P, SN, ST, MS, MC	DS21713
64Kbit I²C compatible										
24AA64	1.8-5.5	Yes	32 bytes	400 kHz	5 ms	8	1,000,000	I	P, SN, ST, MS, MC	DS21189
24LC64	2.5-5.5	Yes	32 bytes	400 kHz	5 ms	8	1,000,000	I, E	P, SN, ST, MS, MC	DS21189
24AA65	1.8-5.5	Yes	64 bytes	400 kHz	2 ms	8	1M/10M	O	P, SM	DS21073
24LC65	2.5-5.5	Yes	64 bytes	400 kHz	2 ms	8	1M/10M	I	P, SM	DS21073
24C65	4.5-5.5	Yes	64 bytes	400 kHz	2 ms	8	1M/10M	I	P, SM	DS21073
128Kbit I²C compatible										
24AA128	1.8-5.5	Yes	64 bytes	400 kHz	5 ms	8	1,000,000	I	P, SN, ST, MS, MF	DS21191
24LC128	2.5-5.5	Yes	64 bytes	400 kHz	5 ms	8	1,000,000	I, E	P, SN, ST, MS, MF	DS21191
24FC128	1.8-5.5	Yes	64 bytes	1 MHz	5 ms	8	1,000,000	I	P, SN, ST, MS, MF	DS21191
256Kbit I²C compatible										
24AA256	1.8-5.5	Yes	64 bytes	400 kHz	5 ms	8	1,000,000	I	P, SN, ST, MS, MF	DS21203
24LC256	2.5-5.5	Yes	64 bytes	400 kHz	5 ms	8	1,000,000	I, E	P, SN, ST, MS, MF	DS21203
24FC256	1.8-5.5	Yes	64 bytes	1 MHz	5 ms	8	1,000,000	I	P, SN, ST, MS, MF	DS21203

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I²C Compatible

Device	Vcc Range	Write Protect	Page Size	Max Clock	Write Cycle	Cascade	Endurance	Temp Grade	Packages	Data Sheet
512Kbit I²C compatible										
24AA512	1.8-5.5	Yes	128 bytes	400 kHz	5 ms	8	1,000,000	I	P, SM, ST14, MF	DS21754
24LC512	2.5-5.5	Yes	128 bytes	400 kHz	5 ms	8	1,000,000	I, E	P, SM, ST14, MF	DS21754
24FC512	2.5-5.5	Yes	128 bytes	1 MHz	5 ms	8	1,000,000	I	P, SM, ST14, MF	DS21754
24AA515	1.8-5.5	Yes	64 bytes	400 kHz	5 ms	4	1,000,000	I	P, SM	DS21673
24LC515	2.5-5.5	Yes	64 bytes	400 kHz	5 ms	4	1,000,000	I	P, SM	DS21673
24FC515	2.5-5.5	Yes	64 bytes	1 MHz	5 ms	4	1,000,000	I	P, SM	DS21673

Microwire Compatible

Device	Vcc Range	ORG Pin	Word Size	Max Clock	Write Cycle	Endurance	Temp Grade	Packages	Data Sheet
1Kbit Microwire compatible									
93AA46A	1.8-5.5	No	8-bit	2 MHz	6 ms	1,000,000	I	P, SN, ST, MS, OT, MC	DS21749
93AA46B	1.8-5.5	No	16-bit	2 MHz	6 ms	1,000,000	I	P, SN, ST, MS, OT, MC	DS21749
93LC46A	2.5-5.5	No	8-bit	2 MHz	6 ms	1,000,000	I, E	P, SN, ST, MS, OT, MC	DS21749
93LC46B	2.5-5.5	No	16-bit	2 MHz	6 ms	1,000,000	I, E	P, SN, ST, MS, OT, MC	DS21749
93C46A	4.5-5.5	No	8-bit	2 MHz	2 ms	1,000,000	I, E	P, SN, ST, MS, OT, MC	DS21749
93C46B	4.5-5.5	No	16-bit	2 MHz	2 ms	1,000,000	I, E	P, SN, ST, MS, OT, MC	DS21749
93AA46C	1.8-5.5	Yes	8- or 16-bit	3 MHz	6 ms	1,000,000	I	P, SN, ST, MS, MC	DS21749
93LC46C	2.5-5.5	Yes	8- or 16-bit	3 MHz	6 ms	1,000,000	I, E	P, SN, ST, MS, MC	DS21749
93C46C	4.5-5.5	Yes	8- or 16-bit	3 MHz	2 ms	1,000,000	I, E	P, SN, ST, MS, MC	DS21749
2Kbit Microwire compatible									
93AA56A	1.8-5.5	No	8-bit	2 MHz	6 ms	1,000,000	I	P, SN, ST, MS, OT, MC	DS21794
93AA56B	1.8-5.5	No	16-bit	2 MHz	6 ms	1,000,000	I	P, SN, ST, MS, OT, MC	DS21794

P = 8 PDIP, SN = 150 Mil SOIC, SM = 207 Mil SOIC, ST = 8 TSSOP, MS = 8 MSOP, OT = SOT-23, MF = 6x5 mm DFN, ST14 = 14 TSSOP, MC = 2x3 mm DFN

Most devices also available in die and wafer form. Please contact Microchip sales office.

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Microwire Compatible

Device	Vcc Range	ORG Pin	Word Size	Max Clock	Write Cycle	Endurance	Temp Grade	Packages	Data Sheet
2Kbit Microwire compatible (continued)									
93LC56A	2.5-5.5	No	8-bit	2 MHz	6 ms	1,000,000	I, E	P, SN, ST, MS, OT, MC	DS21794
93LC56B	2.5-5.5	No	16-bit	2 MHz	6 ms	1,000,000	I, E	P, SN, ST, MS, OT, MC	DS21794
93C56A	4.5-5.5	No	8-bit	2 MHz	2 ms	1,000,000	I, E	P, SN, ST, MS, OT, MC	DS21794
93C56B	4.5-5.5	No	16-bit	2 MHz	2 ms	1,000,000	I, E	P, SN, ST, MS, OT, MC	DS21794
93AA56C	1.8-5.5	Yes	8- or 16-bit	3 MHz	6 ms	1,000,000	I	P, SN, ST, MS, MC	DS21794
93LC56C	2.5-5.5	Yes	8- or 16-bit	3 MHz	6 ms	1,000,000	I, E	P, SN, ST, MS, MC	DS21794
93C56C	4.5-5.5	Yes	8- or 16-bit	3 MHz	2 ms	1,000,000	I, E	P, SN, ST, MS, MC	DS21794
4Kbit Microwire compatible									
93AA66A	1.8-5.5	No	8-bit	2 MHz	6 ms	1,000,000	I	P, SN, ST, MS, OT, MC	DS21795
93AA66B	1.8-5.5	No	16-bit	2 MHz	6 ms	1,000,000	I	P, SN, ST, MS, OT, MC	DS21795
93LC66A	2.5-5.5	No	8-bit	2 MHz	6 ms	1,000,000	I, E	P, SN, ST, MS, OT, MC	DS21795
93LC66B	2.5-5.5	No	16-bit	2 MHz	6 ms	1,000,000	I, E	P, SN, ST, MS, OT, MC	DS21795
93C66A	4.5-5.5	No	8-bit	2 MHz	2 ms	1,000,000	I, E	P, SN, ST, MS, OT, MC	DS21795
93C66B	4.5-5.5	No	16-bit	2 MHz	2 ms	1,000,000	I, E	P, SN, ST, MS, OT, MC	DS21795
93AA66C	1.8-5.5	Yes	8- or 16-bit	3 MHz	6 ms	1,000,000	I	P, SN, ST, MS, MC	DS21795
93LC66C	2.5-5.5	Yes	8- or 16-bit	3 MHz	6 ms	1,000,000	I, E	P, SN, ST, MS, MC	DS21795
93C66C	4.5-5.5	Yes	8- or 16-bit	3 MHz	2 ms	1,000,000	I, E	P, SN, ST, MS, MC	DS21795
8Kbit Microwire compatible									
93AA76A	1.8-5.5	No	8-bit	3 MHz	6 ms	1,000,000	I	OT	DS21796
93AA76B	1.8-5.5	No	16-bit	3 MHz	6 ms	1,000,000	I	OT	DS21796
93LC76A	2.5-5.5	No	8-bit	3 MHz	6 ms	1,000,000	I, E	OT	DS21796
93LC76B	2.5-5.5	No	16-bit	3 MHz	6 ms	1,000,000	I, E	OT	DS21796
93C76A	4.5-5.5	No	8-bit	3 MHz	2 ms	1,000,000	I, E	OT	DS21796
93C76B	4.5-5.5	No	16-bit	3 MHz	2 ms	1,000,000	I, E	OT	DS21796
93AA76C	1.8-5.5	Yes	8- or 16-bit	3 MHz	6 ms	1,000,000	I	P, SN, ST, MS, MC	DS21796
93LC76C	2.5-5.5	Yes	8- or 16-bit	3 MHz	6 ms	1,000,000	I, E	P, SN, ST, MS, MC	DS21796
93C76C	4.5-5.5	Yes	8- or 16-bit	3 MHz	2 ms	1,000,000	I, E	P, SN, ST, MS, MC	DS21796

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Microwire Compatible

Device	Vcc Range	ORG Pin	Word Size	Max Clock	Write Cycle	Endurance	Temp Grade	Packages	Data Sheet
16Kbit Microwire compatible									
93AA86A	1.8-5.5	No	8-bit	3 MHz	6 ms	1,000,000	I	OT	DS21797
93AA86B	1.8-5.5	No	16-bit	3 MHz	6 ms	1,000,000	I	OT	DS21797
93LC86A	2.5-5.5	No	8-bit	3 MHz	6 ms	1,000,000	I, E	OT	DS21797
93LC86B	2.5-5.5	No	16-bit	3 MHz	6 ms	1,000,000	I, E	OT	DS21797
93C86A	4.5-5.5	No	8-bit	3 MHz	2 ms	1,000,000	I, E	OT	DS21797
93C86B	4.5-5.5	No	16-bit	3 MHz	2 ms	1,000,000	I, E	OT	DS21797
93AA86C	1.8-5.5	Yes	8- or 16-bit	3 MHz	6 ms	1,000,000	I	P, SN, ST, MS, MC	DS21797
93LC86C	2.5-5.5	Yes	8- or 16-bit	3 MHz	6 ms	1,000,000	I, E	P, SN, ST, MS, MC	DS21797

SPI Compatible Products

Device	Vcc Range	Write Protect	Page Size	Max Clock	Write Cycle	Endurance	Temp Grade	Packages	Data Sheet
1Kbit SPI compatible									
25AA010A	1.8-5.5	Yes	16 byte	10 MHz	5 ms	1,000,000	I	P, MS, SN, ST, MC	DS21832
25LC010A	2.5-5.5	Yes	16 byte	10 MHz	5 ms	1,000,000	I, E	P, MS, SN, ST, MC	DS21832
2Kbit SPI compatible									
25AA020A	1.8-5.5	Yes	16 byte	10 MHz	5 ms	1,000,000	I	P, MS, SN, ST, MC	DS21833
25LC020A	2.5-5.5	Yes	16 byte	10 MHz	5 ms	1,000,000	I, E	P, MS, SN, ST, MC	DS21833
4Kbit SPI compatible									
25AA040A	1.8-5.5	Yes	16 byte	10 MHz	5 ms	1,000,000	I	P, MS, SN, ST, MC	DS21827
25LC040A	2.5-5.5	Yes	16 byte	10 MHz	5 ms	1,000,000	I, E	P, MS, SN, ST, MC	DS21827

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SPI Compatible Products

Device	Vcc Range	Write Protect	Page Size	Max Clock	Write Cycle	Endurance	Temp Grade	Packages	Data Sheet
8Kbit SPI compatible									
25AA080A	1.8-5.5	Yes	16 byte	10 MHz	5 ms	1,000,000	I	P, SN, ST, MS	DS21808
25AA080B	1.8-5.5	Yes	32 byte	10 MHz	5 ms	1,000,000	I	P, SN, ST, MS	DS21808
25LC080A	2.5-5.5	Yes	16 byte	10 MHz	5 ms	1,000,000	I, E	P, SN, ST, MS	DS21808
25LC080B	2.5-5.5	Yes	32 byte	10 MHz	5 ms	1,000,000	I, E	P, SN, ST, MS	DS21808
16Kbit SPI compatible									
25AA160A	1.8-5.5	Yes	16 byte	10 MHz	5 ms	1,000,000	I	P, SN, ST, MS	DS21807
25AA160B	1.8-5.5	Yes	32 byte	10 MHz	5 ms	1,000,000	I	P, SN, ST, MS	DS21807
25LC160A	2.5-5.5	Yes	16 byte	10 MHz	5 ms	1,000,000	I, E	P, SN, ST, MS	DS21807
25LC160B	2.5-5.5	Yes	32 byte	10 MHz	5 ms	1,000,000	I, E	P, SN, ST, MS	DS21807
32Kbit SPI compatible									
25AA320A	1.8-5.5	Yes	32 byte	10 MHz	5 ms	1,000,000	I	P, MS, SN, ST	DS21828
25LC320A	2.5-5.5	Yes	32 byte	10 MHz	5 ms	1,000,000	I, E	P, MS, SN, ST	DS21828
64Kbit SPI compatible									
25AA640A	1.8-5.5	Yes	32 byte	10 MHz	5 ms	1,000,000	I	P, MS, SN, ST	DS21830
25LC640A	2.5-5.5	Yes	32 byte	10 MHz	5 ms	1,000,000	I, E	P, MS, SN, ST	DS21830
128Kbit SPI compatible									
25AA128	1.8-5.5	Yes	64 byte	10 MHz	5 ms	1,000,000	I	P, SN, ST, MF	DS21831
25LC128	2.5-5.5	Yes	64 byte	10 MHz	5 ms	1,000,000	I, E	P, SN, ST, MF	DS21831
256Kbit SPI compatible									
25AA256	1.8-5.5	Yes	64 byte	10 MHz	5 ms	1,000,000	I	P, SN, ST, MF	DS21822
25LC256	2.5-5.5	Yes	64 byte	10 MHz	5 ms	1,000,000	I, E	P, SN, ST, MF	DS21822
512Kbit SPI compatible									
25AA512	1.8-5.5	Yes	128 byte	20 MHz	5 ms	1,000,000	I	P, SN, MF	DS22021
25LC512	2.5-5.5	Yes	128 byte	20 MHz	5 ms	1,000,000	I, E	P, SN, MF	DS22021

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SPI Compatible Products

Device	Vcc Range	Write Protect	Page Size	Max Clock	Write Cycle	Endurance	Temp Grade	Packages	Data Sheet
1 Mbit SPI compatible									
25AA1024	1.8-5.5	Yes	256 byte	20 MHz	5 ms	1,000,000	I	P, SM, MF	DS21836
25LC1024	2.5-5.5	Yes	256 byte	20 MHz	5 ms	1,000, 000	I, E	P, SM, MF	DS21836

Plug-and-Play® and ID Products

Device	Density	Vcc Range	Write Protect	Page Size	Max Clock	Write Cycle	Type	Endurance	Temp Grade	Packages	Data Sheet
Serial EEPROMs for DRAM DIMM modules											
24LCS52	2Kbit	2.5-5.5	Yes	16 bytes	400 kHz	5 ms	DDR	1,000,000	I	P, SN, ST, MS, MC	DS21166
24AA52	2Kbit	1.8-5.5	Yes	16 bytes	400 kHz	5 ms	DDR	1,000,000	I	P, SN, ST, MS, MC	DS21166
24LC024	2Kbit	2.5-5.5	Yes	16 bytes	400 kHz	5 ms	DDR	1,000,000	I, E	P, SN, ST, MS, MC	DS21210
24LC025	2Kbit	2.5-5.5	No	16 bytes	400 kHz	5 ms	DDR	1,000,000	I, E	P, SN, ST, MS, MC	DS21210
Serial EEPROMs for VESA® monitors, projectors and flat panels											
24LC21A	1Kbit	2.5-5.5	No	8 bytes	400 kHz	10 ms	—	1,000,000	I	P, SN	DS21160
24LCS21A	1Kbit	2.5-5.5	Yes	8 bytes	400 kHz	10 ms	—	1,000,000	I	P, SN	DS21161
24LCS22A	2Kbit	2.5-5.5	Yes	8 bytes	400 kHz	10 ms	—	1,000,000	I	P, SN	DS21682
34LC02	2Kbit	2.5-5.5	Yes	16 bytes	400 kHz	5 ms	DDR2/3	1,000,000	I/E	P, SN, ST, MS, MC	DS22029
34AA02	2Kbit	1.7-5.5	Yes	16 bytes	400 kHz	5 ms	DDR2/3	1,000,000	I	P, SN, ST, MS, MC	DS22029
34LV02	2Kbit	1.5-5.5	Yes	16 bytes	400 kHz	5 ms	DDR2/3	1,000,000	I	P, SN, ST, MS, MC	DS22029
Serial EEPROMs for other ID applications											
24AA00	128 bit	1.8-5.5	No	N/A	400 kHz	4 ms	—	1,000,000	I	P, SN, ST, OT, MC	DS21178
24LC00	128 bit	2.5-5.5	No	N/A	400 kHz	4 ms	—	1,000,000	I	P, SN, ST, OT, MC	DS21178
24C00	128 bit	4.5-5.5	No	N/A	400 kHz	4 ms	—	1,000,000	I, E	P, SN, ST, OT, MC	DS21178

P = 8 PDIP, SN = 150 Mil SOIC, SM = 207 Mil SOIC, ST = 8 TSSOP, MS = 8 MSOP, OT = SOT-23, MF = 8 DFN, ST14 = 14 TSSOP

Most devices also available in die and wafer form. Please contact Microchip sales office.

Smart Card Devices

Device	Vcc Range	Write Protect	Page Size	Max Clock	Write Cycle	Endurance	Temp Grade	Packages	Pb-Free Available	Data Sheet
Smart-Card devices (meet ISO 7816 bondout)										
24AA01SC	1.8-5.5	Yes	8 bytes	400 kHz	5 ms	1,000,000	I	W, WF, S	N/A	DS21748
24LC01SC	2.5-5.5	Yes	8 bytes	400 kHz	5 ms	1,000,000	I	W, WF, S	N/A	DS21748
24AA02SC	1.8-5.5	Yes	8 bytes	400 kHz	5 ms	1,000,000	I	W, WF, S	N/A	DS21747
24LC02SC	2.5-5.5	Yes	8 bytes	400 kHz	5 ms	1,000,000	I	W, WF, S	N/A	DS21747
24AA04SC	1.8-5.5	Yes	16 bytes	400 kHz	5 ms	1,000,000	I	W, WF, S	N/A	DS21745
24LC04SC	2.5-5.5	Yes	16 bytes	400 kHz	5 ms	1,000,000	I	W, WF, S	N/A	DS21745
24AA08SC	1.8-5.5	Yes	16 bytes	400 kHz	5 ms	1,000,000	I	W, WF, S	N/A	DS21746
24LC08SC	2.5-5.5	Yes	16 bytes	400 kHz	5 ms	1,000,000	I	W, WF, S	N/A	DS21746
24AA16SC	1.8-5.5	Yes	16 bytes	400 kHz	5 ms	1,000,000	I	W, WF, S	N/A	DS20093
24LC16SC	2.5-5.5	Yes	16 bytes	400 kHz	5 ms	1,000,000	I	W, WF, S	N/A	DS20093
24AA32ASC	1.8-5.5	Yes	32 bytes	400 kHz	5 ms	1,000,000	I	W, WF, S	N/A	DS21723
24LC32ASC	2.5-5.5	Yes	32 bytes	400 kHz	5 ms	1,000,000	I	W, WF, S	N/A	DS21723
24AA64SC	1.8-5.5	Yes	32 bytes	400 kHz	5 ms	1,000,000	I	W, WF, S	N/A	DS21716
24LC64SC	2.5-5.5	Yes	32 bytes	400 kHz	5 ms	1,000,000	I	W, WF, S	N/A	DS21716
24AA128SC	1.8-5.5	Yes	64 bytes	400 kHz	5 ms	1,000,000	I	W, WF, S	N/A	DS20095
24LC128SC	2.5-5.5	Yes	64 bytes	400 kHz	5 ms	1,000,000	I	W, WF, S	N/A	DS20095
24AA256SC	1.8-5.5	Yes	64 bytes	400 kHz	5 ms	1,000,000	I	W, WF, S	N/A	DS20094
24LC256SC	2.5-5.5	Yes	64 bytes	400 kHz	5 ms	1,000,000	I	W, WF, S	N/A	DS20094
24AA512SC	1.8-5.5	Yes	128 bytes	400 kHz	5 ms	1,000,000	I	W, WF, S	N/A	DS21785
24LC512SC	2.5-5.5	Yes	128 bytes	400 kHz	5 ms	1,000,000	I	W, WF, S	N/A	DS21785

W = wafer, WF = wafer on frame, S = single die in waffle pack.

Standard backgrind thickness are 11 and 15 mil and unground (29 mils).

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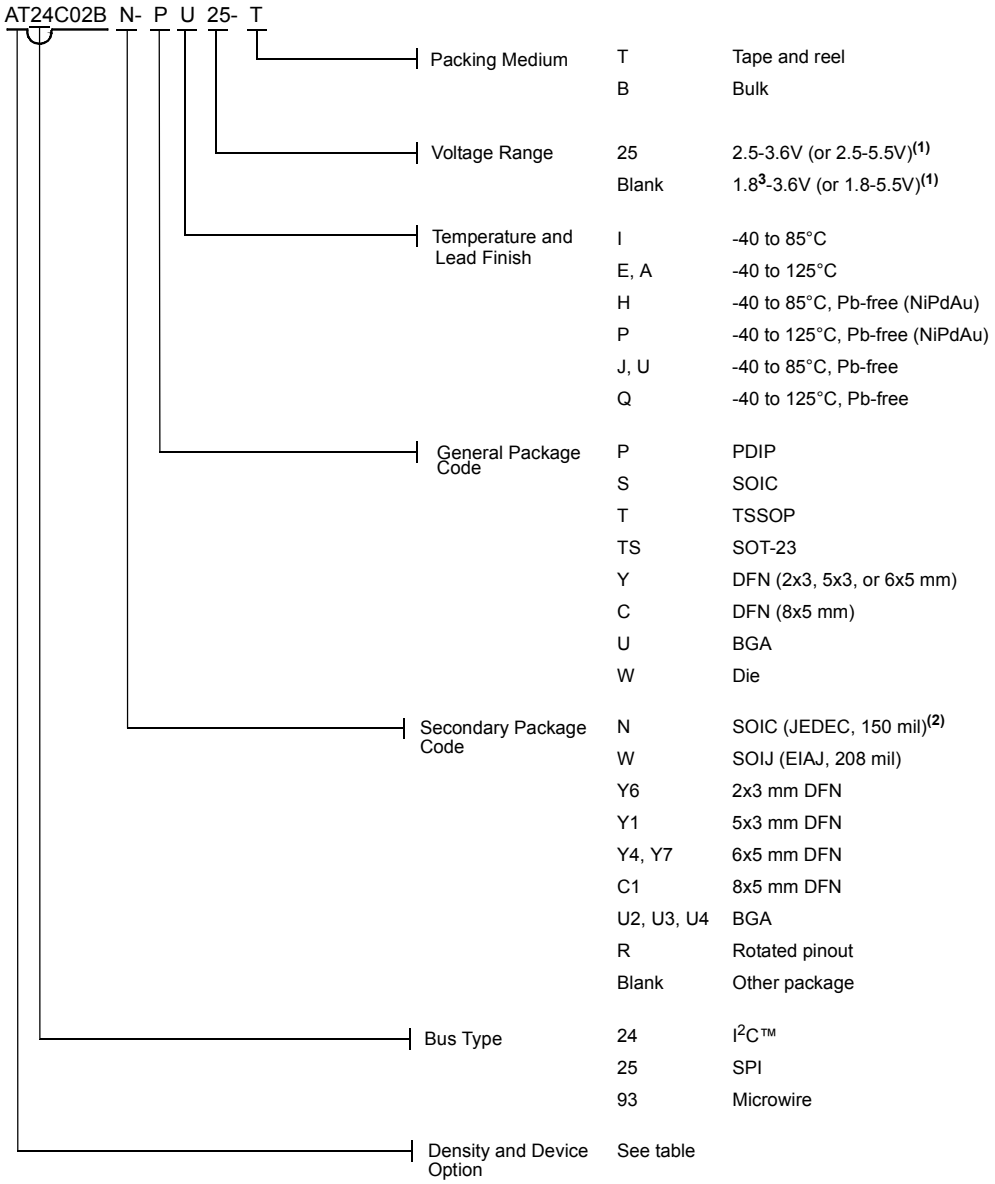
SERIAL EEPROMS

Competitor Part Numbering Guide

In order to cross-reference a competitor device to a compatible Microchip device, use Microchip's powerful MAPS tool available for free at www.microchip.com/MAPS. You can also decode the competitor part number here, where we have provided a means to translate each code or character.

Atmel Serial EEPROM Part Number Designations for Newer Products

(See also the separate table for Older Atmel Products)



Device Option	Bus	Density	Comment
AT24C01B(1)	I²C™	1 Kbit	
AT24C02(1)	I²C	2 Kbit	
AT24HC02B(1)	I²C	2 Kbit	1/2 array WP
AT34C02C(3)	I²C	2 Kbit	DIMM serial presence detect, 1.7-3.6V
AT24HC04B(1)	I²C	4 Kbit	1/2 array WP
AT24C16B	I²C	16 Kbit	Whole array WP, 1.8-3.6V
AT24C32C	I²C	32 Kbit	Whole array WP, 1.8-3.6V
AT24C64C	I²C	64 Kbit	Whole array WP, 1.8-3.6V
AT24C128B	I²C	128 Kbit	1.8-3.6V
AT24C256B	I²C	256 Kbit	1.8-3.6V
AT24C512B	I²C	512 Kbit	1.8-3.6V
AT24C1024B	I²C	1 Mbit	-1.8 version is maximum 3.6V; -2.7 max. is 5.5V
AT25512	SPI	512 Kbit	
AT93C46D	Microwire	1 Kbit	x8 or x16
AT93C46E	Microwire	1 Kbit	x16 (no ORG pin)

Note 1: AT24C01B, 24C02B, 24HC02B and 24HC04B have maximum voltages of 5.5V.

2: The “N” secondary package code is not always used.

3: The AT34C02C has a 1.7-3.6V range.

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Atmel Serial EEPROM Part Number Designations for Older Products

(See also the separate table for Newer Atmel Products)

AT24C32A N- 10 S U- 2.7 T

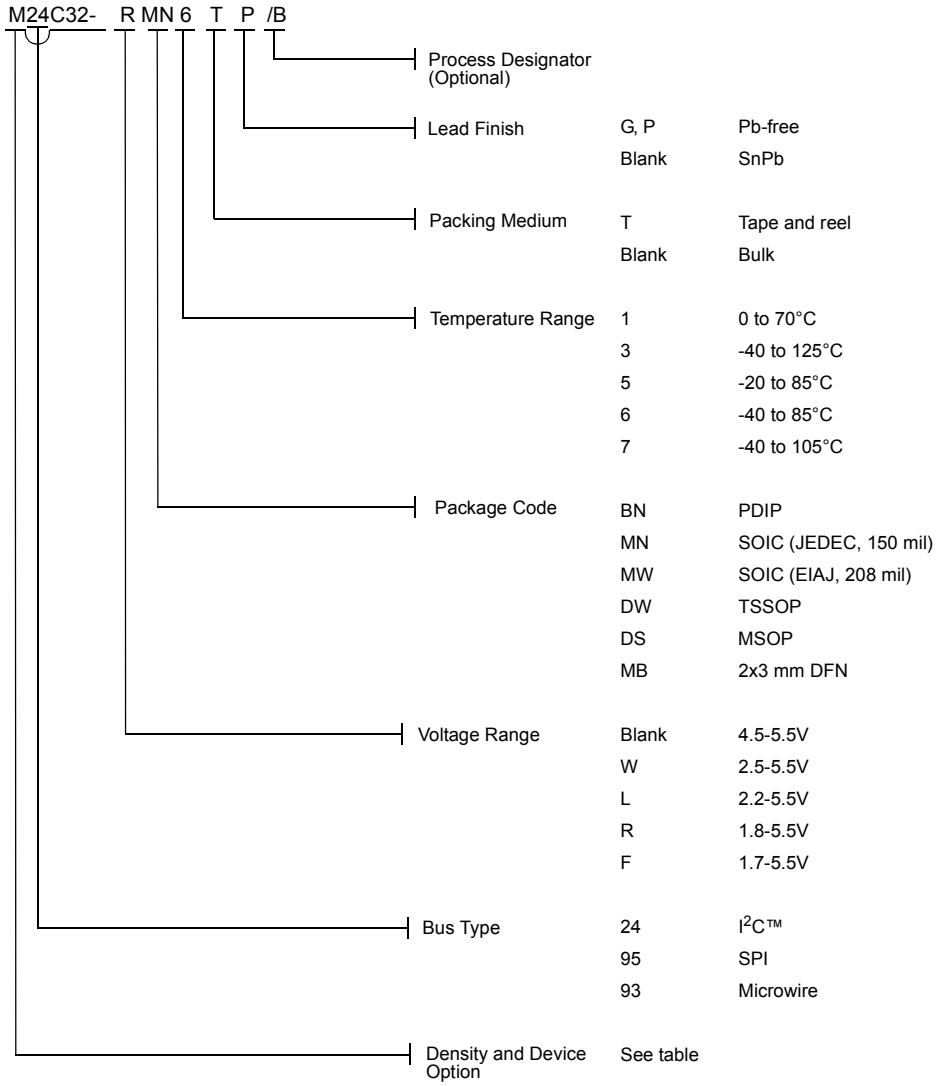
Packing Medium	T	Tape and reel
	B	Bulk
Voltage Range	5.0	4.5-5.5V
	2.7	2.7-5.5V
	1.8	1.8-5.5V (or 1.8-3.6V)(1)
	1.7	1.7-3.6V
Temperature and Lead Finish	I	-40 to 85°C
	E, A	-40 to 125°C
	J, U	-40 to 85°C, Pb-free
	H	-40 to 85°C, Pb-free (NiPdAu)
	Q	-40 to 125°C, Pb-free
General Package Code	P	PDIP
	S	SOIC
	T	TSSOP
	TS	SOT-23
	Y	DFN (2x3, 5x3, or 6x5 mm)
	C	DFN (8x5 mm)
	U	BGA
	W	Die
Secondary Package Code	N	SOIC (JEDEC, 150 mil)(2)
	W	SOIJ (EIAJ, 208 mil)
	Y1	5x3 DFN
	Y4	6x5 DFN
	Y6	2x3 DFN
	C1	8x5 DFN
	U2, U3, U4	BGA
	R	Rotated pinout
	Blank	Other package
Bus Type	24	I²C™
	25	SPI
	93	Microwire
Density and Device Option	See table	

Note 1: AT24C128-1.8, AT24CS128-1.8 and AT24C256-1.8 have voltage ranges of 1.8-3.6V.

2: The “N” secondary package code is not always used.

Device Option	Bus	Density	Comment
AT24C01, C11	I²C™	1 Kbit	No WP, no address pins
AT24C01A	I²C	1 Kbit	Whole array WP, 3 address pins
AT24C02	I²C	2 Kbit	Whole array WP
AT24C02A	I²C	2 Kbit	1/2 array WP
AT34C02/02B	I²C	2 Kbit	DIMM serial presence detect
AT24C04	I²C	4 Kbit	Whole array WP
AT24C04A	I²C	4 Kbit	1/2 array WP
AT24C08	I²C	8 Kbit	No WP
AT24C08A	I²C	8 Kbit	Whole array WP
AT24C16	I²C	16 Kbit	1/2 array WP, no address pins
AT24C16A	I²C	16 Kbit	Whole array WP, no address pins
AT24C164	I²C	16 Kbit	Whole array WP, 3 address pins
AT24C32	I²C	32 Kbit	1/4 array WP
AT24C32A	I²C	32 Kbit	Whole array WP
AT24C64/64B	I²C	64 Kbit	1/4 array WP
AT24C64A	I²C	64 Kbit	Whole array WP
AT24C128(1)/CS128	I²C	128 Kbit	-1.8 version is maximum 3.6V; -2.7 max is 5.5V
AT24C256(1)	I²C	256 Kbit	-1.8 version is maximum 3.6V; -2.7 max is 5.5V
AT24C512	I²C	512 Kbit	-1.8 version is maximum 3.6V; -2.7 max is 5.5V
AT24C1024	I²C	1 Mbit	
AT25010/010A	SPI	1 Kbit	
AT25020/020A	SPI	2 Kbit	
AT25040/040A	SPI	4 Kbit	
AT25080/080A	SPI	8 Kbit	
AT25160/160A	SPI	16 Kbit	
AT25320/320A	SPI	32 Kbit	
AT25640/640A	SPI	64 Kbit	
AT25128/128A	SPI	128 Kbit	
AT25256/256A	SPI	256 Kbit	
AT25HP256	SPI	256 Kbit	
AT25HP512	SPI	512 Kbit	
AT25P1024	SPI	1 Mbit	
AT93C46/46D	Microwire	1 Kbit	
AT93C46A/46C/46E	Microwire	1 Kbit	x16 only (no ORG pin)
AT93C56/56A		2 Kbit	
AT93C66/66A		4 Kbit	
AT93C86A	Microwire	16 Kbit	

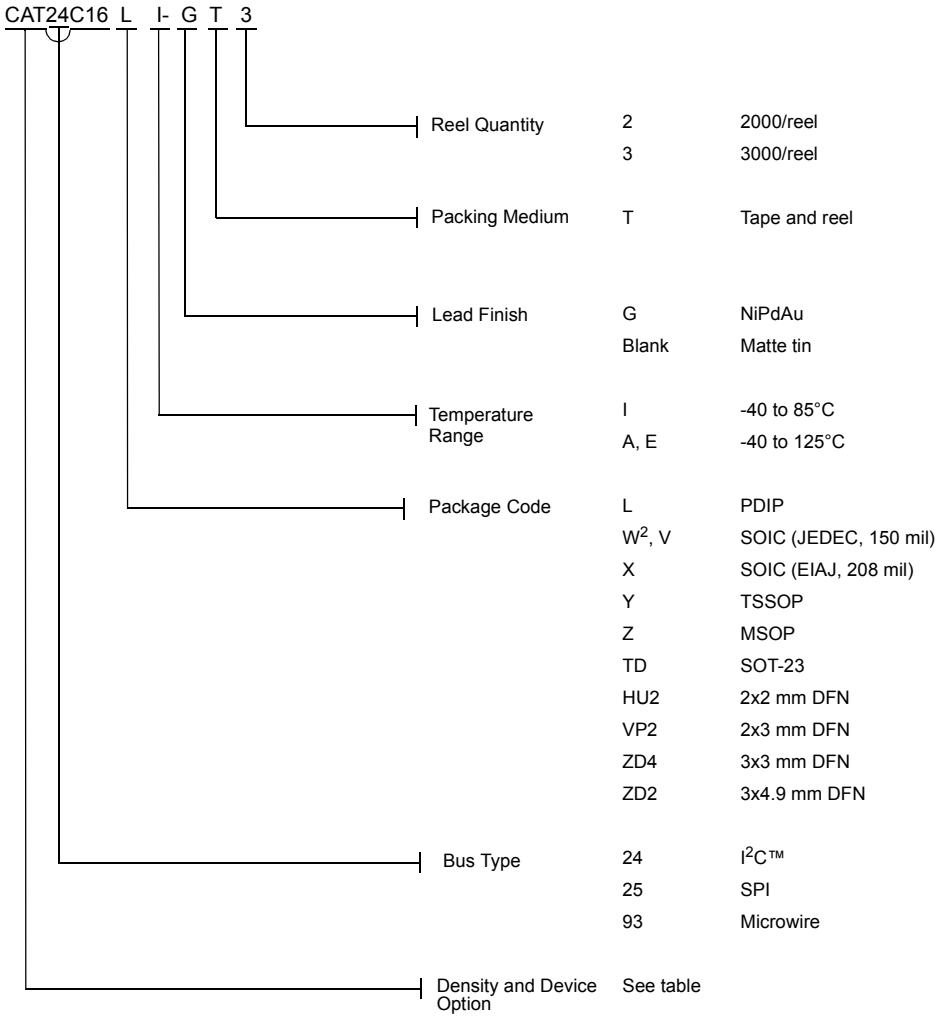
STMicroelectronics Serial EEPROM Part Number Designations



Device Option	Bus	Density	Comment
M24C01	I^2C™	1 Kbit	
M24C02	I^2C	2 Kbit	
M34C02	I^2C	2 Kbit	DIMM serial presence detect
M34E02	I^2C	2 Kbit	DIMM serial presence detect
M34F04	I^2C	4 Kbit	1/2 array WP
M24C04	I^2C	4 Kbit	
M24C08	I^2C	8 Kbit	
M24C16	I^2C	16 Kbit	
M24C32	I^2C	32 Kbit	
M24C64	I^2C	64 Kbit	
M34D64	I^2C	64 Kbit	1/4 array write-protect
M24128-B	I^2C	128 Kbit	
M24256-B	I^2C	128 Kbit	
M24512	I^2C	512 Kbit	
M24M01	I^2C	1 Mbit	
M95010	SPI	1 Kbit	
M95020	SPI	2 Kbit	
M95040	SPI	4 Kbit	
M95080	SPI	8 Kbit	
M95160	SPI	16 Kbit	
M95320	SPI	32 Kbit	
M95640	SPI	64 Kbit	
M95128	SPI	128 Kbit	
M95256	SPI	256 Kbit	
M95512	SPI	512 Kbit	
M95M01	SPI	1 Mbit	
M93C46	Microwire	1 Kbit	
M93C56	Microwire	2 Kbit	
M93C66	Microwire	4 Kbit	
M93C76	Microwire	8 Kbit	
M93C86	Microwire	16 Kbit	

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Catalyst Serial EEPROM Part Number Designations for Newer Products
(See also the separate table for Older Catalyst Products)



Note 1: Voltage range for all parts is 1.8-5.5V.
2: For 93-series products, package code “W” is an alternate, rotated pinout. “V” is the standard pinout.

Device Option	Bus	Density	Comment
CAT24C01	I²C™	1 Kbit	
CAT24C02	I²C	2 Kbit	Full array WP
CAT34C02	I²C	2 Kbit	DIMM serial presence detect; 1.7-5.5V
CAT24C03	I²C	2 Kbit	1/2 array WP
CAT24C04	I²C	4 Kbit	Full array WP
CAT24C05	I²C	4 Kbit	1/2 array WP
CAT24C08	I²C	8 Kbit	
CAT24C16	I²C	16 Kbit	No address pins
CAT24C164	I²C	16 Kbit	3 address pins
CAT24C32	I²C	32 Kbit	
CAT24C64	I²C	64 Kbit	
CAT24C128	I²C	128 Kbit	
CAT24C256	I²C	256 Kbit	
CAT25010	SPI	1 Kbit	
CAT25020	SPI	2 Kbit	
CAT25040	SPI	4 Kbit	
CAT25080	SPI	8 Kbit	
CAT25160	SPI	16 Kbit	
CAT25320	SPI	32 Kbit	
CAT25640	SPI	64 Kbit	
CAT93C46	Microwire	1 Kb	
CAT93C46R	Microwire	1 Kb	
CAT93C66	Microwire	2 Kb	Older die revs follow the “old” part number convention
CAT93C76	Microwire	8 Kb	

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Catalyst Serial EEPROM Part Number Designations for Older Products
(See also the separate table for Newer Catalyst Products)

CAT24WC16 P I- 1.8- G TE13

Packing Medium	TE13, T2, T3 Tape and Reel	
Lead Finish	Blank	See package code below
	G	NiPdAu
Voltage Range	3	3.0-5.5V
	Blank	2.5-5.5V
	1.8	1.8-5.5V
Temperature Range	Blank	0 to 70°C
	I	-40 to 85°C
	A	-40 to 105°C
	E	-40 to 125°C
Package Code	P	PDIP
	J^2, S	SOIC (JEDEC, 150 mil)
	K	SOIC (EIAJ, 208 mil)
	U	TSSOP
	TP	SOT-23
	R	MSOP
	SP2	2x3 mm DFN
	L, GL	PDIP, Pb-free
	TB, GTB	SOT-23, Pb-free
	W^2, V, GW, GV	SOIC (JEDEC, 150 mil), Pb-free
	X, GX	SOIC (EIAJ, 208 mil), Pb-free
	Y, GY	TSSOP, Pb-free
	Z, GZ	MSOP, Pb-free
	VP2	2x3 mm DFN, Pb-free
Bus Type	24	I^2C™
	25	SPI
	93	Microwire
Density and Device Option	See table	

Device Option	Bus	Density	Comment
CAT24C00(1, 3)	I^2C™	128 bit	
CAT24FC01(3)	I^2C	1 Kbit	
CAT24WC01	I^2C	1 Kbit	
CAT24C01B(3)	I^2C	1 Kbit	No WP
CAT24FC02(3)/WC02	I^2C	2 Kbit	
CAT24WC04	I^2C	4 Kbit	
CAT24WC08	I^2C	8 Kbit	
CAT24WC16(3)	I^2C	16 Kbit	
CAT24WC164(3)	I^2C	16 Kbit	3 address pins
CAT24FC17(3)	I^2C	16 Kbit	1/2 array WP
CAT24FC32(3)/FC32A(3)/WC32	I^2C	32 Kbit	
CAT24WC33	I^2C	32 Kbit	1/4 array WP
CAT24FC64(3)/WC64	I^2C	64 Kbit	
CAT24F65(3)/WC65(3)/FC66(3)	I^2C	64 Kbit	
CAT24WC66	I^2C	64 Kbit	
CAT24WC128/AC128/WC129(3)	I^2C	128 Kbit	
CAT24FC256(3)	I^2C	256 Kbit	
CAT24WC256/WC257(3)	I^2C	256 Kbit	
CAT25C01(3)/C11(3)	SPI	1 Kbit	
CAT25C02(3)/C03(3)	SPI	2 Kbit	
CAT25C04(3)/C05(3)	SPI	4 Kbit	
CAT25C08/C09(3)	SPI	8 Kbit	
CAT25C16/C17(3)	SPI	16 Kbit	
CAT25C32/C33(3)	SPI	32 Kbit	
CAT25C64/C65(3)	SPI	64 Kbit	
CAT25C128	SPI	128 Kbit	
CAT25C256	SPI	256 Kbit	
93HC46(3)	Microwire	1 Kbit	
93C56/C57	Microwire	2 Kbit	
93C66	Microwire	4 Kbit	
93C86	Microwire	16 Kbit	

Note 1: CAT24C00 has a voltage range of 1.8 to 5.5V.
2: For 93-series products, package codes “W” and ”J” are alternate, rotated pinouts. “V” and “S” are standard pinouts.
3: Discontinued part.

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SECTION 3
FAMILY DATA SHEETS

I²C™ Serial EEPROM Family Data Sheet 3-1
1K-16K Microwire Compatible Serial EEPROM Family Data Sheet 3-31
SPI Serial EEPROM Family Data Sheet 3-57
Speciality Product References 3-89

I²C is a trademark of Philips Corporation.
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I²C™ Serial EEPROM Family Data Sheet

Features:

- 128-bit through 1024 Kbit Devices
- Single Supply with Operation Down to 1.7V for 24AAXX Devices
- Low-Power CMOS Technology:
  - 1 mA active current, typical
  - 1 μA standby current, typical (I-temp)
- 2-Wire Serial Interface Bus, I²C™ Compatible
- Schmitt Trigger Inputs for Noise Suppression
- Output Slope Control to Eliminate Ground Bounce
- 400 kHz (≥ 2.5V): 24LCXX and 24AAXX
- 1 MHz (≥ 2.5V) and 400 kHz (1.7V): 24FCXX
- Self-Timed Write Cycle (including Auto-Erase)
- Page Write Buffer
- Hardware Write-Protect Available on Most Devices
- Factory Programming (QTP) Available
- ESD Protection >4,000V
- 1 Million Erase/Write Cycles
- Data Retention >200 years
- 8-lead PDIP, SOIC, TSSOP and MSOP Packages
- 5-lead SOT-23 Package (Most 1-16 Kbit Devices)
- 8-lead 2x3mm and 5x6mm DFN Packages Available
- Pb-Free and RoHS Compliant
- Available for Extended Temperature Ranges:
  - Industrial (I): -40°C to +85°C
  - Automotive (E): -40°C to +125°C

Description:

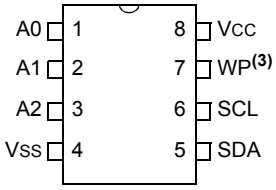
The Microchip Technology Inc. 24CXX, 24LCXX, 24AAXX and 24FCXX (24XX*) devices are a family of 128-bit through 1024 Kbit Electrically Erased PROMs. The devices are organized in blocks of x8-bit memory with 2-wire serial interfaces. Low-voltage design permits operation down to 1.7V (for 24AAXX devices), with standby and active currents of only 1 μA and 1 mA, respectively. Devices 1 Kbit and larger have page write capability. Parts having functional address lines allow connection of up to 8 devices on the same bus. The 24XX family is available in the standard 8-pin PDIP, surface mount SOIC, TSSOP and MSOP packages. Most 128-bit through 16 Kbit devices are also available in the 5-lead SOT-23 package. DFN packages (2x3mm or 5x6mm) are also available. All packages are Pb-free (Matte Tin) finish.

Note: This document is an overview. For detailed specifications, please consult the individual product data sheet, available at www.microchip.com.

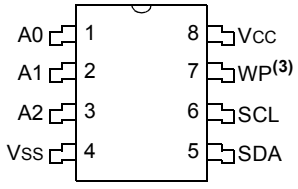
*24XX is used in this document as a generic part number for 24 series devices in this data sheet. 24XX64, for example, represents all voltages of the 64 Kbit device.

Package Types(1)

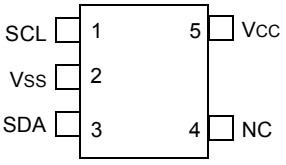
PDIP/SOIC



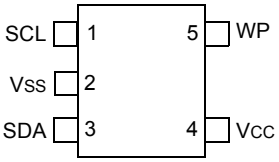
TSSOP/MSOP(2)



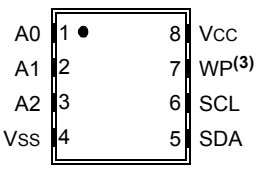
SOT-23-5 (24XX00)



SOT-23-5 (all except 24XX00)



DFN



Note 1: Pins A0, A1, A2 and WP are not used by some devices (no internal connections). See Table 1-1, Device Selection Table, for details.

2: Pins A0 and A1 are no-connects for the 24XX128 and 24XX256 MSOP devices.

3: Pin 7 is "not used" for 24XX00, 24XX025 and 24C01C.

3 Family Data Sheets

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TABLE 1-1: DEVICE SELECTION TABLE

Part Number	Vcc Range	Max. Clock Frequency	Page Size	Write-Protect Array	Functional Address Pins	Temp. Range	Packages[5]
128-bit devices							
24AA00	1.7-5.5V	400 kHz[1]	—	None	None	I	P, SN, ST, OT, MC
24LC00	2.5-5.5V	400 kHz[1]				I	
24C00	4.5-5.5V	400 kHz				I, E	
1 Kb devices							
24AA01	1.7-5.5V	400 kHz [2]	8 bytes	Entire Array	None	I	P, SN, ST, MS, OT, MC
24LC01B	2.5-5.5V	400 kHz				I, E	
24AA014	1.7-5.5V	400 kHz[2]	16 bytes	Entire Array	A0, A1, A2	I	P, SN, ST, MS, MC
24LC014	2.5-5.5V	400 kHz				I	
24AA01H[6]	1.7-5.5v	400 kHz[1]	16 bytes	Upper Half	A0, A1, A2	I	P, SN, ST, MS, OT, MC
24LC01H[6]	2.5-5.5v	400 kHz[1]	16 bytes	Upper Half	A0, A1, A2	I, E	P, SN, ST, MS, OT, MC
24C01C	4.5V-5.5V	400 kHz	16 bytes	None	A0, A1, A2	I, E	P, SN, ST, MC
2 Kb devices							
24AA02	1.7-5.5V	400 kHz [2]	8 bytes	Entire Array	None	I	P, SN, ST, MS, OT, MC
24LC02B	2.5-5.5V	400 kHz				I, E	
24AA024	1.7-5.5V	400 kHz[2]	16 bytes	Entire Array	A0, A1, A2	I	P, SN, ST, MS, MC
24LC024	2.5-5.5V	400 kHz				I	
24AA025	1.7-5.5V	400 kHz[2]	16 bytes	None	A0, A1, A2	I	P, SN, ST,MS, MC
24LC025	2.5-5.5V	400 kHz				I	
24AA02H[6]	1.7-5.5v	400 kHz[1]	16 bytes	Upper Half	A0, A1, A2	I	P, SN, ST, MS, OT, MC
24LC02H[6]	2.5-5.5v	400 kHz[1]	16 bytes	Upper Half	A0, A1, A2	I, E	P, SN, ST, MS, OT, MC
24C02C	4.5-5.5V	400 kHz	16 bytes	Upper Half of Array	A0, A1, A2	I, E	P, SN, ST, MC
4 Kb devices							
24AA04	1.7-5.5V	400 kHz [2]	16 bytes	Entire Array	None	I	P, SN, ST, MS, OT, MC
24LC04B	2.5-5.5V	400 kHz				I, E	
8 Kb devices							
24AA08	1.7-5.5V	400 kHz [2]	16 bytes	Entire Array	None	I	P, SN, ST, MS, OT, MC
24LC08B	2.5-5.5V	400 kHz				I, E	
16 Kb devices							
24AA16	1.7-5.5V	400 kHz [2]	16 bytes	Entire Array	None	I	P, SN, ST, MS, OT, MC
24LC16B	2.5-5.5V	400 kHz				I, E	
32 Kb devices							
24AA32A	1.7-5.5V	400 kHz [2]	32 bytes	Entire Array	A0, A1, A2	I	P, SN, SM, ST, MS, MC
24LC32A	2.5-5.5V	400 kHz				I, E	

Note 1: 100 kHz for Vcc <4.5V.

2: 100 kHz for Vcc <2.5V.

3: 400 kHz for Vcc <2.5V.

4: Pins A0 and A1 are no-connects for the 24XX128 and 24XX256 in the MSOP package.

5: P = 8-PDIP, SN = 8-SOIC (3.90 mm JEDEC), ST = 8-TSSOP, OT = 5 or 6-SOT23, MC = 2x3mm DFN, MS = 8-MSOP, SM = 8-SOIC (200 mil EIAJ), MF = 5x6mm DFN.

6: Available Q4 2007.

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TABLE 1-1: DEVICE SELECTION TABLE (CONTINUED)

Part Number	Vcc Range	Max. Clock Frequency	Page Size	Write-Protect Array	Functional Address Pins	Temp. Range	Packages(5)
64 Kb devices							
24AA64	1.7-5.5V	400 kHz (2)	32 bytes	Entire Array	A0, A1, A2	I	P, SN, SM, ST, MS, MC
24LC64	2.5-5.5V	400 kHz				I, E	
24FC64	1.7-5.5V	1 MHz(3)				I	
128 Kb devices							
24AA128	1.7-5.5V	400 kHz (2)	64 bytes	Entire Array	A0, A1, A2(4)	I	P, SN, SM, ST, MS, MF
24LC128	2.5-5.5V	400 kHz				I, E	
24FC128	1.7-5.5V	1 MHz(3)				I	
256 Kb devices							
24AA256	1.7-5.5V	400 kHz (2)	64 bytes	Entire Array	A0, A1, A2(4)	I	P, SN, SM, ST, MS, MF
24LC256	2.5-5.5V	400 kHz				I, E	
24FC256	1.7-5.5V	1 MHz(3)				I	
512 Kb devices							
24AA512	1.7-5.5V	400 kHz (2)	128 bytes	Entire Array	A0, A1, A2	I	P, SM, MF,
24LC512	2.5-5.5V	400 kHz				I, E	
24FC512	1.7-5.5V(3)	1 MHz				I	
1024 Kb devices							
24AA1025	1.7-5.5V	400 kHz (2)	128 bytes	Entire Array	A0, A1	I	P, SM
24LC1025	2.5-5.5V	400 kHz				I, E	
24FC1025	1.7-5.5V(3)	1 MHz				I	

Note 1: 100 kHz for Vcc <4.5V.

2: 100 kHz for Vcc <2.5V.

3: 400 kHz for Vcc <2.5V.

4: Pins A0 and A1 are no-connects for the 24XX128 and 24XX256 in the MSOP package.

5: P = 8-PDIP, SN = 8-SOIC (3.90 mm JEDEC), ST = 8-TSSOP, OT = 5 or 6-SOT23, MC = 2x3mm DFN, MS = 8-MSOP, SM = 8-SOIC (200 mil EIAJ), MF = 5x6mm DFN.

6: Available Q4 2007.

2.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (†)

VCC.....6.5V

All inputs and outputs w.r.t. VSS ..... -0.6V to VCC +1.0V

Storage temperature .....-65°C to +150°C

Ambient temperature with power applied .....-40°C to +125°C

ESD protection on all pins .....≥ 4 kV

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 2-1: DC CHARACTERISTICS

DC CHARACTERISTICS			**Electrical Characteristics:** Industrial (I): VCC = +1.7V to 5.5V TA = -40°C to +85°C Automotive (E): VCC = +2.5V to 5.5V TA = -40°C to 125°C			
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
D1	—	A0, A1, A2, SCL, SDA and WP pins:	—	—	—	—
D2	VIH	High-level input voltage	0.7 VCC	—	V	—
D3	VIL	Low-level input voltage	—	0.3 VCC 0.2 VCC	V V	VCC ≥ 2.5V VCC < 2.5V
D4	VHYS	Hysteresis of Schmitt Trigger inputs (SDA, SCL pins)	0.05 VCC	—	V	**(Note 1)**
D5	VOL	Low-level output voltage	—	0.40	V	IOL = 3.0 mA @ VCC = 2.5V
D6	ILI	Input leakage current	—	±1	µA	VIN = VSS or VCC
D7	ILO	Output leakage current	—	±1	µA	VOUT = VSS or VCC
D8	CIN, COUT	Pin capacitance (all inputs/outputs)	—	10	pF	VCC = 5.0V **(Note 1)** TA = 25°C, FCLK = 1 MHz
D9	ICC Read	Operating current	—	500 400 1	µA µA mA	24XX1025 24XX128, 256, 512: All except 24XX128, 256, 512, 1025: (VCC = 5.5V, SCL = 400 kHz)
	ICC Write		—	3 5	mA mA	All except 24XX512 and 24XX1025 24XX512 and 24XX1025 (VCC = 5.5V)
D10	ICCS	Standby current	— — — —	1 5 50 5	µA µA µA µA	All except 24XX1025 24XX1025 24C01C and 24C02C only (TA = -40°C to +85°C) All except 24XX1025 (TA = -40°C to +125°C) SCL = SDA = VCC = 5.5V A0, A1, A2, WP = VSS or VCC

Note 1: This parameter is periodically sampled and not 100% tested.

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TABLE 2-2: AC CHARACTERISTICS – ALL EXCEPT 24XX00, 24C01C AND 24C02C

AC CHARACTERISTICS			Electrical Characteristics: Industrial (I): VCC = +1.7V to 5.5V TA = -40°C to +85°C Automotive (E): VCC = +2.5V to 5.5V TA = -40°C to 125°C			
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
1	FCLK	Clock frequency	— — — —	100 400 400 1000	kHz	1.7V ≤ VCC < 2.5V 2.5V ≤ VCC ≤ 5.5V 1.7V ≤ VCC < 2.5V 24FCXXX 2.5V ≤ VCC ≤ 5.5V 24FCXXX
2	THIGH	Clock high time	4000 600 600 500	— — — —	ns	1.7V ≤ VCC < 2.5V 2.5V ≤ VCC ≤ 5.5V 1.7V ≤ VCC < 2.5V 24FCXXX 2.5V ≤ VCC ≤ 5.5V 24FCXXX
3	TLOW	Clock low time	4700 1300 1300 500	— — — —	ns	1.7V ≤ VCC < 2.5V 2.5V ≤ VCC ≤ 5.5V 1.7V ≤ VCC < 2.5V 24FCXXX 2.5V ≤ VCC ≤ 5.5V 24FCXXX
4	TR	SDA and SCL rise time **(Note 1)**	— — —	1000 300 300	ns	1.7V ≤ VCC < 2.5V 2.5V ≤ VCC ≤ 5.5V 1.7V ≤ VCC ≤ 5.5V 24FCXXX
5	TF	SDA and SCL fall time **(Note 1)**	— —	300 100	ns	All except 24FCXXX 1.7V ≤ VCC ≤ 5.5V 24FCXXX
6	THD:STA	Start condition hold time	4000 600 600 250	— — — —	ns	1.7V ≤ VCC < 2.5V 2.5V ≤ VCC ≤ 5.5V 1.7V ≤ VCC < 2.5V 24FCXXX 2.5V ≤ VCC ≤ 5.5V 24FCXXX
7	TSU:STA	Start condition setup time	4700 600 600 250	— — — —	ns	1.7V ≤ VCC < 2.5V 2.5V ≤ VCC ≤ 5.5V 1.7V ≤ VCC < 2.5V 24FCXXX 2.5V ≤ VCC ≤ 5.5V 24FCXXX
8	THD:DAT	Data input hold time	0	—	ns	**(Note 2)**
9	TSU:DAT	Data input setup time	250 100 100	— — —	ns	1.7V ≤ VCC < 2.5V 2.5V ≤ VCC ≤ 5.5V 1.7V ≤ VCC ≤ 5.5V 24FCXXX
10	TSU:STO	Stop condition setup time	4000 600 600 250	— — — —	ns	1.7 V ≤ VCC < 2.5V 2.5 V ≤ VCC ≤ 5.5V 1.7V ≤ VCC < 2.5V 24FCXXX 2.5 V ≤ VCC ≤ 5.5V 24FCXXX
11	TSU:WP	WP setup time (32K and above only)	4000 600 600	— — —	ns	1.7V ≤ VCC < 2.5V 2.5V ≤ VCC ≤ 5.5V 1.7V ≤ VCC ≤ 5.5V 24FCXXX
12	THD:WP	WP hold time (32K and above only)	4700 1300 1300	— — —	ns	1.7V ≤ VCC < 2.5V 2.5V ≤ VCC ≤ 5.5V 1.7V ≤ VCC ≤ 5.5V 24FCXXX

Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

3: This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model, which can be obtained from Microchip's web site: www.microchip.com.

4: 24FCXXX denotes the 24FC64, 24FC128, 24FC256, 24FC512 and 24FC1025 devices.

TABLE 2-2: AC CHARACTERISTICS – ALL EXCEPT 24XX00, 24C01C AND 24C02C (CONTINUED)

AC CHARACTERISTICS			Electrical Characteristics: Industrial (I): V_{CC} = +1.7V to 5.5V T_A = -40°C to +85°C Automotive (E): V_{CC} = +2.5V to 5.5V T_A = -40°C to 125°C			
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
13	T_{AA}	Output valid from clock **(Note 2)**	— — — —	3500 900 900 400	ns	1.7V ≤ V_{CC} < 2.5V 2.5V ≤ V_{CC} ≤ 5.5V 1.7V ≤ V_{CC} < 2.5V 24FCXXX 2.5V ≤ V_{CC} ≤ 5.5V 24FCXXX
14	T_{BUF}	Bus free time: Time the bus must be free before a new transmission can start	4700 1300 1300 500	— — — —	ns	1.7V ≤ V_{CC} < 2.5V 2.5V ≤ V_{CC} ≤ 5.5V 1.7V ≤ V_{CC} < 2.5V 24FCXXX 2.5V ≤ V_{CC} ≤ 5.5V 24FCXXX
15	T_{OF}	Output fall time from V_{IH} minimum to V_{IL} maximum C_B ≤ 100 pF	10 + 0.1C_B	250 250	ns	All except 24FCXXX **(Note 1)** 24FCXXX **(Note 1)**
16	T_{SP}	Input filter spike suppression (SDA and SCL pins)	—	50	ns	All except 24FCXXX **(Note 1)**
17	T_{WC}	Write cycle time (byte or page)	—	5	ms	
18	—	Endurance	1,000,000	—	cycles	25°C **(Note 3)**

Note 1: Not 100% tested. C_B = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

3: This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model, which can be obtained from Microchip's web site: www.microchip.com.

4: 24FCXXX denotes the 24FC64, 24FC128, 24FC256, 24FC512 and 24FC1025 devices.

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TABLE 2-3: AC CHARACTERISTICS – 24XX00, 24C01C AND 24C02C

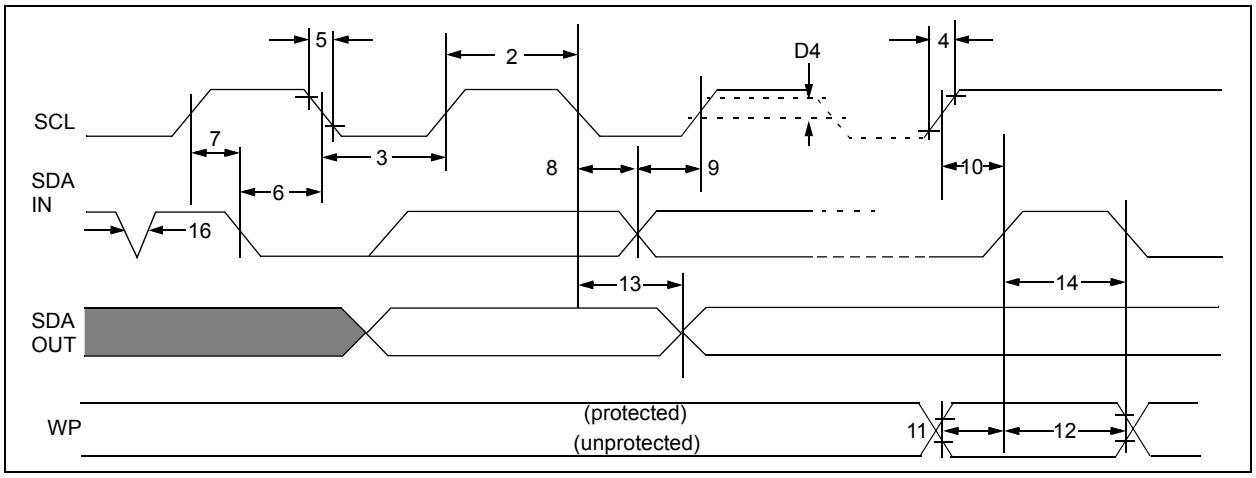
All Parameters apply across all recommended operating ranges unless otherwise noted	Industrial (I): T_A = -40°C to +85°C, V_{CC} = 1.7V to 5.5V Automotive (E): T_A = -40°C to +125°C, V_{CC} = 4.5V to 5.5V				
Parameter	**Symbol**	**Min.**	**Max.**	**Units**	**Conditions**
Clock frequency	F_{CLK}	— — —	100 100 400	kHz	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.7V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 5.5V
Clock high time	T_{HIGH}	4000 4000 600	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.7V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 5.5V
Clock low time	T_{LOW}	4700 4700 1300	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.7V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 5.5V
SDA and SCL rise time **(Note 1)**	T_R	— — —	1000 1000 300	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.7V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 5.5V
SDA and SCL fall time	T_F	—	300	ns	**(Note 1)**
Start condition hold time	$T_{HD:STA}$	4000 4000 600	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.7V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 5.5V
Start condition setup time	$T_{SU:STA}$	4700 4700 600	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.7V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 5.5V
Data input hold time	$T_{HD:DAT}$	0	—	ns	**(Note 2)**
Data input setup time	$T_{SU:DAT}$	250 250 100	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.7V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 5.5V
Stop condition setup time	$T_{SU:STO}$	4000 4000 600	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.7V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 5.5V
Output valid from clock **(Note 2)**	T_{AA}	— — —	3500 3500 900	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.7V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 5.5V
Bus free time: Time the bus must be free before a new transmission can start	T_{BUF}	4700 4700 1300	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.7V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 5.5V
Output fall time from V_{IH} minimum to V_{IL} maximum	T_{OF}	20+0.1 CB	250	ns	**(Note 1)**, CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	T_{SP}	—	50	ns	**(Note 1)**
Write cycle time	T_{WC}	—	4 1.5	ms	24XX00 24C01C, 24C02C
Endurance		1,000,000	—	cycles	**(Note 3)**

Note 1: Not 100% tested. C_B = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

3: This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be obtained from Microchip's web site: www.microchip.com.

FIGURE 2-1: EXAMPLE BUS TIMING DATA



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3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Name	8-Pin PDIP and SOIC	8-Pin TSSOP and MSOP	5-Pin SOT-23 24XX00	5-Pin SOT-23 All except 24XX00	8-Pin 5x6 DFN and 2x3 DFN	Function
A0	1	1(1)	—	—	1	User configurable Chip Select(3)(4)
A1	2	2(1)	—	—	2	User configurable Chip Select(3)(4)
A2	3	3	—	—	3	User configurable Chip Select(3)(4)
VSS	4	4	2	2	4	Ground
SDA	5	5	3	3	5	Serial Data
SCL	6	6	1	1	6	Serial Clock
(NC)	—	—	4	—	—	Not Connected
WP	7(2)	7(2)	—	5	7	Write-Protect Input
VCC	8	8	5	4	8	Power Supply

Note 1: Pins 1 and 2 are not connected for the 24XX128 and 24XX256 MSOP packages.
2: Pin 7 is not used for 24XX00, 24XX025 and 24C01C.
3: Pins A0, A1 and A2 are not used by some devices (no internal connections). See Table 1-1 for details.
4: Pin A2 should be tied to a Logic High in the 24XX1025 for proper operation.

3.1 A0, A1, A2 Chip Address Inputs

The A0, A1 and A2 pins are not used by the 24XX01 through 24XX16 devices.

The A0, A1 and A2 inputs are used by the 24C01C, 24C02C, 24XX014, 24XX024, 24XX025 and the 24XX32 through 24XX1025 for multiple device operations. The levels on these inputs are compared with the corresponding bits in the slave address. The chip is selected if the compare is true.

For the 24XX128 and 24XX256 in the MSOP package only, pins A0 and A1 are not connected.

Up to eight devices (two for the 24XX128 and 24XX256 MSOP package) may be connected to the same bus by using different Chip Select bit combinations.

In most applications, the chip address inputs A0, A1 and A2 are hard-wired to logic '0' or logic '1'. For applications in which these pins are controlled by a microcontroller or other programmable device, the chip address pins must be driven to logic '0' or logic '1' before normal device operation can proceed.

Note:	In the 24XX1025, the A2 pin is not configurable, it must be tied to VCC in order for this device to operate properly.

3.2 Serial Data (SDA)

This is a bidirectional pin used to transfer addresses and data into and out of the device. It is an open drain terminal. Therefore, the SDA bus requires a pull-up resistor to VCC (typical 10 kΩ for 100 kHz, 2 kΩ for 400 kHz and 1 MHz).

For normal data transfer, SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the Start and Stop conditions.

3.3 Serial Clock (SCL)

This input is used to synchronize the data transfer to and from the device.

3.4 Write-Protect (WP)

This pin must be connected to either VSS or VCC. If tied to VSS, write operations are enabled. If tied to VCC, write operations are inhibited but read operations are not affected. See Table 1-1 for the write-protect scheme of each device.

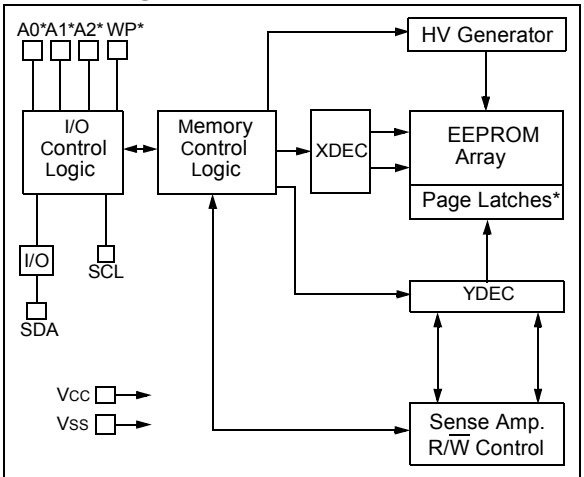
3.5 Power Supply (VCC)

A VCC threshold detect circuit is employed which disables the internal erase/write logic if VCC is below 1.5V at nominal conditions. For the 24C00, 24C01C and 24C02C devices, the erase/write logic is disabled below 3.8V at nominal conditions.

4.0 FUNCTIONAL DESCRIPTION

Each 24XX device supports a bidirectional, 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter, while a device receiving data is defined as a receiver. The bus has to be controlled by a master device which generates the Serial Clock (SCL), controls the bus access and generates the Start and Stop conditions, while the 24XX works as slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated.

Block Diagram



* A0, A1, A2, WP and page latches are not used by some devices.

See Table 1-1, Device Selection Table, for details.

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5.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as a Start or Stop condition.

Accordingly, the following bus conditions have been defined (Figure 5-1).

5.1 Bus Not Busy (A)

Both data and clock lines remain high.

5.2 Start Data Transfer (B)

A high-to-low transition of the SDA line while the clock (SCL) is high determines a Start condition. All commands must be preceded by a Start condition.

5.3 Stop Data Transfer (C)

A low-to-high transition of the SDA line while the clock (SCL) is high determines a Stop condition. All operations must be ended with a Stop condition.

5.4 Data Valid (D)

The state of the data line represents valid data when, after a Start condition, the data line is stable for the duration of the high period of the clock signal.

The data on the line must be changed during the low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a Start condition and terminated with a Stop condition. The number of data bytes transferred between Start and Stop conditions is determined by the master device.

5.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this Acknowledge bit.

Note:	During a write cycle, the 24XX will not acknowledge commands.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end-of-data to the slave by not generating an Acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24XX) will leave the data line high to enable the master to generate the Stop condition (Figure 5-2).

FIGURE 5-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS

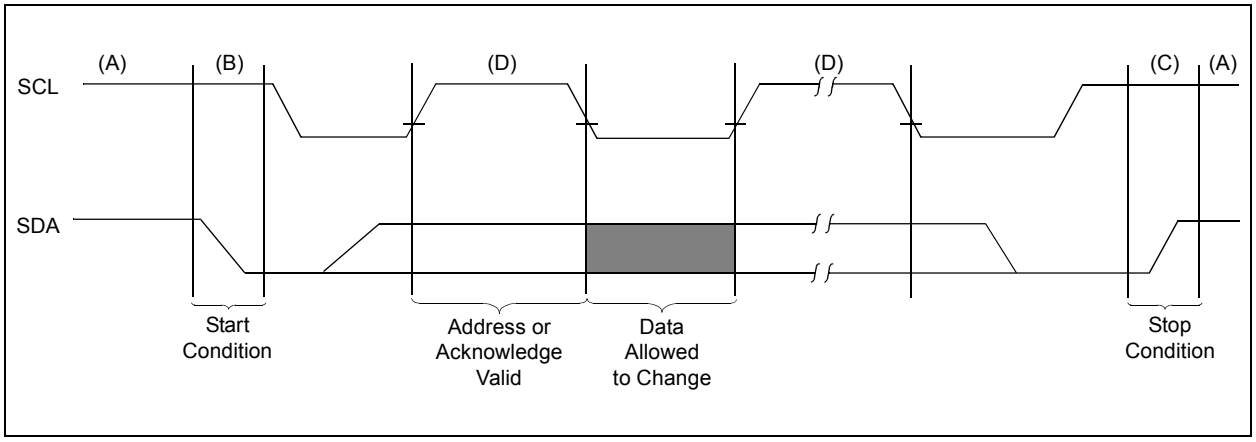
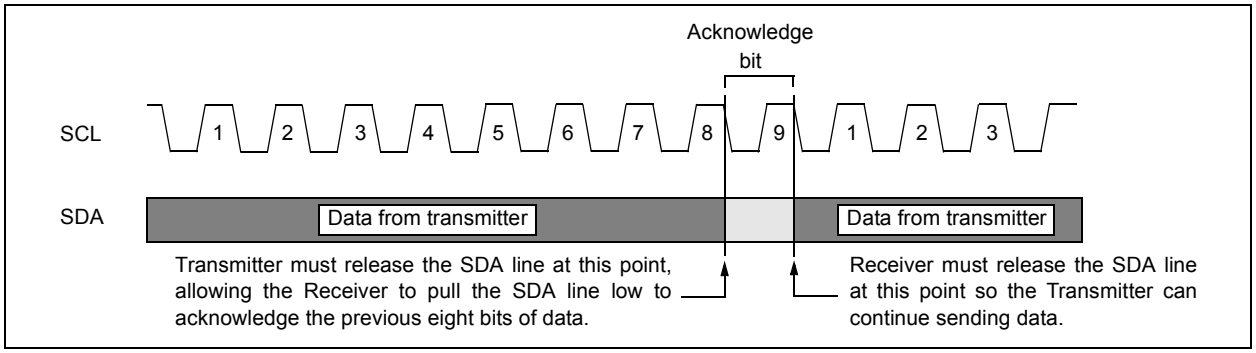


FIGURE 5-2: ACKNOWLEDGE TIMING



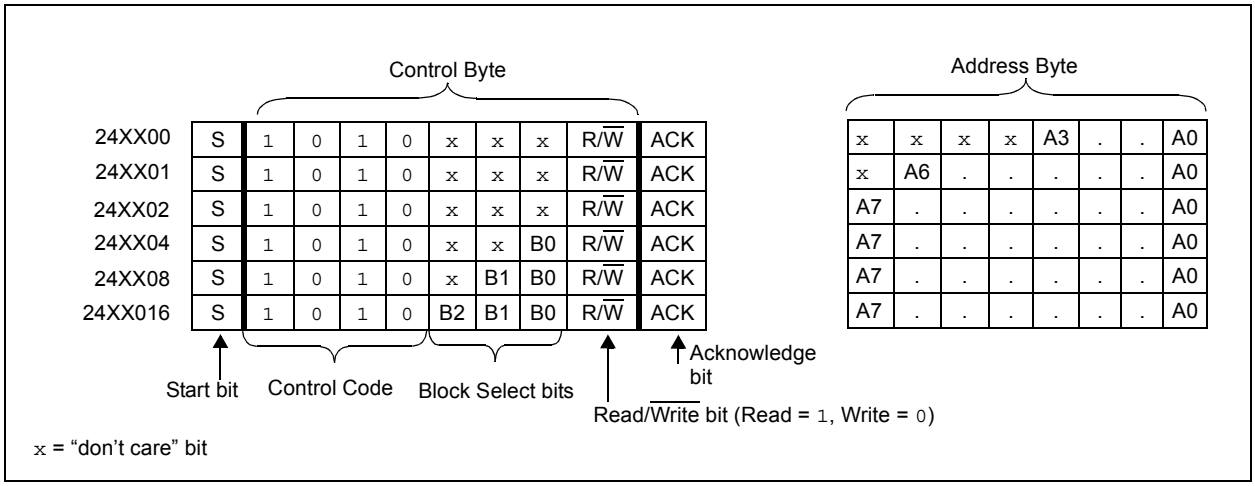
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5.6 Device Addressing For Devices Without Functional Address Pins

A control byte is the first byte received following the Start condition from the master device (Figure 5-3). The control byte begins with a four-bit control code. For the 24XX, this is set as '1010' binary for read and write operations. The next three bits of the control byte are the block-select bits (B2, B1, B0). They are used by the master device to select which of the 256-word blocks of memory are to be accessed. These bits are in effect the three Most Significant bits of the word address. Note that B2, B1 and B0 are "don't care" for the 24XX00, the 24XX01 and 24XX02. B2 and B1 are "don't care" for the 24XX04. B2 is "don't care" for the 24XX08.

The last bit of the control byte defines the operation to be performed. When set to '1', a read operation is selected. When set to '0' a write operation is selected. Following the Start condition, the 24XX monitors the SDA bus. Upon receiving a '1010' code, the block select bits and the R/$\overline{W}$ bit, the slave device outputs an Acknowledge signal on the SDA line. The address byte follows the acknowledge.

FIGURE 5-3: CONTROL AND ADDRESS BYTE ASSIGNMENTS FOR DEVICES WITHOUT ADDRESS PINS



5.7 Device Addressing For Devices With Functional Address Pins

A control byte is the first byte received following the Start condition from the master device (Figure 5-4). The control byte begins with a 4-bit control code. For the 24XX, this is set as '1010' binary for read and write operations. The next three bits of the control byte are the Chip Select bits (A2, A1, A0). The Chip Select bits allow the use of up to eight 24XX devices on the same bus and are used to select which device is accessed. The Chip Select bits in the control byte must correspond to the logic levels on the corresponding A2, A1 and A0 pins for the device to respond. These bits are, in effect, the three Most Significant bits of the word address.

For 24XX128 and 24XX256 in the MSOP package, the A0 and A1 pins are not connected. During device addressing, the A0 and A1 Chip Select bits (Figure 5-4) should be set to '0'. Only two 24XX128 or 24XX256 MSOP packages can be connected to the same bus.

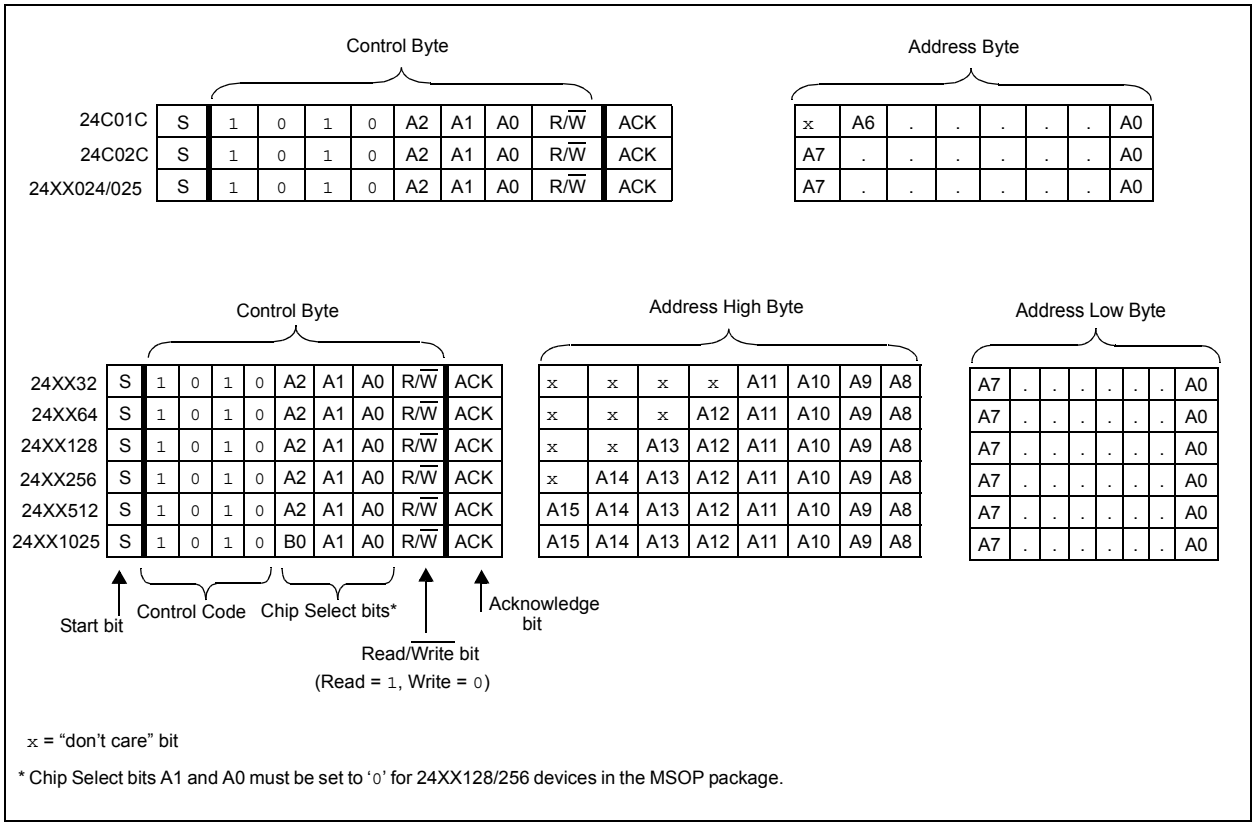
The last bit of the control byte defines the operation to be performed. When set to a '1', a read operation is selected. When set to a '0', a write operation is selected.

For higher density devices (24XX32 through 24XX1025), the next two bytes received define the address of the first data byte. Depending on the product density, not all bits in the address high byte are used. A15, A14, A13 and A12 are "don't care" for 24XX32. A15, A14 and A13 are "don't care" for 24XX64. A15 and A14 are "don't care" for 24XX128. A15 is "don't care" for 24XX256. All address bits are used for the 24XX512 and 24XX1025. The upper address bits are transferred first, followed by the Less Significant bits.

Following the Start condition, the 24XX monitors the SDA bus. Upon receiving a '1010' code, appropriate device select bits and the R/$\overline{W}$ bit, the slave device outputs an Acknowledge signal on the SDA line. The address byte(s) follow the acknowledge.

The 24XX1025 has an internal address boundary limitation that is divided into two segments of 512 Kbits. Block select bit 'B0' is used to control access to each segment. Contiguous writes cannot be performed across this boundary.

FIGURE 5-4: CONTROL AND ADDRESS BYTE ASSIGNMENTS FOR DEVICES WITH ADDRESS PINS



x = "don't care" bit

* Chip Select bits A1 and A0 must be set to '0' for 24XX128/256 devices in the MSOP package.

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5.7.1 CONTIGUOUS ADDRESSING ACROSS MULTIPLE DEVICES

Chip Select bits A2, A1 and A0 can be used to expand the contiguous address space by adding up to eight 24XXs on the same bus. Software can use the three address bits of the control byte as the three Most Significant bits of the address byte. For example, in the 24XX32 devices, software can use A0 of the **control byte** as address bit A12; A1 as address bit A13; and A2 as address bit A14 (Table 5-1). It is not possible to sequentially read across device boundaries.

TABLE 5-1: CONTROL BYTE ADDRESS BITS

	Maximum Devices	Maximum Contiguous Address Space	Chip Select Bit A2	Chip Select Bit A1	Chip Select Bit A0
1K (24C01C)	8	8 Kb	A10	A9	A8
1K (24XX014)	8	8 Kb	A10	A9	A8
2K (24C02C)	8	16 Kb	A10	A9	A8
2K (24XX024/025)	8	16 Kb	A10	A9	A8
32K (24XX32)	8	256 Kb	A14	A13	A12
64K (24XX64)	8	512 Kb	A15	A14	A13
128K (24XX128)	8(1)	1 Mb	A16*	A15*	A14
256K (24XX256)	8(1)	2 Mb	A17*	A16*	A15
512K (24XX512)	8	4 Mb	A18	A17	A16
1024K (24XX1025)	4(2)	4 Mb	B0(3)	A17	A16

Note 1: Up to two 24XX128 or 24XX256 devices in the MSOP package can be added for up to 256 kb or 512 kb of address space, respectively. Bits A0 and A1 must be set to '0'.

2: Using the block select bit 'B0', up to four 24XX1025 devices can be cascaded together.

3: For proper operation of the 24XX1025 the A2 pin must be tied to a logic high. Software addressing uses B0 to select between upper and lower 512 Kbit segments of memory.

6.0 WRITE OPERATIONS

6.1 Byte Write

A byte write operation begins with a Start condition from the master followed by the four-bit control code (see Figure 6-1 and Figure 6-2). The next 3 bits are either the Block Address bits (for devices without address pins) or the Chip Select bits (for devices with address pins). Then the master transmitter clocks the R/$\overline{W}$ bit (which is a logic low) onto the bus. The slave then generates an Acknowledge bit during the ninth clock cycle.

The next byte transmitted by the master is the address byte (for 128-bit to 16 Kbit devices) or the high-order address byte (for 32-1024 Kbit devices). For 32 through 1024 Kbit devices, the high-order address byte is followed by the low-order address byte. In either case, each address byte is acknowledged by the 24XX and the address bits are latched into the internal address counter of the 24XX.

For the 24XX00 devices, only the lower four address bits are used by the device. The upper four bits are “don’t cares.”

After receiving the ACK from the 24XX acknowledging the final address byte, the master device transmits the data word to be written into the addressed memory location. The 24XX acknowledges again and the master generates a Stop condition, which initiates the internal write cycle.

If an attempt is made to write to an array with the WP pin held high, the device will acknowledge the command, but no write cycle will occur, no data will be written, and the device will immediately accept a new command. After a byte Write command, the internal address counter will increment to the next address location. During a write cycle, the 24XX will not acknowledge commands.

FIGURE 6-1: BYTE WRITE: 128-BIT TO 16 KBIT DEVICES

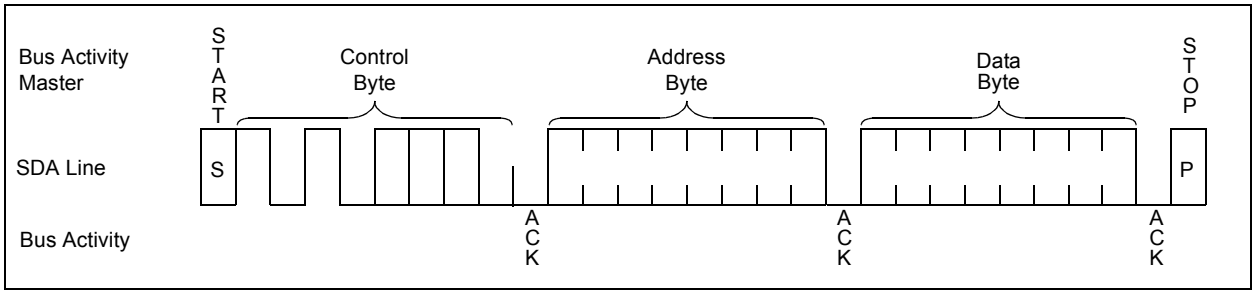
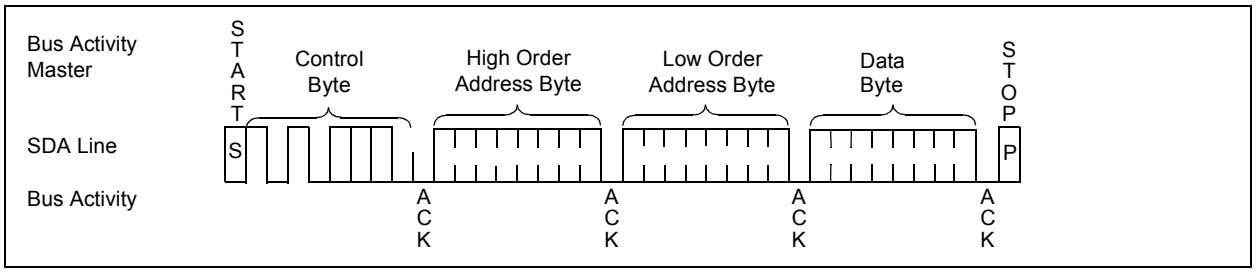


FIGURE 6-2: BYTE WRITE: 32 TO 1024 KBIT DEVICES



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6.2 Page Write

The write control byte, word address byte(s), and the first data byte are transmitted to the 24XX in much the same way as in a byte write (see Figure 6-3 and Figure 6-4). The exception is that instead of generating a Stop condition, the master transmits up to one page of bytes[(1)], which is temporarily stored in the on-chip page buffer. This data is then written into memory once the master has transmitted a Stop condition. Upon receipt of each word, the internal address counter is incremented by one. If the master should transmit more than one page of data prior to generating the Stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the Stop condition is received, an internal write cycle begins. During the write cycle, the 24XX will not acknowledge commands.

Page writes can be any number of bytes within a page (up to the page size), starting at any address. Only the data bytes being addressed will be changed within the page.

If an attempt is made to write to the array with the WP pin held high, the device will acknowledge the command, but no write cycle will occur, no data will be written and the device will immediately accept a new command.

Note 1:	See Device Selection Table 1-1 for the page size of each device.

6.3 Write-Protection

The WP pin allows the user to write-protect the array when the pin is tied to VCC. See Device Selection Table 1-1 for the write-protect scheme of each device. If tied to VSS, the write protection is disabled. Please refer to the product data sheet for complete details.

Note:	Page write operations are limited to writing bytes within a single physical page, **regardless** of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or 'page size') and end at addresses that are integer multiples of [page size – 1]. If a Page Write command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page, as might be expected. It is therefore necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

FIGURE 6-3: PAGE WRITE: 1 KB TO 16 KBIT DEVICES

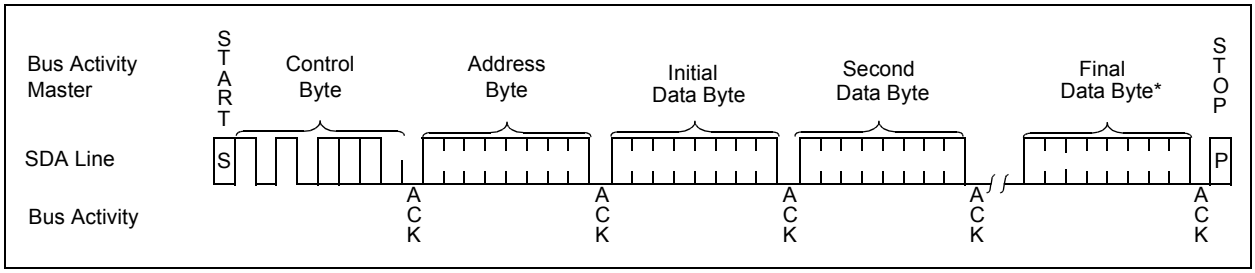
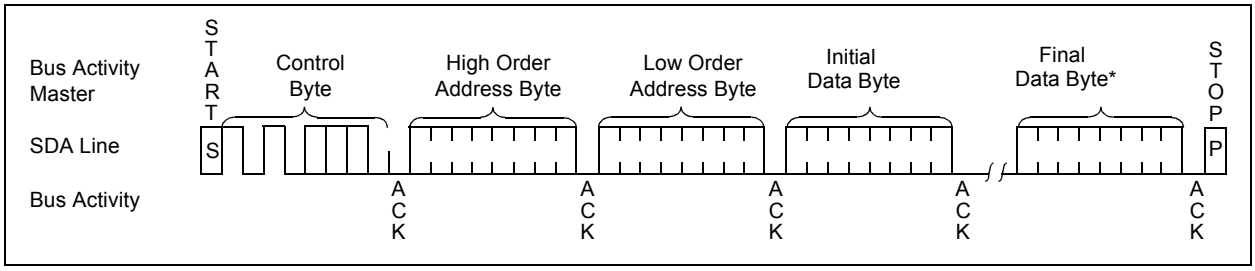


FIGURE 6-4: PAGE WRITE: 32 TO 1024 KBIT DEVICES

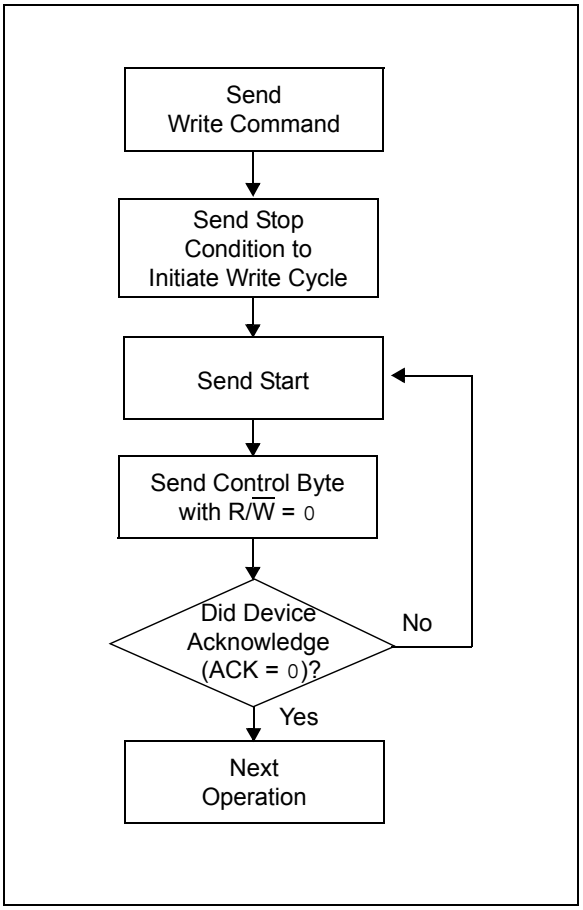


* See Table 1-1 for maximum number of data bytes in a page.

7.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge commands during a write cycle, this can be used to determine when the cycle is complete (This feature can be used to maximize bus throughput). Once the Stop condition for a Write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a Start condition, followed by the control byte for a Write command ($R/\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If no ACK is returned, the Start bit and control byte must be re-sent. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next Read or Write command. See Figure 7-1 for flow diagram.

FIGURE 7-1: ACKNOWLEDGE POLLING FLOW



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8.0 READ OPERATION

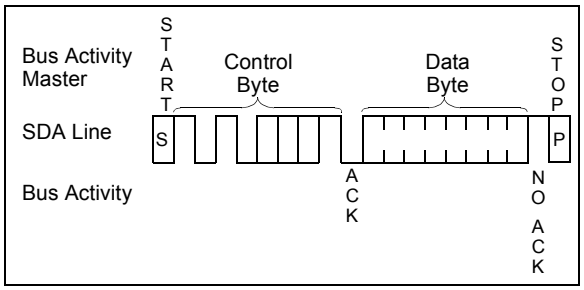
Read operations are initiated in much the same way as write operations with the exception that the R/$\overline{W}$ bit of the control byte is set to '1'. There are three basic types of read operations: current address read, random read and sequential read.

8.1 Current Address Read

The 24XX contains an address counter that maintains the address of the last byte accessed, internally incremented by '1'. Therefore, if the previous read or write operation was to address 'n' (n is any legal address), the next current address read operation would access data from address n + 1.

Upon receipt of the control byte with R/$\overline{W}$ bit set to '1', the 24XX issues an acknowledge and transmits the 8-bit data byte. The master will not acknowledge the transfer, but does generate a Stop condition and the 24XX discontinues transmission (Figure 8-1).

FIGURE 8-1: CURRENT ADDRESS READ



8.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, the byte address must first be set. This is done by sending the byte address to the 24XX as part of a write operation (R/$\overline{W}$ bit set to '0'). Once the byte address is sent, the master generates a Start condition following the acknowledge. This terminates the write operation, but not before the internal address counter is set. The master then issues the control byte again, but with the R/$\overline{W}$ bit set to a '1'. The 24XX will then issue an acknowledge and transmit the 8-bit data byte. The master will not acknowledge the transfer but does generate a Stop condition, which causes the 24XX to discontinue transmission (Figure 8-2 and Figure 8-3). After a random Read command, the internal address counter will increment to the next address location.

FIGURE 8-2: RANDOM READ: 128-BIT TO 16 KBIT DEVICES

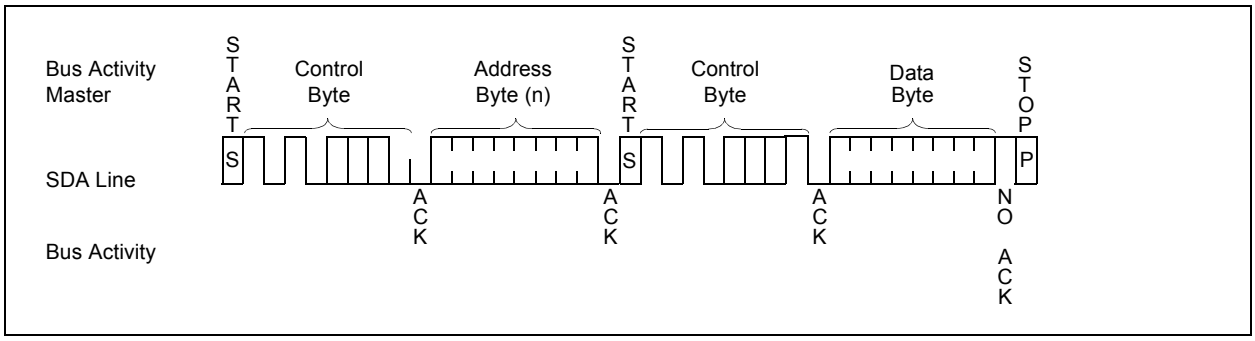
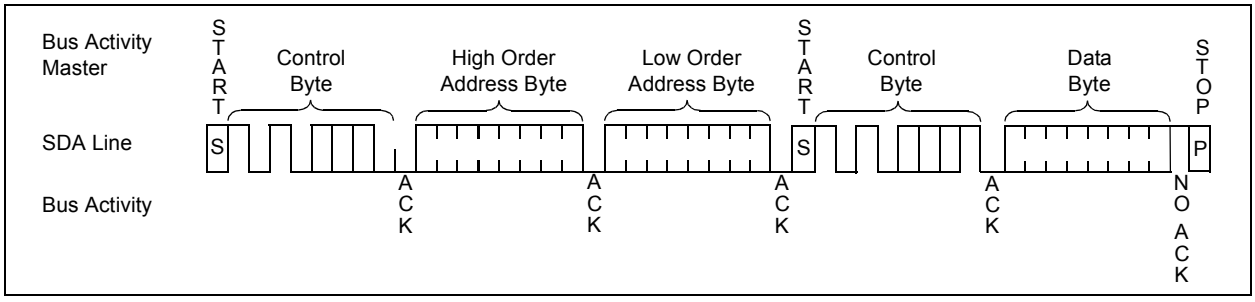


FIGURE 8-3: RANDOM READ: 32 TO 1024 KBIT DEVICES

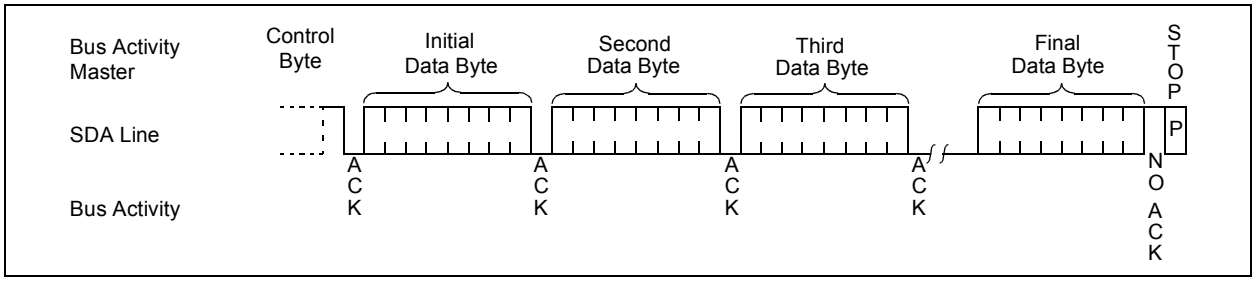


3 Family Data Sheets

8.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24XX transmits the first data byte, the master issues an acknowledge as opposed to the Stop condition used in a random read. This acknowledge directs the 24XX to transmit the next sequentially addressed data byte (Figure 8-4). Following the final byte transmitted to the master, the master will NOT generate an acknowledge but will generate a Stop condition. To provide sequential reads, the 24XX contains an internal Address Pointer which is incremented by one at the completion of each operation. This Address Pointer allows the entire memory contents to be serially read during one operation. If the last address byte in the array is acknowledged, the Address Pointer will roll over to address 0x00.

FIGURE 8-4: SEQUENTIAL READ



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APPENDIX A: REVISION HISTORY

Revision A

Original release of document. Combined Serial EEPROM 24XXX device data sheets.

Revision B (02/2007)

Change 1.8V to 1.7V; Removed 14-Lead TSSOP Package; Replaced Package Drawings; Revised Product ID Section. Updates throughout.

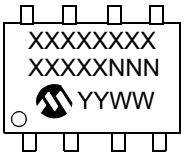
Revision C (07/2007)

Added 24AA1025/LC1025/FC1025 part; Updates throughout; Replaced Package Drawings (Rev. AP).

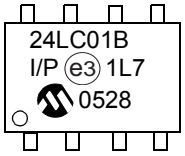
9.0 PACKAGING INFORMATION

9.1 Package Marking Information

8-Lead PDIP



Example:



8-Lead PDIP Package Marking							
Device	**Line 1 Marking**	**Device**	**Line 1 Marking**	**Device**	**Line 1 Marking**	**Device**	**Line 1 Marking**
24AA00	24AA00	24LC00	24LC00	24C00	24C00		
24AA01	24AA01	24LC01B	24LC01B				
24AA014	24AA014	24LC014	24LC014				
				24C01C	24C01C		
24AA02	24AA02	24LC02B	24LC02B				
24AA024	24AA024	24LC024	24LC024				
24AA025	24AA025	24LC025	24LC025				
				24C02C	24C02C		
24AA04	24AA04	24LC04B	24LC04B				
24AA08	24AA08	24LC08B	24LC08B				
24AA16	24AA16	24LC16B	24LC16B				
24AA32A	24AA32A	24LC32A	24LC32A				
24AA64	24AA64	24LC64	24LC64			24FC64	24FC64
24AA128	24AA128	24LC128	24LC128			24FC128	24FC128
24AA256	24AA256	24LC256	24LC256			24FC256	24FC256
24AA512	24AA512	24LC512	24LC512			24FC512	24FC512
24AA1025	24AA1025	24LC1025	24LC1025			24FC1025	24FC1025

Legend:	XX...X	Part number or part number code
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code (2 characters for small packages)
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn) plated devices

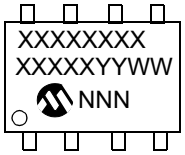
Note: For very small packages with no room for the Pb-free JEDEC designator (e3), the marking will only appear on the outer carton or reel label.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

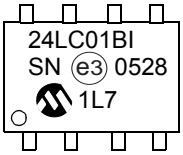
Note: Please visit www.microchip.com/Pbfree for the latest information on Pb-free conversion.

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8-Lead SOIC



Example:



8-Lead SOIC Package Marking							
Device	**Line 1 Marking**	**Device**	**Line 1 Marking**	**Device**	**Line 1 Marking**	**Device**	**Line 1 Marking**
24AA00	24AA00T	24LC00	24LC00T	24C00	24C00T		
24AA01	24AA01T	24LC01B	24LC01BT				
24AA014	24AA014T	24LC014	24LC014T				
				24C01C	24C01CT		
24AA02	24AA02T	24LC02B	24LC02BT				
24AA024	24AA024T	24LC024	24LC024T				
24AA025	24AA025T	24LC025	24LC025T				
				24C02C	24C02CT		
24AA04	24AA04T	24LC04B	24LC04BT				
24AA08	24AA08T	24LC08B	24LC08BT				
24AA16	24AA16T	24LC16B	24LC16BT				
24AA32A	24AA32AT	24LC32A	24LC32AT				
24AA64	24AA64T	24LC64	24LC64T			24FC64	24FC64T
24AA128	24AA128T	24LC128	24LC128T			24FC128	24FC128T
24AA256	24AA256T	24LC256	24LC256T			24FC256	24FC256T
24AA512	24AA512T	24LC512	24LC512T			24FC512	24FC512T
24AA1025	24AA1025	24LC1025	24LC1025			24FC1025	24FC1025

Note: T = Temperature range: I = Industrial, E = Extended

Legend:	XX...X	Part number or part number code
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code (2 characters for small packages)
	e3	Pb-free JEDEC designator for Matte Tin (Sn) plated devices

Note: For very small packages with no room for the Pb-free JEDEC designator e3, the marking will only appear on the outer carton or reel label.

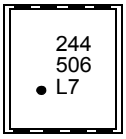
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

Note: Please visit www.microchip.com/Pbfree for the latest information on Pb-free conversion.

8-Lead 2x3 DFN



Example:



8-Lead 2x3mm DFN Package Marking							
Device	**Industrial Line 1 Marking**	**Device**	**Industrial Line 1 Marking**	**E-Temp Line 1 Marking**	**Device**	**Industrial Line 1 Marking**	**E-Temp Line 1 Marking**
24AA00	201	24LC00	204	205	24C00	207	208
24AA01	211	24LC01B	214	215			
24AA014	2N1	24LC014	2N4	2N5			
					24C01C	2N7	2N8
24AA02	221	24LC02B	224	225			
24AA024	2P1	24LC024	2P4	2P5			
24AA025	2R1	24LC025	2R4	2R5			
					24C02C	2P7	2P8
24AA04	231	24LC04B	234	235			
24AA08	241	24LC08B	244	245			
24AA16	251	24LC16B	254	255			
24AA32A	261	24LC32A	264	265			
24AA64	271	24LC64	274	275	24FC64	27A	27B

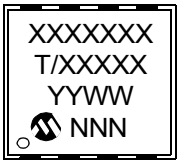
Legend:	XX...X	Part number or part number code
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code (2 characters for small packages)
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn) plated devices

Note: For very small packages with no room for the Pb-free JEDEC designator (e3), the marking will only appear on the outer carton or reel label.

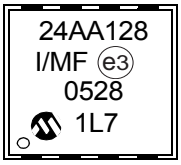
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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8-Lead DFN



Example:



8-Lead 5x6mm DFN Package Marking					
Device	**Line 1 Marking**	**Device**	**Line 1 Marking**	**Device**	**Line 1 Marking**
24AA128	24AA128	24LC128	24LC128	24FC128	24FC128
24AA256	24AA256	24LC256	24LC256	24FC256	24FC256
24AA512	24AA512	24LC512	24LC512	24FC512	24FC512

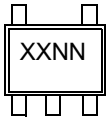
Note: Temperature range (T) listed on second line. I = Industrial, E = Extended

Legend:	XX...X	Part number or part number code
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code (2 characters for small packages)
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn) plated devices

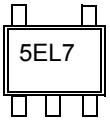
Note: For very small packages with no room for the Pb-free JEDEC designator (e3), the marking will only appear on the outer carton or reel label.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

5-Lead SOT-23



Example:



5-Lead SOT-23 Package Marking										
Device	**Comm. Marking**	**Indust. Marking**	**Device**	**Comm. Marking**	**Indust. Marking**	**E-Temp Marking**	**Device**	**Comm. Marking**	**Indust. Marking**	**E-Temp Marking**
24AA00	A0NN	B0NN	24LC00	L0NN	M0NN	N0NN	24C00	C0NN	D0NN	E0NN
24AA01	A1NN	B1NN	24LC01B	L1NN	M1NN	N1NN				
24AA02	A2NN	B2NN	24LC02B	L2NN	M2NN	N2NN				
24AA04	A3NN	B3NN	24LC04B	L3NN	M3NN	N3NN				
24AA08	A4NN	B4NN	24LC08B	L4NN	M4NN	N4NN				
24AA16	A5NN	B5NN	24LC16B	L5NN	M5NN	N5NN				

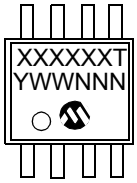
Legend:	XX...X	Part number or part number code
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code (2 characters for small packages)
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn) plated devices

Note: For very small packages with no room for the Pb-free JEDEC designator (e3), the marking will only appear on the outer carton or reel label.

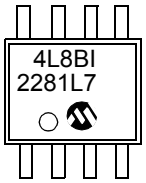
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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8-Lead MSOP (150 mil)



Example:



8-Lead MSOP Package Marking							
Device	**Line 1 Marking**	**Device**	**Line 1 Marking**	**Device**	**Line 1 Marking**	**Device**	**Line 1 Marking**
24AA01	4A01T	24LC01B	4L1BT				
24AA014	4A14T	24LC014	4L14T				
				24C01C	4C1CT		
24AA02	4A02T	24LC02B	4L2BT				
24AA024	4A24T	24LC024	4L24T				
24AA025	4A25T	24LC025	4L25T				
				24C02C	4C2CT		
24AA04	4A04T	24LC04B	4L4BT				
24AA08	4A08T	24LC08B	4L8BT				
24AA16	4A16T	24LC16B	4L16T				
24AA32A	4A32AT	24LC32A	4L32AT				
24AA64	4A64T	24LC64	4L64T			24FC64	4F64T
24AA128	4A128T	24LC128	4L128T			24FC128	4F128T
24AA256	4A256T	24LC256	4L256T			24FC256	4F256T

Note: T = Temperature range: I = Industrial, E = Extended

Legend:	XX...X	Part number or part number code
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code (2 characters for small packages)
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn) plated devices

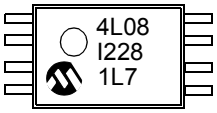
Note: For very small packages with no room for the Pb-free JEDEC designator (e3), the marking will only appear on the outer carton or reel label.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead TSSOP



Example:



8-Lead TSSOP Package Marking							
Device	**Line 1 Marking**	**Device**	**Line 1 Marking**	**Device**	**Line 1 Marking**	**Device**	**Line 1 Marking**
24AA00	4A00	24LC00	4L00	24C00	4C00		
24AA01	4A01	24LC01B	4L1B				
24AA014	4A14	24LC014	4L14				
				24C01C	4C1C		
24AA02	4A02	24LC02B	4L02				
24AA024	4A24	24LC024	4L24				
24AA025	4A25	24LC025	4L25				
				24C02C	4C2C		
24AA04	4A04	24LC04B	4L04				
24AA08	4A08	24LC08B	4L08				
24AA16	4A16	24LC16B	4L16				
24AA32A	4AA	24LC32A	4LA				
24AA64	4AB	24LC64	4LB			24FC64	4FB
24AA128	4AC	24LC128	4LC			24FC128	4FC
24AA256	4AD	24LC256	4LD			24FC256	4FD

Note: T = Temperature range: I = Industrial, E = Extended

Legend:	XX...X	Part number or part number code
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code (2 characters for small packages)
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn) plated devices

Note: For very small packages with no room for the Pb-free JEDEC designator (e3), the marking will only appear on the outer carton or reel label.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	X	/XX
Device Part Number (Table 1-1)	Packaging Medium	Temperature Range	Package

Device: See Table 1-1

Temperature Range:
- I = -40°C to +85°C
- E = -40°C to +125°C

Packaging Medium:
- T = Tape and Reel
- Blank = Tube

Package:
- P = Plastic DIP (300 mil body), 8-lead
- SN = Plastic SOIC (3.90 mm body), 8-lead
- SM = Plastic SOIC (208 mil body), 8-lead
- ST = Plastic TSSOP (4.4 mm), 8-lead
- MS = MSOP (3.0 mm), 8-lead
- OT = SOT-23, 5-lead (Tape and Reel only)
- MC = 2x3 mm DFN, 8-lead (Tape and Reel only)
- MF = 5x6 mm DFN, 8-lead

Examples:

a) 24AA014-I/SN: 1 Kbit, Industrial Temperature, 1.7V, SOIC package

b) 24AA02T-I/OT: 2 Kbit, Industrial Temperature, 1.7V, SOT-23 package, Tape and Reel

c) 24LC16B-I/P: 16 Kbit, Industrial Temperature, 2.5V, PDIP package

d) 24LC32A-E/MS: 32 Kbit, Extended Temperature, 2.5V, MSOP package

e) 24LC64T-I/MC: 64 Kbit, Industrial Temperature, 2.5V 2x3 mm DFN package, Tape and Reel

f) 24FC512T-I/SM: 512 Kbit, Industrial Temperature, 1 MHz, SOIC package, Tape and Reel

NOTES:

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1K-16K Microwire Compatible Serial EEPROMs

Features:

- Densities from 1 Kbits through 16 Kbits
- Low-Power CMOS Technology
- Available With or Without ORG Function:

  With ORG Function:
  - ORG pin at Logic Low: 8-bit word
  - ORG pin at Logic High: 16-bit word

  Without ORG Function:
  - 'A' version: 8-bit word
  - 'B' version: 16-bit word
- Program Enable Pin:
  - Write-protect for entire array (93XX76C and 93XX86C only)
- Self-Timed Erase/Write Cycles (including auto-erase)
- Automatic ERAL Before WRAL
- Power-On/Off Data Protection Circuitry
- Industry Standard 3-Wire Serial I/O
- Device Status Signal (Ready/$\overline{\text{Busy}}$)
- Sequential Read Function
- 1,000,000 E/W Cycles
- Data Retention > 200 Years
- Pb-Free and RoHS Compliant
- Temperature Ranges Supported:
  - Industrial (I) -40°C to +85°C
  - Automotive (E) -40°C to +125°C

Pin Function Table

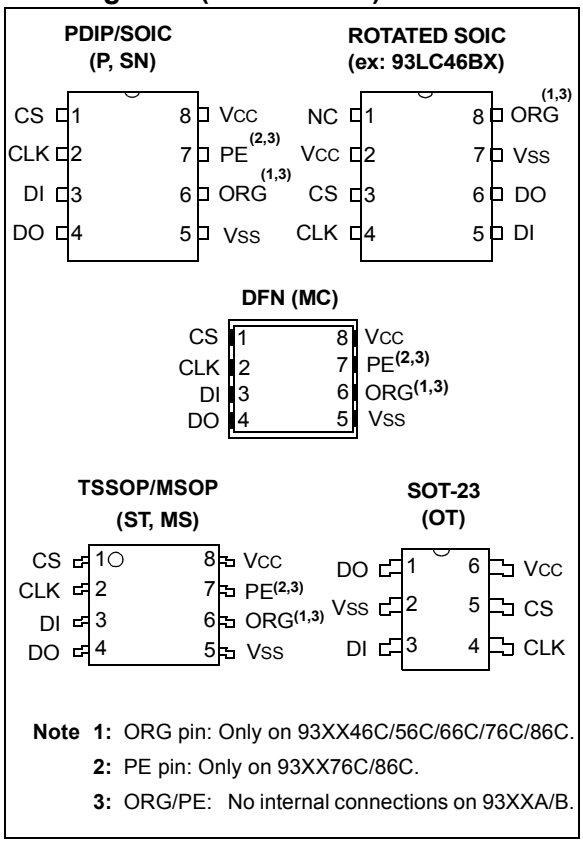
Name	Function
CS	Chip Select
CLK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
VSS	Ground
PE	Program Enable
ORG	Memory Configuration
VCC	Power Supply

Note: ORG and PE functionality not available in all products. See Table 1-1, Device Selection Table.

Description:

Microchip Technology Inc. supports the 3-wire Microwire bus with low-voltage serial Electrically Erasable PROMs (EEPROM) that range in density from 1 Kbits up to 16 Kbits. Each density is available with and without the ORG functionality, and selected by the part number ordered. Advanced CMOS technology makes these devices ideal for low-power, nonvolatile memory applications. The entire series of Microwire devices are available in the standard 8-lead PDIP and SOIC packages, as well as the more advanced packaging such as the 8-lead MSOP, 8-lead TSSOP, 6-lead SOT-23, and 8-lead DFN (2x3). All packages are Pb-free.

Pin Diagrams (not to scale)



Note 1: ORG pin: Only on 93XX46C/56C/66C/76C/86C.
2: PE pin: Only on 93XX76C/86C.
3: ORG/PE: No internal connections on 93XXA/B.

TABLE 1-1: DEVICE SELECTION TABLE

Part Number	Density (Kbits)	Vcc Range	ORG Pin	Organization (Words)	PE Pin	Temp Range	Packages
93XX46A/B/C							
93AA46A	1	1.8-5.5	No	128 x 8 bits	No	I	P, SN, ST, MS, OT, MC
93AA46B	1	1.8-5.5	No	64 x 16 bits	No	I	P, SN, ST, MS, OT, MC
93AA46C	1	1.8-5.5	Yes	Selectable x8 or x16	No	I	P, SN, ST, MS, MC
93LC46A	1	2.5-5.5	No	128 x 8 bits	No	I, E	P, SN, ST, MS, OT, MC
93LC46B	1	2.5-5.5	No	64 x 16 bits	No	I, E	P, SN, ST, MS, OT, MC
93LC46C	1	2.5-5.5	Yes	Selectable x8 or x16	No	I, E	P, SN, ST, MS, MC
93C46A	1	4.5-5.5	No	128 x 8 bits	No	I, E	P, SN, ST, MS, OT, MC
93C46B	1	4.5-5.5	No	64 x 16 bits	No	I, E	P, SN, ST, MS, OT, MC
93C46C	1	4.5-5.5	Yes	Selectable x8 or x16	No	I, E	P, SN, ST, MS, MC
93AA46AX/BX/CX, 93LC46AX/BX/CX, 93C46AX/BX/CX (Alternate pinout with die rotated 90°)							
93AA46AX	1	1.8-5.5	No	128 x 8 bits	No	I	P, SN, ST, MS, OT, MC
93AA46BX	1	1.8-5.5	No	64 x 16 bits	No	I	P, SN, ST, MS, OT, MC
93AA46CX	1	1.8-5.5	Yes	Selectable x8 or x16	No	I	P, SN, ST, MS, MC
93LC46AX	1	2.5-5.5	No	128 x 8 bits	No	I, E	P, SN, ST, MS, OT, MC
93LC46BX	1	2.5-5.5	No	64 x 16 bits	No	I, E	P, SN, ST, MS, OT, MC
93LC46CX	1	2.5-5.5	Yes	Selectable x8 or x16	No	I, E	P, SN, ST, MS, MC
93C46AX	1	4.5-5.5	No	128 x 8 bits	No	I, E	P, SN, ST, MS, OT, MC
93C46BX	1	4.5-5.5	No	64 x 16 bits	No	I, E	P, SN, ST, MS, OT, MC
93C46CX	1	4.5-5.5	Yes	Selectable x8 or x16	No	I, E	P, SN, ST, MS, MC
93XX56A/B/C							
93AA56A	2	1.8-5.5	No	256 x 8 bits	No	I	P, SN, ST, MS, OT, MC
93AA56B	2	1.8-5.5	No	128 x 16 bits	No	I	P, SN, ST, MS, OT, MC
93AA56C	2	1.8-5.5	Yes	Selectable x8 or x16	No	I	P, SN, ST, MS, MC
93LC56A	2	2.5-5.5	No	256 x 8 bits	No	I, E	P, SN, ST, MS, OT, MC
93LC56B	2	2.5-5.5	No	128 x 16 bits	No	I, E	P, SN, ST, MS, OT, MC
93LC56C	2	2.5-5.5	Yes	Selectable x8 or x16	No	I, E	P, SN, ST, MS, MC
93C56A	2	4.5-5.5	No	256 x 8 bits	No	I, E	P, SN, ST, MS, OT, MC
93C56B	2	4.5-5.5	No	128 x 16 bits	No	I, E	P, SN, ST, MS, OT, MC
93C56C	2	4.5-5.5	Yes	Selectable x8 or x16	No	I, E	P, SN, ST, MS, MC
93XX66A/B/C							
93AA66A	4	1.8-5.5	No	512 x 8 bits	No	I	P, SN, ST, MS, OT, MC
93AA66B	4	1.8-5.5	No	256 x 16 bits	No	I	P, SN, ST, MS, OT, MC
93AA66C	4	1.8-5.5	Yes	Selectable x8 or x16	No	I	P, SN, ST, MS, MC
93LC66A	4	2.5-5.5	No	512 x 8 bits	No	I, E	P, SN, ST, MS, OT, MC
93LC66B	4	2.5-5.5	No	256 x 16 bits	No	I, E	P, SN, ST, MS, OT, MC
93LC66C	4	2.5-5.5	Yes	Selectable x8 or x16	No	I, E	P, SN, ST, MS, MC
93C66A	4	4.5-5.5	No	512 x 8 bits	No	I, E	P, SN, ST, MS, OT, MC
93C66B	4	4.5-5.5	No	256 x 16 bits	No	I, E	P, SN, ST, MS, OT, MC
93C66C	4	4.5-5.5	Yes	Selectable x8 or x16	No	I, E	P, SN, ST, MS, MC

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TABLE 1-1: DEVICE SELECTION TABLE (CONTINUED)

Part Number	Density (Kbits)	Vcc Range	ORG Pin	Organization (Words)	PE Pin	Temp Range	Packages
93XX76A/B/C							
93AA76A	8	1.8-5.5	No	1024 x 8 bits	No	I	OT
93AA76B	8	1.8-5.5	No	512 x 16 bits	No	I	OT
93AA76C	8	1.8-5.5	Yes	Selectable x8 or x16	Yes	I	P, SN, ST, MS, MC
93LC76A	8	2.5-5.5	No	1024 x 8 bits	No	I, E	OT
93LC76B	8	2.5-5.5	No	512 x 16 bits	No	I, E	OT
93LC76C	8	2.5-5.5	Yes	Selectable x8 or x16	Yes	I, E	P, SN, ST, MS, MC
93C76A	8	4.5-5.5	No	1024 x 8 bits	No	I, E	OT
93C76B	8	4.5-5.5	No	512 x 16 bits	No	I, E	OT
93C76C	8	4.5-5.5	Yes	Selectable x8 or x16	Yes	I, E	P, SN, ST, MS, MC
93XX86A/B/C							
93AA86A	16	1.8-5.5	No	2048 x 8 bits	No	I	OT
93AA86B	16	1.8-5.5	No	1024 x 16 bits	No	I	OT
93AA86C	16	1.8-5.5	Yes	Selectable x8 or x16	Yes	I	P, SN, ST, MS, MC
93LC86A	16	2.5-5.5	No	2048 x 8 bits	No	I, E	OT
93LC86B	16	2.5-5.5	No	1024 x 16 bits	No	I, E	OT
93LC86C	16	2.5-5.5	Yes	Selectable x8 or x16	Yes	I, E	P, SN, ST, MS, MC
93C86A	16	4.5-5.5	No	2048 x 8 bits	No	I, E	OT
93C86B	16	4.5-5.5	No	1024 x 16 bits	No	I, E	OT
93C86C	16	4.5-5.5	Yes	Selectable x8 or x16	Yes	I, E	P, SN, ST, MS, MC

2.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(†)

VCC.....7.0V

All inputs and outputs w.r.t. VSS ..... -0.6V to VCC +1.0V

Storage temperature .....-65°C to +150°C

Ambient temperature with power applied .....-40°C to +125°C

ESD protection on all pins .....≥ 4 kV

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 2-1: DC CHARACTERISTICS

All parameters apply over the specified ranges unless otherwise noted.			VCC = 1.8V to 5.5V Industrial (I): TA = -40°C to +85°C Automotive (E): TA = -40°C to +125°C				
Param. No.	**Symbol**	**Parameter**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
D1	VIH1 VIH2	High-level input voltage	2.0 0.7 VCC	— —	VCC +1 VCC +1	V V	VCC ≥ 2.7V VCC < 2.7V
D2	VIL1 VIL2	Low-level input voltage	-0.3 -0.3	— —	0.8 0.2 VCC	V V	VCC ≥ 2.7V VCC < 2.7V
D3	VOL1 VOL2	Low-level output voltage	— —	— —	0.4 0.2	V V	IOL = 2.1 mA, VCC = 4.5V IOL = 100 µA, VCC = 2.5V
D4	VOH1 VOH2	High-level output voltage	2.4 VCC-0.2	— —	— —	V V	IOH = -400 µA, VCC = 4.5V IOH = -100 µA, VCC = 2.5V
D5	ILI	Input leakage current	—	—	±1	µA	VIN = VSS to VCC
D6	ILO	Output leakage current	—	—	±1	µA	VOUT = VSS to VCC
D7	CIN, COUT	Pin capacitance (all inputs/outputs)	—	—	7	pF	VIN/VOUT = 0V **(Note 1)** TA = 25°C, FCLK = 1 MHz
D8	ICC write	Write current	—	—	2	mA	FCLK = 3 MHz, VCC = 5.5V (93XX46X/56X/66X)
			— —	— 500	3 —	mA µA	FCLK = 3 MHz, VCC = 5.5V (93XX76X/86X) FCLK = 2 MHz, VCC = 2.5V
D9	ICC read	Read current	— — —	— — 100	1 500 —	mA µA µA	FCLK = 3 MHz, VCC = 5.5V FCLK = 2 MHz, VCC = 3.0V FCLK = 2 MHz, VCC = 2.5V
D10	ICCS	Standby current	— —	— —	1 5	µA µA	I-Temp **(Note 2, 3)** E-Temp CLK = Cs = 0V ORG = DI = VSS or VCC
D11	VPOR	VCC voltage detect	— —	1.5V 3.8V	— —	V V	93AAX6A/B/C, 93LCX6A/B/C, 93CX6A/B/C **(Note 1)**

Note 1: This parameter is periodically sampled and not 100% tested.

2: ORG and PE pins not available on ‘A’ or ‘B’ versions.

3: Ready/$\overline{\text{Busy}}$ status must be cleared from DO, see **Section 4.4 “Data Out (DO)”**.

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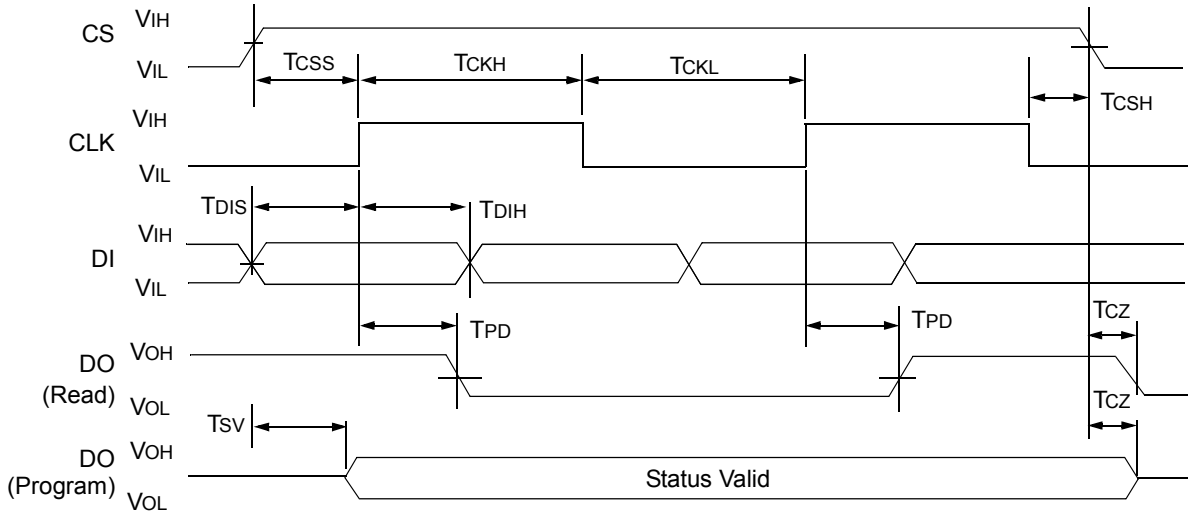
TABLE 2-2: AC CHARACTERISTICS

All parameters apply over the specified ranges unless otherwise noted.			V_{CC} = 1.8V to 5.5V Industrial (I): T_A = -40°C to +85°C Automotive (E): T_A = -40°C to +125°C			
Param. No.	**Symbol**	**Parameter**	**Min.**	**Max.**	**Units**	**Conditions**
A1	F_{CLK}	Clock frequency	—	3 2 1	MHz MHz MHz	4.5V ≤ V_{CC} < 5.5V 2.5V ≤ V_{CC} < 4.5V 1.8V ≤ V_{CC} < 2.5V
A2	T_{CKH}	Clock high time	200 250 450	—	ns ns ns	4.5V ≤ V_{CC} < 5.5V 2.5V ≤ V_{CC} < 4.5V 1.8V ≤ V_{CC} < 2.5V
A3	T_{CKL}	Clock low time	100 200 450	—	ns ns ns	4.5V ≤ V_{CC} < 5.5V 2.5V ≤ V_{CC} < 4.5V 1.8V ≤ V_{CC} < 2.5V
A4	T_{CSS}	Chip Select setup time	50 100 250	—	ns ns ns	4.5V ≤ V_{CC} < 5.5V 2.5V ≤ V_{CC} < 4.5V 1.8V ≤ V_{CC} < 2.5V
A5	T_{CSH}	Chip Select hold time	0	—	ns	1.8V ≤ V_{CC} < 5.5V
A6	T_{CSL}	Chip Select low time	250	—	ns	1.8V ≤ V_{CC} < 5.5V
A7	T_{DIS}	Data input setup time	50 100 250	—	ns ns ns	4.5V ≤ V_{CC} < 5.5V 2.5V ≤ V_{CC} < 4.5V 1.8V ≤ V_{CC} < 2.5V
A8	T_{DIH}	Data input hold time	50 100 250	—	ns ns ns	4.5V ≤ V_{CC} < 5.5V 2.5V ≤ V_{CC} < 4.5V 1.8V ≤ V_{CC} < 2.5V
A9	T_{PD}	Data output delay time	—	100	ns	4.5V ≤ V_{CC} < 5.5V, CL = 100 pF (93C76X/86X)
			—	200 250 400	ns ns ns	4.5V ≤ V_{CC} < 5.5V, CL = 100 pF 2.5V ≤ V_{CC} < 4.5V, CL = 100 pF 1.8V ≤ V_{CC} < 2.5V, CL = 100 pF
A10	T_{CZ}	Data output disable time	—	100 200	ns ns	4.5V ≤ V_{CC} < 5.5V, **(Note 1)** 1.8V ≤ V_{CC} < 4.5V, **(Note 1)**
A11	T_{SV}	Status valid time	—	200 300 500	ns ns ns	4.5V ≤ V_{CC} < 5.5V, CL = 100 pF 2.5V ≤ V_{CC} < 4.5V, CL = 100 pF 1.8V ≤ V_{CC} < 2.5V, CL = 100 pF
A12	T_{WC}	Program cycle time	—	5	ms	Erase/Write mode 93XX76X/86X (AA and LC versions)
			—	6	ms	93XX46X/56X/66X (AA and LC versions)
A13	T_{WC}		—	2	ms	93C46X/56X/66X/76X/86X
A14	T_{EC}	Program cycle time	—	6	ms	ERAL mode, 4.5V ≤ V_{CC} ≤ 5.5V
A15	T_{WL}		—	15	ms	WRAL mode, 4.5V ≤ V_{CC} ≤ 5.5V
A16	—	Endurance	1M	—	cycles	25°C, V_{CC} = 5.0V, **(Note 2)**

Note 1: This parameter is periodically sampled and not 100% tested.

2: This application is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which may be downloaded from Microchip's web site at www.microchip.com.

FIGURE 2-1: SYNCHRONOUS DATA TIMING



Note: Status Valid Time (TSV) is relative to CS.

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TABLE 2-3: INSTRUCTION SET FOR 93XX46A/B/C

Instruction	SB	Opcode	Address								Data In	Data Out	Req. CLK Cycles
93XX46B OR 93XX46C WITH ORG = 1 (16-BIT WORD ORGANIZATION)													
ERASE	1	11		A5	A4	A3	A2	A1	A0		—	(RDY/$\overline{BSY}$)	9
ERAL	1	00		1	0	x	x	x	x		—	(RDY/$\overline{BSY}$)	9
EWDS	1	00		0	0	x	x	x	x		—	High-Z	9
EWEN	1	00		1	1	x	x	x	x		—	High-Z	9
READ	1	10		A5	A4	A3	A2	A1	A0		—	D15-D0	25
WRITE	1	01		A5	A4	A3	A2	A1	A0		D15-D0	(RDY/$\overline{BSY}$)	25
WRAL	1	00		0	1	x	x	x	x		D15-D0	(RDY/$\overline{BSY}$)	25
93XX46A OR 93XX46C WITH ORG = 0 (8-BIT WORD ORGANIZATION)													
ERASE	1	11		A6	A5	A4	A3	A2	A1	A0	—	(RDY/$\overline{BSY}$)	10
ERAL	1	00		1	0	x	x	x	x	x	—	(RDY/$\overline{BSY}$)	10
EWDS	1	00		0	0	x	x	x	x	x	—	High-Z	10
EWEN	1	00		1	1	x	x	x	x	x	—	High-Z	10
READ	1	10		A6	A5	A4	A3	A2	A1	A0	—	D7-D0	18
WRITE	1	01		A6	A5	A4	A3	A2	A1	A0	D7-D0	(RDY/$\overline{BSY}$)	18
WRAL	1	00		0	1	x	x	x	x	x	D7-D0	(RDY/$\overline{BSY}$)	18

TABLE 2-4: INSTRUCTION SET FOR 93XX56A/B/C

Instruction	SB	Opcode	Address									Data In	Data Out	Req. CLK Cycles
93XX56B OR 93XX56C WITH ORG = 1 (16-BIT WORD ORGANIZATION)														
ERASE	1	11		x	A6	A5	A4	A3	A2	A1	A0	—	(RDY/$\overline{BSY}$)	11
ERAL	1	00		1	0	x	x	x	x	x	x	—	(RDY/$\overline{BSY}$)	11
EWDS	1	00		0	0	x	x	x	x	x	x	—	High-Z	11
EWEN	1	00		1	1	x	x	x	x	x	x	—	High-Z	11
READ	1	10		x	A6	A5	A4	A3	S2	A1	A0	—	D15-D0	27
WRITE	1	01		x	A6	A5	A4	A3	S2	A1	A0	D15-D0	(RDY/$\overline{BSY}$)	27
WRAL	1	00		0	1	x	x	x	x	x	x	D15-D0	(RDY/$\overline{BSY}$)	27
93XX56A OR 93XX56C WITH ORG = 0 (8-BIT WORD ORGANIZATION)														
ERASE	1	11	x	A7	A6	A5	A4	A3	A2	A1	A0	—	(RDY/$\overline{BSY}$)	12
ERAL	1	00	1	0	x	x	x	x	x	x	x	—	(RDY/$\overline{BSY}$)	12
EWDS	1	00	0	0	x	x	x	x	x	x	x	—	High-Z	12
EWEN	1	00	1	1	x	x	x	x	x	x	x	—	High-Z	12
READ	1	10	x	A7	A6	A5	A4	A3	A2	A1	A0	—	D7-D0	20
WRITE	1	01	x	A7	A6	A5	A4	A3	A2	A1	A0	D7-D0	(RDY/$\overline{BSY}$)	20
WRAL	1	00	0	1	x	x	x	x	x	x	x	D7-D0	(RDY/$\overline{BSY}$)	20

TABLE 2-5: INSTRUCTION SET FOR 93XX66A/B/C

Instruction	SB	Opcode	Address									Data In	Data Out	Req. CLK Cycles
93XX66B OR 93XX66C WITH ORG = 1 (16-BIT WORD ORGANIZATION)														
ERASE	1	11		A7	A6	A5	A4	A3	A2	A1	A0	—	(RDY/$\overline{BSY}$)	11
ERAL	1	00		1	0	x	x	x	x	x	x	—	(RDY/$\overline{BSY}$)	11
EWDS	1	00		0	0	x	x	x	x	x	x	—	High-Z	11
EWEN	1	00		1	1	x	x	x	x	x	x	—	High-Z	11
READ	1	10		A7	A6	A5	A4	A3	A2	A1	A0	—	D15-D0	27
WRITE	1	01		A7	A6	A5	A4	A3	A2	A1	A0	D15-D0	(RDY/$\overline{BSY}$)	27
WRAL	1	00		0	1	x	x	x	x	x	x	D15-D0	(RDY/$\overline{BSY}$)	27
93XX66A OR 93XX66C WITH ORG = 0 (8-BIT WORD ORGANIZATION)														
ERASE	1	11		A8	A7	A6	A5	A4	A3	A2	A1	A0	—	(RDY/$\overline{BSY}$)	12
ERAL	1	00		1	0	x	x	x	x	x	x	x	—	(RDY/$\overline{BSY}$)	12
EWDS	1	00		0	0	x	x	x	x	x	x	x	—	High-Z	12
EWEN	1	00		1	1	x	x	x	x	x	x	x	—	High-Z	12
READ	1	10		A8	A7	A6	A5	A4	A3	A2	A1	A0	—	D7-D0	20
WRITE	1	01		A8	A7	A6	A5	A4	A3	A2	A1	A0	D7-D0	(RDY/$\overline{BSY}$)	20
WRAL	1	00		0	1	x	x	x	x	x	x	x	D7-D0	(RDY/$\overline{BSY}$)	20

TABLE 2-6: INSTRUCTION SET FOR 93XX76A/B/C

Instruction	SB	Opcode	Address											Data In	Data Out	Req. CLK Cycles
93XX76B OR 93XX76C WITH ORG = 1 (16-BIT WORD ORGANIZATION)																
ERASE	1	11		x	A8	A7	A6	A5	A4	A3	A2	A1	A0	—	(RDY/$\overline{BSY}$)	13
ERAL	1	00		1	0	x	x	x	x	x	x	x	x	—	(RDY/$\overline{BSY}$)	13
EWDS	1	00		0	0	x	x	x	x	x	x	x	x	—	High-Z	13
EWEN	1	00		1	1	x	x	x	x	x	x	x	x	—	High-Z	13
READ	1	10		x	A8	A7	A6	A5	A4	A3	A2	A1	A0	—	D15-D0	29
WRITE	1	01		x	A8	A7	A6	A5	A4	A3	A2	A1	A0	D15-D0	(RDY/$\overline{BSY}$)	29
WRAL	1	00		0	1	x	x	x	x	x	x	x	x	D15-D0	(RDY/$\overline{BSY}$)	29
93XX76A OR 93XX76C WITH ORG = 0 (8-BIT WORD ORGANIZATION)																
ERASE	1	11	x	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	—	(RDY/$\overline{BSY}$)	14
ERAL	1	00	1	0	x	x	x	x	x	x	x	x	x	—	(RDY/$\overline{BSY}$)	14
EWDS	1	00	0	0	x	x	x	x	x	x	x	x	x	—	High-Z	14
EWEN	1	00	1	1	x	x	x	x	x	x	x	x	x	—	High-Z	14
READ	1	10	x	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	—	D7-D0	22
WRITE	1	01	x	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	D7-D0	(RDY/$\overline{BSY}$)	22
WRAL	1	00	0	1	x	x	x	x	x	x	x	x	x	D7-D0	(RDY/$\overline{BSY}$)	22

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TABLE 2-7: INSTRUCTION SET FOR 93XX86A/B/C

Instruction	SB	Opcode	Address										Data In	Data Out	Req. CLK Cycles
93XX86B OR 93XX86C WITH ORG = 1 (16-BIT WORD ORGANIZATION)															
ERASE	1	11		A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	—	(RDY/$\overline{BSY}$)	13
ERAL	1	00		1	0	x	x	x	x	x	x	x	x	—	(RDY/$\overline{BSY}$)	13
EWDS	1	00		0	0	x	x	x	x	x	x	x	x	—	High-Z	13
EWEN	1	00		1	1	x	x	x	x	x	x	x	x	—	High-Z	13
READ	1	10		A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	—	D15-D0	29
WRITE	1	01		A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	D15-D0	(RDY/$\overline{BSY}$)	29
WRAL	1	00		0	1	x	x	x	x	x	x	x	x	D15-D0	(RDY/$\overline{BSY}$)	29
93XX86A OR 93XX86C WITH ORG = 0 (8-BIT WORD ORGANIZATION)															
ERASE	1	11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	—	(RDY/$\overline{BSY}$)	14
ERAL	1	00	1	0	x	x	x	x	x	x	x	x	x	—	(RDY/$\overline{BSY}$)	14
EWDS	1	00	0	0	x	x	x	x	x	x	x	x	x	—	High-Z	14
EWEN	1	00	1	1	x	x	x	x	x	x	x	x	x	—	High-Z	14
READ	1	10	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	—	D7-D0	22
WRITE	1	01	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	D7-D0	(RDY/$\overline{BSY}$)	22
WRAL	1	00	0	1	x	x	x	x	x	x	x	x	x	D7-D0	(RDY/$\overline{BSY}$)	22

3.0 FUNCTIONAL DESCRIPTION

When the ORG pin is connected to VCC, the (x16) organization is selected. When it is connected to ground, the (x8) organization is selected. Instructions, addresses and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normally held in a High-Z state except when reading data from the device, or when checking the Ready/Busy status during a programming operation. The Ready/Busy status can be verified during an Erase/Write operation by polling the DO pin; DO low indicates that programming is still in progress, while DO high indicates the device is ready. DO will enter the High-Z state on the falling edge of CS.

3.1 Start Condition

The Start bit is detected by the device if CS and DI are both high with respect to the positive edge of CLK for the first time.

Before a Start condition is detected, CS, CLK and DI may change in any combination (except to that of a Start condition), without resulting in any device operation (Read, Write, Erase, EWEN, EWDS, ERAL or WRAL). As soon as CS is high, the device is no longer in Standby mode.

An instruction following a Start condition will only be executed if the required opcode, address and data bits for any particular instruction are clocked in.

Note:	When preparing to transmit an instruction, either the CLK or DI signal levels must be at a logic low as CS is toggled active high.

3.2 Data In/Data Out (DI/DO)

It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a “bus conflict” to occur during the “dummy zero” that precedes the read operation, if A0 is a logic high level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A0. The higher the current sourcing capability of the driver, the higher the voltage at the Data Out pin. In order to limit this current, a resistor should be connected between DI and DO.

3.3 Data Protection

All modes of operation are inhibited when VCC is below a typical voltage of 1.5V for ‘93AAXX’ and ‘93LCXX’ devices or 3.8V for ‘93CXX’ devices.

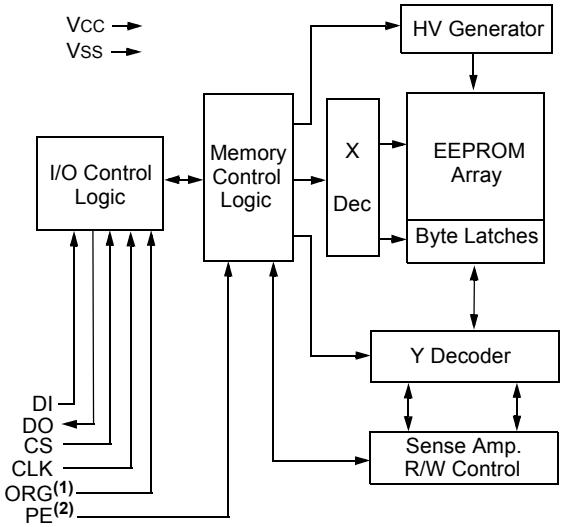
The EWEN and EWDS commands give additional protection against accidentally programming during normal operation.

Note:	For added protection, an EWDS command should be performed after every write operation and an external 10 kΩ pull-down protection resistor should be added to the CS pin.

After power-up, the device is automatically in the EWDS mode. Therefore, an `EWEN` instruction must be performed before the initial `ERASE` or `WRITE` instruction can be executed.

Note:	To prevent accidental writes to the array in the 93XX76C/86C devices, set the PE pin to a logic low.

Block Diagram



Note 1: ORG pin: Only on 93XX46C/56C/66C/76C/86C.

2: PE pin: Only on 93XX76C/86C.

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3.4 ERASE

The ERASE instruction forces all data bits of the specified address to the logical '1' state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle, except on '93CXX' devices where the rising edge of CLK before the last address bit initiates the write cycle.

The DO pin indicates the Ready/$\overline{\text{Busy}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL). DO at logical '0' indicates that programming is still in progress. DO at logical '1' indicates that the register at the specified address has been erased and the device is ready for another instruction.

Note:	After the Erase cycle is complete, issuing a Start bit and then taking CS low will clear the Ready/$\overline{\text{Busy}}$ status from DO.

FIGURE 3-1: ERASE TIMING FOR 93AAXX AND 93LCXX DEVICES

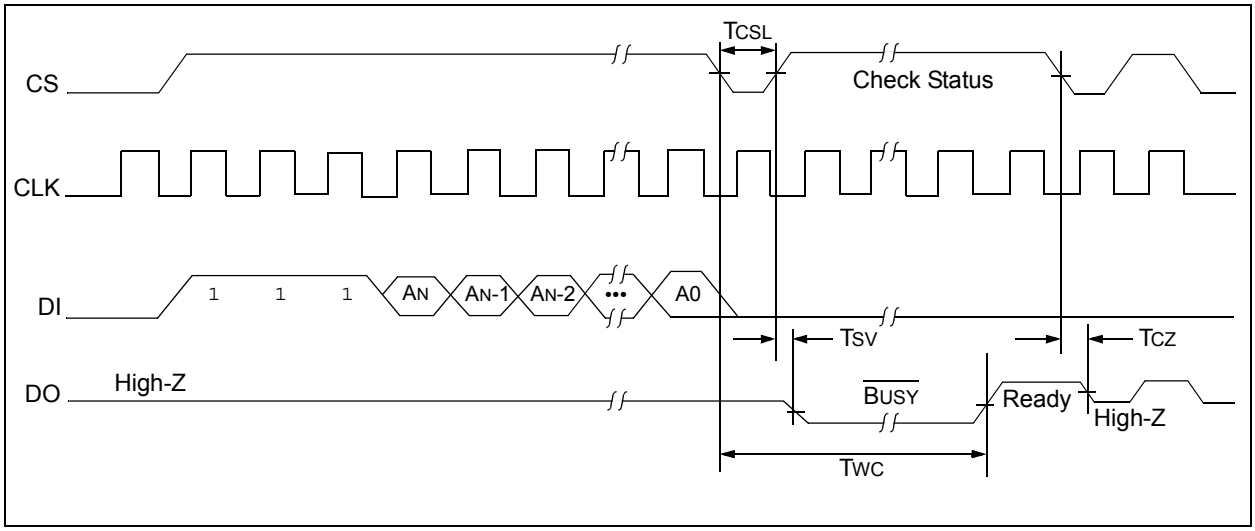
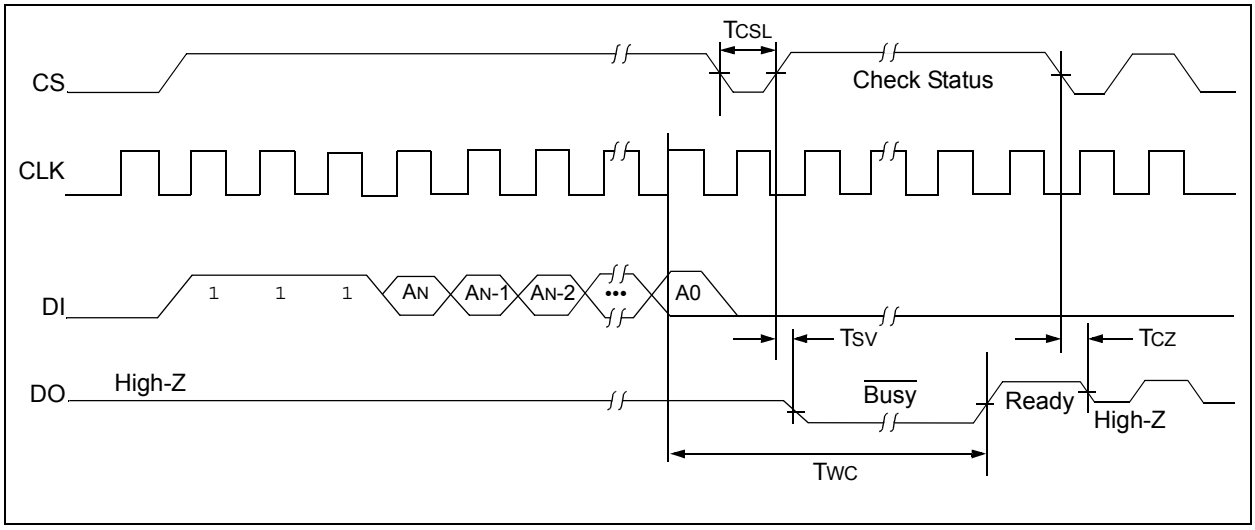


FIGURE 3-2: ERASE TIMING FOR 93CXX DEVICES



3.5 ERASE ALL (ERAL)

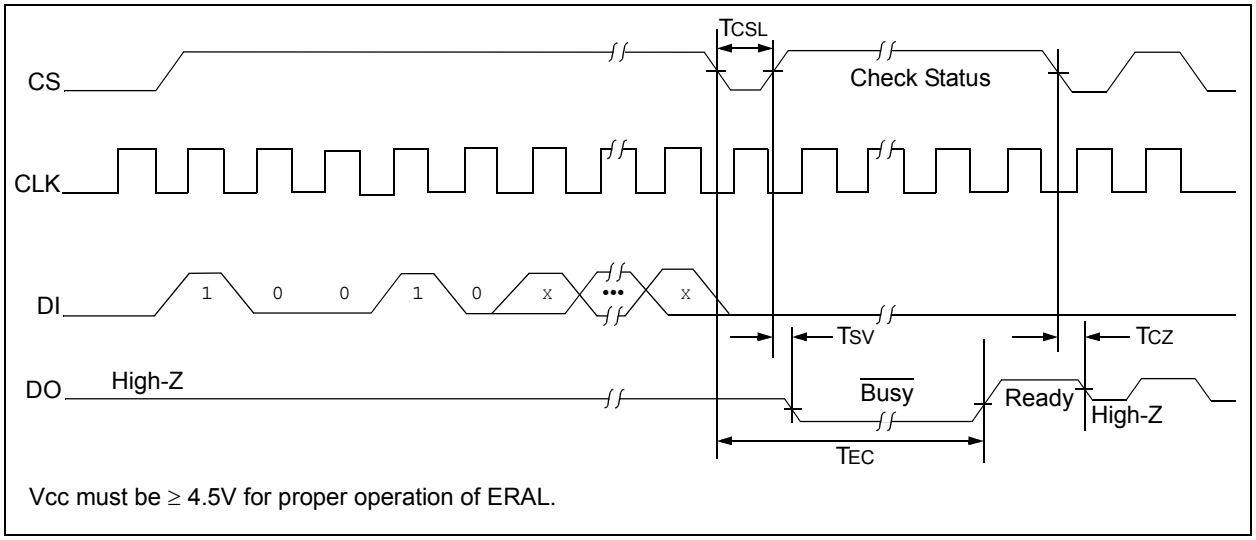
The Erase All (ERAL) instruction will erase the entire memory array to the logical '1' state. The ERAL cycle is identical to the Erase cycle, except for the different opcode. The ERAL cycle is completely self-timed and commences at the falling edge of the CS, except on '93CXX' devices where the rising edge of CLK before the last data bit initiates the write cycle. Clocking of the CLK pin is not necessary after the device has entered the ERAL cycle.

The DO pin indicates the Ready/$\overline{\text{Busy}}$ status of the device, if CS is brought high after a minimum of 250 ns low (TCSL).

VCC must be ≥ 4.5V for proper operation of ERAL.

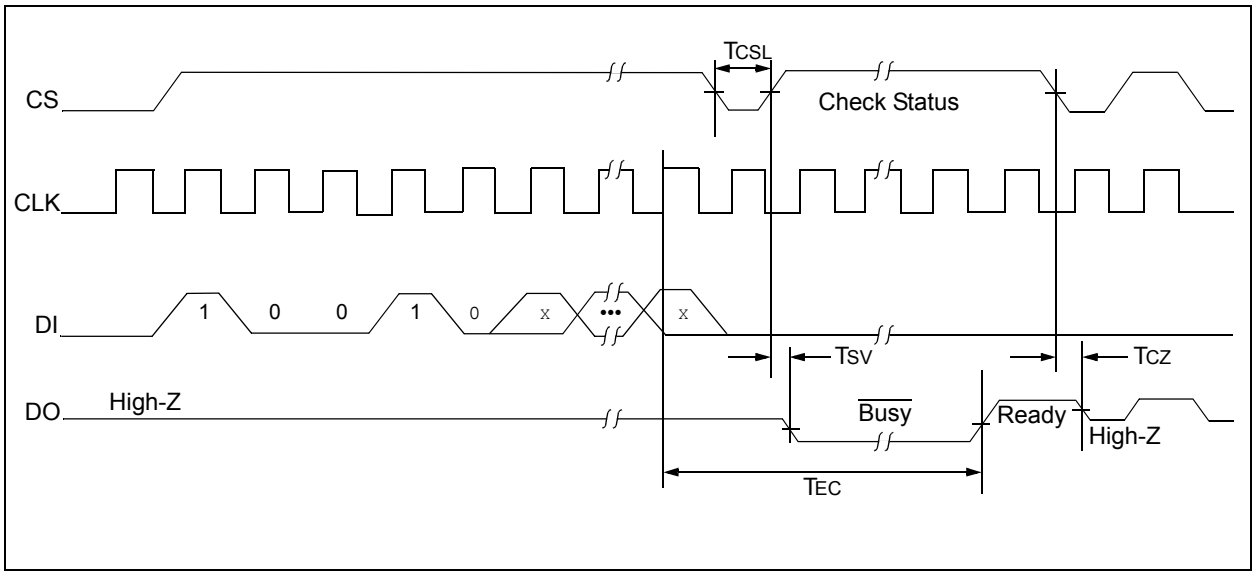
Note:	After the ERAL command is complete, issuing a Start bit and then taking CS low will clear the Ready/$\overline{\text{Busy}}$ status from DO.

FIGURE 3-3: ERAL TIMING FOR 93AAXX AND 93LCXX DEVICES



Vcc must be ≥ 4.5V for proper operation of ERAL.

FIGURE 3-4: ERAL TIMING FOR 93CXX DEVICES



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3.6 ERASE/WRITE DISABLE And ENABLE (EWDS/EWEN)

The 93XX series devices power-up in the Erase/Write Disable (EWDS) state. All programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once the EWEN instruction is executed, programming remains enabled until an EWDS instruction is executed or VCC is removed from the device.

To protect against accidental data disturbance, the EWDS instruction can be used to disable all Erase/Write functions and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

FIGURE 3-5: EWDS TIMING

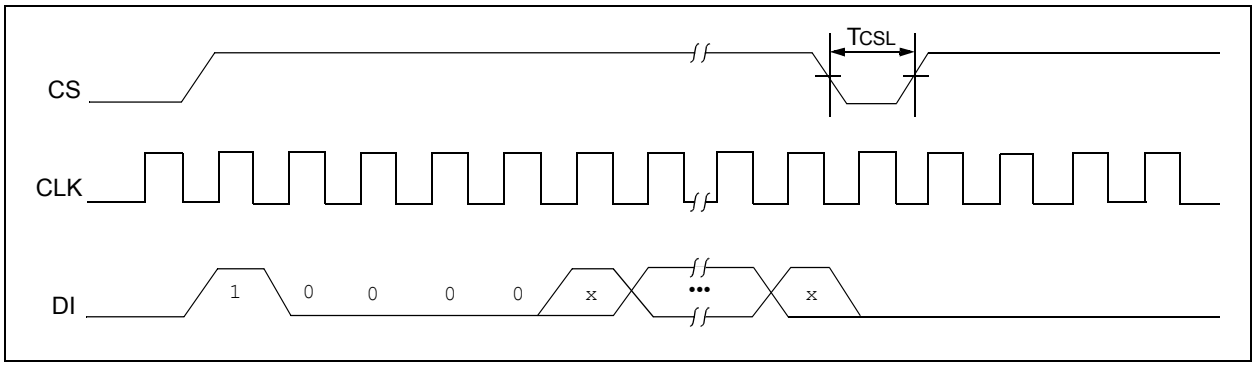
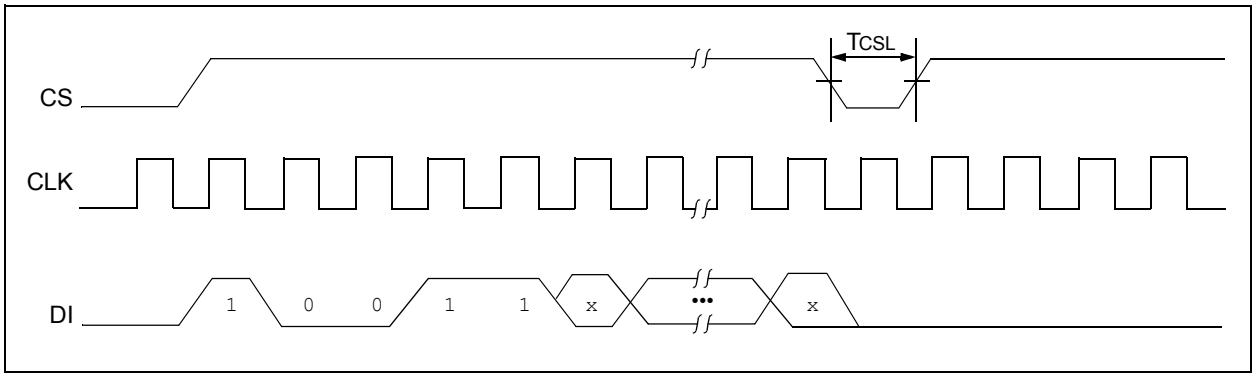


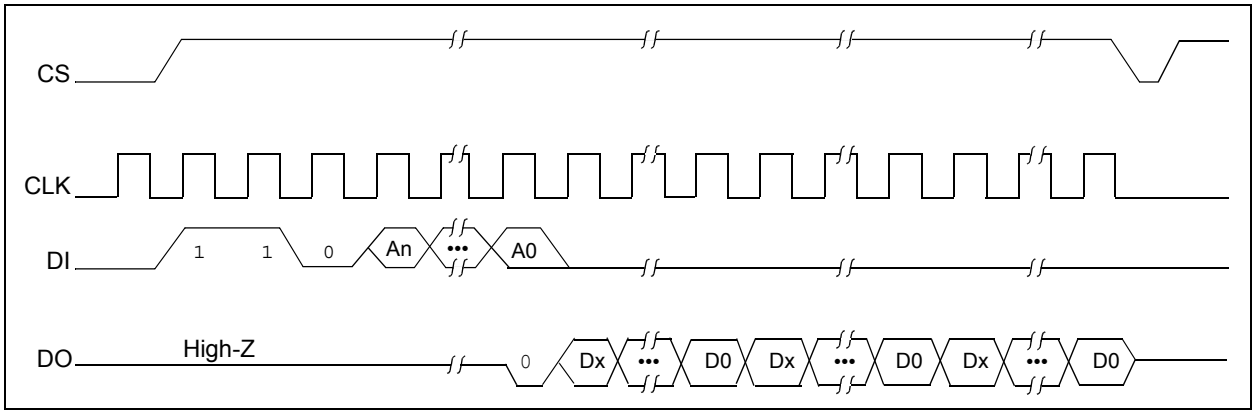
FIGURE 3-6: EWEN TIMING



3.7 READ

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy zero bit precedes the 8-bit (If ORG pin is low or A-version devices) or 16-bit (If ORG pin is high or B-version devices) output string. The output data bits will toggle on the rising edge of the CLK and are stable after the specified time delay (TPD). Sequential read is possible when CS is held high. The memory data will automatically cycle to the next register and output sequentially.

FIGURE 3-7: READ TIMING



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3.8 WRITE

The WRITE instruction is followed by 8 bits (If ORG is low or A-version devices) or 16 bits (If ORG pin is high or B-version devices) of data which are written into the specified address. For 93AAXX and 93LCXX devices, after the last data bit is clocked into DI, the falling edge of CS initiates the self-timed auto-erase and programming cycle. For 93CXX devices, the self-timed auto-erase and programming cycle is initiated by the rising edge of CLK on the last data bit.

The DO pin indicates the Ready/$\overline{\text{Busy}}$ status of the device, if CS is brought high after a minimum of 250 ns low (TCSL). DO at logical '0' indicates that programming is still in progress. DO at logical '1' indicates that the register at the specified address has been written with the data specified and the device is ready for another instruction.

Note:	For devices with PE functionality such as the 93XX76C or 93XX86C, the write sequence requires a logic high signal on the PE pin prior to the rising edge of clock on the last data bit.

Note:	After the Write cycle is complete, issuing a Start bit and then taking CS low will clear the Ready/$\overline{\text{Busy}}$ status from DO.

FIGURE 3-8: WRITE TIMING FOR 93AAXX AND 93LCXX DEVICES

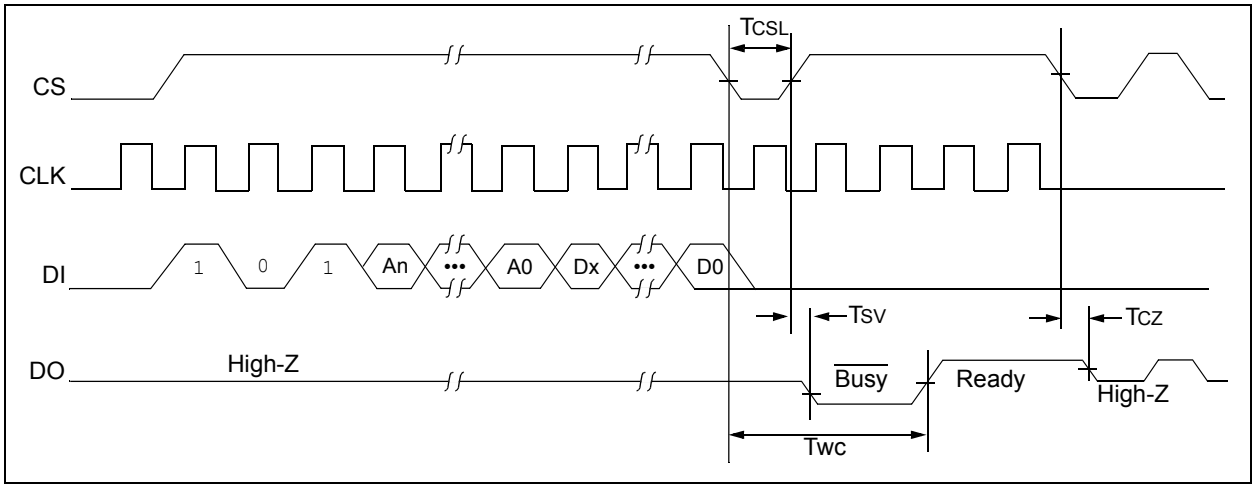
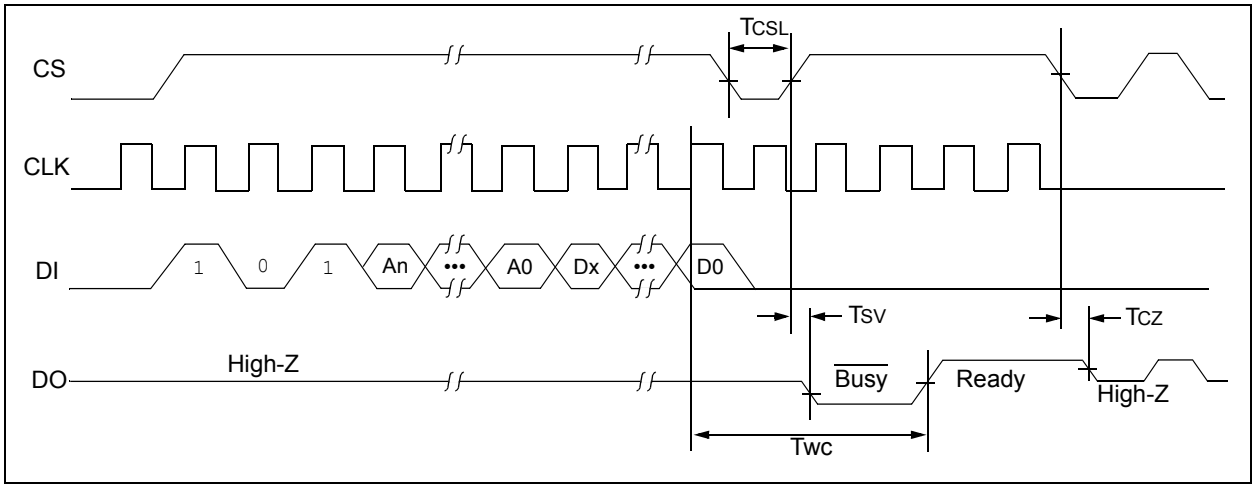


FIGURE 3-9: WRITE TIMING FOR 93CXX DEVICES



3.9 WRITE ALL (WRAL)

The Write All (WRAL) instruction will write the entire memory array with the data specified in the command. For 93AAXX and 93LCXX devices, after the last data bit is clocked into DI, the falling edge of CS initiates the self-timed auto-erase and programming cycle. For 93CXX devices, the self-timed auto-erase and programming cycle is initiated by the rising edge of CLK on the last data bit. Clocking of the CLK pin is not necessary after the device has entered the WRAL cycle. The WRAL command does include an automatic ERAL cycle for the device. Therefore, the WRAL instruction does not require an ERAL instruction, but the chip must be in the EWEN status.

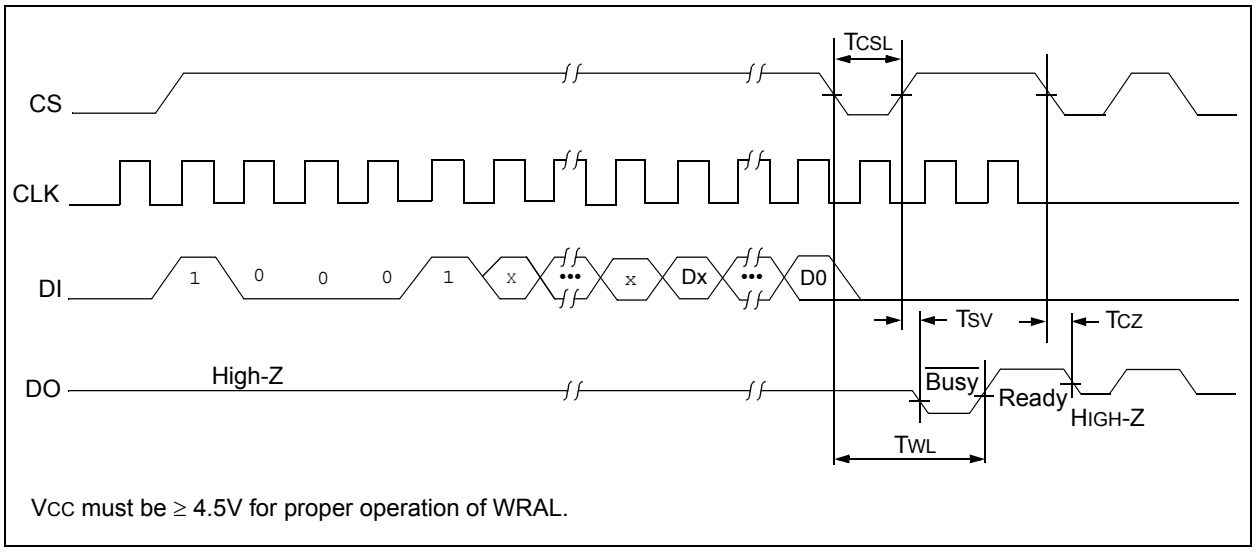
The DO pin indicates the Ready/$\overline{\text{Busy}}$ status of the device if CS is brought high after a minimum of 250 ns low (T_{CSL}).

V_{CC} must be ≥ 4.5V for proper operation of WRAL.

Note:	For devices with PE functionality such as the 93XX76C or 93XX86C, the write sequence requires a logic high signal on the PE pin prior to the rising edge of clock on the last data bit.

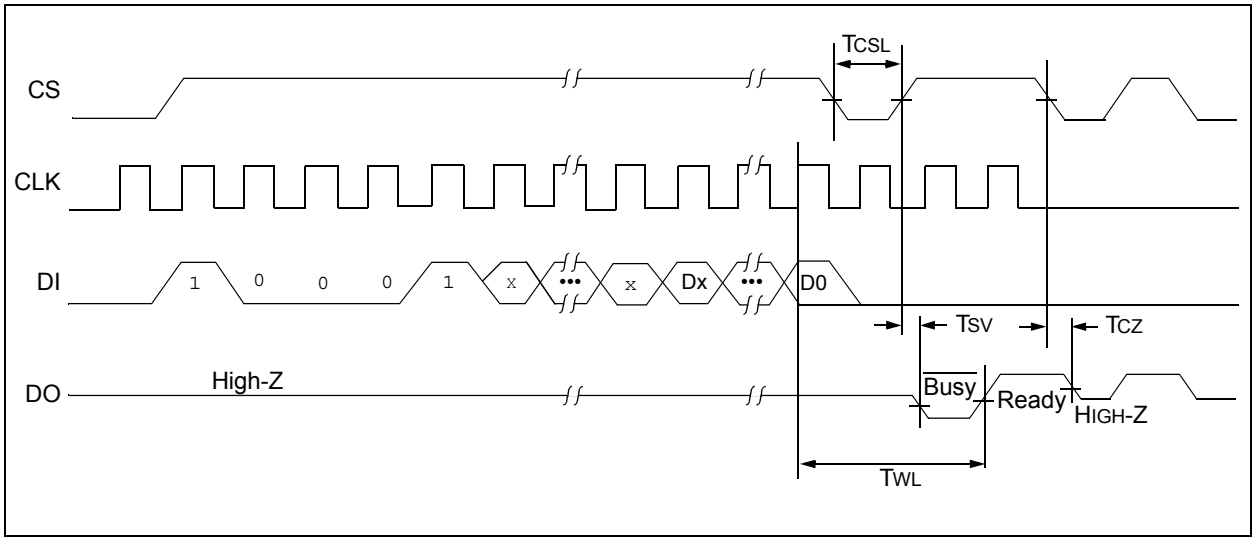
Note:	After the Write All cycle is complete, issuing a Start bit and then taking CS low will clear the Ready/$\overline{\text{Busy}}$ status from DO.

FIGURE 3-10: WRAL TIMING FOR 93AAXX AND 93LCXX DEVICES



V_{CC} must be ≥ 4.5V for proper operation of WRAL.

FIGURE 3-11: WRAL TIMING FOR 93CXX DEVICES



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4.0 PIN DESCRIPTIONS

TABLE 4-1: PIN DESCRIPTIONS

Name	SOIC/PDIP/MSOP/ TSSOP/DFN	SOT-23	Function
CS	1	5	Chip Select
CLK	2	4	Serial Clock
DI	3	3	Data In
DO	4	1	Data Out
VSS	5	2	Ground
ORG	6	N/A	Organization (93XX46C/56C/66C/76C/86C)
NC(1)			No connect on 93XXA/B devices
PE	7	N/A	Program Enable (93XX76C/86C)
NC(1)			No connect on 93XXA/B devices
VCC	8	6	Power Supply

Note 1: With no internal connection, logic levels on NC pins are “don’t cares.”

4.1 Chip Select (CS)

A high level selects the device; a low level deselects the device and forces it into Standby mode. However, a programming cycle which is already in progress will be completed, regardless of the Chip Select (CS) input signal. If CS is brought low during a program cycle, the device will go into Standby mode as soon as the programming cycle is completed.

CS must be low for 250 ns minimum (TCSL) between consecutive instructions. If CS is low, the internal control logic is held in a Reset status.

4.2 Serial Clock (CLK)

The Serial Clock is used to synchronize the communication between a master device and the 93XX series device. Opcodes, address and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at high or low level) and can be continued anytime with respect to Clock High Time (TCKH) and Clock Low Time (TCKL). This gives the controlling master freedom in preparing opcode, address and data.

CLK is a “don’t care” if CS is low (device deselected). If CS is high, but the Start condition has not been detected (DI = 0), any number of clock cycles can be received by the device without changing its status (i.e., waiting for a Start condition).

CLK cycles are not required during the self-timed Write (i.e., auto Erase/Write) cycle.

After detection of a Start condition the specified number of clock cycles (respectively low-to-high transitions of CLK) must be provided. These clock cycles are required to clock in all required opcode, address and data bits before an instruction is executed. CLK and DI then become “don’t care” inputs waiting for a new Start condition to be detected.

4.3 Data In (DI)

Data In (DI) is used to clock in a Start bit, opcode, address and data synchronously with the CLK input.

4.4 Data Out (DO)

Data Out (DO) is used in the Read mode to output data synchronously with the CLK input (TPD after the positive edge of CLK).

This pin also provides Ready/$\overline{\text{Busy}}$ status information during Erase and Write cycles. Ready/$\overline{\text{Busy}}$ status information is available on the DO pin if CS is brought high after being low for minimum Chip Select Low Time (TCSL) and an erase or write operation has been initiated.

The Status signal is not available on DO, if CS is held low during the entire Erase or Write cycle. In this case, DO is in the High-Z mode. If status is checked after the Erase/Write cycle, the data line will be high to indicate the device is ready.

Note:	After the Read cycle is complete, issuing a Start bit and then taking CS low will clear the Ready/$\overline{\text{Busy}}$ status from DO.

4.5 Organization (ORG)

When the ORG pin is connected to VCC or Logic HI, the (x16) memory organization is selected. When the ORG pin is tied to VSS or Logic LO, the (x8) memory organization is selected. For proper operation, ORG must be tied to a valid logic level.

For devices without the ORG functionality, there is no internal connection to the ORG pin. In these devices the functionality has been set at the factory to support a single word size.

'A' series devices – x8 organization

'B' series devices – x16 organization

4.6 Program Enable (PE)

A logic level on the PE pin will enable or disable the ability to write data to the memory array in only the 8-lead 93XX76C and 93XX86C devices. For all other devices the PE function is not present and the PE pin is a no connect. When driving the PE pin to a logic High, the device can be programmed, but when the PE pin is driven Low, programming is inhibited. This pin is used in parallel with the EWEN/EWDS latch to protect the memory array from inadvertent writes, as shown in Table 4-2.

In either the 93XX76C or 93XX86C devices, the PE pin must be tied to a specific logic level and cannot be floated. In all other devices without the PE function, the PE pin has no internal connections and programming is always enabled.

TABLE 4-2: WRITE PROTECTION SCHEME

EWEN/EWDS Latch	PE Pin*	Array WRITE
Enabled	1	Yes
Disabled	1	No
Enabled	0	No
Disabled	0	No

* PE pin level does not alter the state of the EWEN/EWDS latch.

Note: For devices with PE functionality such as 93XX76C or 93XX86C, the write sequence requires a logic high signal on the PE pin prior to the rising edge of clock on the last data bit.

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APPENDIX A: REVISION HISTORY

Revision A

Original release of document. Combined all the 93-Series Microwire Serial EEPROM device data sheets.

Revision B

Revised 2x3 (MC) DFN package drawing.

Revision C

Correction to Table 2-6, 93XX76A (EWDS).

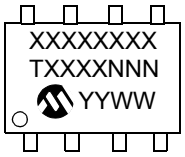
Revision D (03/2007)

Revised Description; Delete Pb-free notes; Replaced Package Drawings; Revised Product ID System.

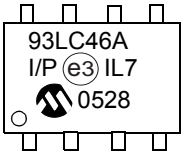
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

8-Lead PDIP



Example: Pb-free



3-Wire 8-Lead PDIP Package Marking					
Part	**Line 1 Marking**	**Part**	**Line 1 Marking**	**Part**	**Line 1 Marking**
93AA46A	93AA46A	93LC46A	93LC46A	93C46A	93C46A
93AA46B	93AA46B	93LC46B	93LC46B	93C46B	93C46B
93AA46C	93AA46C	93LC46C	93LC46C	93C46C	93C46C
93AA56A	93AA56A	93LC56A	93LC56A	93C56A	93C56A
93AA56B	93AA56B	93LC56B	93LC56B	93C56B	93C56B
93AA56C	93AA56C	93LC56C	93LC56C	93C56C	93C56C
93AA66A	93AA66A	93LC66A	93LC66A	93C66A	93C66A
93AA66B	93AA66B	93LC66B	93LC66B	93C66B	93C66B
93AA66C	93AA66C	93LC66C	93LC66C	93C66C	93C66C
93AA76A	93AA76A	93LC76A	93LC76A	93C76A	93C76A
93AA76B	93AA76B	93LC76B	93LC76B	93C76B	93C76B
93AA76C	93AA76C	93LC76C	93LC76C	93C76C	93C76C
93AA86A	93AA86A	93LC86A	93LC86A	93C86A	93C86A
93AA86B	93AA86B	93LC86B	93LC86B	93C86B	93C86B
93AA86C	93AA86C	93LC86C	93LC86C	93C86C	93C86C

Note: Temperature range on second line.

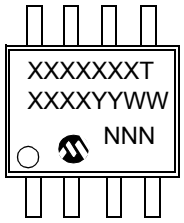
Legend:	XX...X	Part number or part number code
	T	Temperature (I, E)
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code (2 characters for small packages)
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)

Note: For very small packages with no room for the Pb-free JEDEC designator (e3), the marking will only appear on the outer carton or reel label.

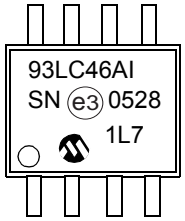
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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8-Lead SOIC



Example: Pb-free



3-Wire 8-Lead SOIC (SN) Package Marking					
Part	**Line 1 Marking**	**Part**	**Line 1 Marking**	**Part**	**Line 1 Marking**
93AA46A	93AA46AT	93LC46A	93LC46AT	93C46A	93C46AT
93AA46B	93AA46BT	93LC46B	93LC46BT	93C46B	93C46BT
93AA46C	93AA46CT	93LC46C	93LC46CT	93C46C	93C46CT
93AA56A	93AA56AT	93LC56A	93LC56AT	93C56A	93C56AT
93AA56B	93AA56BT	93LC56B	93LC56BT	93C56B	93C56BT
93AA56C	93AA56CT	93LC56C	93LC56CT	93C56C	93C56CT
93AA66A	93AA66AT	93LC66A	93LC66AT	93C66A	93C66AT
93AA66B	93AA66BT	93LC66B	93LC66BT	93C66B	93C66BT
93AA66C	93AA66CT	93LC66C	93LC66CT	93C66C	93C66CT
93AA76A	93AA76AT	93LC76A	93LC76AT	93C76A	93C76AT
93AA76B	93AA76BT	93LC76B	93LC76BT	93C76B	93C76BT
93AA76C	93AA76CT	93LC76C	93LC76CT	93C76C	93C76CT
93AA86A	93AA86AT	93LC86A	93LC86AT	93C86A	93C86AT
93AA86B	93AA86BT	93LC86B	93LC86BT	93C86B	93C86BT
93AA86C	93AA86CT	93LC86C	93LC86CT	93C86C	93C86CT

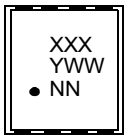
Note: T = Temperature Range: I = Industrial, E = Extended

Legend:	XX...X	Part number or part number code
	T	Temperature (I, E)
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code (2 characters for small packages)
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)

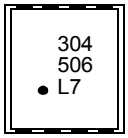
Note: For very small packages with no room for the Pb-free JEDEC designator (e3), the marking will only appear on the outer carton or reel label.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead 2x3 DFN



Example:



3-Wire 2x3 DFN Package Marking								
Part	**Industrial Line 1 Marking**	**E-Temp Line 1 Marking**	**Part**	**Industrial Line 1 Marking**	**E-Temp Line 1 Marking**	**Part**	**Industrial Line 1 Marking**	**E-Temp Line 1 Marking**
93AA46A	301	302	93LC46A	304	305	93C46A	307	308
93AA46B	311	312	93LC46B	314	315	93C46B	317	318
93AA46C	321	322	93LC46C	324	325	93C46C	327	328
93AA56A	331	332	93LC56A	334	335	93C56A	337	338
93AA56B	341	342	93LC56B	344	345	93C56B	347	348
93AA56C	351	352	93LC56C	354	355	93C56C	357	358
93AA66A	361	362	93LC66A	364	365	93C66A	367	368
93AA66B	371	372	93LC66B	374	375	93C66B	377	378
93AA66C	381	382	93LC66C	384	385	93C66C	387	388
93AA76C	3B1	3B2	93LC76C	3B4	3B5	93C76C	3B7	3B8
93AA86C	3E1	3E2	93LC86C	3E4	3E5	93C86C	3E7	3E8

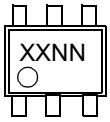
Legend:	XX...X	Part number or part number code
	T	Temperature (I, E)
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code (2 characters for small packages)
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)

Note: For very small packages with no room for the Pb-free JEDEC designator (e3), the marking will only appear on the outer carton or reel label.

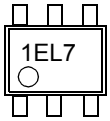
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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6-Lead SOT-23



Example:



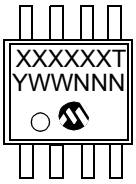
3-Wire 6-Lead SOT-23 Package Marking								
Part	**Industrial Line 1 Marking**	**E-Temp Line 1 Marking**	**Part**	**Industrial Line 1 Marking**	**E-Temp Line 1 Marking**	**Part**	**Industrial Line 1 Marking**	**E-Temp Line 1 Marking**
93AA46A	1BNN	1CNN	93LC46A	1ENN	1FNN	93C46A	1HNN	1JNN
93AA46B	1LNN	1MNN	93LC46B	1PNN	1RNN	93C46B	1TNN	1UNN
93AA56A	2BNN	2CNN	93LC56A	2ENN	2FNN	93C56A	2HNN	2JNN
93AA56B	2LNN	2MNN	93LC56B	2PNN	2RNN	93C56B	2TNN	2UNN
93AA66A	3BNN	3CNN	93LC66A	3ENN	3FNN	93C66A	3HNN	3JNN
93AA66B	3LNN	3MNN	93LC66B	3PNN	3RNN	93C66B	3TNN	3UNN
93AA76A	4BNN	4CNN	93LC76A	4ENN	4FNN	93C76A	4HNN	4JNN
93AA76B	4LNN	4MNN	93LC76B	4PNN	4RNN	93C76B	4TNN	4UNN
93AA86A	5BNN	5CNN	93LC86A	5ENN	5FNN	93C86A	5HNN	5JNN
93AA86B	5LNN	5MNN	93LC86B	5PNN	5RNN	93C86B	5TNN	5UNN

Legend:	XX...X	Part number or part number code
	T	Temperature (I, E)
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code (2 characters for small packages)
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)

Note: For very small packages with no room for the Pb-free JEDEC designator (e3), the marking will only appear on the outer carton or reel label.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead MSOP (150 mil)



Example:



3-Wire 8-Lead MSOP Package Marking					
Part	**Line 1 Marking**	**Part**	**Line 1 Marking**	**Part**	**Line 1 Marking**
93AA46A	3A46AT	93LC46A	3L46AT	93C46A	3C46AT
93AA46B	3A46BT	93LC46B	3L46BT	93C46B	3C46BT
93AA46C	3A46CT	93LC46C	3L46CT	93C46C	3C46CT
93AA56A	3A56AT	93LC56A	3L56AT	93C56A	3C56AT
93AA56B	3A56BT	93LC56B	3L56BT	93C56B	3C56BT
93AA56C	3A56CT	93LC56C	3L56CT	93C56C	3C56CT
93AA66A	3A66AT	93LC66A	3L66AT	93C66A	3C66AT
93AA66B	3A66BT	93LC66B	3L66BT	93C66B	3C66BT
93AA66C	3A66CT	93LC66C	3L66CT	93C66C	3C66CT
93AA76A	3A76AT	93LC76A	3L76AT	93C76A	3C76AT
93AA76B	3A76BT	93LC76B	3L76BT	93C76B	3C76BT
93AA76C	3A76CT	93LC76C	3L76CT	93C76C	3C76CT
93AA86A	3A86AT	93LC86A	3L86AT	93C86A	3C86AT
93AA86B	3A86BT	93LC86B	3L86BT	93C86B	3C86BT
93AA86C	3A86CT	93LC86C	3L86CT	93C86C	3C86CT

Note: T = Temperature Range: I = Industrial, E = Extended

Legend:	XX...X	Part number or part number code
	T	Temperature (I, E)
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code (2 characters for small packages)
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)

Note: For very small packages with no room for the Pb-free JEDEC designator (e3), the marking will only appear on the outer carton or reel label.

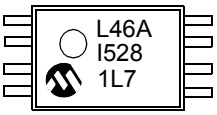
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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8-Lead TSSOP



Example:



3-Wire 8-Lead TSSOP Package Marking					
Part	**Line 1 Marking**	**Part**	**Line 1 Marking**	**Part**	**Line 1 Marking**
93AA46A	A46A	93LC46A	L46A	93C46A	C46A
93AA46B	A46B	93LC46B	L46B	93C46B	C46B
93AA46C	A46C	93LC46C	L46C	93C46C	C46C
93AA56A	A56A	93LC56A	L56A	93C56A	C56A
93AA56B	A56B	93LC56B	L56B	93C56B	C56B
93AA56C	A56C	93LC56C	L56C	93C56C	C56C
93AA66A	A66A	93LC66A	L66A	93C66A	C66A
93AA66B	A66B	93LC66B	L66B	93C66B	C66B
93AA66C	A66C	93LC66C	L66C	93C66C	C66C
93AA76A	A76A	93LC76A	L76A	93C76A	C76A
93AA76B	A76B	93LC76B	L76B	93C76B	C76B
93AA76C	A76C	93LC76C	L76C	93C76C	C76C
93AA86A	A86A	93LC86A	L86A	93C86A	C86A
93AA86B	A86B	93LC86B	L86B	93C86B	C86B
93AA86C	A86C	93LC86C	L86C	93C86C	C86C

Note: Temperature range on second line.

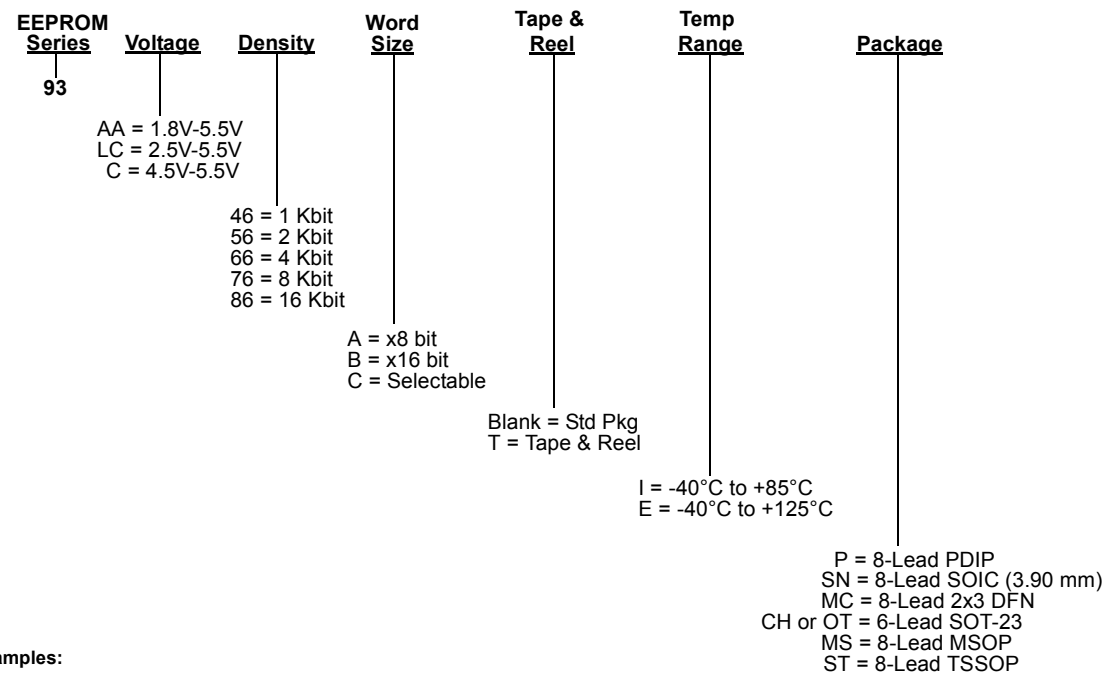
Legend:	XX...X	Part number or part number code
	T	Temperature (I, E)
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code (2 characters for small packages)
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)

Note: For very small packages with no room for the Pb-free JEDEC designator (e3), the marking will only appear on the outer carton or reel label.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Examples:

a) 93AA46A-I/MS: 1K, 128x8 Serial EEPROM, Industrial Temperature, MSOP package, 1.8V

b) 93AA46BT-I/OT: 1K, 64x16 Serial EEPROM, SOT-23 package, tape and reel, 1.8V

c) 93AA46CT-I/MS: 1K, 128x8 or 64x16 Serial EEPROM, MSOP package, tape and reel, 1.8V

d) 93AA46BX-I/SN: 1K, 128x8 Serial EEPROM, Industrial temperature, SOIC package (alternate pinout), tape and reel package, 1.8V

e) 93LC66A-I/MS: 4K, 512x8 Serial EEPROM, MSOP package, 2.5V

f) 93LC66BT-I/OT: 4K, 256x16 Serial EEPROM, SOT-23 package, tape and reel, 2.5V

g) 93C86AT-I/OT: 16K, 2048x8 Serial EEPROM, SOT-23 package, tape and reel, 5.0V

h) 93C86BT-I/OT: 16K, 1024x16 Serial EEPROM, SOT-23 package, tape and reel, 5.0V

i) 93C86CT-I/MC: 16K, 2048x8 or 1024x16 Serial EEPROM, DFN Industrial temperature, tape and reel package, 5.0V

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SPI Serial EEPROM Family Data Sheet

Features:

- Max Clock Speed
  - 10 MHz (1K-256K)
  - 20 MHz (512K-1M)
- Byte and Page-level Write Operations
- Low-power CMOS Technology
  - Typical Write current: 5 mA
  - Typical Read current: 5 mA @ 10 MHz
    7 mA @ 20 MHz
  - Typical Standby current: 1 μA
- Write Cycle Time: 5 ms max.
  6 ms max. (25XX1024)
- Self-timed Erase and Write Cycles
- Erase Functions (25XX512 and 25XX1024)
  - Page Erase: 6 ms max.
  - Sector Erase: 15 ms max.
  - Chip Erase: 15 ms max.
- Built-in Write Protection
  - Power on/off data protection circuitry
  - Write enable latch
  - Write-protect pin
- Block/Sector Write Protection
  - Protect none, 1/4, 1/2 or all of array
- Sequential Read
- High Reliability
  - Data retention: > 200 years
  - ESD protection: > 4000V
  - Endurance > 1M Erase/Write Cycles
- Available in Standard 8-pin and 6-pin Packages
- Temperature Ranges Supported:
  - Industrial (I): -40°C to +85°C
  - Automotive (E): -40°C to +125°C

Pin Function Table

Name	Function
$\overline{CS}$	Chip Select
SO	Serial Data Output
$\overline{WP}$	Write-Protect
VSS	Ground
SI	Serial Data Input
SCK	Serial Clock Input
$\overline{HOLD}$	Hold Input
VCC	Supply Voltage

Description:

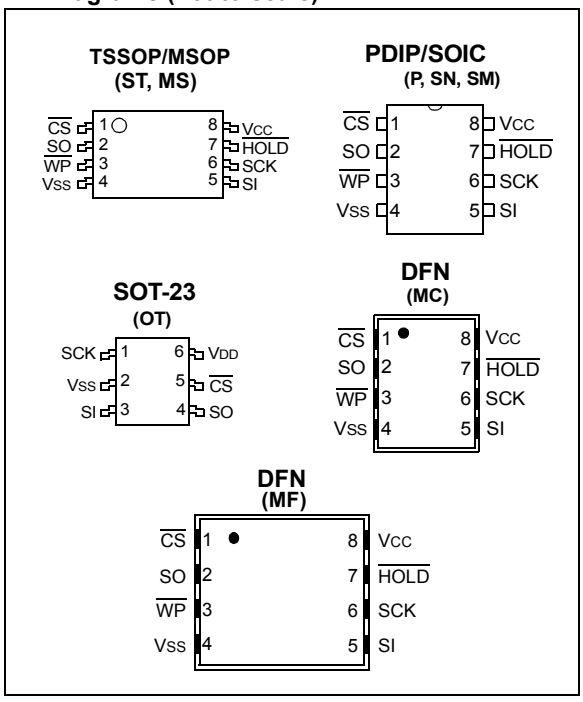
Microchip Technology Inc. supports the Serial Peripheral Interface (SPI) compatible serial bus architecture with low-voltage serial Electrically Erasable PROMs (EEPROM) that range in density from 1 Kbits up to 1 Mbits. Byte-level and page-level functions are supported, but the higher density 512 Kbit and 1 Mbit devices also feature Sector and Chip erase functions typically associated with Flash-based products.

The bus signals required are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a Chip Select ($\overline{CS}$) input.

Communication to the device can be paused via the hold pin ($\overline{HOLD}$). While the device is paused, transitions on its inputs will be ignored, with the exception of Chip Select, allowing the host to service higher priority interrupts.

The entire series of SPI compatible devices are available in the standard 8-lead PDIP and SOIC packages, as well as the more advanced packages such as the 8-lead TSSOP, MSOP, 2x3 DFN, 5x6 DFN and 6-lead SOT-23. All packages are RoHS compliant with a Pb-free (Matte Tin) finish.

Pin Diagrams (not to scale)



3 Family Data Sheets

DEVICE SELECTION TABLE

Part Number	Density (bits)	Organization	Vcc Range	Max Speed (MHz)	Page Size (Bytes)	Temp. Range	Packages
25LC010A	1K	128 x 8	2.5-5.5V	10	16	I, E	P, MS, SN, ST, MC, OT
25AA010A	1K	128 x 8	1.8-5.5V	10	16	I	P, MS, SN, ST, MC, OT
25LC020A	2K	256 x 8	2.5-5.5V	10	16	I, E	P, MS, SN, ST, MC, OT
25AA020A	2K	256 x 8	1.8-5.5V	10	16	I	P, MS, SN, ST, MC, OT
25LC040A	4K	512 x 8	2.5-5.5V	10	16	I, E	P, MS, SN, ST, MC, OT
25AA040A	4K	512 x 8	1.8-5.5V	10	16	I	P, MS, SN, ST, MC, OT
25LC080A	8K	1024 x 8	2.5-5.5V	10	16	I, E	P, MS, SN, ST
25AA080A	8K	1024 x 8	1.8-5.5V	10	16	I	P, MS, SN, ST
25LC080B	8K	1024 x 8	2.5-5.5V	10	32	I, E	P, MS, SN, ST
25AA080B	8K	1024 x 8	1.8-5.5V	10	32	I	P, MS, SN, ST
25LC160A	16K	2048 x 8	2.5-5.5V	10	16	I, E	P, MS, SN, ST
25AA160A	16K	2048 x 8	1.8-5.5V	10	16	I	P, MS, SN, ST
25LC160B	16K	2048 x 8	2.5-5.5V	10	32	I, E	P, MS, SN, ST
25AA160B	16K	2048 x 8	1.8-5.5V	10	32	I	P, MS, SN, ST
25LC320A	32K	4096 x 8	2.5-5.5V	10	32	I, E	P, MS, SN, ST
25AA320A	32K	4096 x 8	1.8-5.5V	10	32	I	P, MS, SN, ST
25LC640A	64K	8192 x 8	2.5-5.5V	10	32	I, E	P, MS, SN, ST
25AA640A	64K	8192 x 8	1.8-5.5V	10	32	I	P, MS, SN, ST
25LC128	128K	16,384 x 8	2.5-5.5V	10	64	I, E	P, SN, SM, ST, MF
25AA128	128K	16,384 x 8	1.8-5.5V	10	64	I	P, SN, SM, ST, MF
25LC256	256K	32,768 x 8	2.5-5.5V	10	64	I, E	P, SN, SM, ST, MF
25AA256	256K	32,768 x 8	1.8-5.5V	10	64	I	P, SN, SM, ST, MF
25LC512	512K	65,536 x 8	2.5-5.5V	20	128	I, E	P, SM, MF
25AA512	512K	65,536 x 8	1.8-5.5V	20	128	I	P, SM, MF
25LC1024	1024K	131,072 x 8	2.5-5.5V	20	256	I, E	P, SM, MF
25AA1024	1024K	131,072 x 8	1.8-5.5V	20	256	I	P, SM, MF

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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (†)

VCC.....6.5V

All inputs and outputs w.r.t. VSS .....-0.6V to VCC +1.0V

Storage temperature .....-65°C to +150°C

Ambient temperature under bias.....-40°C to +125°C

ESD protection on all pins.....4 kV

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note: This is an overview of AC and DC Characteristics. Please refer to the device data sheet for production specs.

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS			**Electrical Characteristics:** Industrial (I): VCC = +1.8V to 5.5V TA = -40°C to +85°C Automotive (E): VCC = +2.5V to 5.5V TA = -40°C to 125°C				
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Test Conditions**	**Densities**
D001	VIH	High-level input voltage	.7 VCC	VCC + 1	V		All
D002	VIL	Low-level input voltage	-0.3	0.3 VCC	V	VCC ≥ 2.7V **(Note 1)**	All
D003	VIL		-0.3	0.2 VCC	V	VCC ≥ 2.7V **(Note 1)**	All
D004	VOL	Low-level output voltage	—	0.4	V	IOL = 2.1 mA, VCC = 4.5V	All
D005	VOL		—	0.2	V	IOL = 1.0 mA, VCC = 2.5V	All
D006	VOH	High-level output voltage	VCC -0.5	—	V	IOH = -400 µA	All
D007	ILI	Input leakage current	—	±1	µA	$\overline{CS}$ = VCC, VIN = VSS or VCC	All
D008	ILO	Output leakage current	—	±1	µA	$\overline{CS}$ = VCC, VOUT = VSS or VCC	All
D009	CINT	Internal capacitance (all inputs and outputs)	—	7	pF	TA = 25°C, CLK = 1.0 MHz, VCC = 5.0V **(NOTE 1)**	All
D010	ICC Read	Operating current	—	10 5	mA	VCC = 5.5V; FCLK = 20.0 MHz; Vcc = 2.5V; FCLK = 10.0 MHz	512K and 1M
			2.5 0.5	6 2.5	mA	VCC = 5.5V; FCLK = 10.0 MHz; Vcc = 2.5V; FCLK = 5.0 MHz	1K-256K
D011	ICC WRITE		—	7 5	mA	VCC = 5.5V Vcc = 2.5V	512K and 1M
			0.16 0.15	5 3	mA	VCC = 5.5V VCC = 2.5V	1K-256K
D012	ICCS	Standby current	—	20 12	µA	$\overline{CS}$ = VCC = 5.5V, 125°C $\overline{CS}$ = VCC = 5.5V, 85°C (Inputs tied to VCC or VSS)	512K and 1M
			—	5 1	µA	$\overline{CS}$ = VCC = 5.5V, 125°C $\overline{CS}$ = VCC = 5.5V, 85°C (Inputs tied to VCC or VSS)	1K-256K
D13	ICCSPD	Deep power-down current	—	1	µA	$\overline{CS}$ = VCC = 5.5V (Inputs tied to VCC or VSS)	512K and 1M

Note 1: This parameter is periodically sampled and not 100% tested.

TABLE 1-2: AC CHARACTERISTICS

AC CHARACTERISTICS			Electrical Characteristics: Industrial (I): VCC = +1.8V to 5.5V TA = -40°C to +85°C Automotive (E): VCC = +2.5V to 5.5V TA = -40°C to 125°C				
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**	**Densities**
1	FCLK	Clock frequency	— — —	20 10 2	MHz	4.5 ≤ VCC ≤ 5.5 2.5 ≤ VCC < 4.5 1.8 ≤ VCC < 2.5	512K and 1M
			— — —	10 5 3	MHz	4.5 ≤ VCC ≤ 5.5 2.5 ≤ VCC < 4.5 1.8 ≤ VCC < 2.5	1K-256K
2	TCSS	$\overline{CS}$ setup time	25 50 250		ns ns ns	4.5 ≤ VCC ≤ 5.5 2.5 ≤ VCC < 4.5 1.8 ≤ VCC < 2.5	512K and 1M
			50 100 150	— — —	ns ns ns	4.5 ≤ VCC ≤ 5.5 2.5 ≤ VCC < 4.5 1.8 ≤ VCC < 2.5	1K-256K
3	TCSH	$\overline{CS}$ hold time **(Note 3)**	50 100 150		ns ns ns	4.5 ≤ VCC ≤ 5.5 2.5 ≤ VCC < 4.5 1.8 ≤ VCC < 2.5	512K and 1M
			100 200 250	— — —	ns ns ns	4.5 ≤ VCC ≤ 5.5 2.5 ≤ VCC < 4.5 1.8 ≤ VCC < 2.5	1K-256K
4	TCSD	$\overline{CS}$ disable time	50	—	ns		1K-256K
5	TSU	Data setup time	5 10 50	—	ns ns ns	4.5 ≤ VCC ≤ 5.5 2.5 ≤ VCC < 4.5 1.8 ≤ VCC < 2.5	512K and 1M
			10 20 30	— — —	ns ns ns	4.5 ≤ VCC ≤ 5.5 2.5 ≤ VCC < 4.5 1.8 ≤ VCC < 2.5	1K-256K
6	THD	Data hold time	10 20 100		ns ns ns	4.5 ≤ VCC ≤ 5.5 2.5 ≤ VCC < 4.5 1.8 ≤ VCC < 2.5	512K and 1M
			20 40 50	— — —	ns ns ns	4.5 ≤ VCC ≤ 5.5 2.5 ≤ VCC < 4.5 1.8 ≤ VCC < 2.5	1K-256K
7	TR	CLK rise time **(Note 1)**	—	20	ns		512K and 1M
			—	100	ns		128K and 256K
			—	500	ns		8K and 16K
			—	2000	ns		1K-4K, 32K-64K
8	TF	CLK fall time **(Note 1)**	—	20	ns		512K and 1M
			—	100	ns		128K and 256K
			—	500	ns		8K and 16K
			—	2000	ns		1K-4K, 32K-64K

Note 1: This parameter is periodically sampled and not 100% tested.

2: This parameter is not tested but established by characterization and qualification. For endurance estimates in a specific application, please consult the Total Endurance™ Model, which can be obtained from Microchip's web site: www.microchip.com.

3: Includes THI time.

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TABLE 1-2: AC CHARACTERISTICS (CONTINUED)

AC CHARACTERISTICS			Electrical Characteristics: Industrial (I): VCC = +1.8V to 5.5V TA = -40°C to +85°C Automotive (E): VCC = +2.5V to 5.5V TA = -40°C to 125°C				
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**	**Densities**
9	THI	Clock high time	25 50 250	—	ns ns ns	4.5 ≤ VCC ≤ 5.5 2.5 ≤ VCC < 4.5 1.8 ≤ VCC < 2.5	512K and 1M
			50 100 150	—	ns ns ns	4.5 ≤ VCC ≤ 5.5 2.5 ≤ VCC < 4.5 1.8 ≤ VCC < 2.5	1K-256K
10	TLO	Clock low time	25 50 250	—	ns ns ns	4.5 ≤ VCC ≤ 5.5 2.5 ≤ VCC < 4.5 1.8 ≤ VCC < 2.5	512K and 1M
			50 100 150	—	ns ns ns	4.5 ≤ VCC ≤ 5.5 2.5 ≤ VCC < 4.5 1.8 ≤ VCC < 2.5	1K-256K
11	TCLD	Clock delay time	50	—	ns		All
12	TCLE	Clock enable time	50	—	ns		All
13	TV	Output valid from clock low	—	25 50 250	ns ns ns	4.5 ≤ VCC ≤ 5.5 2.5 ≤ VCC < 4.5 1.8 ≤ VCC < 2.5	512K and 1M
			—	50 100 160	ns ns ns	4.5 ≤ VCC ≤ 5.5 2.5 ≤ VCC < 4.5 1.8 ≤ VCC < 2.5	1K-256K
14	THO	Output hold time **(Note 1)**	0	—	ns		
15	TDIS	Output disable time **(Note 1)**	—	25 50 250	ns ns ns	4.5 ≤ VCC ≤ 5.5 2.5 ≤ VCC < 4.5 1.8 ≤ VCC < 2.5	512K and 1M
			—	40 80 160	ns ns ns	4.5 ≤ VCC ≤ 5.5 2.5 ≤ VCC < 4.5 1.8 ≤ VCC < 2.5	1K-256K
16	THS	$\overline{HOLD}$ setup time	10 20 100	—	ns ns ns	4.5 ≤ VCC ≤ 5.5 2.5 ≤ VCC < 4.5 1.8 ≤ VCC < 2.5	512K and 1M
			20 40 80	—	ns ns ns	4.5 ≤ VCC ≤ 5.5 2.5 ≤ VCC < 4.5 1.8 ≤ VCC < 2.5	1K-256K
17	THH	$\overline{HOLD}$ Hold time	10 20 100	—	ns ns ns	4.5 ≤ VCC ≤ 5.5 2.5 ≤ VCC < 4.5 1.8 ≤ VCC < 2.5	512K and 1M
			20 40 80	—	ns ns ns	4.5 ≤ VCC ≤ 5.5 2.5 ≤ VCC < 4.5 1.8 ≤ VCC < 2.5	1K-256K

Note 1: This parameter is periodically sampled and not 100% tested.

2: This parameter is not tested but established by characterization and qualification. For endurance estimates in a specific application, please consult the Total Endurance™ Model, which can be obtained from Microchip's web site: www.microchip.com.

3: Includes THI time.

TABLE 1-2: AC CHARACTERISTICS (CONTINUED)

AC CHARACTERISTICS			Electrical Characteristics: Industrial (I): VCC = +1.8V to 5.5V TA = -40°C to +85°C Automotive (E): VCC = +2.5V to 5.5V TA = -40°C to 125°C				
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**	**Densities**
18	THZ	$\overline{HOLD}$ low to output High-Z **(Note 1)**	15 30 150	—	ns ns ns	4.5 ≤ VCC ≤ 5.5 2.5 ≤ VCC < 4.5 1.8 ≤ VCC < 2.5	512K and 1M
			30 60 160	—	ns ns ns	4.5 ≤ VCC ≤ 5.5 2.5 ≤ VCC < 4.5 1.8 ≤ VCC < 2.5	1K-256K
19	THV	$\overline{HOLD}$ high to output valid	15 30 150	—	ns ns ns	4.5 ≤ VCC ≤ 5.5 2.5 ≤ VCC < 4.5 1.8 ≤ VCC < 2.5	512K and 1M
			30 60 160	—	ns ns ns	4.5 ≤ VCC ≤ 5.5 2.5 ≤ VCC < 4.5 1.8 ≤ VCC < 2.5	1K-256K
20	TREL	$\overline{CS}$ high to Standby mode	—	100	µs	1.8V ≤ VCC ≥ 5.5V	512K and 1M
21	TPD	$\overline{CS}$ high to Deep power-down	—	100	µs	1.8V ≤ VCC ≥ 5.5V	512K and 1M
22	TCE	Chip erase cycle time	—	15	ms	1.8V ≤ VCC ≥ 5.5V	512K and 1M
23	TSE	Sector erase cycle time	—	15	ms	1.8V ≤ VCC ≥ 5.5V	512K and 1M
24	TWC	Internal write cycle time	—	6	ms	Byte or Page mode and Page Erase	512K and 1M
			—	5	ms	Byte or Page mode	1K-256K
25	—	Endurance **(Note 2)**	> 1M	—	E/W Cycles	Per Page	512K and 1M
						Per Byte	1K-256K

Note 1: This parameter is periodically sampled and not 100% tested.

2: This parameter is not tested but established by characterization and qualification. For endurance estimates in a specific application, please consult the Total Endurance™ Model, which can be obtained from Microchip's web site: www.microchip.com.

3: Includes THI time.

TABLE 1-3: AC TEST CONDITIONS

AC Waveform:	
VLO = 0.2V	—
VHI = VCC - 0.2V	**(Note 1)**
VHI = 4.0V	**(Note 2)**
CL = 30 pF	—
Timing Measurement Reference Level	
Input Output	0.5 VCC 0.5 VCC

Note 1: For VCC ≤ 4.0V.

2: For VCC > 4.0V.

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FIGURE 1-1: HOLD TIMING

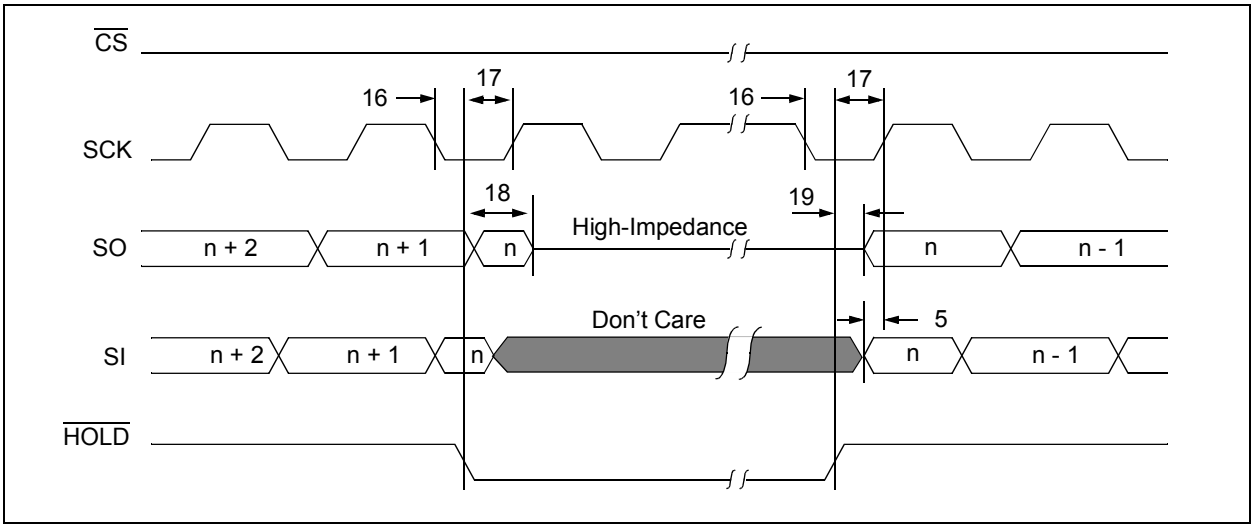


FIGURE 1-2: SERIAL INPUT TIMING

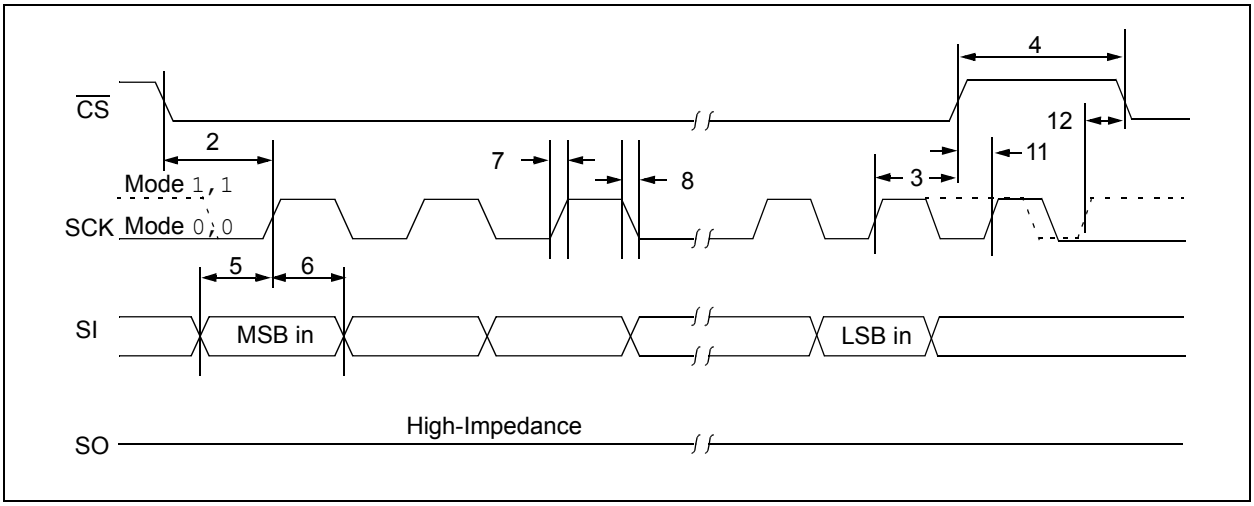
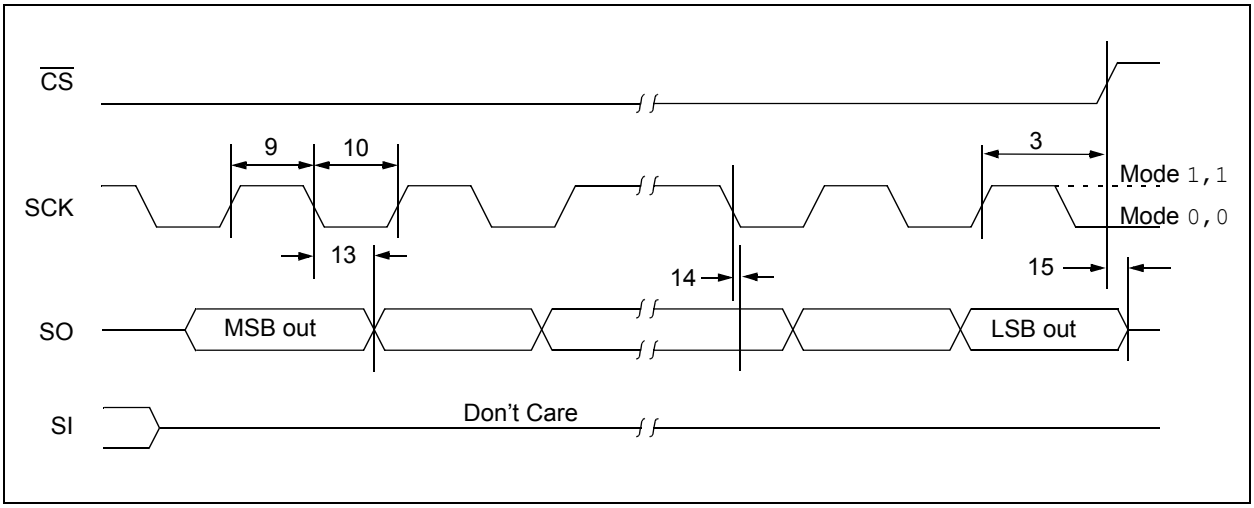


FIGURE 1-3: SERIAL OUTPUT TIMING



2.0 FUNCTIONAL DESCRIPTION

2.1 Principles of Operation

The 25-Series of Serial EEPROMs is designed to interface directly with the Serial Peripheral Interface (SPI) port of many of today's popular microcontroller families, including Microchip's PIC® microcontrollers. It may also interface with microcontrollers that do not have a built-in SPI port by using discrete I/O lines programmed properly in firmware to match the SPI protocol.

This family of EEPROMs contains an 8-bit instruction register. The device is accessed via the SI pin, with data being clocked in on the rising edge of SCK. The $\overline{CS}$ pin must be low and the $\overline{HOLD}$ pin must be high for the entire operation.

Table 2-1 contains a list of the possible instruction bytes and format for device operation. All instructions, addresses and data are transferred MSB first, LSB last.

Data (SI) is sampled on the first rising edge of SCK after $\overline{CS}$ goes low. If the clock line is shared with other peripheral devices on the SPI bus, the user can assert the $\overline{HOLD}$ input and place the EEPROM in 'HOLD' mode. After releasing the $\overline{HOLD}$ pin, operation will resume from the point when the $\overline{HOLD}$ was asserted.

Block Diagram

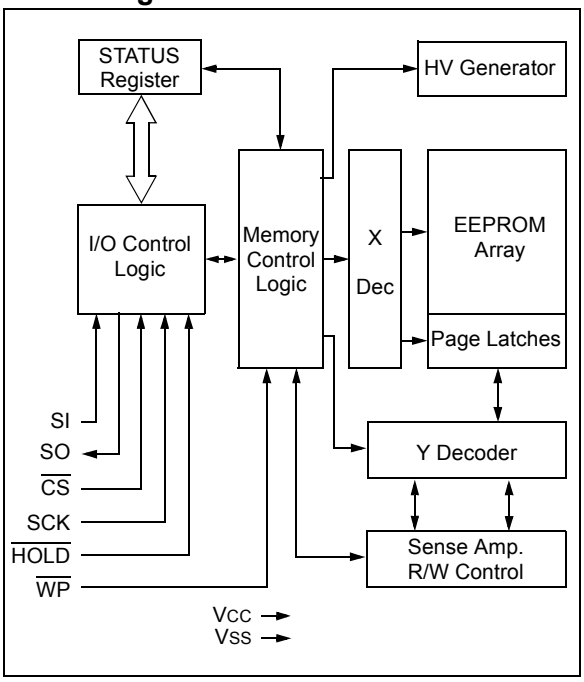


TABLE 2-1: INSTRUCTION SET

Instruction Name	Instruction Format	Description
Instructions for all devices.		
READ	0000 0011	Read data from memory array beginning at selected address
WRITE	0000 0010	Write data to memory array beginning at selected address
WREN	0000 0110	Set the write enable latch (enable write operations)
WRDI	0000 0100	Reset the write enable latch (disable write operations)
RDSR	0000 0101	Read STATUS register
WRSR	0000 0001	Write STATUS register
Additional Instructions for 25XX512 and 25XX1024		
PE	0100 0010	Page Erase – erase one page in memory array
SE	1101 1000	Sector Erase – erase one sector in memory array
CE	1100 0111	Chip Erase – erase all sectors in memory array
RDID	1010 1011	Release from Deep power-down and read electronic signature
DPD	1011 1001	Deep Power-Down mode

2.2 Read Sequence

The device is selected by pulling $\overline{CS}$ low. The 8-bit READ instruction is transmitted to the EEPROM followed by the address. After the correct READ instruction and address are sent, the data stored in the memory at the selected address is shifted out on the SO pin. The data stored in the memory at the next address can be read sequentially by continuing to provide clock pulses.

The internal Address Pointer is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached, the address counter rolls over to address 00000h, allowing the read cycle to be continued indefinitely. The read operation is terminated by raising the $\overline{CS}$ pin. See Figure 2-1A/B/C for byte read.

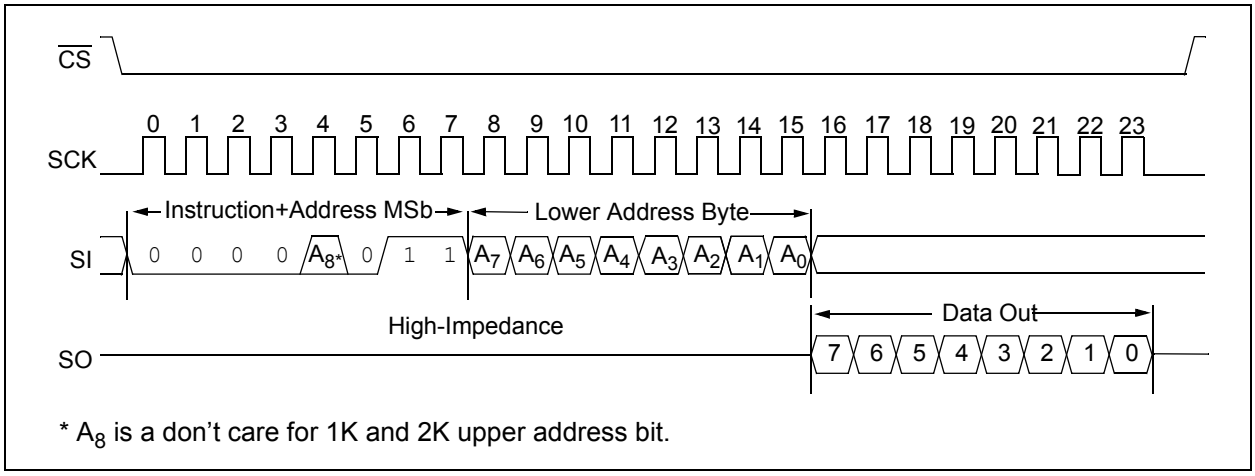
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TABLE 2-2: READ/WRITE SEQUENCE ADDRESSING

Density	Address Bits	Highest Address	Page Size
1K	7	007F	16 Bytes
2K	8	00FF	16 Bytes
4K	9	01FF	16 Bytes
8K	10	03FF	16 or 32 Bytes*
16K	11	07FF	16 or 32 Bytes*
32K	12	0FFF	32 Bytes
64K	12	1FFF	32 Bytes
128K	14	3FFF	64 Bytes
256K	15	7FFF	64 Bytes
512K	16	FFFF	256 Bytes
1024K	17	1FFFF	256 Bytes

Note: Version A – 16 Bytes
Version B – 32 Bytes

FIGURE 2-1A: READ SEQUENCE WITH EITHER 8-BIT OR 9-BIT ADDRESSING



* A_8 is a don't care for 1K and 2K upper address bit.

FIGURE 2-1B: READ SEQUENCE WITH 16-BIT ADDRESSING

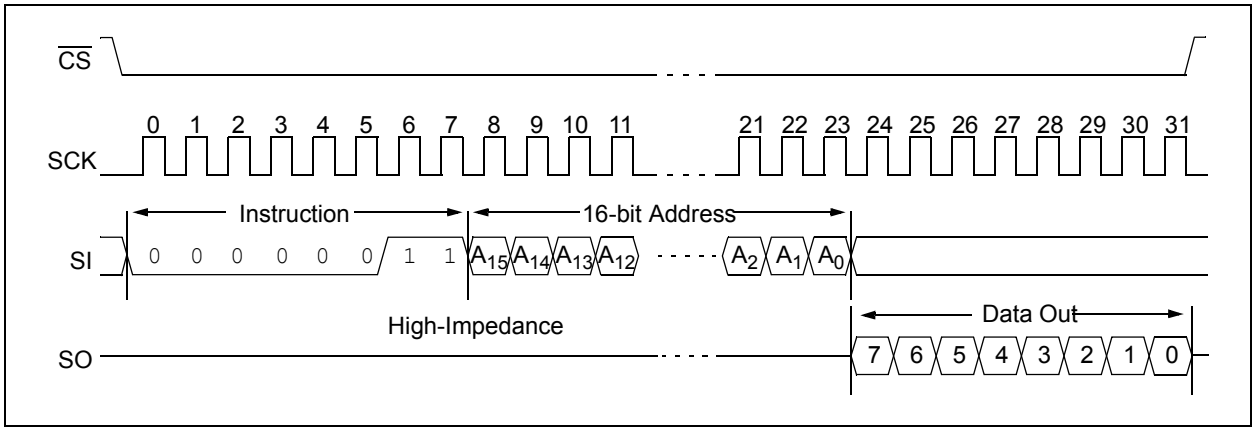
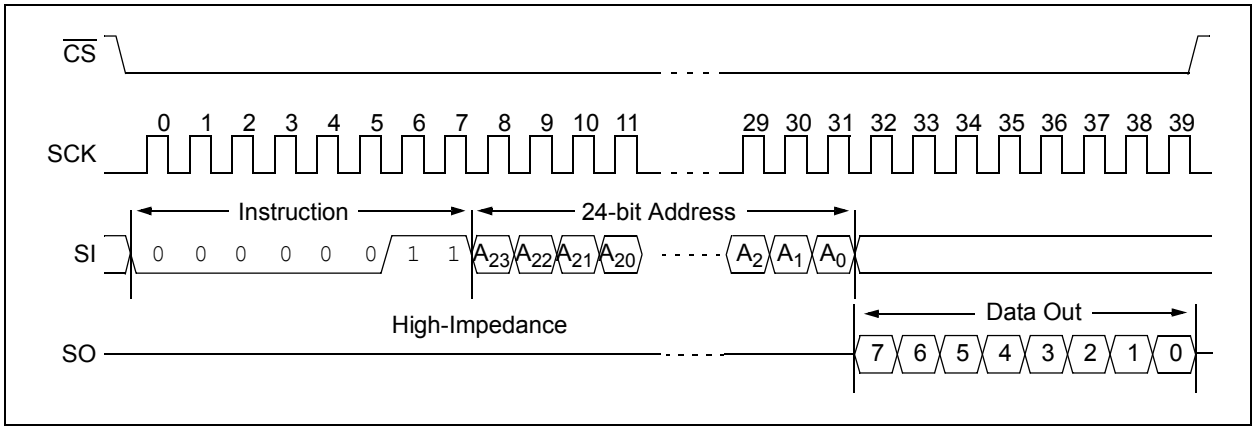


FIGURE 2-1C: READ SEQUENCE WITH 24-BIT ADDRESSING



2.3 Write Sequence

Prior to any attempt to write data to the EEPROM, the write enable latch must be set by issuing the WREN instruction (Figure 2-4). This is done by setting CS low and then clocking out the proper instruction into the EEPROM. After all eight bits of the instruction are transmitted, CS must be brought high to set the write enable latch. If the write operation is initiated immediately after the WREN instruction without CS being brought high, the data will not be written to the array because the write enable latch will not have been properly set.

A write sequence includes an automatic, self timed erase cycle. It is not required to erase any portion of the memory prior to issuing a Write command.

Once the Write Enable Latch is set, the user may proceed by setting CS low, issuing a WRITE instruction, followed by the address and then the data to be written. Depending upon the density, a page of data that ranges from 16 bytes to 256 bytes can be sent to the device before a write cycle is necessary. The only restriction is that all of the bytes must reside in the same page. See Table 2-2 for information on page sizes.

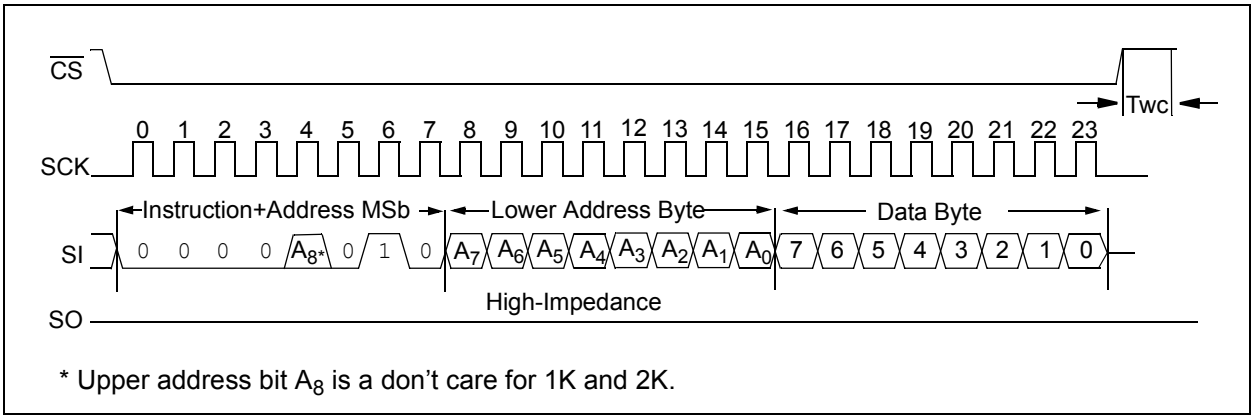
In the 24XX512 and 24XX1024 devices, the entire page is always refreshed regardless of whether the entire page is written. For this reason, endurance for these devices is specified per page.

Note:	Page write operations are limited to writing bytes within a single physical page, regardless of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or 'page size'), and end at addresses that are integer multiples of page size – 1. If a Page Write command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page as might be expected. It is therefore necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

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For the data to be actually written to the array, $\overline{CS}$ must be brought high after the Least Significant bit (D0) of the nth data byte has been clocked in. If $\overline{CS}$ is brought high at any other time, the write operation will not be completed. Refer to Figure 2-2A/B/C and Figure 2-3A/B/C/D for more detailed illustrations on the byte write sequence and the page write sequence, respectively. While the write is in progress, the STATUS register may be read to check the status of the WIP and WEL bits (Figure 2-6). A read attempt of a memory array location will not be possible during a write cycle. When the write cycle is completed, the write enable latch is reset.

FIGURE 2-2A: BYTE WRITE SEQUENCE WITH EITHER 8-BIT OR 9-BIT ADDRESSING



* Upper address bit A_8 is a don't care for 1K and 2K.

FIGURE 2-2B: BYTE WRITE SEQUENCE WITH 16-BIT ADDRESSING

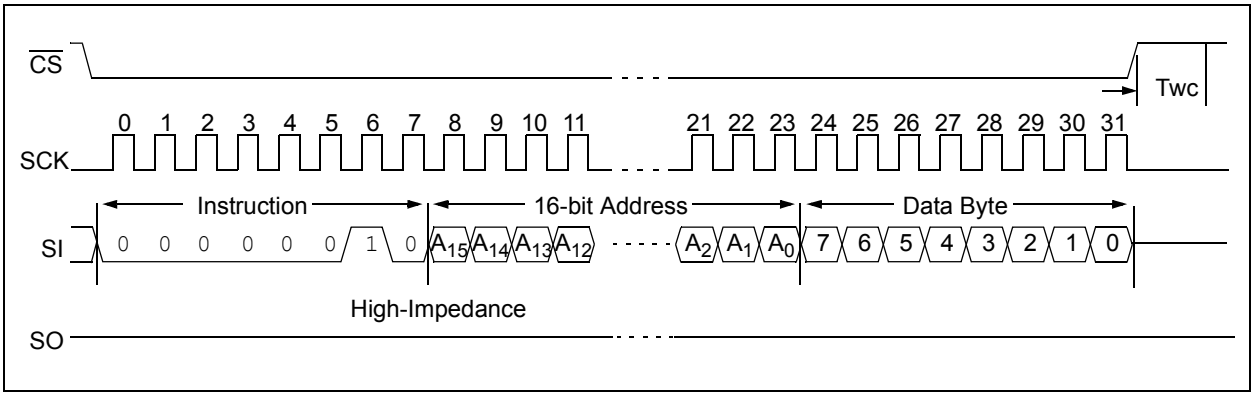


FIGURE 2-2C: BYTE WRITE SEQUENCE WITH 24-BIT ADDRESSING

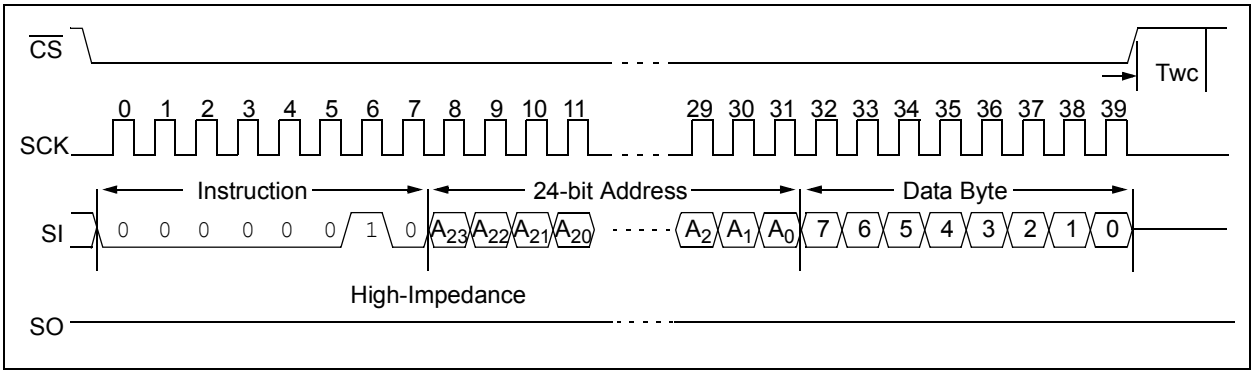
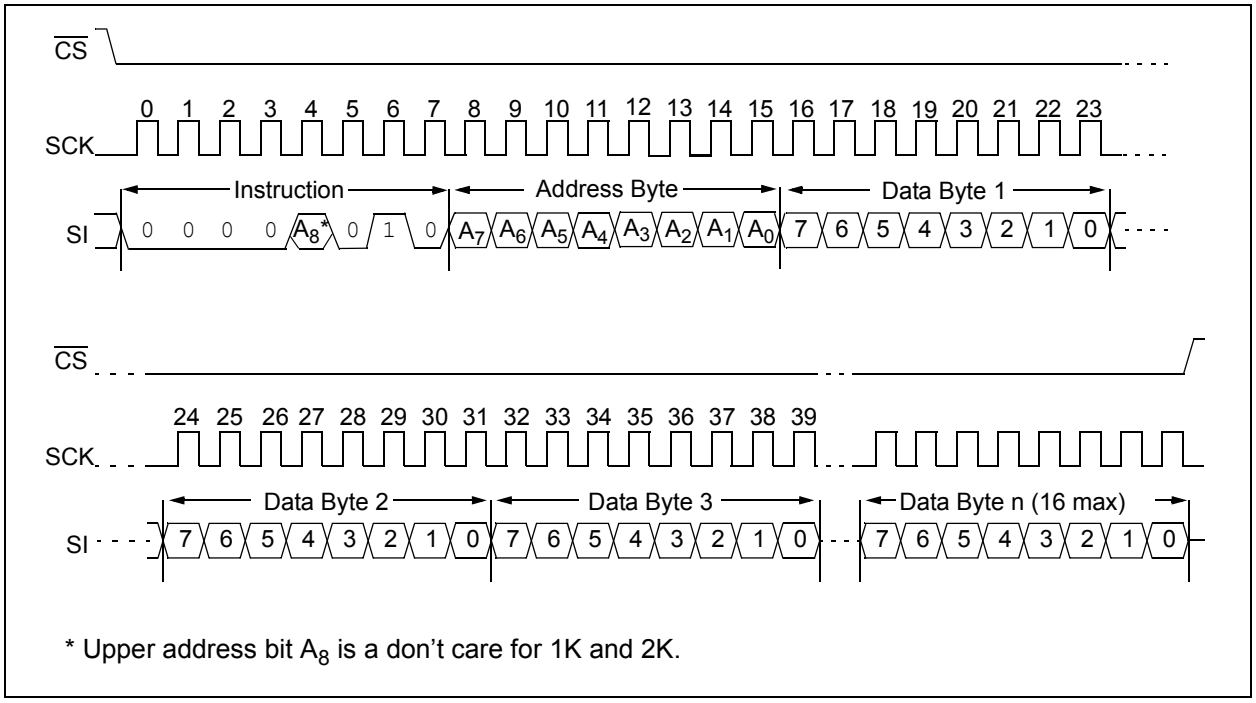
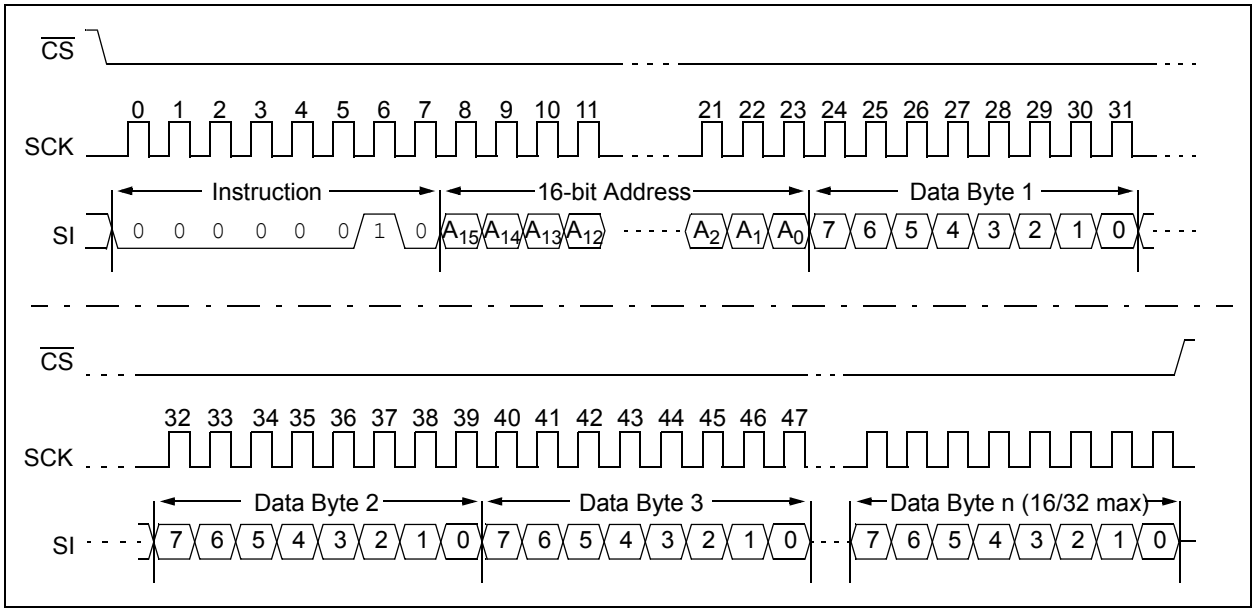


FIGURE 2-3A: PAGE WRITE SEQUENCE WITH EITHER 8-BIT OR 9-BIT ADDRESSING



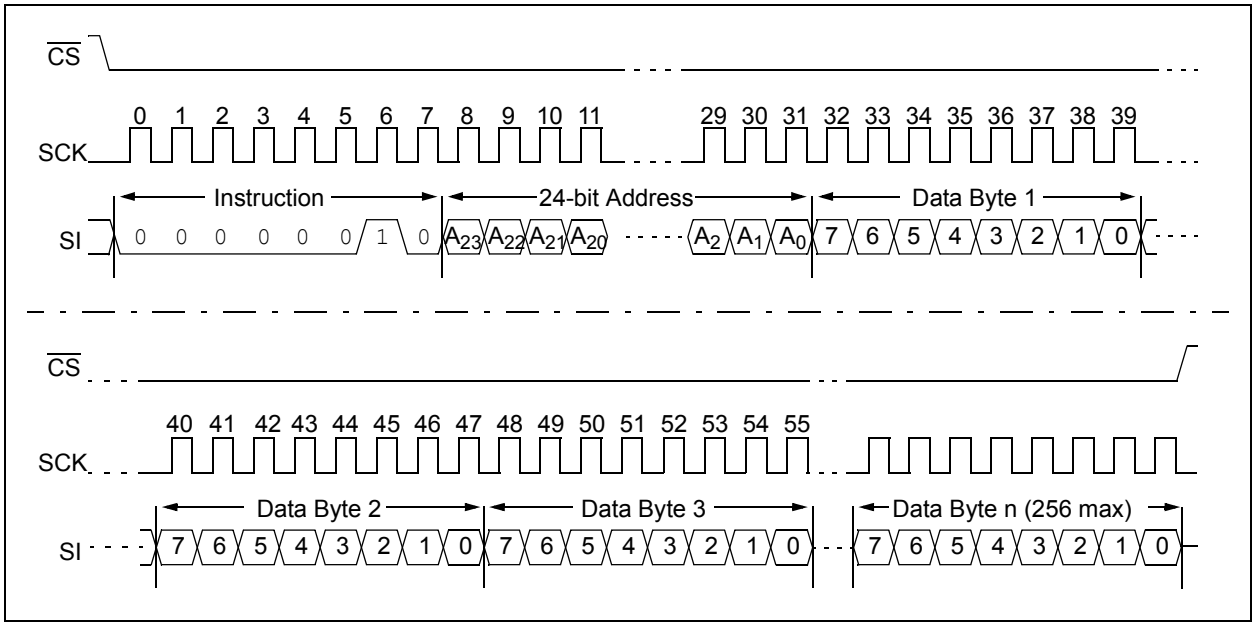
* Upper address bit A_8 is a don't care for 1K and 2K.

FIGURE 2-3B: PAGE WRITE SEQUENCE WITH 16-BIT ADDRESSING



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FIGURE 2-3C: PAGE WRITE SEQUENCE WITH 24-BIT ADDRESSING



2.4 Write Enable (WREN) and Write Disable (WRDI)

The EEPROM contains a write enable latch. See Table 2-4 for the Write-Protect Functionality Matrix. This latch must be set before any write operation will be completed internally. The WREN instruction will set the latch, and the WRDI will reset the latch.

The following is a list of conditions under which the write enable latch will be reset:

- Power-up
- WRDI instruction successfully executed
- WRSR instruction successfully executed
- WRITE instruction successfully executed
- $\overline{WP}$ pin is brought low (1K, 2K, 4K only)

Additional instructions available on 25XX512 and 25XX1024:

- PE instruction successfully executed
- SE instruction successfully executed
- CE instruction successfully executed

FIGURE 2-4: WRITE ENABLE SEQUENCE (WREN)

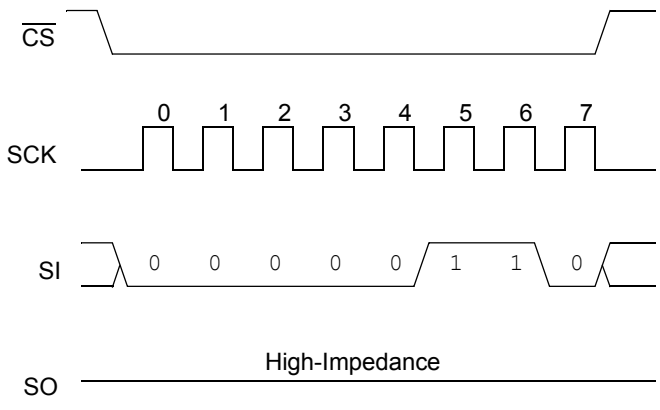
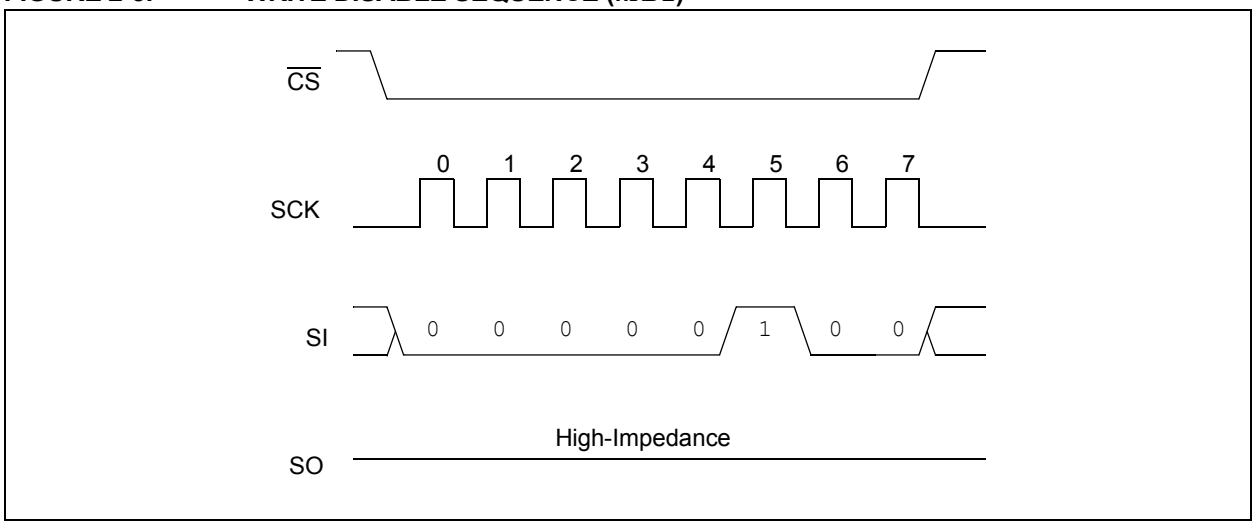


FIGURE 2-5: WRITE DISABLE SEQUENCE (WRDI)



2.5 Read Status Register Instruction (RDSR)

The Read Status Register instruction (RDSR) provides access to the STATUS register. The STATUS register may be read at any time, even during a write cycle. The STATUS register is formatted as follows:

TABLE 2-3: STATUS REGISTER

7	6	5	4	3	2	1	0
W/R	—	—	—	W/R	W/R	R	R
WPEN	X	X	X	BP1	BP0	WEL	WIP
W/R = writable/readable. R = read-only.							

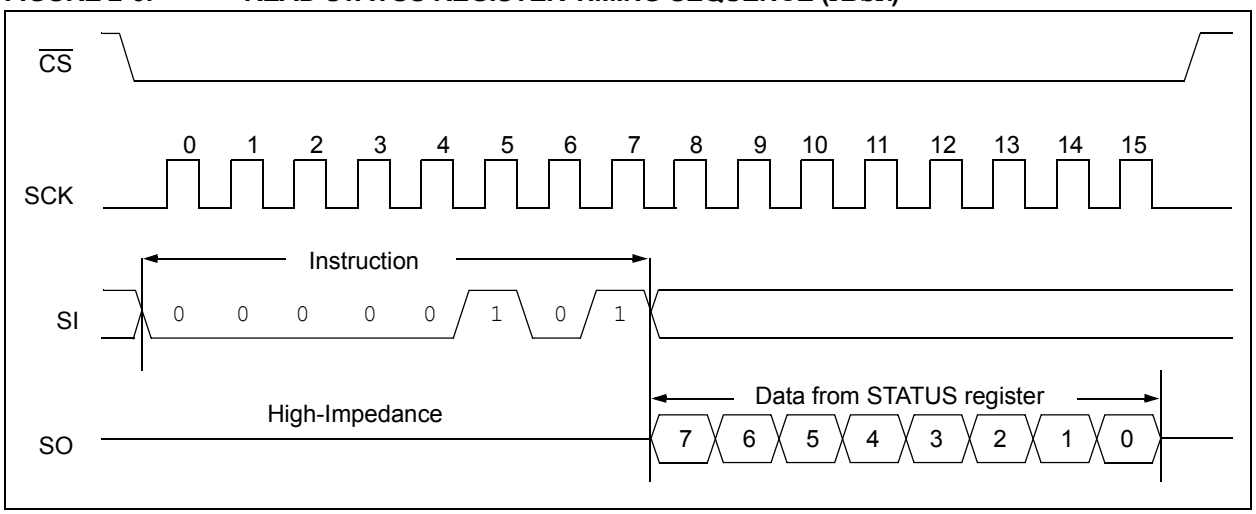
Note: WPEN bit not available in 24XX010A, 24XX020A and 24XX040A devices.

The Write-In-Process (WIP) bit indicates whether the EEPROM is busy with a write operation. When set to a '1', a write is in progress, when set to a '0', no write is in progress. This bit is read-only.

The Write Enable Latch (WEL) bit indicates the status of the write enable latch and is read-only. When set to a '1', the latch allows writes to the array, when set to a '0', the latch prohibits writes to the array. The state of this bit can always be updated via the WREN or WRDI commands regardless of the state of write protection on the STATUS register. These commands are shown in Figure 2-4 and Figure 2-5.

The Block Protection (BP0 and BP1) bits indicate which blocks are currently write-protected. These bits are set by the user issuing the WRSR instruction. These bits are nonvolatile and are shown in Table 2-4. See Figure 2-6 for the RDSR timing sequence.

FIGURE 2-6: READ STATUS REGISTER TIMING SEQUENCE (RDSR)



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2.6 Write Status Register Instruction (WRSR)

The Write Status Register instruction (WRSR) allows the user to write to the nonvolatile bits in the STATUS register as shown in Table 2-3. The user is able to select one of four levels of protection for the array by writing to the appropriate bits in the STATUS register. The array is divided up into four segments. The user has the ability to write-protect none, one, two, or all four of the segments of the array. The partitioning is controlled as is shown in Table 2-4.

In EEPROM densities starting at 8 Kbits and higher, the Write-Protect Enable (WPEN) bit is a nonvolatile bit that is available as an enable bit for the $\overline{WP}$ pin. The Write-Protect ($\overline{WP}$) pin and the Write-Protect Enable (WPEN) bit in the STATUS register control the programmable hardware write-protect feature. Hardware write protection is enabled when $\overline{WP}$ pin is low and the WPEN bit is high. Hardware write protection is disabled when either the $\overline{WP}$ pin is high or the WPEN bit is low. When the chip is hardware write-protected, only writes to nonvolatile bits in the STATUS register are disabled. See Table 2-6 for a matrix of functionality on the WPEN bit. See Figure 2-7 for the WRSR timing sequence.

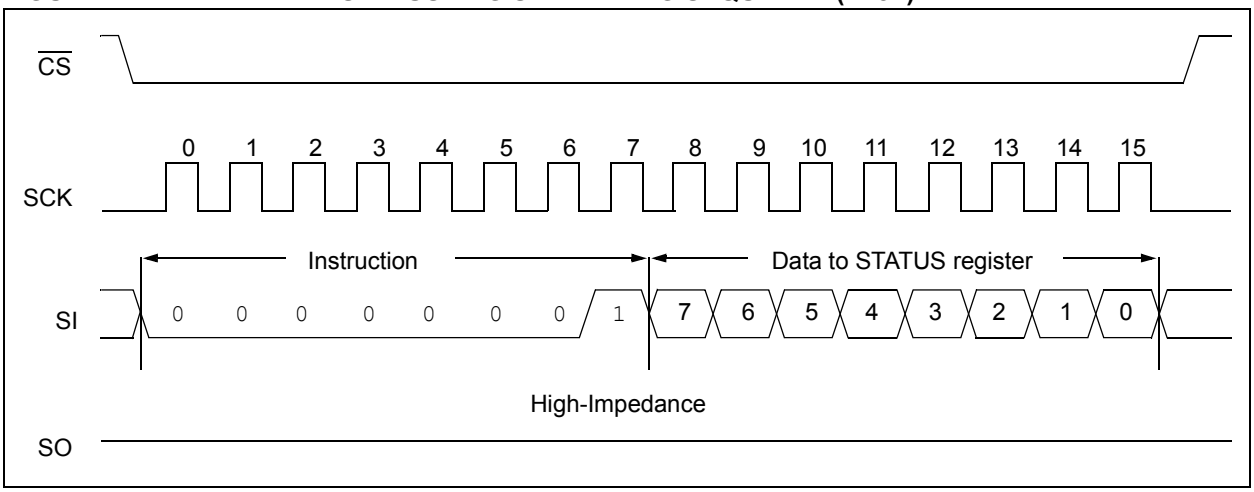
TABLE 2-4: ARRAY PROTECTION

BP1	BP0	Array Addresses Write-Protected	Array Addresses Unprotected
0	0	none	All (Sectors 0, 1, 2 and 3)
0	1	Upper 1/4 (Sector 3)	Lower 3/4 (Sectors 0, 1 and 2)
1	0	Upper 1/2 (Sectors 2 and 3)	Lower 1/2 (Sectors 0 and 1)
1	1	All (Sectors 0, 1, 2 and 3)	none

TABLE 2-5: ARRAY PROTECTED ADDRESS LOCATIONS

Density	Upper 1/4 (Sector 3)	Upper 1/2 (Sectors 2 and 3)	All Sectors
1K	60h-7Fh	40h-7Fh	00h-7Fh
2K	C0h-FFh	80h-FFh	00h-FFh
4K	180h-1FFh	100h-1FFh	000h-1FFh
8K	300h-3FFh	200h-3FFh	000h-3FFh
16K	600h-7FFh	400h-7FFh	000h-7FFh
32K	C00h-FFFh	800h-FFFh	000h-FFFh
64K	1800h-1FFFh	1000h-1FFFh	0000h-1FFFh
128K	3000h-3FFFh	2000h-3FFFh	0000h-3FFFh
256K	6000h-7FFFh	4000h-7FFFh	0000h-7FFFh
512K	C000h-FFFFh	8000h-FFFFh	0000h-FFFFh
1024K	18000h-1FFFFh	10000h-1FFFFh	00000h-1FFFFh

FIGURE 2-7: WRITE STATUS REGISTER TIMING SEQUENCE (WRSR)



2.7 Data Protection

The following protection has been implemented to prevent inadvertent writes to the array:

- The write enable latch is reset on power-up
- A write enable instruction must be issued to set the write enable latch
- After a byte write, page write or STATUS register write, the write enable latch is reset
- $\overline{CS}$ must be set high after the proper number of clock cycles to start an internal write cycle
- Access to the array during an internal write cycle is ignored and programming is continued

2.8 Power-On State

The Serial EEPROM powers on in the following state:

- The device is in low-power Standby mode ($\overline{CS}$ = 1)
- The write enable latch is reset
- SO is in high-impedance state
- A high-to-low-level transition on $\overline{CS}$ is required to enter active State

TABLE 2-6: WRITE-PROTECT FUNCTIONALITY MATRIX

WEL (SR bit 1)	WPEN (SR bit 7) *	$\overline{WP}$ (pin 3)	Protected Blocks	Unprotected Blocks	STATUS Register
0	X	X	Protected	Protected	Protected
1	0	X	Protected	Writable	Writable
1	1	0 (low)	Protected	Writable	Protected
1	1	1 (high)	Protected	Writable	Writable

X = Don't Care
* = WPEN bit is not available on 24XX010A/020A/040A.

2.9 Page Erase

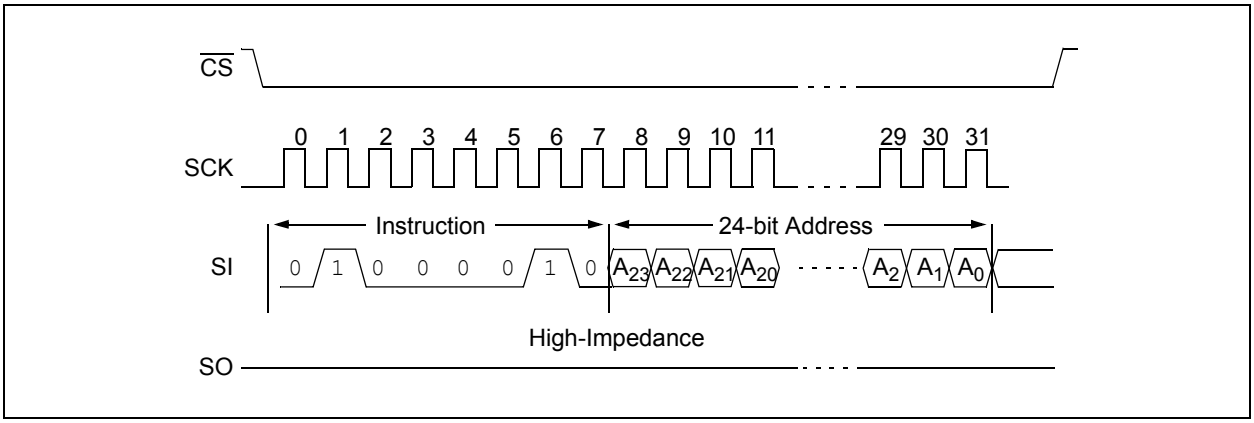
The Page Erase is a typical Flash function that has been implemented only on the 512 Kbit and 1024 Kbit Serial EEPROMs. This function is used to erase all bits (FFh) inside a given page. A Write Enable (WREN) instruction must be given prior to attempting a Page Erase. This is done by setting $\overline{CS}$ low and then clocking out the proper instruction into the EEPROM. After all eight bits of the instruction are transmitted, the $\overline{CS}$ must be brought high to set the write enable latch.

The Page Erase function is entered by driving $\overline{CS}$ low, followed by the instruction code (Figure 2-8A/B) and two or three address bytes. Any address inside the page to be erased is a valid address.

$\overline{CS}$ must then be driven high after the last bit if the address or the Page Erase will not execute. Once the $\overline{CS}$ is driven high, the self-timed Page Erase cycle is started. The WIP bit in the STATUS register can be read to determine when the Page Erase cycle is complete.

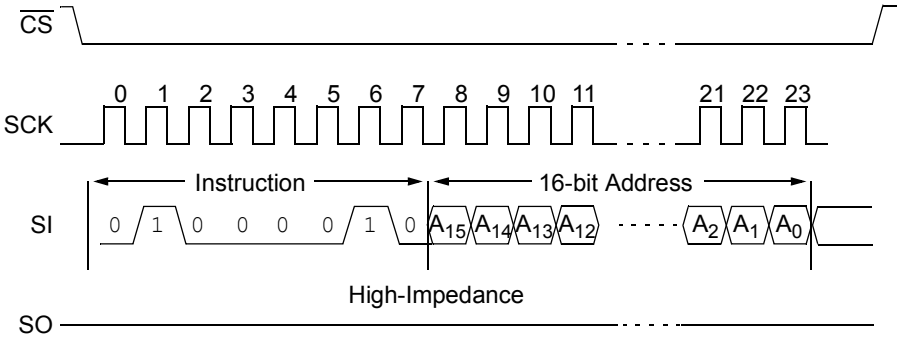
If a Page Erase function is given to an address that has been protected by the Block Protect bits (BP0, BP1) then the sequence will be aborted and no erase will occur.

FIGURE 2-8A: PAGE ERASE SEQUENCE WITH 24-BIT ADDRESSING



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FIGURE 2-8B: PAGE ERASE SEQUENCE WITH 16-BIT ADDRESSING



2.10 Sector Erase

The Sector Erase is a typical Flash function that has been implemented only on the 512 Kbit and 1024 Kbit Serial EEPROMs. This function is used to erase all bits (FFh) inside a given sector. A Write Enable (WREN) instruction must be given prior to attempting a Sector Erase. This is done by setting $\overline{CS}$ low and then clocking out the proper instruction into the EEPROM. After all eight bits of the instruction are transmitted, the $\overline{CS}$ must be brought high to set the write enable latch.

The Sector Erase function is entered by driving $\overline{CS}$ low, followed by the instruction code (Figure 2-9A/B), and two or three address bytes. Any address inside the sector to be erased is a valid address.

$\overline{CS}$ must then be driven high after the last bit if the address or the Sector Erase will not execute. Once the $\overline{CS}$ is driven high, the self-timed Sector Erase cycle is started. The WIP bit in the STATUS register can be read to determine when the Sector Erase cycle is complete.

If a `SECTOR ERASE` instruction is given to an address that has been protected by the Block Protect bits (BP0, BP1) then the sequence will be aborted and no erase will occur.

See Table 2-2 and Table 2-3 for Sector Addressing.

FIGURE 2-9A: SECTOR ERASE SEQUENCE WITH 24-BIT ADDRESSING

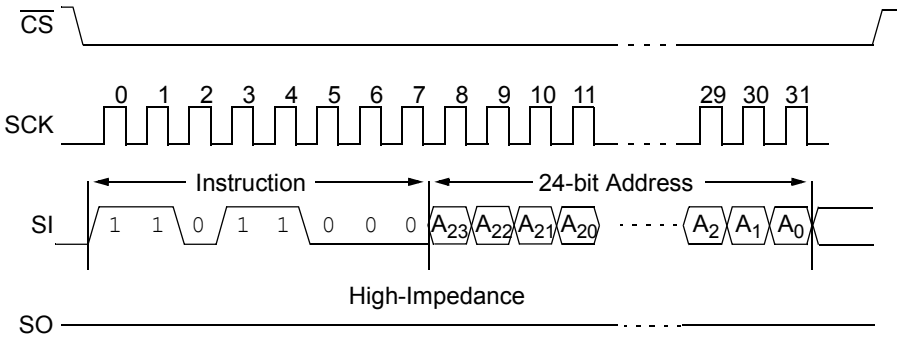
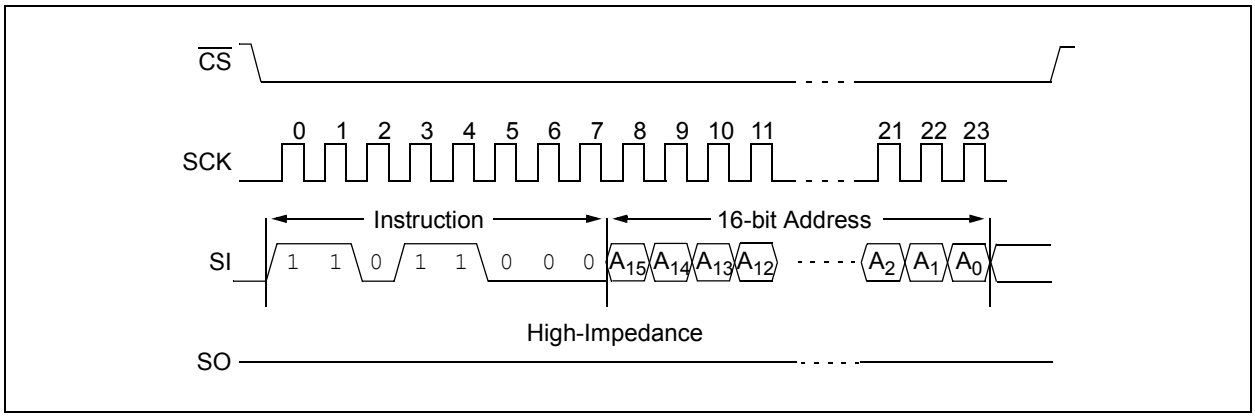


FIGURE 2-9B: SECTOR ERASE SEQUENCE WITH 16-BIT ADDRESSING

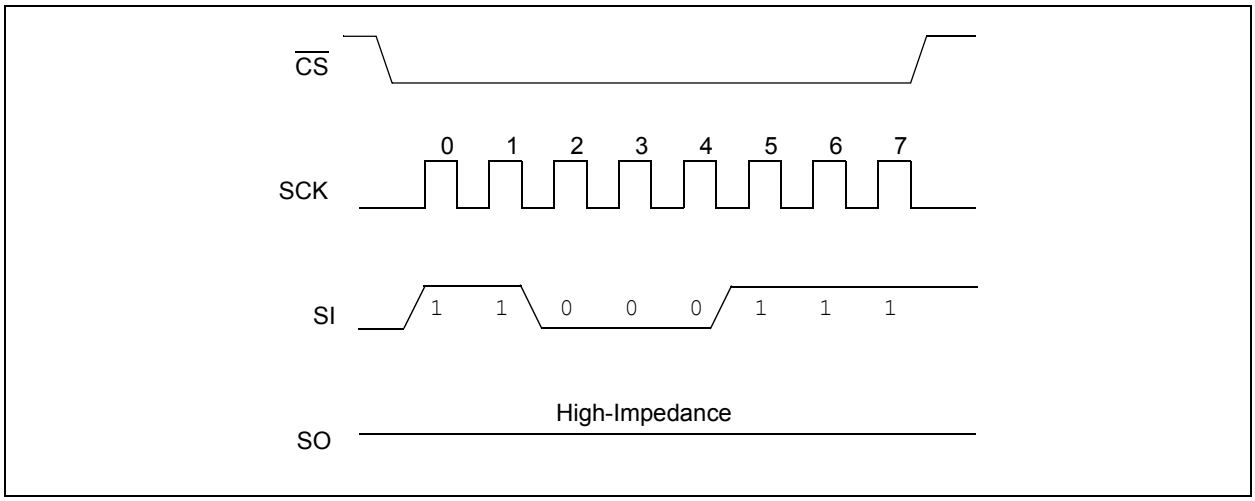


2.11 Chip Erase

The Chip Erase function will erase all bits (FFh) in the array. A Write Enable (WREN) instruction must be given prior to executing a Chip Erase. This is done by setting $\overline{CS}$ low and then clocking out the proper instruction into the EEPROM. After all eight bits of the instruction are transmitted, the $\overline{CS}$ must be brought high to set the write enable latch. The Chip Erase function is entered by driving the $\overline{CS}$ low, followed by the instruction code (Figure 2-10) onto the SI line.

The $\overline{CS}$ pin must be driven high after the eighth bit of the instruction code has been given or the Chip Erase function will not be executed. Once the $\overline{CS}$ pin is driven high, the self-timed Chip Erase function begins. While the device is executing the Chip Erase function the WIP bit in the STATUS register can be read to determine when the Chip Erase function is complete. The Chip Erase function is ignored if either of the Block Protect bits (BP0, BP1) are not '0', meaning ¼, ½, or all of the array is protected.

FIGURE 2-10: CHIP ERASE SEQUENCE



2.12 Deep Power-Down Mode

Deep Power-Down mode is available on the high-density 25XX512 and 25XX1024 Serial EEPROMs and is the lowest power consumption state for these devices. While in the Deep Power-Down mode, these devices will not respond to any of the Read or Write commands, and therefore it can be used as an additional software write protection feature.

The Deep Power-Down mode is entered by driving $\overline{CS}$ low, followed by the instruction code (Figure 2-11) onto the SI line, followed by driving $\overline{CS}$ high.

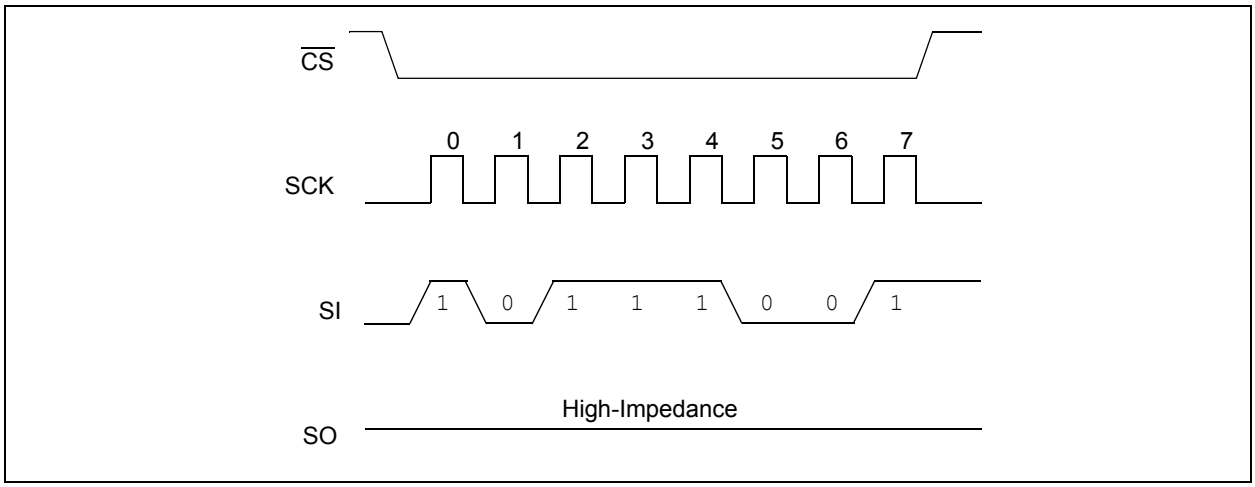
If the $\overline{CS}$ pin is not driven high after the eighth bit of the instruction code has been given, the device will not execute Deep power-down. Once the $\overline{CS}$ line is driven high, there is a delay (T_{DP}) before the current settles to its lowest consumption.

All instructions given during Deep Power-Down mode are ignored except the Read Electronic Signature Command (RDID). The RDID command will release the device from Deep power-down and outputs the electronic signature on the SO pin, and then returns the device to Standby mode after delay (T_{REL}).

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Deep Power-Down mode automatically releases at device power-down. Once power is restored to the device, it will power-up in the Standby mode.

FIGURE 2-11: DEEP POWER-DOWN SEQUENCE



2.13 Release from Deep Power-Down and Read Electronic Signature

Once a device has entered Deep Power-Down mode all instructions are ignored except the Release from Deep Power-down and Read Electronic Signature command. This command can also be used when the device is not in Deep Power-down, to read the electronic signature out on the SO pin unless another command is being executed such as Erase, Program or Write STATUS register.

Release from Deep Power-Down mode and Read Electronic Signature is entered by driving $\overline{CS}$ low, followed by the RDID instruction code (Figure 2-12A/B).Then a dummy address of 24 bits (A23-A0) for the 25XX1024 and 16 bits (A15-A0) for the 25XX512 can be sent. After the last bit of the dummy address is clocked in, the 8-bit Electronic signature is clocked out on the SO pin. After the signature has been read out at least once, the sequence can be terminated by driving $\overline{CS}$ high. The device will then return to Standby mode and will wait to be selected so it can be given new instructions. If additional clock cycles are sent after the electronic signature has been read once, it will continue to output the signature on the SO line until the sequence is terminated.

FIGURE 2-12A: RELEASE FROM DEEP POWER-DOWN AND READ ELECTRONIC SIGNATURE (24-BITS)

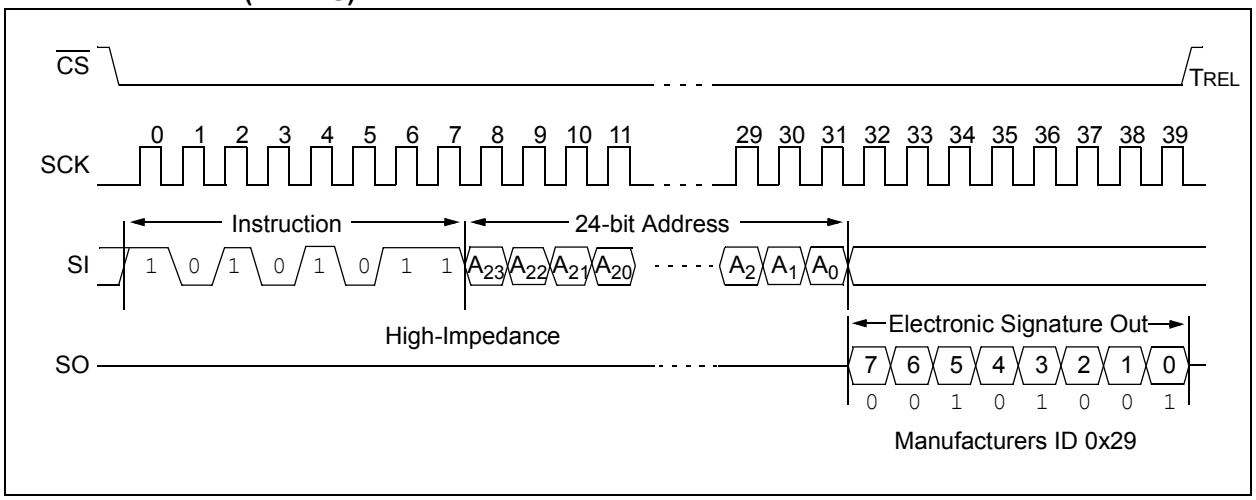
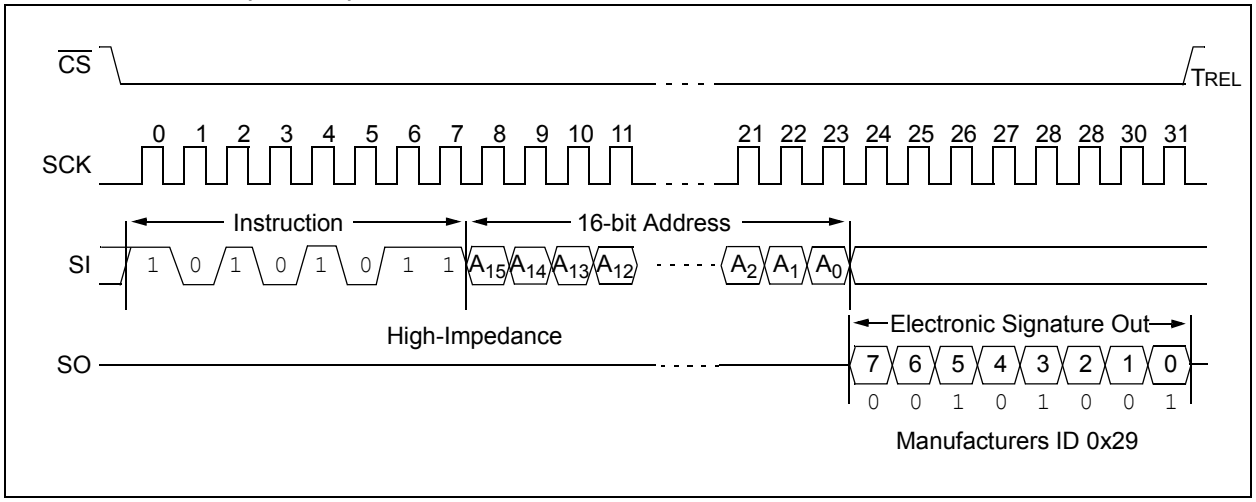


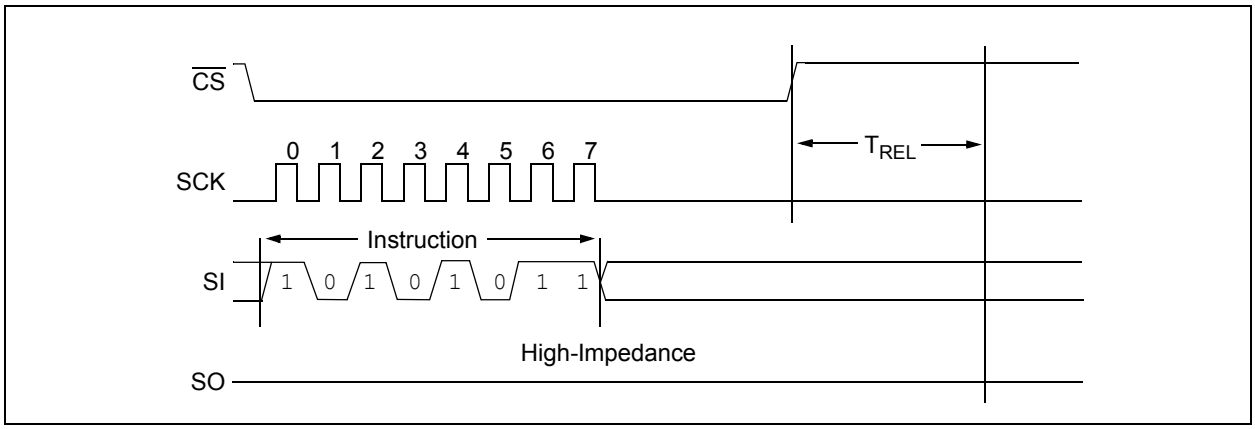
FIGURE 2-12B: RELEASE FROM DEEP POWER-DOWN AND READ ELECTRONIC SIGNATURE (16-BITS)



Driving $\overline{CS}$ high after the 8-bit RDID command, but before the Electronic Signature has been transmitted, will still ensure the device will be taken out of Deep Power-Down mode. However, there is a delay TREL that occurs before the device returns to Standby mode (ICCS), as shown in Figure 2-13.

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FIGURE 2-13: RELEASE FROM DEEP POWER-DOWN



3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Name	Pin Number	Function
$\overline{CS}$	1	Chip Select Input
SO	2	Serial Data Output
$\overline{WP}$	3	Write-Protect Pin
VSS	4	Ground
SI	5	Serial Data Input
SCK	6	Serial Clock Input
$\overline{HOLD}$	7	Hold Input
VCC	8	Supply voltage

3.1 Chip Select ($\overline{CS}$)

A low level on this pin selects the device. A high level deselects the device and forces it into Standby mode. However, a programming cycle which is already initiated or in progress will be completed, regardless of the $\overline{CS}$ input signal. If $\overline{CS}$ is brought high during a program cycle, the device will go into Standby mode as soon as the programming cycle is complete. When the device is deselected, SO goes to the high-impedance state, allowing multiple parts to share the same SPI bus. A low-to-high transition on $\overline{CS}$ after a valid write sequence initiates an internal write cycle. After power-up, a low level on $\overline{CS}$ is required prior to any sequence being initiated.

3.2 Serial Output (SO)

The SO pin is used to transfer data out of the EEPROM. During a read cycle, data is shifted out on this pin after the falling edge of the serial clock.

3.3 Write-Protect ($\overline{WP}$)

The $\overline{WP}$ pin is a hardware write-protect input pin. In the lower densities of 4 Kbits and below, a logic low on this pin will reset the write enable latch and programming will be inhibited. However, if a write cycle is already in progress, $\overline{WP}$ going low will not change or disable the write cycle. See Table 2-4 for the Write-Protect Functionality Matrix.

In densities of 8 Kbits and higher the $\overline{WP}$ pin is used in conjunction with the WPEN bit in the STATUS register to prohibit writes to the nonvolatile bits in the STATUS register. When $\overline{WP}$ is low and WPEN is high, writing to the nonvolatile bits in the STATUS register are disabled. All other operations will function normally. When $\overline{WP}$ is set to a logic high, all functions, including writes to the nonvolatile bits in the STATUS register will operate normally. If the WPEN bit is set, a logic low on the $\overline{WP}$ pin during a STATUS register write sequence will disable writing to the STATUS register. If an internal write cycle has already begun, $\overline{WP}$ going low will have no effect on the write in progress.

The $\overline{WP}$ pin function is blocked when the WPEN bit in the STATUS register is low. This allows the user to install the EEPROM in a system with $\overline{WP}$ pin grounded and still be able to write to the STATUS register. The $\overline{WP}$ pin functions will be enabled when the WPEN bit is set to a logic high.

3.4 Serial Input (SI)

The SI pin is used to transfer data into the device. It receives instructions, addresses and data. Data is latched on the rising edge of the serial clock

3.5 Serial Clock (SCK)

The SCK is used to synchronize the communication between a master and the EEPROM. Instructions, addresses or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin is updated after the falling edge of the clock input.

3.6 Hold ($\overline{HOLD}$)

The $\overline{HOLD}$ pin is used to suspend transmission to the EEPROM while in the middle of a serial sequence without having to retransmit the entire sequence again. It must be held high any time this function is not being used. Once the device is selected and a serial sequence is underway, the $\overline{HOLD}$ pin may be pulled low to pause further serial communication without resetting the serial sequence. The $\overline{HOLD}$ pin must be brought low while SCK is low, otherwise the $\overline{HOLD}$ function will not be invoked until the next SCK high-to-low transition. The EEPROM must remain selected during this sequence. The SI, SCK and SO pins are in a high-impedance state during the time the device is paused and transitions on these pins will be ignored. To resume serial communication, $\overline{HOLD}$ must be brought high while the SCK pin is low, otherwise serial communication will not resume. Pulling the $\overline{HOLD}$ line low at any time will tri-state the SO line.

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APPENDIX A: REVISION HISTORY

Revision A (05/2007)

Original release of document.
(Package Drawings Rev. AP)

Revision B (06/2007)

- Updated the 6-Lead SOT-23 packaging information
- Updated the Product Identification System information
- Minor corrections throughout document

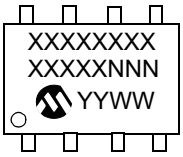
Revision C (08/2007)

Removed “Preliminary” status for 512, 640A and 1024 devices.

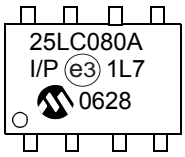
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

8-Lead PDIP



Example: Pb-Free



8-Lead PDIP Package Marking (Pb-Free)			
Device	**Line 1 Marking**	**Device**	**Line 1 Marking**
25AA010A	25AA010A	25LC010A	25LC010A
25AA020A	25AA020A	25LC020A	25LC020A
25AA040A	25AA040A	25LC040A	25LC040A
25AA080A	25AA080A	25LC080A	25LC080A
25AA080B	25AA080B	25LC080B	25LC080B
25AA160A	25AA160A	25LC160A	25LC160A
25AA160B	25AA160B	25LC160B	25LC160B
25AA320A	25AA320A	25LC320A	25LC320A
25AA640A	25AA640A	25LC640A	25LC640A
25AA128	25AA128	25LC128	25LC128
25AA256	25AA256	25LC256	25LC256
25AA512	25AA512	25LC512	25LC512
25AA1024	25AA1024	25LC1024	25LC1024
Note: T = Temperature Grade (I, E).			

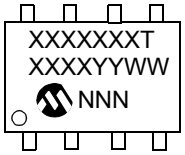
Legend:	XX...X	Part number or part number code
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code (2 characters for small packages)
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn) plated devices

Note: For very small packages with no room for the Pb-free JEDEC designator (e3), the marking will only appear on the outer carton or reel label.

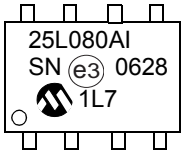
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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8-Lead SOIC



Example: Pb-Free



8-Lead SOIC Package Marking (Pb-Free)			
Device	**Line 1 Marking**	**Device**	**Line 1 Marking**
25AA010A	25AA01AT	25LC010A	25LC01AT
25AA020A	25AA02AT	25LC020A	25LC02AT
25AA040A	25AA04AT	25LC040A	25LC04AT
25AA080A	25A080AT	25LC080A	25L080AT
25AA080B	25A080BT	25LC080B	25L080BT
25AA160A	25A160AT	25LC160A	25L160AT
25AA160B	25A160BT	25LC160B	25L160BT
25AA320A	25AA32AT	25LC320A	25LC32AT
25AA640A	25AA64AT	25LC640A	25LC64AT
25AA128**(2)**	25AA128T	25LC128	25LC128T
25AA256**(2)**	25AA256T	25LC256	25LC256T
25AA512**(2)**	25AA512T	25LC512	25LC512T
25AA1024**(3)**	25AA1024	25LC1024	25LC1024

Note 1: T = Temperature Grade (I, E).
2: Density available in SN and SM versions.
3: Density only available in SM.

Legend:	XX...X	Part number or part number code
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code (2 characters for small packages)
	e3	Pb-free JEDEC designator for Matte Tin (Sn) plated devices

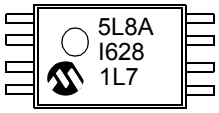
Note: For very small packages with no room for the Pb-free JEDEC designator e3, the marking will only appear on the outer carton or reel label.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead TSSOP



Example: Pb-Free



8-Lead TSSOP Package Marking (Pb-Free)			
Device	**Line 1 Marking**	**Device**	**Line 1 Marking**
25AA010A	5A1A	25LC010A	5L1A
25AA020A	5A2A	25LC020A	5L2A
25AA040A	5A4A	25LC040A	5L4A
25AA080A	5A8A	25LC080A	5L8A
25AA080B	5A8B	25LC080B	5L8B
25AA160A	5AAA	25LC160A	5LAA
25AA160B	5AAB	25LC160B	5LAB
25AA320A	5ABA	25LC320A	5LBA
25AA640A	5ACA	25LC640A	5LCA
25AA128	5AD	25LC128	5LD
25AA256	5AE	25LC256	5LE
Note: T = Temperature Grade (I, E).			

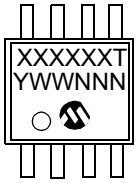
Legend:	XX...X	Part number or part number code
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code (2 characters for small packages)
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn) plated devices

Note: For very small packages with no room for the Pb-free JEDEC designator (e3), the marking will only appear on the outer carton or reel label.

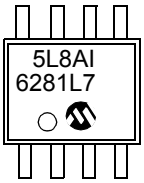
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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8-Lead MSOP



Example: Pb-Free



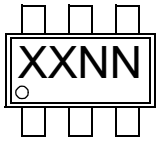
8-Lead MSOP Package Marking (Pb-Free)			
Device	**Line 1 Marking**	**Device**	**Line 1 Marking**
25AA010A	5A1AT	25LC010A	5L1AT
25AA020A	5A2AT	25LC020A	5L2AT
25AA040A	5A4AT	25LC040A	5L4AT
25AA080A	5A8AT	25LC080A	5L8AT
25AA080B	5A8BT	25LC080B	5L8BT
25AA160A	5AAAT	25LC160A	5LAAT
25AA160B	5AABT	25LC160B	5LABT
25AA320A	5ABAT	25LC320A	5LBAT
25AA640A	5ACAT	25LC640A	5LCAT
Note: T = Temperature Grade (I, E).			

Legend:	XX...X	Part number or part number code
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code (2 characters for small packages)
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn) plated devices

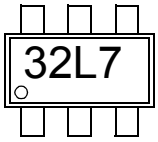
Note: For very small packages with no room for the Pb-free JEDEC designator (e3), the marking will only appear on the outer carton or reel label.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

6-Lead SOT-23



Example: Pb-Free



6-Lead SOT-23 Package Marking (Pb-Free)				
Device	**I-Temp Marking**	**Device**	**I-Temp Marking**	**E-Temp Marking**
25AA010A	12NN	25LC010A	15NN	16NN
25AA020A	22NN	25LC020A	25NN	26NN
25AA040A	32NN	25LC040A	35NN	36NN

Legend:	XX...X	Part number or part number code
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code (2 characters for small packages)
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn) plated devices

Note: For very small packages with no room for the Pb-free JEDEC designator (e3), the marking will only appear on the outer carton or reel label.

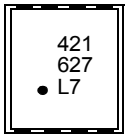
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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8-Lead 2x3 DFN



Example: Pb-Free



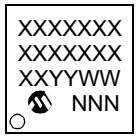
8-Lead 2x3 DFN Package Marking (Pb-Free)				
Device	**I-Temp Marking**	**Device**	**I-Temp Marking**	**E-Temp Marking**
25AA010A	401	25LC010A	404	405
25AA020A	411	25LC020A	414	415
25AA040A	421	25LC040A	424	425
Note: NN = Alphanumeric Traceability Code.				

Legend:	XX...X	Part number or part number code
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code (2 characters for small packages)
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn) plated devices

Note: For very small packages with no room for the Pb-free JEDEC designator (e3), the marking will only appear on the outer carton or reel label.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead 6x5 DFN-S



Example: Pb-Free



8-Lead 6x5 DFN-S Package Marking (Pb-Free)			
Device	**Line 1 Marking**	**Device**	**Line 1 Marking**
25AA128	25AA128	25LC128	25LC128
25AA256	25AA256	25LC256	25LC256
25AA512	25AA512	25LC512	25LC512
25AA1024	25AA1024	25LC1024	25LC1024
Note: T = Temperature Grade (I, E)			

Legend:	XX...X	Part number or part number code
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code (2 characters for small packages)
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn) plated devices

Note: For very small packages with no room for the Pb-free JEDEC designator (e3), the marking will only appear on the outer carton or reel label.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	X	/XX
Device Part Number	Packaging Medium	Temperature Range	Package

Device:	EEPROM Series – 25 Voltage – AA = 1.8V-5.5V LC = 2.5V-5.5V	
Density:	010A 020A 040A 080A 080B 160A 160B 320A 640A 128 256 512 1024	= 1 Kbit = 2 Kbit = 4 Kbit = 8 Kbit = 8 Kbit = 16 Kbit = 16 Kbit = 32 Kbit = 64 Kbit = 128 Kbit = 256 Kbit = 512 Kbit = 1024 Kbit (1Mbit)
Temperature Range:	I E	= -40°C to +85°C = -40°C to +125°C
Packaging Medium:	T Blank	= Tape and Reel (T/R) = Std. Pkg.
Package:	P SN SM ST MS MC MF OT	= 8-lead Plastic DIP (300 mil body) = 8-lead Plastic SOIC (3.90 mm body) = 8-lead Plastic SOIC (5.28 mm body) = 8-lead Plastic TSSOP (4.4 mm) = 8-lead Plastic MSOP (3.0 mm) = 8-lead 2x3 mm DFN (T/R only) = 8-lead 6x5 mm DFN = 6-lead SOT-23 (T/R only)

Examples:

a) 25AA010A-I/SN: 1K
b) 25AA040A-I/MS: 4K
c) 25LC040AT-I/OT: 4K
d) 25LC1024-I/SM: 1M
e) 25LC040AT-I/MC

NOTES:

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Specialty Product References

In addition to a broad general purpose serial EEPROM product line, Microchip also offers several application-specific devices listed in the table below. Data sheets for these devices are not included in this data book but are available at Microchip's EEPROM web page: www.microchip.com/memory.

Application Specific Devices

Application	Part Number	Data Sheet Number
DIMM serial presence detect DDR	24LCS52, 24AA52	DS21166
DIMM serial presence detect DDR	24LC024, 24AA024, 24LC025, 24AA025	DS21210
DIMM serial presence detect DDR2, DDR3	34LC02, 34AA02, 34LV02	DS22029
VESA® "Plug and Play"	24LCS21A	DS21161
VESA® "Plug and Play"	24LCS22A	DS21682
Ultra-high endurance Smart Serial™ EEPROM	24C65, 24LC65, 24AA65	DS21073

NOTES:

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SECTION 4
APPLICATION NOTES

AN1028	Recommended Usage of Microchip I^2C™ Serial EEPROM Devices	4-1
AN1029	Recommended Usage of Microchip Microwire Serial EEPROM Devices	4-9
AN1040	Recommended Usage of Microchip SPI Serial EEPROM Devices	4-13

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AN1028

Recommended Usage of Microchip I²C™ Serial EEPROM Devices

Author: *Chris Parris*
Microchip Technology Inc.

INTRODUCTION

The majority of embedded control systems require nonvolatile memory. Because of their small footprint, byte level flexibility, low I/O pin requirement, low-power consumption, and low cost, serial EEPROMs are a popular choice for nonvolatile storage. Microchip Technology has addressed this need by offering a full line of serial EEPROMs covering industry standard serial communication protocols for two-wire (I²C™), three-wire (Microwire), and SPI communication. Serial EEPROM devices are available in a variety of densities, operational voltage ranges, and packaging options.

In order to achieve a highly robust application when utilizing serial EEPROMs, the designer must consider more than just the data sheet specifications.

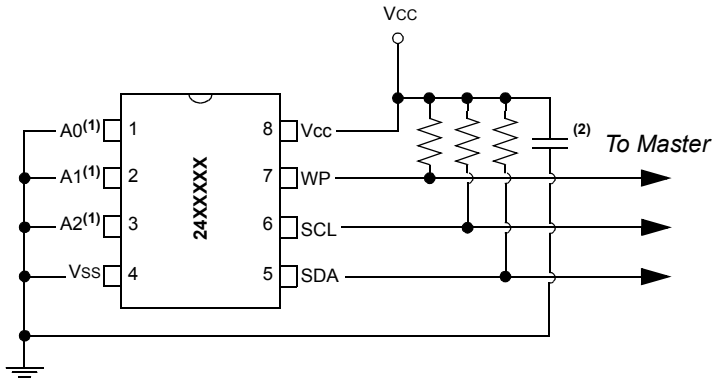
There are a number of conditions which could potentially result in nonstandard operation. The details of such conditions depend greatly upon the serial protocol being used.

This application note provides assistance and guidance with the use of Microchip I²C serial EEPROMs. These recommendations are not meant as requirements; however, their adoption will lead to a more robust overall design. The following topics are discussed:

- Chip Address Inputs
- Write-Protect Feature
- Power Supply
- Checking for Acknowledge
- Acknowledge Polling
- Increasing Data Throughput
- Bus Pull-up Resistors
- Software Reset Sequence

Figure 1 shows the suggested connections for using Microchip I²C serial EEPROMs. The basis for these connections will be explained in the sections which follow.

FIGURE 1: RECOMMENDED CONNECTIONS FOR 24XXXX SERIES DEVICES



Note 1: Pins A0, A1 and A2 are not internally connected in some devices.
2: A decoupling capacitor (typically 0.1 μF) should be used to help filter out small ripples on Vcc.

4 Application Notes

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CHIP ADDRESS INPUTS

The Chip Address input pins (A0, A1 and A2) are used on a number of devices to support multiple device operation. On devices with this feature, the levels on these inputs are compared with the corresponding bits in the slave address, and the device is selected if the comparison is true. Note that the Chip Address pins are not internally connected on some devices. Refer to the appropriate device data sheet for more details.

For devices with internally connected Chip Address pins, these inputs must be hard-wired to either logic '0' or logic '1'. That is, they cannot be left floating, otherwise the device will not operate correctly. Note that the 24XX515 and 24XX1025 devices require that the A2 pin always be held at logic '1' for proper operation.

In some applications, the Chip Address inputs are controlled by a microcontroller or other programmable device. In such instances, the inputs must be driven to either logic '0' or logic '1' before normal device operation can proceed.

WRITE-PROTECT FEATURE

For devices with write-protect functionality, the WP pin provides a hardware write-protect feature which allows the user to protect the entire array when the pin is tied to VCC. If tied to VSS, the write protection is disabled.

A pull-up resistor connected to the WP pin can be used to ensure the device remains write-protected during power-up/power-down and any other time the pin is not being driven explicitly. This helps to guard against unwanted writes which may occur due to noise on the SDA/SCL lines or for other reasons. In order for a write cycle to be initiated, the WP pin must be driven to logic '0', otherwise the write cycle will not execute.

If the designer chooses not to control the WP pin, but rather to always disable write protection, the pin must be hard-wired to logic '0'. As with the Chip Address inputs, this pin cannot be left floating, otherwise the device will not operate correctly.

Note that some devices do not support write-protect functionality.

POWER SUPPLY

Microchip serial EEPROMs feature a high amount of protection from unintentional writes and data corruption while power is within normal operating levels. But certain considerations should be made regarding power-up and power-down conditions to ensure the same level of protection during those times when power is not within normal operating levels.

As shown in Figure 1, a decoupling capacitor (typically 0.1 μF) should be used to help filter out small ripples on VCC.

Power-Up

On power-up, VCC should always begin at 0V and rise straight to its normal operating level to ensure a proper Power-on Reset. VCC should not linger at an ambiguous level (i.e., below the minimum operating voltage).

Brown-Out Conditions

For added protection, Microchip serial EEPROMs feature a Brown-out Reset circuit. However, if VCC happens to fall below the minimum operating voltage for the serial EEPROM, it is recommended that VCC be brought down fully to 0V before returning to normal operating level. This will help to ensure that the device is reset properly.

Furthermore, if the microcontroller features a Brown-out Reset with a threshold higher than that of the serial EEPROM, bringing VCC down to 0V will allow both devices to be reset together. Otherwise, the microcontroller may reset during communication while the EEPROM keeps its current state. In this case, a software Reset sequence would be required before beginning further communication.

Power Failure During a Write Cycle

During a write cycle, VCC must remain above the minimum operating voltage for the entire duration of the cycle (typically 5 ms max. for most devices). If VCC falls below this minimum voltage at any point for any length of time, data integrity cannot be ensured. It will result in marginally programmed data that may or may not be correct. Furthermore, because the EEPROM cells were not able to be fully programmed, the device will have shorter data retention time than specified in the data sheet.

CHECKING FOR ACKNOWLEDGE

One of the many benefits of I^2C communication is the Acknowledge bit transmitted after every byte is received. Except during write cycles, Microchip serial EEPROMs will always transmit this bit low after receiving each byte, assuming a valid Start bit and control byte were already received. Due to this, the master can monitor the ACK bit received throughout an operation to detect any errors that may occur. It is always good practice to check if a logic '1' is received for the ACK during transmission, which would indicate that the EEPROM did not respond. At that point, an error-handling routine would be required to determine why the device did not respond and, if necessary, to perform a software Reset sequence.

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ACKNOWLEDGE POLLING

Write operations on serial EEPROMs require that a write cycle time be observed after initiating the write, allowing the device time to store the data. During this time, normal device operation is disabled, and any attempts by the master to access the device will be ignored. Therefore, it is important that the master wait for the write cycle to end before attempting to access the EEPROM again.

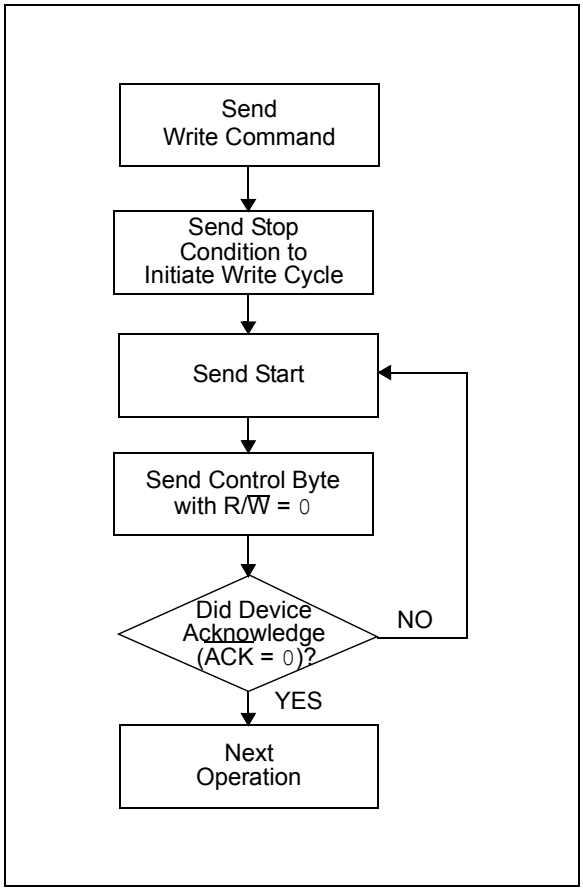
Each device has a specified worst-case write cycle time, typically listed as TWC. A simple method for ensuring that the write cycle time is observed is to perform a delay for the amount of time specified before accessing the EEPROM again. However, it is not uncommon for a device to complete a write cycle in less than the maximum specified time. As such, using the previously shown delay method results in a period of time in which the EEPROM has finished writing, but the master is still waiting.

In order to eliminate this extra period of time, and therefore operate more efficiently, it is highly recommended to take advantage of the Acknowledge Polling feature. Since Microchip's I^2C serial EEPROM devices will not acknowledge during a write cycle, the device can continuously be polled until an ACK bit is received, thus indicating that the write is complete. This is done after the Stop condition takes place to initiate the internal write cycle of the device.

Procedure

Once the Stop condition for a Write command has been issued from the master, the device initiates the internally timed write cycle, and ACK polling can be initiated immediately. This involves the master sending a Start condition followed by the control byte for a Write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If no ACK is returned, then the Start bit and control byte must be sent again. If the cycle is complete, the device will return the ACK and the master can then proceed with the next Read or Write command. See Figure 2 for details.

FIGURE 2: ACKNOWLEDGE POLLING FLOW



INCREASING DATA THROUGHPUT

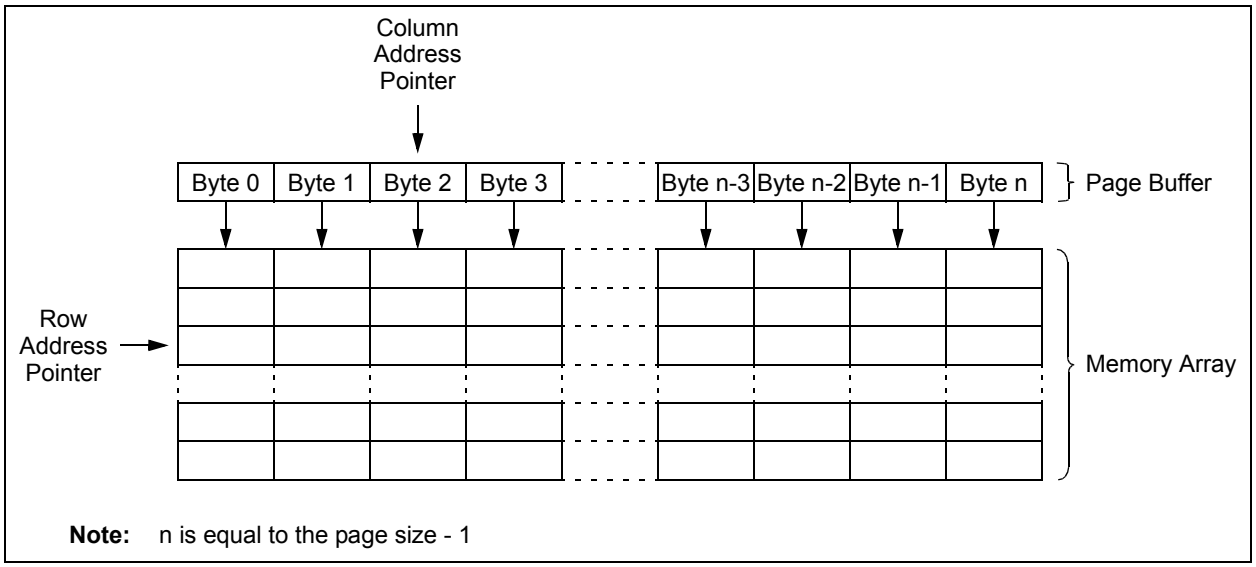
Page Writes

Most Microchip I^2C serial EEPROMs feature a page buffer for use during write operations. This allows the user to write any number of bytes from one to the maximum page size in a single operation. This can provide for a significant decrease in the total write time when writing a large number of bytes.

Page write operations are limited to writing within a single physical page, regardless of the number of bytes actually being written. This is because the memory array is physically stored as a two-dimensional array, as shown in Figure 3. When the word address is given at the beginning of a write operation, both the row and column Address Pointers are set. The row Address Pointer selects which row, or page, is accessed, whereas the column Address Pointer selects which byte from the chosen page is accessed first. Upon transmission of each data byte, the column Address Pointer is automatically incremented. However, during a write operation, the page Address Pointer is not incremented, which means that attempting to cross a page boundary during a page write operation will result in the data being looped back to the beginning of the page.

Note that physical page boundaries start at addresses that are multiples of the page size. For example, the 24XX512 features a 128-byte page size, which means that physical pages on the device begin at addresses 0x0000, 0x0080, 0x0100, and so on.

FIGURE 3: PAGE BUFFER BLOCK DIAGRAM



Procedure

The write control byte, word address, and the first data byte are transmitted to the device in the same way as in a byte write operation. But instead of generating a Stop condition, the master continues transmitting additional data bytes, which are temporarily stored in the on-chip page buffer, up to the maximum page size of the device. As with the byte write operation, once the Stop condition is received, an internal write cycle will begin during which all bytes stored in the page buffer will be written.

Write Time Comparisons

In order to accurately calculate the full period of time required to write a particular amount of data to a device, two things must be considered.

- **Load time** is the amount of time needed to complete all bus operations. This includes generating Start and Stop conditions, as well as transmitting the control, address, and data bytes (including ACKs). This amount of time is dependent on the bus clock speed, the number of data bytes to be written, and the addressing scheme of the particular device (some devices utilize a 1-byte address, whereas others use a 2-byte address).

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- **Write cycle time** is the time during which the device is executing its internal write cycle. As described in the previous section (“Acknowledge Polling”), there is a specified maximum write cycle time for each device. However, the internal write cycle typically completes in less time than specified. As such, both worst-case (5 ms) and typical (3 ms at TAMB = 25 °C) calculations are provided in Table 1.

The following equations were used to calculate the values for Table 1:

EQUATION 1: WRITE TIME EQUATIONS

$$T_{LOAD} = \frac{9 \cdot (1 + \#\text{ address bytes} + \#\text{ data bytes}) + 1}{F_{CLK}}$$

$$T_{TOTAL} = (T_{LOAD} + T_{WC}) \cdot \#\text{ write operations}$$

TABLE 1: WRITE TIME COMPARISONS

Device	Page Size (bytes)	# of Bytes to Write	Write Mode(1)	Clock Speed (kHz)	Load Time Per Operation (ms)	Total Time (ms) Worst-Case(2)	Total Time (ms) Typical(3)
24LC01B	8	1	Byte	100	0.28	5.28	3.28
		8	Byte	100	0.28	42.24	26.24
		8	Page	100	0.91	5.91	3.91
		1	Byte	400	0.07	5.07	3.07
		8	Byte	400	0.07	40.56	24.56
		8	Page	400	0.23	5.23	3.23
24LC16B	16	1	Byte	100	0.28	5.28	3.28
		16	Byte	100	0.28	84.48	52.48
		16	Page	100	1.63	6.63	4.63
		1	Byte	400	0.07	5.07	3.07
		16	Byte	400	0.07	81.12	49.12
		16	Page	400	0.41	5.41	3.41
24LC512	128	1	Byte	100	0.37	5.37	3.37
		128	Byte	100	0.37	687.36	431.36
		128	Page	100	11.80	16.80	14.80
		1	Byte	400	0.09	5.09	3.09
		128	Byte	400	0.09	651.84	395.84
		128	Page	400	2.95	7.95	5.95

Note 1: Byte Write mode signifies that only 1 byte is written during a single write operation. Page Write mode signifies that a full page is written during a single write operation.

2: Worst-case calculations assume a 5 ms timed delay is used.

3: Typical calculations assume Acknowledge polling is used, with typical TWC = 3 ms, TAMB = 25 °C.

From these examples, it is clear that both page writes and Acknowledge polling can provide significant time savings. Writing 128 bytes to the 24LC512 via byte writes at 400 kHz requires roughly 652 ms worst-case. Switching to Acknowledge polling brings that down to roughly 396 ms (assuming typical conditions), nearly a 40% decrease. Additionally, changing to page writes further lowers the time to an impressive 5.95 ms, a decrease of over 98%. Overall, the two techniques provide a combined time savings of nearly 646 ms, increasing the total data throughput a staggering 109 times over.

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BUS PULL-UP RESISTORS

For proper operation, pull-up resistors are required for both SCL and SDA buses. However, the resistor value chosen can have a vast impact on the performance of the system. Specifically, three limiting factors must be considered when selecting pull-up resistor (R_P) values:

- Supply voltage (V_{CC})
- Total Bus Capacitance (C_{BUS})
- Total High-Level Input Current (I_{IH})

Supply Voltage (V_{CC})

Supply voltage limits the minimum R_P value due to maximum low-level output voltage (V_{OL}) specifications. Meaning that, for a given V_{CC} level, a smaller pull-up resistor will result in a higher output voltage. For Microchip I^2C devices, the V_{OL} specification is a maximum of 0.4V at 3 mA. In other words, if there is a voltage drop across R_P of V_{CC}-0.4V, it cannot be sourcing more than 3 mA. Applying Ohm's Law yields Equation 2.

EQUATION 2: MINIMUM R_P VALUE

$$R_{PMIN} = \frac{V_{CC} - V_{OL}}{I_{OL}} = \frac{V_{CC} - 0.4V}{3\ mA}$$

Total Bus Capacitance (C_{BUS})

Bus capacitance includes all pin, connection, and wire capacitance on the bus. Due to the RC time constant, higher bus capacitance requires a smaller pull-up resistor to meet a particular rise time, and therefore, clock speed. This is an important consideration for designs consisting of many devices on a single bus.

Equation 3 is the general equation used to characterize charging of a capacitive load as a function of time. This allows for calculation of the amount of time required for the bus voltage to rise to a particular value for a specific pull-up resistance and bus capacitance.

EQUATION 3: CAPACITOR CHARGING

$$V(t) = V_0(1 - e^{-t \S (RC)})$$

$$\Rightarrow -t = (RC)\ln\left(1 - \frac{V(t)}{V_0}\right)$$

Bus rise time (T_R) is defined as the amount of time required for the voltage to rise from V_{IL} to V_{IH}. Equation 3 is applied to calculate the bus rise time for V_{IL}=0.3*V_{CC} and V_{IH}=0.7*V_{CC}, and the result is shown in Equation 4. Note that because V_{IL} and V_{IH} are specified as functions of V_{CC}, the final equation is independent of V_{CC}, as long as the V_{IL} specification does not change.

EQUATION 4: BUS RISE TIME

$$-T_1 = (RC)\ln\left(1 - \frac{V_{IL}}{V_{CC}}\right) = (RC)\ln(1 - 0.3)$$

$$\Rightarrow T_1 = 0.356675 \cdot RC$$

$$-T_2 = (RC)\ln\left(1 - \frac{V_{IH}}{V_{CC}}\right) = (RC)\ln(1 - 0.7)$$

$$\Rightarrow T_2 = 1.20397 \cdot RC$$

$$T_R = T_2 - T_1 = 0.847298 \cdot RC$$

Equation 4 can be quite useful in calculating bus rise time; however, such a parameter is already specified in the data sheet for different bus speeds. As such, the equation must be rearranged to be of any use in determining the maximum value of R_P as limited by bus rise time. This results in Equation 5.

EQUATION 5: MAX. R_P DUE TO RISE TIME

$$R_{PMAX} = \frac{T_R}{0.847298 \cdot C_{BUS}}$$

Total High-Level Input Current (I_{IH})

The total high-level input current for a line is the total amount of current which will be flowing through the pull-up resistor when there are no contentions and the line is allowed to be pulled up by the resistor. This current consists of the sum of the input leakage currents for all devices connected to the bus, as well as any other current being sunk by the devices through the input pin.

Because some current will always exist through the pull-up resistor even without bus contention, the effective voltage seen at the pin will be lower than V_{CC} due to the voltage drop across the resistor. This voltage drop must be small enough that the voltage at the pin will still be considered a high by the device. That is, the voltage at the pin must be higher than V_{IH} combined with the high-level input noise margin (V_{HMAR}). Applying Ohm's Law once again results in Equation 6.

EQUATION 6: MAX. R_P DUE TO CURRENT

$$R_{PMAX} = \frac{V_{CC} - (V_{IH} + V_{HMAR})}{I_{IH}}$$

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Example Resistor Value Calculation

Here is an example of how to use the previous equations to select the appropriate pull-up resistor value. The following parameters will be used:

TABLE 2: EXAMPLE PARAMETERS

Parameter	Value	Units
V_{CC}	5.0	V
T_R	300[1]	ns
C_{BUS}	100	pF
V_{IH}	3.5[2]	V
V_{HMAR}	1.0[3]	V
I_{IH}	10	μA

Note 1: T_R based on desired clock speed of 400 kHz.

2: V_{IH} derived from 0.7*V_{CC} spec.

3: V_{HMAR} derived from 0.2*V_{CC} spec.

By applying Equation 2, Equation 5 and Equation 6, the following resistor value limits were calculated:

TABLE 3: RESISTOR VALUE LIMITS

Limit	Value	Limiting Factor
R_{PMIN}	1.533 kΩ	Supply Voltage
R_{PMAX}	3.541 kΩ	Bus Capacitance
R_{PMAX}	50 kΩ	Input Current

Although the input current is small enough that, at the specified V_{CC} level, a 50 kΩ resistor would not create too large of a voltage drop, such a large resistor would be far too slow for the specified bus capacitance. Therefore, the range of acceptable resistor values is from 1.533 kΩ to 3.541 kΩ. It is recommended to choose a value near the middle of the range to provide as much guard banding as possible. For this example, a 2.2 kΩ pull-up resistor would be ideal.

Bus Speed vs. Power Consumption

In order to reach a given bus speed, larger bus capacitance requires smaller pull-up resistors. For instance, in the above example, the calculated value for R_{PMAX} due to bus capacitance was 3.541 kΩ at 100 pF. However, if the bus capacitance were increased to roughly 231 pF, the new R_{PMAX} value would be 1.533 kΩ. This smaller resistor would, in turn, allow more current to be drawn when a device pulls down the bus. Specifically, a maximum of 3.26 mA at 1.533 kΩ versus 1.41 mA at 3.541 kΩ.

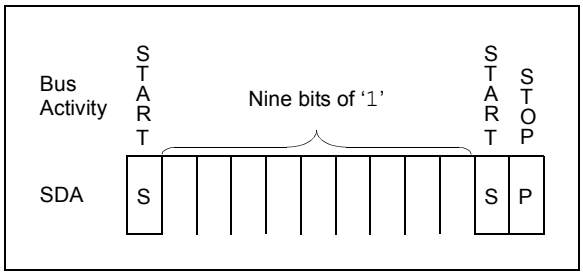
Larger currents due to smaller pull-up resistors can have a considerable effect on power consumption and battery life. As such, it is recommended that the slowest bus speed tolerable by the design be chosen. In the example above, simply decreasing to 100 kHz (1000 ns rise time) allows for a 5.109 kΩ pull-up resistor to be used, at 231 pF. This lowers the maximum current to 0.979 mA.

SOFTWARE RESET SEQUENCE

At times it may become necessary to perform a software Reset sequence to ensure the serial EEPROM is in a correct and known state. This could be useful, for example, if the EEPROM has powered up into an incorrect state (due to excessive bus noise, etc.), or if the microcontroller is reset during communication. The following sequence can be sent in order to ensure that the serial EEPROM device is properly reset:

- Start bit
- Clock in nine bits of '1'
- Start bit
- Stop bit

FIGURE 4: SOFTWARE RESET SEQUENCE



The first Start bit will cause the device to reset from a state in which it is expecting to receive data from the microcontroller. In this mode, the device is monitoring the data bus in Receive mode and can detect the Start bit which forces an internal Reset.

The nine bits of '1' are used to force a Reset of those devices that could not be reset by the previous Start bit. This occurs only if the device is in a mode where it is either driving an acknowledge on the bus (low), or is in an Output mode and is driving a data bit of '0' out on the bus. In both of these cases the previous Start bit (defined as SDA going low while SCL is high) could not be generated due to the device holding the bus low. By sending nine bits of '1' it is ensured that the device will see a NACK (i.e., the microcontroller does not drive the bus low to acknowledge data sent by the EEPROM), which also forces an internal Reset.

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The second Start bit is sent to guard against the rare possibility of an erroneous write that could occur if the microcontroller was reset while sending a Write command to the EEPROM, and, the EEPROM was driving an ACK on the bus when the first Start bit was sent. In this special case, if this second Start bit was not sent, and instead the Stop bit was sent, the device could initiate a write cycle. This potential for an erroneous write occurs only in the event of the microcontroller being reset while sending a Write command to the EEPROM.

The final Stop bit terminates bus activity and puts the EEPROM in Standby mode.

This sequence does not affect any other I^2C devices which may be on the bus as they will simply disregard it as an invalid command.

In situations where the software Reset sequence is needed, a bus conflict is likely to occur. When using the MSSP module, this will cause the Bus Collision Flag (BCLIF) to be set and, therefore, will block any further bus transactions. In order to issue a software Reset, the module will need to be disabled and the software Reset sequence will need to be bit-banged. Once the software Reset sequence is complete, the module can be re-enabled, the Bus Collision Flag cleared, and the MSSP module will be ready for normal bus operations.

SUMMARY

This application note illustrates recommended techniques for increasing design robustness when using Microchip I^2C serial EEPROMs. These recommendations fall directly in line with how Microchip designs, manufactures, qualifies, and tests its serial EEPROMs and will allow the devices to operate within the data sheet parameters. It is suggested that the concepts detailed in this application note be incorporated into any system which utilizes an I^2C serial EEPROM.

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AN1029

Recommended Usage of Microchip Microwire Serial EEPROM Devices

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INTRODUCTION

The majority of embedded control systems require nonvolatile memory. Because of their small footprint, byte level flexibility, low I/O pin requirement, low-power consumption, and low cost, serial EEPROMs are a popular choice for nonvolatile storage. Microchip Technology has addressed this need by offering a full line of serial EEPROMs covering industry standard serial communication protocols for two-wire (I^2C™), three-wire (Microwire), and SPI communication. Serial EEPROM devices are available in a variety of densities, operational voltage ranges, and packaging options.

In order to achieve a highly robust application when utilizing serial EEPROMs, the designer must consider more than just the data sheet specifications.

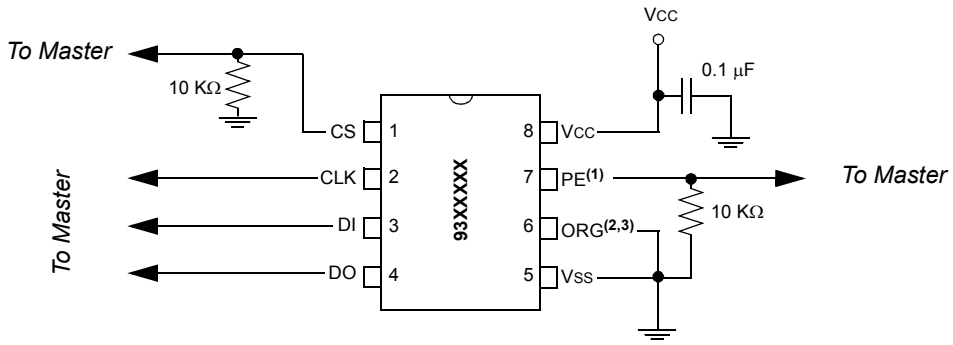
There are a number of conditions which could potentially result in nonstandard operation. The details of such conditions depend greatly upon the serial protocol being used.

This application note provides assistance and guidance with the use of Microchip Microwire serial EEPROMs. These recommendations are not meant as requirements; however, their adoption will lead to a more robust overall design. The following topics are discussed:

- Chip Select and Program Enable Inputs
- Proper Write Sequence
- Resetting the State Machine
- Using a Hardware SPI port for Microwire communication
- Tying DI and DO together
- Power-up/Power-down

Figure 1 shows the suggested connections for using Microchip Microwire serial EEPROMs. The basis for these connections will be explained in the sections which follow.

FIGURE 1: RECOMMENDED CONNECTIONS FOR 93XXXX SERIES DEVICES



Note 1: PE pins exist on only the 93XX76X and 93XX86X devices (8K and 16K devices).
Note 2: ORG is in x8 configuration when tied to VSS. For x16 operation, this pin needs to be tied to VCC.
Note 3: Devices with A or B suffix will not have an ORG pin.

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CHIP SELECT AND PROGRAM ENABLE INPUTS

During power-up and power-down routines, most microcontrollers have a period of time in which they float I/O lines before the processor is fully initialized. It is during this time that any external device controlled by the microcontroller may be able to recognize and react to spurious commands or line noise. Therefore, a pull-down resistor should be used on the CS line to keep the EEPROM de-selected during power-up/power-down cycles or any event where the EEPROM is not intended to be selected. Furthermore, a pull-down resistor should be used on the PE pin of the 93XX76X and 93XX86X devices to prevent any unwanted writes during similar power-up/power-down events.

PROPER WRITE SEQUENCE

Microwire serial EEPROMs do not give you the ability to monitor whether or not the device is enabled for writes. Also, the 1-4K Microwire devices do not have a Program Enable pin to allow hardware to control when writes are allowed. It is up to the user to control exactly when the device is able to be written to and also protect the device after a write has been completed. Therefore, a Write command should not be considered complete until the Erase/Write Disable (EWDS) command has been issued following a Write command. So, all Write commands should begin with an Erase/Write Enable (EWEN), followed by the desired write sequence, and end with an Erase/Write Disable (EWDS). The EWDS command cannot be issued during the write cycle, any commands issued while a write is in progress will be ignored by the device.

This practice has two benefits. First, it protects the device further against unwanted writes in the event of a Reset or other system interruption. Second, by issuing a Start bit at the beginning of the Erase/Write Disable command, the device will reset the Ready/busy status on the DO line and return the device to a true Standby mode where the device will consume its least amount of current.

RESETTING THE STATE MACHINE

A Reset of the state machine can be accomplished by deselecting the device as long as the required number of clock cycles for a given command has not been reached. However, once the required clock cycles have been met, the command will execute upon completion of that command even if additional clocks are given after a valid command. Any additional clocks given to the device after a valid command are treated as “don’t cares”.

Additionally, if the device is suspected of having any type of power loss (POR or BOR) event, then once V_{CC} is restored, it is recommended that the CS line be toggled Low (inactive), High (Active), Low (inactive). This will allow for the state machine to have a better Reset and possibly be able to recover from a short or spurious power interruption. See Power-up/Power-down section for further details on POR/BOR events.

USING A HARDWARE SPI PORT FOR MICROWIRE COMMUNICATION

Many of today’s popular Microcontrollers offer a module that can be used to send SPI commands. The Microwire structure is set up in such a manner that many of these hardware protocol ports can be used to control the Microwire protocol by setting up the module correctly. The particulars of how to set up the port depend greatly on manufacturer, individual data sheets should be referenced for details. Microchip has Application Notes available on how to set this up for PIC® Microcontrollers.

THEORY OF OPERATION

To use an SPI port (MSSP) to communicate with Microchip’s Microwire Serial EEPROMs, the bytes to be output to the 93XXX must be aligned such that the LSB of the address is the 8th bit (LSB) of a byte to be output. From there the bits should fill the byte from right to left consecutively. If more that 8 bits are required, then two bytes will be required to be output. This same method will work for any 93XXX series device but the data sheet must be referenced for these because density and organization will change the number of bits sent for each command. We will use the 93LC66C organized in x16 format as an example below. Since more than 8 bits are required to control a 93LC66C, two consecutive bytes are required as shown in Figure 2.

High Byte (Where the Start bit, opcode bits and address MSb reside)

The High Byte is configured in the following format: SB is the Start bit. OP1 is the MSb of the op code and OP0 is the opcode LSb. The CS line can be set before the byte is output because the leading 0’s output to the 93XXX prevent a Start bit from being recognized by the 93XXX until the first high bit is sent.

Low Byte (8 Address bits)

The Low Byte contains A7-A0, which are the address bits required to access 256 bytes in x16 mode.

FIGURE 2: COMMAND ALIGNMENT

High Byte								Low Byte							
0	0	0	0	0	SB	OP1	OP0	A7	A6	A5	A4	A3	A2	A1	A0

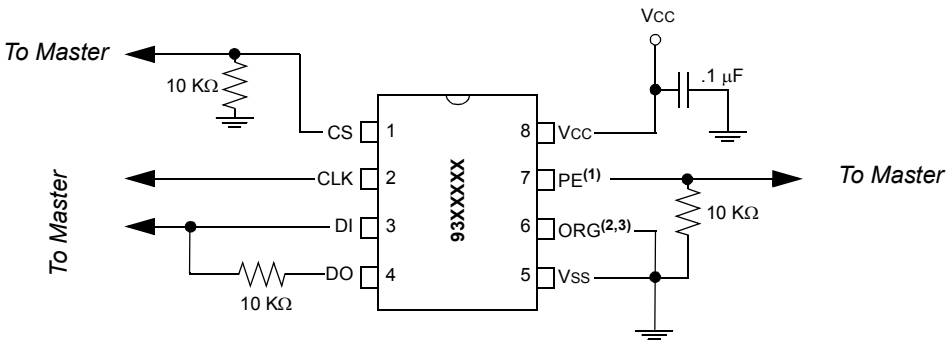
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TYING DI AND DO TOGETHER

Many customers inquire about making the Microwire protocol truly 3-wire by tying the DI and DO lines together. However, a potential for bus contention exists if the microcontroller attempts to drive the DI pin while the memory is driving DO. This is especially true when using an SPI port on the microcontroller and you rely on dummy zeros to be driven on the bus before the Start bit gets issued (since DO drives high for Ready until the next Start bit). To prevent this bus contention issue, it is necessary to use a series resistor (~10K Ohm) on the DO line from the DI line instead of a direct connection, as shown in Figure 3.

Another potential problem with tying DI and DO together occurs as CS is brought high after the write cycle has been initiated and valid clock transitions occur on the CLK line during the write cycle. This can cause the device to see an inadvertent Start condition when the write cycle ends (and the DO line drives high to signal the Ready state). This is caused by the fact that the TWC of the device is variable (depending on process, voltage and temperature) and, therefore, causes the write cycle to end in an asynchronous fashion with respect to the clock. For example, if CS is high when the write cycle ends and DO goes high (thereby pulling DI high), then a low-to-high transition on the CLK will be seen as a valid Start condition when it may not have been intended to be a Start condition.

FIGURE 3: Tying DI and DO Together



Note 1: PE pins exist on only the 93XX76X and 93XX86X devices.

Note 2: ORG is in x8 configuration when tied to VSS. For x16 operation, this pin needs to be tied to VCC.

Note 3: Devices with A or B suffix will not have an ORG pin.

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POWER-UP/POWER-DOWN

Microchip serial EEPROMs feature a high amount of protection from unintentional writes and data corruption while power is within normal operating levels. But certain considerations should be made regarding power-up and power-down conditions to ensure the same level of protection during those times when power is not within normal operating levels.

Power Failure During a Write Cycle

During a write cycle, VCC must remain above the minimum operating voltage for the entire duration of the cycle (typically 5 ms max. for most devices). If VCC falls below this minimum at any point for any length of time, data integrity cannot be ensured. It will result in marginally programmed data that may or may not be correct. Furthermore, because the EEPROM cells were not able to be fully programmed, the device will have shorter data retention time than specified in the data sheet.

Power-Up

On power-up, VCC should always begin at 0V and rise straight to its normal operating level to ensure a proper Power-on Reset. VCC should not linger at an ambiguous level (i.e., below the minimum operating voltage).

Brown-Out Conditions

If VCC happens to fall below the minimum operating voltage for the serial EEPROM, it is recommended that VCC be brought down fully to 0V before returning to normal operating level. This will help to ensure that the device is reset properly.

Furthermore, if the microcontroller features a Brown-out Reset with a threshold higher than that of the serial EEPROM, bringing VCC down to 0V will allow both devices to be reset together. Otherwise, the microcontroller may reset during communication while the EEPROM keeps its current state. In this case, a software Reset sequence would be required before beginning further communication.

CONCLUSION

Although not required for operation, utilizing these recommendations on Microwire Serial EEPROM designs will result in a more robust overall design. These recommendations fall directly in line with how Microchip designs, manufactures, qualifies and tests its Serial EEPROMs and will allow the devices to operate fully within the data sheet parameters.

QUESTION AND ANSWER

Q: What would happen if I inadvertently sent either too many or too few clocks during a Write command.

A: If you send too many clocks to the device and then drop the CS line to initiate the write cycle, the extra clocks will be ignored but the command will execute. If you do not send enough clocks and then drop the CS line, then the command will abort and no write will take place.

Q: I am using a 93LC56C device in my application and I am having problems getting it to work correctly. The read sequence seems to work fine, but I am unable to write any data to the part.

A: First, make sure you are issuing an EWEN command prior to attempting a write. But a problem such as this is usually caused by either not giving the part the required number of bits for the command before dropping the CS line or by not dropping the CS line at all. The Write command will not commence until the CS line is brought low.

Q: I am confused, do I have to toggle the CS line low in-between every command?

A: Yes, the CS line must go low for at least 250 ns between each command. If you are doing a Write command and you bring CS low to activate the Data Polling mode, you must toggle CS low again after the Ready signal has been given by the device before the next Start bit can be sent.

Q: If VCC drops during a write cycle will other data in the array be corrupted, or just the data being written?

A: Only the data being written will be corrupted if VCC goes away during a write cycle. Other data bytes will be unaffected.

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AN1040

Recommended Usage of Microchip SPI Serial EEPROM Devices

Author: *Chris Parris*
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INTRODUCTION

The majority of embedded control systems require nonvolatile memory. Because of their small footprint, byte level flexibility, low I/O pin requirement, low-power consumption and low cost, serial EEPROMs are a popular choice for nonvolatile storage. Microchip Technology has addressed this need by offering a full line of serial EEPROMs covering industry standard serial communication protocols for two-wire (I^2C™), three-wire (Microwire), and SPI communication. Serial EEPROM devices are available in a variety of densities, operational voltage ranges and packaging options.

In order to achieve a highly robust application when utilizing serial EEPROMs, the designer must consider more than just the data sheet specifications.

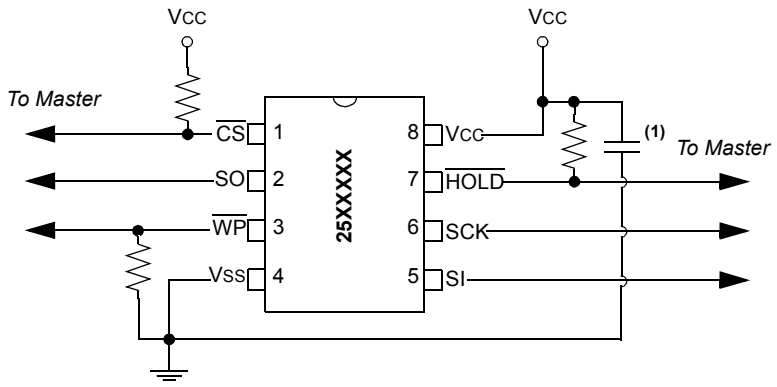
There are a number of conditions which could potentially result in nonstandard operation. The details of such conditions depend greatly upon the serial protocol being used.

This application note provides assistance and guidance with the use of Microchip SPI serial EEPROMs. These recommendations are not meant as requirements; however, their adoption will lead to a more robust overall design. The following topics are discussed:

- Input Considerations
- Write-Protection Features
- Power Supply
- Write Enable and Disable
- WIP Polling
- Increasing Data Throughput

Figure 1 shows the suggested connections for using Microchip SPI serial EEPROMs. The basis for these connections will be explained in the sections which follow.

FIGURE 1: RECOMMENDED CONNECTIONS FOR 25XXXX SERIES DEVICES



Note 1: A decoupling capacitor (typically 0.1 μF) should be used on VCC.

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INPUT CONSIDERATIONS

It is never good practice to leave an input pin floating. This can cause high standby current as well as undesired functionality. If a pin is left floating, it can either float low or high. Which direction the signal goes is dependant upon a number of factors, including noise in the system and capacitive coupling. Because of this, the level seen by the input circuitry is relatively random and likely to change during operation.

Such unpredictable input levels can have devastating effects on device operation. For example, Microchip's SPI serial EEPROMs feature a $\overline{\text{HOLD}}$ pin which allows the user to suspend the clock mid-stream. If this pin were to float low (active), the device would no longer react to any clock pulses received and communication would be disrupted.

Therefore, any unused input pins should always be tied to a proper level, such as high for an active-low input. Moreover, it is recommended that, if the microcontroller has extra, tri-state I/O pins available, connections be made to these unused inputs along with a pull-down/pull-up resistor, as shown in Figure 1. This will allow for the inputs to be used at a later date simply by modifying firmware.

Although the $\overline{\text{CS}}$ pin should always be driven by the microcontroller during normal operation, it has potential for floating during power-down/power-up. As such, this pin should also have a pull-up resistor to avoid undesired commands due to noise during these conditions.

WRITE PROTECTION FEATURES

There are two different write protection schemes featured in Microchip's SPI serial EEPROM family of devices. One for the 4 Kb and smaller devices, and one for 8 Kb and larger devices.

For the 25XX010A to 25XX040A, the $\overline{\text{WP}}$ pin acts as a normal hardware write-protect pin. That is, if the $\overline{\text{WP}}$ pin is low (active), the Write Enable Latch (WEL) is cleared and cannot be set until the pin is brought high (inactive). This means that any attempted writes to either the array or the STATUS register will be blocked. Note that bringing the $\overline{\text{WP}}$ pin high does not set the WEL again. Another `WREN` instruction is required in order to do this.

For the 25XX080A/B and up, the $\overline{\text{WP}}$ pin acts in conjunction with the Write-Protect Enable (WPEN) bit in the STATUS register. If the WPEN bit is cleared, the $\overline{\text{WP}}$ pin is a don't care. If the WPEN bit is set, the $\overline{\text{WP}}$ pin can be used to block attempted STATUS register writes. Note that for these devices, the $\overline{\text{WP}}$ pin has no effect on array writes, regardless of the state of the WPEN bit. Only the Block Protect (BP) bits can block an attempted write to the array on these devices. Once the BP bits have been set, however, the $\overline{\text{WP}}$ pin can be used with the WPEN bit to prevent them from being cleared, thus preventing writes to the array as well.

POWER SUPPLY

Microchip serial EEPROMs feature a high amount of protection from unintentional writes and data corruption while power is within normal operating levels. But certain considerations should be made regarding power-up and power-down conditions to ensure the same level of protection during those times when power is not within normal operating levels.

As shown in Figure 1, a decoupling capacitor (typically 0.1 μF) should be used to help filter out small ripples on V_{CC}.

Power-Up

On power-up, V_{CC} should always begin at 0V and rise straight to its normal operating level to ensure a proper Power-on Reset. V_{CC} should not linger at an ambiguous level (i.e., below the minimum operating voltage).

Brown-Out Conditions

For added protection, Microchip serial EEPROMs feature a Brown-out Reset circuit. However, if V_{CC} happens to fall below the minimum operating voltage for the serial EEPROM, it is recommended that V_{CC} be brought down fully to 0V before returning to normal operating level. This will help to ensure that the device is reset properly.

Furthermore, if the microcontroller features a Brown-out Reset with a threshold higher than that of the serial EEPROM, bringing V_{CC} down to 0V will allow both devices to be reset together. Otherwise, the microcontroller may reset during communication while the EEPROM keeps its current state. In this case, a software Reset sequence would be required before beginning further communication.

Power Failure During a Write Cycle

During a write cycle, V_{CC} must remain above the minimum operating voltage for the entire duration of the cycle (typically 5 ms max. for most devices). If V_{CC} falls below this minimum voltage at any point for any length of time, data integrity cannot be ensured. It will result in marginally programmed data that may or may not be correct. Furthermore, because the EEPROM cells were not able to be fully programmed, the device will have shorter data retention time than specified in the data sheet.

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WRITE ENABLE AND DISABLE

Microchip SPI serial EEPROMs feature a Write Enable Latch (WEL) as bit 1 of the STATUS register. This latch is used to allow write operations to occur to the array or STATUS register. When set to a '1', writes are enabled. When set to a '0', all writes are blocked. The WEL can only be set by issuing a valid Write Enable (WREN) instruction, but can be reset upon a number of conditions:

- Power-up
- Write Disable (WRDI) instruction successfully executed
- Write STATUS register (WRSR) instruction successfully executed
- Write instruction successfully executed

And on the 25XX010A-25XX040A only:

- $\overline{WP}$ pin is brought low (active)

Note that for the Write, WRSR, and WRDI instructions, the WEL is only reset if the instruction is executed successfully. This means that if, for some reason, the instruction is not valid, the WEL will not be reset. For example, if a write is attempted in an area of the array protected by the Block Protect (BP) bits, then the instruction will not succeed and the WEL will remain set.

For Write and WRSR instructions, the WEL is cleared at the end of the write cycle.

It is highly recommended that the WEL only be set immediately before issuing a Write or WRSR instruction in order to minimize the chance of an undesired write operation.

WIP POLLING

Write operations on serial EEPROMs require that a write cycle time be observed after initiating the write, allowing the device time to store the data. During this time, normal device operation is disabled and any attempts by the master to access the memory array on the device will be ignored. Therefore, it is important that the master wait for the write cycle to end before attempting to access the EEPROM again.

Each device has a specified worst-case write cycle time, typically listed as TWC. A simple method for ensuring that the write cycle time is observed is to perform a delay for the amount of time specified before accessing the EEPROM again. However, it is not uncommon for a device to complete a write cycle in less than the maximum specified time. As such, using the previously shown delay method results in a period of time in which the EEPROM has finished writing, but the master is still waiting.

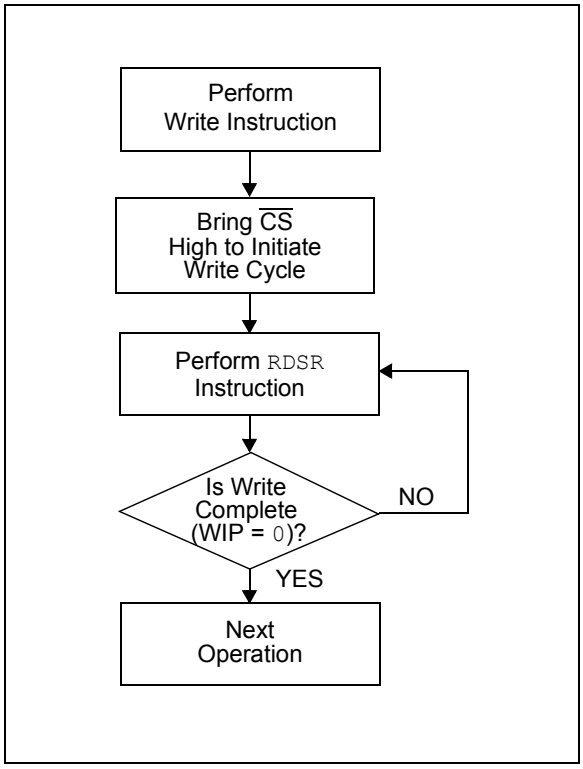
In order to eliminate this extra period of time, and therefore operate more efficiently, it is highly recommended to take advantage of the WIP Polling feature.

During both an array write and a STATUS register write, the STATUS register in Microchip's SPI serial EEPROMs can still be read. This allows the user to check the state of the Write-In-Progress (WIP) bit. This is a read-only bit, set only while a write operation is in progress. Once the operation completes, the WIP (and the WEL) are cleared. Therefore, the STATUS register can continue to be read in order to monitor the value of the WIP bit to determine when the write cycle completes.

Procedure

Once $\overline{CS}$ is brought high at the end of the Write instruction, the device initiates the internally timed write cycle, and WIP polling can begin immediately. This involves performing a Read STATUS register (RDSR) instruction and checking the value read for the WIP bit. If it is high, the device is still writing. If it is low, the write cycle is complete and the master can proceed with the next instruction. See Figure 2 for details.

FIGURE 2: WIP POLLING FLOW



INCREASING DATA THROUGHPUT

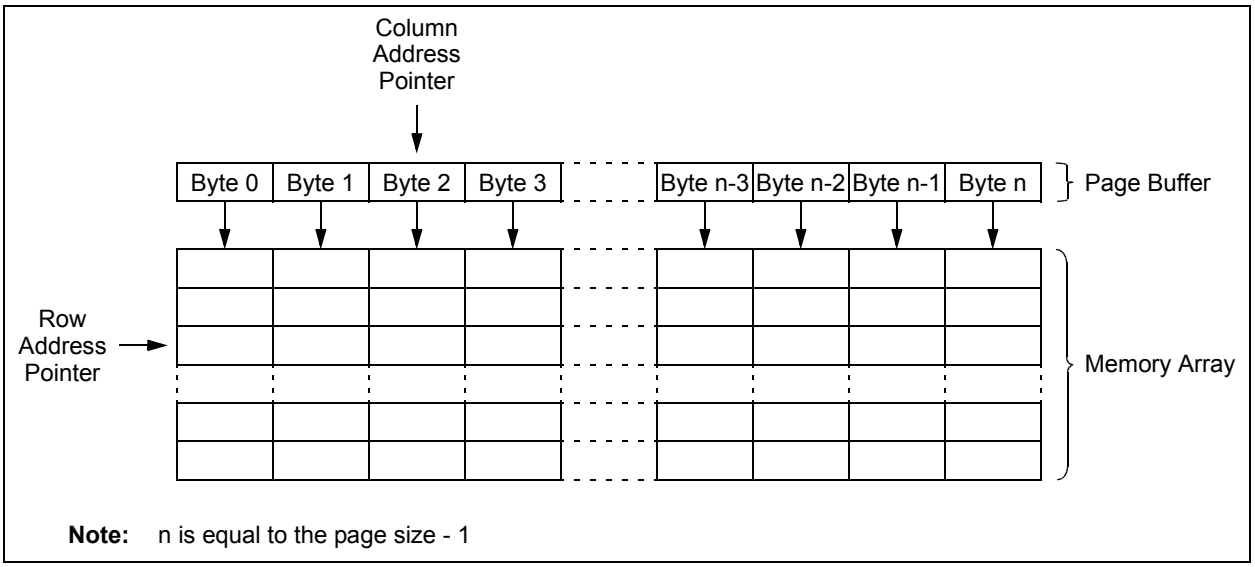
Page Writes

All Microchip SPI serial EEPROMs feature a page buffer for use during write operations. This allows the user to write any number of bytes from one to the maximum page size in a single operation. This can provide for a significant decrease in the total write time when writing a large number of bytes.

Page write operations are limited to writing within a single physical page, regardless of the number of bytes actually being written. This is because the memory array is physically stored as a two-dimensional array, as shown in Figure 3. When the word address is given at the beginning of a write operation, both the row and column Address Pointers are set. The row Address Pointer selects which row, or page, is accessed, whereas the column Address Pointer selects which byte from the chosen page is accessed first. Upon transmission of each data byte, the column Address Pointer is automatically incremented. However, during a write operation, the page Address Pointer is not incremented, which means that attempting to cross a page boundary during a page write operation will result in the data being looped back to the beginning of the page.

Note that physical page boundaries start at addresses that are multiples of the page size. For example, the 25XX256 features a 64-byte page size, which means that physical pages on the device begin at addresses 0x0000, 0x0040, 0x0080, and so on.

FIGURE 3: PAGE BUFFER BLOCK DIAGRAM



Procedure

After enabling writes by issuing a WREN command, the write instruction, word address, and the first data byte are transmitted to the device in the same way as in a byte write operation. But instead of toggling $\overline{CS}$ high, the master continues transmitting additional data bytes, which are temporarily stored in the on-chip page buffer, up to the maximum page size of the device (with care being taken not to wrap around the page). As with the byte write operation, once $\overline{CS}$ is toggled high, an internal write cycle will begin during which all bytes stored in the page buffer will be written.

Write Time Comparisons

In order to accurately calculate the full period of time required to write a particular amount of data to a device, two things must be considered.

- **Load time** is the amount of time needed to complete all bus operations. This includes all $\overline{CS}$-related timings, issuing the necessary `WREN` instructions, as well as transmitting the Write instruction, address and data bytes. This amount of time is dependent on the bus clock speed, the number of data bytes to be written, and the addressing scheme of the particular device (some devices utilize a 1-byte address, whereas others use a 2-byte address).

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- **Write cycle time** is the time during which the device is executing its internal write cycle. As described in the previous section ("WIP Polling"), there is a specified maximum write cycle time for each device. However, the internal write cycle typically completes in less time than specified. As such, both worst-case (5 ms) and typical (3 ms at TAMB = 25 °C) calculations are provided in Table 1.

The following equations were used to calculate the values for Table 1:

EQUATION 1: WRITE TIME EQUATIONS

$$T_{LOAD} = \frac{8 \cdot (2 + \#\text{ addr bytes} + \#\text{ data bytes})}{F_{CLK}} + 150\text{ ns}$$

$$T_{TOTAL} = (T_{LOAD} + T_{WC}) \cdot \#\text{ write operations}$$

TABLE 1: WRITE TIME COMPARISONS

Device	Page Size (bytes)	# of Bytes to Write	Write Mode(1)	Clock Speed (MHz)	Load Time Per Operation (µs)	Total Time (ms) Worst-Case(2)	Total Time (ms) Typical(3)
25LC010A	16	1	Byte	1	32.15	5.03	3.03
		16	Byte	1	32.15	80.51	48.51
		16	Page	1	152.15	5.15	3.15
		1	Byte	10	3.35	5.00	3.00
		16	Byte	10	3.35	80.05	48.05
		16	Page	10	15.35	5.02	3.02
25LC160B	32	1	Byte	1	40.15	5.04	3.04
		32	Byte	1	40.15	161.28	97.28
		32	Page	1	288.15	5.29	3.29
		1	Byte	10	4.15	5.00	3.00
		32	Byte	10	4.15	160.13	96.13
		32	Page	10	28.95	5.03	3.03
25LC256	64	1	Byte	1	40.15	5.04	3.04
		64	Byte	1	40.15	322.57	194.57
		64	Page	1	544.15	5.54	3.54
		1	Byte	10	4.15	5.00	3.00
		64	Byte	10	4.15	320.27	192.27
		64	Page	10	54.55	5.05	3.05

Note 1: Byte Write mode signifies that only 1 byte is written during a single write operation. Page Write mode signifies that a full page is written during a single write operation.

2: Worst-case calculations assume a 5 ms timed delay is used.

3: Typical calculations assume WIP polling is used, with typical TWC = 3 ms, TAMB = 25 °C.

From these examples, it is clear that both page writes and WIP polling can provide significant time savings. Writing 64 bytes to the 25LC256 via byte writes at 1 MHz requires roughly 320 ms worst-case. Switching to WIP polling brings that down to roughly 192 ms (assuming typical conditions), nearly a 40% decrease. Additionally, changing to page writes further lowers the time to an impressive 3.05 ms, a decrease of over 98%. Overall, the two techniques provide a combined time savings of over 317 ms, increasing the total data throughput a staggering 105 times over.

SUMMARY

This application note illustrates recommended techniques for increasing design robustness when using Microchip SPI serial EEPROMs. These recommendations fall directly in line with how Microchip designs, manufactures, qualifies and tests its serial EEPROMs and will allow the devices to operate within the data sheet parameters. It is suggested that the concepts detailed in this application note be incorporated into any system which utilizes an SPI serial EEPROM.

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NOTES:

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SECTION 5
PACKAGING

Package Outline Drawings 5-1
Product Tape and Reel Specifications 5-11
Solder Reflow Recommendation 5-19
Overview of Microchip Die/Wafer Support 5-23

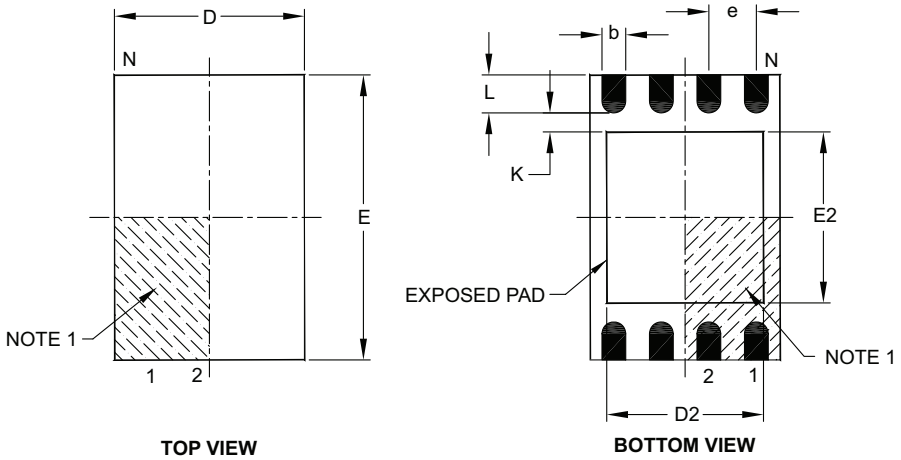
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Package Outline Drawings

8-Lead Plastic Dual Flat, No Lead Package (MC) – 2x3x0.9 mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		2.00 BSC	
Overall Width	E		3.00 BSC	
Exposed Pad Length	D2	1.30	–	1.75
Exposed Pad Width	E2	1.50	–	1.90
Contact Width	b	0.18	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

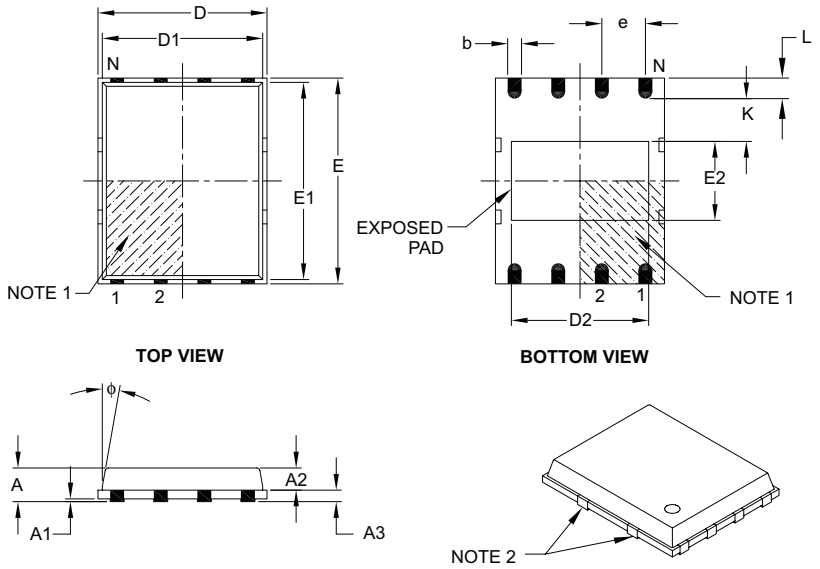
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-123B

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8-Lead Plastic Dual Flat, No Lead Package (MF) – 6x5 mm Body [DFN-S] PUNCH SINGULATED

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	–	0.85	1.00
Molded Package Thickness	A2	–	0.65	0.80
Standoff	A1	0.00	0.01	0.05
Base Thickness	A3		0.20 REF	
Overall Length	D		4.92 BSC	
Molded Package Length	D1		4.67 BSC	
Exposed Pad Length	D2	3.85	4.00	4.15
Overall Width	E		5.99 BSC	
Molded Package Width	E1		5.74 BSC	
Exposed Pad Width	E2	2.16	2.31	2.46
Contact Width	b	0.35	0.40	0.47
Contact Length	L	0.50	0.60	0.75
Contact-to-Exposed Pad	K	0.20	–	–
Model Draft Angle Top	ϕ	–	–	12°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

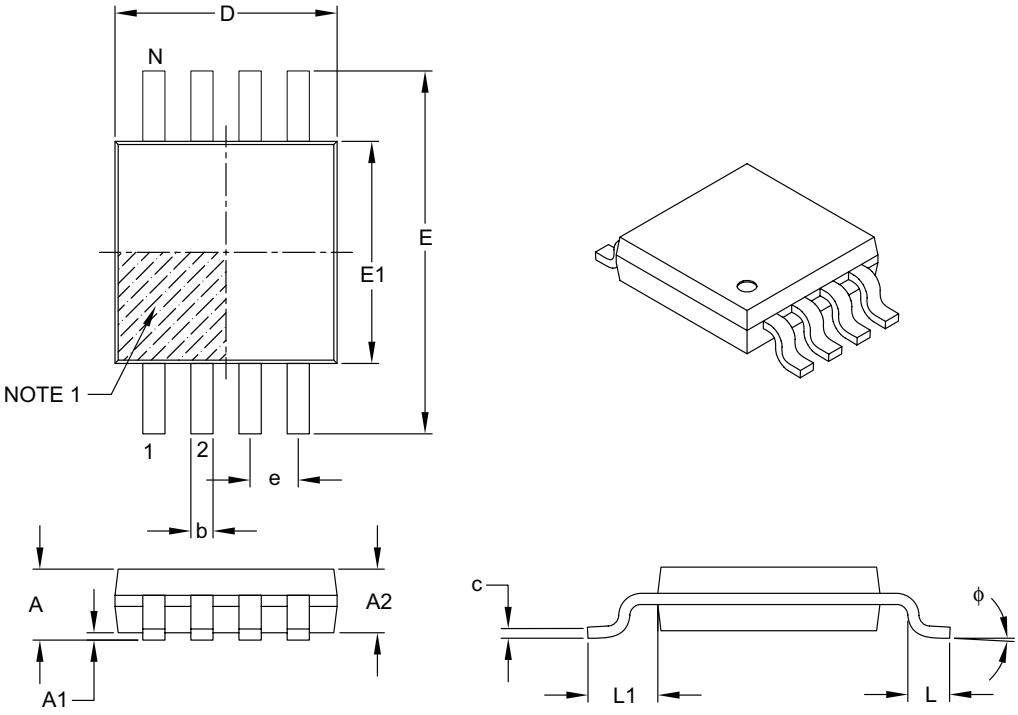
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-113B

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8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	–	0.15
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Overall Length	D		3.00 BSC	
Foot Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.08	–	0.23
Lead Width	b	0.22	–	0.40

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

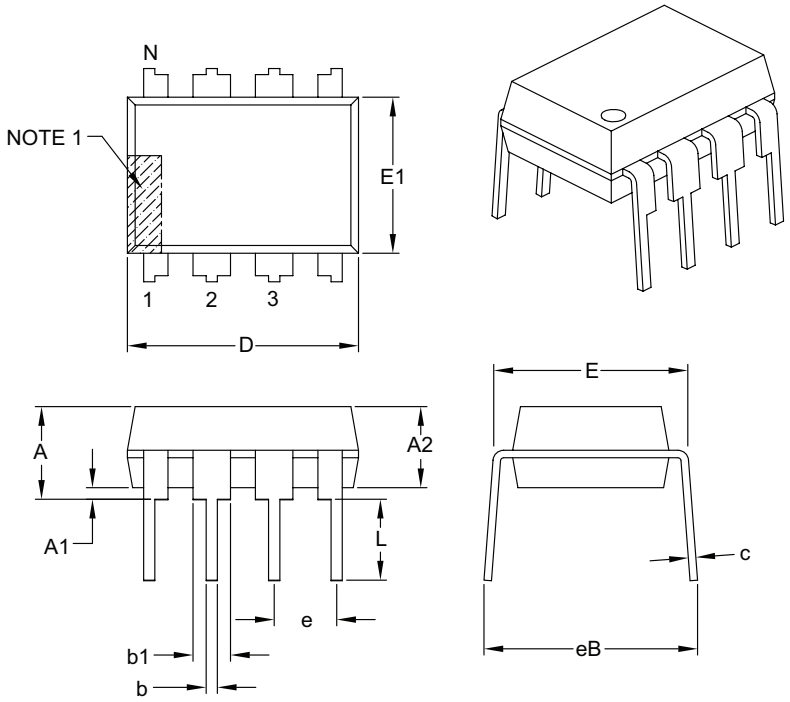
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111B

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8-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

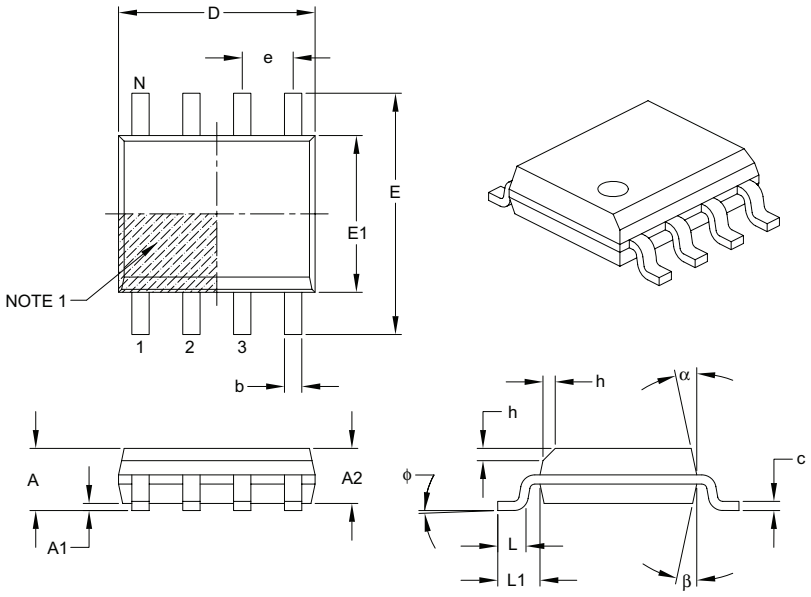
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-018B

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8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

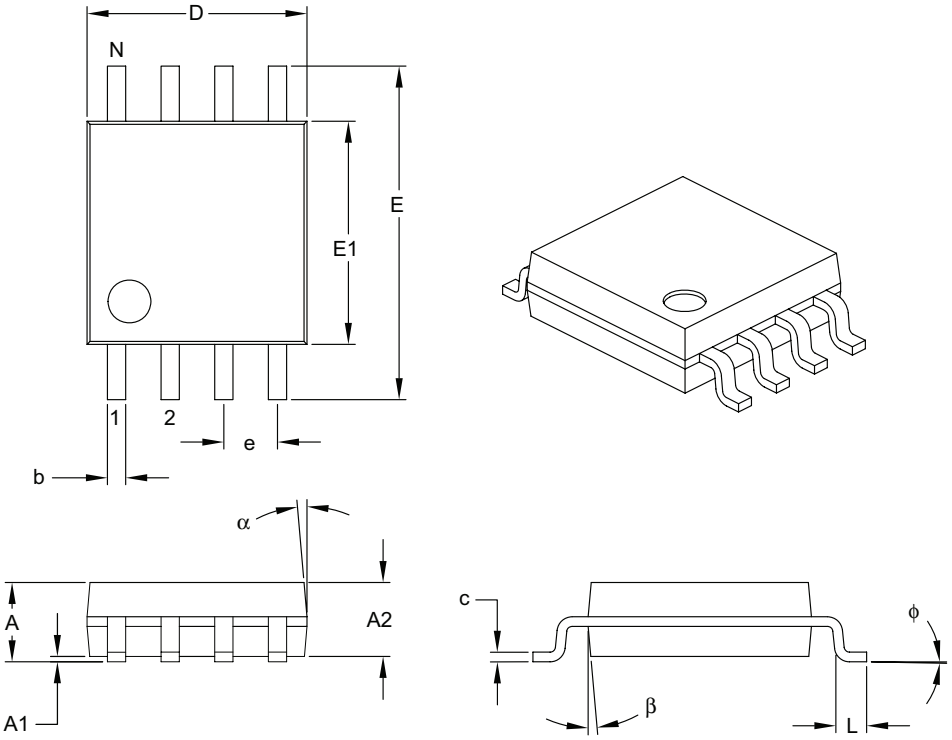
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-057B

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8-Lead Plastic Small Outline (SM) – Medium, 5.28 mm Body [SOIJ]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	1.77	–	2.03
Molded Package Thickness	A2	1.75	–	1.98
Standoff §	A1	0.05	–	0.25
Overall Width	E	7.62	–	8.26
Molded Package Width	E1	5.11	–	5.38
Overall Length	D	5.13	–	5.33
Foot Length	L	0.51	–	0.76
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.15	–	0.25
Lead Width	b	0.36	–	0.51
Mold Draft Angle Top	α	–	–	15°
Mold Draft Angle Bottom	β	–	–	15°

Notes:

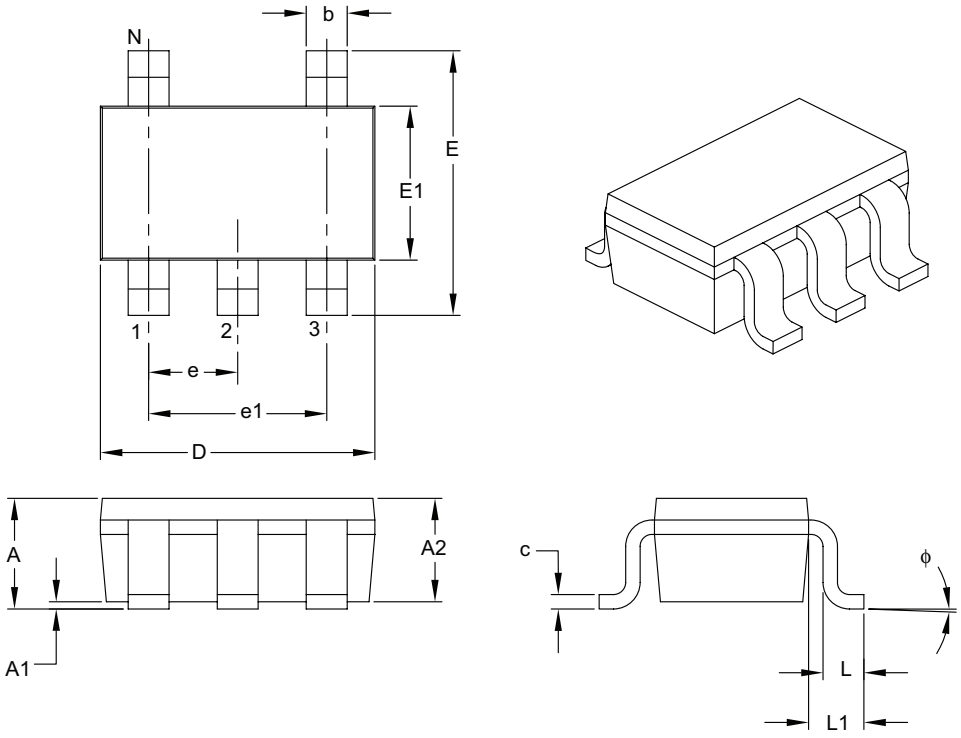
1. SOIJ, JEITA/EIAJ Standard, formerly called SOIC.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.

Microchip Technology Drawing C04-056B

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5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		5	
Lead Pitch	e		0.95 BSC	
Outside Lead Pitch	e1		1.90 BSC	
Overall Height	A	0.90	–	1.45
Molded Package Thickness	A2	0.89	–	1.30
Standoff	A1	0.00	–	0.15
Overall Width	E	2.20	–	3.20
Molded Package Width	E1	1.30	–	1.80
Overall Length	D	2.70	–	3.10
Foot Length	L	0.10	–	0.60
Footprint	L1	0.35	–	0.80
Foot Angle	ϕ	0°	–	30°
Lead Thickness	c	0.08	–	0.26
Lead Width	b	0.20	–	0.51

Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

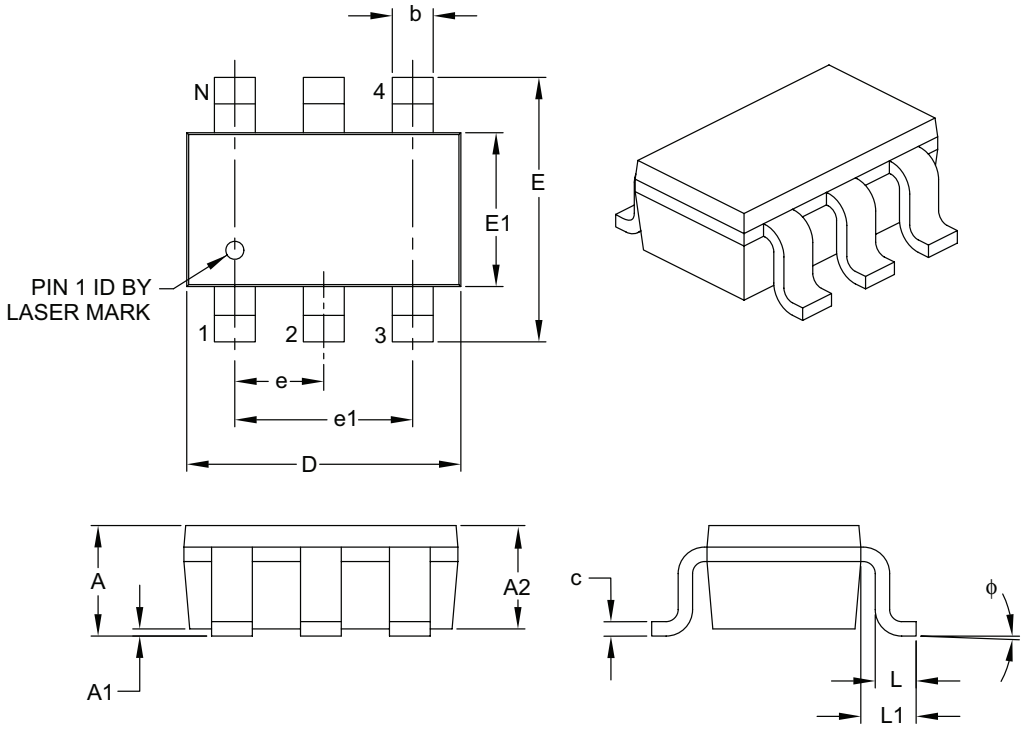
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-091B

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6-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		6	
Pitch	e		0.95 BSC	
Outside Lead Pitch	e1		1.90 BSC	
Overall Height	A	0.90	–	1.45
Molded Package Thickness	A2	0.89	–	1.30
Standoff	A1	0.00	–	0.15
Overall Width	E	2.20	–	3.20
Molded Package Width	E1	1.30	–	1.80
Overall Length	D	2.70	–	3.10
Foot Length	L	0.10	–	0.60
Footprint	L1	0.35	–	0.80
Foot Angle	ϕ	0°	–	30°
Lead Thickness	c	0.08	–	0.26
Lead Width	b	0.20	–	0.51

Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

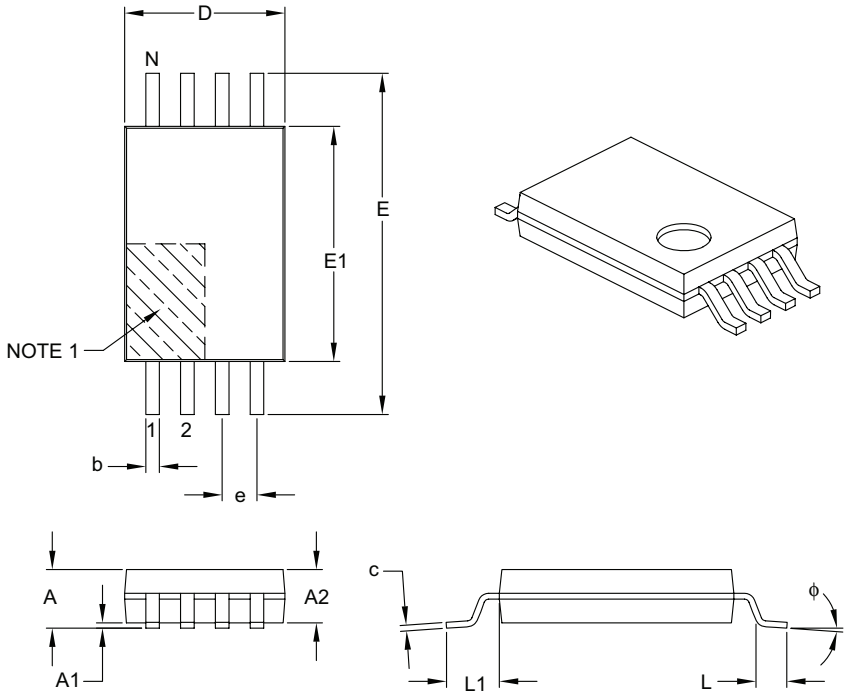
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-028B

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8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	–	0.15
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	2.90	3.00	3.10
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.19	–	0.30

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-086B

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NOTES:

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Product Tape and Reel Specifications

FIGURE 1: EMBOSSED CARRIER DIMENSIONS (8, 12, 16, AND 24 MM TAPE ONLY)

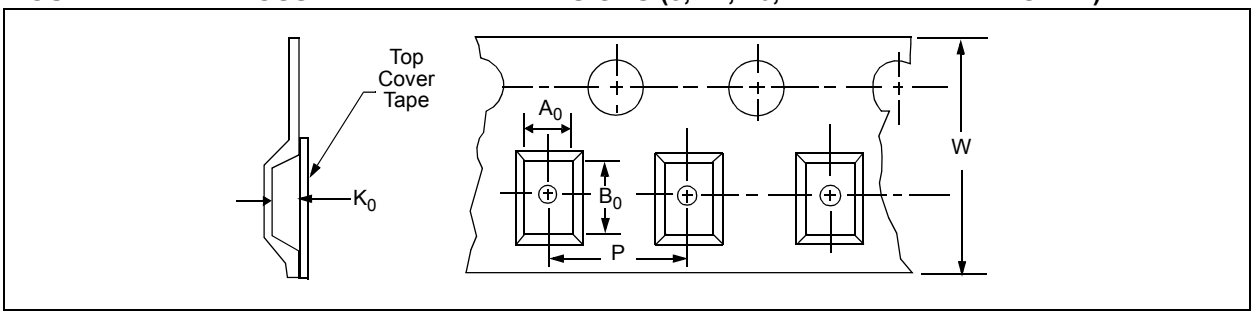


TABLE 1: CARRIER TAPE/CAVITY DIMENSIONS

Case Outline	Package Type		Carrier Dimensions		Cavity Dimensions			Output Quantity Units	Reel Diameter in mm
			W mm	P mm	A0 mm	B0 mm	K0 mm		
SN	SOIC .150”	8L	12	8	6.4	5.2	2.1	3300	330
SO	SOIC .300”	16L	16	12	10.9	10.7	3.0	1000	330
SO	SOIC .300”	18L	24 24	12 16	10.9 11.1	13.3 12.0	3.0 2.8	1600 1100	330 330
SO	SOIC .300”	20L	24	12	10.9	13.3	3.0	1600	330
SO	SOIC .300”	24L	24	12	10.9	16.0	3.0	1000	330
SO	SOIC .300”	28L	24 24	12 12	10.9 11.1	18.3 18.5	3.0 3.0	1600 1600	330 330
L	PLCC	28L	24	16	13.0	13.0	4.9	750	330
L	PLCC	32L	24	16	13.1	15.5	3.9	900	330
L	PLCC	44L	32 32	24 24	18.0 18.0	18.0 18.0	4.9 5.0	500 500	330
L	PLCC	68L	44	32	25.6	25.6	5.8	300	330
L	PLCC	84L	44	36	30.7	30.7	5.8	200	330
SM	SOIC .208”	8L	16	12	8.3	5.7	2.3	2100	330
SL	SOIC .150”	14L	16	8	6.5	9.5	2.1	2600	330
SL	SOIC .150”	16L	16	8	6.5	10.3	2.1	2600	330
TS	TSOP	28L/32L	32	16	8.6	20.6	2.1	1500	330
SS	SSOP	20L	16	12	8.4	7.7	2.5	1600	330
SS	SSOP	28L	24	12	8.4	10.9	2.4	2100	330
PQ	MQFP	44L	24	24	14.2	14.2	2.8	900	330
PT	TQFP	44L/64L	24	16	12.4	12.4	2.2	1200	330
VS	VSOP	28L	24	12	8.7	13.9	2.1	2500	330

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TABLE 1: CARRIER TAPE/CAVITY DIMENSIONS (CONTINUED)

Case Outline	Package Type		Carrier Dimensions		Cavity Dimensions			Output Quantity Units	Reel Diameter in mm
			W mm	P mm	A0 mm	B0 mm	K0 mm		
ST	TSSOP	8L	12	8	7.0	3.6	1.6	2500	330
ST	TSSOP	14L	16	8	6.8	5.4	1.6	2500	330
ST	TSSOP	20L	16	8	6.8	6.9	1.6	2500	330
TT	SOT-23	3L	8	4	3.15	2.77	1.22	3000	180
OT	SOT-23	5L/6L	8	4	3.2	3.2	1.4	3000	180
MS	MSOP	8L/10L	12	8	5.3	3.6	1.4	2500	330
LT	SC-70	5L	8	4	2.24	2.34	1.22	3000	180
MF	DFN 3x3		12	8	3.3	3.3	1.1	3300	330
MF	DFN 5x6		12	8	5.3	6.3	1.2	3300	330
ML	QFN 6x6		16	12	6.3	6.3	1.1	1600	330
ML	QFN 8x8		16	12	8.3	8.3	1.1	1600	330

FIGURE 2: SOP, SOIC, MSOP, QSOP DEVICES

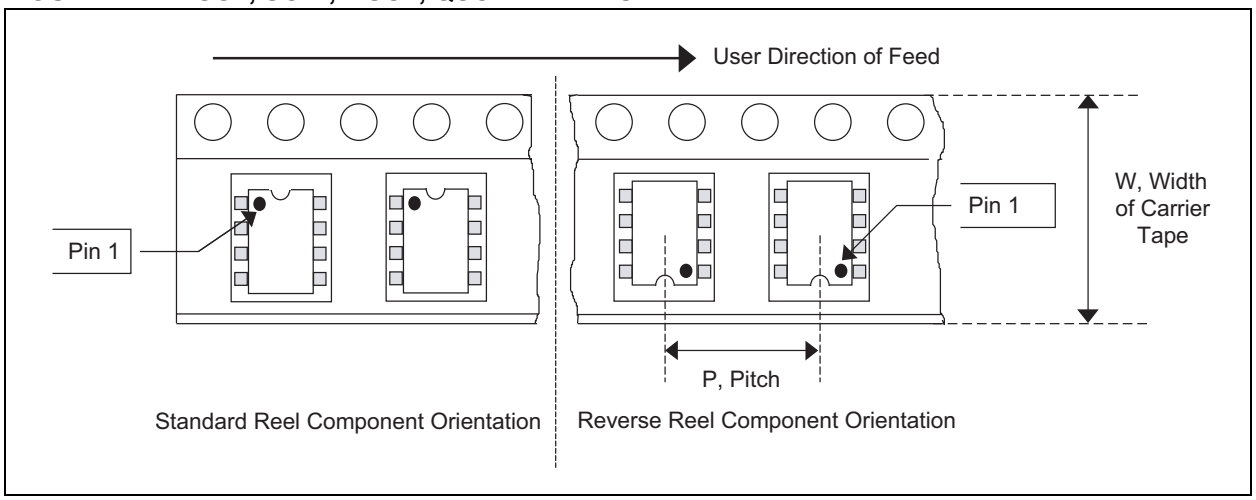
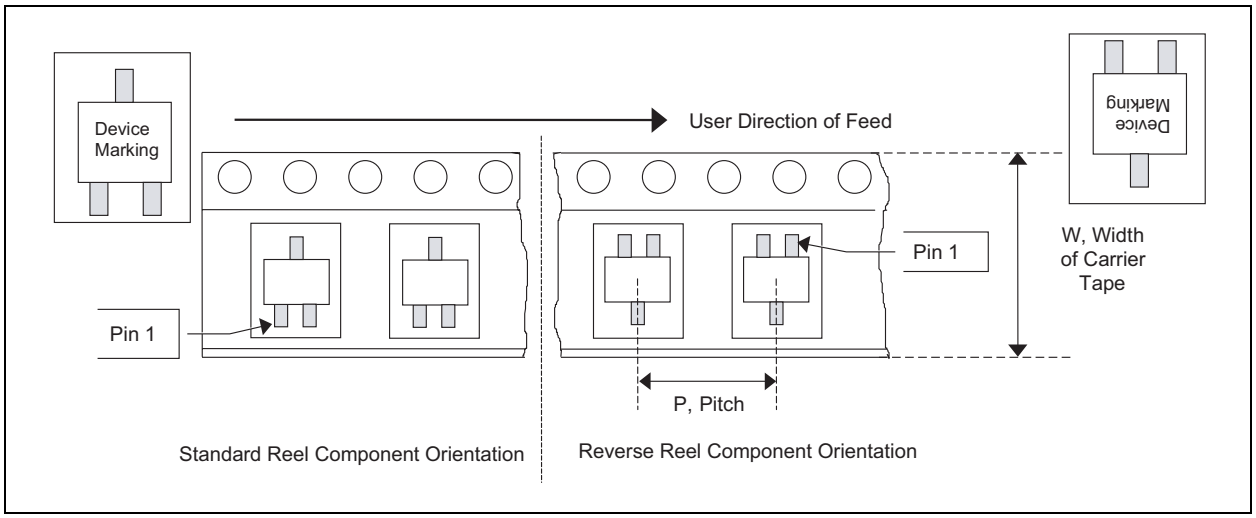


FIGURE 3: 3L SOT-23/SC-70 DEVICES



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FIGURE 4: 5L SOT-23/SC-70 DEVICES

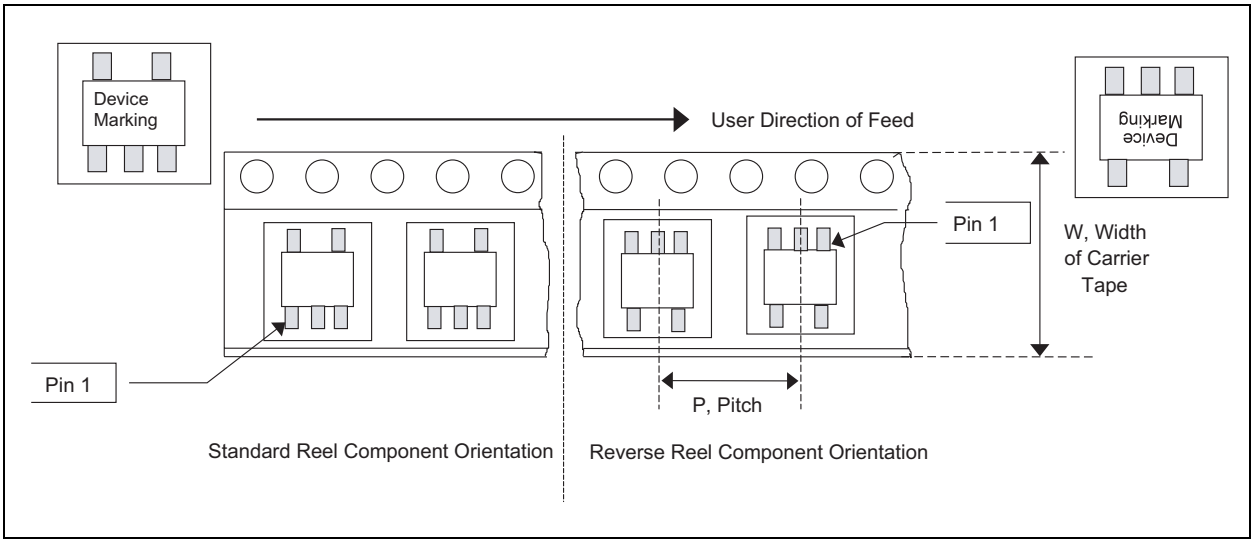
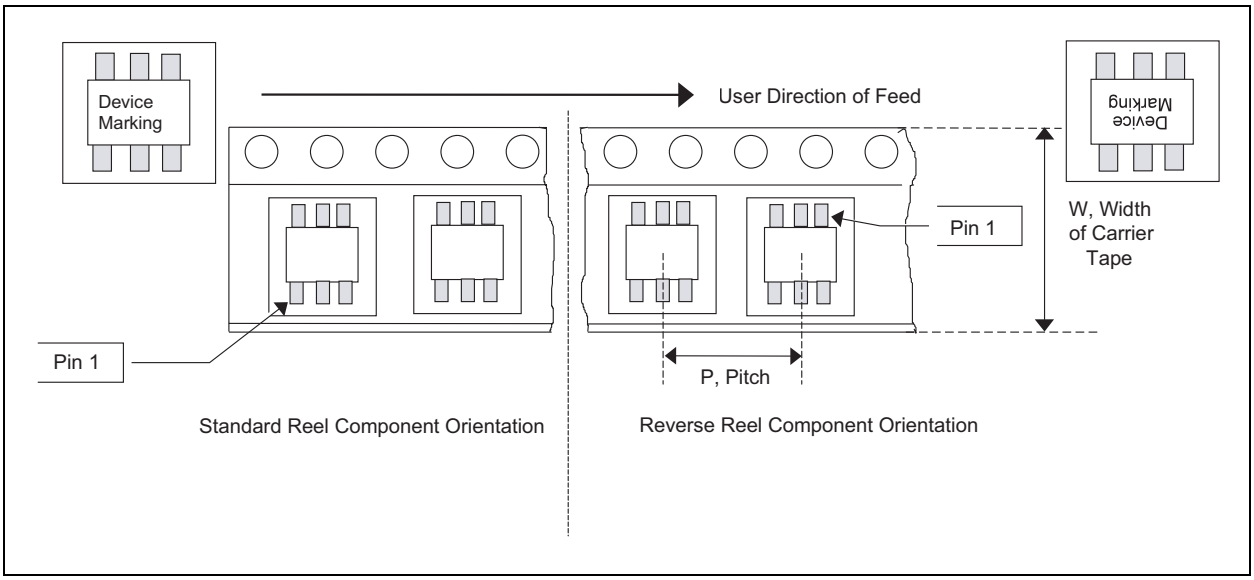


FIGURE 5: 6L SOT-23 DEVICES



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FIGURE 6: 3L SOT-223 DEVICES

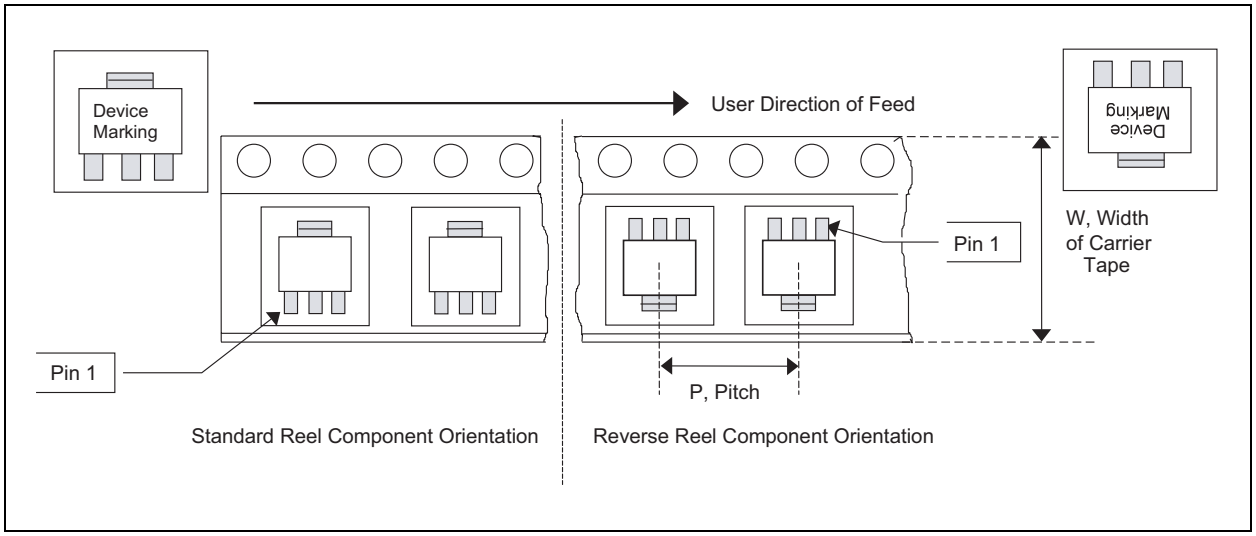
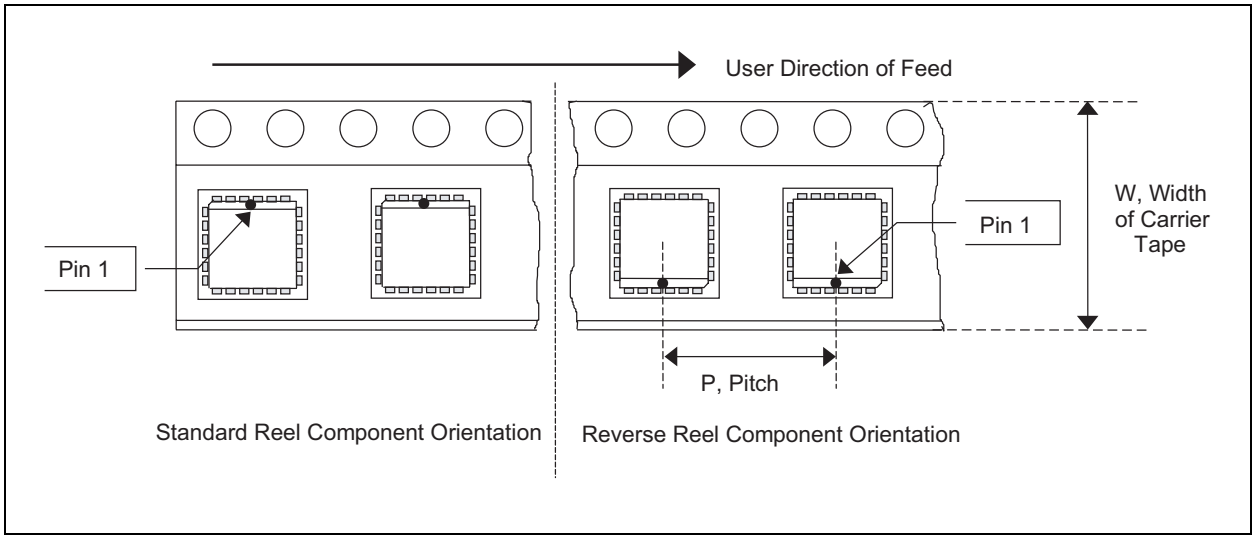


FIGURE 7: PLCC DEVICES



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FIGURE 8: MQFP DEVICES

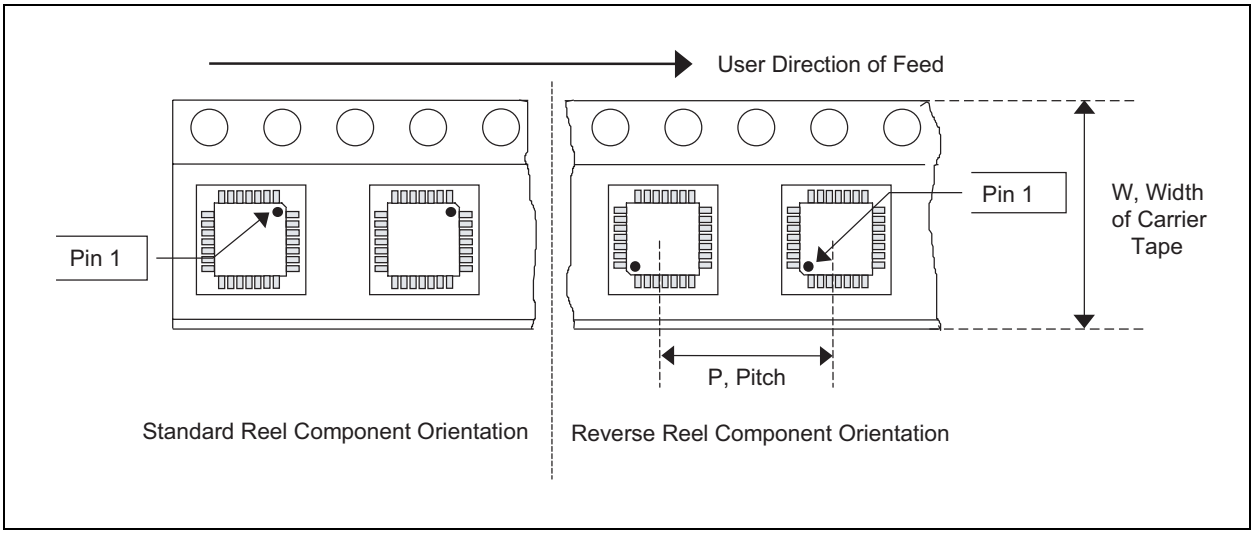


FIGURE 9: 4L SOT-143 DEVICES

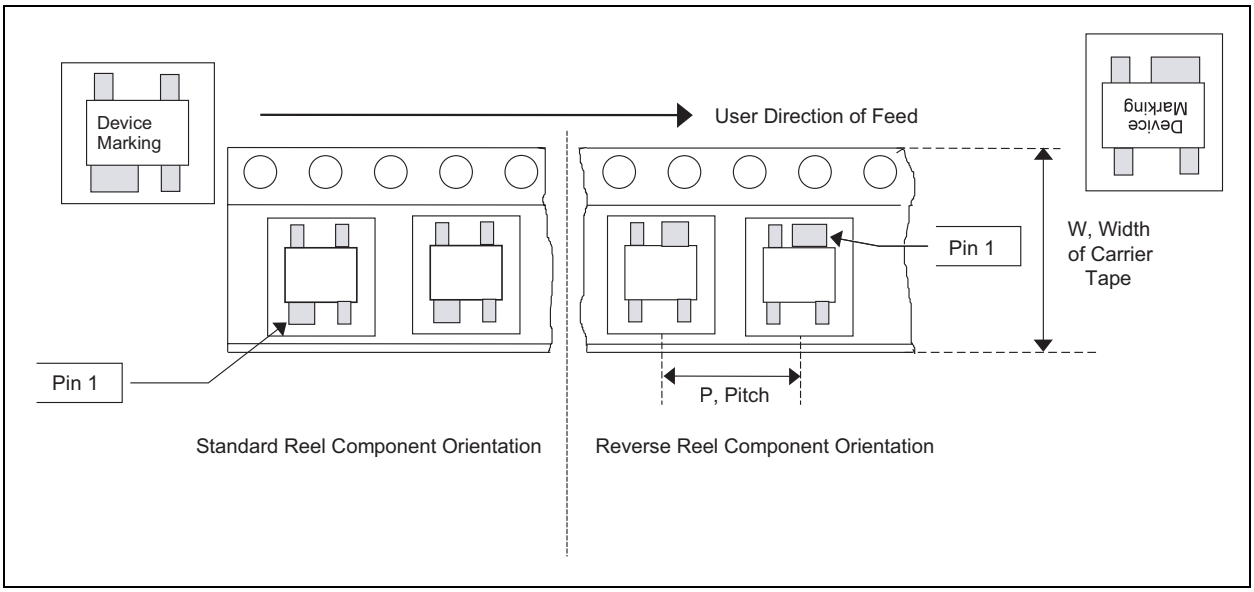


FIGURE 10: 3L/5L/7L DDPAK AND 3L DPAK DEVICES

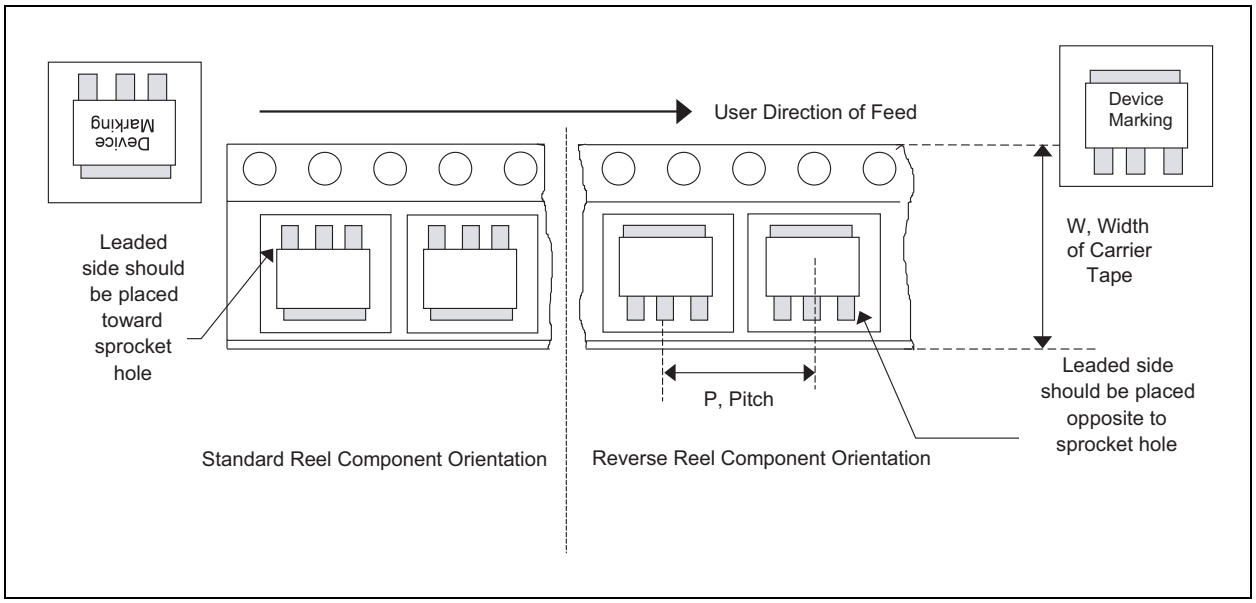


FIGURE 11: SOT-89 DEVICES

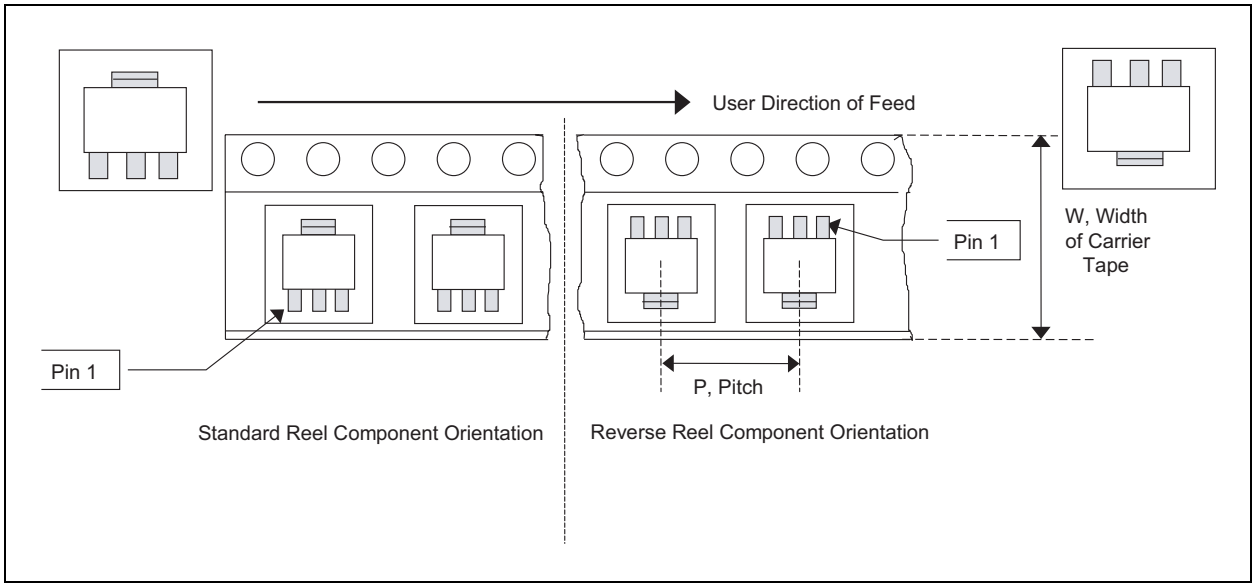
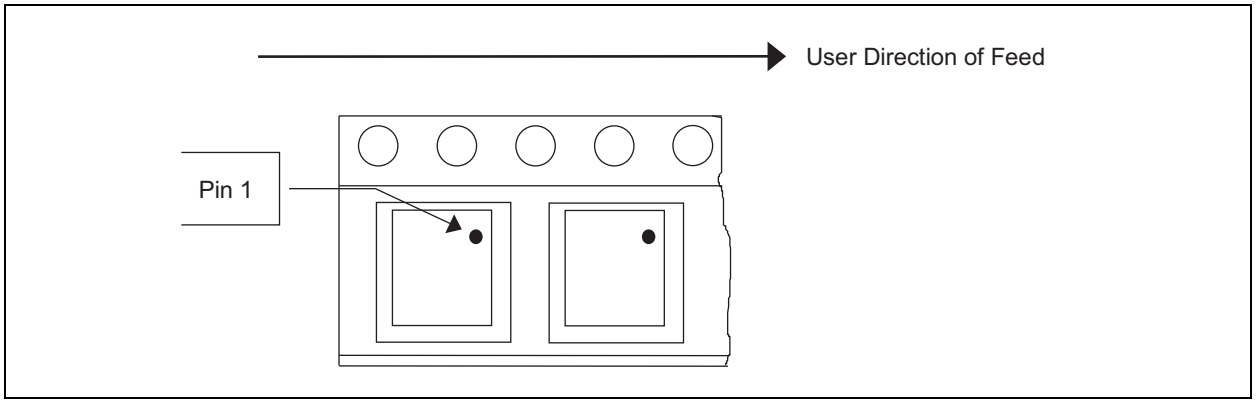
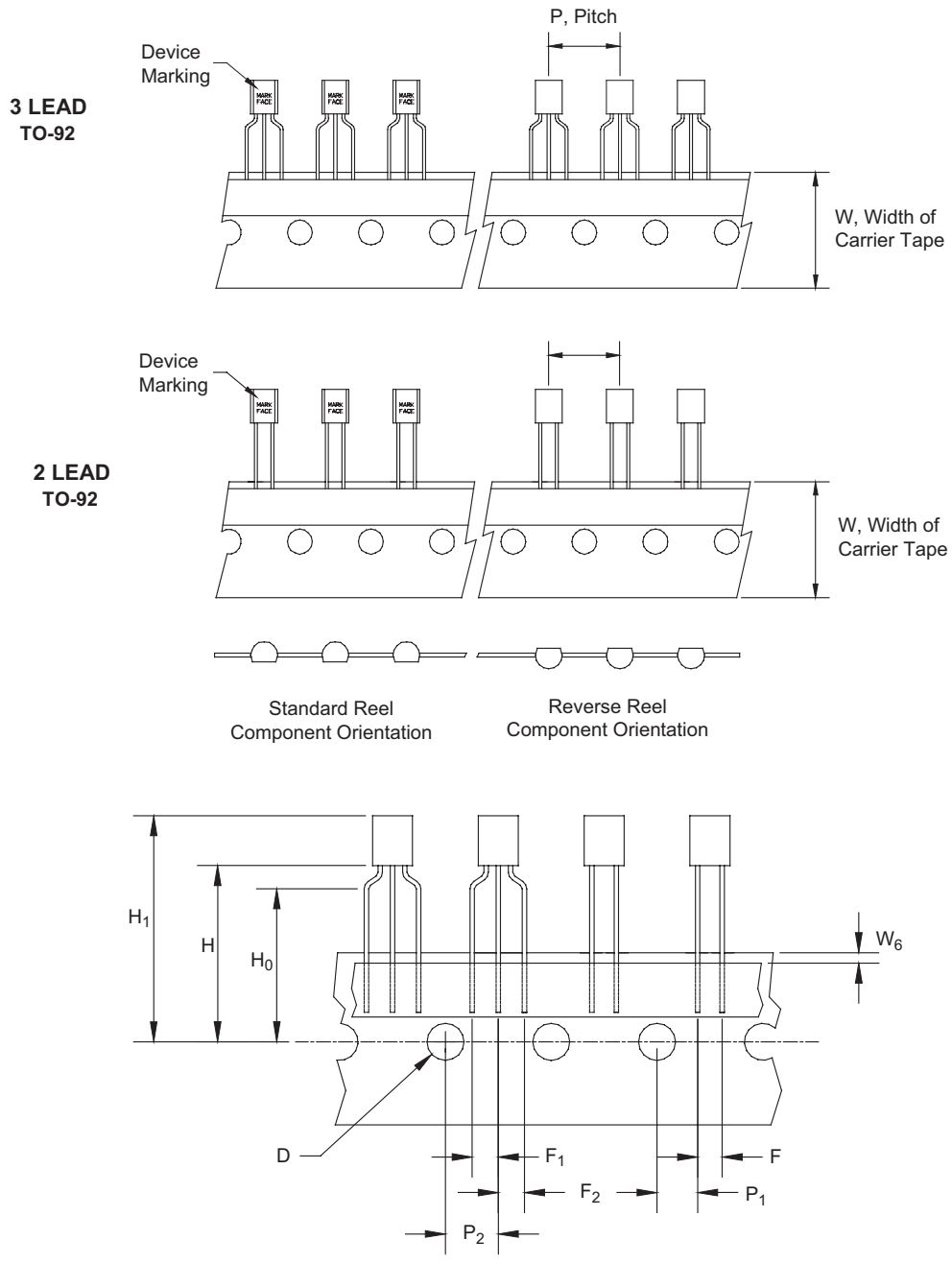


FIGURE 12: DFN/QFN DEVICES



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FIGURE 13: TO-92 DEVICES



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PACKAGING

DIMENSIONS AND TOLERANCES

All component taping diagrams, dimensions, tolerances, and component positioning requirements are those which are specified per EIA Standard EIA-481, current revision.

For the 8-lead SOIC EIAJ Type II Package and 16 mm Carrier Tape width, the component taping diagrams, dimensions, and tolerances, and component positioning requirements are those which are specified per EIAJ Standard RC-1009B, current revision.

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AN233

Solder Reflow Recommendation

Author: *Ravi Sharma*
Microchip Technology Inc.

INTRODUCTION

The electronic manufacturing industry is moving towards lead-free, environmentally safe assembly processes. Factors that should be considered when switching to lead-free soldering materials include:

- circuit board thickness
- fabrication complexity
- surface finish
- assembly process compatibility

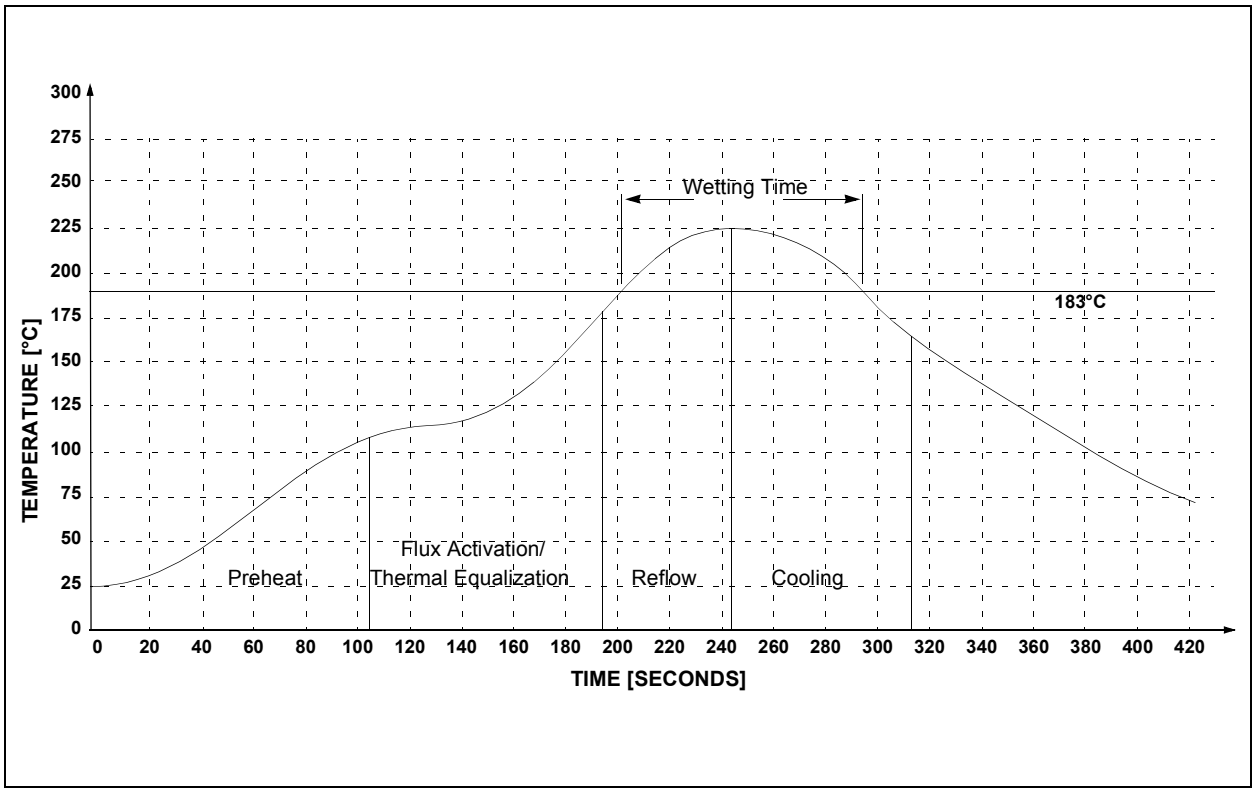
This Application Note focuses on solder reflow recommendation for packages with Matte Tin and Tin/ Lead finishes.

BASICS OF THE REFLOW PROCESS

Lead-free soldering techniques have been available for some years. However, they do not always meet the same physical criteria for attachments as alloys containing lead. In the past, the most common alloy for joining electronic components was the mixture of 63% tin and 37% lead. This composition of tin and lead provided excellent bonding strength as well as enough elasticity to withstand the thermal stresses in the product's operating environment. As electronic manufacturers move away from this longtime standard PbSn alloy toward Pb-free solder alloys such as tin-silver-copper (Sn-Ag-Cu), melting and eutectic temperatures also change, requiring modification to the solder reflow profile.

As a starting point for a review of the basics of the reflow process, a typical thermal reflow profile is shown in Figure 1. The process typically undergoes five distinct transitions, as seen in the diagram.

FIGURE 1: Sn/Pb TYPICAL REFLOW PROFILE



5 Packaging

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The five transition periods for the typical reflow process are:

1. **Preheat** – Brings the assembly from 25°C to 80-150°C and evaporates solvents from the solder paste.
2. **Flux Activation** – Dried solder paste is heated to a temperature in which the flux will react with the oxide and contaminants on the surfaces to be joined.
3. **Thermal Equalization** – Achieves temperature equalization approximately 25-50°C below the reflow temperature. Actual time and temperature will depend on the mass and materials used.
4. **Reflow** – In this stage, the assembly is brought to the temperature sufficient to produce reflow of the solder. Note the “wetting time” is shown as the time the solder is in a liquid state around 183°C on the curve.
5. **Cool Down** – This is the final stage in the process where gradual cooling should be used. Slower cool down produces a finer grain structure in the solder joint, which will yield a more fatigue-resistant solder joint.

FIGURE 2: JEDEC REFLOW PROFILES FOR Sn-Pb AND Pb-FREE ASSEMBLIES

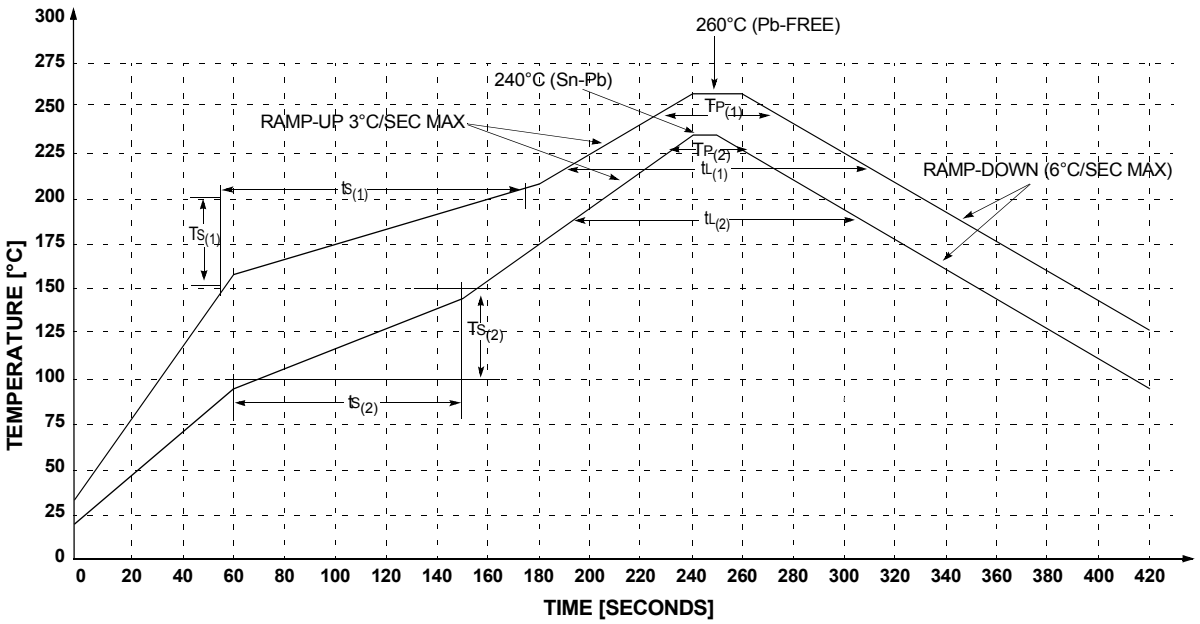


TABLE 1: TIME AND TEMPERATURE PARAMETRICS

Sym.	Min.	Max.	Units	Test Conditions
$Ts_{(1)}$	150	200	°C	Pb-Free
$Ts_{(2)}$	100	150	°C	Sn-Pb
$ts_{(1)}$	60	180	Sec	Pb-Free
$ts_{(2)}$	60	120	Sec	Sn-Pb
$tl_{(1)}$	60	150	Sec	Pb-Free
$tl_{(2)}$	60	150	Sec	Sn-Pb
$Tp_{(1)}$	245	260	°C	Pb-Free
$Tp_{(2)}$	225	240	°C	Sn-Pb

For reference, reflow conditions from IPC/JEDEC J-STD-020C are reproduced in Figure 2 and Table 1.

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Solder Reflow Recommendations

Figure 3 shows Microchip's recommended profiles for Pb-free devices. These devices are plated with matte Tin (Pure Sn) and contain no lead. They can be used in standard tin-lead (SnPb) applications, using a profile that is equal to or above the lower line in the plot, or in Pb-free solder such as Tin-Silver-Copper (Sn-Ag-Cu) with profiles up to and including the upper line on the plot.

Figure 4 shows Microchips's recommended profiles for standard devices with 63%/37% tin-lead (Sn-Pb) solder finish. The reflow profile for these devices can be anywhere between the upper and lower curves shown in Figure 4. Please note that the peak temperature is lower than that of the Pb-free devices.

FIGURE 3: REFLOW PROFILE RECOMMENDATION (Pb-FREE)

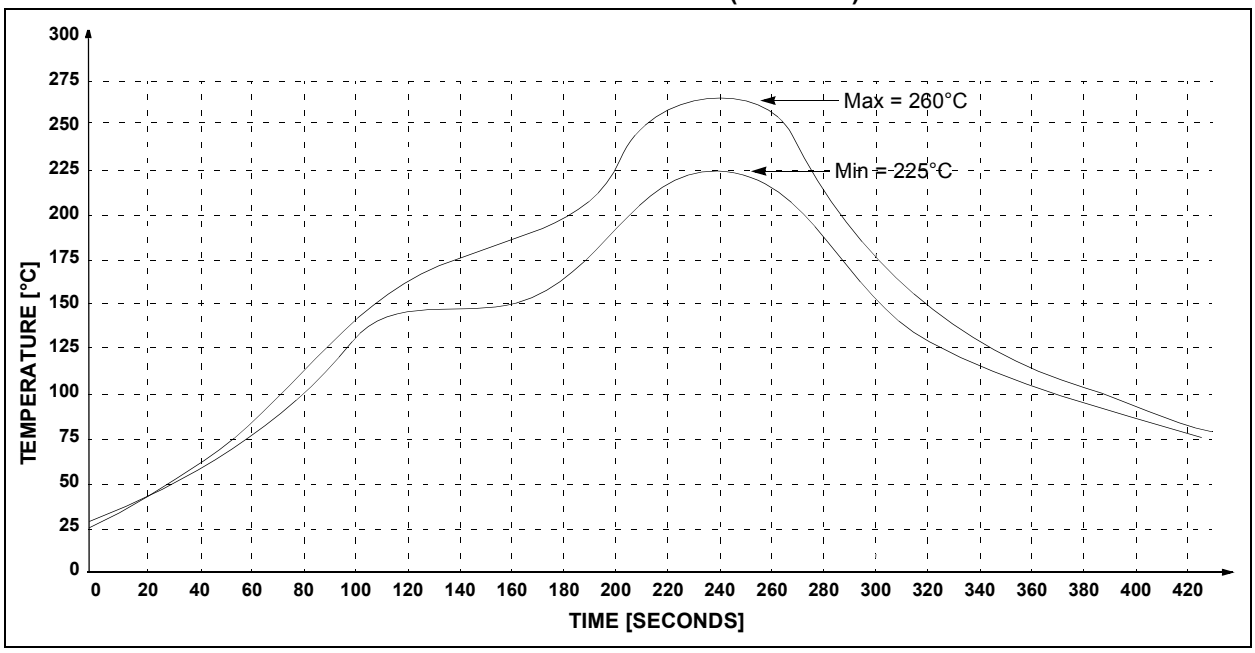
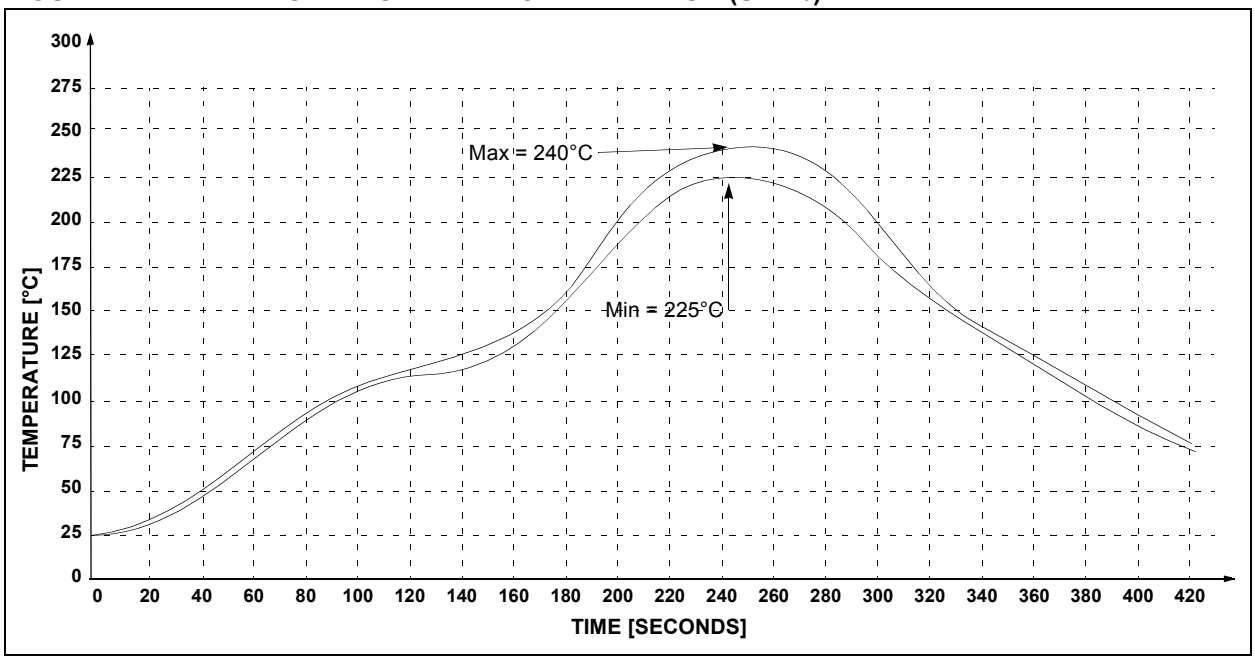


FIGURE 4: REFLOW PROFILE RECOMMENDATION (Sn/Pb)



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CONCLUSIONS

Many new lead-free alloy compositions are being released. When testing the alternative solder compositions the user must consider several issues:

- Is the material selected going to be compatible with the plating on the component leads or the finish specified on the circuit board?
- Will the material chosen compromise product performance, reliability or manufacturability?
- What is the residual effect of the higher temperature required for soldering lead-free alloys on the semiconductor packages, the passive components, and the board itself?

This Application Note addresses the use of Matte Tin and Tin/Lead finishes, and recommends staying within the limits shown in Figure 3 and Figure 4. However, factors such as circuit board thickness, size, package type, and reflow equipment may affect the total profile time.

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Overview of Microchip Die/Wafer Support

INTRODUCTION

In addition to packaged devices, Microchip Technology Inc. devices are available in wafer and die form. All products sold in die or wafers have been characterized and qualified according to the requirements of Microchip Technology Inc. Specifications SPI-41014, “Characterization and Qualification of Integrated Circuits” and QCI-39000, “Worldwide Quality Conformance Requirements”.

PRODUCT INTEGRITY

Product supplied in die or wafer form is fully tested and characterized. Die and wafers are inspected to Microchip Technology Inc. Specification, QCI-30014.

CAUTION

Some EEPROM devices use EPROM cells for device configuration. Exposure to ultraviolet light must be avoided. Exposure to ultraviolet light may cause the device to operate improperly.

Extreme care is urged in the handling and assembly of these products since they are susceptible to damage from electro-static discharge.

PACKAGING OPTIONS

Die/wafer products are available as individual Die in Waffle Pack, Whole Wafers or as Sawn Wafer on Frame. As a standard, all die on a wafer are tested and Ink Dots are used to indicate the bad die on a wafer. Inkless wafers with electronic wafer maps are also available upon request. To acquire individual electronic wafer maps, customers can request a password-protected account on a Microchip FTP site where their wafer maps are stored and easily downloaded.

Various wafer thicknesses are available, which include 8, 11, 15 and 29 mils for unground wafers. Standard wafer thickness varies from product to product, so contact your Microchip Sales Office for details.

ORDERING INFORMATION

Die sales must be initiated by contacting your Microchip Sales Office. To order or to obtain information (on pricing or delivery) for a specific device, use one of the following part numbers.

Standard Thickness Die/Wafer		**EEPROM Examples**
DEVICE_NUMBER/S	Die in Waffle Pack	24LC01B-I/S
DEVICE_NUMBER/W	Whole Wafers	24LC01B-I/W
DEVICE_NUMBER/WF	Sawn Wafer on Frame	24LC01B-I/WF
No Backgrind Wafers		
DEVICE_NUMBER/WNBG	Whole Wafers with Ink	24LC01B-I/WNBG
DEVICE_NUMBER/WNBI	Whole Wafers without Ink	24LC01B-I/WNBI
Standard Die/Wafers with Manufacturing Process Included in Part Number		
DEVICE_NUMBER/SXXX	Die in Waffle Pack	24LC01B-I/S15K
DEVICE_NUMBER/WXXX	Whole Wafers	24LC01B-I/W15K
DEVICE_NUMBER/WFXXX	Sawn Wafer on Frame	24LC01B-I/WF15K

DEVICE_NUMBER is the base part number of the device that you require, the S specifies Die in Waffle Pack, a W specifies a Whole Wafer and WF specifies Sawn Wafer on Frame. Whole wafers specified as NBG are shipped as inked wafers with no backgrind (29 mils) and those specified as NBI are shipped with no backgrind and without Ink.

As further clarification, the manufacturing process is sometimes indicated with a three digit suffix added at the end of the part number. For example, a wafer from the 160K process will use the suffix 16K, one from the 150K process will use 15K and one from the 121K process will use 12K.

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ELECTRICAL SPECIFICATIONS

The functional and electrical specifications of Microchip devices in die form are identical to those of a packaged version. Please refer to individual data sheets for complete details.

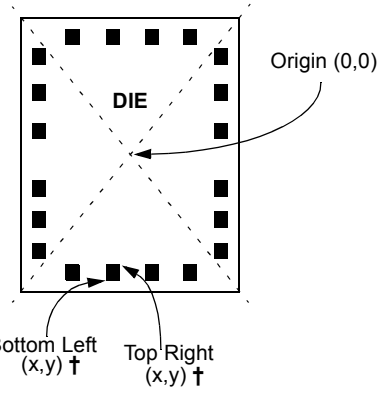
DIE MECHANICAL SPECIFICATIONS

Refer to the individual data sheet for these specifications.

BOND PAD COORDINATES

The die figures have associated bond pad coordinates. These coordinates assist in the attaching of the bond wire to the die. All the dimensions of these coordinates are in micrometers (μm) unless otherwise specified. The origin for the coordinates is the center of the die, as shown in Figure 1. Refer to the specific die data sheet for each device for openings and pitch.

FIGURE 1: DIE COORDINATE ORIGIN



† All dimensions in μm unless specified otherwise.

The die is capable of thermosonic gold or ultrasonic wire bonding. Die meet the minimum conditions of MIL-STD 883, Method 2011 on “Bond Strength (Destructive Bond Pull Test)”. The Bond Pad metallization is silicon doped aluminum.

SUBSTRATE BONDING

Substrate bonding may be required on certain product families. For more information, refer to the specific die data sheet for that product.

SHIPPING OPTIONS

Die Form (/S)

Microchip product in die form can be shipped in waffle pack. The waffle pack has sufficient cavity area to restrain the die, while maintaining their orientation. Lint free paper inserts are placed over the waffle packs, and each pack is secured with a plastic locking clip. Groups of waffle packs are assembled into sets for shipment. A label with lot number, quantity and part number is attached.

These waffle packs are hermetically sealed in bags.

Wafer Form (/W)

Products may also be shipped in wafer form (see ordering information). Wafers are uncut and shipped in a wafer tub. The tub is padded with non-conductive foam. Lint free paper inserts are placed around each wafer. A label with lot number, quantity and part number is attached.

Sawn Wafer on Frames (/WF)

Products may also be shipped on wafer frames. Wafers are mounted on plastic frames and 100% sawn through. Sawn wafer on frames may be shipped in bulk (25 wafers per carrier) or as a single wafer in a carrier. A label with lot number, quantity and part number is attached with each shipment.

Storage Procedures

Temperature and humidity greatly affect the storage life of die. It is recommended that the die be used as soon as possible after receipt.

Upon receipt, the sealed bags should be stored in a cool and dry environment (25°C and 25% relative humidity). In these conditions, sealed bags have a shelf life of 12 months. Temperatures or humidities greater than these will reduce the storage life.

Once a bag containing waffle packs has been opened, the devices should be assembled and encapsulated within 48 hours (assuming 25°C and 25% humidity).

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SECTION 6 DEVELOPMENT TOOLS

Total Endurance™ Software Model 6-1
SEEVAL® 32 Serial EEPROM Designer's Kit 6-2

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Total Endurance™ Software Model



Microchip's revolutionary Total Endurance Software Model provides electronic system designers with unprecedented visibility into Serial EEPROM-based applications. This advanced software model (with a very friendly user interface) eliminates time and guess-work from Serial EEPROM-based designs by accurately predicting the device's performance and reliability within a user-defined application environment. Design trade-off analysis which formerly consumed days or weeks can now be performed in minutes – with a level of accuracy that delivers a truly robust design.

With Microchip's Total Endurance Software Model, users may input the following application parameters:

- Serial EEPROM device type
- Bytes to be written per cycle
- Cycling mode – byte or page
- Data pattern type – random or worst-cast
- Temperature in °C
- Erase/Write cycles per day
- Application lifetime or target PPM level

The model will respond with FIT rate, PPM level, application life and plot of the PPM level versus number of cycles. The model is compatible with Windows® XP, Windows ME, Windows 2000, Windows NT® and Windows 98.

FEATURES

- Automatic or manual recalculation
- Real-time update of data
- Full-screen or windowed graphical view
- Hypertext on-screen help
- Key or slide-bar entry of parameters
- On-screen editing of parameters
- Single-click copy of plot to clipboard
- Numeric export to delimited text file
- Copy into Excel spreadsheet
- Built-in update feature
- On-disk Endurance Tutorial

Ordering Part Number:

Available on the Microchip web site at:

www.microchip.com (Free download).

SEEVAL® 32 Serial EEPROM Designer's Kit



Microchip's SEEVAL 32 Serial EEPROM Evaluation and Programming System supports all Microchip Serial EEPROMs including future devices. Through the use of a ZIF socket, standard DIP packages are directly supported; other packages such as 8-lead SOIC, TSSOP, MSOP, DFN and 5-lead SOT-23 can also be supported by using separate third-party adapters. The SEEVAL 32 system gives the designer or system integrator the ability to read, write or erase any byte, page or the entire array, and to display, save or load this data as a file. Supports all the current Windows® operating systems, including: Windows XP, Windows ME, Windows 2000, Windows NT® 4.0 and also Windows 95/98.

The SEEVAL 32 system provides advanced features to aid in system integration and debug. Through the use of test pins on each system an oscilloscope or other test equipment can be easily connected to evaluate timing and voltage levels. Through the SEEVAL host software, serial EEPROMs can be tested by reading and writing data in the EEPROM under test. Erase/Write Endurance can also be tested by selecting a continuous loop mode to repeatedly read/write/erase the EEPROM.

SEEVAL 32 kits also include the Total Endurance Software Model, a powerful tool which can predict the erase/write endurance of any given serial EEPROM based upon its application parameters: temperature, voltage, cycles per day and bytes per cycle.

SEEVAL 32 Serial EEPROM Designer's Kit Contents
• Total Endurance Software Model • SEEVAL 32 Evaluation and Programming System • Serial EEPROM Sample Pack • SEEVAL 32 Software • RS-232 Interface Cable • Power Supply

Ordering Part Number:

DV243002 SEEVAL 32 Serial EEPROM Development Kit

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