CS43122

122 dB, 24-Bit, 192 kHz DAC for Digital Audio

Features

- 24 Bit Conversion
- Up to 192 kHz Sample Rates
- 122 dB Dynamic Range
- -102 dB THD+N
- Second-Order Dynamic-Element Matching
- Low Clock Jitter Sensitivity
- 102 dB Stop-band attenuation
- Single +5 V supply
- Soft Mute Control
- Digital De-Emphasis for 32, 44.1, and 48 kHz
- External Reference Input
- Pin-compatible with the CS4396

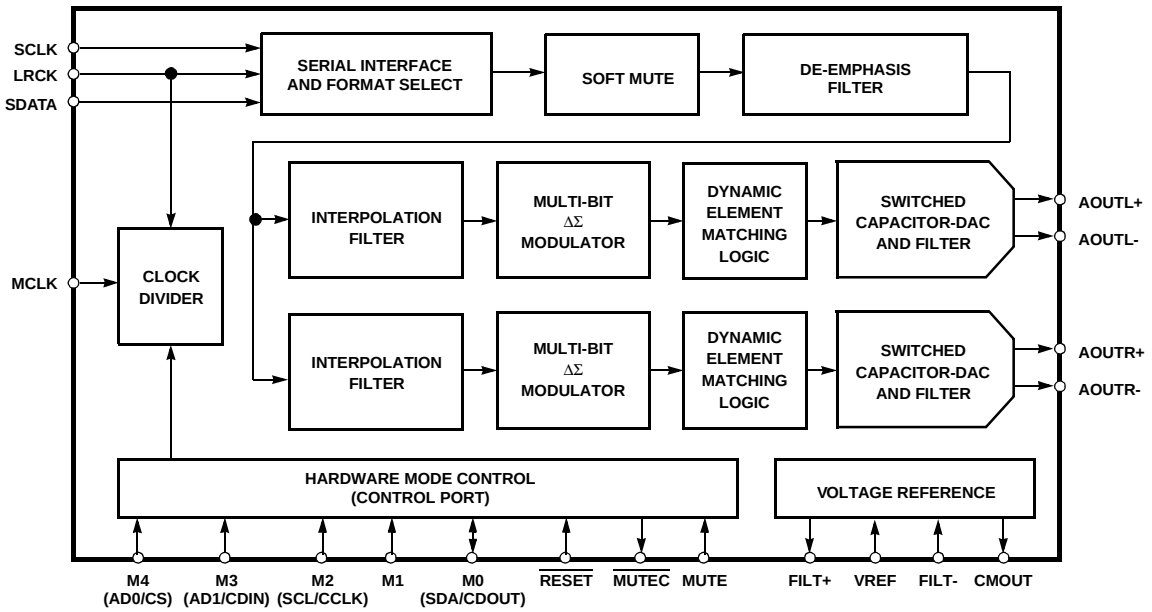
Description

The CS43122 is a complete high performance 24 bit-192 kHz stereo digital-to-analog conversion system. The device includes a digital interpolation filter followed by an oversampled 5 bit delta-sigma modulator which drives second generation dynamic-element-matching (DEM) selection logic. The output from the DEM block controls the input to a multi-element switched capacitor DAC/low-pass filter, with fully-differential outputs. This multi-bit architecture features significantly lower out-of-band noise and jitter sensitivity than traditional 1-bit designs, and the advanced second generation DEM guarantees low noise and distortion at all signal levels.

The CS43122 is the optimal D/A converter solution for any application that requires the highest performance and best possible sound quality including high-end consumer and professional audio products such as Universal DVD players, A/V receivers, Outboard D/A Converters, CD Players, and Mixing Consoles.

ORDERING INFORMATION

CS43122-KS	-10° to 70° C	28-pin SOIC
CDB43122		Evaluation Board



Advance Product Information

This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

CIRRUS LOGIC
P.O. Box 17847, Austin, Texas 78760
(512) 445 7222 FAX: (512) 445 7581
http://www.cirrus.com

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1. CHARACTERISTICS/SPECIFICATIONS

ANALOG CHARACTERISTICS (T_A = 25° C; Logic "1" = VD = 3 V; VA = 5.5 V;VREF=5.5 V Logic "0" = DGND;Full-Scale Output Sine Wave, 997 Hz; MCLK = 12.288 MHz; SCLK = 3.072 MHz; Measurement Bandwidth 10 Hz to 20 kHz, unless otherwise specified. Test load = R_L = 1kΩ, C_L = 10 pF)

Parameter			Symbol	Min	Typ	Max	Unit
Dynamic Performance - Operational Mode 1 (Fs = 48 kHz)							
Dynamic Range		(Note 1)					
	24-Bit	unweighted		TBD	119	-	dB
		A-Weighted		TBD	122	-	dB
	16-Bit	unweighted		-	95	-	dB
	(Note 2)	A-Weighted		-	98	-	dB
Total Harmonic Distortion + Noise		(Note 1)	THD+N				
	24-Bit	0 dB		-	-102	TBD	dB
		-20 dB		-	-99	TBD	dB
		-60 dB		-	-59	TBD	dB
	16-Bit	0 dB		-	-95	-	dB
	(Note 2)	-20 dB		-	-75	-	dB
		-60 dB		-	-35	-	dB

ANALOG CHARACTERISTICS (CONTINUED)

Parameter			Symbol	Min	Typ	Max	Unit
Dynamic Performance - Operational Mode 0 (Fs = 48 kHz)							
Dynamic Range		(Note 1)					
	24-Bit	unweighted		TBD	117	-	dB
		A-Weighted		TBD	120	-	dB
	16-Bit	unweighted		-	95	-	dB
	(Note 2)	A-Weighted		-	98	-	dB
Total Harmonic Distortion + Noise		(Note 1)	THD+N				
	24-Bit	0 dB		-	-100	TBD	dB
		-20 dB		-	-97	TBD	dB
		-60 dB		-	-55	TBD	dB
	16-Bit	0 dB		-	-95	-	dB
	(Note 2)	-20 dB		-	-75	-	dB
		-60 dB		-	-35	-	dB
Dynamic Performance - Operational Mode 1 (Fs = 96 kHz)							
Dynamic Range		(Note 1)					
	24-Bit	unweighted		TBD	117	-	dB
		A-Weighted		TBD	120	-	dB
	40 kHz bandwidth			TBD	114	-	dB
		unweighted		-	92	-	dB
	16-Bit	unweighted		-	98	-	dB
	(Note 2)	A-Weighted					
Total Harmonic Distortion + Noise		(Note 1)	THD+N				
	24-Bit	0 dB		-	-100	TBD	dB
		-20 dB		-	-97	TBD	dB
		-60 dB		-	-55	TBD	dB
	16-Bit	0 dB		-	-95	-	dB
	(Note 2)	-20 dB		-	-75	-	dB
		-60 dB		-	-35	-	dB
Dynamic Performance - Operational Mode 2 (Fs = 192 kHz)							
Dynamic Range		(Note 1)					
	24-Bit	unweighted		TBD	117	-	dB
		A-Weighted		TBD	120	-	dB
	40 kHz bandwidth			TBD	114	-	dB
		unweighted		-	95	-	dB
	16-Bit	unweighted		-	98	-	dB
	(Note 2)	A-Weighted					
Total Harmonic Distortion + Noise		(Note 1)	THD+N				
	24-Bit	0 dB		-	-100	TBD	dB
		-20 dB		-	-97	TBD	dB
		-60 dB		-	-55	TBD	dB
	16-Bit	0 dB		-	-95	-	dB
	(Note 2)	-20 dB		-	-75	-	dB
		-60 dB		-	-35	-	dB

ANALOG CHARACTERISTICS (CONTINUED)

Parameter		Symbol	VD = 3 V			VD = 5 V			Unit
Power Supplies			**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	
Supply Current	normal operation	I_A	-	17	TBD	-	17	TBD	mA
VA = 5 .0V	normal operation	I_D	-	27		-	24		mA
	power-down state	$I_D + I_A$	-	60		-	30	-	µA
Power Dissipation	normal operation		-	166	TBD	-	205	TBD	mW
VA = 5 .0V	power-down		-	0.3	-	-	0.3	-	mW
Power Supply Rejection Ratio (1 kHz)	(Note 3)	PSRR	-	60	-	-	60	-	dB
	(120 Hz)		-	40	-	-	40	-	dB

Parameter		Symbol	Min	Typ	Max	Unit
Analog Output						
Full Scale Differential Output Voltage			TBD	1.33VREF	TBD	Vpp
Common Mode Voltage			-	0.5VREF	-	VDC
Interchannel Gain Mismatch			-	0.1	-	dB
Gain Drift			-	100	-	ppm/°C
Differential DC Offset			-	2.0	TBD	mV
AC-Load Resistance		R_L	1.0	-	-	kΩ
Load Capacitance		C_L	-	-	100	pF
Interchannel Isolation	(1 kHz)		-	90	-	dB

Notes: 1. Triangular PDF dithered data.

2. Performance limited by 16-bit quantization noise.

3. Valid with the recommended capacitor values on FILT+ and CMOUT as shown in Figure 1. Increasing the capacitance will also increase the PSRR.

ANALOG CHARACTERISTICS (Continued)

Parameter	Symbol	Min	Typ	Max	Unit
Combined Digital and On-chip Analog Filter Response - Operational Mode 0					
Passband (Note 4)					
to -0.1 dB corner		-	-	0.470	Fs
to -3 dB corner		-	-	0.492	Fs
Frequency Response 10 Hz to 20 kHz		-.020	-	+0.015	dB
Passband Ripple		-	-	±0.0001	dB
StopBand		.5465	-	-	Fs
StopBand Attenuation (Note 5)		102	-	-	dB
Group Delay (Note 6)	tgd	-	37/Fs	-	s
De-emphasis Error (Note 7)					
Fs = 32 kHz		-	-	±0.10	dB
(Relative to 1 kHz) Fs = 44.1 kHz		-	-	±0.10	dB
Fs = 48 kHz		-	-	±0.13	dB
Combined Digital and On-chip Analog Filter Response - Operational Mode 1					
Passband (Note 4)					
to -0.1 dB corner		0	-	0.448	Fs
to -3 dB corner		0	-	0.486	Fs
Frequency Response 10 Hz to 20 kHz		-0.017	-	0.035	dB
Passband Ripple		-	-	±0.0008	dB
StopBand		.570	-	-	Fs
StopBand Attenuation (Note 5)		82	-	-	dB
Group Delay	tgd	-	20/Fs	-	s
Combined Digital and On-chip Analog Filter Response - Operational Mode 2					
Passband (Note 4)					
to -0.1 dB corner		-	-	0.385	Fs
to -3 dB corner		-	-	0.472	Fs
Frequency Response 10 Hz to 20 kHz		0	-	+0.015	dB
Passband Ripple		-	-	±0.00065	dB
StopBand		0.635	-	-	Fs
StopBand Attenuation (Note 5)		83	-	-	dB
Group Delay	tgd	-	11/Fs	-	s

Notes:
4. Response is clock dependent and will scale with Fs. Note that the response plots (Figures 7-18) have been normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs.
5. For Operational Mode 0, the Measurement Bandwidth is 0.5465 Fs to 1.4 Fs.
   For Operational Mode 1, the Measurement Bandwidth is 0.570 Fs to 1.4 Fs.
   For Operational Mode 2, the Measurement Bandwidth is 0.635 Fs to 1.3 Fs.
6. Group Delay for Fs=48 kHz 37/48 kHz=770 µs
7. De-emphasis is available only in Operational Mode 0.

DIGITAL CHARACTERISTICS (T_A = 25° C; VD = 3.0 V - 5.25 V)

Parameters		Symbol	Min	Typ	Max	Units
High-Level Input Voltage	VD = 5 V	V_{IH}	2.0	-	-	V
	VD = 3 V		2.0	-	-	V
Low-Level Input Voltage	VD = 5 V	V_{IL}	-	-	0.8	V
	VD = 3 V		-	-	0.8	V
Input Leakage Current		I_{in}	-	-	±10	µA
Input Capacitance			-	8	-	pF
Maximum MUTEC Drive Current			-	3	-	mA

ABSOLUTE MAXIMUM RATINGS (AGND = 0 V, all voltages with respect to ground.)

Parameter		Symbol	Min	Max	Unit
DC Power Supply:	Positive Analog	VA	-0.3	6.0	V
	Positive Digital	VD	-0.3	6.0	V
	Reference Voltage	VREF	-0.3	VA	V
Input Current, Any Pin Except Supplies		I_{in}	-	±10	mA
Digital Input Voltage		V_{IND}	-0.3	(VD)+0.4	V
Ambient Operating Temperature (power applied)		T_A	-55	125	°C
Storage Temperature		T_{stg}	-65	150	°C

WARNING: WARNING:Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS (DGND = 0V; all voltages with respect to ground)

Parameter		Symbol	Min	Typ	Max	Unit
DC Power Supply:	Positive Digital	VD	3.0	3.3	5.25	V
	Positive Analog	VA	5.25	5.5	5.75	V
	Reference Voltage	VREF	5.25	5.5	VA	V
Specified Temperature Range		T_A	-10	-	70	°C

SWITCHING CHARACTERISTICS (T_A= -10 to 70° C; Logic 0 = AGND = DGND; Logic 1 = VD = 5.25 to 3.0 Volts; C_L = 20 pF)

Parameter		Symbol	Min	Typ	Max	Unit
Input Sample Rate	(Operational Mode 0)	Fs	16	-	55	kHz
	(Operational Mode 1)	Fs	45	-	105	kHz
	(Operational Mode 2)	Fs	95	-	200	kHz
LRCK Duty Cycle			45	50	55	%
MCLK Frequency	(Operational Mode 0, 256 Fs) (Operational Mode 1, 128 Fs) (Operational Mode 2, 64 Fs)		4.096	-	14.08	MHz
MCLK Frequency	(Operational Mode 0, 384 Fs) (Operational Mode 1, 192 Fs) (Operational Mode 2, 96 Fs)		6.144	-	21.12	MHz
MCLK Frequency	(Operational Mode 0, 512 Fs) (Operational Mode 1, 256 Fs) (Operational Mode 2 , 128 Fs)		8.192	-	28.16	MHz
MCLK Frequency	(Operational Mode 0, 768 Fs) (Operational Mode 1, 384 Fs) (Operational Mode 2 , 192 Fs)		12.288	-	42.24	MHz
MCLK Duty Cycle			40	50	60	%
SCLK Frequency	(Operational		-	-	256×Fs	Hz
Mode 0)	(Operational Mode 1)		-	-	128×Fs	Hz
	(Operational Mode 2)		-	-	64×Fs	Hz
SCLK rising to LRCK edge delay		t_{slrd}	20	-	-	ns
SCLK rising to LRCK edge setup time		t_{slrs}	20	-	-	ns
SDATA valid to SCLK rising setup time		t_{sdlrs}	20	-	-	ns
SCLK rising to SDATA hold time		t_{sdh}	20	-	-	ns

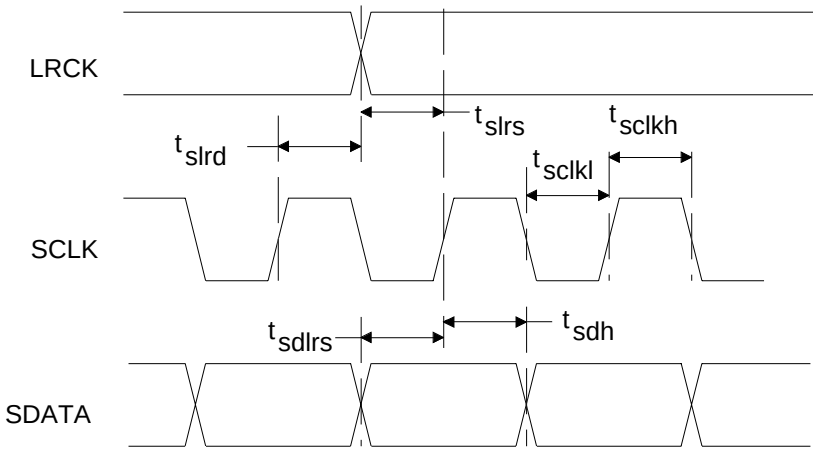


Figure 1. Serial Audio Input Timing

SWITCHING CHARACTERISTICS - CONTROL PORT

(T_A = 25° C; VD = 5.25 V to 3.0 Volts; Inputs: logic 0 = AGND, logic 1 = VD, C_L = 30 pF)

Parameter	Symbol	Min	Max	Unit
2 Wire Mode				
SCL Clock Frequency	f_{scl}	-	100	KHz
RST Rising Edge to Start	t_{irs}	500	-	ns
Bus Free Time Between Transmissions	t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	µs
Clock Low time	t_{low}	4.7	-	µs
Clock High Time	t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	µs
SDA Hold Time from SCL Falling (Note 8)	t_{hdd}	0	-	µs
SDA Setup time to SCL Rising	t_{sud}	250	-	ns
Rise Time of Both SDA and SCL Lines	t_r	-	1	µs
Fall Time of Both SDA and SCL Lines	t_f	-	300	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	µs

Notes: 8. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

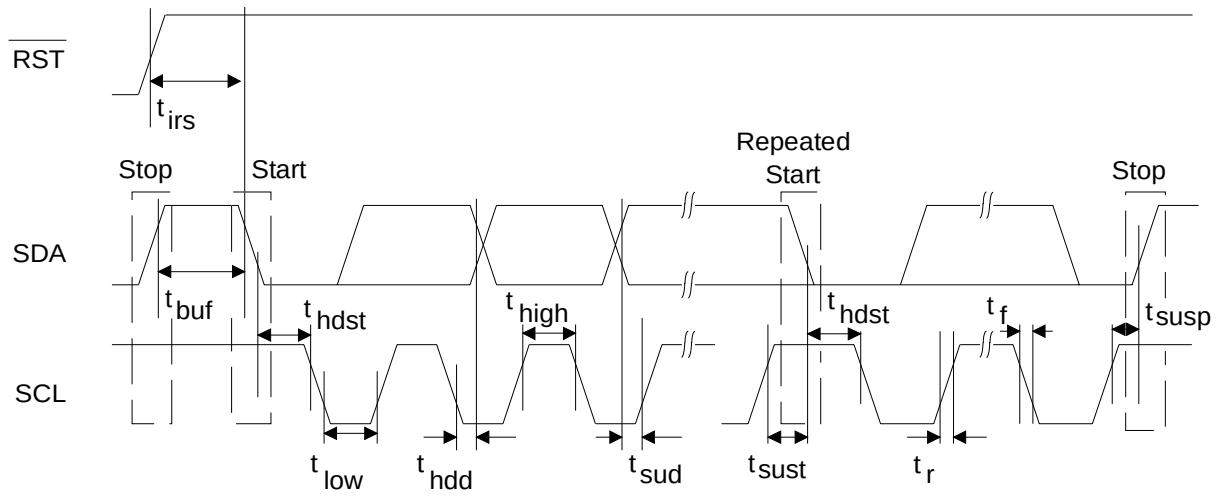


Figure 2. 2 Wire Mode Control Port Timing

SWITCHING CHARACTERISTICS - CONTROL PORT

(T_A = 25° C; VD = 5.25 V to 3.0 Volts; Inputs: logic 0 = AGND, logic 1 = VD, C_L = 30 pF)

Parameter		Symbol	Min	Max	Unit
SPI Mode					
CCLK Clock Frequency		f_{sclk}	-	6	MHz
RST Rising Edge to CS Falling		t_{srs}	500	-	ns
CCLK Edge to CS Falling	(Note 9)	t_{spi}	500	-	ns
$\overline{CS}$ High Time Between Transmissions		t_{csh}	1.0	-	µs
CS Falling to CCLK Edge		t_{css}	20	-	ns
CCLK Low Time		t_{scl}	66	-	ns
CCLK High Time		t_{sch}	66	-	ns
CDIN to CCLK Rising Setup Time		t_{dsu}	40	-	ns
CCLK Rising to DATA Hold Time	(Note 10)	t_{dh}	15	-	ns
Rise Time of CCLK and CDIN	(Note 11)	t_{r2}	-	100	ns
Fall Time of CCLK and CDIN	(Note 11)	t_{f2}	-	100	ns
CCLK Falling to CDOUT valid		t_{ov}	45		ns

Notes: 9. t_{spi} only needed before first falling edge of $\overline{CS}$ after $\overline{RST}$ rising edge. t_{spi} = 0 at all other times.

10. Data must be held for sufficient time to bridge the transition time of CCLK.

11. For F_{SCK} < 1 MHz

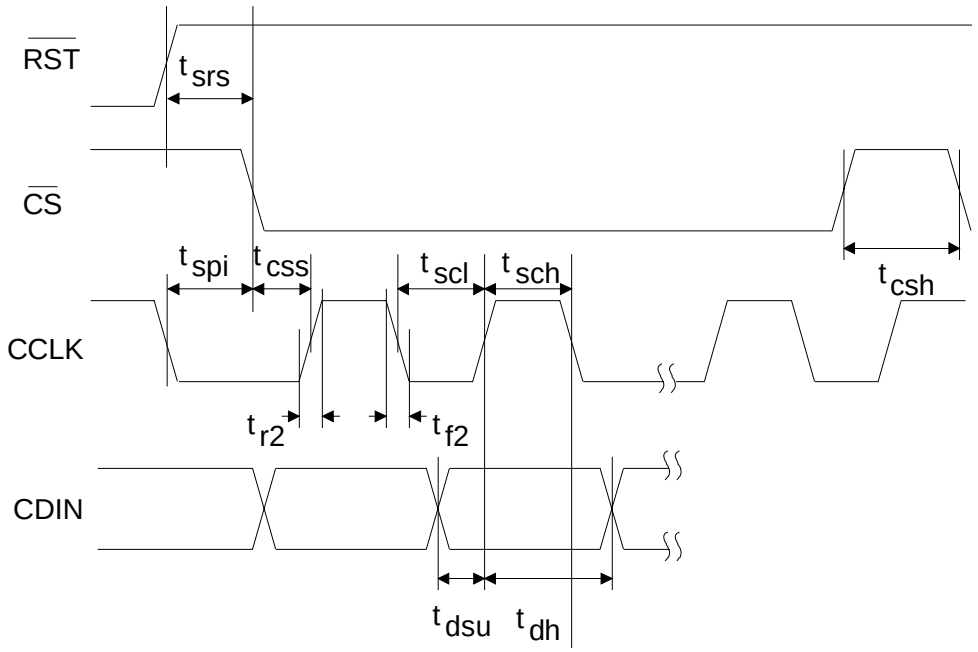


Figure 3. SPI Control Port Timing

2. TYPICAL CONNECTION DIAGRAM

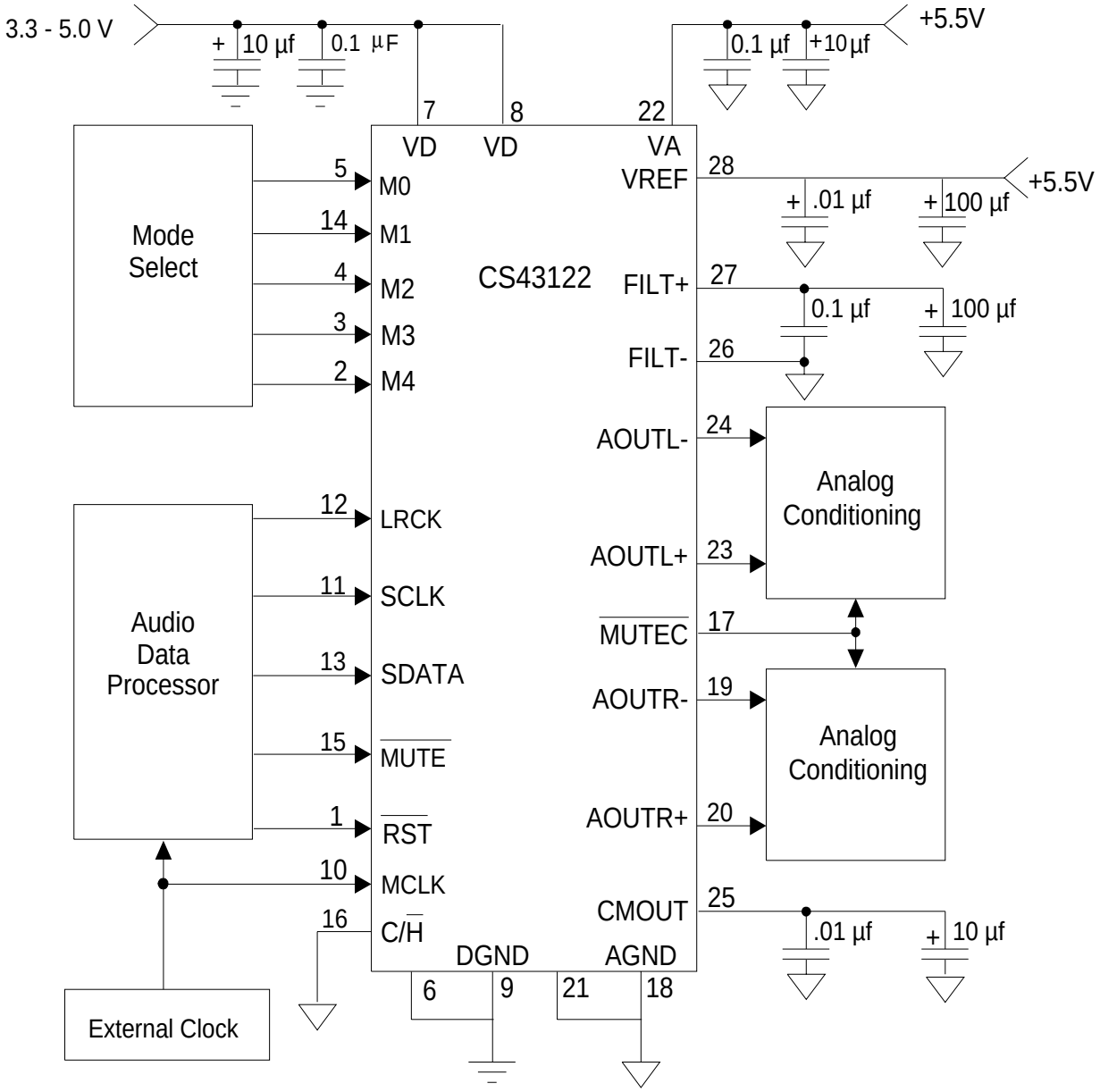


Figure 4. Typical Connection Diagram

3. REGISTER DESCRIPTION

3.1 MODE CONTROL REGISTER (ADDRESS 01H)

7	6	5	4	3	2	1	0
CAL	$\overline{\text{MUTE}}$	M4	M3	M2	M1	M0	PDN
0	0	0	0	0	0	0	0

4.11 Differential DC offset calibration (CAL)

Default = 0

0 - Disabled

1 - Enabled

Function:

Enabling this function will initiate a calibration to minimize the differential DC offset. This function will be automatically reset following completion of the calibration sequence.

4.12 Soft Mute (MUTE)

Default = 0

0 - Disabled

1 - Enabled

Function:

The analog outputs will ramp to a muted state when enabled. The ramp requires 1152 left/right clock cycles in Operational Mode 0, 2304 cycles in Operational Mode 1 and 4608 cycles in Operational Mode 2 . The bias voltage on the outputs will be retained and $\overline{\text{MUTEC}}$ will go low at the completion of the ramp period.

The analog outputs will ramp to a normal state when this function transitions from the enabled to disabled state. The ramp requires 1152 left/right clock cycles in Operational Mode 0, 2304 cycles in Operational Mode 1 and 4608 cycles in Operational Mode 2 . The $\overline{\text{MUTEC}}$ will go high immediately on disabling of $\overline{\text{MUTE}}$.

4.13 Mode Select (M4-M0)

Default = 00000

Function:

The Mode Select pins determine the operational mode of the device as detailed in Tables 4-7. The options include:

Selection of the Digital Interface Format which determines the required relationship between the Left/Right clock, serial clock and serial data as detailed in Figures 20-23

Selection of the standard 15 µs/50 µs digital de-emphasis filter response, Figure 28, which requires reconfiguration of the digital filter to maintain the proper filter response for 32, 44.1 or 48 kHz sample rates.

Selection of the appropriate operational clocking mode to match the input sample rates.

4.14 Power Down (PDN)

Default = 1

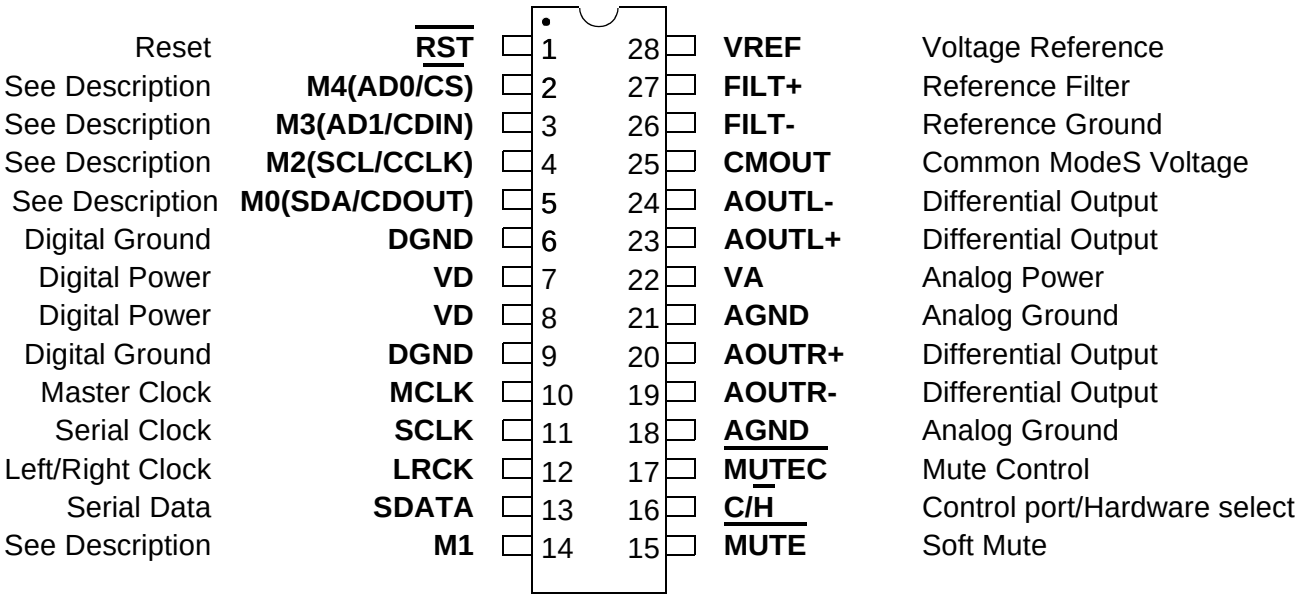
0 - Disabled

1 - Enabled

Function:

The analog and digital sections will be placed into a power-down mode when this function is enabled. This bit must be cleared to resume normal operation.

4. PIN DESCRIPTION



$\overline{\text{RST}}$	1	**Reset** (*Input*) - The device enters a low power mode and all internal state machines registers are reset when low. When high, the device will be in a normal operation mode.
DGND	6, 9	**Digital Ground** (*Input*) - Digital ground reference.
VD	7, 8	**Digital Power** (*Input*) - Digital power supply. Typically 3.0 to 5.0 VDC.

MCLK	10	**Master Clock** (*Input*) - The master clock frequency must be either 256x, 384x, 512x or 768x the input sample rate in Operational Mode 0; either 128x, 192x 256x or 384x the input sample rate in Operational Mode 1 ; or 64x, 96x 128x or 192x the input sample rate in Operational Mode 2 . Tables 4-6 illustrate the standard audio sample rates and the required master clock frequencies.

Sample Rate (kHz)	MCLK (MHz)			
	256x	384x	512x	768x
32	8.1920	12.2880	16.3840	24.5760
44.1	11.2896	16.9344	22.5792	33.8688
48	12.2880	18.4320	24.5760	36.8640

Table 1. Operational Mode 0 (16 to 55 kHz sample rates) Common Clock Frequencies

Sample Rate (kHz)	MCLK (MHz)			
	128x	192x	256x	384x
48	6.1440	8.1920	12.2880	16.3840
64	8.1920	12.2880	16.3840	24.5760
88.2	11.2896	16.9344	22.5792	33.8688
96	12.2880	18.4320	24.5760	36.8640

Table 2. Operational Mode 1 (45 to 105 kHz sample rates) Common Clock Frequencies

Sample Rate (kHz)	MCLK (MHz)			
	64x	96x	128x	192x
176.4	11.2896	16.9344	22.5792	33.8688
192	12.2880	18.4320	24.5760	36.8640

Table 3. Operational Mode 2 (95 to 200 kHz sample rates) Common Clock Frequencies

SCLK	11	**Serial Clock** *(Input)* - Clocks individual bits of serial data into the SDATA pin. The required relationship between the Left/Right clock, serial clock and serial data is defined by either the Mode Control Byte in Control Port Mode or the M0 - M4 pins in Hardware Mode. The options are detailed in Figures 20-23.
LRCK	12	**Left/Right Clock** *(Input)* - The Left/Right clock determines which channel is currently being input on the serial audio data input, SDATA. The frequency of the Left/Right clock must be at the input sample rate. Audio samples in Left/Right sample pairs will be simultaneously output from the digital-to-analog converter whereas Right/Left pairs will exhibit a one sample period difference. The required relationship between the Left/Right clock, serial clock and serial data is defined by the Mode Control Byte and the options are detailed in Figures 20-23.
SDATA	13	**Serial Audio Data** *(Input)* - Two's complement MSB-first serial data is input on this pin. The data is clocked into SDATA via the serial clock and the channel is determined by the Left/Right clock. The required relationship between the Left/Right clock, serial clock and serial data is defined by the Mode Control Byte and the options are detailed inin Figures 20-23.

MUTE	15	**Soft Mute** *(Input)* - The analog outputs will ramp to a muted state when enabled. The ramp requires 1152 left/right clock cycles in Operational Mode 0, 2304 cycles in Operational Mode 1 and 4608 cycles in Operational Mode 2 . The bias voltage on the outputs will be retained and MUTEC will go active at the completion of the ramp period. The analog outputs will ramp to a normal state when this function transitions from the enabled to disabled state. The ramp requires 1152 left/right clock cycles in Operational Mode 0, 2304 cycles in Operational Mode 1 and 4608 cycles in Operational Mode 2 . The MUTEC will release immediately on setting MUTE = 1. The converter analog outputs will mute when enabled. The bias voltage on the outputs will be retained and MUTEC will go active during the mute period
C/H	16	**Control Port / Hardware Mode Select** *(Input)* - Determines if the device will operate in either the Hardware Mode or Control Port Mode.
MUTEC	17	**Mute Control** *(Output)* **-** The Mute Control pin goes low during power-up initialization, reset, muting, master clock to left/right clock frequency ratio is incorrect or power-down. This pin is intended to be used as a control for an external mute circuit to prevent the clicks and pops that can occur in any single supply system. Use of Mute Control is not mandatory but recommended for designs requiring the absolute minimum in extraneous clicks and pops.
AGND	18, 21	**Analog Ground** *(Inputs)* - Analog ground reference.
AOUTR- , AOUTR+ **AOUTL- , AOUTL+**	19, 20, 23, 24	**Differential Analog Outputs** *(Outputs)* **-** The full scale differential analog output level is specified in the Analog Characteristics specifications table.
VA	22	**Analog Power** *(Input)* **-** Power for the analog and reference circuits. Typically 5.5 VDC.
CMOUT	25	**Common Mode Voltage** *(Output)* **-** Filter connection for internal bias voltage, typically 50% of VREF. Capacitors must be connected from CMOUT to analog ground, as shown in the Typical Connection Diagram. CMOUT has a typical source impedence of 25 kΩ and any current drawn from this pin will alter device performance.
FILT-	26	**Reference Ground** *(Input)* - Ground reference for the internal sampling circuits. Must be connected to analog ground.
FILT+	27	**Reference Filter** *(Output)* **-** Positive reference for internal sampling circuits. External capacitors are required from FILT+ to analog ground, as shown in the Typical Connection Diagram. The recommended values will typically provide 60 dB of PSRR at 1 kHz and 40 dB of PSRR at 120 Hz. FILT+ is not intended to supply external current.
VREF	28	**Voltage Reference Input** *(Input)* - Analog voltage reference. Typically 5.5 VDC.
M0, M1, M2, M3, M4 (Hardware Mode)	2, 3, 4, 5,14	**Mode Select** *(Inputs)* - The Mode Select pins determine the operational mode of the device as detailed in Tables 4-7. The options include; Selection of the Digital Interface Format which determines the required relationship between the Left/Right clock, serial clock and serial data as detailed in Figures 20-23Selection of the standard 15 µs/50 µs digital de-emphasis filter response, Figure 28, which requires reconfiguration of the digital filter to maintain the proper filter response for 32, 44.1 or 48 kHz sample rates. Selection of the appropriate clocking mode to match the input sample rates.
AD0 / CS (Control Port Mode)	2	**Address Bit 0 / Chip Select** *(Input)* - In 2 wire mode, AD0 is a chip address bit. CS is used to enable the control port interface in SPI mode. The device will enter the SPI mode at anytime a high to low transition is detected on this pin. Once the device has entered the SPI mode, it will remain until either the part is reset or undergoes a power-down cycle.

AD1/CDIN (Control Port Mode)	3	**Address Bit 1 / Control Data Input** *(Input)* - In 2 Wire Mode, AD1 is a chip address bit. CDIN is the control data input line for the control port interface in SPI mode.
SCL/CCLK (Control Port Mode)	4	**Serial Control Interface Clock** *(Input)* - In 2 Wire Mode, SCL clocks the serial control data into or from SDA/CDOUT. In SPI mode, CCLK clocks the serial data into AD1/CDIN and out of SDA/CDOUT.
SDA/CDOUT (Control Port Mode)	5	**Serial Control Data I/O** *(Input/Output)* - In 2 Wire Mode, SDA is a data input/output. CDOUT is the control data output for the control port interface in SPI mode.
M1 (Control Port Mode)	14	**Mode Select** *(Input)* - This pin is not used in Control Port Mode and must be terminated to ground.

5. APPLICATIONS

5.1 Recommended Power-up Sequence

1) Hold $\overline{\text{RST}}$ high until the power supplies, master clock, and left/right clock are stable.
2) Bring $\overline{\text{RST}}$ high.

6. CONTROL PORT INTERFACE

The control port is used to load all the internal settings of the CS43122. The operation of the control port may be completely asynchronous to the audio sample rate. However, to avoid potential interference problems, the control port pins should remain static if no operation is required.

The control port has 2 modes: SPI and "2 wire", with the CS43122 operating as a slave device in both modes. If 2 wire operation is desired, AD0/$\overline{\text{CS}}$ should be tied to VD or DGND. If the CS43122 ever detects a high to low transition on AD0/$\overline{\text{CS}}$ after power-up, SPI mode will be selected.

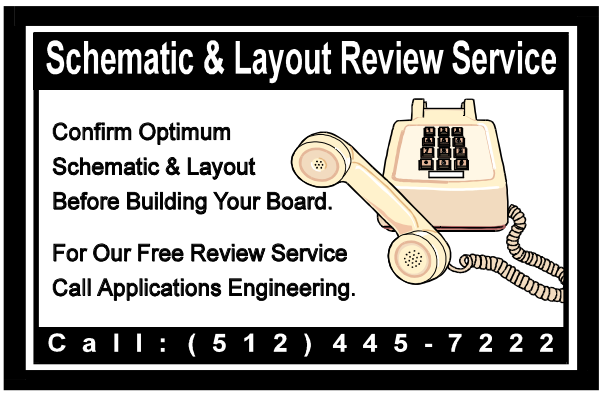
6.1 SPI Mode

In SPI mode, $\overline{\text{CS}}$ is the CS43122 chip select signal, CCLK is the control port bit clock, CDIN is the input data line from the microcontroller, CDOUT is the data output and the chip address is 0010000. The data is clocked on the rising edge of CCLK.

Figure 5 shows the operation of the control port in SPI mode. To write to a register, bring $\overline{\text{CS}}$ low. The first 7 bits on CDIN form the chip address, and must be 0010000. The eighth bit is a read/write indicator (R/$\overline{\text{W}}$). The next 8 bits form the Memory Address Pointer (MAP), which is set to 01h. The next 8 bits are the data which will be placed into the register designated by the MAP.

6.2 2 Wire Mode

In 2 Wire Mode, SDA is a bi-directional data line. Data is clocked into and out of the part by the clock, SCL, with the clock to data relationship as shown in Figure 2. There is no $\overline{\text{CS}}$ pin. Pins AD0 and AD1 form the partial chip address and should be tied to VD or DGND as required. The 7-bit address field, which is the first byte sent to the CS43122, must be 00100(AD1)(AD0) where (AD1) and (AD0) match the setting of the AD0 and AD1 pins. The eighth bit of the address byte is the R/$\overline{\text{W}}$ bit (high for a read, low for a write). If the operation is a write, the next byte is the Memory Address Pointer, MAP, which selects the register to be read or written. The MAP is then followed by the data to be written. If the operation is a read, then the contents of the register pointed to by the MAP will be output after the chip address.



6.3 Memory Address Pointer (MAP)

7	6	5	4	3	2	1	0
INCR	Reserved	Reserved	Reserved	Reserved	MAP2	MAP1	MAP0
0	0	0	0	0	0	0	1

INCR (Auto MAP Increment Enable)
Default = '0'
0 - Disabled
1 - Enabled

MAP0-2 (Memory Address Pointer)
Default = '001'

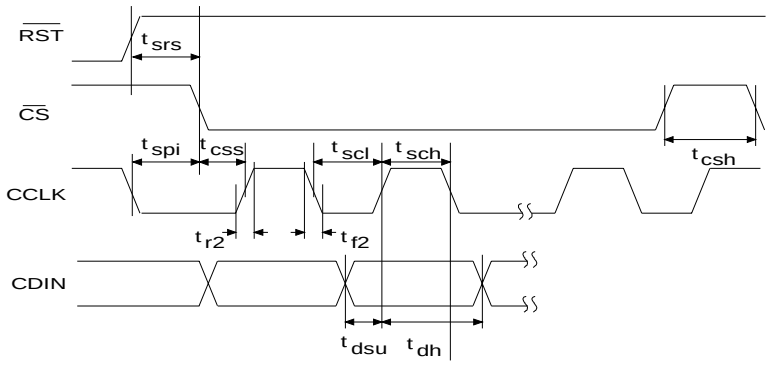
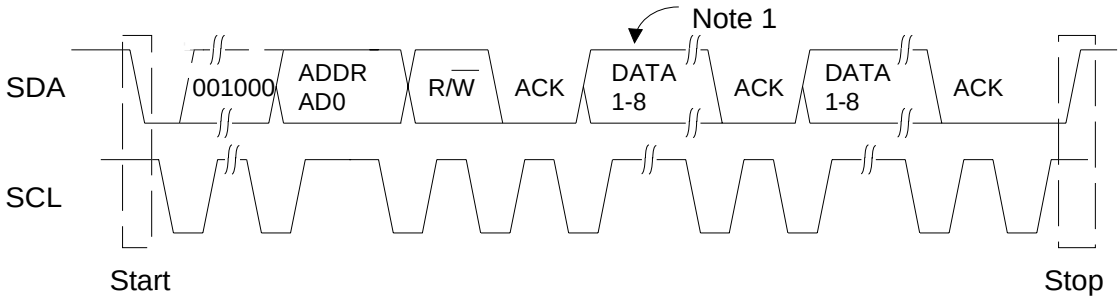


Figure 5. Control Port Timing, SPI mode



Note: If operation is a write, this byte contains the Memory Address Pointer, MAP.

Figure 6. Control Port Timing, 2 wire Mode

M4	M1 (DIF1)	M0 (DIF0)	DESCRIPTION	FORMAT	FIGURE
0	0	0	Left Justified, up to 24-bit data	0	20
0	0	1	I^2S, up to 24-bit data	1	21
0	1	0	Right Justified, 16-bit Data	2	22
0	1	1	Right Justified, 24-bit Data	3	23

Table 4. Operational Mode 0 (16 to 55 kHz) Digital Interface Format Options

M4	M3 (DEM1)	M2 (DEM0)	DESCRIPTION	FIGURE
0	0	0	32 kHz De-Emphasis	19
0	0	1	44.1 kHz De-Emphasis	19
0	1	0	48 kHz De-Emphasis	19
0	1	1	De-Emphasis Disabled	-

Table 5. Operational Mode 0 (16 to 55 kHz) De-Emphasis Options

M4	M3	M2	M1	M0	DESCRIPTION
1	1	1	0	0	Left Justified up to 24-bit data, Format 0
1	1	1	0	1	I^2S up to 24-bit data, Format 1
1	1	1	1	0	Right Justified 16-bit data, Format 2
1	1	1	1	1	Right Justified 24-bit data, Format 3

Table 6. Operational Mode 1 (45 to 105 kHz) Sample Rate Mode Options

M4	M3	M2	M1	M0	DESCRIPTION
1	1	0	0	0	Left Justified up to 24-bit data, Format 0
1	1	0	0	1	I^2S up to 24-bit data, Format 1
1	1	0	1	0	Right Justified 16-bit data, Format 2
1	1	0	1	1	Right Justified 24-bit data, Format 3

Table 7. Operational Mode 2 (95 to 200 kHz) Sample Rate Mode Options

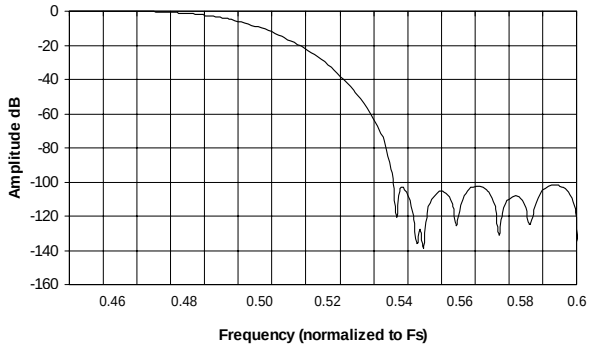


Figure 7. Operational Mode 0 Transition Band

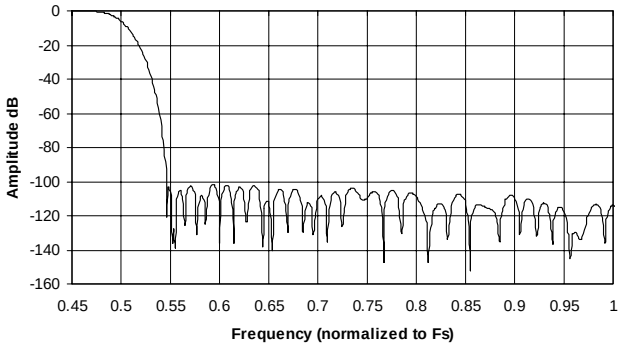


Figure 8. Operational Mode 0 Stopband Rejection

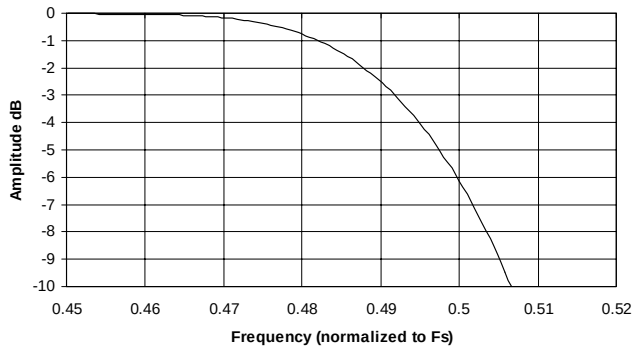


Figure 9. Operational Mode 0 Transition Band

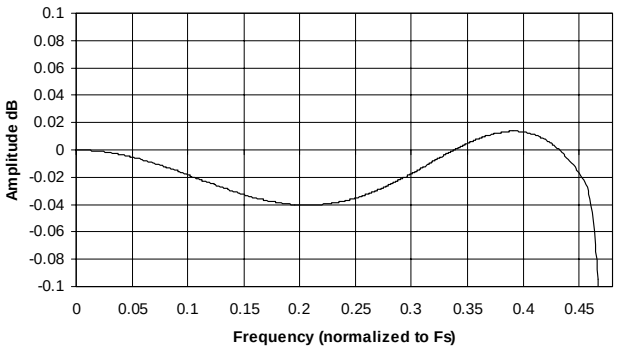


Figure 10. Operational Mode 0 Frequency Response

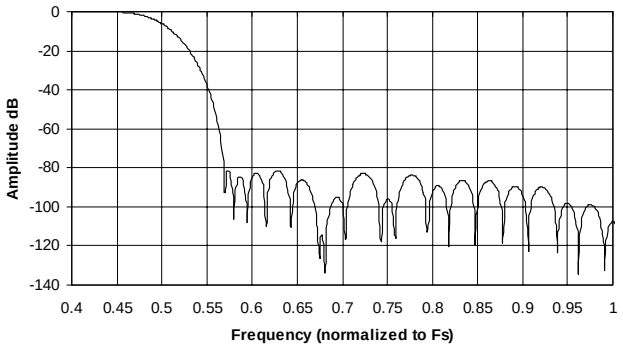


Figure 11. Operational Mode 0 Stopband

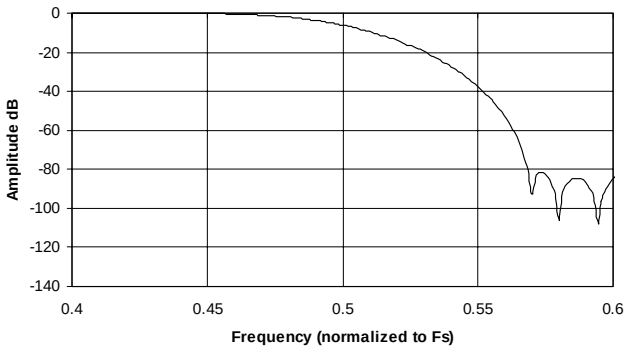


Figure 12. Operational Mode 0 Transition Band

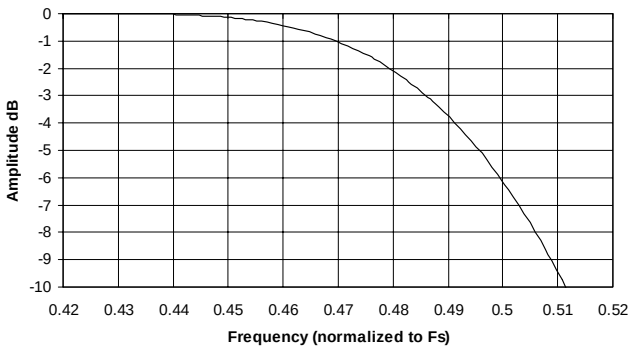


Figure 13. Operational Mode 0 Transition Band

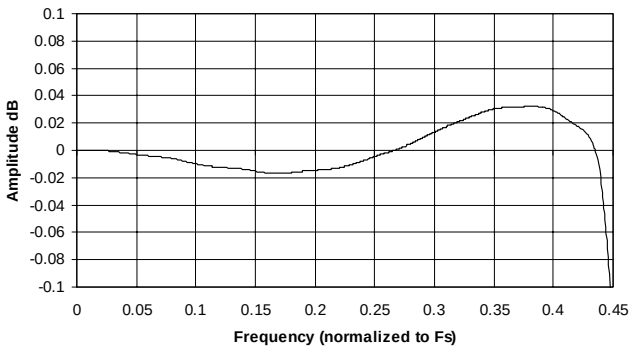


Figure 14. Operational Mode 0 Frequency Response

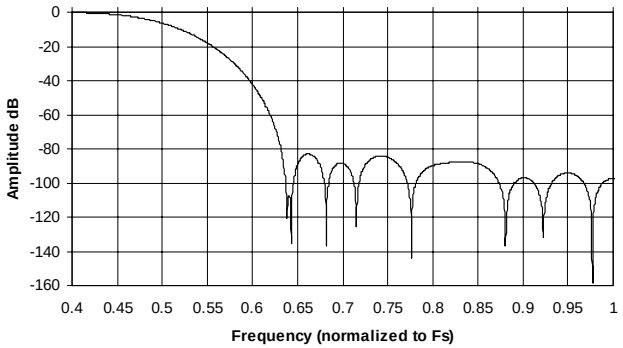


Figure 15. Operational Mode 2 Stopband Rejection

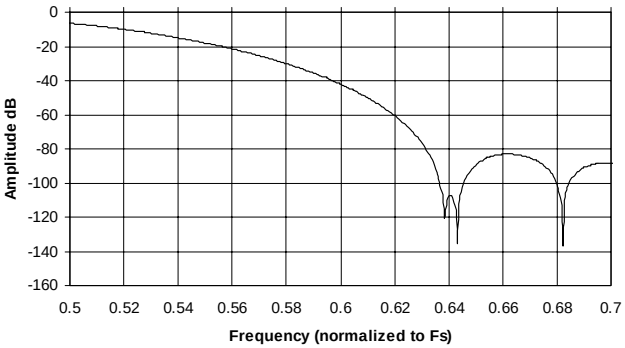


Figure 16. Operational Mode 2 Transition Band

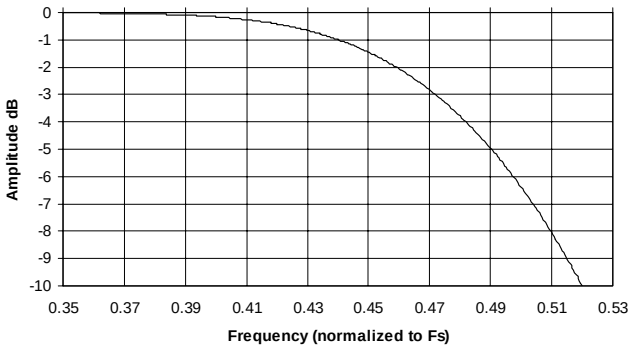


Figure 17. Operational Mode 2 Transition Band

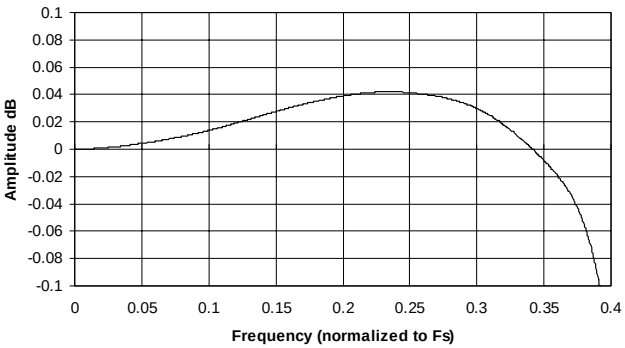


Figure 18. Operational Mode 2 Frequency Response

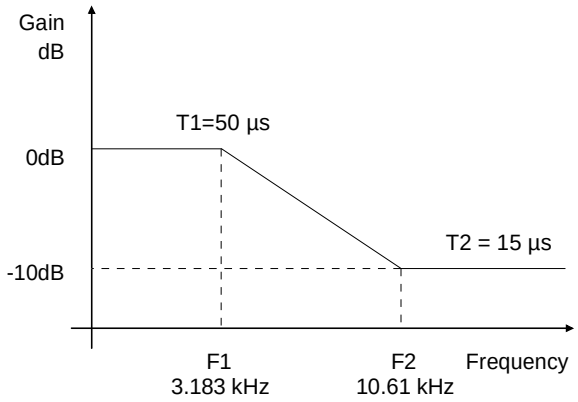


Figure 19. De-Emphasis Curve

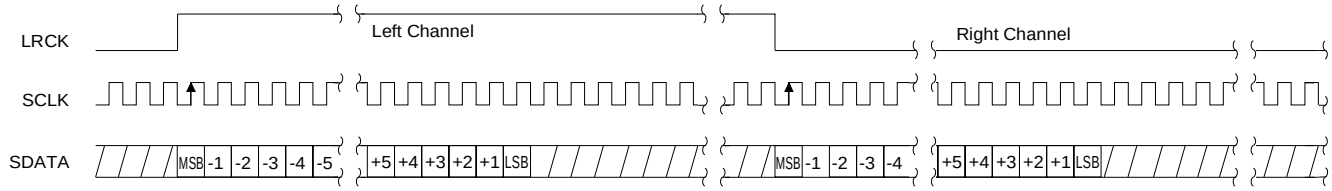


Figure 20. Format 0, Left Justified

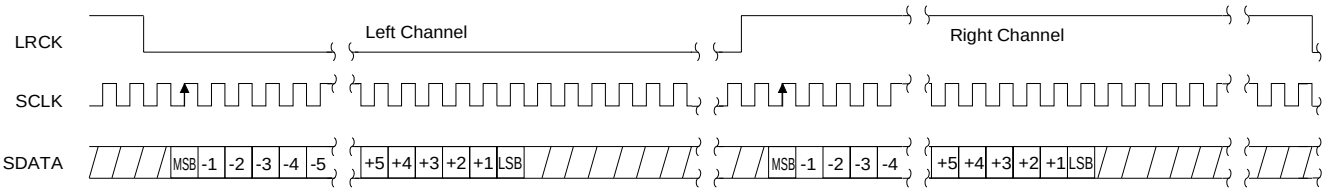


Figure 21. Format 1, I^2S

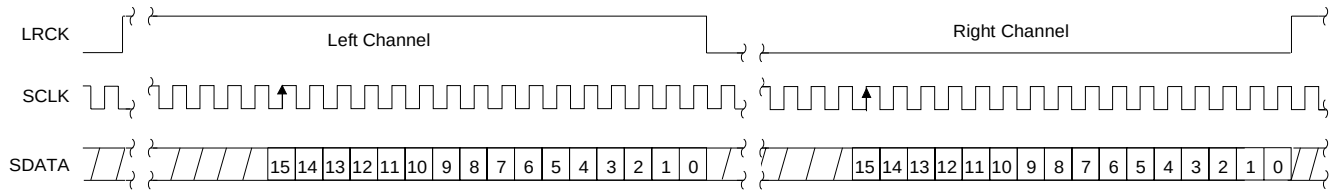


Figure 22. Format 2, Right Justified, 16-Bit Data

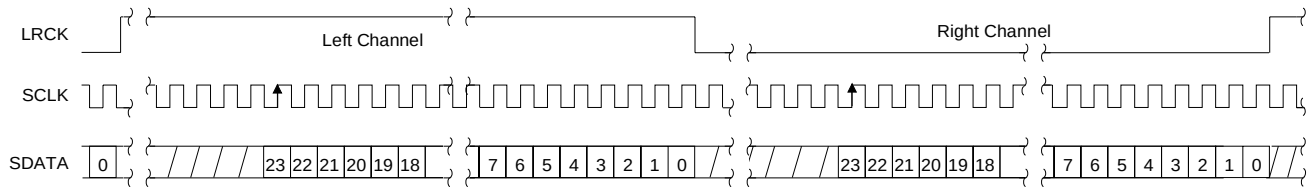


Figure 23. Format 3, Right Justified, 24-Bit Data

7. PARAMETER DEFINITIONS

Total Harmonic Distortion + Noise (THD+N)

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels.

Dynamic Range

The ratio of the full scale rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic range is a signal-to-noise measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is then added to the resulting measurement to refer the measurement to full scale. This technique ensures that the distortion components are below the noise level and do not effect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307.

Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with all zeros to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

Gain Error

The deviation from the nominal full scale analog output for a full scale digital input.

Gain Drift

The change in gain value with temperature. Units in ppm/°C.

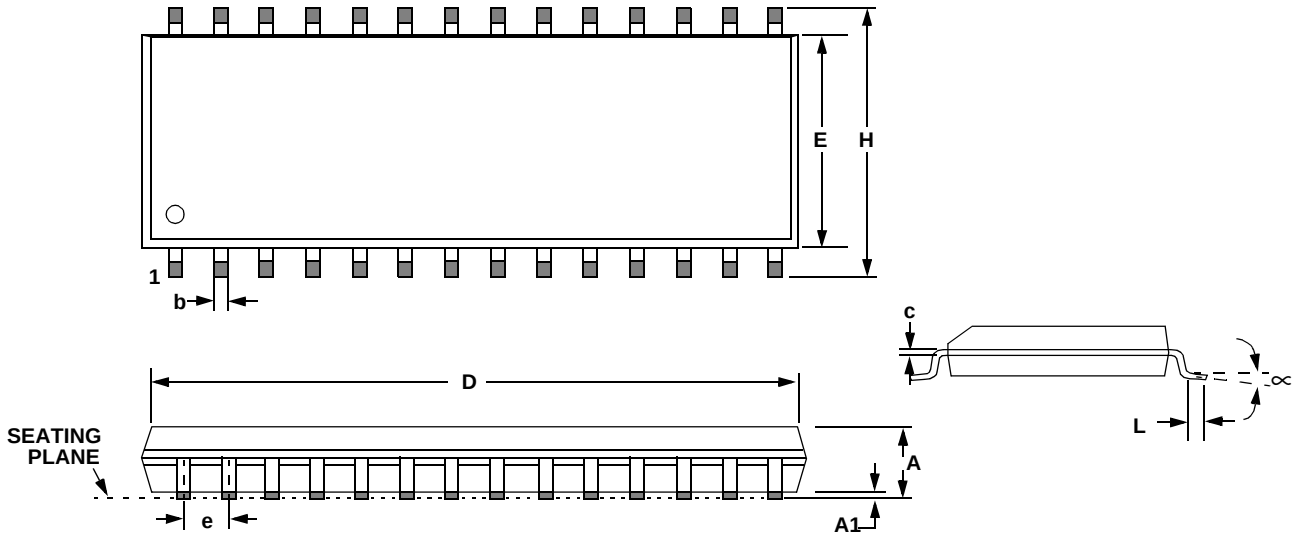
8. REFERENCES

1) "How to Achieve Optimum Performance from Delta-Sigma A/D & D/A Converters" by Steven Harris. Paper presented at the 93rd Convention of the Audio Engineering Society, October 1992.

2) CDB43122 Evaluation Board Datasheet

9. PACKAGE DIMENSIONS

28L SOIC (300 MIL BODY) PACKAGE DRAWING



	INCHES			MILLIMETERS		
DIM	**MIN**	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**
A	0.093	0.098	0.104	2.35	2.50	2.65
A1	0.004	0.008	0.012	0.10	0.20	0.30
b	0.013	0.017	0.020	0.33	0.42	0.51
C	0.009	0.011	0.013	0.23	0.28	0.32
D	0.697	0.705	0.713	17.70	17.90	18.10
E	0.291	0.295	0.299	7.40	7.50	7.60
e	0.040	0.050	0.060	1.02	1.27	1.52
H	0.394	0.407	0.419	10.00	10.34	10.65
L	0.016	0.026	0.050	0.40	0.65	1.27
∝	0°	4°	8°	0°	4°	8°

JEDEC #: MS-013

Controling Dimension is Millimeters

• Notes •


SMART
Analog
™