CSD15380F3 20-V N-Channel FemtoFET™ MOSFET

1 Features

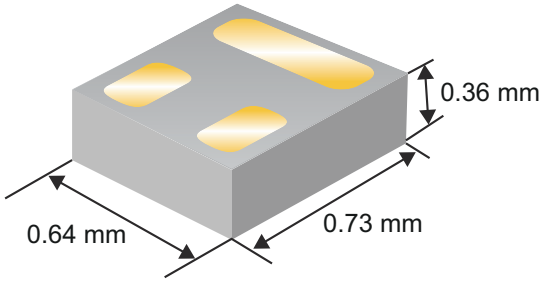
- Ultra-low C_{iss} and C_{oss}
- Ultra-low Q_g and Q_{gd}
- Ultra-small footprint
  - 0.73 mm × 0.64 mm
- Ultra-low profile
  - 0.36-mm max height
- Integrated ESD protection diode
  - Rated > 4-kV HBM
  - Rated > 2-kV CDM
- Lead and halogen free
- RoHS compliant

2 Applications

- Optimized for load switch applications
- Optimized for general purpose switching applications
- Battery applications
- Handheld and mobile applications

3 Description

This 20-V, 990-mΩ, N-Channel FemtoFET™ MOSFET is designed and optimized to minimize the footprint in many handheld and mobile applications. Ultra-low capacitance improves switching speeds. When used in data line applications, the low capacitance minimizes noise coupling. This technology is capable of replacing standard small signal MOSFETs while providing a substantial reduction in footprint size.



Typical Part Dimensions

Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	20		V
Q_g	Gate Charge Total (4.5 V)	0.216		nC
Q_{gd}	Gate Charge Gate-to-Drain	0.027		nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = 2.5 V	2220	mΩ
		V_{GS} = 4.5 V	1170	
		V_{GS} = 8 V	990	
$V_{GS(th)}$	Threshold Voltage	1.1		V

Device Information(1)

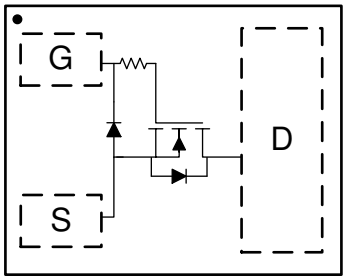
DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD15380F3	3000	7-Inch Reel	Femto 0.73-mm × 0.64-mm Land Grid Array (LGA)	Tape and Reel
CSD15380F3T	250			

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

T_A = 25°C (unless otherwise stated)		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	20	V
V_{GS}	Gate-to-Source Voltage	10	V
I_D	Continuous Drain Current(1)	0.9	A
	Continuous Drain Current(2)	0.5	
I_{DM}	Pulsed Drain Current(3)	1.6	A
P_D	Power Dissipation(1)	1.4	W
	Power Dissipation(2)	0.5	
$V_{(ESD)}$	Human-Body Model (HBM)	4	kV
	Charged-Device Model (CDM)	2	
T_J, T_{stg}	Operating Junction and Storage Temperature	–55 to 150	°C

(1) Typical $R_{\theta JA}$ = 90°C/W on 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu pad on a 0.06-in (1.52-mm) thick FR4 PCB
(2) Typical $R_{\theta JA}$ = 255°C/W on min Cu board
(3) Pulse duration ≤ 100 µs, duty cycle ≤ 1%.



Top View

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (July 2017) to Revision B (February 2022)	Page
• Changed ultra-low profile bullet from 0.35 mm to 0.36 mm in height	1
• Updated ultra-low profile image height from 0.35 mm to 0.36 mm	1
• Changed ultra-low profile image height from 0.35 mm to 0.36 mm	7
• Added FemtoFET Surface Mount Guide note	8

Changes from Revision A (July 2017) to Revision B (November 2018)	Page
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5 Specifications

5.1 Electrical Characteristics

T_A = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_{DS} = 250 µA	20			V
I_{DSS}	Drain-to-Source leakage current	V_{GS} = 0 V, V_{DS} = 16 V			50	nA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = 10 V			25	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_{DS} = 2.5 µA	0.85	1.10	1.35	V
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = 2.5 V, I_{DS} = 0.1 A		2220	4000	mΩ
		V_{GS} = 4.5 V, I_{DS} = 0.1 A		1170	1460	
		V_{GS} = 8 V, I_{DS} = 0.1 A		990	1190	
g_{fs}	Transconductance	V_{DS} = 2 V, I_{DS} = 0.1 A		0.64		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 10 V, f = 1 MHz		8.1	10.5	pF
C_{oss}	Output capacitance			5.9	7.7	pF
C_{rss}	Reverse transfer capacitance			0.13	0.17	pF
R_G	Series gate resistance			9.6		Ω
Q_g	Gate charge total (4.5 V)	V_{DS} = 10 V, I_{DS} = 0.1 A		0.216	0.281	nC
Q_{gd}	Gate charge gate-to-drain			0.027		nC
Q_{gs}	Gate charge gate-to-source			0.077		nC
$Q_{g(th)}$	Gate charge at V_{th}			0.048		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = 10 V, V_{GS} = 4.5 V, I_{DS} = 0.1 A, R_G = 0 Ω		3		ns
t_r	Rise time			1		ns
$t_{d(off)}$	Turnoff delay time			7		ns
t_f	Fall time			7		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = 0.1 A, V_{GS} = 0 V		0.85	1	V

5.2 Thermal Information

T_A = 25°C (unless otherwise stated)

THERMAL METRIC		TYPICAL VALUES	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)	90	°C/W
	Junction-to-ambient thermal resistance(2)	255	

(1) Device mounted on FR4 material with 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu.
(2) Device mounted on FR4 material with minimum Cu mounting area.

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5.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise stated)

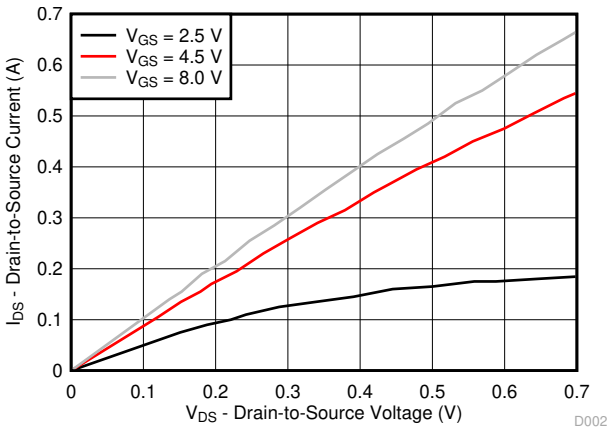
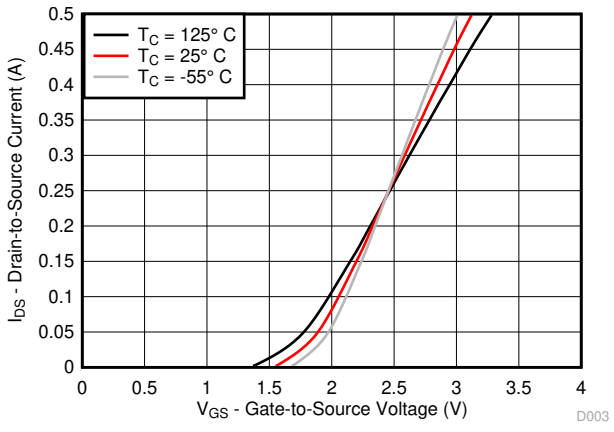


Figure 5-1. Saturation Characteristics



V_{DS} = 5 V

Figure 5-2. Transient Thermal Impedance

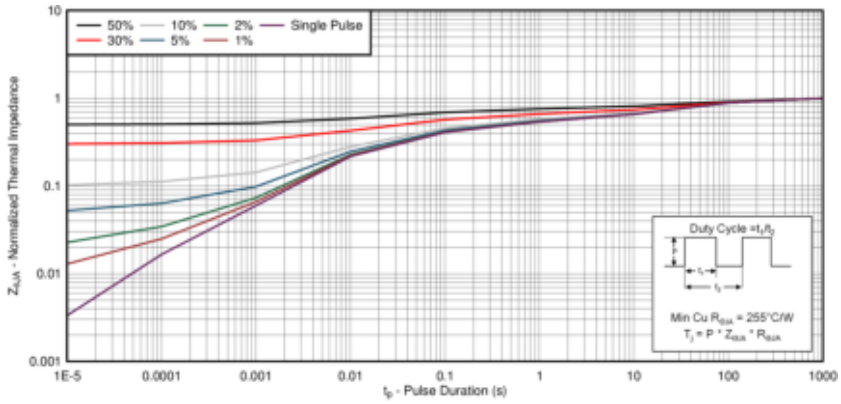
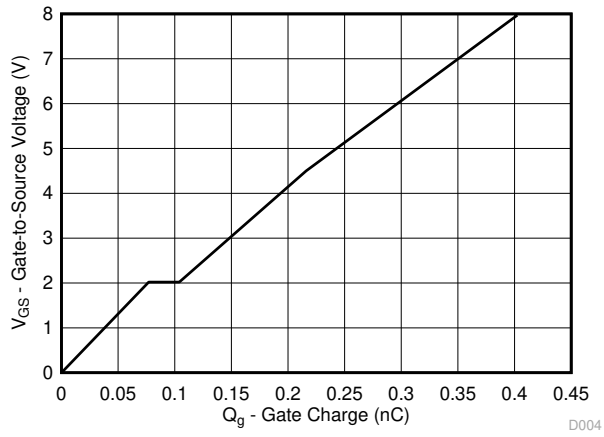


Figure 5-3. Transient Thermal Impedance



V_{DS} = 10 V I_D = 0.1 A

Figure 5-4. Gate Charge

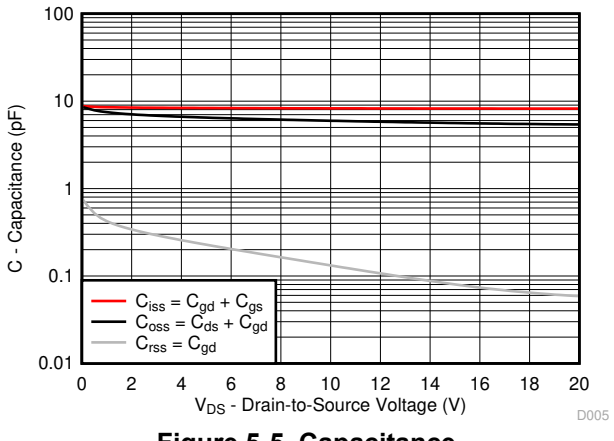
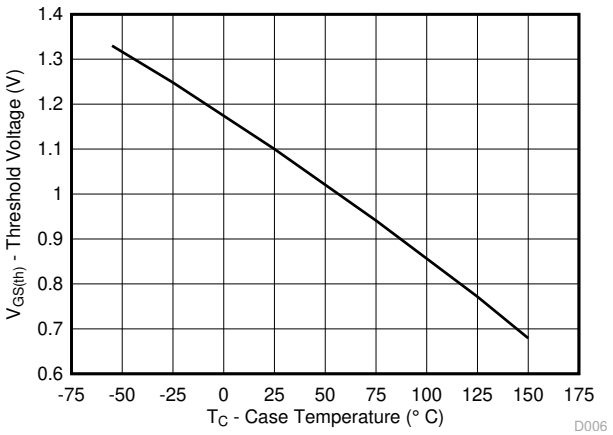


Figure 5-5. Capacitance

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I_D = 2.5 µA

Figure 5-6. Threshold Voltage vs Temperature

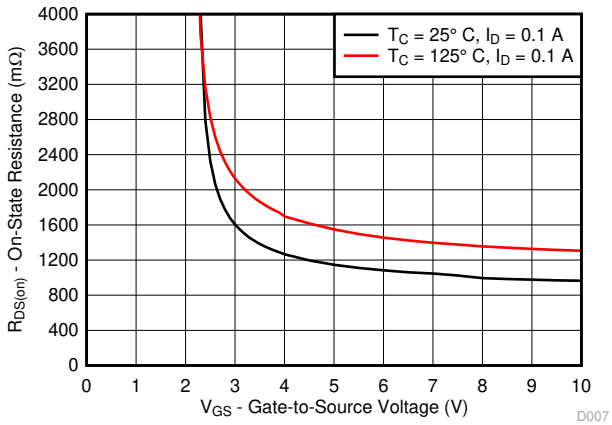
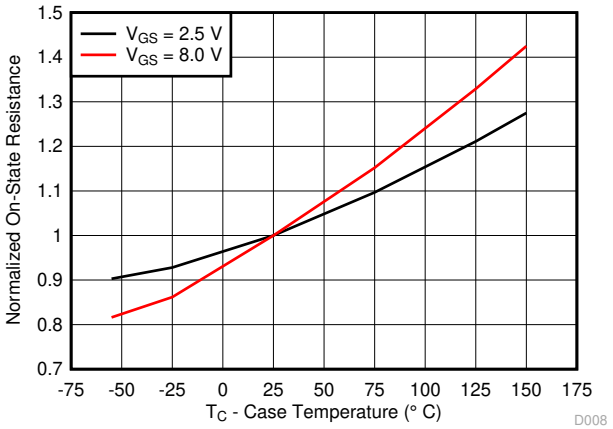


Figure 5-7. On-State Resistance vs Gate-to-Source Voltage



I_D = 0.1 A

Figure 5-8. Normalized On-State Resistance vs Temperature

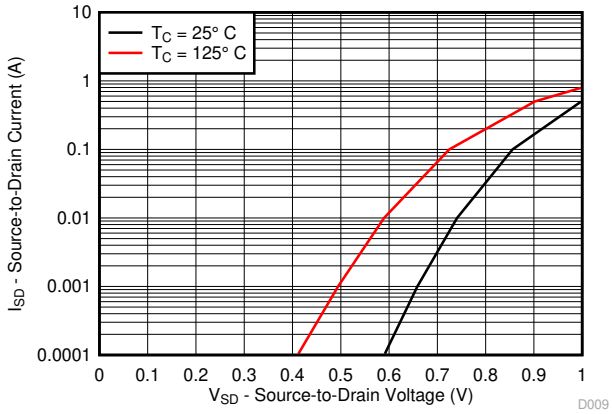
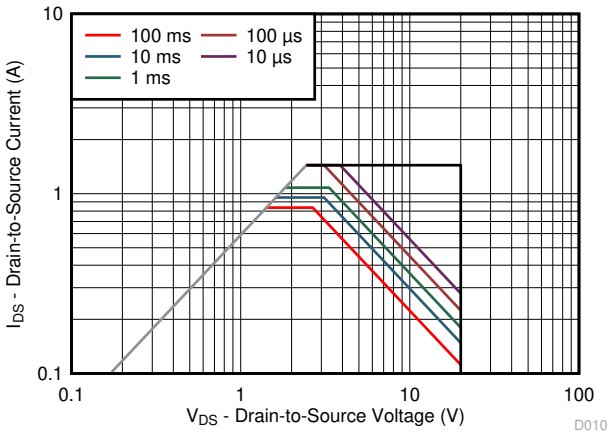


Figure 5-9. Typical Diode Forward Voltage



Single pulse, typical $R_{\theta JA}$ = 255°C/W (min Cu)

Figure 5-10. Maximum Safe Operating Area

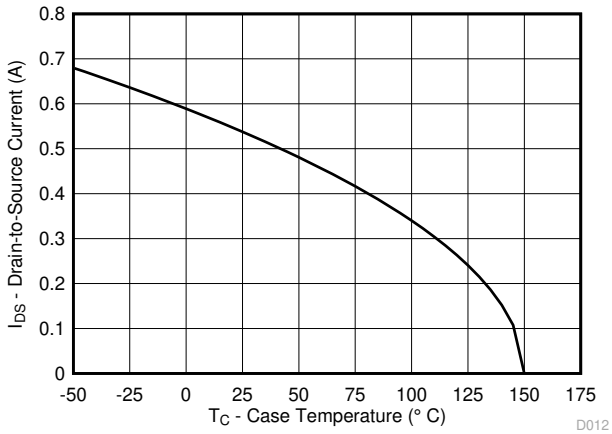


Figure 5-11. Maximum Drain Current vs Temperature

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6 Device and Documentation Support

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Trademarks

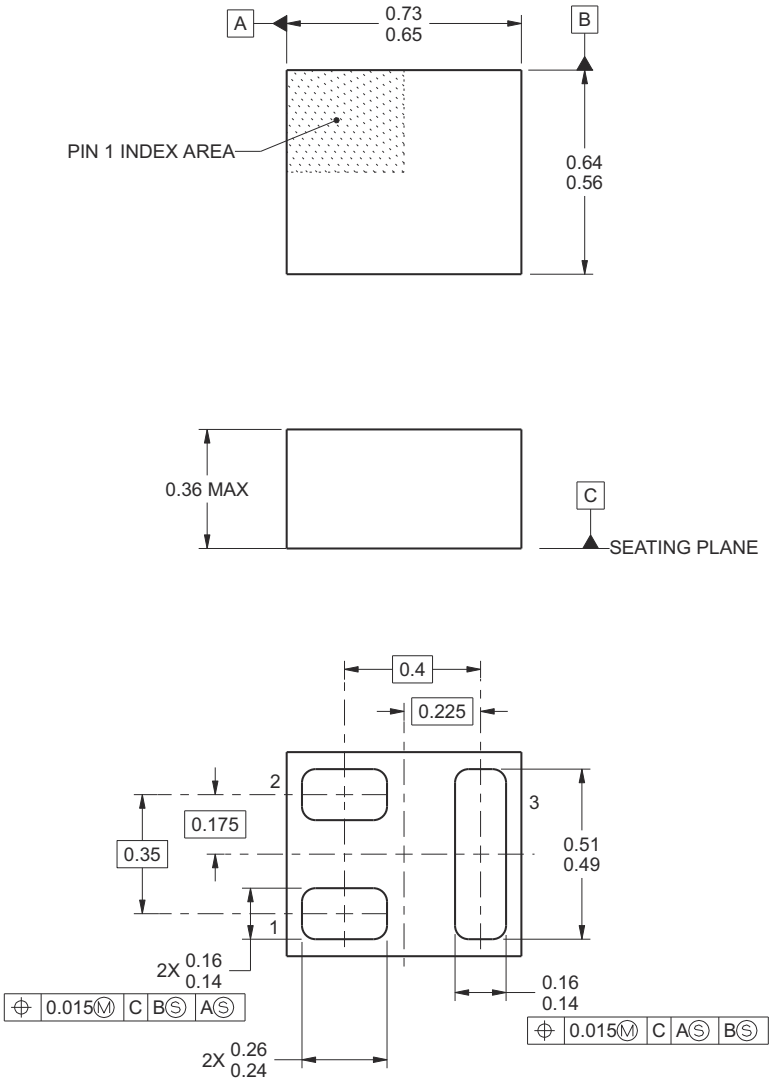
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7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Mechanical Dimensions



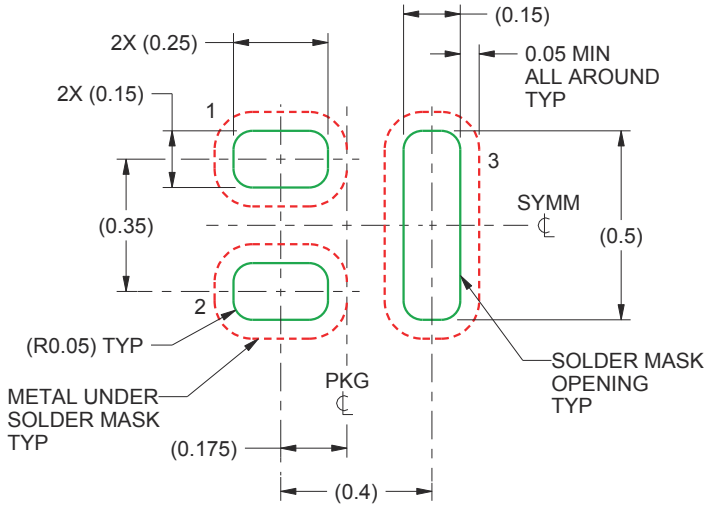
A. All linear dimensions are in millimeters (dimensions and tolerancing per AME T14.5M-1994).
B. This drawing is subject to change without notice.
C. This package is a lead-free solder land design.

Table 7-1. Pin Configuration

POSITION	DESIGNATION
Pin 1	Gate
Pin 2	Source
Pin 3	Drain

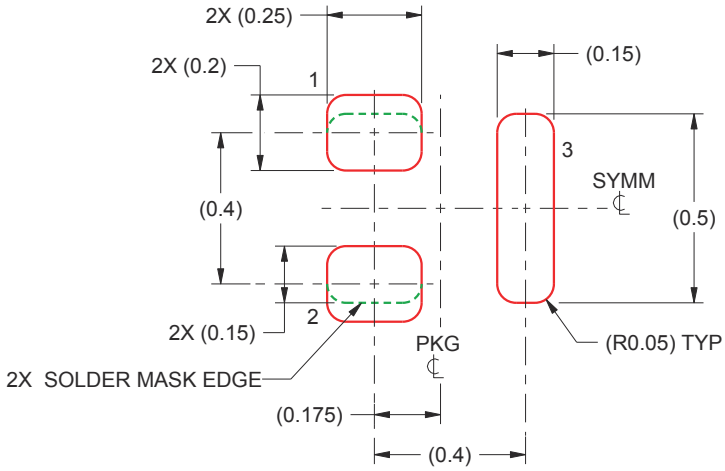
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7.2 Recommended Minimum PCB Layout



A. All dimensions are in millimeters.
B. For more information, see *FemtoFET Surface Mount Guide* (SLRA003D).

7.3 Recommended Stencil Pattern



A. All dimensions are in millimeters.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD15380F3	Active	Production	PICOSTAR (YJM) | 3	3000 | LARGE T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	6
CSD15380F3.B	Active	Production	PICOSTAR (YJM) | 3	3000 | LARGE T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	6
CSD15380F3T	Active	Production	PICOSTAR (YJM) | 3	250 | SMALL T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	6
CSD15380F3T.B	Active	Production	PICOSTAR (YJM) | 3	250 | SMALL T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	6

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

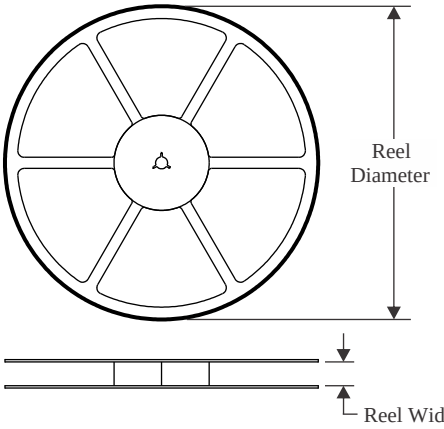
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

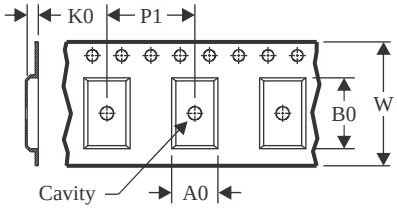
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

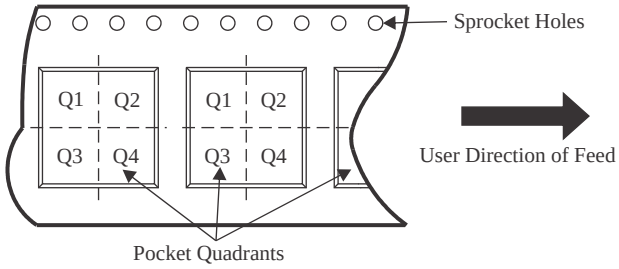


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

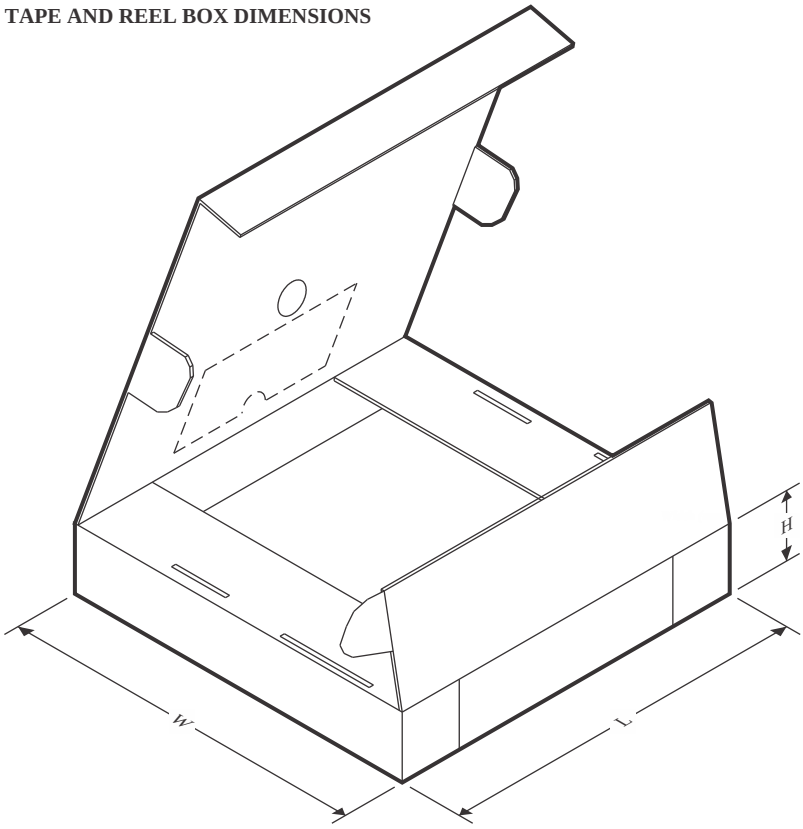
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD15380F3	PICOSTAR	YJM	3	3000	180.0	8.4	1.94	0.79	0.44	4.0	8.0	Q2
CSD15380F3T	PICOSTAR	YJM	3	250	180.0	8.4	1.94	0.79	0.44	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

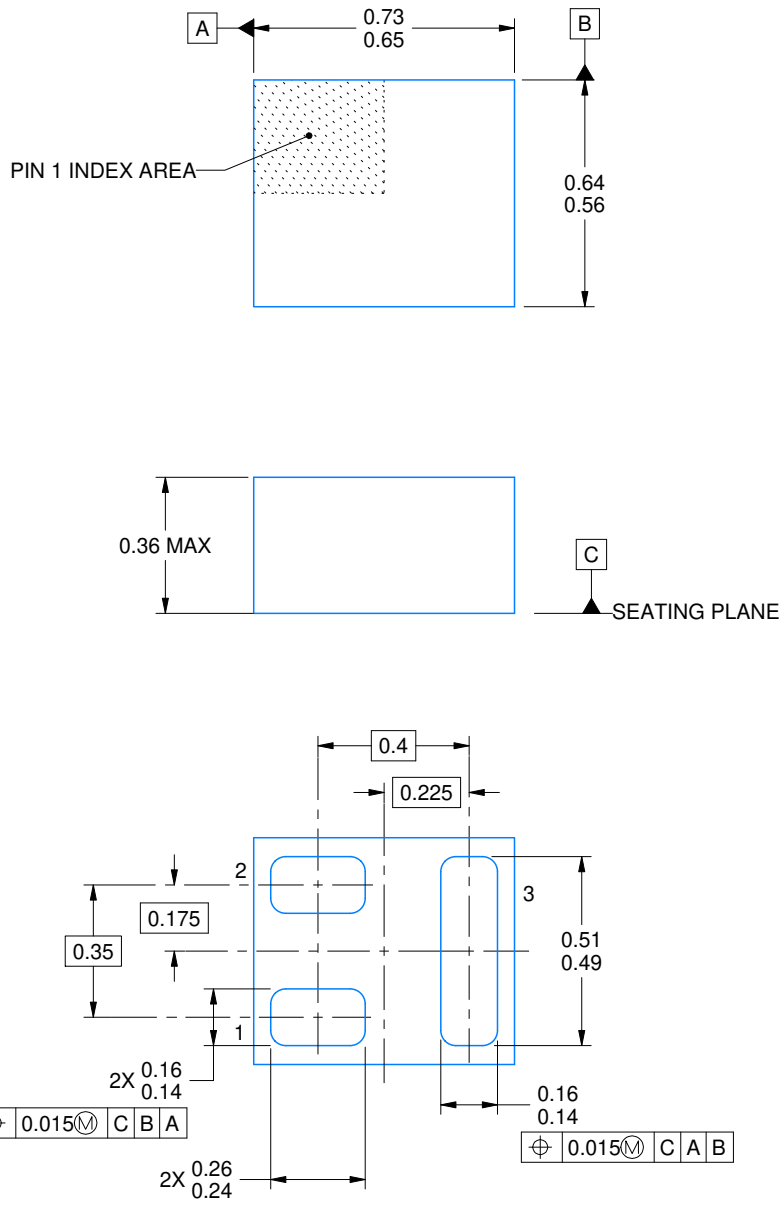
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD15380F3	PICOSTAR	YJM	3	3000	182.0	182.0	20.0
CSD15380F3T	PICOSTAR	YJM	3	250	182.0	182.0	20.0

PACKAGE OUTLINE

YJM0003A

PicoStar™ - 0.36 mm max height

PicoStar™

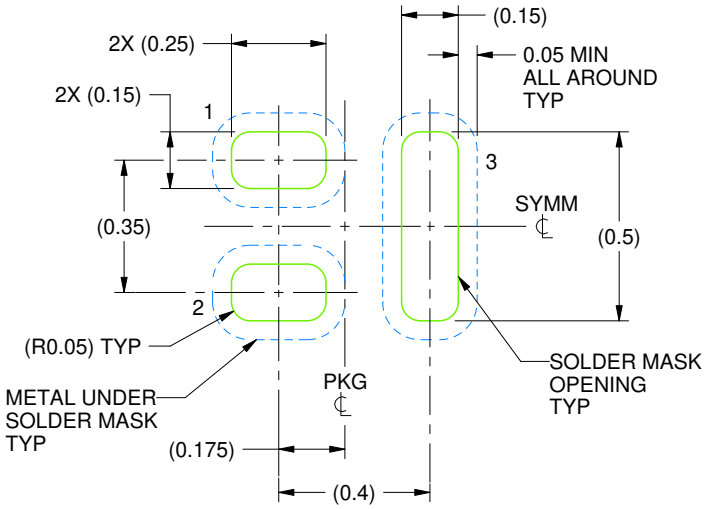


4222304/B 03/2022

PicoStar is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.
3. This package is a Pb-free bump design. Bump finish may vary. To determine the exact finish, refer to the device datasheet or contact a local TI representative.

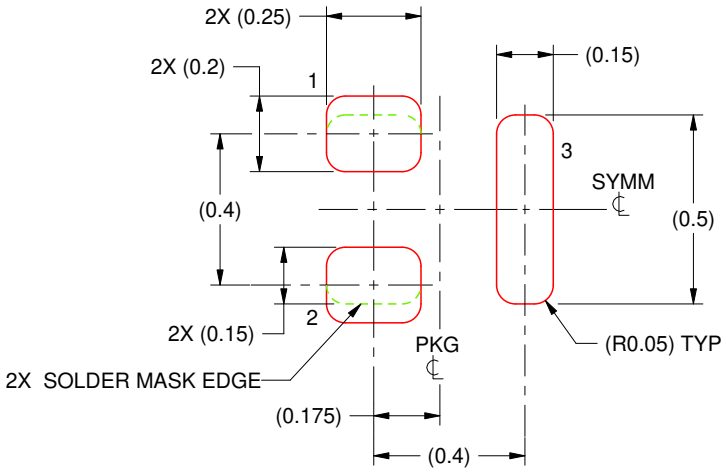


LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:50X

4222304/B 03/2022

NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:50X

4222304/B 03/2022

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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