TEXAS INSTRUMENTS

CSD17581Q5A

SLPS630 – SEPTEMBER 2016

CSD17581Q5A 30-V N-Channel NexFET™ Power MOSFETs

1 Features

- Low Q_g and Q_{gd}
- Low $R_{DS(on)}$
- Low Thermal Resistance
- Avalanche Rated
- Lead-Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 5-mm × 6-mm Plastic Package

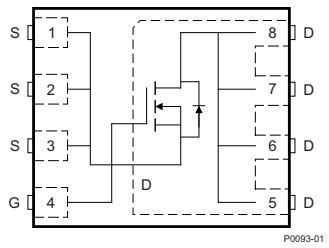
2 Applications

- Point-of-Load Synchronous Buck Converter for Applications in Networking, Telecom, and Computing Systems
- Optimized for Control FET Applications

3 Description

This 30-V, 2.9-mΩ, SON 5-mm × 6-mm NexFET™ power MOSFET is designed to minimize losses in power conversion applications.

Top View



Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	30		V
Q_g	Gate Charge Total (4.5 V)	20		nC
Q_{gd}	Gate Charge Gate to Drain	4		nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = 4.5 V	3.5	mΩ
		V_{GS} = 10 V	2.9	mΩ
$V_{GS(th)}$	Threshold Voltage	1.3		V

Device Information(1)

DEVICE	MEDIA	QTY	PACKAGE	SHIP
CSD17581Q5A	13-Inch Reel	2500	SON 5.00 × 6.00 mm Plastic Package	Tape and Reel
CSD17581Q5AT	7-Inch Reel	250		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

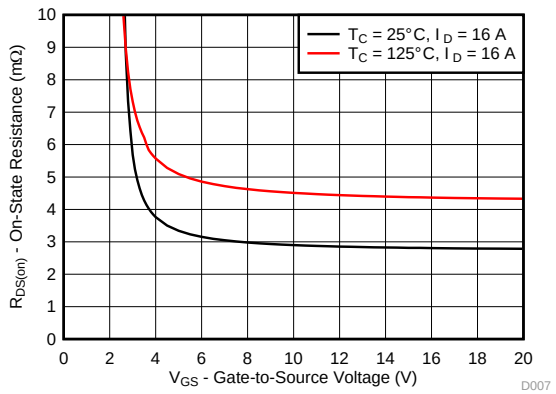
Absolute Maximum Ratings

T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	30	V
V_{GS}	Gate-to-Source Voltage	±20	V
I_D	Continuous Drain Current (Package Limited)	60	A
	Continuous Drain Current (Silicon Limited), T_C = 25°C	123	
	Continuous Drain Current(1)	24	
I_{DM}	Pulsed Drain Current(2)	256	A
P_D	Power Dissipation(1)	3.1	W
	Power Dissipation, T_C = 25°C	83	
T_J, T_{stg}	Operating Junction Temperature, Storage Temperature	–55 to 150	°C
E_{AS}	Avalanche Energy, Single Pulse I_D = 39 A, L = 0.1 mH, R_G = 25 Ω	76	mJ

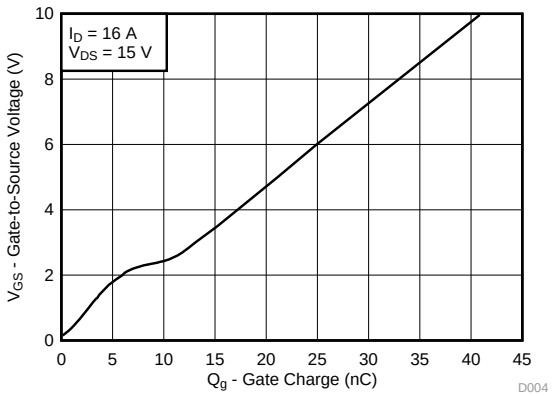
(1) Typical $R_{\theta JA}$ = 40°C/W on a 1-in², 2-oz Cu pad on a 0.06-in thick FR4 PCB.

(2) Max $R_{\theta JC}$ = 1.5°C/W, pulse duration ≤100 µs, duty cycle ≤1%

$R_{DS(on)}$ vs V_{GS}



Gate Charge



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

DATE	REVISION	NOTES
September 2016	*	Initial release.

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5 Specifications

5.1 Electrical Characteristics

T_A = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_D = 250 µA	30			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = 24 V			1	µA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	1.0	1.3	1.7	V
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = 4.5 V, I_D = 16 A		3.5	4.2	mΩ
		V_{GS} = 10 V, I_D = 16 A		2.9	3.4	mΩ
g_{fs}	Transconductance	V_{DS} = 3 V, I_D = 16 A		85		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 15 V, f = 1 MHz		2800	3640	pF
C_{oss}	Output capacitance			342	445	pF
C_{rss}	Reverse transfer capacitance			150	195	pF
R_G	Series gate resistance			1.8	3.6	Ω
Q_g	Gate charge total (4.5 V)	V_{DS} = 15 V, I_D = 16 A		20	25	nC
Q_g	Gate charge total (10 V)			41	54	nC
Q_{gd}	Gate charge gate-to-drain			4.0		nC
Q_{gs}	Gate charge gate-to-source			6.9		nC
$Q_{g(th)}$	Gate charge at V_{th}			3.6		nC
Q_{oss}	Output charge	V_{DS} = 15 V, V_{GS} = 0 V		11.7		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = 15 V, V_{GS} = 10 V, I_{DS} = 16 A, R_G = 0 Ω		12		ns
t_r	Rise time			21		ns
$t_{d(off)}$	Turnoff delay time			25		ns
t_f	Fall time			10		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = 16 A, V_{GS} = 0 V		0.8	1.0	V
Q_{rr}	Reverse recovery charge	V_{DS}= 15 V, I_F = 16 A, di/dt = 300 A/µs		13		nC
t_{rr}	Reverse recovery time			11		ns

5.2 Thermal Information

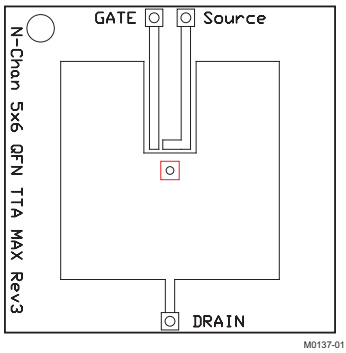
T_A = 25°C (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance(1)			1.5	°C
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)(2)			50	

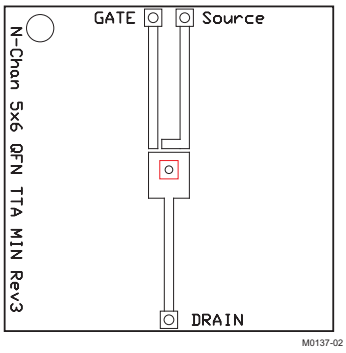
(1) $R_{\theta JC}$ is determined with the device mounted on a 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu pad on a 1.5-in × 1.5-in (3.81-cm × 3.81-cm), 0.06-in (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.

(2) Device mounted on FR4 material with 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu.

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Max $R_{\theta JA}$ = 50°C/W when mounted on 1-in^2 (6.45-cm^2) of 2-oz (0.071-mm) thick Cu.



Max $R_{\theta JA}$ = 125°C/W when mounted on a minimum pad area of 2-oz (0.071-mm) thick Cu.

5.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise stated)

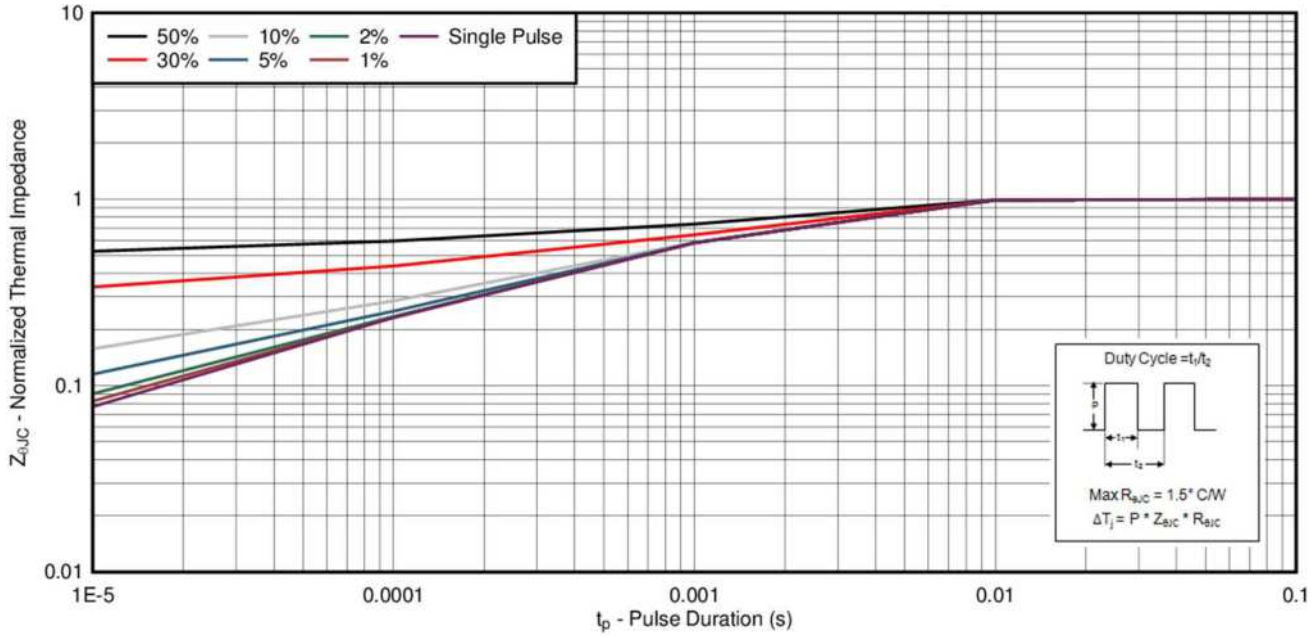


Figure 1. Transient Thermal Impedance

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Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)

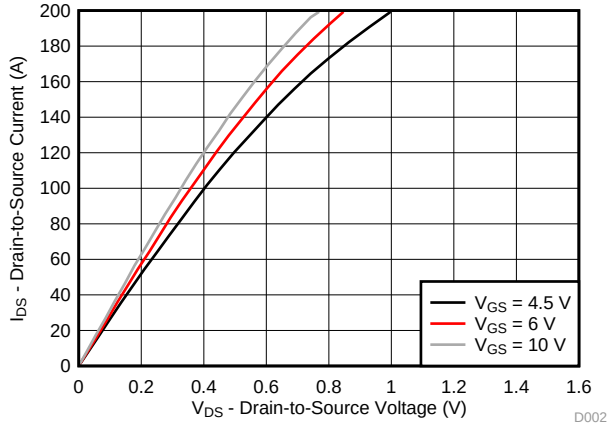


Figure 2. Saturation Characteristics

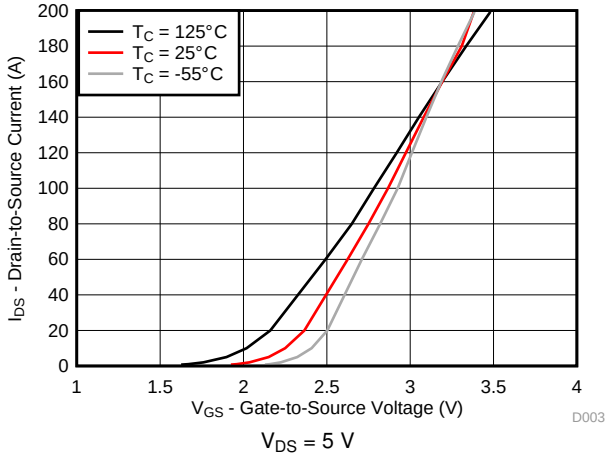


Figure 3. Transfer Characteristics

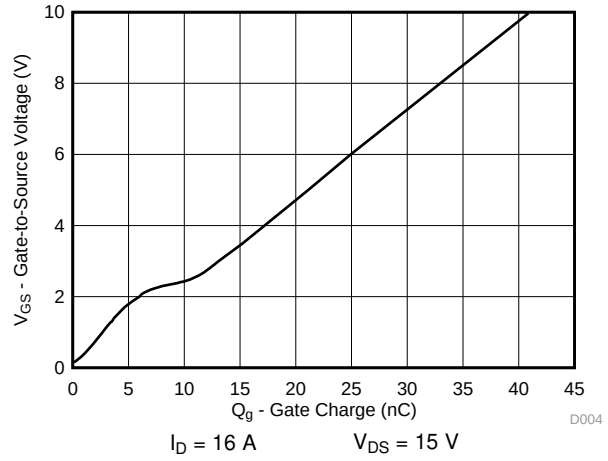


Figure 4. Gate Charge

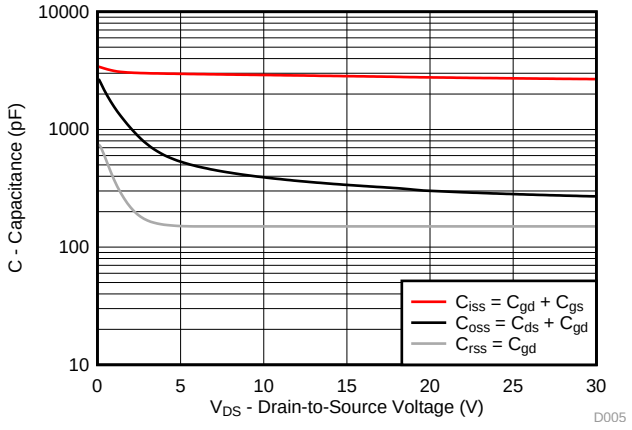


Figure 5. Capacitance

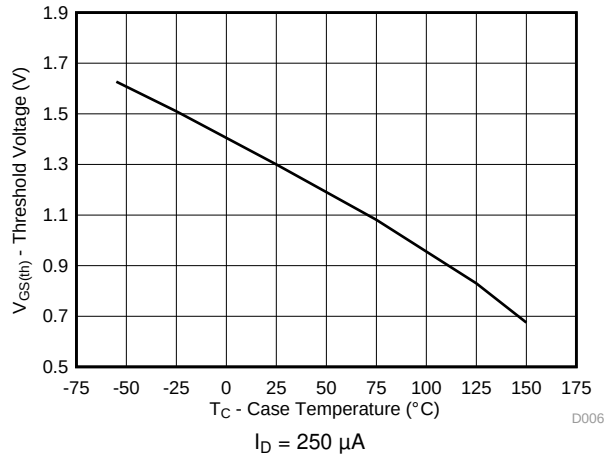


Figure 6. Threshold Voltage vs Temperature

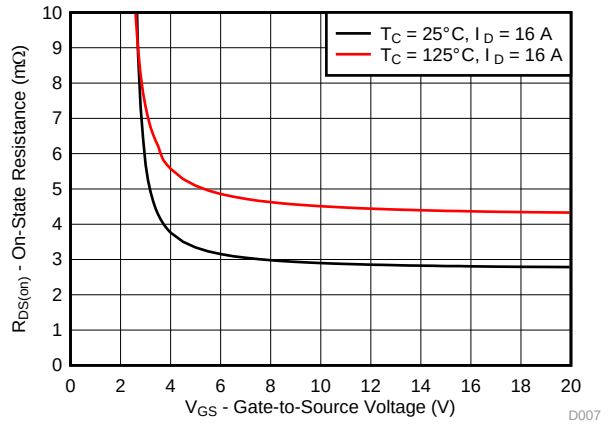


Figure 7. On-State Resistance vs Gate-to-Source Voltage

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Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)

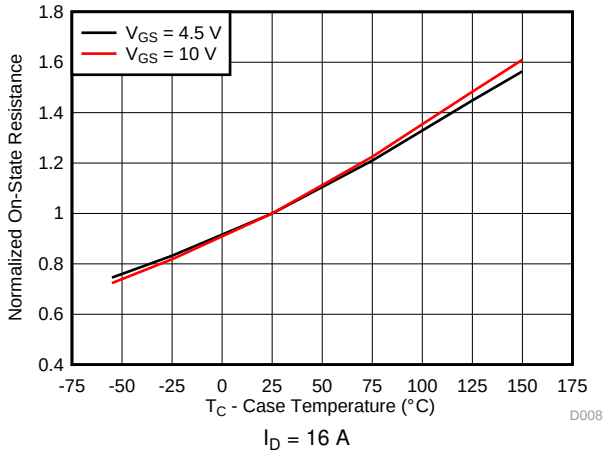


Figure 8. Normalized On-State Resistance vs Temperature

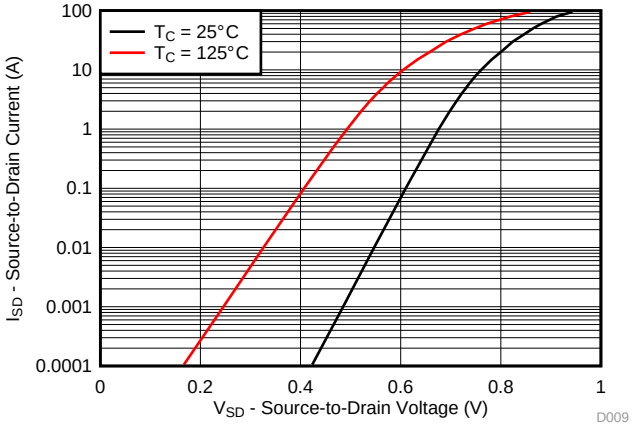


Figure 9. Typical Diode Forward Voltage

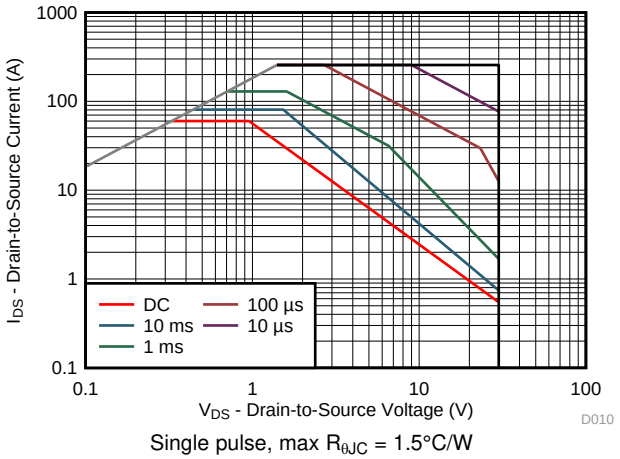


Figure 10. Maximum Safe Operating Area (SOA)

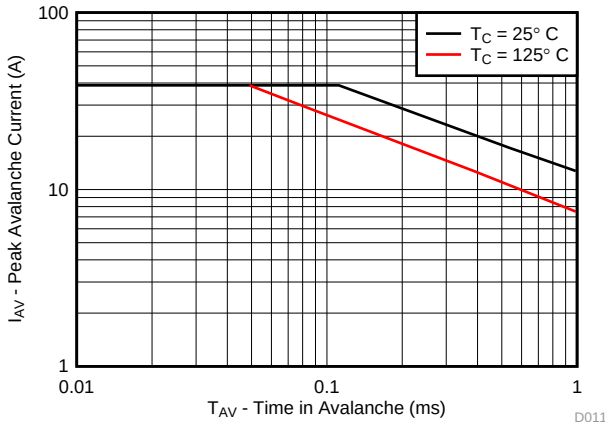


Figure 11. Single Pulse Unclamped Inductive Switching

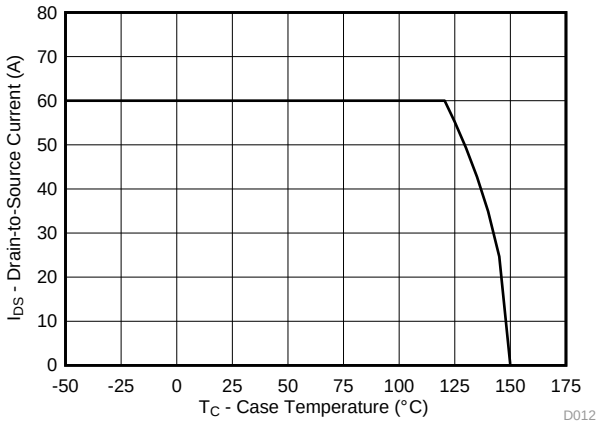


Figure 12. Maximum Drain Current vs Temperature

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6 Device and Documentation Support

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.3 Trademarks

NexFET, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

6.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.5 Glossary

SLYZ022 — *TI Glossary*.

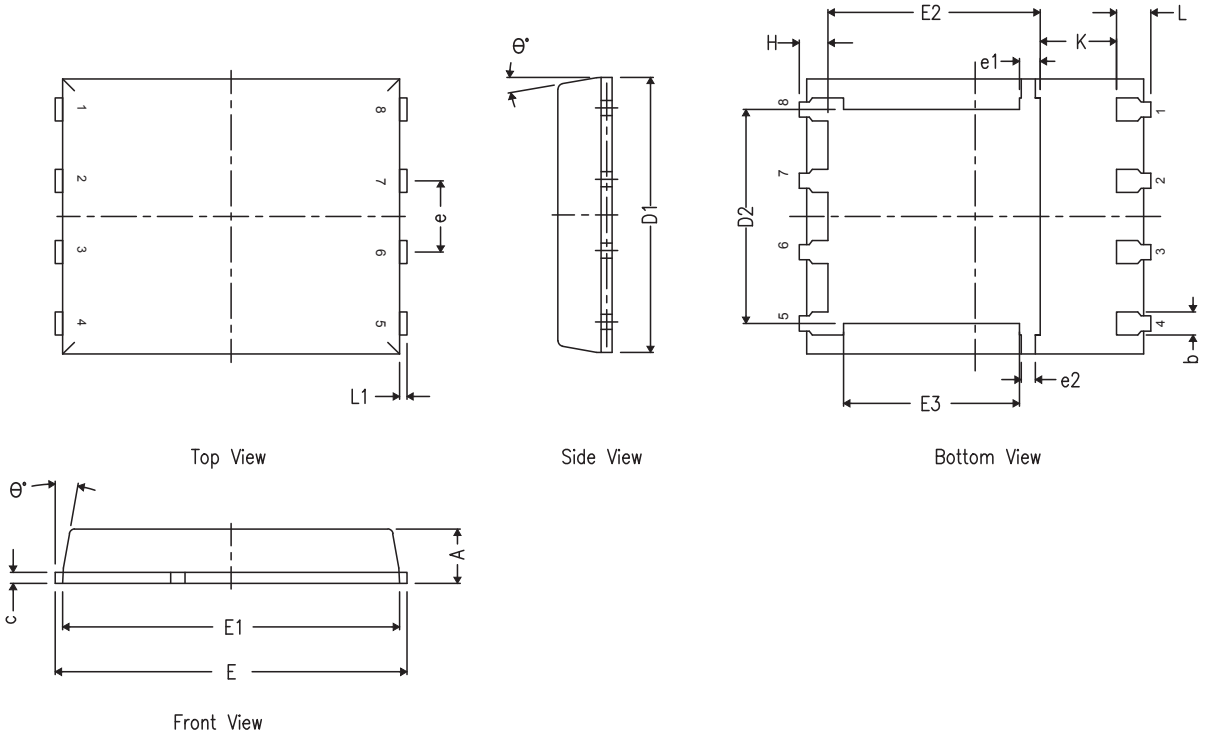
This glossary lists and explains terms, acronyms, and definitions.

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7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

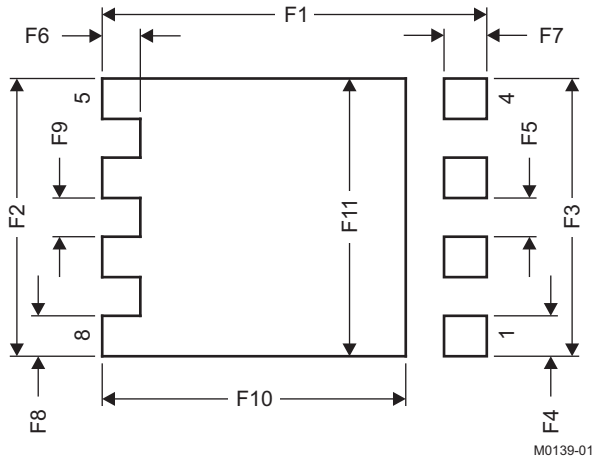
7.1 Q5A Package Dimensions



DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
b	0.33	0.41	0.51
c	0.20	0.25	0.34
D1	4.80	4.90	5.00
D2	3.61	3.81	4.02
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
E3	3.03	3.13	3.23
e	1.17	1.27	1.37
e1	0.27	0.37	0.47
e2	0.15	0.25	0.35
H	0.41	0.56	0.71
K	1.10	—	—
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
θ	0°	—	12°

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7.2 Recommended PCB Pattern

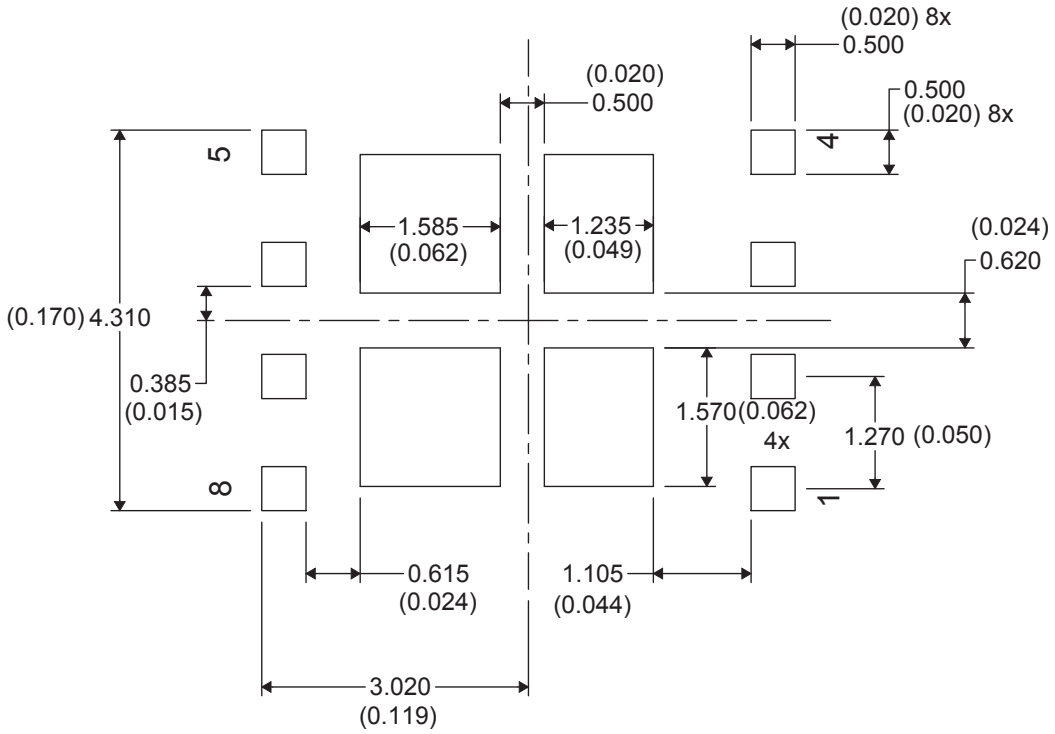


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
F1	6.205	6.305	0.244	0.248
F2	4.46	4.56	0.176	0.18
F3	4.46	4.56	0.176	0.18
F4	0.65	0.7	0.026	0.028
F5	0.62	0.67	0.024	0.026
F6	0.63	0.68	0.025	0.027
F7	0.7	0.8	0.028	0.031
F8	0.65	0.7	0.026	0.028
F9	0.62	0.67	0.024	0.026
F10	4.9	5	0.193	0.197
F11	4.46	4.56	0.176	0.18

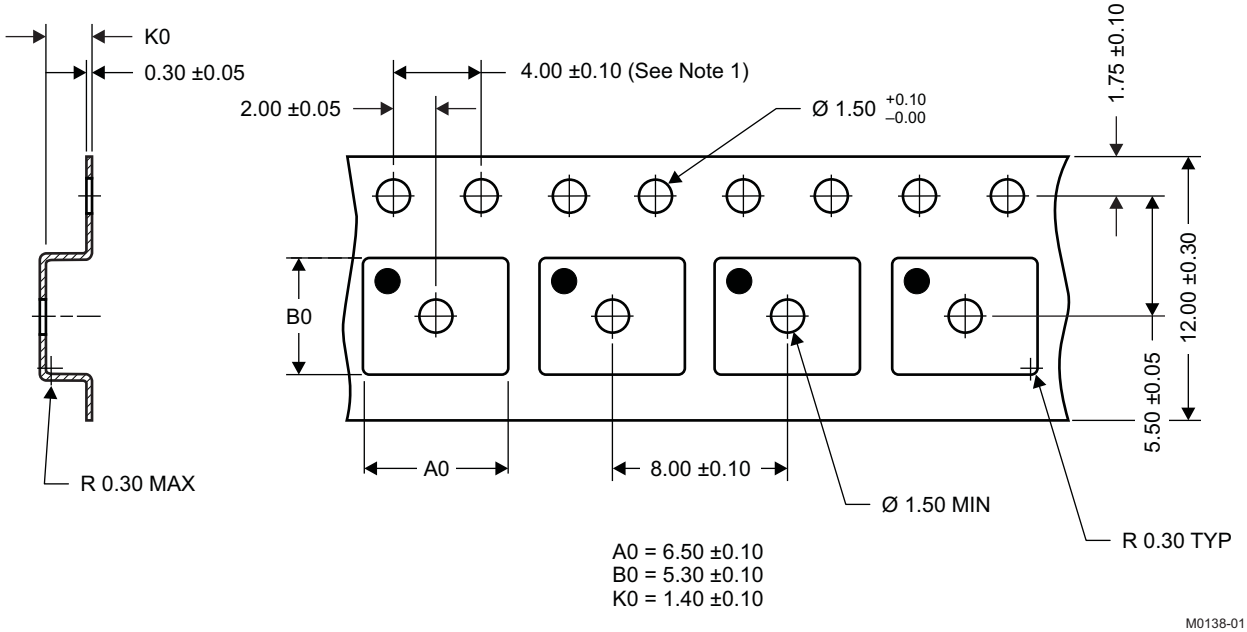
For recommended circuit layout for PCB designs, see application note SLPA005 – *Reducing Ringing Through PCB Layout Techniques*.

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7.3 Recommended Stencil Opening



7.4 Q5A Tape and Reel Information



Notes:

1. 10-sprocket hole-pitch cumulative tolerance ±0.2
2. Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm
3. Material: black static-dissipative polystyrene
4. All dimensions are in mm (unless otherwise specified)
5. A0 and B0 measured on a plane 0.3 mm above the bottom of the pocket

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD17581Q5A	Active	Production	VSONP (DQJ) | 8	2500 | LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD17581
CSD17581Q5A.B	Active	Production	VSONP (DQJ) | 8	2500 | LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD17581
CSD17581Q5AT	Active	Production	VSONP (DQJ) | 8	250 | SMALL T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD17581
CSD17581Q5AT.B	Active	Production	VSONP (DQJ) | 8	250 | SMALL T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD17581

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

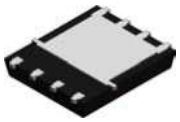
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

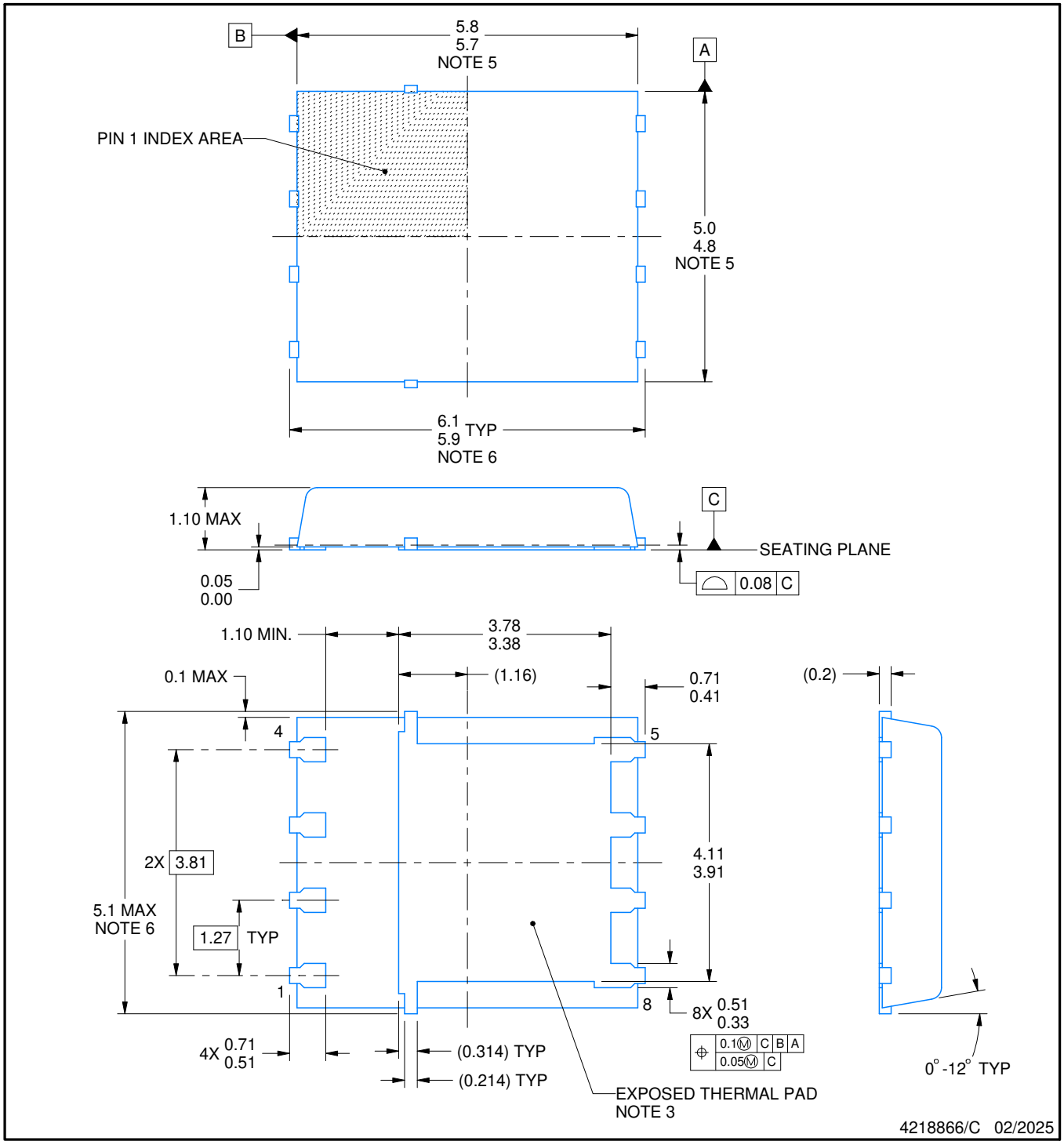


PACKAGE OUTLINE

DQJ0008A

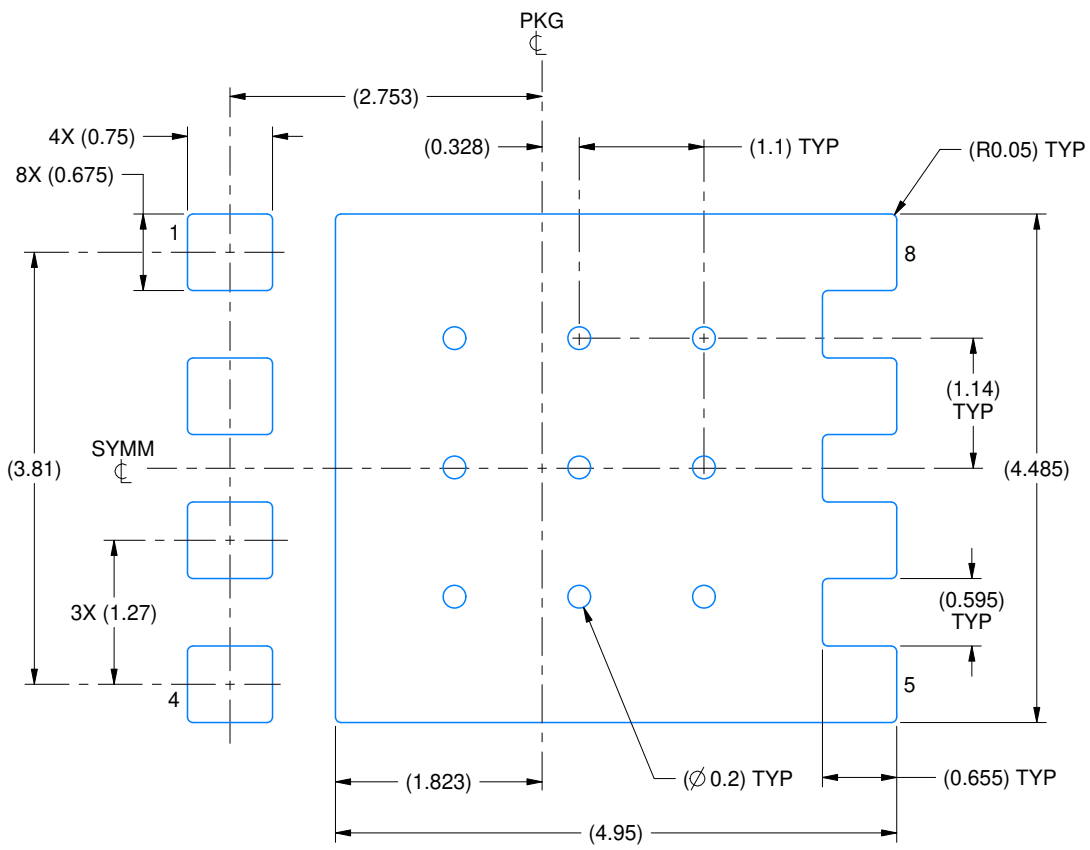
VSONP - 1.1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

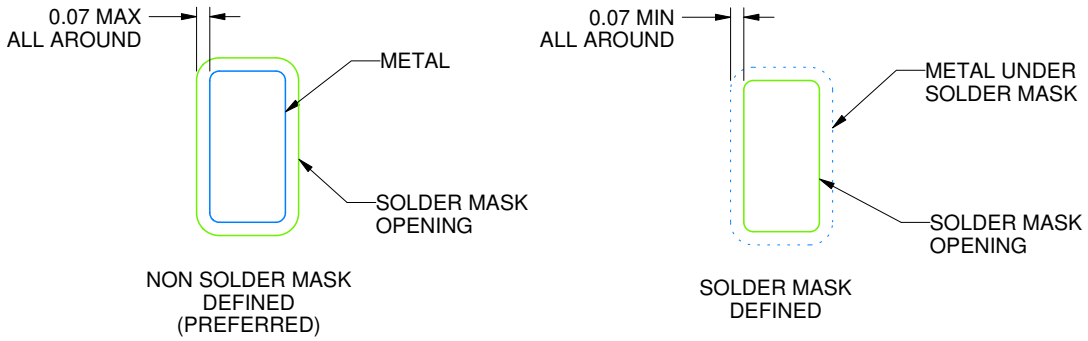


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Metalized features are supplier options and may not be on the package.
5. These dimensions do not include mold flash protrusions or gate burrs.
6. These dimensions include interterminal flash or protrusion. Interterminal flash or protrusion shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE: 15X

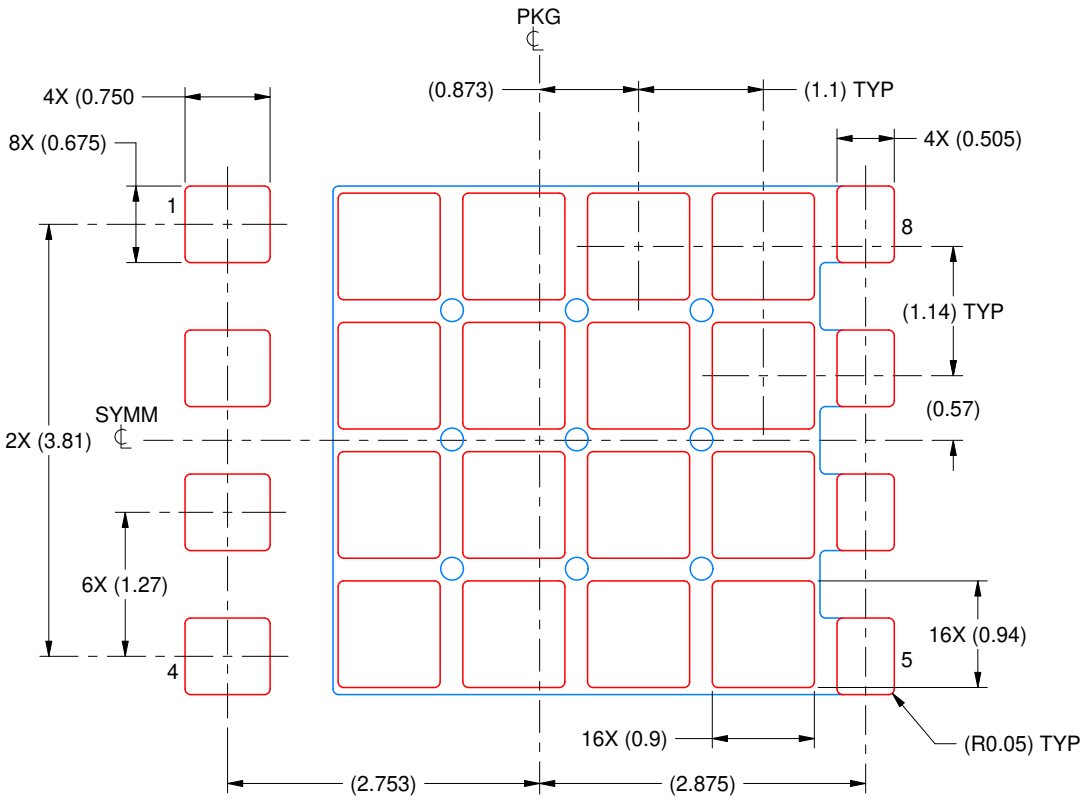


SOLDER MASK DETAILS

4218866/C 02/2025

NOTES: (continued)

7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
8. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD:
70% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE: 15X

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NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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