CSD18532NQ5B 60-V N-Channel NexFET™ Power MOSFET

1 Features

- Ultra-Low Q_g and Q_{gd}
- Low-Thermal Resistance
- Avalanche Rated
- Lead-Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 5-mm × 6-mm Plastic Package

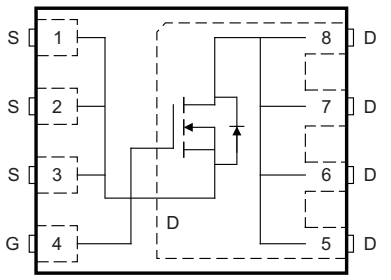
2 Applications

- DC-DC Conversion
- Secondary Side Synchronous Rectifier
- Isolated Converter Primary Side Switch
- Motor Control

3 Description

This 60-V, 2.7-mΩ, 5-mm × 6-mm SON NexFET™ power MOSFET has been designed to minimize losses in power conversion applications.

Top View



Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	60		V
Q_g	Gate Charge Total (10 V)	49		nC
Q_{gd}	Gate Charge Gate-to-Drain	7.9		nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = 6 V	3.5	mΩ
		V_{GS} = 10 V	2.7	
$V_{GS(th)}$	Threshold Voltage	2.8		V

Device Information

DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD18532NQ5B	2500	13-Inch Reel	SON 5.00-mm × 6.00-mm Plastic Package	Tape and Reel
CSD18532NQ5BT	250	7-Inch Reel		

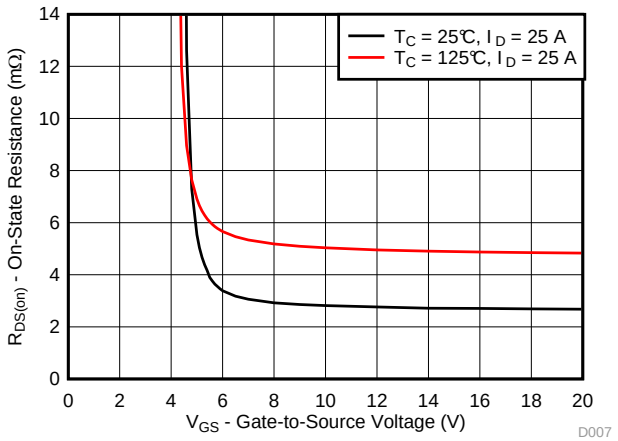
Absolute Maximum Ratings

T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	60	V
V_{GS}	Gate-to-Source Voltage	±20	V
I_D	Continuous Drain Current (Package Limited)	100	A
	Continuous Drain Current (Silicon Limited), T_C = 25°C	151	
	Continuous Drain Current(1)	21	
I_{DM}	Pulsed Drain Current(2)	400	A
P_D	Power Dissipation(1)	3.1	W
	Power Dissipation, T_C = 25°C	156	
T_J, T_{stg}	Operating Junction Temperature, Storage Temperature	–55 to 150	°C
E_{AS}	Avalanche Energy, Single Pulse I_D = 85 A, L = 0.1 mH, R_G = 25 Ω	360	mJ

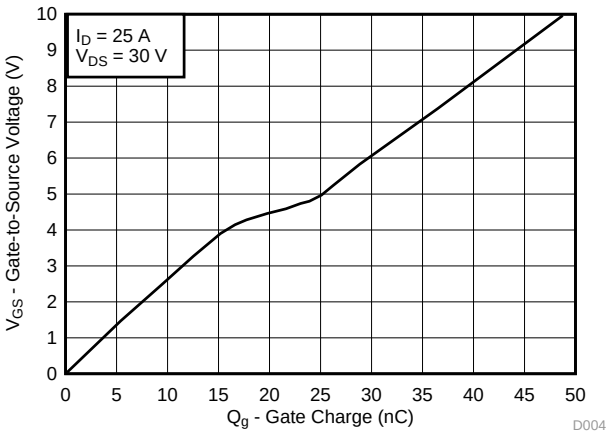
(1) Typical $R_{\theta JA}$ = 40°C/W on a 1-in², 2-oz Cu pad on a 0.06-in thick FR4 PCB.

(2) Max $R_{\theta JC}$ = 0.8°C/W, pulse duration ≤ 100 µs, duty cycle ≤ 1%.

$R_{DS(on)}$ vs V_{GS}



Gate Charge



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (May 2017) to Revision C **Page**

- Extended the V_{DS} on Figure 5 to 60 V ... 4

Changes from Revision A (December 2015) to Revision B **Page**

- Added *Receiving Notification of Documentation Updates* section. ... 7
- Changed the dimension between pads 3 and 4 from 0.028 inches: to 0.050 inches in the *Recommended PCB Pattern* section diagram. ... 9

Changes from Original (June 2014) to Revision A **Page**

- Added part number to title. ... 1
- Added 7" reel to *Ordering Information*. ... 1
- Updated pulsed current conditions. ... 1
- Added line for Power Dissipation, T_C = 25°C in *Absolute Maximum Ratings* table. ... 1
- Updated Figure 1 to show $R_{\theta JC}$ curves. ... 4
- Updated SOA in Figure 10 ... 6
- Added *Device and Documentation Support* section. ... 7
- Updated *Mechanical, Packaging, and Orderable Information* and mechanical drawings. ... 8

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5 Specifications

5.1 Electrical Characteristics

T_A = 25°C unless otherwise stated

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_D = 250 µA	60			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = 48 V			1	µA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2.4	2.8	3.4	V
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = 6 V, I_D = 25 A		3.5	4.4	mΩ
		V_{GS} = 10 V, I_D = 25 A		2.7	3.4	
g_{fs}	Transconductance	V_{DS} = 30 V, I_D = 25 A		140		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 30 V, f = 1 MHz		4100	5340	pF
C_{oss}	Output capacitance			495	644	pF
C_{rss}	Reverse transfer capacitance			16	21	pF
R_G	Series gate resistance			1.2	2.4	Ω
Q_g	Gate charge total (10 V)	V_{DS} = 30 V, I_D = 25 A		49	64	nC
Q_{gd}	Gate charge gate-to-drain			7.9		nC
Q_{gs}	Gate charge gate-to-source			16		nC
$Q_{g(th)}$	Gate charge at V_{th}			11		nC
Q_{oss}	Output charge	V_{DS} = 30 V, V_{GS} = 0 V		69		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = 30 V, V_{GS} = 10 V, I_{DS} = 25 A, R_G = 0 Ω		8.2		ns
t_r	Rise time			8.7		ns
$t_{d(off)}$	Turnoff delay time			20		ns
t_f	Fall time			2.7		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = 25 A, V_{GS} = 0 V		0.8	1	V
Q_{rr}	Reverse recovery charge	V_{DS} = 30 V, I_F = 25 A, di/dt = 300 A/µs		139		nC
t_{rr}	Reverse recovery time			64		ns

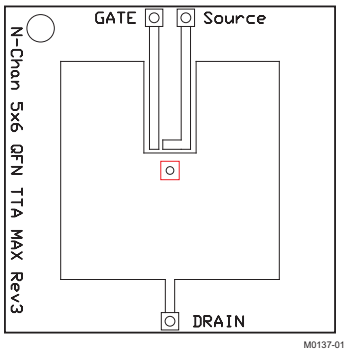
5.2 Thermal Information

T_A = 25°C unless otherwise stated

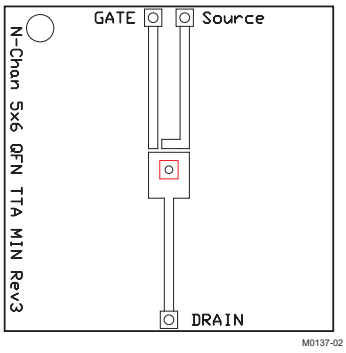
THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance (1)			0.8	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance (1) (2)			50	°C/W

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu pad on a 1.5-in × 1.5-in (3.81-cm × 3.81-cm), 0.06-in (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu.

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Max $R_{\theta JA}$ = 50°C/W when mounted on 1 in^2 (6.45 cm^2) of 2-oz (0.071-mm) thick Cu.



Max $R_{\theta JA}$ = 125°C/W when mounted on a minimum pad area of 2-oz. (0.071-mm) thick Cu.

5.3 Typical MOSFET Characteristics

T_A = 25°C unless otherwise stated

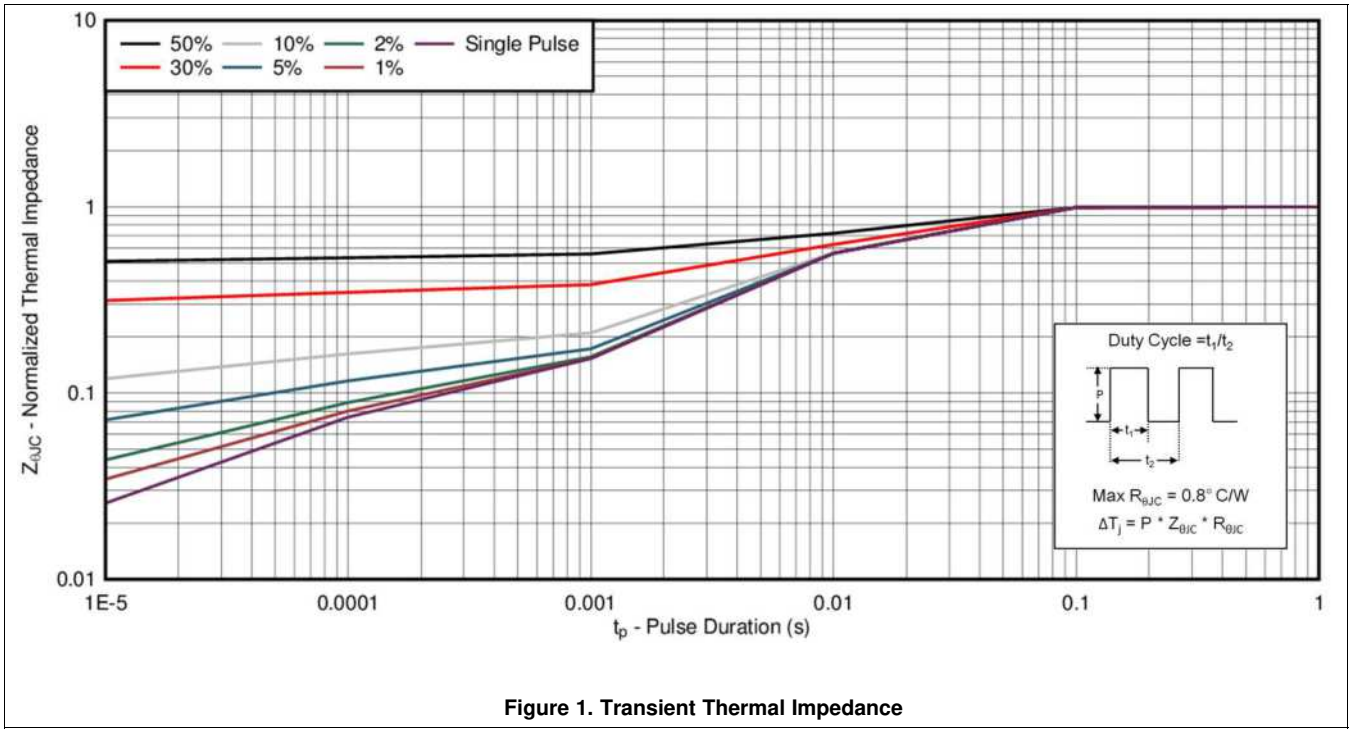


Figure 1. Transient Thermal Impedance

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Typical MOSFET Characteristics (continued)

T_A = 25°C unless otherwise stated

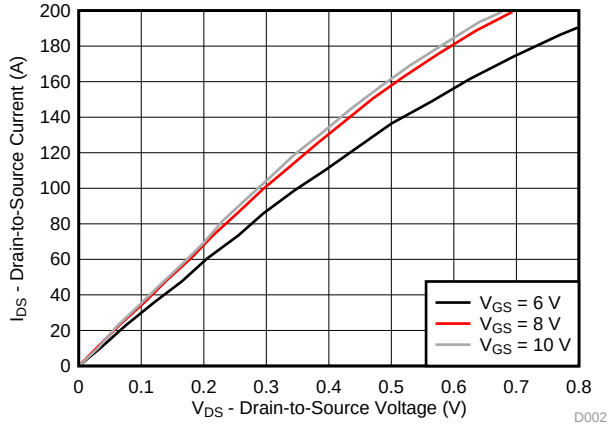


Figure 2. Saturation Characteristics

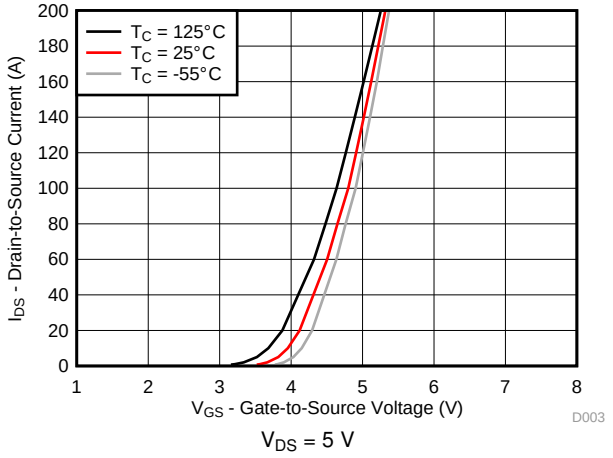


Figure 3. Transfer Characteristics

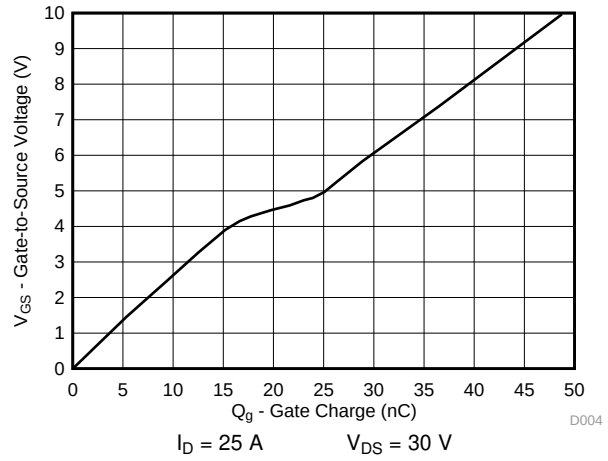


Figure 4. Gate Charge

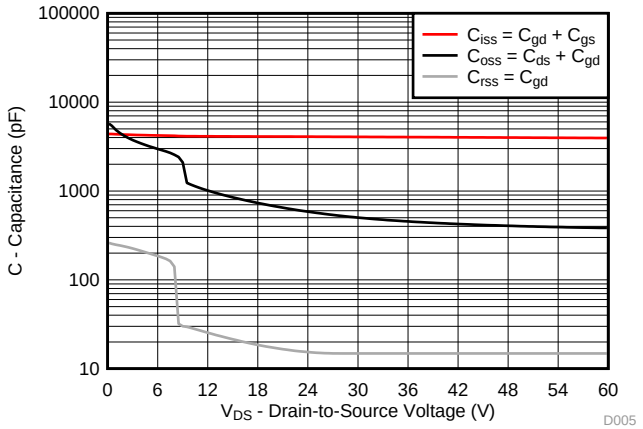


Figure 5. Capacitance

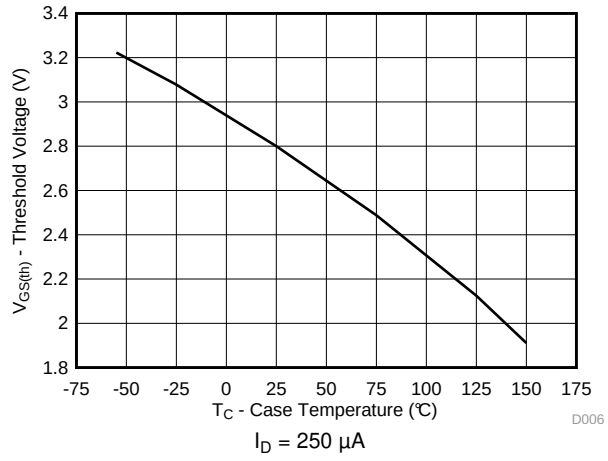


Figure 6. Threshold Voltage vs Temperature

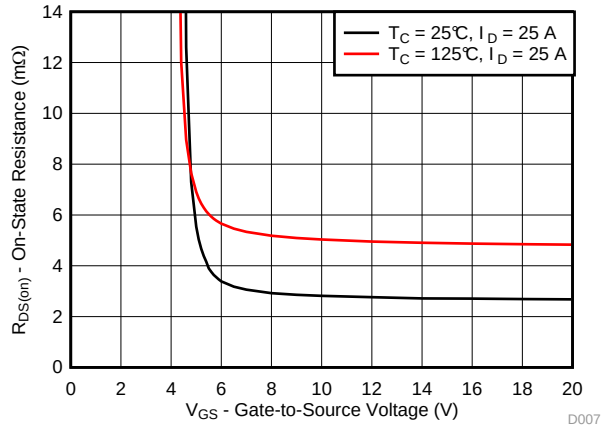
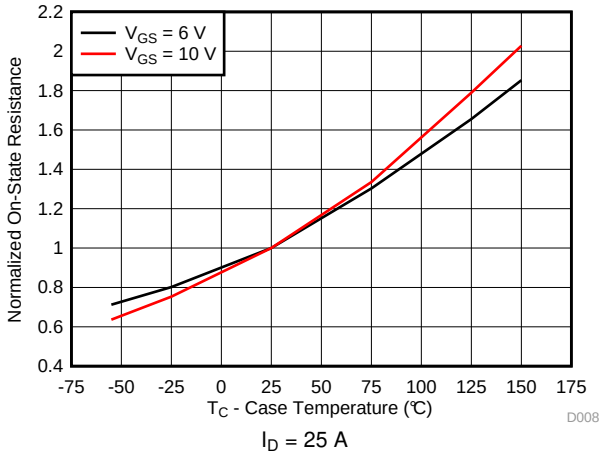


Figure 7. On-State Resistance vs Gate-to-Source Voltage

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Typical MOSFET Characteristics (continued)

T_A = 25°C unless otherwise stated



ID = 25 A

Figure 8. Normalized On-State Resistance vs Temperature

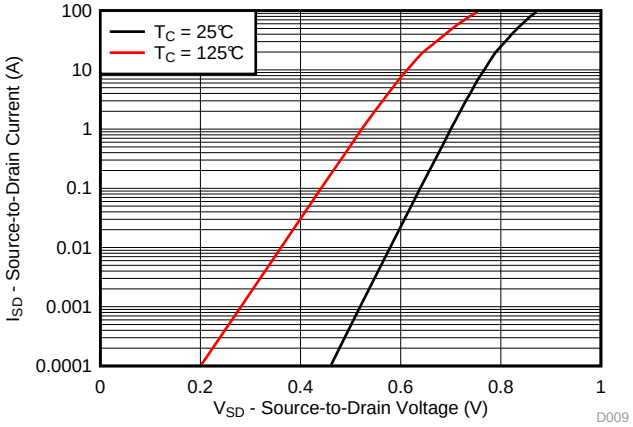
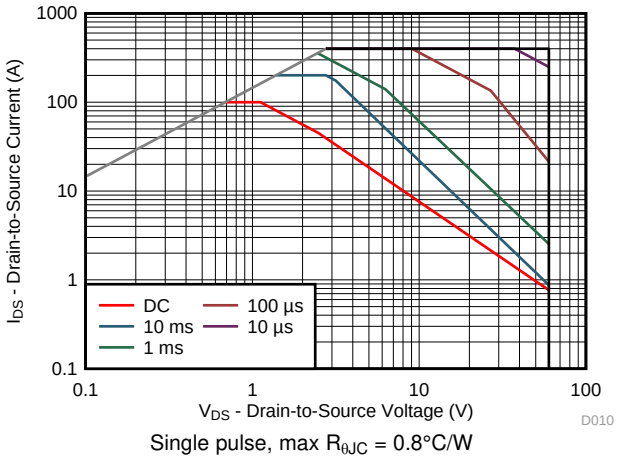


Figure 9. Typical Diode Forward Voltage



Single pulse, max $R_{\theta JC}$ = 0.8°C/W

Figure 10. Maximum Safe Operating Area

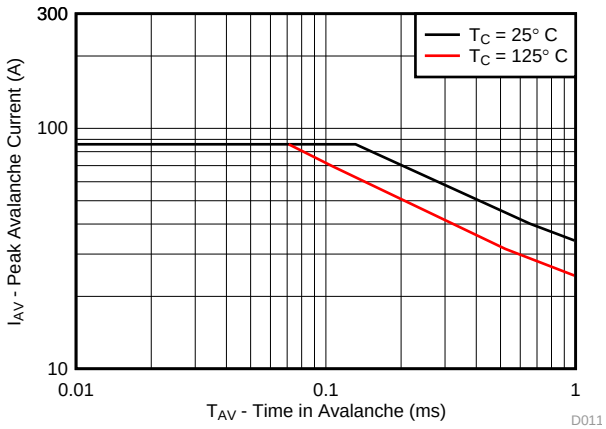


Figure 11. Single Pulse Unclamped Inductive Switching

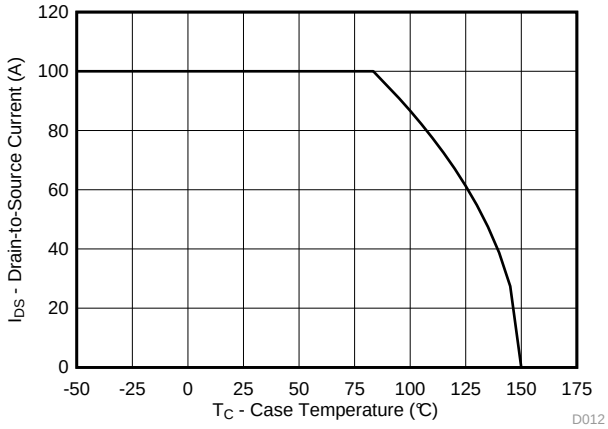


Figure 12. Maximum Drain Current vs Temperature

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6 Device and Documentation Support

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.3 Trademarks

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6.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.5 Glossary

SLYZ022 — *TI Glossary*.

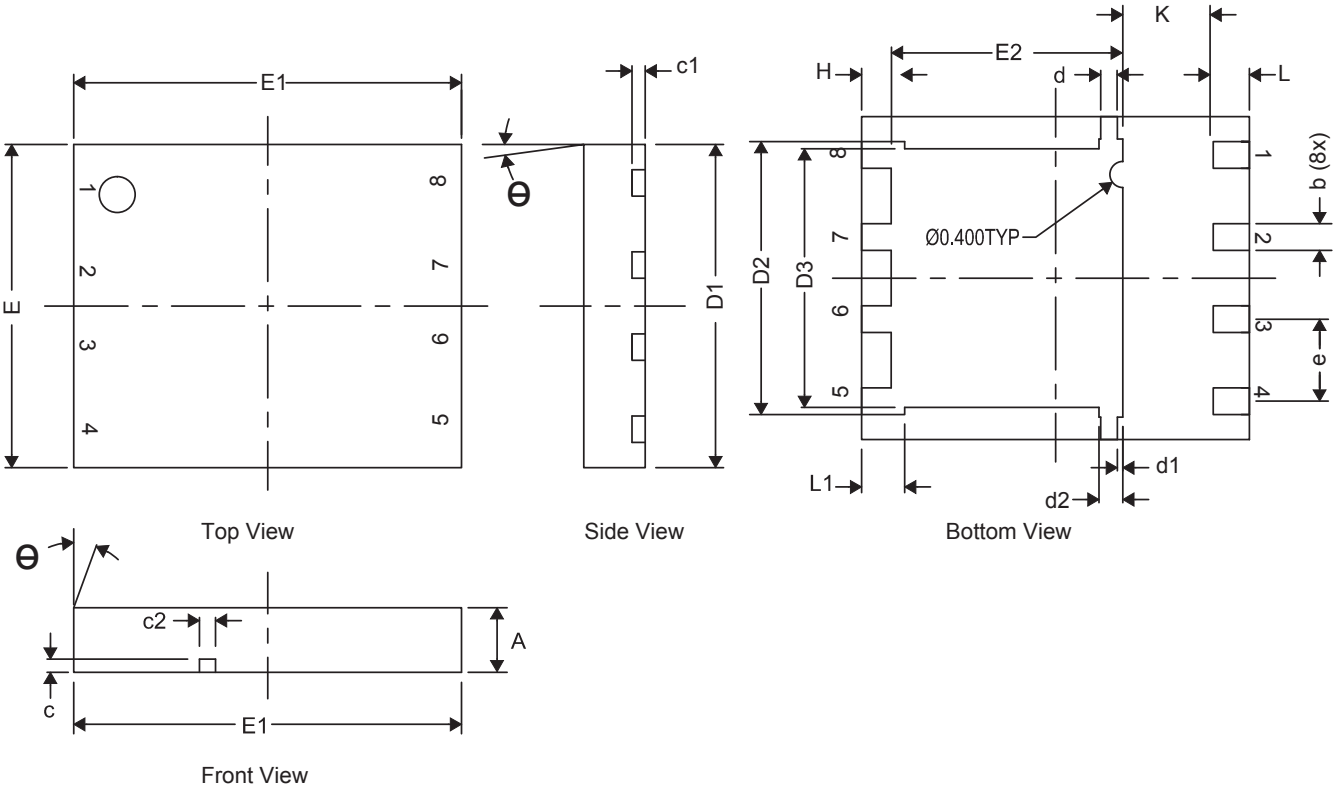
This glossary lists and explains terms, acronyms, and definitions.

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7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

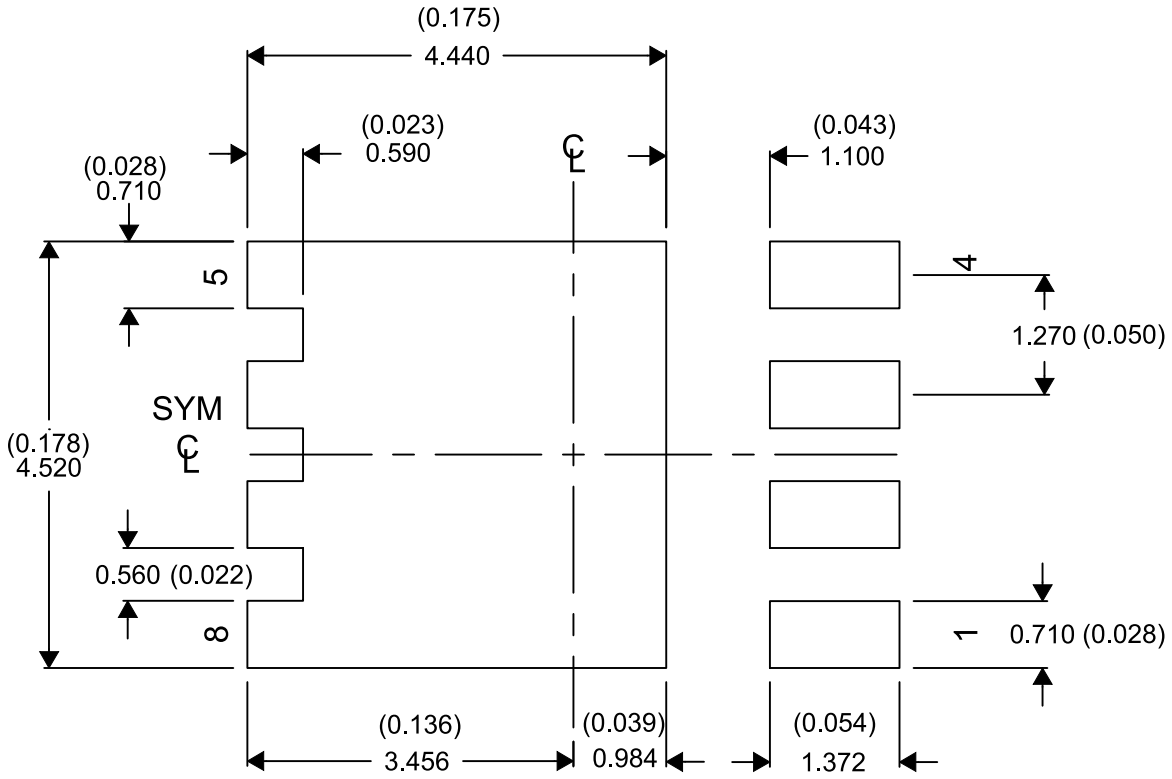
7.1 Q5B Package Dimensions



DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.80	1.00	1.05
b	0.36	0.41	0.46
c	0.15	0.20	0.25
c1	0.15	0.20	0.25
c2	0.20	0.25	0.30
D1	4.90	5.00	5.10
D2	4.12	4.22	4.32
d	0.20	0.25	0.30
E	4.90	5.00	5.10
E1	5.90	6.00	6.10
E2	3.48	3.58	3.68
e		1.27 TYP	
L	0.46	0.56	0.66
θ	0°	—	—
K		1.40 TYP	

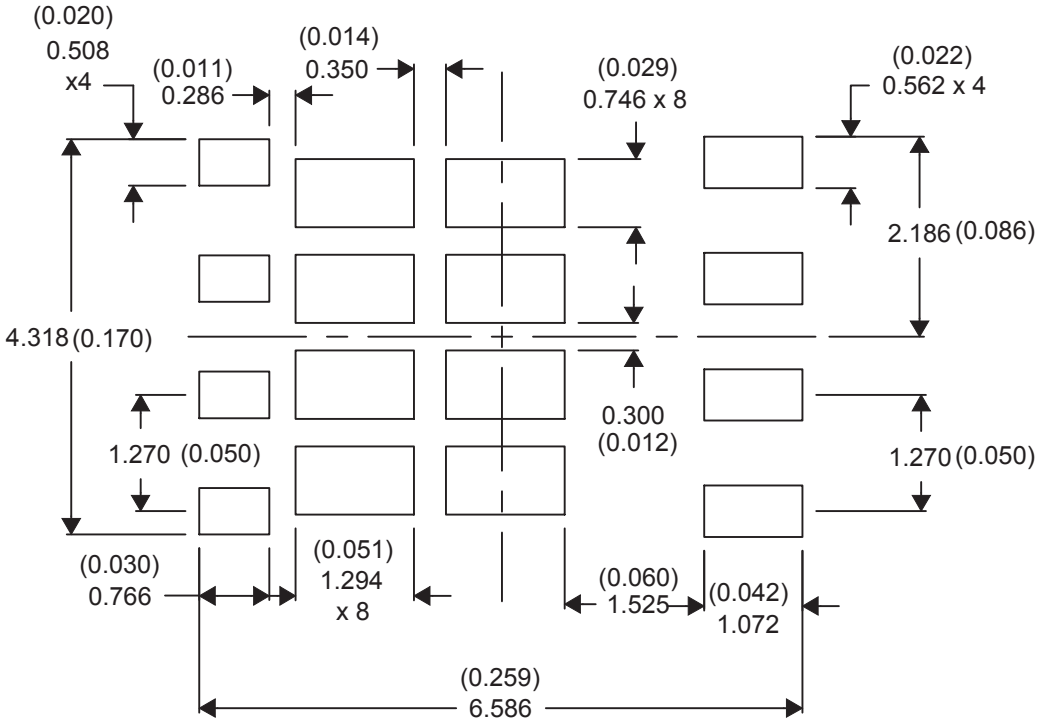
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7.2 Recommended PCB Pattern

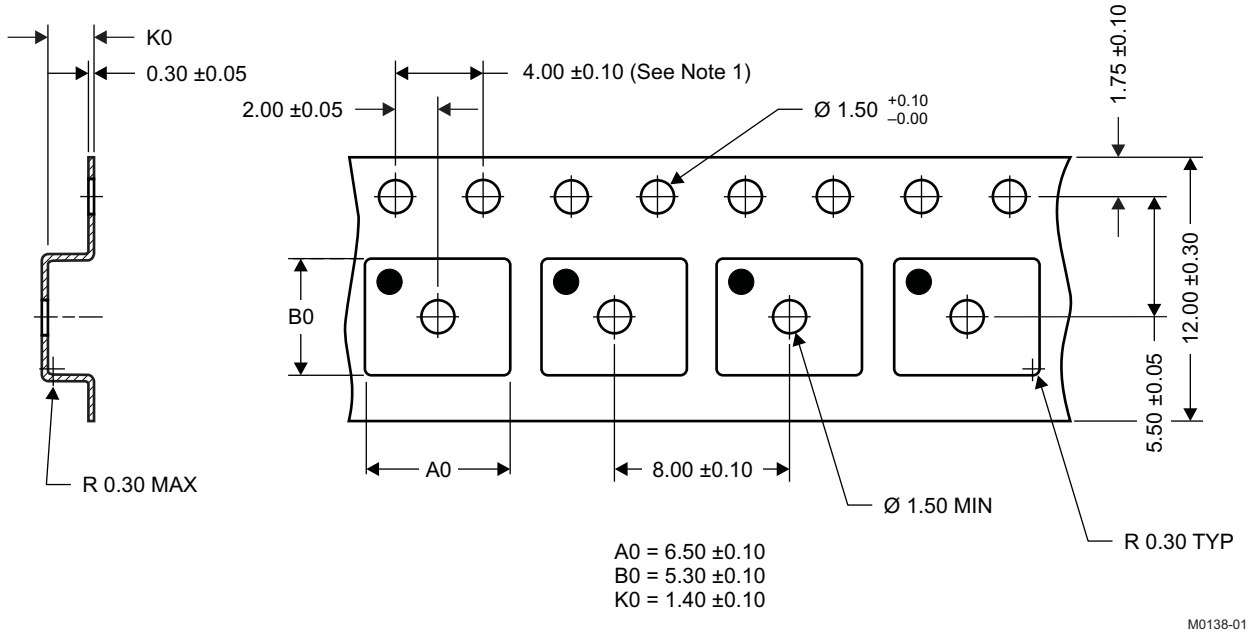


For recommended circuit layout for PCB designs, see *Reducing Ringing Through PCB Layout Techniques* (SLPA005).

7.3 Recommended Stencil Pattern



7.4 Q5B Tape and Reel Information



Notes:

1. 10-sprocket hole-pitch cumulative tolerance ±0.2.
2. Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm.
3. Material: black static-dissipative polystyrene.
4. All dimensions are in mm (unless otherwise specified).
5. A0 and B0 measured on a plane 0.3 mm above the bottom of the pocket.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD18532NQ5B	Active	Production	VSON-CLIP (DNK) | 8	2500 | LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	18532N
CSD18532NQ5B.B	Active	Production	VSON-CLIP (DNK) | 8	2500 | LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	18532N
CSD18532NQ5BT	Active	Production	VSON-CLIP (DNK) | 8	250 | SMALL T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	18532N
CSD18532NQ5BT.B	Active	Production	VSON-CLIP (DNK) | 8	250 | SMALL T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	18532N

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

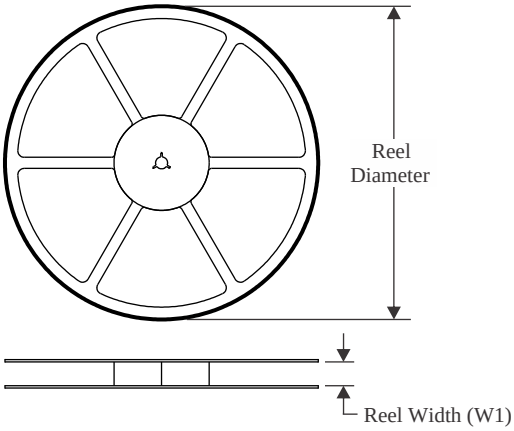
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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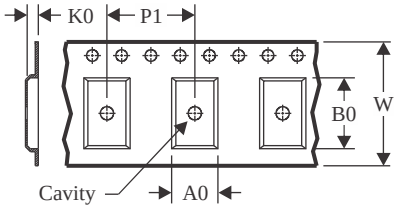
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

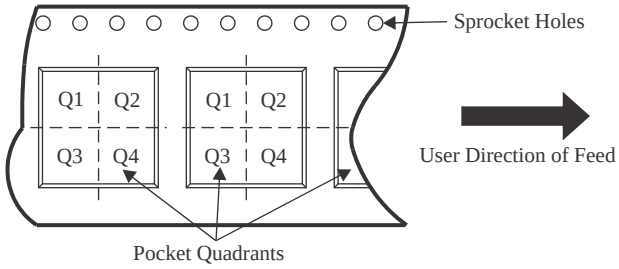


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

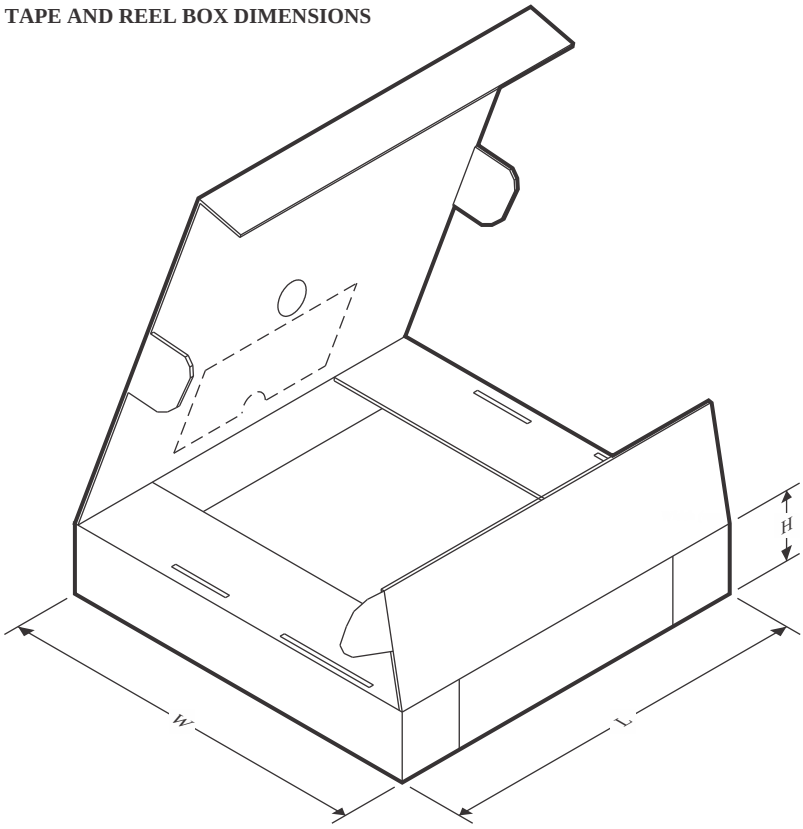
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD18532NQ5BT	VSON-CLIP	DNK	8	250	330.0	12.4	6.3	5.3	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD18532NQ5BT	VSON-CLIP	DNK	8	250	335.0	335.0	32.0

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