CSD19531KCS 100V N-Channel NexFET™ Power MOSFET

1 Features

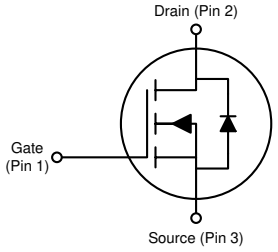
- Ultra-low Q_g and Q_{gd}
- Low-thermal resistance
- Avalanche rated
- Lead-free terminal plating
- RoHS compliant
- Halogen free
- TO-220 plastic package

2 Applications

- Secondary side synchronous rectifier
- Hot swap telecom
- Motor control

3 Description

This 100V, 6.4mΩ, TO-220 NexFET™ power MOSFET is designed to minimize losses in power conversion applications.





Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	100		V
Q_g	Gate Charge Total (10V)	37		nC
Q_{gd}	Gate Charge Gate-to-Drain	7.5		nC
$R_{DS(on)}$	Drain-to-Source On Resistance	V_{GS} = 6V	7.3	mΩ
		V_{GS} = 10V	6.4	
$V_{GS(th)}$	Threshold Voltage	2.7		V

Device Information(1)

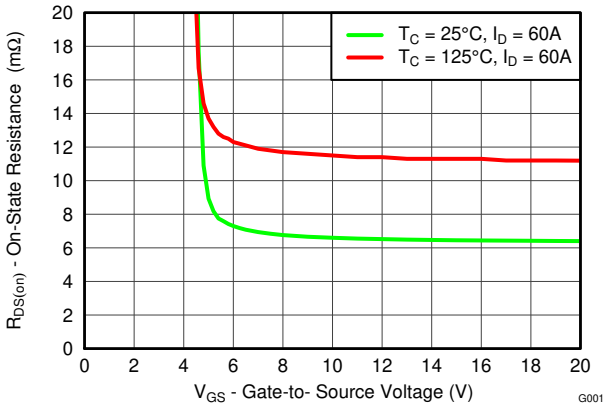
DEVICE	PACKAGE	MEDIA	QTY	SHIP
CSD19531KCS	TO-220 Plastic Package	Tube	50	Tube

(1) For all available packages, see the orderable addendum at the end of the data sheet.

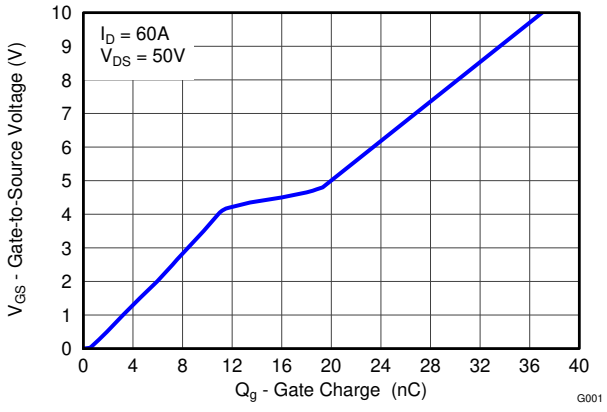
Absolute Maximum Ratings

T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	100	V
V_{GS}	Gate-to-Source Voltage	±20	V
I_D	Continuous Drain Current (Package Limited)	100	A
	Continuous Drain Current (Silicon Limited), T_C = 25°C	110	
	Continuous Drain Current (Silicon Limited), T_C = 100°C	78	
I_{DM}	Pulsed Drain Current(1)	285	A
P_D	Power Dissipation	214	W
T_J, T_{stg}	Operating Junction, Storage Temperature	–55 to 175	°C
E_{AS}	Avalanche Energy, Single Pulse I_D = 60A, L = 0.1mH, R_G = 25Ω	180	mJ

(1) Max $R_{\theta JC}$ = 0.7° C/W, pulse duration ≤ 100µs, duty cycle ≤ 1%.



$R_{DS(on)}$ vs V_{GS}



Gate Charge

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Specifications

4.1 Electrical Characteristics

T_A = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0V, I_D = 250µA	100			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0V, V_{DS} = 80V			1	µA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0V, V_{GS} = 20V			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_D = 250µA	2.2	2.7	3.3	V
$R_{DS(on)}$	Drain-to-source on resistance	V_{GS} = 6V, I_D = 60A		7.3	8.8	mΩ
		V_{GS} = 10V, I_D = 60A		6.4	7.7	
g_{fs}	Transconductance	V_{DS} = 10V, I_D = 60A		137		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0V, V_{DS} = 50V, f = 1MHz		2980	3870	pF
C_{oss}	Output capacitance			560	728	pF
C_{rss}	Reverse transfer capacitance			13	17	pF
R_G	Series gate resistance			1.3	2.6	Ω
Q_g	Gate charge total (10V)	V_{DS} = 50V, I_D = 60A		38	49	nC
Q_{gd}	Gate charge gate-to-drain			7.5		nC
Q_{gs}	Gate charge gate-to-source			11.9		nC
$Q_{g(th)}$	Gate charge at V_{th}			7.3		nC
Q_{oss}	Output charge	V_{DS} = 50V, V_{GS} = 0V		98		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = 50V, V_{GS} = 10V, I_{DS} = 60A, R_G = 0Ω		8.4		ns
t_r	Rise Time			7.2		ns
$t_{d(off)}$	Turnoff delay time			16		ns
t_f	Fall time			4.1		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = 60A, V_{GS} = 0V		0.9	1	V
Q_{rr}	Reverse recovery charge	V_{DS}= 50V, I_F = 60A, di/dt = 300A/µs		270		nC
t_{rr}	Reverse recovery time			83		ns

4.2 Thermal Information

T_A = 25°C (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance			0.7	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance			62	°C/W

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4.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise stated)

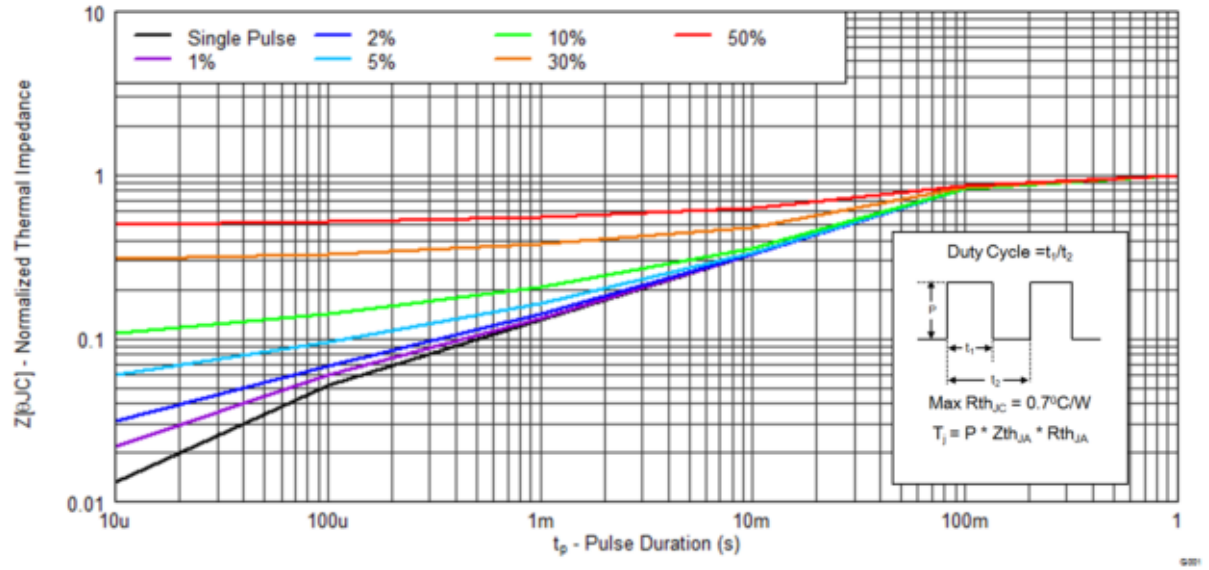

Figure 4-1. Transient Thermal Impedance

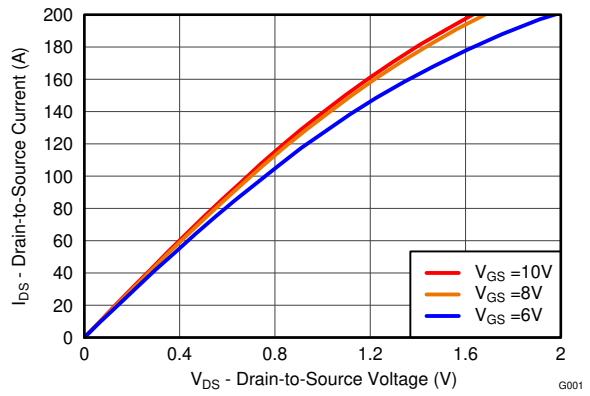

Figure 4-2. Saturation Characteristics

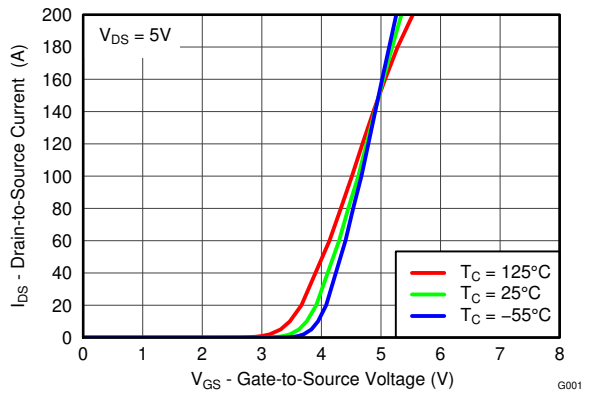

Figure 4-3. Transfer Characteristics

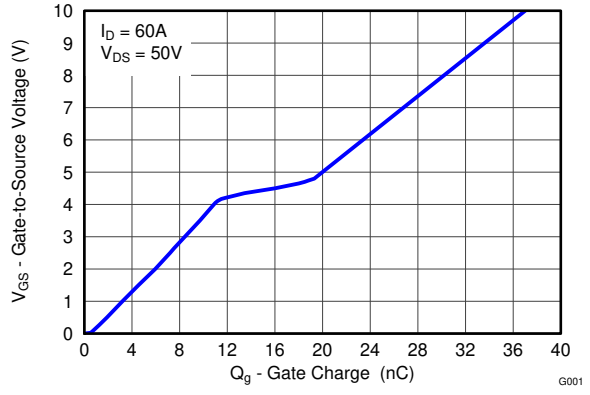

Figure 4-4. Gate Charge

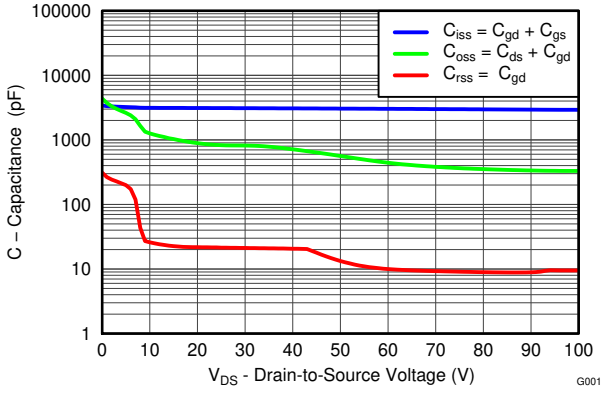

Figure 4-5. Capacitance

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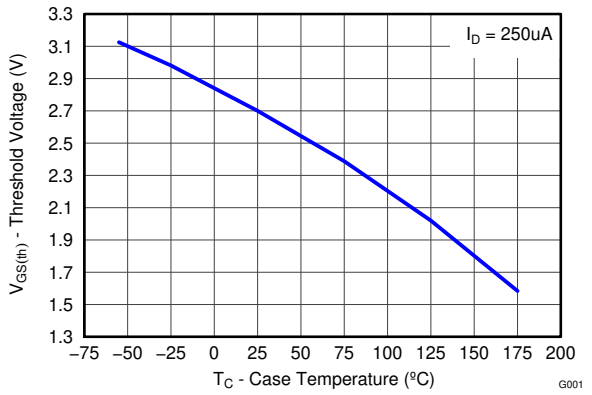

Figure 4-6. Threshold Voltage vs Temperature

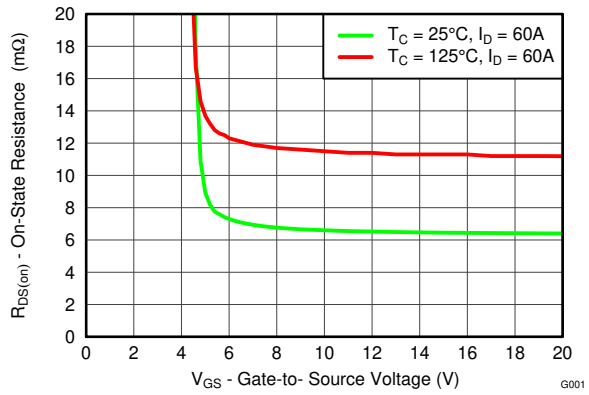

Figure 4-7. On-State Resistance vs Gate-to-Source Voltage

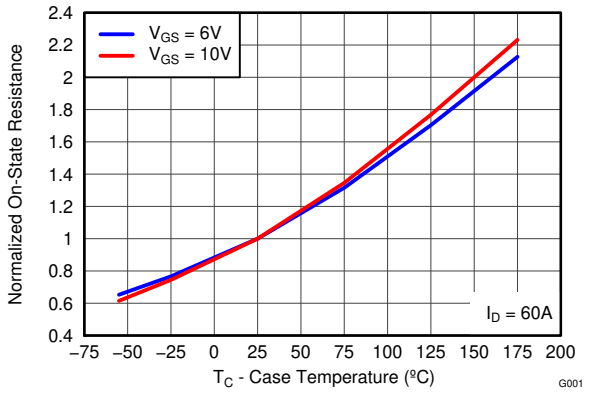

Figure 4-8. Normalized On-State Resistance vs Temperature

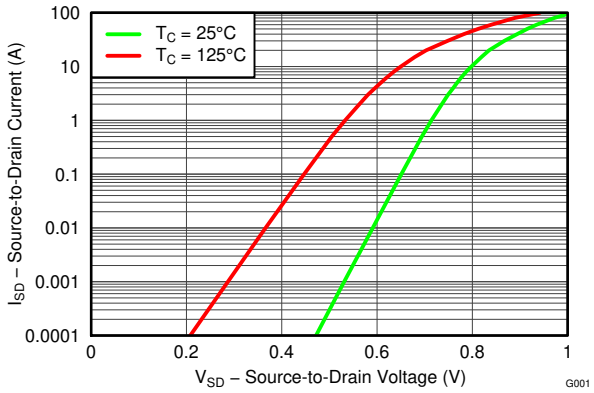

Figure 4-9. Typical Diode Forward Voltage

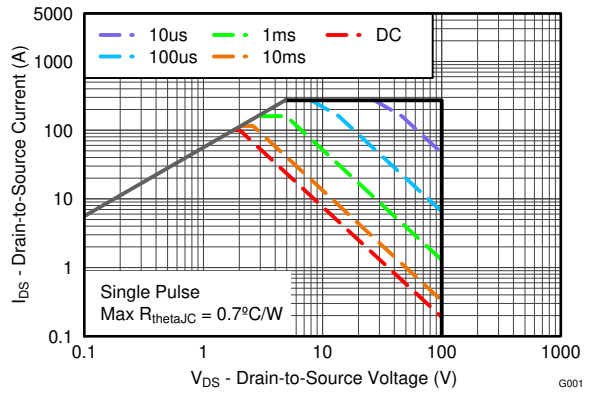

Figure 4-10. Maximum Safe Operating Area

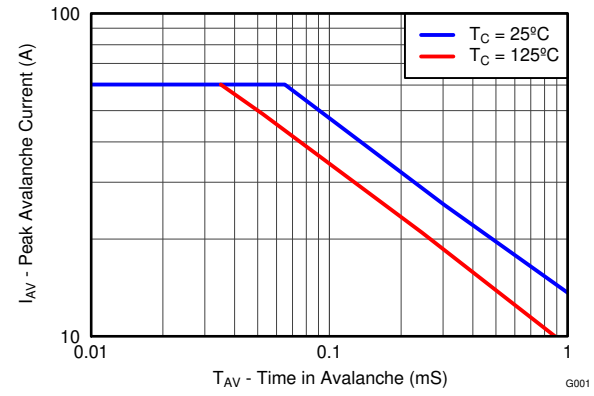

Figure 4-11. Single Pulse Unclamped Inductive Switching

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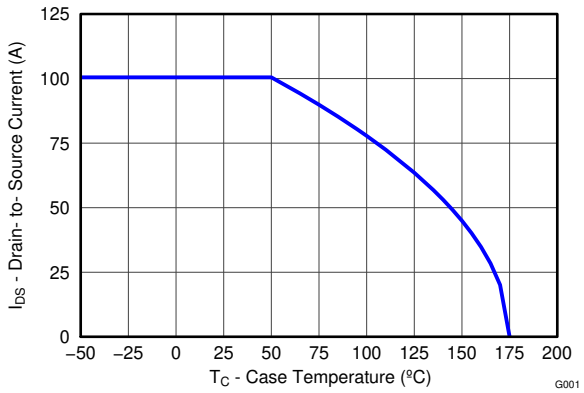

Figure 4-12. Maximum Drain Current vs Temperature

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5 Device and Documentation Support

5.1 Third-Party Products Disclaimer

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5.2 Documentation Support

5.2.1 Related Documentation

5.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

5.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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5.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

5.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

6 Revision History

Changes from Revision C (March 2017) to Revision D (May 2024)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1

Changes from Revision B (June 2014) to Revision C (March 2017)	Page

Changes from Revision A (May 2014) to Revision B (June 2014)	Page
• Added value for max Q_g	3

Changes from Revision * (September 2013) to Revision A (May 2014) **Page**

- Updated the silicon limited currents to reflect increase in device operating temperature range 1
- Increased pulsed current to reflect new conditions 1
- Increased max power dissipation to reflect new conditions 1
- Increased operating and junction temperature range to 175°C 1
- Updated the pulsed drain current conditions..... 1
- Changed Figure 4-1 from a normalized $R_{\theta JA}$ curve to a normalized $R_{\theta JC}$ curve 4
- Updated Figure 4-6 to reflect increase in device operating temperature range 4
- Updated Figure 4-8 to reflect increase in device operating temperature range 4
- Updated Figure 4-10 to reflect measured SOA data 4
- Updated Figure 4-12 to reflect increase in device operating temperature range 4

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7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD19531KCS	Active	Production	TO-220 (KCS) | 3	50 | TUBE	ROHS Exempt	SN	N/A for Pkg Type	-55 to 175	CSD19531KCS
CSD19531KCS.B	Active	Production	TO-220 (KCS) | 3	50 | TUBE	ROHS Exempt	SN	N/A for Pkg Type	-55 to 175	CSD19531KCS

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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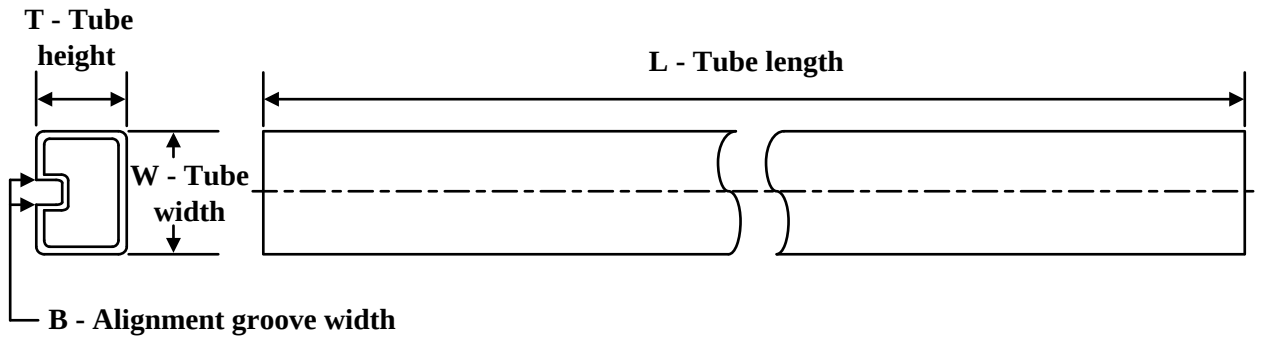
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CSD19531KCS	KCS	TO-220	3	50	532	34.1	700	9.6
CSD19531KCS.B	KCS	TO-220	3	50	532	34.1	700	9.6

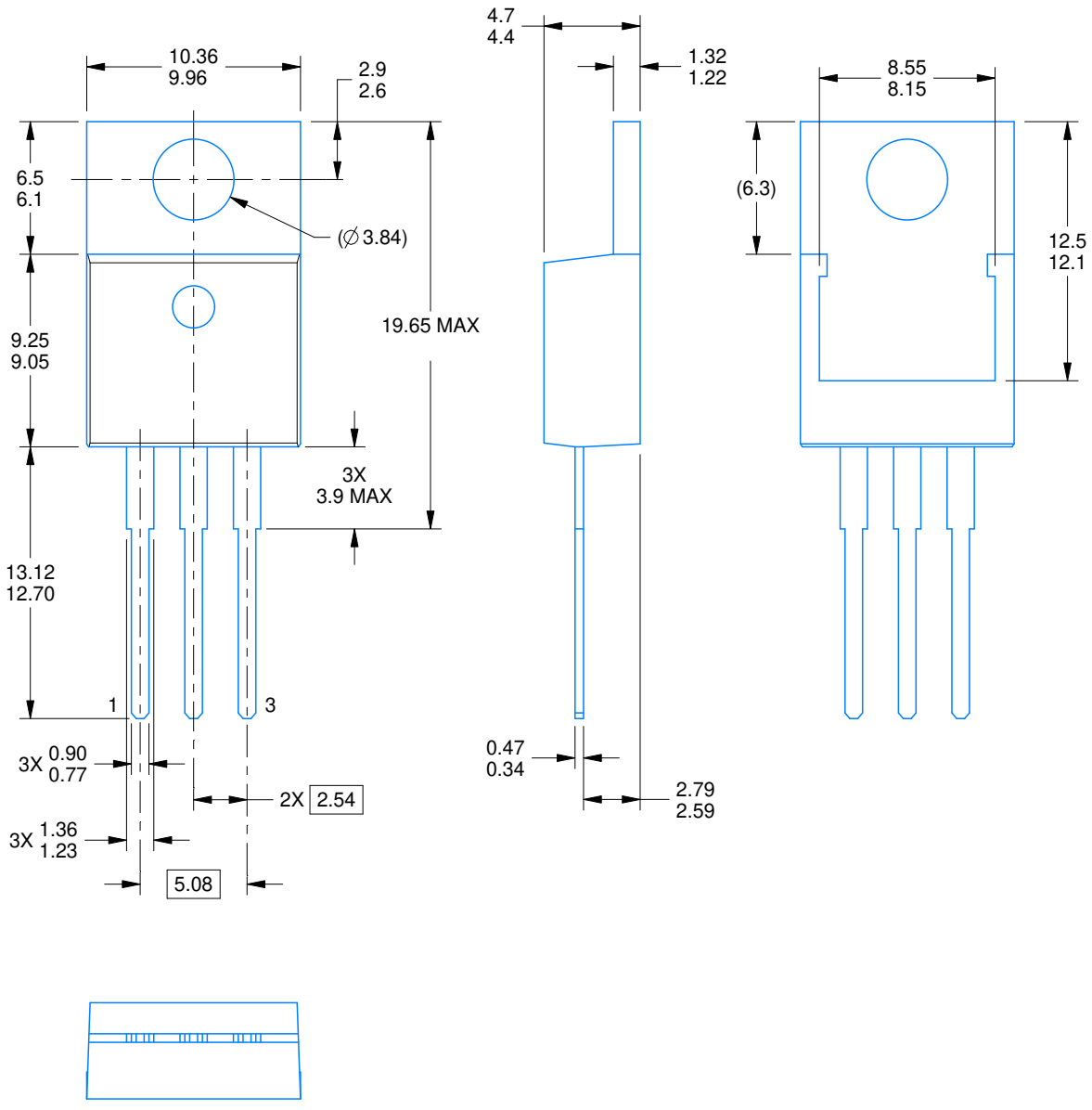


PACKAGE OUTLINE

KCS0003B

TO-220 - 19.65 mm max height

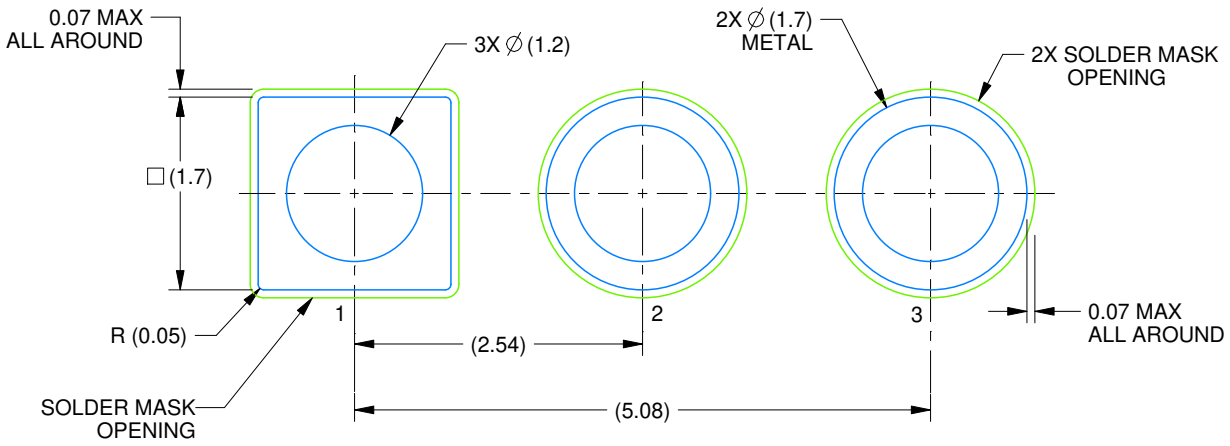
TO-220



4222214/B 08/2018

NOTES:

1. Dimensions are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-220.



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE:15X

4222214/B 08/2018

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