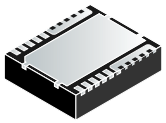
CSD95372BQ5MC Synchronous Buck NexFET™ Smart Power Stage

1 Features

- 60-A Continuous Operating Current Capability
- 93.4% System Efficiency at 30 A
- Low Power Loss of 2.8 W at 30 A
- High-Frequency Operation (up to 1.25 MHz)
- Diode Emulation Mode With FCCM
- Temperature-Compensated Bidirectional Current Sense
- Analog Temperature Output (600 mV at 0°C)
- Fault Monitoring
  - High-Side Short, Overcurrent, and Overtemperature Protection
- 3.3-V and 5-V PWM Signal Compatible
- Tri-State PWM Input
- Integrated Bootstrap Diode
- Optimized Deadtime for Shoot-Through Protection
- High-Density SON 5 × 6 mm Footprint
- Ultra-Low Inductance Package
- System-Optimized PCB Footprint
- DualCool™ Packaging
- RoHS Compliant – Lead-Free Terminal Plating
- Halogen-Free



2 Applications

- Multiphase Synchronous Buck Converters
  - High-Frequency Applications
  - High-Current, Low Duty-Cycle Applications
- POL DC-DC Converters
- Memory and Graphic Cards
- Desktop and Server VR11.x / VR12.x V-Core and Memory Synchronous Converters

3 Description

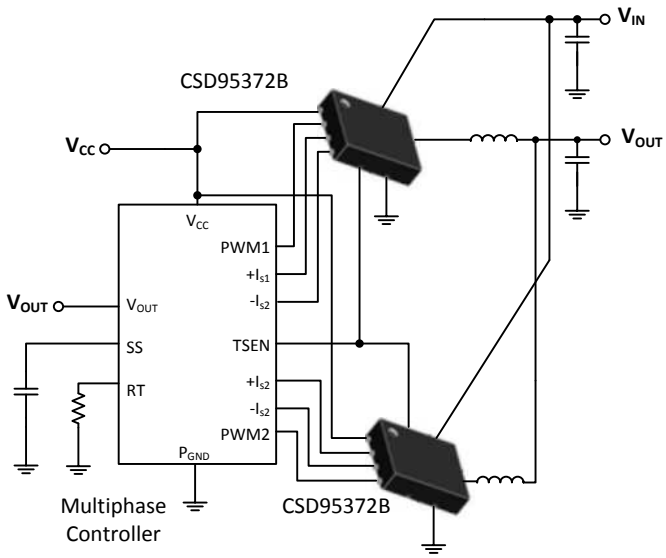
The CSD95372BQ5MC NexFET™ smart power stage is a highly optimized design for use in a high-power, high-density synchronous buck converter. This product integrates the driver IC and Power MOSFETs to complete the power stage switching function. This combination produces high-current, high-efficiency, and high-speed switching capability in a small 5 mm × 6 mm outline package. It also integrates the accurate current sensing and temperature sensing functionality to simplify system design and improve accuracy. In addition, the PCB footprint is optimized to help reduce design time and simplify the completion of the overall system design.

Device Information(1)

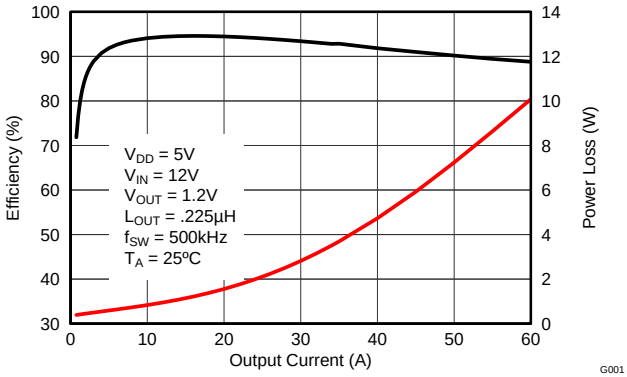
DEVICE	MEDIA	QTY	PACKAGE	SHIP
CSD95372BQ5MC	13-Inch Reel	2500	SON 5 × 6 mm DualCool Package	Tape and Reel
CSD95372BQ5MCT	7-Inch Reel	250		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Application Diagram



Typical Power Stage Efficiency and Power Loss



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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9 Mechanical, Packaging, and Orderable Information ... 7
9.1 Mechanical Drawing ... 7
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9.3 Recommended Stencil Opening ... 8

4 Revision History

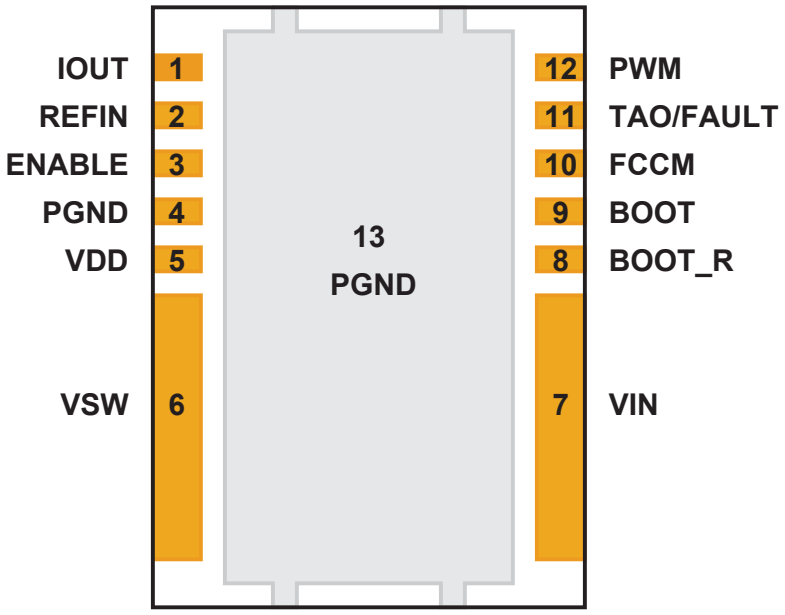
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (April 2014) to Revision A	Page
• Updated *Application Schematic* to show I_{OUT} (not I_{MON}) for each CSD95372B	5
• Corrected MAX A dimensions in *Mechanical Drawing* table to 1.050 mm (0.041 inch)	7

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5 Pin Configuration and Functions

Top View



Pin Functions

PIN		DESCRIPTION
NAME	NUMBER	
BOOT	9	Bootstrap capacitor connection. Connect a minimum of 0.1 µF 16 V X7R ceramic capacitor from BOOT to BOOT_R pins. The bootstrap capacitor provides the charge to turn on the control FET. The bootstrap diode is integrated.
BOOT_R	8	Return path for HS gate driver, connected to V_{SW} internally.
ENABLE	3	Enables device operation. If ENABLE = logic HIGH, turns on device. If ENABLE = logic LOW, the device is turned off and both MOSFET gates are actively pulled low. An internal 100 kΩ pulldown resistor will pull the ENABLE pin LOW if left floating.
FCCM	10	This pin enables the Diode Emulation function. When this pin is held LOW, Diode Emulation Mode is enabled for sync FET. When FCCM is HIGH, the device is operated in Forced Continuous Conduction Mode. An internal 5 µA current source will pull the FCCM pin to 3.3 V if left floating.
IOUT	1	Output of current sensing amplifier. V(IOUT) – V(REFIN) is proportional to the phase current.
P_{GND}	4	Power ground, connected directly to pin 13.
P_{GND}	13	Power ground
PWM	12	Pulse width modulated 3-state input from external controller. Logic LOW sets control FET gate low and sync FET gate high. Logic HIGH sets control FET gate high and sync FET gate low. Open or High Z sets both MOSFET gates low if greater than the tri-state shutdown hold-off time (t_{3HT}).
REFIN	2	External reference voltage input for current sensing amplifier
TAO/ FAULT	11	Temperature Analog Output. Reports a voltage proportional to the die temperature. An ORing diode is integrated in the IC. When used in multiphase application, a single wire can be used to connect the TAO pins of all the ICs. Only the highest temperature will be reported. TAO will be pulled up to 3.3 V if thermal shutdown occurs. TAO should be bypassed to P_{GND} with a 1 nF 16 V X7R ceramic capacitor.
V_{DD}	5	Supply voltage to gate driver and internal circuitry
V_{IN}	7	Input voltage pin. Connect input capacitors close to this pin.
V_{SW}	6	Phase node connecting the HS MOSFET source and LS MOSFET drain – pin connection to the output inductor.

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6 Specifications

6.1 Absolute Maximum Ratings

T_A = 25°C (unless otherwise noted)(1)

		MIN	MAX	UNIT
	V_{IN} to P_{GND}	–0.3	25	V
	V_{IN} to V_{SW}	–0.3	25	V
	V_{IN} to V_{SW} (10 ns)	–7	27	V
	V_{SW} to P_{GND}	–0.3	20	V
	V_{SW} to P_{GND} (10 ns)	–7	23	V
	V_{DD} to P_{GND}	–0.3	7	V
	ENABLE, PWM, FCCM. TAO, IOUT, REFIN to P_{GND}	–0.3	V_{DD} + 0.3 V	V
	BOOT to BOOT_R(2)	–0.3	V_{DD} + 0.3 V	V
P_D	Power dissipation		12	W
T_J	Operating junction	–55	150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Should not exceed 7 V

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM)	±2000	V
		Charged device model (CDM)	±500	

6.3 Recommended Operating Conditions

T_A = 25° (unless otherwise noted)

			MIN	MAX	UNIT
V_{DD}	Gate drive voltage		4.5	5.5	V
V_{IN}	Input supply voltage(1)			16	V
V_{OUT}	Output voltage			5.5	V
I_{OUT}	Continuous output current	V_{IN} = 12 V, V_{DD} = 5V, V_{OUT} = 3.3 V, f_{SW} = 500 kHz, L_{OUT} = 0.47 µH(2)		60	A
I_{OUT-PK}	Peak output current(3)			90	A
f_{SW}	Switching frequency	C_{BST} = 0.1 µF (min)		1250	kHz
	On time duty cycle	f_{SW} = 1 MHz		85%	
	Minimum PWM on time		40		ns
	Operating temperature		–40	125	°C

(1) Operating at high V_{IN} can create excessive AC voltage overshoots on the switch node (V_{SW}) during MOSFET switching transients. For reliable operation, the switch node (V_{SW}) to ground voltage must remain at or below the Absolute Maximum Ratings.
(2) Measurement made with six 10-µF (TDK C3216X5R1C106KT or equivalent) ceramic capacitors placed across V_{IN} to P_{GND} pins.
(3) System conditions as defined in Note 1. Peak Output Current is applied for t_p = 50 µs

6.4 Thermal Information

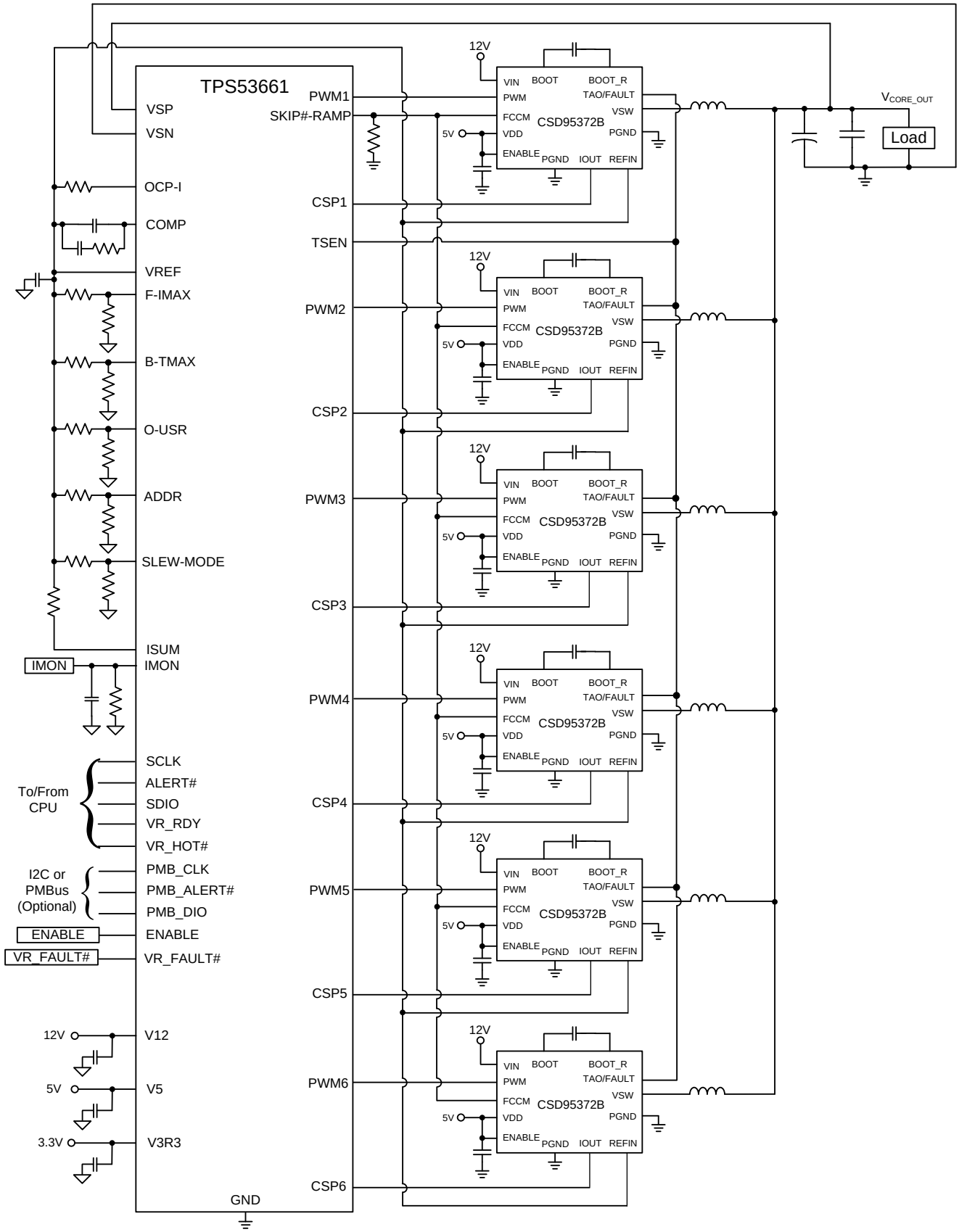
T_A = 25°C (unless otherwise noted)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC(top)}$	Junction-to-case (top of package) thermal resistance (1)			5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance(2)			1.5	°C/W

(1) $R_{\theta JC(top)}$ is determined with the device mounted on a 1 inch² (6.45 cm²), 2-oz (0.071 mm thick) Cu pad on a 1.5 inches x 1.5 inches, 0.06-inch (1.52 mm) thick FR4 board.
(2) $R_{\theta JB}$ value based on hottest board temperature within 1 mm of the package.

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7 Application Schematic



8 Device and Documentation Support

8.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

8.2 Trademarks

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8.3 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.4 Glossary

SLYZ022 — *TI Glossary*.

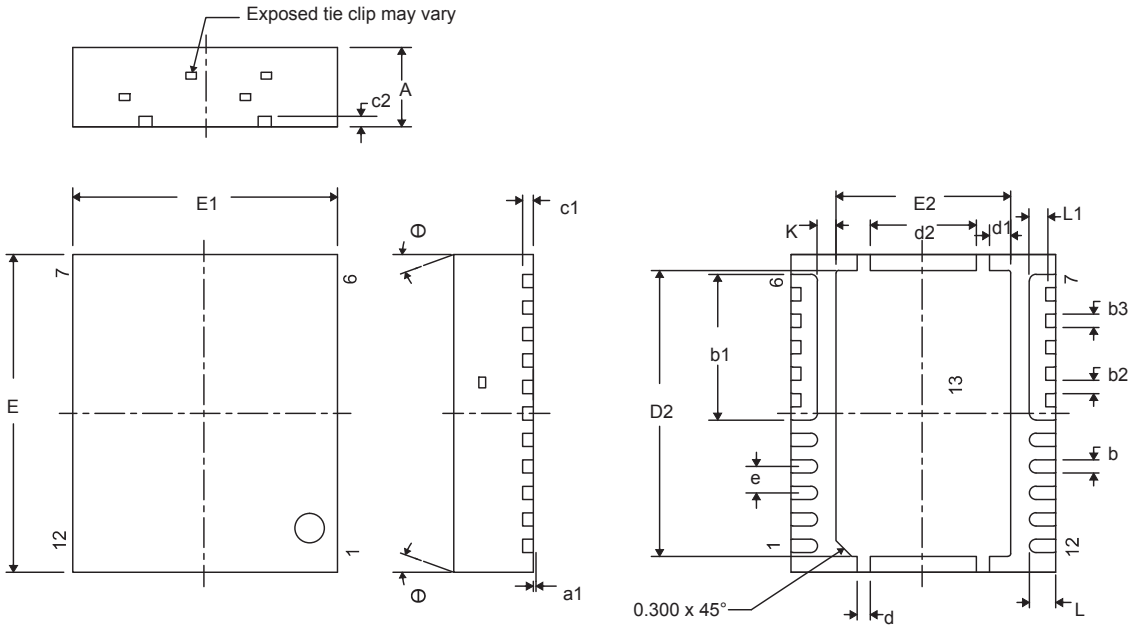
This glossary lists and explains terms, acronyms, and definitions.

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9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

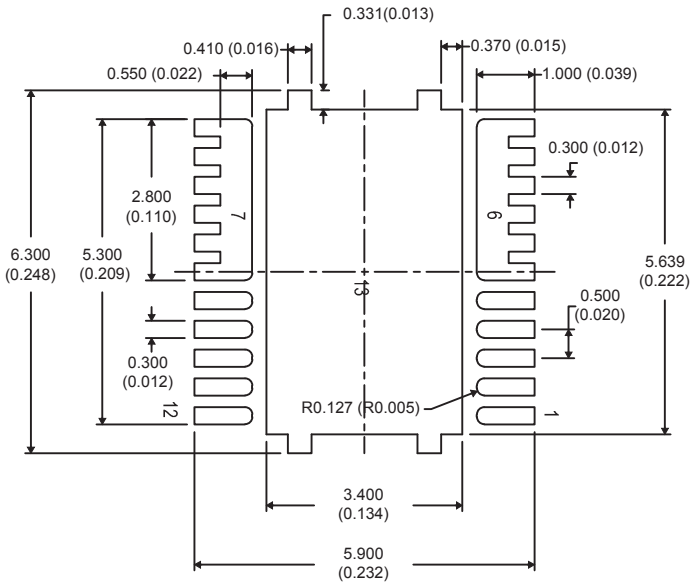
9.1 Mechanical Drawing



DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.950	1.000	1.050	0.037	0.039	0.041
a1	0.000	0.000	0.050	0.000	0.000	0.002
b	0.200	0.250	0.320	0.008	0.010	0.013
b1		2.750 TYP			0.108 TYP	
b2	0.200	0.250	0.320	0.008	0.010	0.013
b3		0.250 TYP			0.010 TYP	
c1	0.150	0.200	0.250	0.006	0.008	0.010
c2	0.200	0.250	0.300	0.008	0.010	0.012
D2	5.300	5.400	5.500	0.209	0.213	0.217
d	0.200	0.250	0.300	0.008	0.010	0.012
d1	0.350	0.400	0.450	0.014	0.016	0.018
d2	1.900	2.000	2.100	0.075	0.079	0.083
E	5.900	6.000	6.100	0.232	0.236	0.240
E1	4.900	5.000	5.100	0.193	0.197	0.201
E2	3.200	3.300	3.400	0.126	0.130	0.134
e		0.500 TYP			0.020 TYP	
K		0.350 TYP			0.014 TYP	
L	0.400	0.500	0.600	0.016	0.020	0.024
L1	0.210	0.310	0.410	0.008	0.012	0.016
θ	0.00	—	—	0.00	—	—

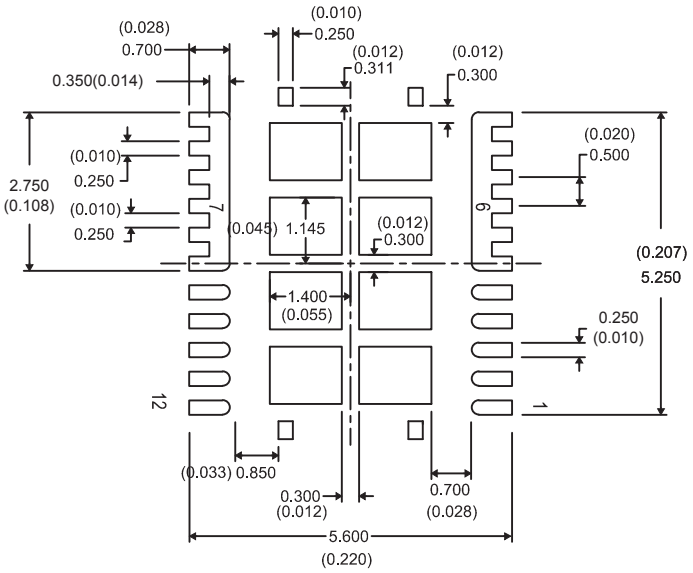
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9.2 Recommended PCB Land Pattern



1. Dimensions are in mm (inches).

9.3 Recommended Stencil Opening



1. Dimensions are in mm (inches).
2. Stencil thickness is 100 µm.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD95372BQ5MC	Active	Production	VSON-CLIP (DMC) | 12	2500 | LARGE T&R	ROHS Exempt	SN	Level-2-260C-1 YEAR	-55 to 150	95372BMC
CSD95372BQ5MC.A	Active	Production	VSON-CLIP (DMC) | 12	2500 | LARGE T&R	ROHS Exempt	SN	Level-2-260C-1 YEAR	-55 to 150	95372BMC
CSD95372BQ5MCT	Active	Production	VSON-CLIP (DMC) | 12	250 | SMALL T&R	ROHS Exempt	SN	Level-2-260C-1 YEAR	-55 to 150	95372BMC
CSD95372BQ5MCT.A	Active	Production	VSON-CLIP (DMC) | 12	250 | SMALL T&R	ROHS Exempt	SN	Level-2-260C-1 YEAR	-55 to 150	95372BMC

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

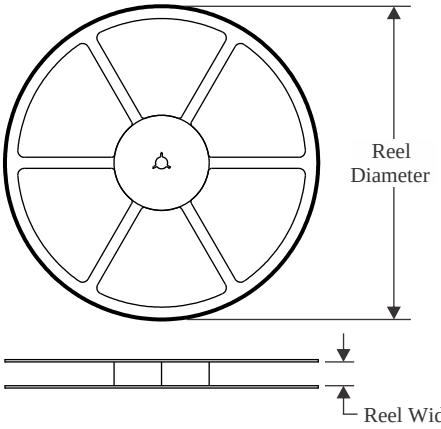
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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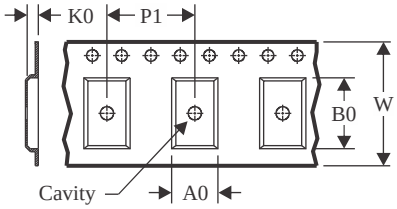
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

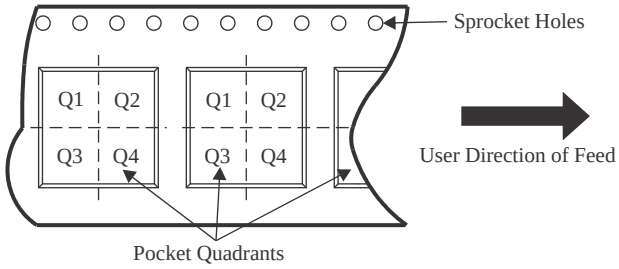


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

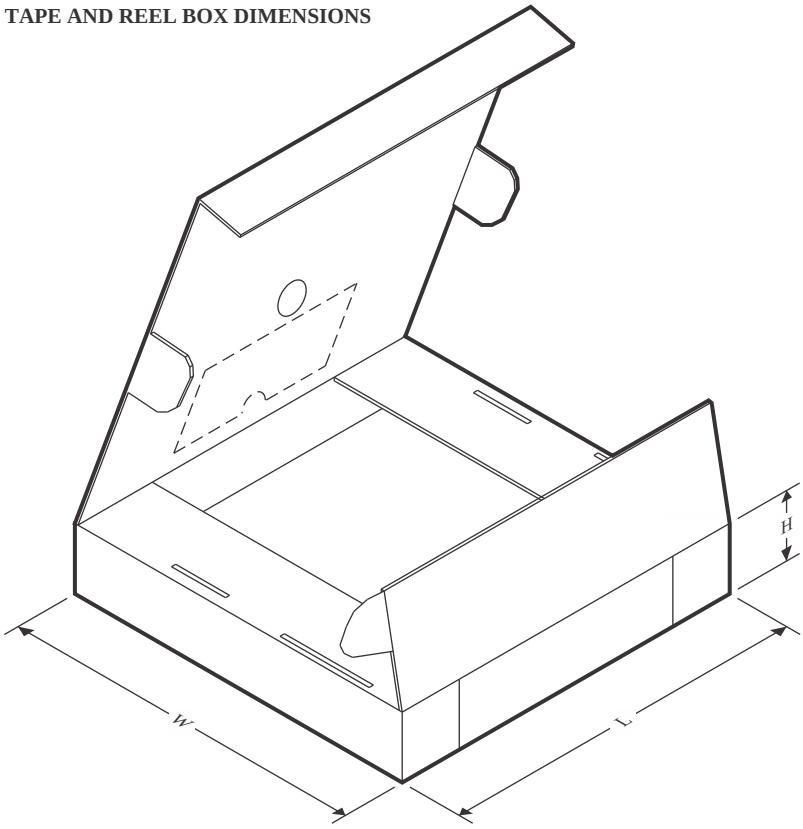
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD95372BQ5MC	VSON-CLIP	DMC	12	2500	330.0	12.4	5.3	6.3	1.2	8.0	12.0	Q1
CSD95372BQ5MCT	VSON-CLIP	DMC	12	250	180.0	12.4	5.3	6.3	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD95372BQ5MC	VSON-CLIP	DMC	12	2500	367.0	367.0	38.0
CSD95372BQ5MCT	VSON-CLIP	DMC	12	250	213.0	191.0	35.0

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