DAC081S101 8-Bit Micro Power Digital-to-Analog Converter with Rail-to-Rail Output

Check for Samples: DAC081S101

FEATURES

- **Guaranteed Monotonicity**
- **Low Power Operation**
- **Rail-to-Rail Voltage Output**
- **Power-on Reset to Zero Volts Output**
- **SYNC Interrupt Facility**
- **Wide Power Supply Range (+2.7V to +5.5V)**
- **Small Packages**
- **Power Down Feature**

APPLICATIONS

- **Battery-Powered Instruments**
- **Digital Gain and Offset Adjustment**
- **Programmable Voltage & Current Sources**
- **Programmable Attenuators**

DESCRIPTION

The DAC081S101 is a full-featured, general purpose 8-bit voltage-output digital-to-analog converter (DAC) that can operate from a single +2.7V to 5.5V supply and consumes just 175 µA of current at 3.6 Volts. The on-chip output amplifier allows rail-to-rail output swing and the three wire serial interface operates at clock rates up to 30 MHz over the specified supply voltage range and is compatible with standard SPI™, QSPI, MICROWIRE and DSP interfaces. Competitive devices are limited to 20 MHz clock rates at supply voltages in the 2.7V to 3.6V range.

The supply voltage for the DAC081S101 serves as its voltage reference, providing the widest possible output dynamic range. A power-on reset circuit ensures that the DAC output powers up to zero volts and remains there until there is a valid write to the device. A power-down feature reduces power consumption to less than a microWatt.

The low power consumption and small packages of the DAC081S101 make it an excellent choice for use in battery operated equipment.

The DAC081S101 is a direct replacement for the AD5300 and is one of a family of pin compatible DACs, including the 10-bit DAC101S101 and the 12-bit DAC121S101. The DAC081S101 operates over the extended industrial temperature range of −40°C to +105°C.

Table 1. Key Specifications

		VALUE
Resolution		8 bits
DNL		+0.04, -0.02 LSB (typ)
Output Settling Time		3 µs (typ)
Zero Code Error		3.8mV (typ)
Full-Scale Error		−0.07 %FS (typ)
Power Consumption	Normal Mode	0.63 mW (3.6V) / 1.41 mW (5.5V) typ
	Pwr Down Mode	0.14 µW (3.6V) / 0.33 µW (5.5V) typ

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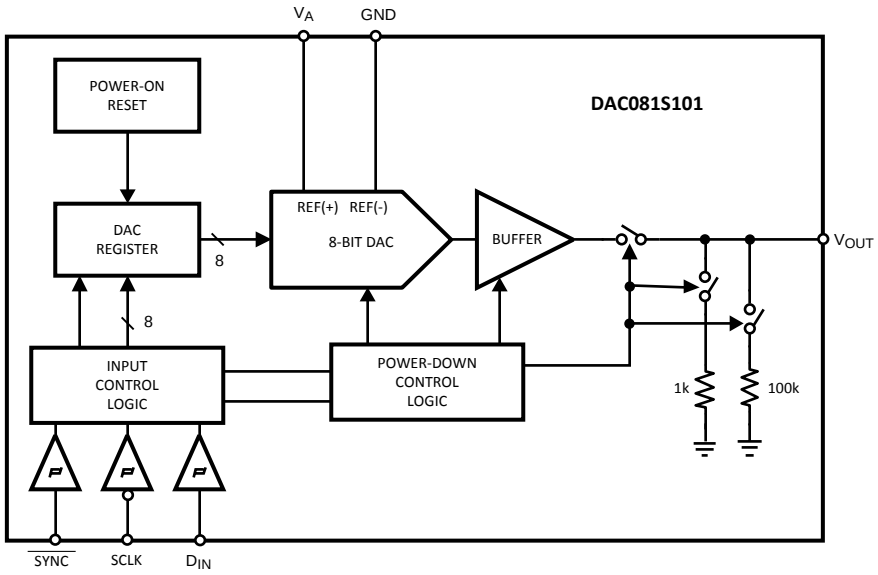
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Pin Configuration



Block Diagram



Pin Descriptions

Name	SOT-23 Pin No.	VSSOP Pin No.	Description
V_{OUT}	1	4	DAC Analog Output Voltage.
GND	2	8	Ground reference for all on-chip circuitry.
V_A	3	1	Power supply and Reference input. Should be decoupled to GND.
D_{IN}	4	7	Serial Data Input. Data is clocked into the 16-bit shift register on the falling edges of SCLK after the fall of $\overline{SYNC}$.
SCLK	5	6	Serial Clock Input. Data is clocked into the input shift register on the falling edges of this pin.
$\overline{SYNC}$	6	5	Frame synchronization input for the data input. When this pin goes low, it enables the input shift register and data is transferred on the falling edges of SCLK. The DAC is updated on the 16th clock cycle unless $\overline{SYNC}$ is brought high before the 16th clock, in which case the rising edge of $\overline{SYNC}$ acts as an interrupt and the write sequence is ignored by the DAC.
NC		2, 3	No Connect. There is no internal connection to these pins.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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Absolute Maximum Ratings (1)(2)

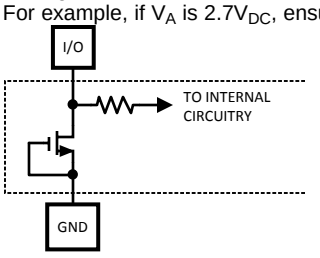
Supply Voltage, V_A	6.5V
Voltage on any Input Pin	−0.3V to (V_A + 0.3V)
Input Current at Any Pin (3)	10 mA
Package Input Current (3)	20 mA
Power Consumption at T_A = 25°C	See (4)
ESD Susceptibility (5) Human Body Model Machine Model	 2500V 250V
Soldering Temperature, Infrared, 10 Seconds (6)	235°C
Storage Temperature	−65°C to +150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) All voltages are measured with respect to GND = 0V, unless otherwise specified
(3) When the input voltage at any pin exceeds the power supplies (that is, less than GND, or greater than V_A), the current at that pin should be limited to 10 mA. The 20 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 10 mA to two.
(4) The absolute maximum junction temperature ($T_J$max) for this device is 150°C. The maximum allowable power dissipation is dictated by $T_J$max, the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature (T_A), and can be calculated using the formula $P_D MAX = (T_J max - T_A) / \theta_{JA}$. The values for maximum power dissipation will be reached only when the device is operated in a severe fault condition (e.g., when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Obviously, such conditions should always be avoided.
(5) Human body model is 100 pF capacitor discharged through a 1.5 kΩ resistor. Machine model is 220 pF discharged through ZERO Ohms.
(6) See the section entitled "Surface Mount" found in any post 1986 National Semiconductor Linear Data Book for methods of soldering surface mount devices.

Operating Ratings (1)(2)

Operating Temperature Range	−40°C ≤ T_A ≤ +105°C
Supply Voltage, V_A (3)	+2.7V to 5.5V
Any Input Voltage (4)	−0.1 V to (V_A + 0.1 V)
Output Load	0 to 1500 pF
SCLK Frequency	Up to 30 MHz

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) All voltages are measured with respect to GND = 0V, unless otherwise specified
(3) To guarantee accuracy, it is required that V_A be well bypassed.
(4) The analog inputs are protected as shown below. Input voltage magnitudes up to V_A + 300 mV or to 300 mV below GND will not damage this device. However, errors in the conversion result can occur if any input goes above V_A or below GND by more than 100 mV. For example, if V_A is 2.7V_{DC}, ensure that −100mV ≤ input voltages ≤2.8V_{DC} to ensure accurate conversions.



Package Thermal Resistances

Package	θ_{JA}
8-Lead VSSOP	240°C/W
6-Lead SOT	250°C/W

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Electrical Characteristics

Values shown in this table are design targets and are subject to change before product release.

The following specifications apply for V_A = +2.7V to +5.5V, R_L = 2kΩ to GND, C_L = 200 pF to GND, f_{SCLK} = 30 MHz, input code range 4 to 251. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$**: all other limits T_A = 25°C, unless otherwise specified.

Parameter		Test Conditions	Typical (1)	Limits (1)	Units (Limits)
STATIC PERFORMANCE					
	Resolution			**8**	Bits (min)
	Monotonicity			**8**	Bits (min)
INL	Integral Non-Linearity		+0.16	**+0.75**	LSB (max)
			−0.12	**−0.75**	LSB (min)
DNL	Differential Non-Linearity		+0.04	**+0.1**	LSB (max)
			−0.02	**−0.1**	LSB (min)
ZE	Zero Code Error	I_{OUT} = 0	+3.8	**+15**	mV (max)
FSE	Full-Scale Error	I_{OUT} = 0	−0.07	**−1.0**	%FSR (max)
GE	Gain Error	All ones Loaded to DAC register	−0.10	**±1.0**	%FSR (max)
ZCED	Zero Code Error Drift		−20		µV/°C
TC GE	Gain Error Tempco	V_A = 3V	−0.7		ppm/°C
		V_A = 5V	−1.0		ppm/°C
OUTPUT CHARACTERISTICS					
	Output Voltage Range	(2)		**0** **V_A**	V (min) V (max)
ZCO	Zero Code Output	V_A = 3V, I_{OUT} = 10 µA	2.0		mV
		V_A = 3V, I_{OUT} = 100 µA	5.0		mV
		V_A = 5V, I_{OUT} = 10 µA	3.0		mV
		V_A = 5V, I_{OUT} = 100 µA	5.4		mV
FSO	Full Scale Output	V_A = 3V, I_{OUT} = 10 µA	2.986		V
		V_A = 3V, I_{OUT} = 100 µA	2.976		V
		V_A = 5V, I_{OUT} = 10 µA	4.976		V
		V_A = 5V, I_{OUT} = 100 µA	4.970		V
	Maximum Load Capacitance	R_L = ∞	1500		pF
		R_L = 2kΩ	1500		pF
	DC Output Impedance		1.3		Ohm
I_{OS}	Output Short Circuit Current	V_A = 5V, V_{OUT} = 0V, Input code = FFh	−63		mA
		V_A = 3V, V_{OUT} = 0V, Input code = FFh	−50		mA
		V_A = 5V, V_{OUT} = 5V, Input code = 00h	74		mA
		V_A = 3V, V_{OUT} = 3V, Input code = 00h	53		mA

(1) Typical figures are at T_J = 25°C, and represent most likely parametric norms. Test limits are guaranteed to TI's AOQL (Average Outgoing Quality Level).

(2) This parameter is guaranteed by design and/or characterization and is not tested in production.

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Electrical Characteristics (continued)

Values shown in this table are design targets and are subject to change before product release.

The following specifications apply for V_A = +2.7V to +5.5V, R_L = 2kΩ to GND, C_L = 200 pF to GND, f_{SCLK} = 30 MHz, input code range 4 to 251. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$**: all other limits T_A = 25°C, unless otherwise specified.

Parameter		Test Conditions		Typical (1)	Limits (1)	Units (Limits)
LOGIC INPUT						
I_{IN}	Input Current(3)				**±1**	µA (max)
V_{IL}	Input Low Voltage(3)	V_A = 5V			**0.8**	V (max)
		V_A = 3V			**0.5**	V (max)
V_{IH}	Input High Voltage(3)	V_A = 5V			**2.4**	V (min)
		V_A = 3V			**2.1**	V (min)
C_{IN}	Input Capacitance(3)				**3**	pF (max)
POWER REQUIREMENTS						
I_A	Supply Current (output unloaded)	Normal Mode f_{SCLK} = 30 MHz	V_A = 5.5V	256	**328**	µA (max)
			V_A = 3.6V	174	**224**	µA (max)
		Normal Mode f_{SCLK} = 20 MHz	V_A = 5.5V	221	**294**	µA (max)
			V_A = 3.6V	154	**200**	µA (max)
		Normal Mode f_{SCLK} = 0	V_A = 5.0V	142		µA (max)
			V_A = 3.0V	107		µA (max)
		All PD Modes, f_{SCLK} = 30 MHz	V_A = 5.0V	83		µA (max)
			V_A = 3.0V	42		µA (max)
		All PD Modes, f_{SCLK} = 20 MHz	V_A = 5.0V	56		µA (max)
			V_A = 3.0V	28		µA (max)
		All PD Modes, f_{SCLK} = 0 (3)	V_A = 5.5V	0.06	**1.0**	µA (max)
			V_A = 3.6V	0.04	**1.0**	µA (max)
P_C	Power Consumption (output unloaded)	Normal Mode f_{SCLK} = 30 MHz	V_A = 5.5V	1.41	**1.80**	mW (max)
			V_A = 3.6V	0.63	**0.81**	mW (max)
		Normal Mode f_{SCLK} = 20 MHz	V_A = 5.5V	1.22	**1.62**	mW (max)
			V_A = 3.6V	0.55	**0.72**	mW (max)
		Normal Mode f_{SCLK} = 0	V_A = 5.0V	0.71		µW (max)
			V_A = 3.0V	0.32		µW (max)
		All PD Modes, f_{SCLK} = 30 MHz	V_A = 5.0V	0.42		µW (max)
			V_A = 3.0V	0.13		µW (max)
		All PD Modes, f_{SCLK} = 20 MHz	V_A = 5.0V	0.28		µW (max)
			V_A = 3.0V	0.08		µW (max)
		All PD Modes, f_{SCLK} = 0 (3)	V_A = 5.5V	0.33	**5.5**	µW (max)
			V_A = 3.6V	0.14	**3.6**	µW (max)
I_{OUT} / I_A	Power Efficiency	I_{LOAD} = 2mA	V_A = 5V	91		%
			V_A = 3V	94		%

(3) This parameter is guaranteed by design and/or characterization and is not tested in production.

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AC and Timing Characteristics

Values shown in this table are design targets and are subject to change before product release.
The following specifications apply for V_A = +2.7V to +5.5V, R_L = 2kΩ to GND, C_L = 200 pF to GND, f_{SCLK} = 30 MHz, input code range 4 to 251. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$**: all other limits T_A = 25°C, unless otherwise specified.

Parameter		Test Conditions		Typical	Limits	Units (Limits)
f_{SCLK}	SCLK Frequency				**30**	MHz (max)
t_s	Output Voltage Settling Time (1)	40h to C0h code change, R_L = 2kΩ	$C_L \le$ 200 pF	3	**5**	µs (max)
SR	Output Slew Rate			1		V/µs
	Glitch Impulse	Code change from 80h to 7Fh		12		nV-sec
	Digital Feedthrough			0.5		nV-sec
t_{WU}	Wake-Up Time	V_A = 5V		6		µs
		V_A = 3V		39		µs
$1/f_{SCLK}$	SCLK Cycle Time				**33**	ns (min)
t_H	SCLK High time			5	**13**	ns (min)
t_L	SCLK Low Time			5	**13**	ns (min)
t_{SUCL}	Set-up Time $\overline{SYNC}$ to SCLK Rising Edge			−15	**0**	ns (min)
t_{SUD}	Data Set-Up Time			2.5	**5**	ns (min)
t_{DHD}	Data Hold Time			2.5	**4.5**	ns (min)
t_{CS}	SCLK fall to rise of $\overline{SYNC}$	V_A = 5V		0	**3**	ns (min)
		V_A = 3V		−2	**1**	ns (min)
t_{SYNC}	$\overline{SYNC}$ High Time	2.7 ≤ V_A ≤ 3.6		9	**20**	ns (min)
		3.6 ≤ V_A ≤ 5.5		5	**10**	ns (min)

(1) This parameter is guaranteed by design and/or characterization and is not tested in production.

Specification Definitions

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB, which is V_{REF} / 256 = V_A / 256.

DIGITAL FEEDTHROUGH is a measure of the energy injected into the analog output of the DAC from the digital inputs when the DAC outputs are not updated. It is measured with a full-scale code change on the data bus.

FULL-SCALE ERROR is the difference between the actual output voltage with a full scale code (FFh) loaded into the DAC and the value of V_A x 255 / 256.

GAIN ERROR is the deviation from the ideal slope of the transfer function. It can be calculated from Zero and Full-Scale Errors as GE = FSE - ZE, where GE is Gain error, FSE is Full-Scale Error and ZE is Zero Error.

GLITCH IMPULSE is the energy injected into the analog output when the input code to the DAC register changes. It is specified as the area of the glitch in nanovolt-seconds.

INTEGRAL NON-LINEARITY (INL) is a measure of the deviation of each individual code from a straight line through the input to output transfer function. The deviation of any given code from this straight line is measured from the center of that code value. The end point method is used. INL for this product is specified over a limited range, per the Electrical Tables.

LEAST SIGNIFICANT BIT (LSB) is the bit that has the smallest value or weight of all bits in a word. This value is

$$LSB = V_{REF} / 2^n \quad (1)$$

where V_{REF} is the supply voltage for this product, and "n" is the DAC resolution in bits, which is 8 for the DAC081S101.

MAXIMUM LOAD CAPACITANCE is the maximum capacitance that can be driven by the DAC with output stability maintained.

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MONOTONICITY is the condition of being monotonic, where the DAC has an output that never decreases when the output code increases.

MOST SIGNIFICANT BIT (MSB) is the bit that has the largest value or weight of all bits in a word. Its value is 1/2 of V_A.

POWER EFFICIENCY is the ratio of the output current to the total supply current. The output current comes from the power supply. The difference between the supply and output currents, is the power consumed by the device without a load.

SETTLING TIME is the time for the output to settle within 1/2 LSB of the final value after the input code is updated.

WAKE-UP TIME is the time for the output to settle to within 1/2 LSB of the final value after the device is commanded to the active mode from any of the power down modes.

ZERO CODE ERROR is the output error, or voltage, present at the DAC output after a code of 00h has been entered.

Transfer Characteristic

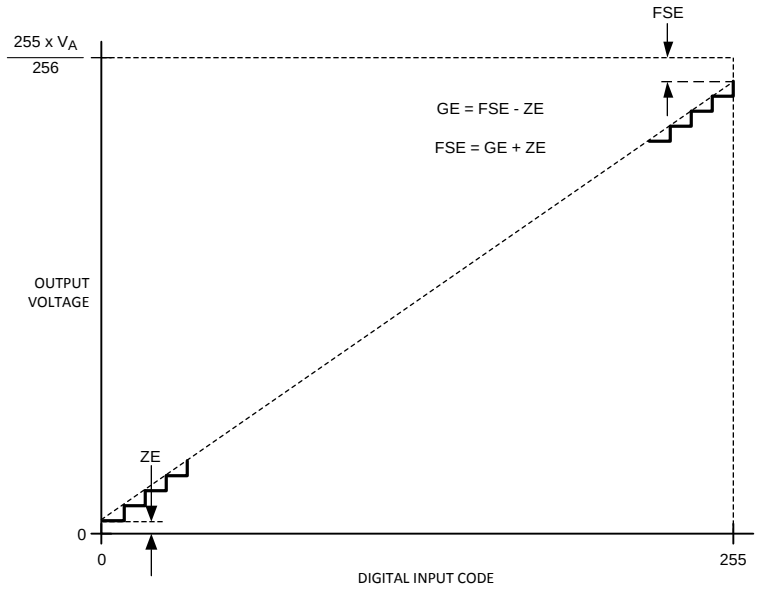


Figure 1. Input / Output Transfer Characteristic

Timing Diagram

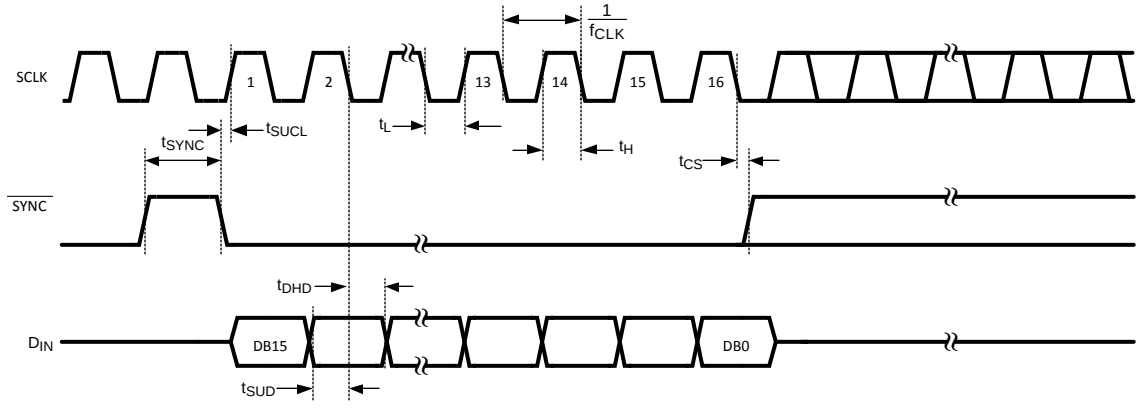


Figure 2. DAC081S101 Timing

Typical Performance Characteristics

f_{SCLK} = 30 MHz, T_A = 25C, Input Code Range 4 to 251, unless otherwise stated

DNL at V_A = 3.0V

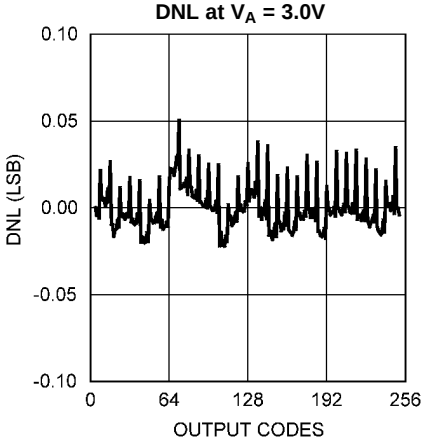


Figure 3.

DNL at V_A = 5.0V

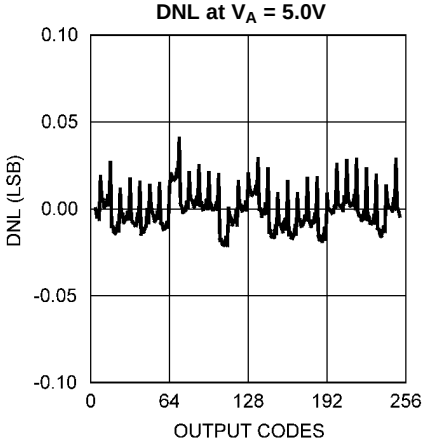


Figure 4.

INL at V_A = 3.0V

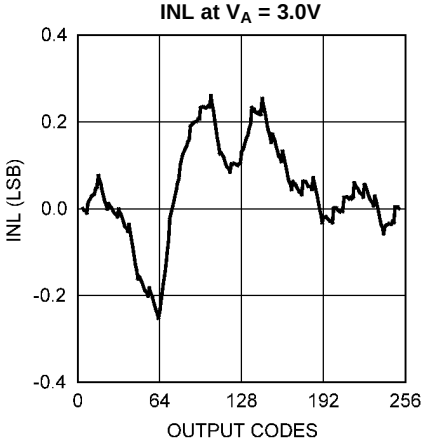


Figure 5.

INL at V_A = 5.0V

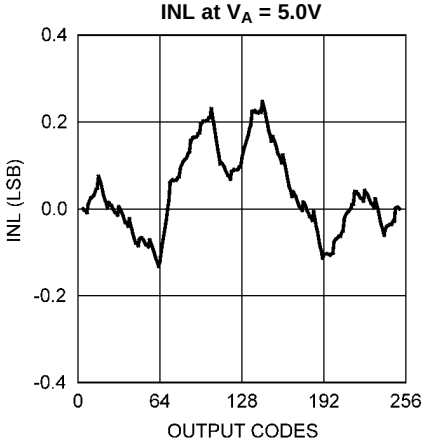


Figure 6.

TUE at V_A = 3.0V

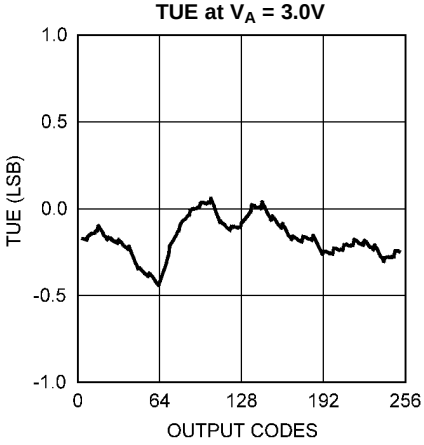


Figure 7.

TUE at V_A = 5.0V

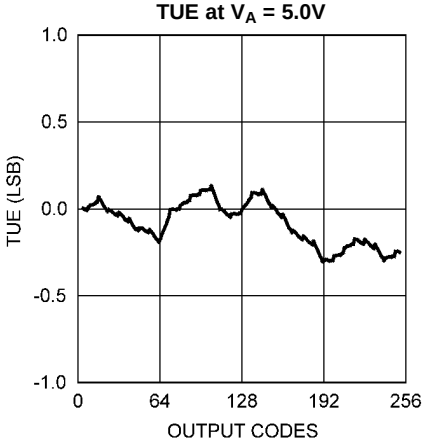


Figure 8.

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Typical Performance Characteristics (continued)

f_{SCLK} = 30 MHz, T_A = 25C, Input Code Range 4 to 251, unless otherwise stated

DNL vs. V_A

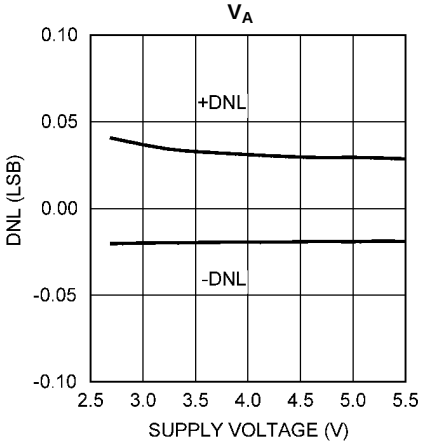


Figure 9.

INL vs. V_A

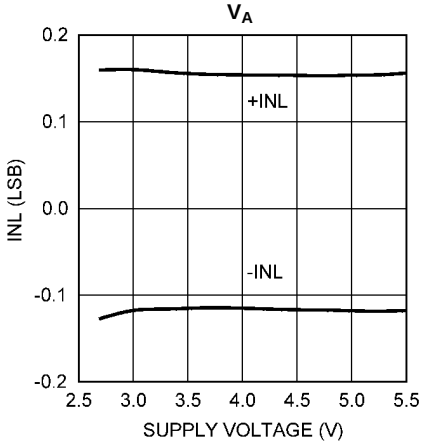


Figure 10.

3V DNL vs. f_{SCLK}

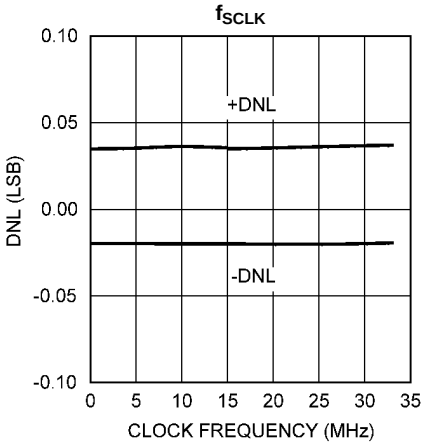


Figure 11.

5V DNL vs. f_{SCLK}

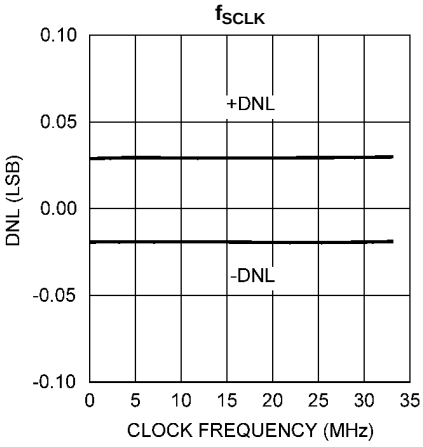


Figure 12.

3V DNL vs. Clock Duty Cycle

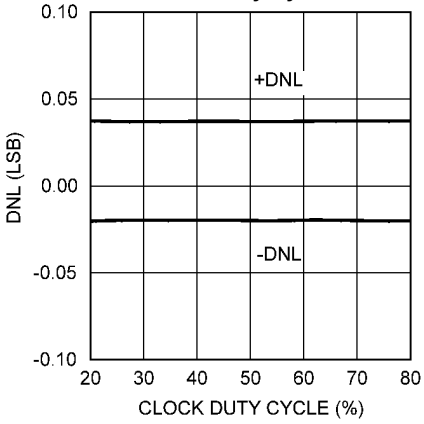


Figure 13.

5V DNL vs. Clock Duty Cycle

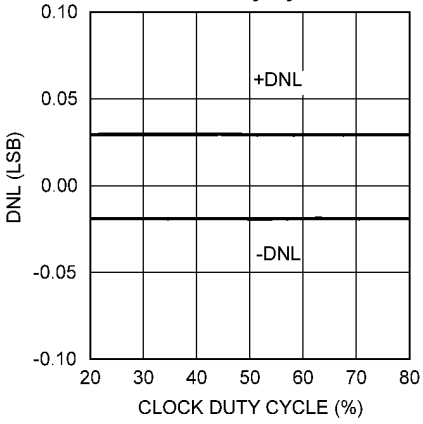


Figure 14.

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Typical Performance Characteristics (continued)

f_{SCLK} = 30 MHz, T_A = 25C, Input Code Range 4 to 251, unless otherwise stated

3V DNL vs. Temperature

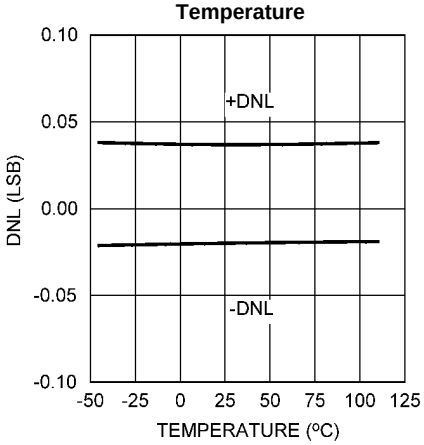


Figure 15.

5V DNL vs. Temperature

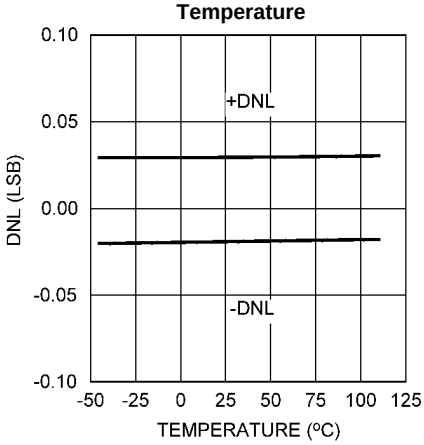


Figure 16.

3V INL vs. f_{SCLK}

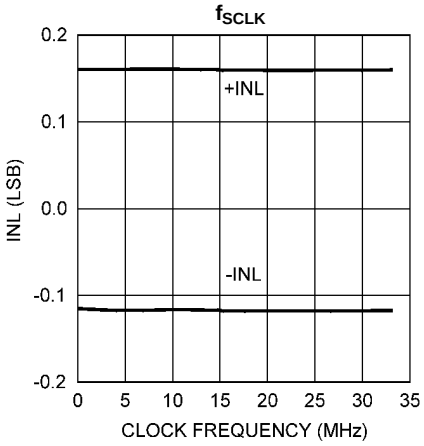


Figure 17.

5V INL vs. f_{SCLK}

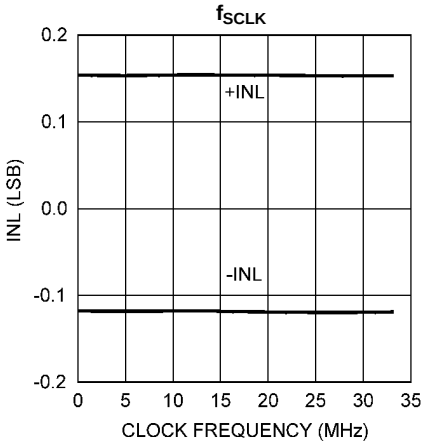


Figure 18.

3V INL vs. Clock Duty Cycle

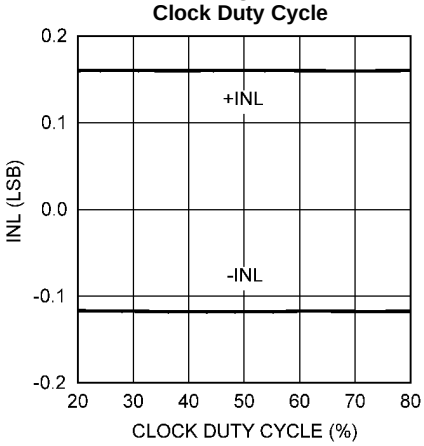


Figure 19.

5V INL vs. Clock Duty Cycle

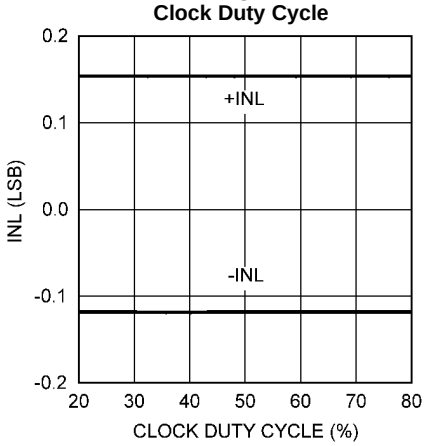


Figure 20.

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Typical Performance Characteristics (continued)

f_{SCLK} = 30 MHz, T_A = 25C, Input Code Range 4 to 251, unless otherwise stated

3V INL vs. Temperature

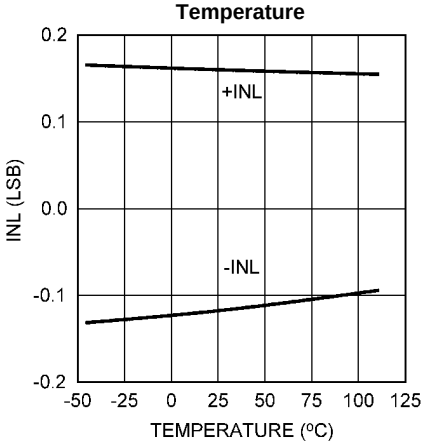


Figure 21.

5V INL vs. Temperature

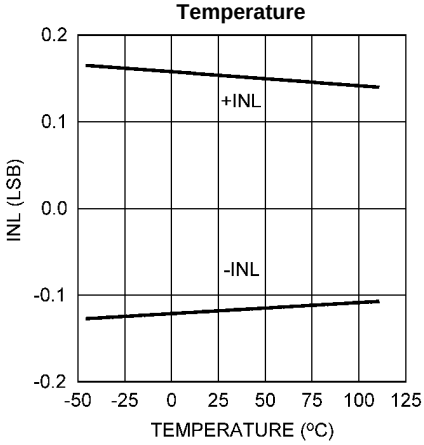


Figure 22.

Zero Code Error vs. f_{SCLK}

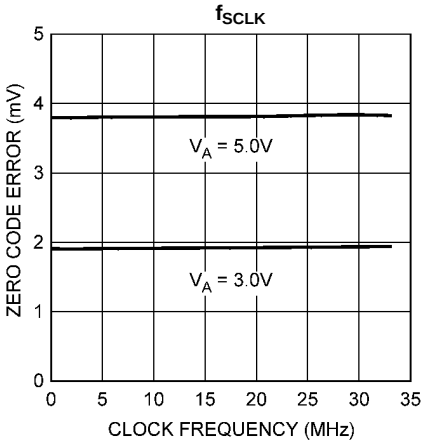


Figure 23.

Zero Code Error vs. Clock Duty Cycle

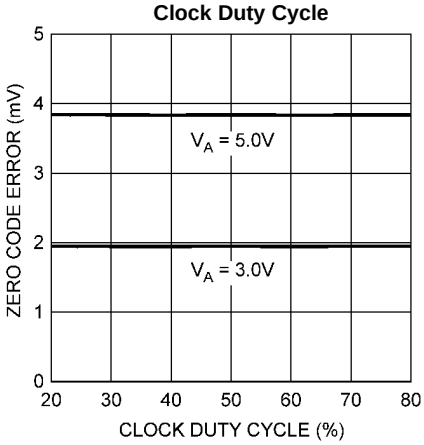


Figure 24.

Zero Code Error vs. Temperature

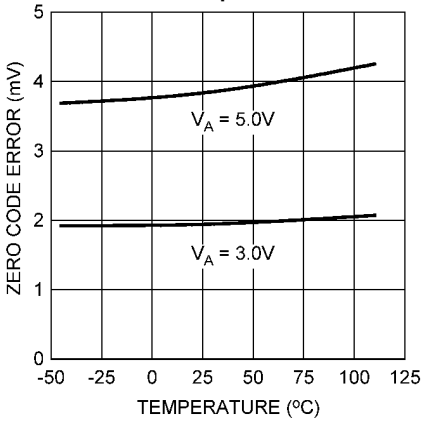


Figure 25.

Full-Scale Error vs. f_{SCLK}

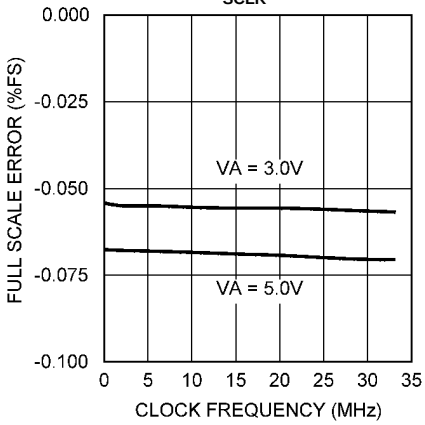


Figure 26.

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Typical Performance Characteristics (continued)

f_{SCLK} = 30 MHz, T_A = 25C, Input Code Range 4 to 251, unless otherwise stated

Full-Scale Error vs. Clock Duty Cycle

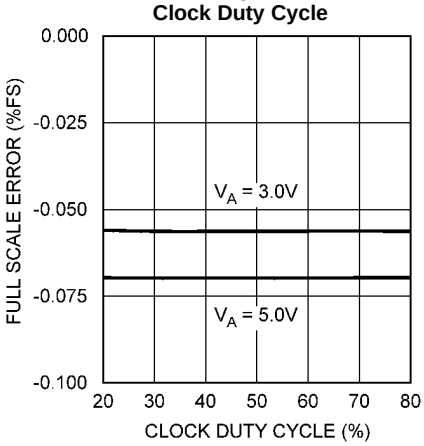


Figure 27.

Full-Scale Error vs. Temperature

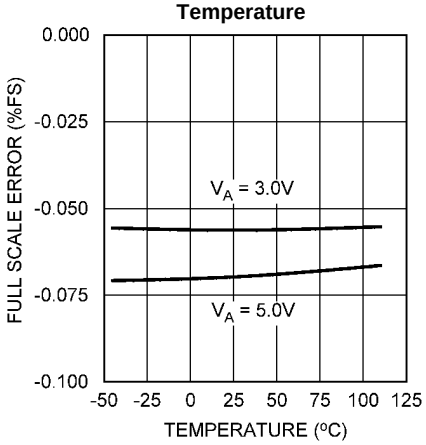


Figure 28.

Supply Current vs. V_A

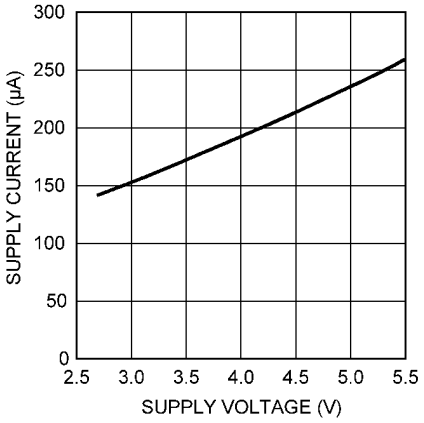


Figure 29.

Supply Current vs. Temperature

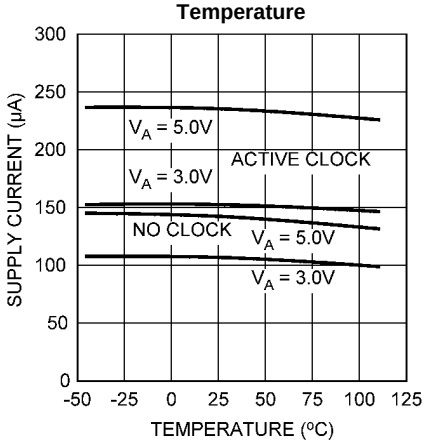


Figure 30.

5V Glitch Response

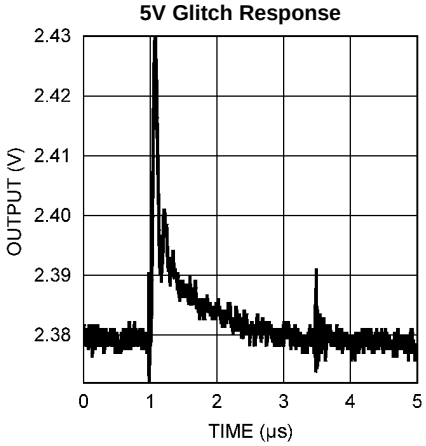


Figure 31.

Power-On Reset

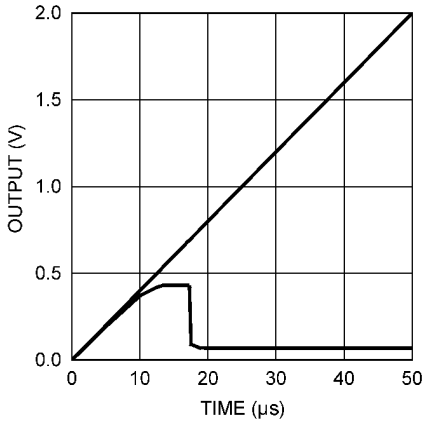


Figure 32.

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Typical Performance Characteristics (continued)

f_{SCLK} = 30 MHz, T_A = 25C, Input Code Range 4 to 251, unless otherwise stated

3V Wake-Up Time

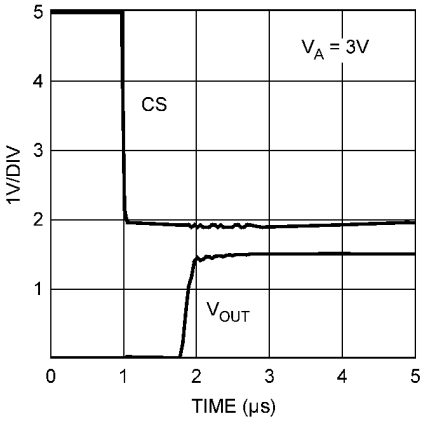


Figure 33.

5V Wake-Up Time

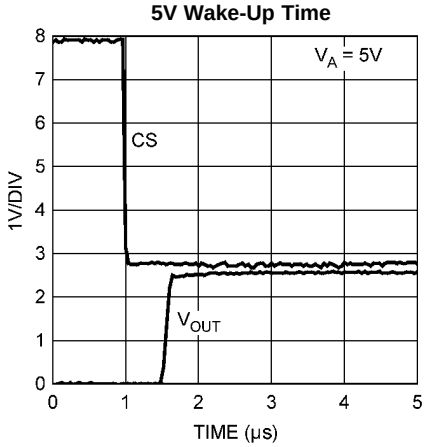


Figure 34.

FUNCTIONAL DESCRIPTION

DAC SECTION

The DAC081S101 is fabricated on a CMOS process with an architecture that consists of switches and a resistor string that are followed by an output buffer. The power supply serves as the reference voltage. The input coding is straight binary with an ideal output voltage of:

$$V_{OUT} = V_A \times (D / 256) \quad (2)$$

where *D* is the decimal equivalent of the binary code that is loaded into the DAC register and can take on any value between 0 and 255.

RESISTOR STRING

The resistor string is shown in Figure 35. This string consists of 4096 equal valued resistors with a switch at each junction of two resistors, plus a switch to ground. The code loaded into the DAC register determines which switch is closed, connecting the proper node to the amplifier. This configuration guarantees that the DAC is monotonic.

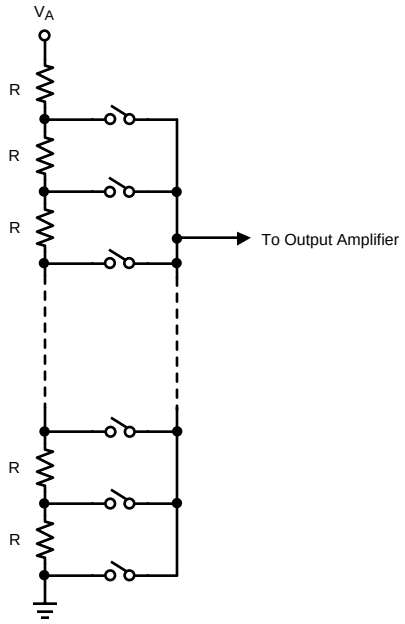


Figure 35. DAC Resistor String

OUTPUT AMPLIFIER

The output buffer amplifier is a rail-to-rail type, providing an output voltage range of 0V to V_A. All amplifiers, even rail-to-rail types, exhibit a loss of linearity as the output approaches the supply rails (0V and V_A, in this case). For this reason, linearity is specified over less than the full output range of the DAC. The output capabilities of the amplifier are described in the Electrical Tables.

SERIAL INTERFACE

The three-wire interface is compatible with SPI, QSPI and MICROWIRE as well as most DSPs. See the Timing Diagram for information on a write sequence.

A write sequence begins by bringing the $\overline{\text{SYNC}}$ line low. Once $\overline{\text{SYNC}}$ is low, the data on the D_{IN} line is clocked into the 16-bit serial input register on the falling edges of SCLK. On the 16th falling clock edge, the last data bit is clocked in and the programmed function (a change in the mode of operation and/or a change in the DAC register contents) is executed. At this point the $\overline{\text{SYNC}}$ line may be kept low or brought high. In either case, it must be brought high for the minimum specified time before the next write sequence as a falling edge of $\overline{\text{SYNC}}$ is used to initiate the next write cycle.

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Since the $\overline{SYNC}$ and D_{IN} buffers draw more current when they are high, they should be idled low between write sequences to minimize power consumption.

INPUT SHIFT REGISTER

The input shift register, Figure 36, has sixteen bits. The first two bits are "don't cares" and are followed by two bits that determine the mode of operation (normal mode or one of three power-down modes). The contents of the serial input register are transferred to the DAC register on the sixteenth falling edge of SCLK. See Timing Diagram, Figure 2.

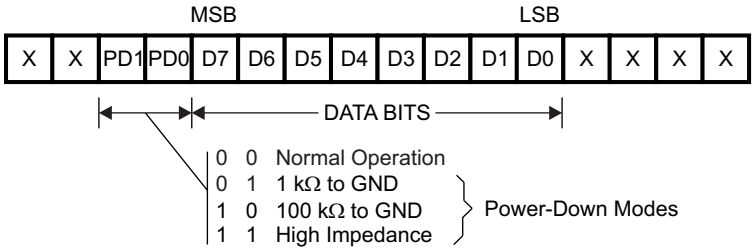


Figure 36. Input Register Contents

Normally, the $\overline{SYNC}$ line is kept low for at least 16 falling edges of SCLK and the DAC is updated on the 16th SCLK falling edge. However, if $\overline{SYNC}$ is brought high before the 16th falling edge, the shift register is reset and the write sequence is invalid. The DAC register is not updated and there is no change in the mode of operation or in the output voltage.

POWER-ON RESET

The power-on reset circuit controls the output voltage during power-up. Upon application of power the DAC register is filled with zeros and the output voltage is 0 Volts and remains there until a valid write sequence is made to the DAC.

POWER-DOWN MODES

The DAC081S101 has four modes of operation. These modes are set with two bits (DB13 and DB12) in the control register.

Table 2. Modes of Operation

DB13	DB12	Operating Mode
0	0	Normal Operation
0	1	Power-Down with 1kΩ to GND
1	0	Power-Down with 100kΩ to GND
1	1	Power-Down with Hi-Z

When both DB13 and DB12 are 0, the device operates normally. For the other three possible combinations of these bits the supply current drops to its power-down level and the output is pulled down with either a 1kΩ or a 100KΩ resistor, or is in a high impedance state, as described in Table 2.

The bias generator, output amplifier, the resistor string and other linear circuitry are all shut down in any of the power-down modes. However, the contents of the DAC register are unaffected when in power-down, so when coming out of power down the output voltage returns to the same voltage it was before entering power down. Minimum power consumption is achieved in the power-down mode with SCLK disabled and $\overline{SYNC}$ and D_{IN} idled low. The time to exit power-down (Wake-Up Time) is typically t_{WU} µsec as stated in the A.C. and Timing Characteristics Table.

APPLICATION INFORMATION

The simplicity of the DAC081S101 implies ease of use. However, it is important to recognize that any data converter that utilizes its supply voltage as its reference voltage will have essentially zero PSRR (Power Supply Rejection Ratio). Therefore, it is necessary to provide a noise-free supply voltage to the device.

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DSP/MICROPROCESSOR INTERFACING

Interfacing the DAC081S101 to microprocessors and DSPs is quite simple. The following guidelines are offered to hasten the design process.

ADSP-2101/ADSP2103 Interfacing

Figure 37 shows a serial interface between the DAC081S101 and the ADSP-2101/ADSP2103. The DSP should be set to operate in the SPORT Transmit Alternate Framing Mode. It is programmed through the SPORT control register and should be configured for Internal Clock Operation, Active Low Framing and 16-bit Word Length. Transmission is started by writing a word to the Tx register after the SPORT mode has been enabled.

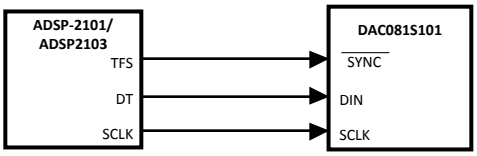


Figure 37. ADSP-2101/2103 Interface

80C51/80L51 Interface

A serial interface between the DAC081S101 and the 80C51/80L51 microcontroller is shown in Figure 38. The $\overline{\text{SYNC}}$ signal comes from a bit-programmable pin on the microcontroller. The example shown here uses port line P3.3. This line is taken low when data is to transmitted to the DAC081S101. Since the 80C51/80L51 transmits 8-bit bytes, only eight falling clock edges occur in the transmit cycle. To load data into the DAC, the P3.3 line must be left low after the first eight bits are transmitted. A second write cycle is initiated to transmit the second byte of data, after which port line P3.3 is brought high. The 80C51/80L51 transmit routine must recognize that the 80C51/80L51 transmits data with the LSB first while the DAC081S101 requires data with the MSB first.

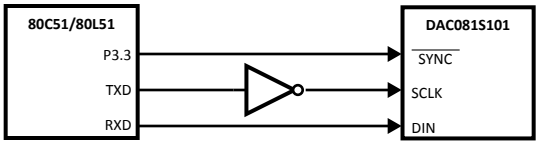


Figure 38. 80C51/80L51 Interface

68HC11 Interface

A serial interface between the DAC081S101 and the 68HC11 microcontroller is shown in Figure 39. The $\overline{\text{SYNC}}$ line of the DAC081S101 is driven from a port line (PC7 in the figure), similar to the 80C51/80L51.

The 68HC11 should be configured with its CPOL bit as a zero and its CPHA bit as a one. This configuration causes data on the MOSI output to be valid on the falling edge of SCLK. PC7 is taken low to transmit data to the DAC. The 68HC11 transmits data in 8-bit bytes with eight falling clock edges. Data is transmitted with the MSB first. PC7 must remain low after the first eight bits are transferred. A second write cycle is initiated to transmit the second byte of data to the DAC, after which PC7 should be raised to end the write sequence.

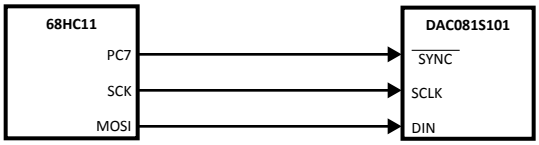


Figure 39. 68HC11 Interface

Microwire Interface

Figure 40 shows an interface between a Microwire compatible device and the DAC081S101. Data is clocked out on the rising edges of the SCLK signal.

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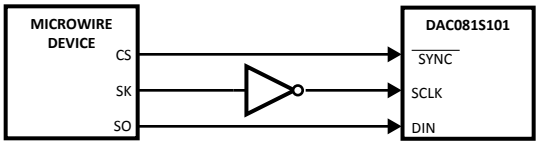


Figure 40. Microwire Interface

USING REFERENCES AS POWER SUPPLIES

Recall the need for a quiet supply source for devices that use their power supply voltage as a reference voltage.

Since the DAC081S101 consumes very little power, a reference source may be used as the supply voltage. The advantages of using a reference source over a voltage regulator are accuracy and stability. Some low noise regulators can also be used for the power supply of the DAC081S101. Listed below are a few power supply options for the DAC081S101.

LM4130

The LM4130 reference, with its 0.05% accuracy over temperature, is a good choice as a power source for the DAC081S101. Its primary disadvantage is the lack of 3V and 5V versions. However, the 4.096V version is useful if a 0 to 4.095V output range is desirable or acceptable. Bypassing the LM4130 VIN pin with a 0.1µF capacitor and the VOUT pin with a 2.2µF capacitor will improve stability and reduce output noise. The LM4130 comes in a space-saving 5-pin SOT23.

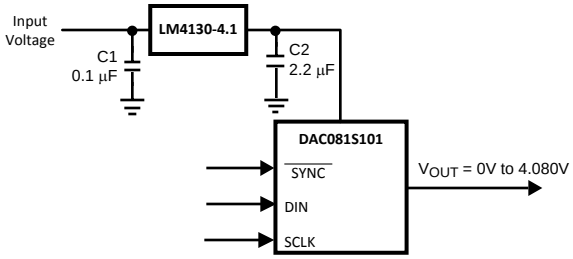


Figure 41. The LM4130 as a power supply

LM4050

Available with accuracy of 0.44%, the LM4050 shunt reference is also a good choice as a power regulator for the DAC081S101. It does not come in a 3 Volt version, but 4.096V and 5V versions are available. It comes in a space-saving 3-pin SOT-23.

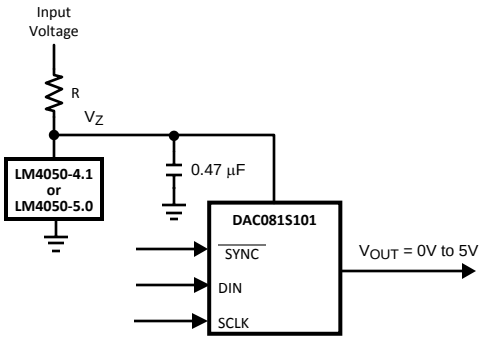


Figure 42. The LM4050 as a power supply

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The minimum resistor value in the circuit of Figure 42 should be chosen such that the maximum current through the LM4050 does not exceed its 15 mA rating. The conditions for maximum current include the input voltage at its maximum, the LM4050 voltage at its minimum, the resistor value at its minimum due to tolerance, and the DAC081S101 draws zero current. The maximum resistor value must allow the LM4050 to draw more than its minimum current for regulation plus the maximum DAC081S101 current in full operation. The conditions for minimum current include the input voltage at its minimum, the LM4050 voltage at its maximum, the resistor value at its maximum due to tolerance, and the DAC081S101 draws its maximum current. These conditions can be summarized as

$$R(min) = (V_{IN}(max) - V_Z(min) / (I_A(min) + I_Z(max)) \quad (3)$$

and

$$R(max) = (V_{IN}(min) - V_Z(max) / (I_A(max) + I_Z(min)) \quad (4)$$

where $V_Z(min)$ and $V_Z(max)$ are the nominal LM4050 output voltages ± the LM4050 output tolerance over temperature, $I_Z(max)$ is the maximum allowable current through the LM4050, $I_Z(min)$ is the minimum current required by the LM4050 for proper regulation, $I_A(max)$ is the maximum DAC081S101 supply current, and $I_A(min)$ is the minimum DAC081S101 supply current.

LP3985

The LP3985 is a low noise, ultra low dropout voltage regulator with a 3% accuracy over temperature. It is a good choice for applications that do not require a precision reference for the DAC081S101. It comes in 3.0V, 3.3V and 5V versions, among others, and sports a low 30 µV noise specification at low frequencies. Since low frequency noise is relatively difficult to filter, this specification could be important for some applications. The LP3985 comes in a space-saving 5-pin SOT-23 and 5-bump DSBGA packages.

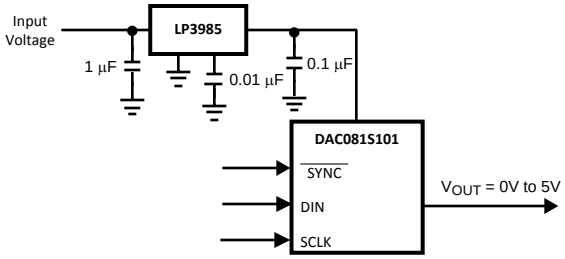


Figure 43. Using the LP3985 regulator

An input capacitance of 1.0µF without any ESR requirement is required at the LP3985 input, while a 1.0µF ceramic capacitor with an ESR requirement of 5mΩ to 500mΩ is required at the output. Careful interpretation and understanding of the capacitor specification is required to ensure correct device operation.

LP2980

The LP2980 is an ultra low dropout regulator with a 0.5% or 1.0% accuracy over temperature, depending upon grade. It is available in 3.0V, 3.3V and 5V versions, among others.

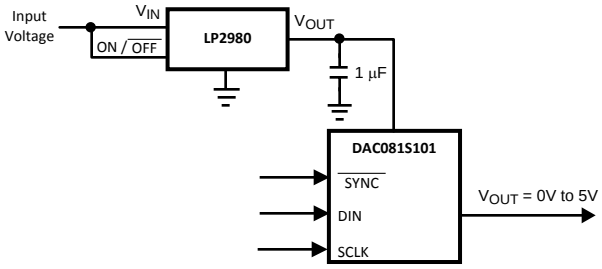


Figure 44. Using the LP2980 regulator

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Like any low dropout regulator, the LP2980 requires an output capacitor for loop stability. This output capacitor must be at least 1.0µF over temperature, but values of 2.2µF or more will provide even better performance. The ESR of this capacitor should be within the range specified in the LP2980 data sheet. Surface-mount solid tantalum capacitors offer a good combination of small size and ESR. Ceramic capacitors are attractive due to their small size but generally have ESR values that are too low for use with the LP2980. Aluminum electrolytic capacitors are typically not a good choice due to their large size and have ESR values that may be too high at low temperatures.

BIPOLAR OPERATION

The DAC081S101 is designed for single supply operation and thus has a unipolar output. However, a bipolar output may be obtained with the circuit in Figure 45. This circuit will provide an output voltage range of ±5 Volts. A rail-to-rail amplifier should be used if the amplifier supplies are limited to ±5V.

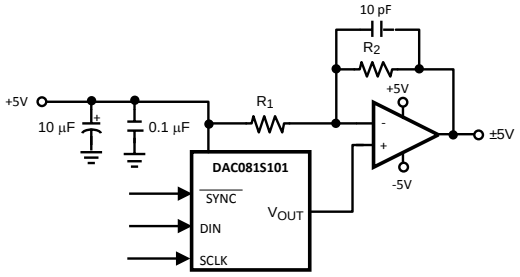


Figure 45. Bipolar Operation

The output voltage of this circuit for any code is found to be

$$V_O = (V_A \times (D / 256) \times ((R1 + R2) / R1) - V_A \times R2 / R1) \quad (5)$$

where D is the input code in decimal form. With V_A = 5V and R1 = R2,

$$V_O = (10 \times D / 256) - 5V \quad (6)$$

A list of rail-to-rail amplifiers suitable for this application are indicated in Table 3.

Table 3. Some Rail-to-Rail Amplifiers

AMP	PKGS	Typ V_{OS}	Typ I_{SUPPLY}
LMC7111	PDIP-8 SOT-23-5	0.9 mV	25 µA
LM7301	SO-8 SOT-23-5	0.03 mV	620 µA
LM8261	SOT-23-5	0.7 mV	1 mA

LAYOUT, GROUNDING, AND BYPASSING

For best accuracy and minimum noise, the printed circuit board containing the DAC081S101 should have separate analog and digital areas. The areas are defined by the locations of the analog and digital power planes. Both of these planes should be located in the same board layer. There should be a single ground plane. A single ground plane is preferred if digital return current does not flow through the analog ground area. Frequently a single ground plane design will utilize a "fencing" technique to prevent the mixing of analog and digital ground current. Separate ground planes should only be utilized when the fencing technique is inadequate. The separate ground planes must be connected in one place, preferably near the DAC081S101. Special care is required to guarantee that digital signals with fast edge rates do not pass over split ground planes. They must always have a continuous return path below their traces.

The DAC081S101 power supply should be bypassed with a 10µF and a 0.1µF capacitor as close as possible to the device with the 0.1µF right at the device supply pin. The 10µF capacitor should be a tantalum type and the 0.1µF capacitor should be a low ESL, low ESR type. The power supply for the DAC081S101 should only be used for analog circuits.

Avoid crossover of analog and digital signals and keep the clock and data lines on the component side of the board. The clock and data lines should have controlled impedances.

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REVISION HISTORY

Changes from Revision B (February 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	19

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DAC081S101CIMK/NO.A	Active	Production	SOT-23-THIN (DDC) | 6	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 105	X65C
DAC081S101CIMK/NO.B	Active	Production	SOT-23-THIN (DDC) | 6	1000 | SMALL T&R	-	Call TI	Call TI	-40 to 105	
DAC081S101CIMK/NOPB	Active	Production	SOT-23-THIN (DDC) | 6	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 105	X65C
DAC081S101CIMKX/NO.A	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 105	X65C
DAC081S101CIMKX/NO.B	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 105	
DAC081S101CIMKX/NOPB	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 105	X65C
DAC081S101CIMM/NO.A	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 105	X64C
DAC081S101CIMM/NO.B	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	-	Call TI	Call TI	-40 to 105	
DAC081S101CIMM/NOPB	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 105	X64C
DAC081S101CIMMX/NO.A	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 105	X64C
DAC081S101CIMMX/NO.B	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	-	Call TI	Call TI	-40 to 105	
DAC081S101CIMMX/NOPB	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 105	X64C

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

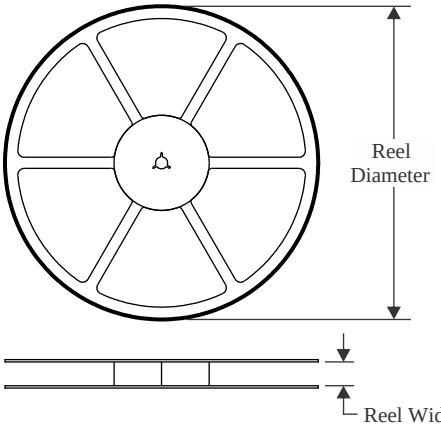
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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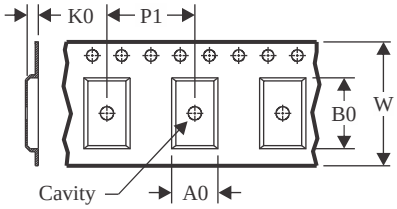
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

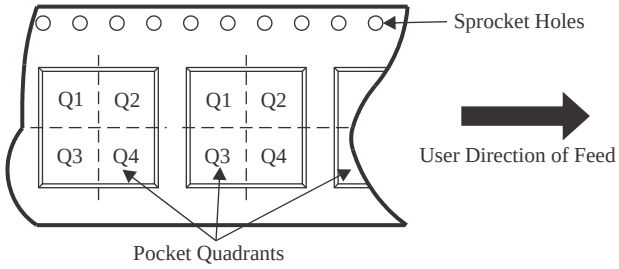


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

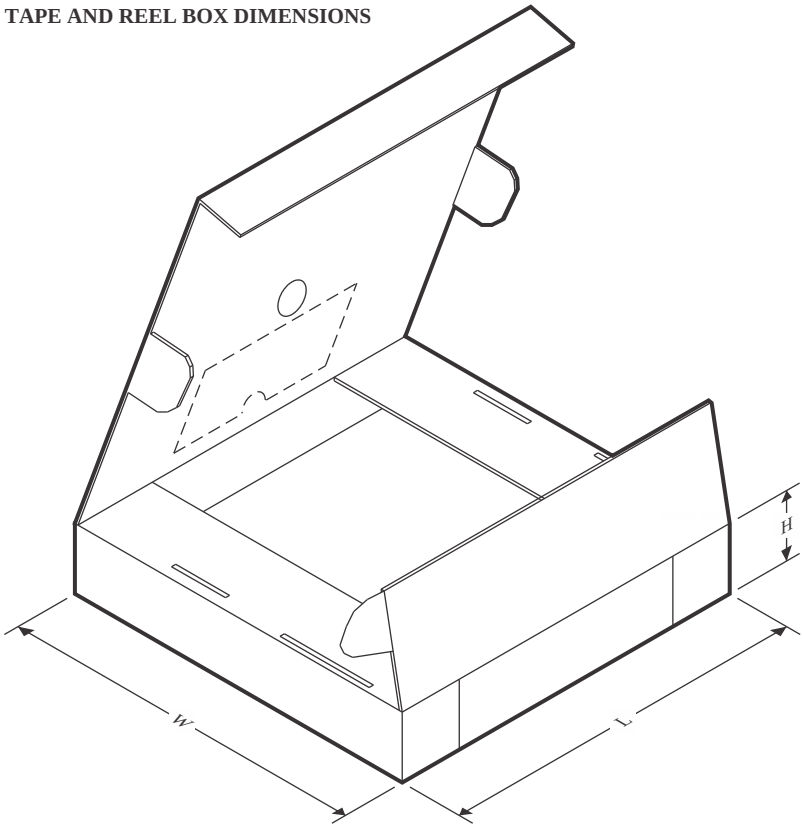
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC081S101CIMK/NOPB	SOT-23-THIN	DDC	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
DAC081S101CIMKX/NOPB	SOT-23-THIN	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
DAC081S101CIMM/NOPB	VSSOP	DGK	8	1000	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
DAC081S101CIMMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

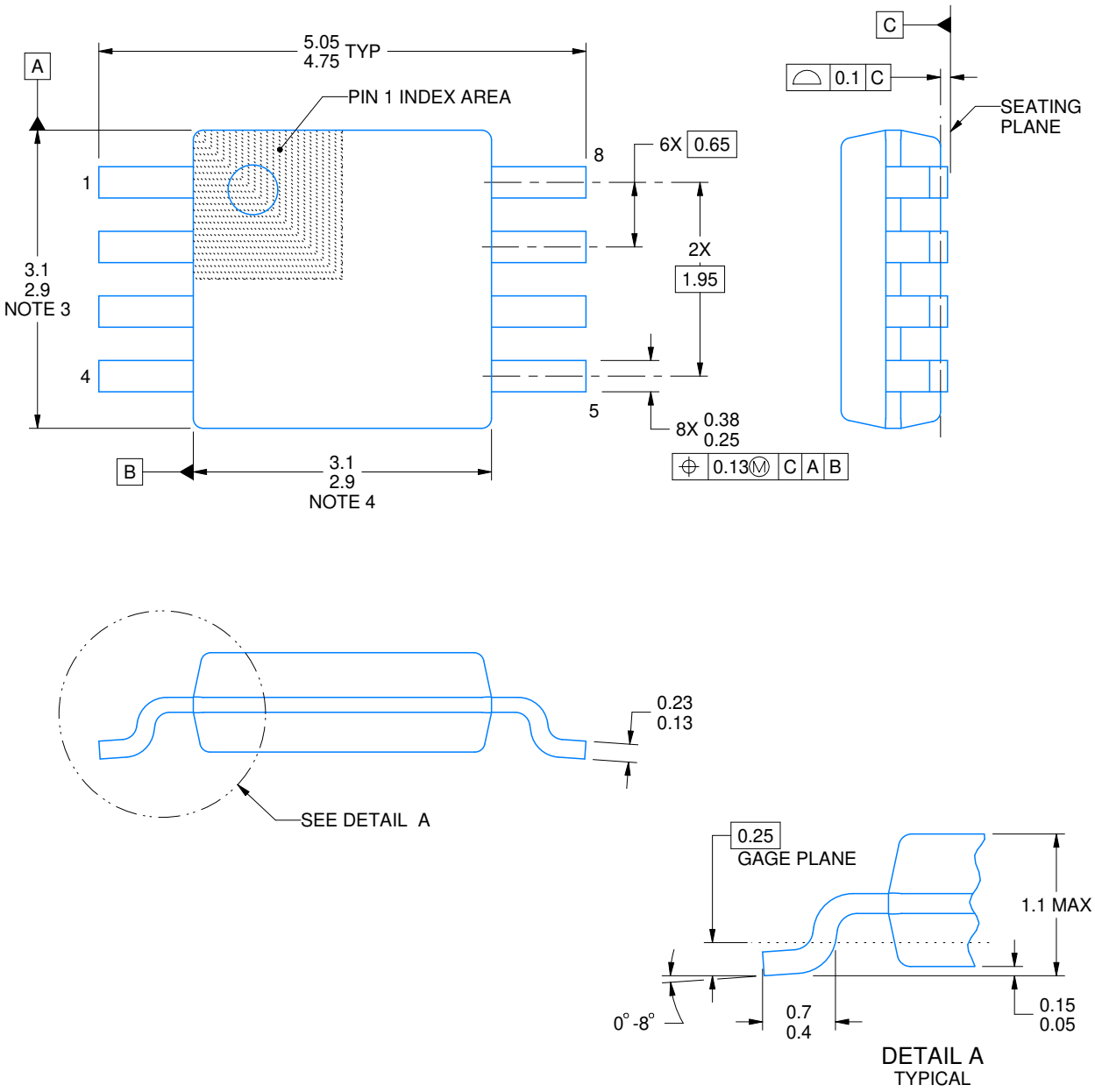
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC081S101CIMK/NOPB	SOT-23-THIN	DDC	6	1000	210.0	185.0	35.0
DAC081S101CIMKX/ NOPB	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0
DAC081S101CIMM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
DAC081S101CIMMX/ NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

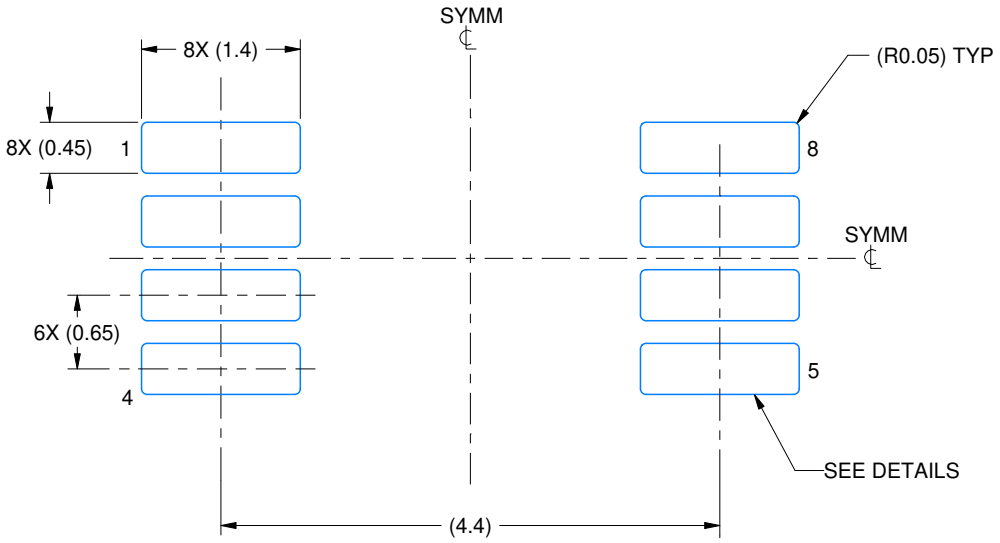


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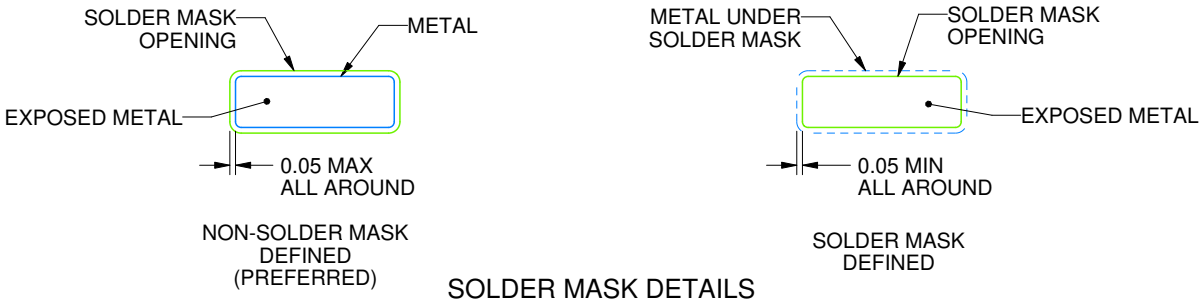
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

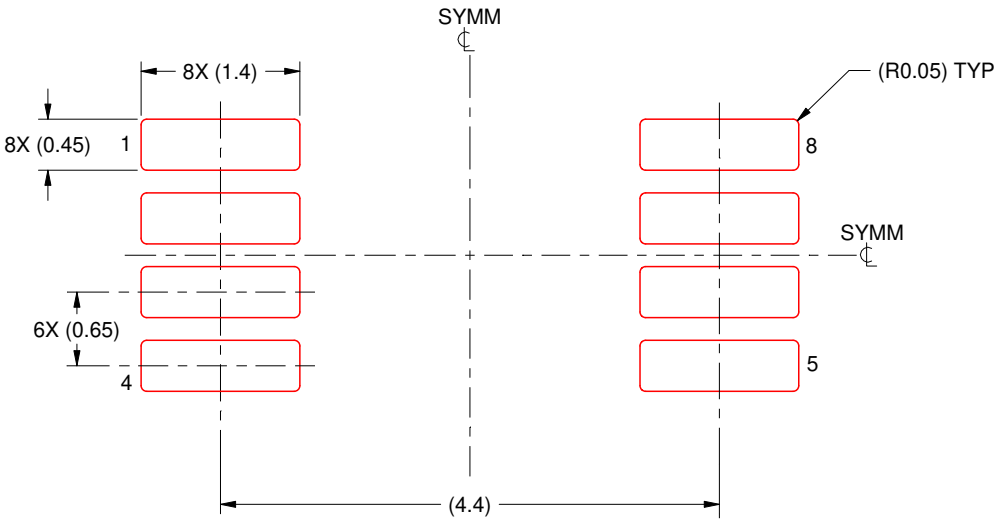


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

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NOTES: (continued)

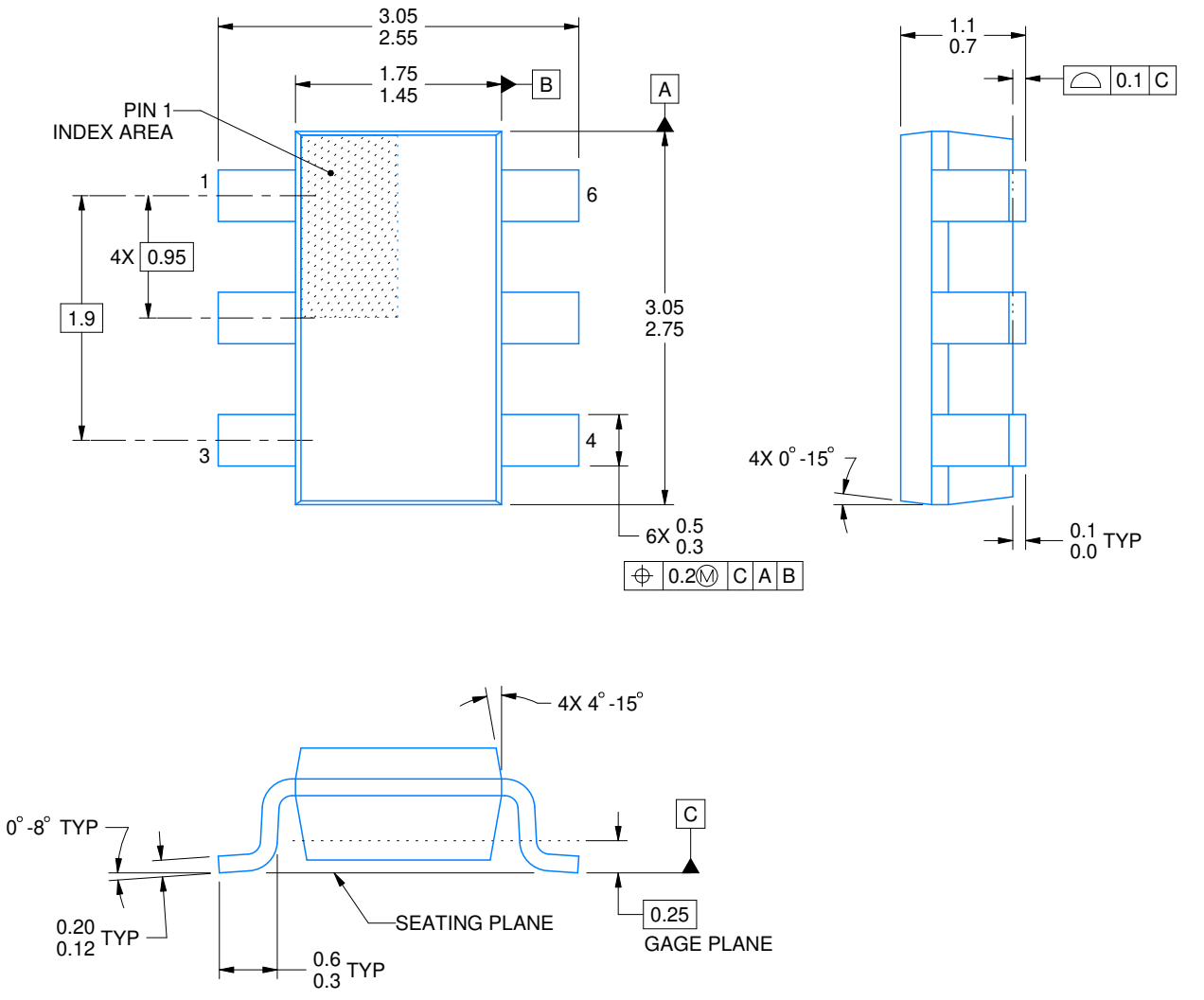
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DDC0006A

SOT-23 - 1.1 max height

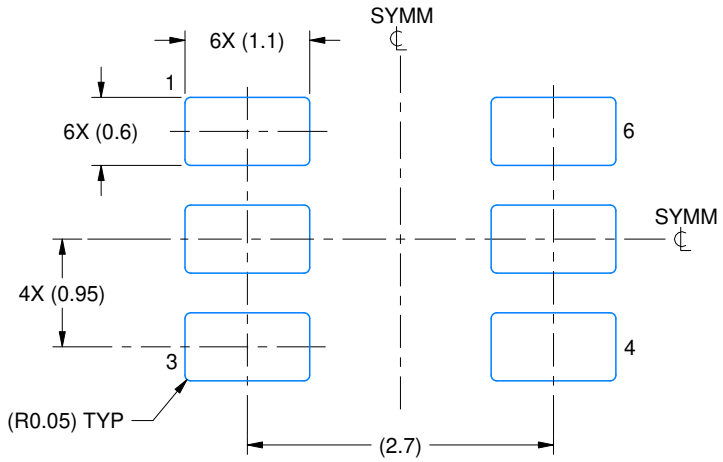
SMALL OUTLINE TRANSISTOR



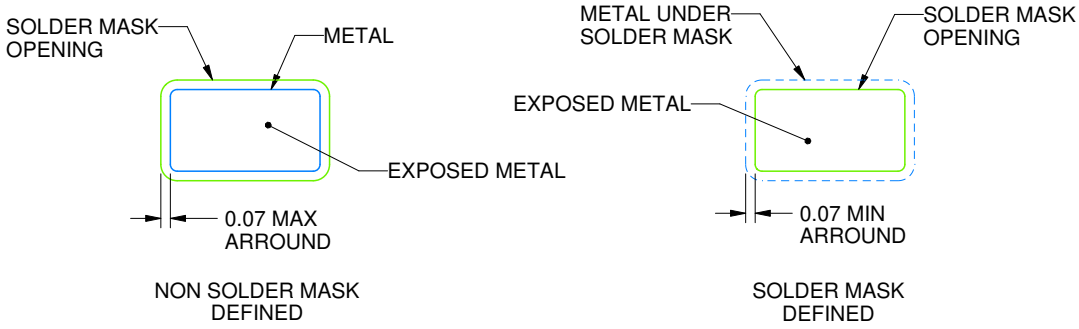
4214841/E 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X

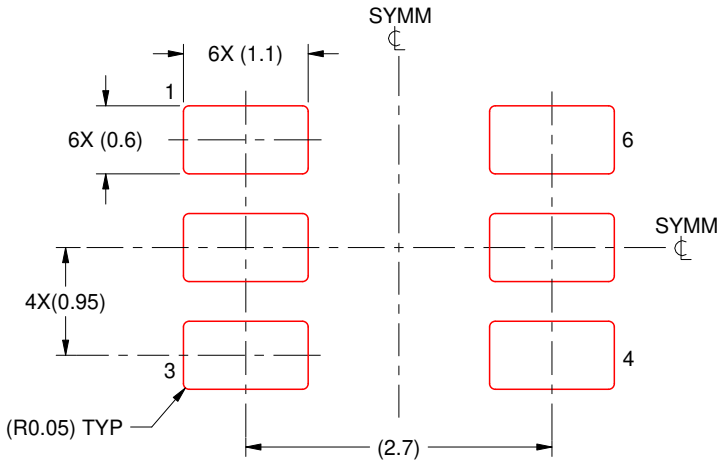


SOLDERMASK DETAILS

4214841/E 08/2024

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214841/E 08/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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