DAC108S085 10-Bit Micro Power OCTAL Digital-to-Analog Converter with Rail-to-Rail Outputs

Check for Samples: DAC108S085

FEATURES

- **Ensured Monotonicity**
- **Low Power Operation**
- **Rail-to-Rail Voltage Output**
- **Daisy Chain Capability**
- **Power-on Reset to 0V**
- **Simultaneous Output Updating**
- **Individual Channel Power Down Capability**
- **Wide power supply range (+2.7V to +5.5V)**
- **Dual Reference Voltages with Range of 0.5V to V_A**
- **Operating Temperature Range of −40°C to +125°C**
- **Industry's Smallest Package**

APPLICATIONS

- **Battery-Powered Instruments**
- **Digital Gain and Offset Adjustment**
- **Programmable Voltage & Current Sources**
- **Programmable Attenuators**
- **Voltage Reference for ADCs**
- **Sensor Supply Voltage**
- **Range Detectors**

KEY SPECIFICATIONS

- **Resolution: 10 Bits**
- **INL: ±2 LSB (Max)**
- **DNL: +0.35/-0.2 LSB (Max)**
- **Settling Time: 6 µs (Max)**
- **Zero Code Error : +15mV (Max)**
- **Full-Scale Error: -0.75% FSR (Max)**
- **Supply Power**
  - **Normal: 1.95 mW (3V)/4,85 mW (5V) (Typ)**
  - **Power Down: 0.3 µW (3V)/1 W (5V) (Typ)**

DESCRIPTION

The DAC108S085 is a full-featured, general purpose OCTAL 10-bit voltage-output digital-to-analog converter (DAC) that can operate from a single +2.7V to +5.5V supply and consumes 1.95 mW at 3V and 4.85 mW at 5V. The DAC108S085 is packaged in a 16-lead WQFN package and a 16-lead TSSOP package. The WQFN package makes the DAC108S085 the smallest OCTAL DAC in its class. The on-chip output amplifiers allow rail-to-rail output swing and the three wire serial interface operates at clock rates up to 40 MHz over the entire supply voltage range. Competitive devices are limited to 25 MHz clock rates at supply voltages in the 2.7V to 3.6V range. The serial interface is compatible with standard SPI™, QSPI, MICROWIRE and DSP interfaces. The DAC108S085 also offers daisy chain operation where an unlimited number of DAC108S085s can be updated simultaneously using a single serial interface.

There are two references for the DAC108S085. One reference input serves channels A through D while the other reference serves channels E through H. Each reference can be set independently between 0.5V and V_A, providing the widest possible output dynamic range. The DAC108S085 has a 16-bit input shift register that controls the mode of operation, the power-down condition, and the DAC channels' register/output value. All eight DAC outputs can be updated simultaneously or individually.

A power-on reset circuit ensures that the DAC outputs power up to zero volts and remain there until there is a valid write to the device. The power-down feature of the DAC108S085 allows each DAC to be independently powered with three different termination options. With all the DAC channels powered down, power consumption reduces to less than 0.3 µW at 3V and less than 1 µW at 5V. The low power consumption and small packages of the DAC108S085 make it an excellent choice for use in battery operated equipment.

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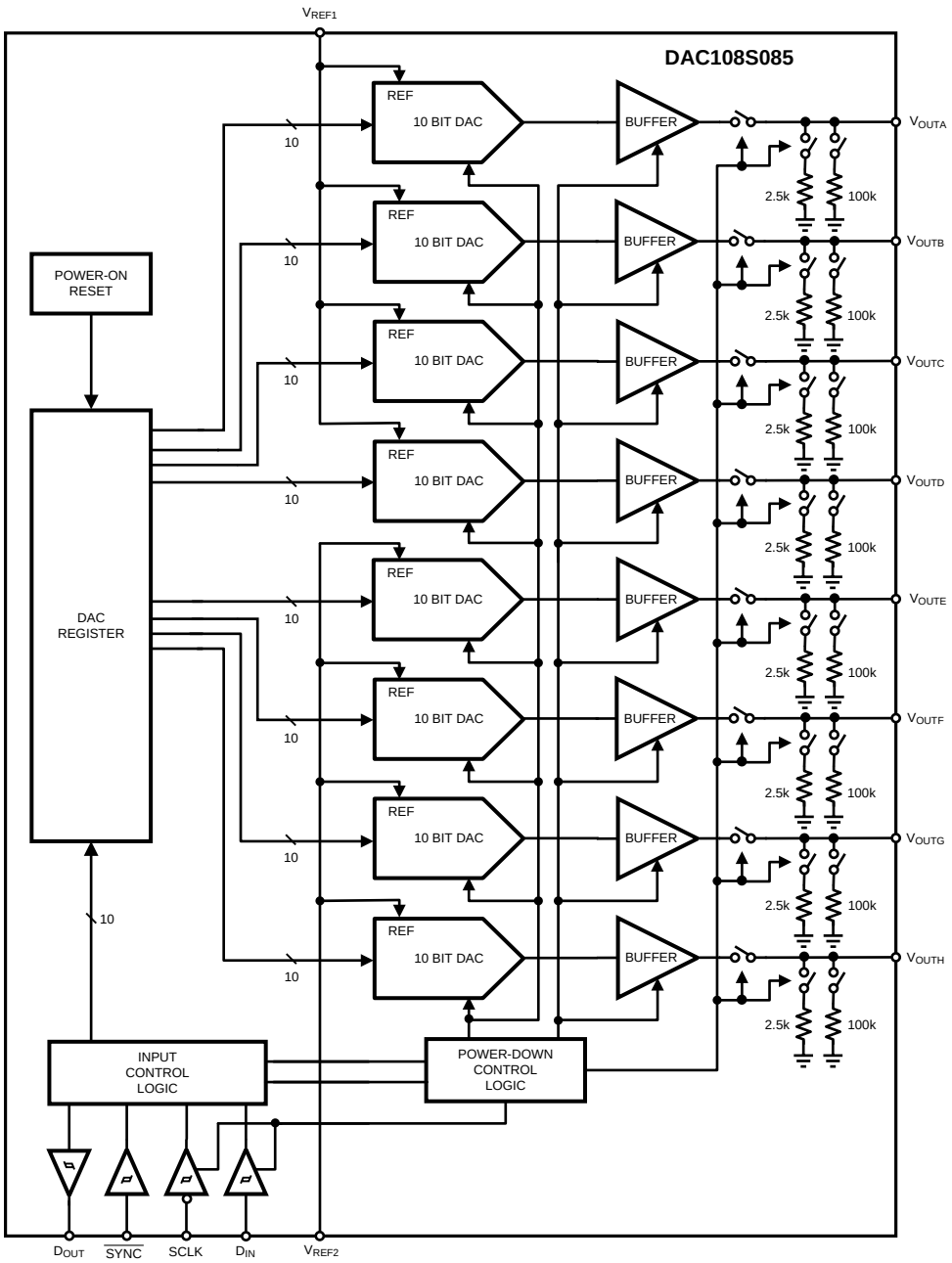
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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DESCRIPTION (CONTINUED)

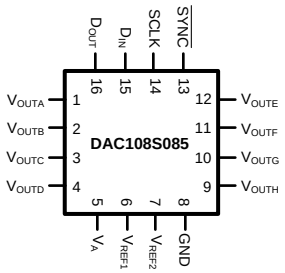
The DAC108S085 is one of a family of pin compatible DACs, including the 8-bit DAC088S085 and the 12-bit DAC128S085. All three parts are offered with the same pinout, allowing system designers to select a resolution appropriate for their application without redesigning their printed circuit board. The DAC108S085 operates over the extended industrial temperature range of −40°C to +125°C.

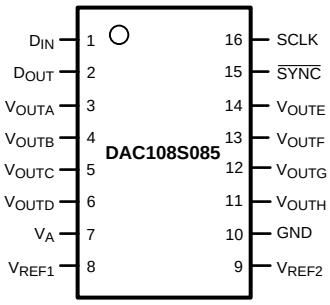
Block Diagram



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Pin Configuration





PIN DESCRIPTIONS

WQFN Pin No.	TSSOP Pin No.	Symbol	Type	Description
1	3	V_{OUTA}	Analog Output	Channel A Analog Output Voltage.
2	4	V_{OUTB}	Analog Output	Channel B Analog Output Voltage.
3	5	V_{OUTC}	Analog Output	Channel C Analog Output Voltage.
4	6	V_{OUTD}	Analog Output	Channel D Analog Output Voltage.
5	7	V_A	Supply	Power supply input. Must be decoupled to GND.
6	8	V_{REF1}	Analog Input	Unbuffered reference voltage shared by Channels A, B, C, and D. Must be decoupled to GND.
7	9	V_{REF2}	Analog Input	Unbuffered reference voltage shared by Channels E, F, G, and H. Must be decoupled to GND.
8	10	GND	Ground	Ground reference for all on-chip circuitry.
9	11	V_{OUTH}	Analog Output	Channel H Analog Output Voltage.
10	12	V_{OUTG}	Analog Output	Channel G Analog Output Voltage.
11	13	V_{OUTF}	Analog Output	Channel F Analog Output Voltage.
12	14	V_{OUTE}	Analog Output	Channel E Analog Output Voltage.
13	15	$\overline{SYNC}$	Digital Input	Frame Synchronization Input. When this pin goes low, data is written into the DAC's input shift register on the falling edges of SCLK. After the 16th falling edge of SCLK, a rising edge of $\overline{SYNC}$ causes the DAC to be updated. If $\overline{SYNC}$ is brought high before the 15th falling edge of SCLK, the rising edge of $\overline{SYNC}$ acts as an interrupt and the write sequence is ignored by the DAC.
14	16	SCLK	Digital Input	Serial Clock Input. Data is clocked into the input shift register on the falling edges of this pin.
15	1	D_{IN}	Digital Input	Serial Data Input. Data is clocked into the 16-bit shift register on the falling edges of SCLK after the fall of $\overline{SYNC}$.
16	2	D_{OUT}	Digital Output	Serial Data Output. D_{OUT} is utilized in daisy chain operation and is connected directly to a D_{IN} pin on another DAC108S085. Data is not available at D_{OUT} unless $\overline{SYNC}$ remains low for more than 16 SCLK cycles.
17		PAD (WQFN only)	Ground	Exposed die attach pad can be connected to ground or left floating. Soldering the pad to the PCB offers optimal thermal performance and enhances package self-alignment during reflow.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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Absolute Maximum Ratings (1) (2) (3)

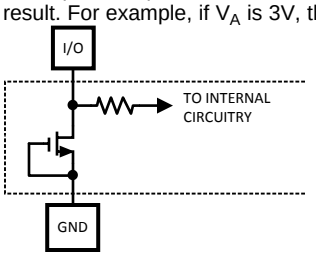
Supply Voltage, V_A		6.5V
Voltage on any Input Pin		−0.3V to 6.5V
Input Current at Any Pin (4)		10 mA
Package Input Current (4)		30 mA
Power Consumption at T_A = 25°C		See (5)
ESD Susceptibility (6)	Human Body Model	2500V
	Machine Model	250V
	Charge Device Mode	1000V
Junction Temperature		+150°C
Storage Temperature		−65°C to +150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not specify specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions. Operation of the device beyond the maximum Operating Ratings is not recommended.
(2) All voltages are measured with respect to GND = 0V, unless otherwise specified.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(4) When the input voltage at any pin exceeds 5.5V or is less than GND, the current at that pin should be limited to 10 mA. The 30 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 10 mA to three.
(5) The absolute maximum junction temperature ($T_J$max) for this device is 150°C. The maximum allowable power dissipation is dictated by $T_J$max, the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature (T_A), and can be calculated using the formula $P_D MAX = (T_J max - T_A) / \theta_{JA}$. The values for maximum power dissipation will be reached only when the device is operated in a severe fault condition (e.g., when input or output pins are driven beyond the operating ratings, or the power supply polarity is reversed). Such conditions should always be avoided.
(6) Human body model is 100 pF capacitor discharged through a 1.5 kΩ resistor. Machine model is 220 pF discharged through 0 Ω. Charge device model simulates a pin slowly acquiring charge (such as from a device sliding down the feeder in an automated assembler) then rapidly being discharged.

Operating Ratings (1) (2)

Operating Temperature Range	−40°C ≤ T_A ≤ +125°C
Supply Voltage, V_A	+2.7V to 5.5V
Reference Voltage, $V_{REF1,2}$	+0.5V to V_A
Digital Input Voltage (3)	0.0V to 5.5V
Output Load	0 to 1500 pF
SCLK Frequency	Up to 40 MHz

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not specify specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions. Operation of the device beyond the maximum Operating Ratings is not recommended.
(2) All voltages are measured with respect to GND = 0V, unless otherwise specified.
(3) The inputs are protected as shown below. Input voltage magnitudes up to 5.5V, regardless of V_A, will not cause errors in the conversion result. For example, if V_A is 3V, the digital input pins can be driven with a 5V logic device.



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Package Thermal Resistances[1][2]

Package	θ_{JA}
16-Lead WQFN	38°C/W
16-Lead TSSOP	130°C/W

(1) Soldering process must comply with Texas Instruments' Reflow Temperature Profile specifications. Refer to http://www.ti.com/packaging.
(2) Reflow temperature profiles are different for lead-free packages.

Electrical Characteristics

The following specifications apply for V_A = +2.7V to +5.5V, $V_{REF1} = V_{REF2} = V_A$, C_L = 200 pF to GND, f_{SCLK} = 30 MHz, input code range 12 to 1011. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$** and all other limits are at T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Typical	Limits[1]	Units (Limits)
STATIC PERFORMANCE					
	Resolution			**10**	Bits (min)
	Monotonicity			**10**	Bits (min)
INL	Integral Non-Linearity		±0.5	**±2**	LSB (max)
DNL	Differential Non-Linearity		+0.08	**+0.35**	LSB (max)
			−0.04	**−0.2**	LSB (min)
ZE	Zero Code Error	I_{OUT} = 0	+5	**+15**	mV (max)
FSE	Full-Scale Error	I_{OUT} = 0	−0.1	**−0.75**	% FSR (max)
GE	Gain Error		−0.2	**−1.0**	% FSR (max)
ZCED	Zero Code Error Drift		−20		µV/°C
TC GE	Gain Error Tempco		−1.0		ppm/°C
OUTPUT CHARACTERISTICS					
	Output Voltage Range			**0** **$V_{REF1,2}$**	V (min) V (max)
I_{OZ}	High-Impedance Output Leakage Current[2]			**±1**	µA (max)
ZCO	Zero Code Output	V_A = 3V, I_{OUT} = 200 µA	10		mV
		V_A = 3V, I_{OUT} = 1 mA	45		mV
		V_A = 5V, I_{OUT} = 200 µA	8		mV
		V_A = 5V, I_{OUT} = 1 mA	34		mV
FSO	Full Scale Output	V_A = 3V, I_{OUT} = 200 µA	2.984		V
		V_A = 3V, I_{OUT} = 1 mA	2.933		V
		V_A = 5V, I_{OUT} = 200 µA	4.987		V
		V_A = 5V, I_{OUT} = 1 mA	4.955		V
I_{OS}	Output Short Circuit Current (source)[3]	V_A = 3V, V_{OUT} = 0V, Input Code = 3FFh	−50		mA
		V_A = 5V, V_{OUT} = 0V, Input Code = 3FFh	−60		mA
I_{OS}	Output Short Circuit Current (sink)[3]	V_A = 3V, V_{OUT} = 3V, Input Code = 000h	50		mA
		V_A = 5V, V_{OUT} = 5V, Input Code = 000h	70		mA
I_O	Continuous Output Current per channel[2]	T_A = 105°C		**10**	mA (max)
		T_A = 125°C		**6.5**	mA (max)
C_L	Maximum Load Capacitance	R_L = ∞	1500		pF
		R_L = 2kΩ	1500		pF
Z_{OUT}	DC Output Impedance		8		Ω

(1) Test limits are specified to AOQL (Average Outgoing Quality Level).
(2) This parameter is specified by design and/or characterization and is not tested in production.
(3) This parameter does not represent a condition which the DAC can sustain continuously. See the continuous output current specification for the maximum DAC output current per channel.

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Electrical Characteristics (continued)

The following specifications apply for V_A = +2.7V to +5.5V, V_{REF1} = V_{REF2} = V_A, C_L = 200 pF to GND, f_{SCLK} = 30 MHz, input code range 12 to 1011. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$** and all other limits are at T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions		Typical	Limits[1]	Units (Limits)
REFERENCE INPUT CHARACTERISTICS						
VREF1,2	Input Range Minimum			0.5	**2.7**	V (min)
	Input Range Maximum				**V_A**	V (max)
	Input Impedance			30		kΩ
LOGIC INPUT CHARACTERISTICS						
I_{IN}	Input Current[4]				**±1**	µA (max)
V_{IL}	Input Low Voltage	V_A = 2.7V to 3.6V		1.0	**0.6**	V (max)
		V_A = 4.5V to 5.5V		1.1	**0.8**	V (max)
V_{IH}	Input High Voltage	V_A = 2.7V to 3.6V		1.4	**2.1**	V (min)
		V_A = 4.5V to 5.5V		2.0	**2.4**	V (min)
C_{IN}	Input Capacitance[4]				**3**	pF (max)
POWER REQUIREMENTS						
V_A	Supply Voltage Minimum				**2.7**	V (min)
	Supply Voltage Maximum				**5.5**	V (max)
I_N	Normal Supply Current for supply pin V_A	f_{SCLK} = 30 MHz, output unloaded	V_A = 2.7V to 3.6V	460	**585**	µA (max)
			V_A = 4.5V to 5.5V	650	**855**	µA (max)
	Normal Supply Current for V_{REF1} or V_{REF2}	f_{SCLK} = 30 MHz, output unloaded	V_A = 2.7V to 3.6V	95	**135**	µA (max)
			V_A = 4.5V to 5.5V	160	**225**	µA (max)
I_{ST}	Static Supply Current for supply pin V_A	f_{SCLK} = 0, output unloaded	V_A = 2.7V to 3.6V	370		µA
			V_A = 4.5V to 5.5V	440		µA
	Static Supply Current for V_{REF1} or V_{REF2}	f_{SCLK} = 0, output unloaded	V_A = 2.7V to 3.6V	95		µA
			V_A = 4.5V to 5.5V	160		µA
I_{PD}	Total Power Down Supply Current for all PD Modes[4]	f_{SCLK} = 30 MHz, SYNC = V_A and D_{IN} = 0V after PD mode loaded	V_A = 2.7V to 3.6V	0.2	**1.5**	µA (max)
			V_A = 4.5V to 5.5V	0.5	**3.0**	µA (max)
		f_{SCLK} = 0, SYNC = V_A and D_{IN} = 0V after PD mode loaded	V_A = 2.7V to 3.6V	0.1	**1.0**	µA (max)
			V_A = 4.5V to 5.5V	0.2	**2.0**	µA (max)
P_N	Total Power Consumption (output unloaded)	f_{SCLK} = 30 MHz output unloaded	V_A = 2.7V to 3.6V	1.95	**3.1**	mW (max)
			V_A = 4.5V to 5.5V	4.85	**7.2**	mW (max)
		f_{SCLK} = 0 output unloaded	V_A = 2.7V to 3.6V	1.68		mW
			V_A = 4.5V to 5.5V	3.80		mW
P_{PD}	Total Power Consumption in all PD Modes[4]	f_{SCLK} = 30 MHz, SYNC = V_A and D_{IN} = 0V after PD mode loaded	V_A = 2.7V to 3.6V	0.6	**5.4**	µW (max)
			V_A = 4.5V to 5.5V	2.5	**16.5**	µW (max)
		f_{SCLK} = 0, SYNC = V_A and D_{IN} = 0V after PD mode loaded	V_A = 2.7V to 3.6V	0.3	**3.6**	µW (max)
			V_A = 4.5V to 5.5V	1	**11**	µW (max)

(4) This parameter is specified by design and/or characterization and is not tested in production.

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A.C. and Timing Characteristics

The following specifications apply for V_A = +2.7V to +5.5V, $V_{REF1,2} = V_A$, C_L = 200 pF to GND, f_{SCLK} = 30 MHz, input code range 12 to 1011. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$** and all other limits are at T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conductions	Typical	Limits (1)	Units (Limits)
f_{SCLK}	SCLK Frequency		40	**30**	MHz (max)
t_s	Output Voltage Settling Time (2)	100h to 300h code change R_L = 2kΩ, C_L = 200 pF	4.5	**6.0**	µs (max)
SR	Output Slew Rate		1		V/µs
GI	Glitch Impulse	Code change from 200h to 1FFh	40		nV-sec
DF	Digital Feedthrough		0.5		nV-sec
DC	Digital Crosstalk		0.5		nV-sec
CROSS	DAC-to-DAC Crosstalk		1		nV-sec
MBW	Multiplying Bandwidth	$V_{REF1,2}$ = 2.5V ± 2Vpp	360		kHz
ONSD	Output Noise Spectral Density	DAC Code = 200h, 10kHz	40		nV/sqrt(Hz)
ON	Output Noise	BW = 30kHz	14		µV
t_{WU}	Wake-Up Time	V_A = 3V	3		µsec
		V_A = 5V	20		µsec
$1/f_{SCLK}$	SCLK Cycle Time		25	**33**	ns (min)
t_{CH}	SCLK High time		7	**10**	ns (min)
t_{CL}	SCLK Low Time		7	**10**	ns (min)
t_{SS}	$\overline{SYNC}$ Set-up Time prior to SCLK Falling Edge		3	**10**	ns (min)
				$1 / f_{SCLK}$ - 3	ns (max)
t_{DS}	Data Set-Up Time prior to SCLK Falling Edge		1.0	**2.5**	ns (min)
t_{DH}	Data Hold Time after SCLK Falling Edge		1.0	**2.5**	ns (min)
t_{SH}	SYNC Hold Time after the 16th falling edge of SCLK		0	**3**	ns (min)
				$1 / f_{SCLK}$ - 3	ns (max)
t_{SYNC}	$\overline{SYNC}$ High Time		5	**15**	ns (min)

(1) Test limits are specified to AOQL (Average Outgoing Quality Level).
(2) This parameter is specified by design and/or characterization and is not tested in production.

Timing Diagrams

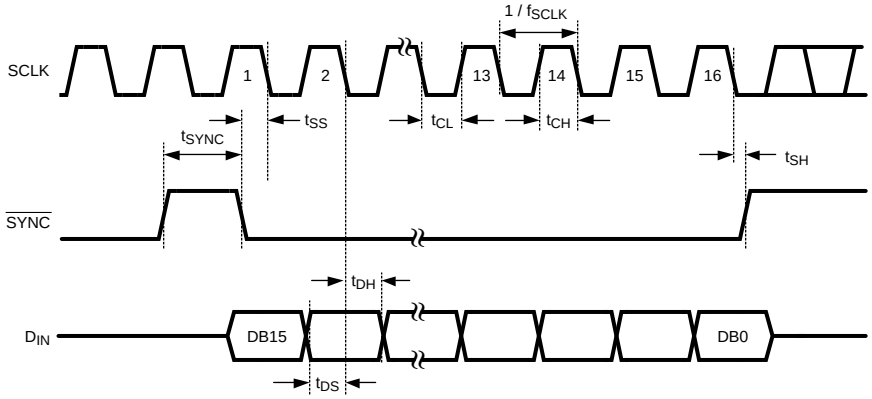


Figure 1. Serial Timing Diagram

Specification Definitions

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB, which is V_{REF} / 1024 = V_A / 1024.

DAC-to-DAC CROSSTALK is the glitch impulse transferred to a DAC output in response to a full-scale change in the output of another DAC.

DIGITAL CROSSTALK is the glitch impulse transferred to a DAC output at mid-scale in response to a full-scale change in the input register of another DAC.

DIGITAL FEEDTHROUGH is a measure of the energy injected into the analog output of the DAC from the digital inputs when the DAC outputs are not updated. It is measured with a full-scale code change on the data bus.

FULL-SCALE ERROR is the difference between the actual output voltage with a full scale code (3FFh) loaded into the DAC and the value of V_A x 1023 / 1024.

GAIN ERROR is the deviation from the ideal slope of the transfer function. It can be calculated from Zero and Full-Scale Errors as GE = FSE - ZE, where GE is Gain error, FSE is Full-Scale Error and ZE is Zero Error.

GLITCH IMPULSE is the energy injected into the analog output when the input code to the DAC register changes. It is specified as the area of the glitch in nanovolt-seconds.

INTEGRAL NON-LINEARITY (INL) is a measure of the deviation of each individual code from a straight line through the input to output transfer function. The deviation of any given code from this straight line is measured from the center of that code value. The end point method is used. INL for this product is specified over a limited range, per the Electrical Tables.

LEAST SIGNIFICANT BIT (LSB) is the bit that has the smallest value or weight of all bits in a word. This value is

$$LSB = V_{REF} / 2^n \quad (1)$$

where V_{REF} is the supply voltage for this product, and "n" is the DAC resolution in bits, which is 10 for the DAC108S085.

MAXIMUM LOAD CAPACITANCE is the maximum capacitance that can be driven by the DAC with output stability maintained.

MONOTONICITY is the condition of being monotonic, where the DAC has an output that never decreases when the input code increases.

MOST SIGNIFICANT BIT (MSB) is the bit that has the largest value or weight of all bits in a word. Its value is 1/2 of V_A.

MULTIPLYING BANDWIDTH is the frequency at which the output amplitude falls 3dB below the input sine wave on $V_{REF1,2}$ with the DAC code at full-scale.

NOISE SPECTRAL DENSITY is the internally generated random noise. It is measured by loading the DAC to mid-scale and measuring the noise at the output.

POWER EFFICIENCY is the ratio of the output current to the total supply current. The output current comes from the power supply. The difference between the supply and output currents is the power consumed by the device without a load.

SETTLING TIME is the time for the output to settle to within 1/2 LSB of the final value after the input code is updated.

TOTAL HARMONIC DISTORTION PLUS NOISE (THD+N) is the ratio of the harmonics plus the noise present at the output of the DACs to the rms level of an ideal sine wave applied to $V_{REF1,2}$ with the DAC code at mid-scale.

WAKE-UP TIME is the time for the output to exit power-down mode. This is the time from the rising edge of $\overline{SYNC}$ to when the output voltage deviates from the power-down voltage of 0V.

ZERO CODE ERROR is the output error, or voltage, present at the DAC output after a code of 000h has been entered.

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Transfer Characteristic

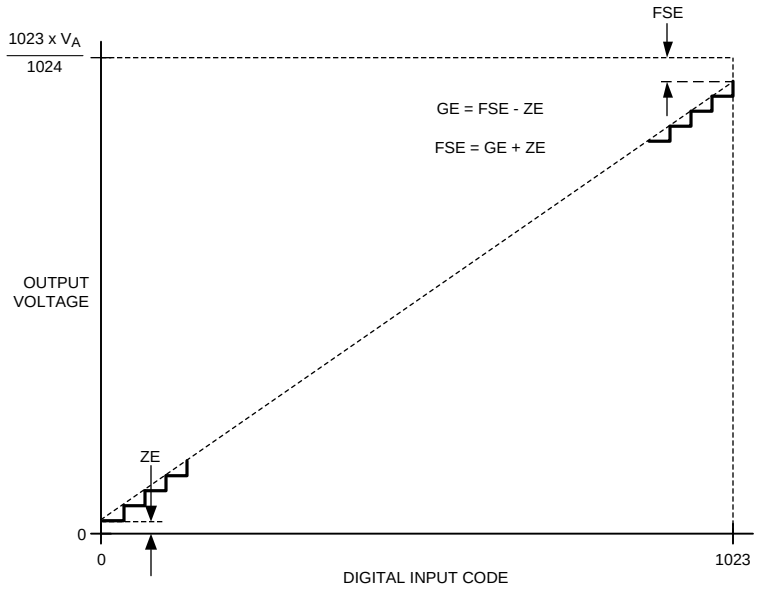


Figure 2. Input / Output Transfer Characteristic

Typical Performance Characteristics

V_A = +2.7V to +5.5V, $V_{REF1,2} = V_A$, f_{SCLK} = 30 MHz, T_A = 25°C, unless otherwise stated

INL vs Code

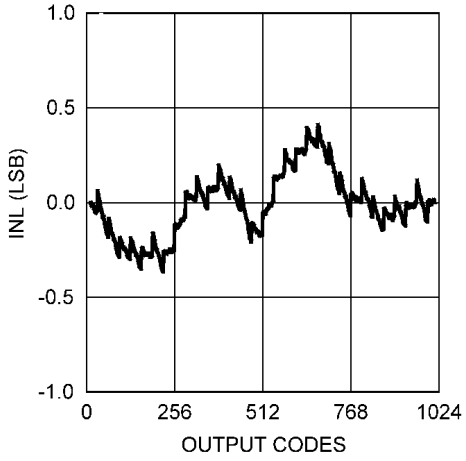


Figure 3.

DNL vs Code

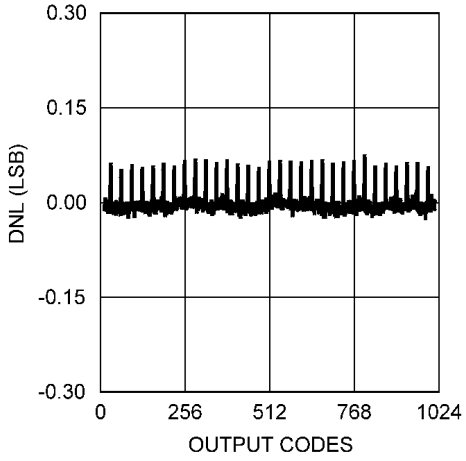


Figure 4.

INL/DNL vs V_{REF}

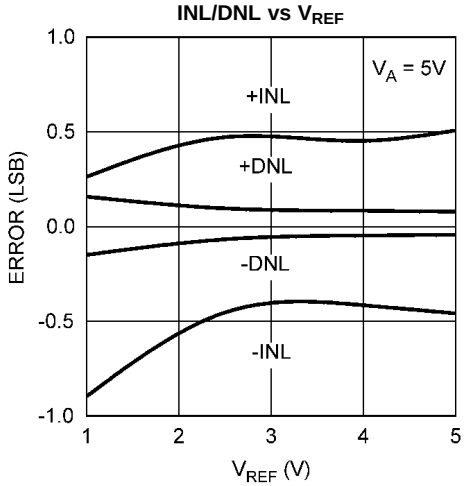


Figure 5.

INL/DNL vs f_{SCLK}

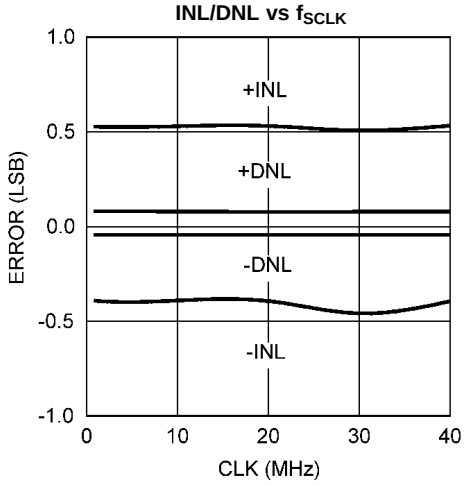


Figure 6.

INL/DNL vs V_A

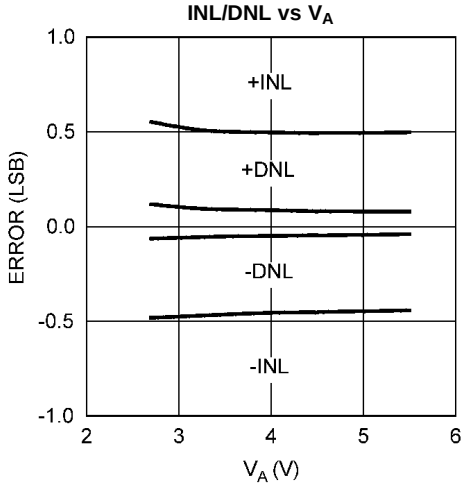


Figure 7.

INL/DNL vs Temperature

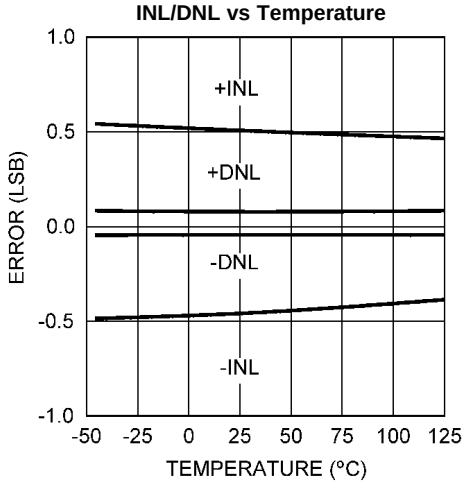


Figure 8.

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Typical Performance Characteristics (continued)

V_A = +2.7V to +5.5V, $V_{REF1,2} = V_A$, f_{SCLK} = 30 MHz, T_A = 25°C, unless otherwise stated

Zero Code Error vs. V_A

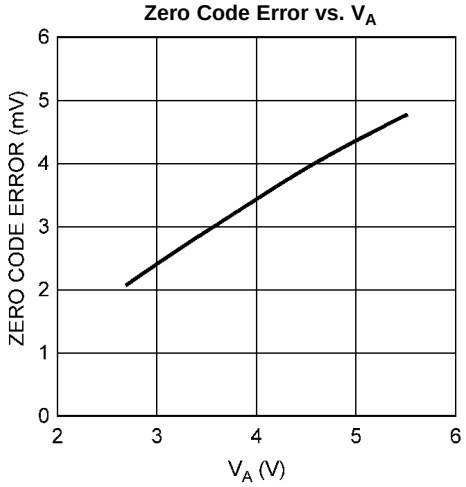


Figure 9.

Zero Code Error vs. V_{REF}

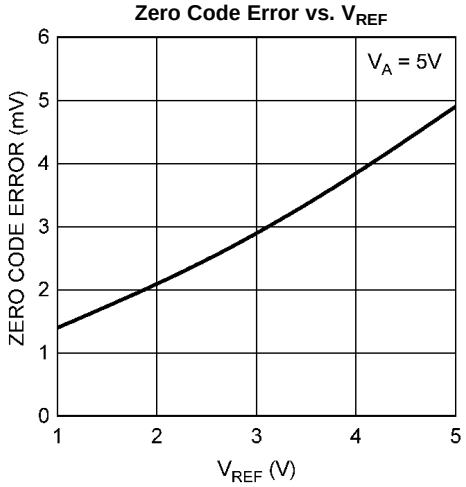


Figure 10.

Zero Code Error vs. f_{SCLK}

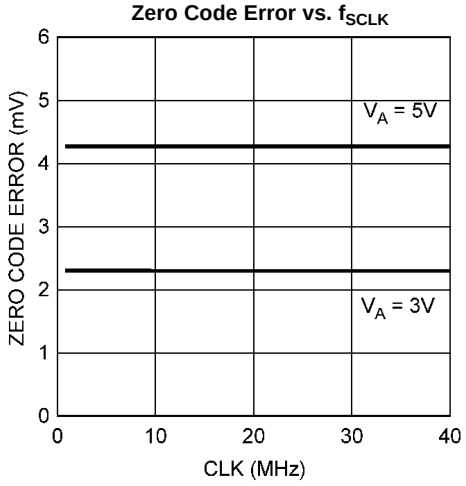


Figure 11.

Zero Code Error vs. Temperature

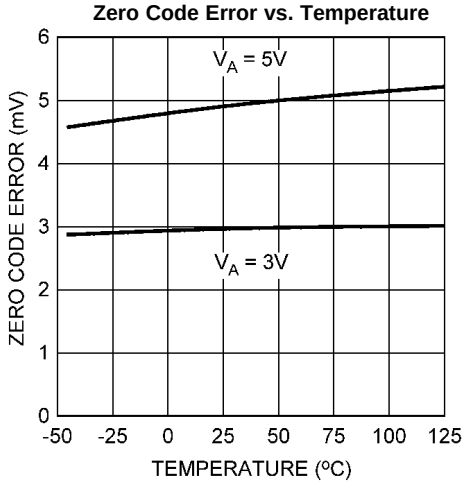


Figure 12.

Full-Scale Error vs. V_A

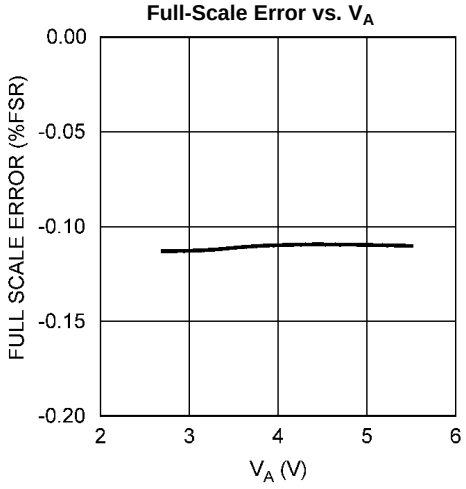


Figure 13.

Full-Scale Error vs. V_{REF}

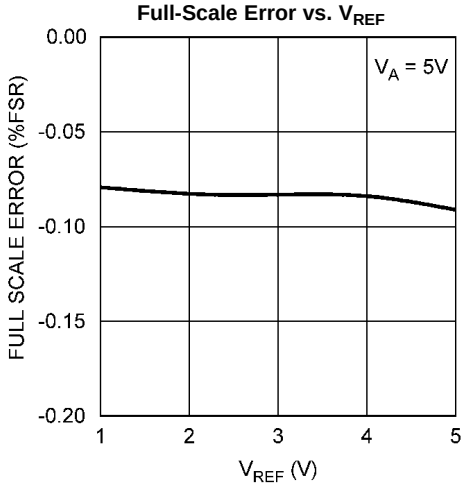


Figure 14.

Typical Performance Characteristics (continued)

V_A = +2.7V to +5.5V, $V_{REF1,2} = V_A$, f_{SCLK} = 30 MHz, T_A = 25°C, unless otherwise stated

Full-Scale Error vs. f_{SCLK}

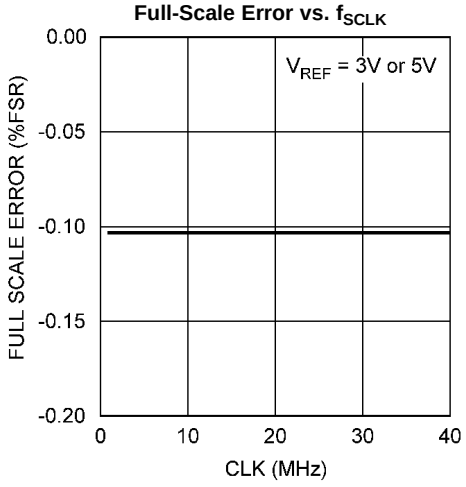


Figure 15.

Full-Scale Error vs. Temperature

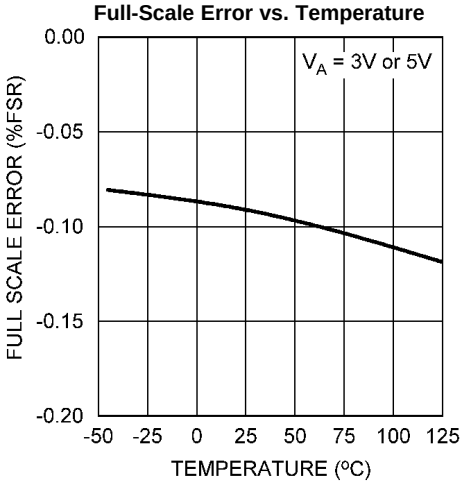


Figure 16.

I_{VA} vs. V_A

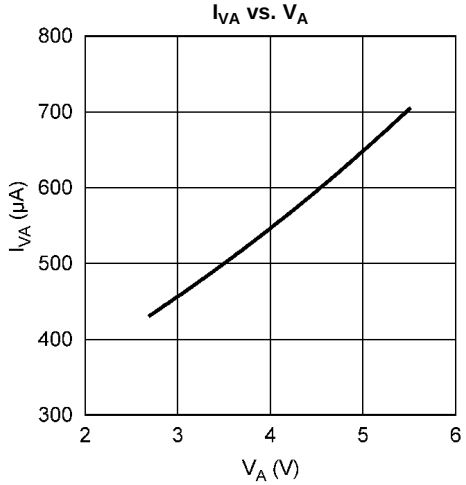


Figure 17.

I_{VA} vs. Temperature

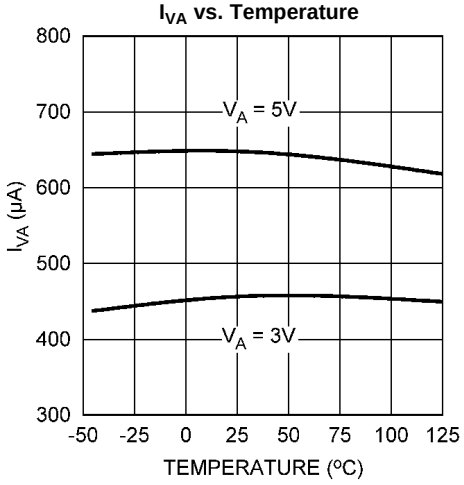


Figure 18.

I_{VREF} vs. V_{REF}

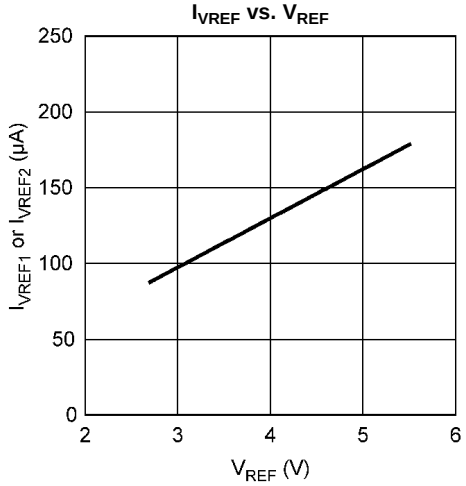


Figure 19.

I_{VREF} vs. Temperature

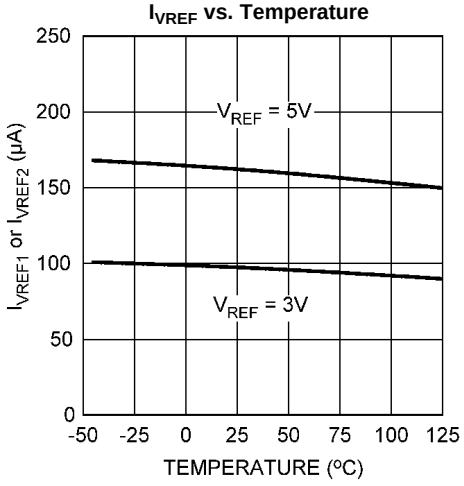


Figure 20.

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Typical Performance Characteristics (continued)

V_A = +2.7V to +5.5V, $V_{REF1,2} = V_A$, f_{SCLK} = 30 MHz, T_A = 25°C, unless otherwise stated

Settling Time

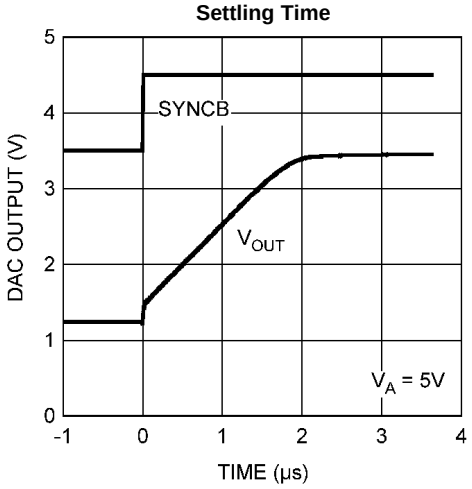


Figure 21.

Glitch Response

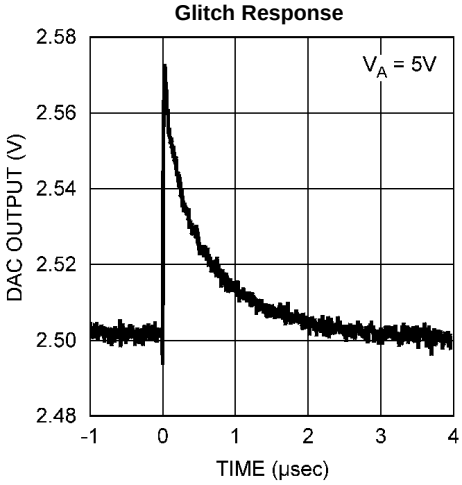


Figure 22.

Wake-Up Time

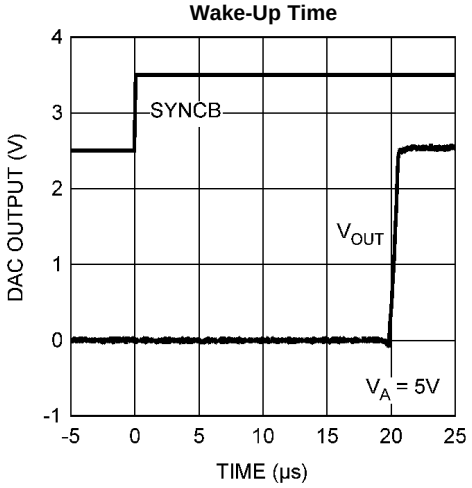


Figure 23.

DAC-to-DAC Crosstalk

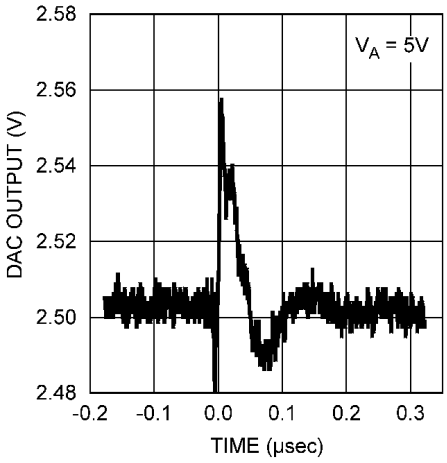


Figure 24.

Power-On Reset

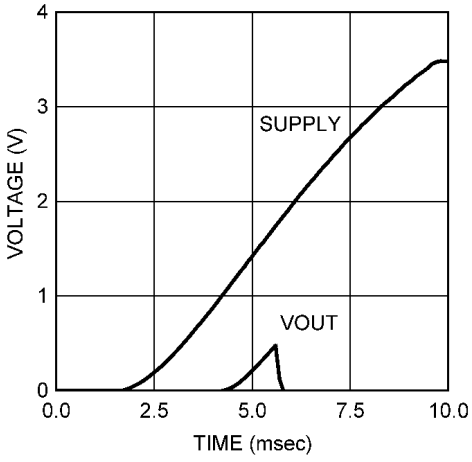


Figure 25.

Multiplying Bandwidth

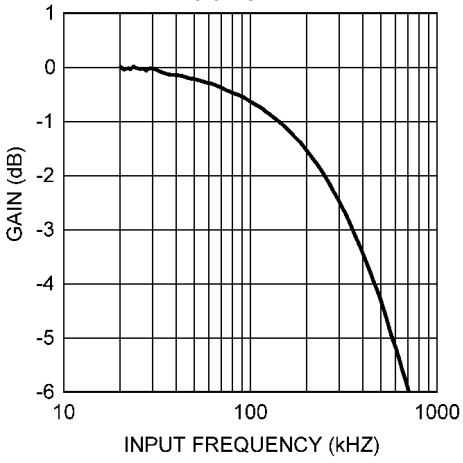


Figure 26.

FUNCTIONAL DESCRIPTION

DAC ARCHITECTURE

The DAC108S085 is fabricated on a CMOS process with an architecture that consists of switches and resistor strings that are followed by an output buffer. The reference voltages are externally applied at V_{REF1} for DAC channels A through D and V_{REF2} for DAC channels E through H.

For simplicity, a single resistor string is shown in Figure 27. This string consists of 1024 equal valued resistors with a switch at each junction of two resistors, plus a switch to ground. The code loaded into the DAC register determines which switch is closed, connecting the proper node to the amplifier. The input coding is straight binary with an ideal output voltage of:

$$V_{OUTA,B,C,D} = V_{REF1} \times (D / 1024) \quad (2)$$

$$V_{OUTE,F,G,H} = V_{REF2} \times (D / 1024)$$

where

- D is the decimal equivalent of the binary code that is loaded into the DAC register (3)

D can take on any value between 0 and 1023. This configuration ensures that the DAC is monotonic.

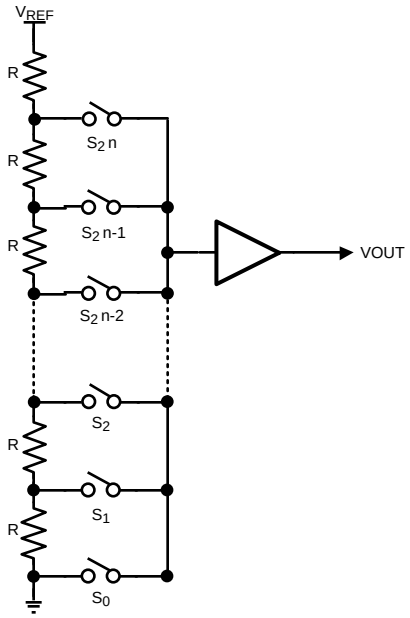


Figure 27. DAC Resistor String

Since all eight DAC channels of the DAC108S085 can be controlled independently, each channel consists of a DAC register and a 10-bit DAC. Figure 28 is a simple block diagram of an individual channel in the DAC108S085. Depending on the mode of operation, data written into a DAC register causes the 10-bit DAC output to be updated or an additional command is required to update the DAC output. Further description of the modes of operation can be found in the Serial Interface description.

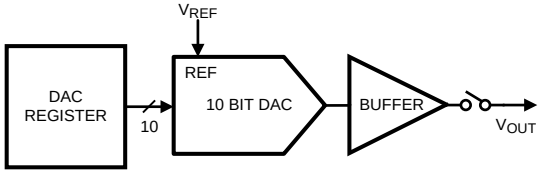


Figure 28. Single Channel Block Diagram

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OUTPUT AMPLIFIERS

The output amplifiers are rail-to-rail, providing an output voltage range of 0V to V_A when the reference is V_A. All amplifiers, even rail-to-rail types, exhibit a loss of linearity as the output approaches the supply rails (0V and V_A, in this case). For this reason, linearity is specified over less than the full output range of the DAC. However, if the reference is less than V_A, there is only a loss in linearity in the lowest codes.

The output amplifiers are capable of driving a load of 2 kΩ in parallel with 1500 pF to ground or to V_A. The zero-code and full-scale outputs for given load currents are available in the Electrical Characteristics.

REFERENCE VOLTAGE

The DAC108S085 uses dual external references, V_{REF1} and V_{REF2}, that are shared by channels A, B, C, D and channels E, F, G, H respectively. The reference pins are not buffered and have an input impedance of 30 kΩ. It is recommended that V_{REF1} and V_{REF2} be driven by voltage sources with low output impedance. The reference voltage range is 0.5V to V_A, providing the widest possible output dynamic range.

SERIAL INTERFACE

The three-wire interface is compatible with SPI™, QSPI and MICROWIRE, as well as most DSPs and operates at clock rates up to 40 MHz. A valid serial frame contains 16 falling edges of SCLK. See the Timing Diagrams for information on a write sequence.

A write sequence begins by bringing the $\overline{\text{SYNC}}$ line low. Once $\overline{\text{SYNC}}$ is low, the data on the D_{IN} line is clocked into the 16-bit serial input register on the falling edges of SCLK. To avoid mis-clocking data into the shift register, it is critical that $\overline{\text{SYNC}}$ not be brought low on a falling edge of SCLK (see minimum and maximum setup times for $\overline{\text{SYNC}}$ in the Timing Characteristics and Figure 29). On the 16th falling edge of SCLK, the last data bit is clocked into the register. The write sequence is concluded by bringing the $\overline{\text{SYNC}}$ line high. Once $\overline{\text{SYNC}}$ is high, the programmed function (a change in the DAC channel address, mode of operation and/or register contents) is executed. To avoid mis-clocking data into the shift register, it is critical that $\overline{\text{SYNC}}$ be brought high between the 16th and 17th falling edges of SCLK (see minimum and maximum hold times for $\overline{\text{SYNC}}$ in the Timing Characteristics and Figure 29).

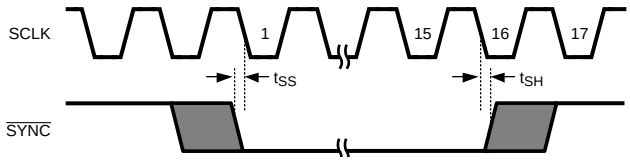


Figure 29. $\overline{\text{CS}}$ Setup and Hold Times

If $\overline{\text{SYNC}}$ is brought high before the 15th falling edge of SCLK, the write sequence is aborted and the data that has been shifted into the input register is discarded. If $\overline{\text{SYNC}}$ is held low beyond the 17th falling edge of SCLK, the serial data presented at D_{IN} will begin to be output on D_{OUT}. More information on this mode of operation can be found in Daisy Chain Operation. In either case, $\overline{\text{SYNC}}$ must be brought high for the minimum specified time before the next write sequence is initiated with a falling edge of $\overline{\text{SYNC}}$.

Since the D_{IN} buffer draws more current when it is high, it should be idled low between write sequences to minimize power consumption. On the other hand, $\overline{\text{SYNC}}$ should be idled high to avoid the activation of daisy chain operation where D_{OUT} is active.

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DAISY CHAIN OPERATION

Daisy chain operation allows communication with any number of DAC108S085s using a single serial interface. As long as the correct number of data bits are input in a write sequence (multiple of sixteen bits), a rising edge of $\overline{SYNC}$ will properly update all DACs in the system.

To support multiple devices in a daisy chain configuration, SCLK and $\overline{SYNC}$ are shared across all DAC108S085s and D_{OUT} of the first DAC in the chain is connected to D_{IN} of the second. Figure 30 shows three DAC108S085s connected in daisy chain fashion. Similar to a single channel write sequence, the conversion for a daisy chain operation begins on a falling edge of $\overline{SYNC}$ and ends on a rising edge of $\overline{SYNC}$. A valid write sequence for n devices in a chain requires n times 16 falling edges to shift the entire input data stream through the chain. Daisy chain operation is specifed for a maximum SCLK speed of 30MHz.

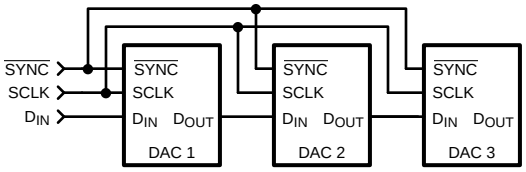


Figure 30. Daisy Chain Configuration

The serial data output pin, D_{OUT}, is available on the DAC108S085 to allow daisy-chaining of multiple DAC108S085 devices in a system. In a write sequence, D_{OUT} remains low for the first fourteen falling edges of SCLK before going high on the fifteenth falling edge. Subsequently, the next sixteen falling edges of SCLK will output the first sixteen data bits entered into D_{IN}. Figure 31 shows the timing of three DAC108S085s in Figure 30. In this instance, It takes forty-eight falling edges of SCLK followed by a rising edge of $\overline{SYNC}$ to load all three DAC108S085s with the appropriate register data. On the rising edge of $\overline{SYNC}$, the programmed function is executed in each DAC108S085 simultaneously.

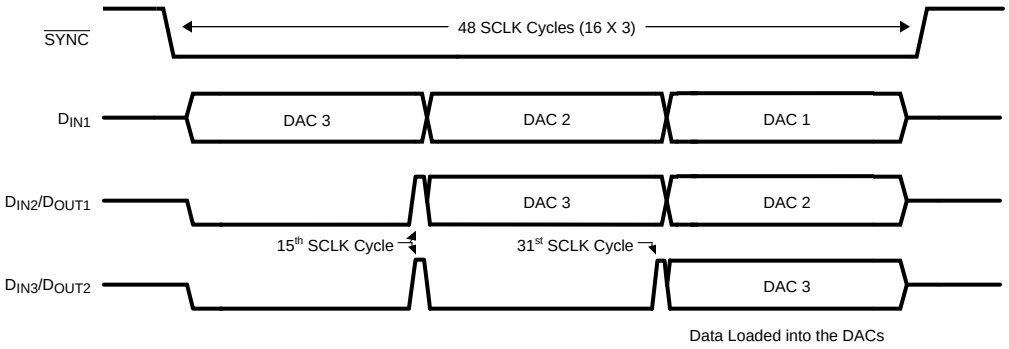


Figure 31. Daisy Chain Timing Diagram

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SERIAL INPUT REGISTER

The DAC108S085 has two modes of operation plus a few special command operations. The two modes of operation are Write Register Mode (WRM) and Write Through Mode (WTM). For the rest of this document, these modes will be referred to as WRM and WTM. The special command operations are separate from WRM and WTM because they can be called upon regardless of the current mode of operation. The mode of operation is controlled by the first four bits of the control register, DB15 through DB12. See Table 1 for a detailed summary.

Table 1. Write Register and Write Through Modes

DB[15:12]	DB[11:0]	Description of Mode
1 0 0 0	X X X X X X X X X X X X	WRM: The registers of each DAC Channel can be written to without causing their outputs to change.
1 0 0 1	X X X X X X X X X X X X	WTM: Writing data to a channel's register causes the DAC output to change.

When the DAC108S085 first powers up, the DAC is in WRM. In WRM, the registers of each individual DAC channel can be written to without causing the DAC outputs to be updated. This is accomplished by setting DB15 to "0", specifying the DAC register to be written to in DB[14:12], and entering the new DAC register setting in DB[11:0] (see Table 2).The DAC108S085 remains in WRM until the mode of operation is changed to WTM. The mode of operation is changed from WRM to WTM by setting DB[15:12] to "1001". Once in WTM, writing data to a DAC channel's register causes the DAC's output to be updated as well. Changing a DAC channel's register in WTM is accomplished in the same manner as it is done in WRM. However, in WTM the DAC's register and output are updated at the completion of the command (see Table 2). Similarly, the DAC108S085 remains in WTM until the mode of operation is changed to WRM by setting DB[15:12] to "1000".

Table 2. Commands Impacted by WRM and WTM

DB15	DB[14:12]	DB[11:0]	Description of Mode
0	0 0 0	D11 D10 ... D2 X X	WRM: D[11:0] written to ChA's data register only WTM: ChA's output is updated by data in D[11:0]
0	0 0 1	D11 D10 ... D2 X X	WRM: D[11:0] written to ChB's data register only WTM: ChB's output is updated by data in D[11:0]
0	0 1 0	D11 D10 ... D2 X X	WRM: D[11:0] written to ChC's data register only WTM: ChC's output is updated by data in D[11:0]
0	0 1 1	D11 D10 ... D2 X X	WRM: D[11:0] written to ChD's data register only WTM: ChD's output is updated by data in D[11:0]
0	1 0 0	D11 D10 ... D2 X X	WRM: D[11:0] written to ChE's data register only WTM: ChE's output is updated by data in D[11:0]
0	1 0 1	D11 D10 ... D2 X X	WRM: D[11:0] written to ChF's data register only WTM: ChF's output is updated by data in D[11:0]
0	1 1 0	D11 D10 ... D2 X X	WRM: D[11:0] written to ChG's data register only WTM: ChG's output is updated by data in D[11:0]
0	1 1 1	D11 D10 ... D2 X X	WRM: D[11:0] written to ChH's data register only WTM: ChH's output is updated by data in D[11:0]

As mentioned previously, the special command operations can be exercised at any time regardless of the mode of operation. There are three special command operations. The first command is exercised by setting data bits DB[15:12] to "1010". This allows a user to update multiple DAC outputs simultaneously to the values currently loaded in their respective control registers. This command is valuable if the user wants each DAC output to be at a different output voltage but still have all the DAC outputs change to their appropriate values simultaneously (see Table 3).

The second special command allows the user to alter the DAC output of channel A with a single write frame. This command is exercised by setting data bits DB[15:12] to "1011" and data bits DB[11:0] to the desired control register value. It also has the added benefit of causing the DAC outputs of the other channels to update to their current control register values as well. A user may choose to exercise this command to save a write sequence. For example, the user may wish to update several DAC outputs simultaneously, including channel A. In order to

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accomplish this task in the minimum number of write frames, the user would alter the control register values of all the DAC channels except channel A while operating in WRM. The last write frame would be used to exercise the special command "Channel A Write Mode". In addition to updating channel A's control register and output to a new value, all of the other channels would be updated as well. At the end of this sequence of write frames, the DAC108S085 would still be operating in WRM (see Table 3).

The third special command allows the user to set all the DAC control registers and outputs to the same level. This command is commonly referred to as "broadcast" mode since the same data bits are being broadcast to all of the channels simultaneously. This command is exercised by setting data bits DB[15:12] to "1100" and data bits DB[11:0] to the value that the user wishes to broadcast to all the DAC control registers. Once the command is exercised, each DAC output is updated by the new control register value. This command is frequently used to set all the DAC outputs to some known voltage such as 0V, $V_{REF}/2$, or Full Scale. A summary of the commands can be found in Table 3.

Table 3. Special Command Operations

DB[15:12]	DB[11:0]	Description of Mode
1 0 1 0	X X X X H G F E D C B A	Update Select: The DAC outputs of the channels selected with a "1" in DB[7:0] are updated simultaneously to the values in their respective control registers.
1 0 1 1	D11 D10 ... D3 D2 X X	Channel A Write: Channel A's control register and DAC output are updated to the data in DB[11:0]. The outputs of the other seven channels are also updated according to their respective control register values.
1 1 0 0	D11 D10 ... D3 D2 X X	Broadcast: The data in DB[11:0] is written to all channels' control register and DAC output simultaneously.

POWER-ON RESET

The power-on reset circuit controls the output voltages of the eight DACs during power-up. Upon application of power, the DAC registers are filled with zeros and the output voltages are set to 0V. The outputs remain at 0V until a valid write sequence is made.

POWER-DOWN MODES

The DAC108S085 has three power-down modes where different output terminations can be selected (see Table 4). With all channels powered down, the supply current drops to 0.1 µA at 3V and 0.2 µA at 5V. By selecting the channels to be powered down in DB[7:0] with a "1", individual channels can be powered down separately or multiple channels can be powered down simultaneously. The three different output terminations include high output impedance, 100k ohm to ground, and 2.5k ohm to ground.

The output amplifiers, resistor strings, and other linear circuitry are all shut down in any of the power-down modes. The bias generator, however, is only shut down if all the channels are placed in power-down mode. The contents of the DAC registers are unaffected when in power-down. Therefore, each DAC register maintains its value prior to the DAC108S085 being powered down unless it is changed during the write sequence which instructed it to recover from power down. Minimum power consumption is achieved in the power-down mode with $\overline{SYNC}$ idled high, D_{IN} idled low, and SCLK disabled. The time to exit power-down (Wake-Up Time) is typically 3 µsec at 3V and 20 µsec at 5V.

Table 4. Power-Down Modes

DB[15:12]	DB[11:8]	7	6	5	4	3	2	1	0	Output Impedance
1 1 0 1	X X X X	H	G	F	E	D	C	B	A	High-Z outputs
1 1 1 0	X X X X	H	G	F	E	D	C	B	A	100 kΩ outputs
1 1 1 1	X X X X	H	G	F	E	D	C	B	A	2.5 kΩ outputs

Applications Information

EXAMPLES PROGRAMMING THE DAC108S085

This section will present the step-by-step instructions for programming the serial input register.

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Updating DAC Outputs Simultaneously

When the DAC108S085 is first powered on, the DAC is operating in Write Register Mode (WRM). Operating in WRM allows the user to program the registers of multiple DAC channels without causing the DAC outputs to be updated. As an example, here are the steps for setting Channel A to a full scale output, Channel B to three-quarters full scale, Channel C to half-scale, Channel D to one-quarter full scale and having all the DAC outputs update simultaneously.

As stated previously, the DAC108S085 powers up in WRM. If the device was previously operating in Write Through Mode (WTM), an extra step to set the DAC into WRM would be required. First, the DAC registers need to be programmed to the desired values. To set Channel A to an output of full scale, write "0FFC" to the control register. This will update the data register for Channel A without updating the output of Channel A. Second, set Channel B to an output of three-quarters full scale by writing "1C00" to the control register. This will update the data register for Channel B. Once again, the output of Channel B and Channel A will not be updated since the DAC is operating in WRM. Third, set Channel C to half scale by writing "2800" to the control register. Fourth, set Channel D to one-quarter full scale by writing "3400" to the control register. Finally, update all four DAC channels simultaneously by writing "A00F" to the control register. This procedure allows the user to update four channels simultaneously with five steps.

Since Channel A was one of the DACs to be updated, one command step could have been saved by writing to Channel A last. This is accomplished by writing to Channel B, C, and D first and using the the special command "Channel A Write" to update Channel A's DAC register and output. This special command has the added benefit of updating all DAC outputs while updating Channel A. With this sequence of commands, the user was able to update four channels simultaneously with four steps. A summary of this command can be found in Table 3.

Updating DAC Outputs Independently

If the DAC108S085 is currently operating in WRM, change the mode of operation to WTM by writing "9XXX" to the control register. Once the DAC is operating in WTM, any DAC channel can be updated in one step. For example, if a design required Channel G to be set to half scale, the user can write "6800" to the control register and Channel G's data register and DAC output will be updated. Similarly, if Channel F's output needed to be set to full scale, "5FFC" would need to be written to the control register. Channel A is the only channel that has a special command that allows its DAC output to be updated in one command regardless of the mode of operation. Setting Channel A's DAC output to full scale could be accomplished in one step by writing "BFFF" to the control register.

USING REFERENCES AS POWER SUPPLIES

While the simplicity of the DAC108S085 implies ease of use, it is important to recognize that the path from the reference input ($V_{REF1,2}$) to the DAC outputs will have zero Power Supply Rejection Ratio (PSRR). Therefore, it is necessary to provide a noise-free supply voltage to $V_{REF1,2}$. In order to utilize the full dynamic range of the DAC108S085, the supply pin (V_A) and $V_{REF1,2}$ can be connected together and share the same supply voltage. Since the DAC108S085 consumes very little power, a reference source may be used as the reference input and/or the supply voltage. The advantages of using a reference source over a voltage regulator are accuracy and stability. Some low noise regulators can also be used. Listed below are a few reference and power supply options for the DAC108S085.

LM4132

The LM4132, with its ±0.05% accuracy over temperature, is a good choice as a reference source for the DAC108S085. The 4.096V version is useful if a 0V to 4.095V output range is desirable. Bypassing the LM4132 voltage input pin with a 4.7µF capacitor and the voltage output pin with a 4.7µF capacitor will improve stability and reduce output noise. The LM4132 comes in a space-saving 5-pin SOT23.

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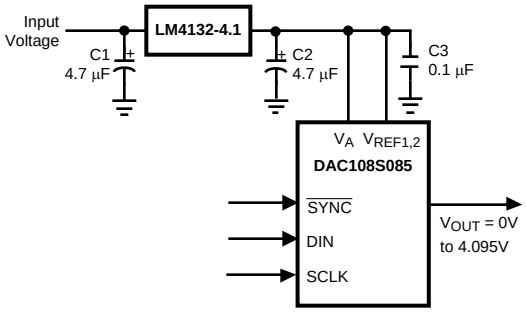


Figure 32. The LM4132 as a power supply

LM4050

Available with accuracy of ±0.1%, the LM4050 shunt reference is also a good choice as a reference for the DAC108S085. It is available in 4.096V and 5V versions and comes in a space-saving 3-pin SOT23.

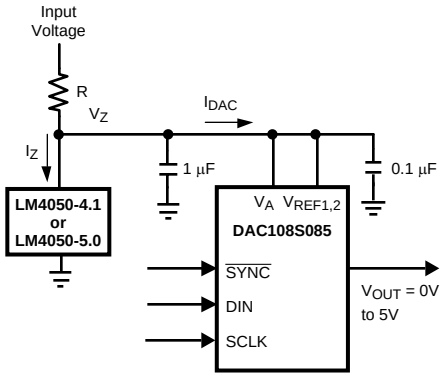


Figure 33. The LM4050 as a power supply

The minimum resistor value in the circuit of must be chosen such that the maximum current through the LM4050 does not exceed its 15 mA rating. The conditions for maximum current include the input voltage at its maximum, the LM4050 voltage at its minimum, and the DAC108S085 drawing zero current. The maximum resistor value must allow the LM4050 to draw more than its minimum current for regulation plus the maximum DAC108S085 current in full operation. The conditions for minimum current include the input voltage at its minimum, the LM4050 voltage at its maximum, the resistor value at its maximum due to tolerance, and the DAC108S085 draws its maximum current. These conditions can be summarized as

$$R(min) = (V_{IN}(max) - V_Z(min)) / I_Z(max) \quad (4)$$

and

$$R(max) = (V_{IN}(min) - V_Z(max)) / ((I_{DAC}(max) + I_Z(min)) \quad (5)$$

where

- V_Z(min) and V_Z(max) are the nominal LM4050 output voltages ± the LM4050 output tolerance over temperature
- I_Z(max) is the maximum allowable current through the LM4050, I_Z(min) is the minimum current required by the LM4050 for proper regulation
- I_{DAC}(max) is the maximum DAC108S085 supply current

LP3985

The LP3985 is a low noise, ultra low dropout voltage regulator with a ±3% accuracy over temperature. It is a good choice for applications that do not require a precision reference for the DAC108S085. It comes in 3.0V, 3.3V and 5V versions, among others, and sports a low 30 µV noise specification at low frequencies. Since low frequency noise is relatively difficult to filter, this specification could be important for some applications. The LP3985 comes in a space-saving 5-pin SOT-23 and 5-bump DSBGA packages.

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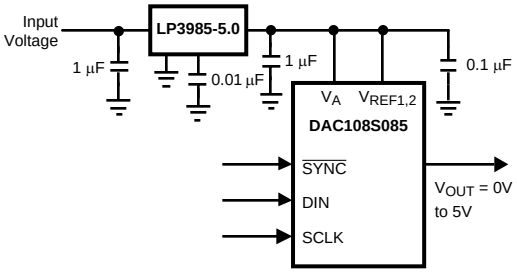


Figure 34. Using the LP3985 regulator

An input capacitance of 1.0µF without any ESR requirement is required at the LP3985 input, while a 1.0µF ceramic capacitor with an ESR requirement of 5mΩ to 500mΩ is required at the output. Careful interpretation and understanding of the capacitor specification is required to ensure correct device operation.

LP2980

The LP2980 is an ultra low dropout regulator with a ±0.5% or ±1.0% accuracy over temperature, depending upon grade. It is available in 3.0V, 3.3V and 5V versions, among others.

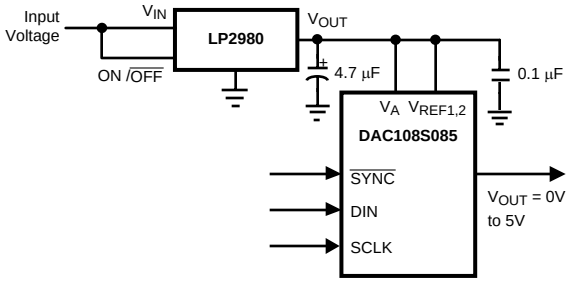


Figure 35. Using the LP2980 regulator

Like any low dropout regulator, the LP2980 requires an output capacitor for loop stability. This output capacitor must be at least 1.0µF over temperature, but values of 2.2µF or more will provide even better performance. The ESR of this capacitor should be within the range specified in the LP2980 data sheet. Surface-mount solid tantalum capacitors offer a good combination of small size and low ESR. Ceramic capacitors are attractive due to their small size but generally have ESR values that are too low for use with the LP2980. Aluminum electrolytic capacitors are typically not a good choice due to their large size and high ESR values at low temperatures.

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BIPOLAR OPERATION

The DAC108S085 is designed for single supply operation and thus has a unipolar output. However, a bipolar output may be achieved with the circuit in. This circuit will provide an output voltage range of ±5 Volts. A rail-to-rail amplifier should be used if the amplifier supplies are limited to ±5V.

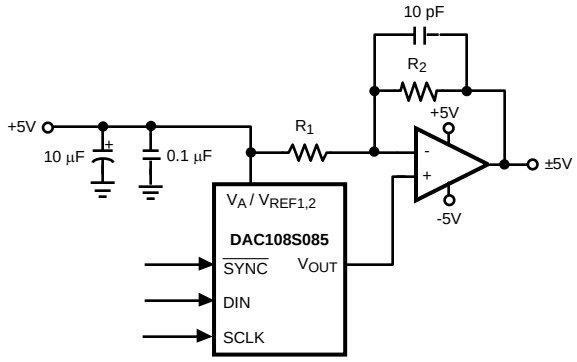


Figure 36. Bipolar Operation

The output voltage of this circuit for any code is found to be

$$V_O = (V_A \times (D / 1024) \times ((R1 + R2) / R1) - V_A \times R2 / R1) \quad (6)$$

$$V_O = (10 \times D / 1024) - 5V$$

where

- D is the input code in decimal form. With V_A = 5V and R1 = R2 (7)

A list of rail-to-rail amplifiers suitable for this application are indicated in .

Table 5. Some Rail-to-Rail Amplifiers

AMP	PKGS	Typ V_{OS}	Typ I_{SUPPLY}
LMP7701	SOT23-5	±37 µV	0.79 mA
LMV841	SOT23-5	−17 µV	1.11 mA
LMC7111	SOT23-5	900 µV	25 µA
LM7301	SOT23-5	30 µV	620 µA
LM8261	SOT23-5	700 µV	1 mA

VARIABLE CURRENT SOURCE OUTPUT

The DAC108S085 is a voltage output DAC but can be easily converted to a current output with the addition of an opamp. In Figure 37, one of the channels of the DAC108S085 is converted to a variable current source capable of sourcing up to 40mA.

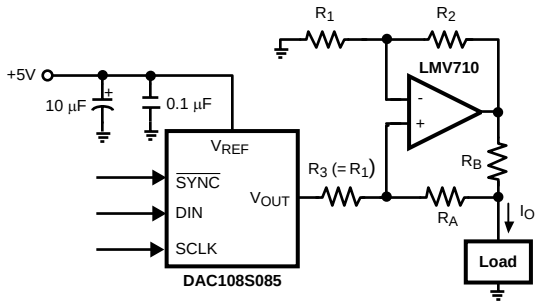


Figure 37. Variable Current Source

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The output current of this circuit (I_O) for any DAC code is found to be

$$I_O = (V_{REF} \times (D / 1024) \times (R_2) / (R_1 \times R_B)$$

where

- D is the input code in decimal form
- $R_2 = R_A + R_B$ (8)

APPLICATION CIRCUITS

The following figures are examples of the DAC108S085 in typical application circuits. These circuits are basic and will generally require modification for specific circumstances.

Industrial Application

Figure 38 shows the DAC108S085 controlling several different circuits in an industrial setting. Channel A is shown providing the reference voltage to the ADC101S625, one of TI's general purpose Analog-to-Digital Converters (ADCs). The reference for the ADC121S625 may be set to any voltage from 0.2V to 5.5V, providing the widest dynamic range possible. Typically, the ADC121S625 will be monitoring a sensor and would benefit from the ADC's reference voltage being adjustable. Channel B is providing the drive or supply voltage for a sensor. By having the sensor supply voltage adjustable, the output of the sensor can be optimized to the input level of the ADC monitoring it. Channel C is defined to adjust the offset or gain of an amplifier stage in the system. Channel D is configured with an opamp to provide an adjustable current source. Being able to convert one of the eight channels of the DAC108S085 to a current output eliminates the need for a separate current output DAC to be added to the circuit. Channel E, in conjunction with an opamp, provides a bipolar output swing for devices requiring control voltages that are centered around ground. Channel F and G are used to set the upper and lower limits for a range detector. Channel H is reserved for providing voltage control or acting as a voltage setpoint.

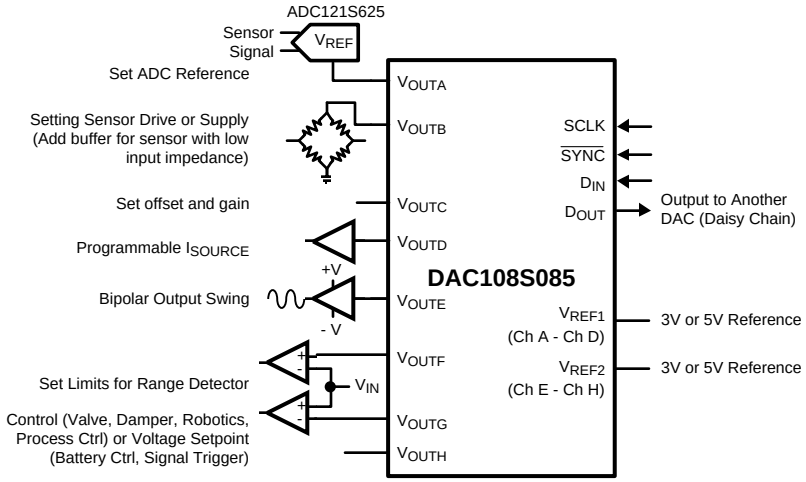


Figure 38. Industrial Application

ADC Reference

Figure 39 shows Channel A of the DAC108S085 providing the drive or supply voltage for a bridge sensor. By having the sensor supply voltage adjustable, the output of the sensor can be optimized to the input level of the ADC monitoring it. The output of the sensor is amplified by a fixed gain amplifier stage with a differential gain of $1 + 2 \times (R_F / R_I)$. The advantage of this amplifier configuration is the high input impedance seen by the output of the bridge sensor. The disadvantage is the poor common-mode rejection ratio (CMRR). The common-mode voltage (V_{CM}) of the bridge sensor is half of Channel A's DAC output. The V_{CM} is amplified by a gain of 1V/V by the amplifier stage and thus becomes the bias voltage for the input of the ADC121S705. Channel B of the DAC108S085 is providing the reference voltage to the ADC121S705. The reference for the ADC121S705 may be set to any voltage from 1V to 5V, providing the widest dynamic range possible.

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The reference voltage for Channel A and B is powered by an external 5V power supply. Since the 5V supply is common to the sensor supply voltage and the reference voltage of the ADC, fluctuations in the value of the 5V supply will have a minimal effect on the digital output code of the ADC. This type of configuration is often referred to as a "Ratio-metric" design. For example, an increase of 5% to the 5V supply will cause the sensor supply voltage to increase by 5%. This causes the gain or sensitivity of the sensor to increase by 5%. The gain of the amplifier stage is unaffected by the change in supply voltage. The ADC121S705 on the other hand, also experiences a 5% increase to its reference voltage. This causes the size of the ADC's least significant bit (LSB) to increase by 5%. As a result of the sensor's gain increasing by 5% and the LSB size of the ADC increasing by the same 5%, there is no net effect on the circuit's performance. It is assumed that the amplifier gain is set low enough to allow for a 5% increase in the sensor output. Otherwise, the increase in the sensor output level may cause the output of the amplifiers to clip.

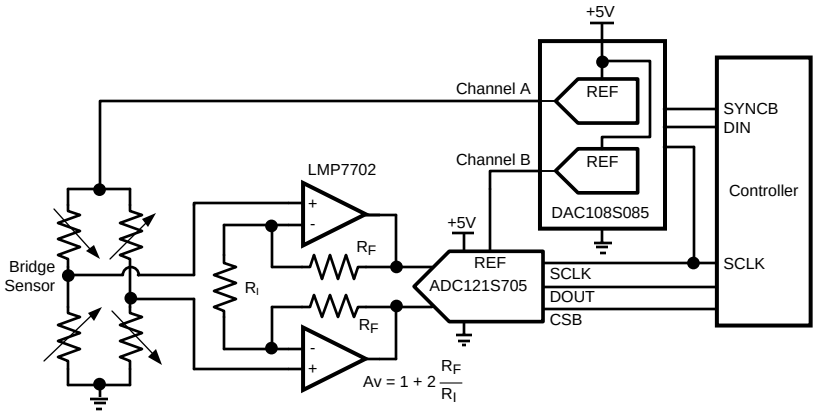


Figure 39. Driving an ADC Reference

Programmable Attenuator

shows one of the channels of the DAC108S085 being used as a single-quadrant multiplier. In this configuration, an AC or DC signal can be driven into one of the reference pins. The SPI interface of the DAC can be used to digitally attenuate the signal to any level from 0dB (full scale) to 0V. This is accomplished without adding any noticeable level of noise to the signal. An amplifier stage is shown in as a reference for applications where the input signal requires amplification. Note how the AC signal in this application is ac-coupled to the amplifier before being amplified. A separate bias voltage is used to set the common-mode voltage for the DAC108S085's reference input to V_A / 2, allowing the largest possible input swing. The multiplying bandwidth of $V_{REF1,2}$ is 360kHz with a V_{CM} of 2.5V and a peak-to-peak signal swing of 2V.

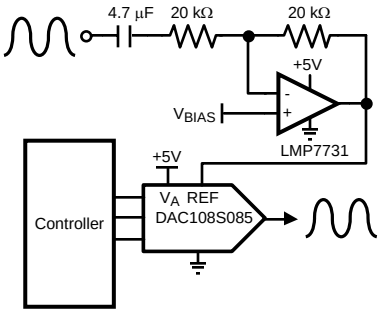


Figure 40. Programmable Attenuator

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DSP/MICROPROCESSOR INTERFACING

Interfacing the DAC108S085 to microprocessors and DSPs is quite simple. The following guidelines are offered to hasten the design process.

ADSP-2101/ADSP2103 Interfacing

Figure 41 shows a serial interface between the DAC108S085 and the ADSP-2101/ADSP2103. The DSP should be set to operate in the SPORT Transmit Alternate Framing Mode. It is programmed through the SPORT control register and should be configured for Internal Clock Operation, Active Low Framing and 16-bit Word Length. Transmission is started by writing a word to the Tx register after the SPORT mode has been enabled.

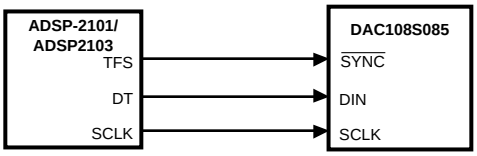


Figure 41. ADSP-2101/2103 Interface

80C51/80L51 Interface

A serial interface between the DAC108S085 and the 80C51/80L51 microcontroller is shown in Figure 42. The SYNC signal comes from a bit-programmable pin on the microcontroller. The example shown here uses port line P3.3. This line is taken low when data is transmitted to the DAC108S085. Since the 80C51/80L51 transmits 8-bit bytes, only eight falling clock edges occur in the transmit cycle. To load data into the DAC, the P3.3 line must be left low after the first eight bits are transmitted. A second write cycle is initiated to transmit the second byte of data, after which port line P3.3 is brought high. The 80C51/80L51 transmit routine must recognize that the 80C51/80L51 transmits data with the LSB first while the DAC108S085 requires data with the MSB first.

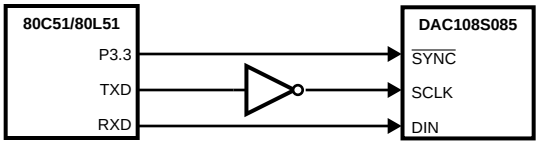


Figure 42. 80C51/80L51 Interface

68HC11 Interface

A serial interface between the DAC108S085 and the 68HC11 microcontroller is shown in Figure 43. The SYNC line of the DAC108S085 is driven from a port line (PC7 in the figure), similar to the 80C51/80L51.

The 68HC11 should be configured with its CPOL bit as a zero and its CPHA bit as a one. This configuration causes data on the MOSI output to be valid on the falling edge of SCLK. PC7 is taken low to transmit data to the DAC. The 68HC11 transmits data in 8-bit bytes with eight falling clock edges. Data is transmitted with the MSB first. PC7 must remain low after the first eight bits are transferred. A second write cycle is initiated to transmit the second byte of data to the DAC, after which PC7 should be raised to end the write sequence.

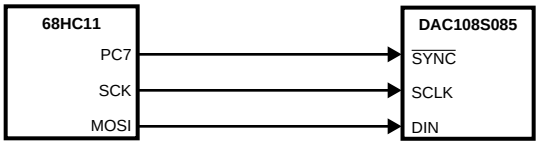


Figure 43. 68HC11 Interface

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Microwire Interface

Figure 44 shows an interface between a Microwire compatible device and the DAC108S085. Data is clocked out on the rising edges of the SK signal. As a result, the SK of the Microwire device needs to be inverted before driving the SCLK of the DAC108S085.

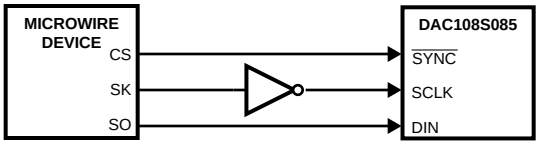


Figure 44. Microwire Interface

LAYOUT, GROUNDING, AND BYPASSING

For best accuracy and minimum noise, the printed circuit board containing the DAC108S085 should have separate analog and digital areas. The areas are defined by the locations of the analog and digital power planes. Both of these planes should be located in the same board layer. A single ground plane is preferred if digital return current does not flow through the analog ground area. Frequently a single ground plane design will utilize a "fencing" technique to prevent the mixing of analog and digital ground current. Separate ground planes should only be utilized when the fencing technique is inadequate. The separate ground planes must be connected in one place, preferably near the DAC108S085. Special care is required to ensure that digital signals with fast edge rates do not pass over split ground planes. They must always have a continuous return path below their traces.

For best performance, the DAC108S085 power supply should be bypassed with at least a 1µF and a 0.1µF capacitor. The 0.1µF capacitor needs to be placed right at the device supply pin. The 1µF or larger valued capacitor can be a tantalum capacitor while the 0.1µF capacitor needs to be a ceramic capacitor with low ESL and low ESR. If a ceramic capacitor with low ESL and low ESR is used for the 1µF value and it can be placed right at the supply pin, the 0.1µF capacitor can be eliminated. Capacitors of this nature typically span the same frequency spectrum as the 0.1µF capacitor and thus eliminate the need for the extra capacitor. The power supply for the DAC108S085 should only be used for analog circuits.

It is also advisable to avoid the crossover of analog and digital signals. This helps minimize the amount of noise from the transitions of the digital signals from coupling onto the sensitive analog signals such as the reference pins and the DAC outputs.

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REVISION HISTORY

Changes from Revision A (March 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	26

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DAC108S085CIMT/NO.A	Active	Production	TSSOP (PW) | 16	92 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	X80C
DAC108S085CIMT/NOPB	Active	Production	TSSOP (PW) | 16	92 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	X80C
DAC108S085CIMTX/NO.A	Active	Production	TSSOP (PW) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	X80C
DAC108S085CIMTX/NO.B	Active	Production	TSSOP (PW) | 16	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
DAC108S085CIMTX/NOPB	Active	Production	TSSOP (PW) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	X80C
DAC108S085CISQ/NO.A	Active	Production	WQFN (RGH) | 16	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	108S085
DAC108S085CISQ/NO.B	Active	Production	WQFN (RGH) | 16	1000 | SMALL T&R	-	Call TI	Call TI	-40 to 125	
DAC108S085CISQ/NOPB	Active	Production	WQFN (RGH) | 16	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	108S085
DAC108S085CISQX/NO.A	Active	Production	WQFN (RGH) | 16	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	108S085
DAC108S085CISQX/NO.B	Active	Production	WQFN (RGH) | 16	4500 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
DAC108S085CISQX/NOPB	Active	Production	WQFN (RGH) | 16	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	108S085

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

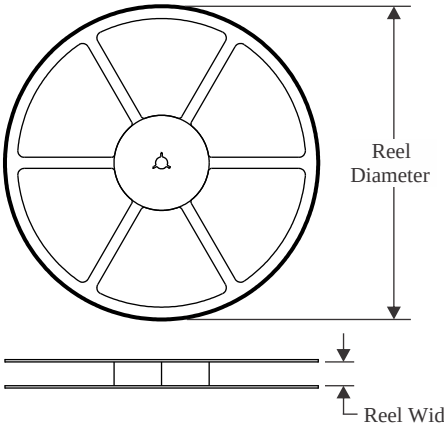
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

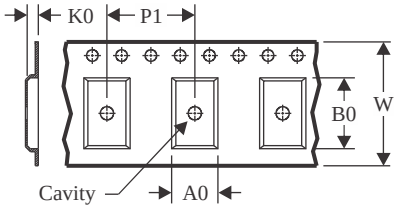
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

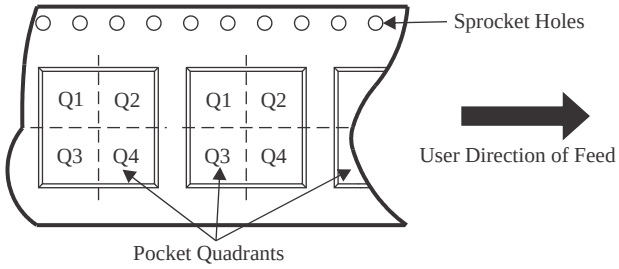


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

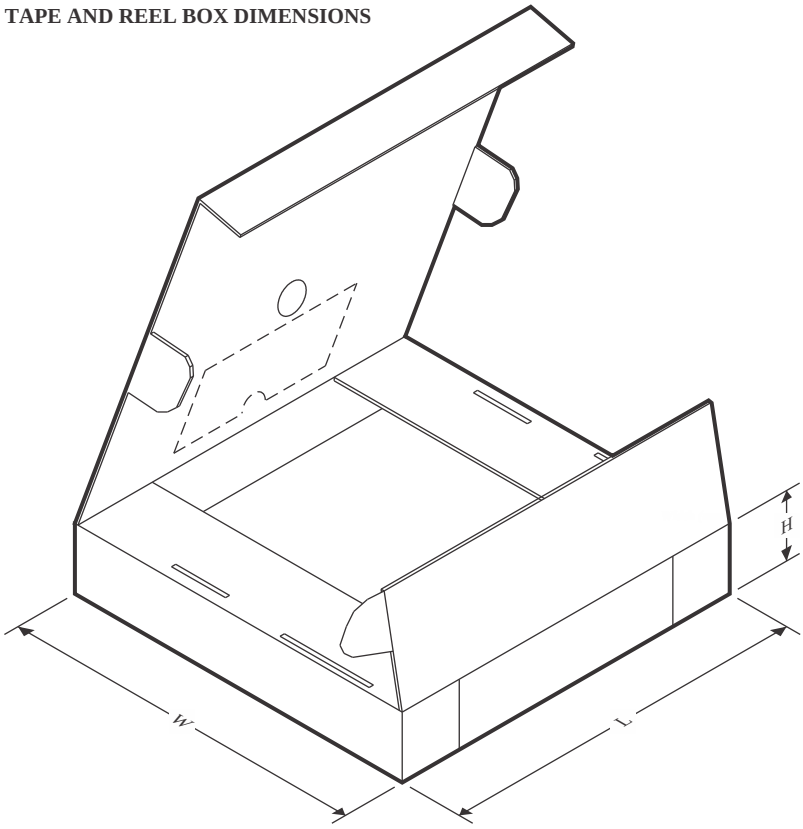
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC108S085CIMTX/ NOPB	TSSOP	PW	16	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
DAC108S085CISQ/NOPB	WQFN	RGH	16	1000	177.8	12.4	4.3	4.3	1.3	8.0	12.0	Q1
DAC108S085CISQX/ NOPB	WQFN	RGH	16	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

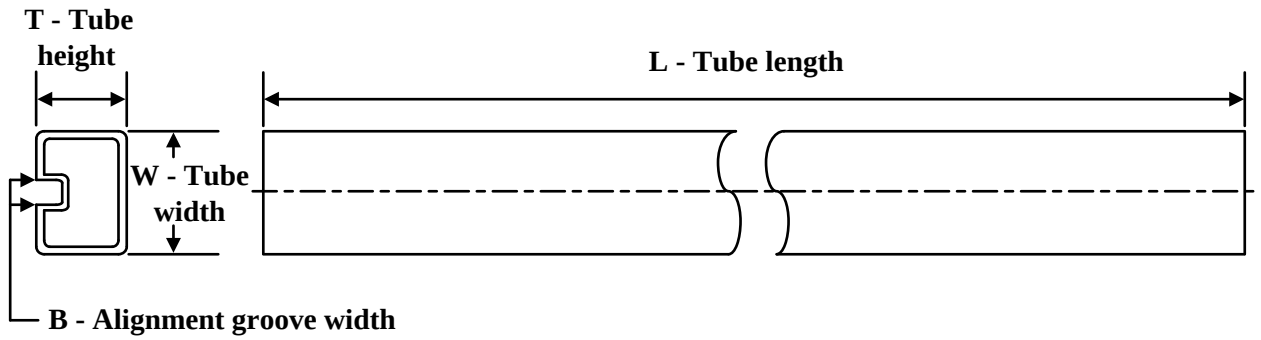
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC108S085CIMTX/ NOPB	TSSOP	PW	16	2500	367.0	367.0	35.0
DAC108S085CISQ/NOPB	WQFN	RGH	16	1000	210.0	185.0	35.0
DAC108S085CISQX/ NOPB	WQFN	RGH	16	4500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

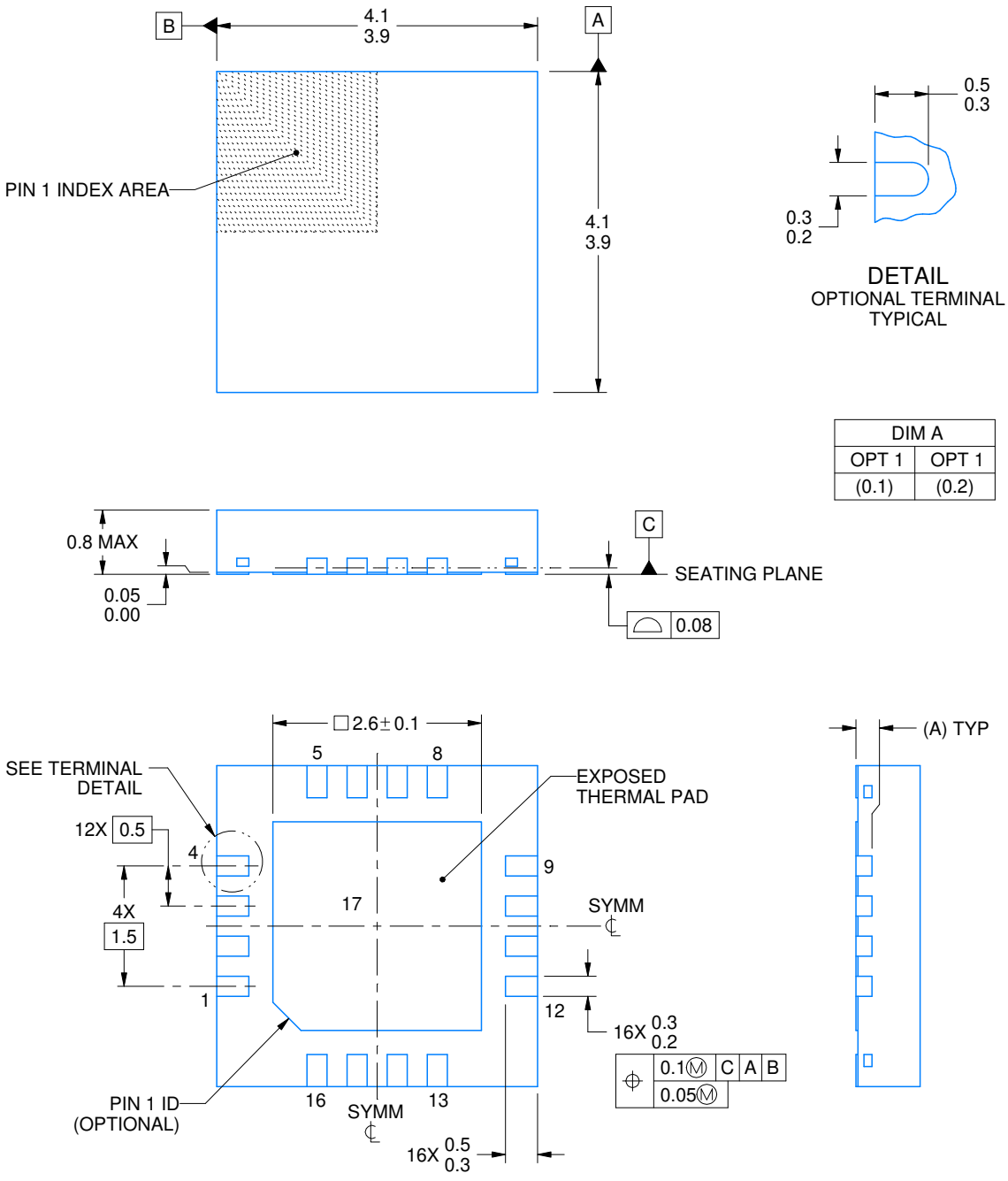
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DAC108S085CIMT/NO.A	PW	TSSOP	16	92	495	8	2514.6	4.06
DAC108S085CIMT/NOPB	PW	TSSOP	16	92	495	8	2514.6	4.06

PACKAGE OUTLINE

RGH0016A

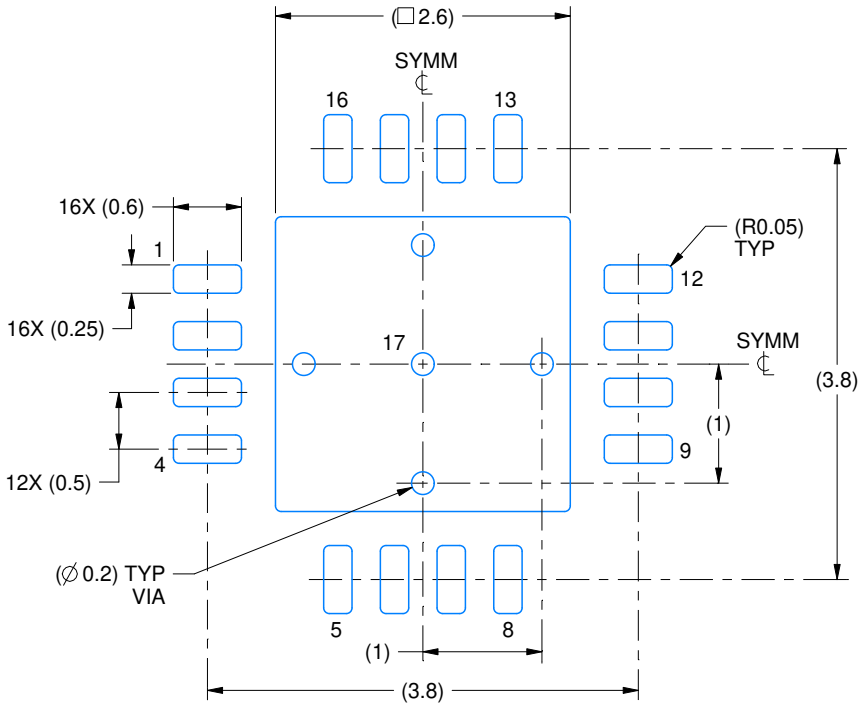
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

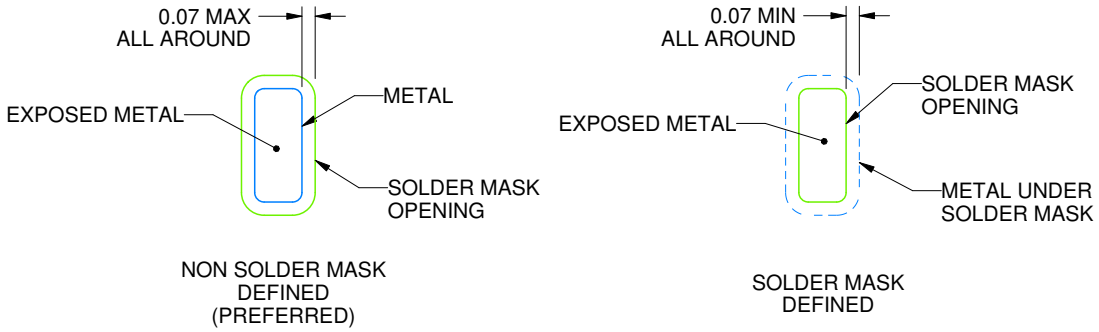


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

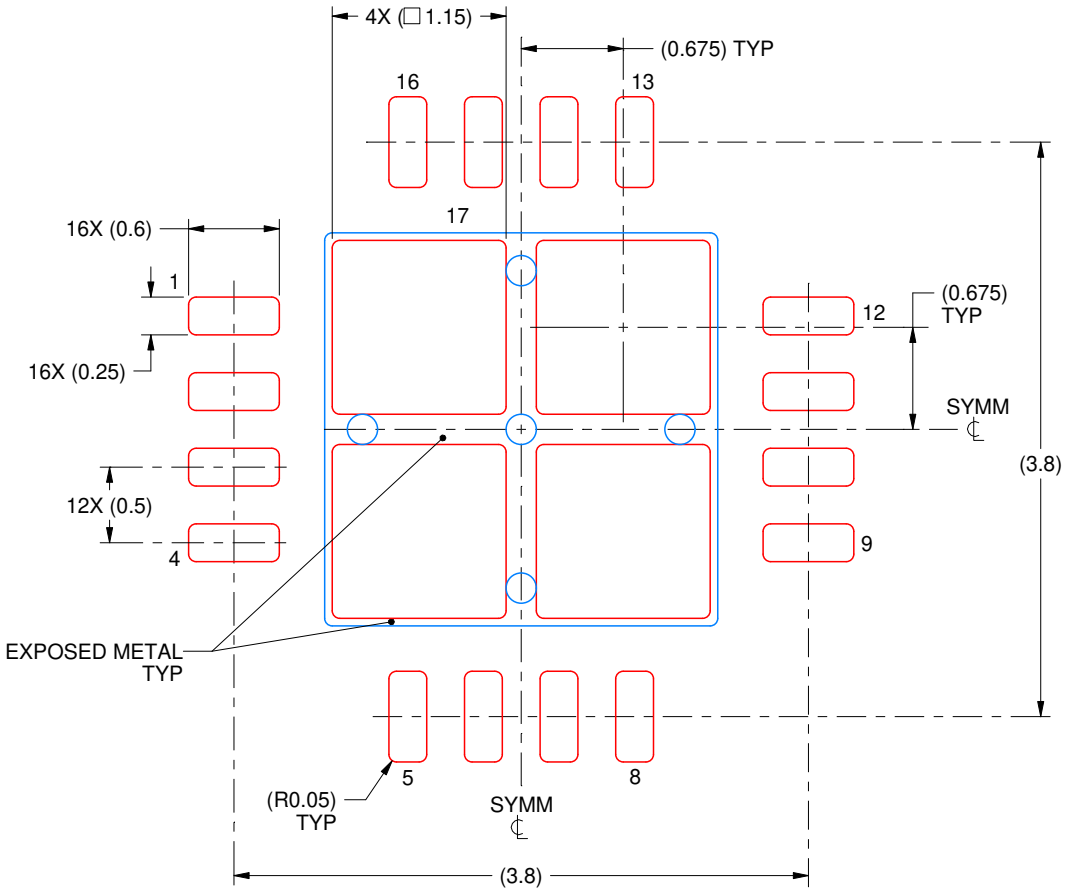


SOLDER MASK DETAILS

4214978/B 01/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4214978/B 01/2017

NOTES: (continued)

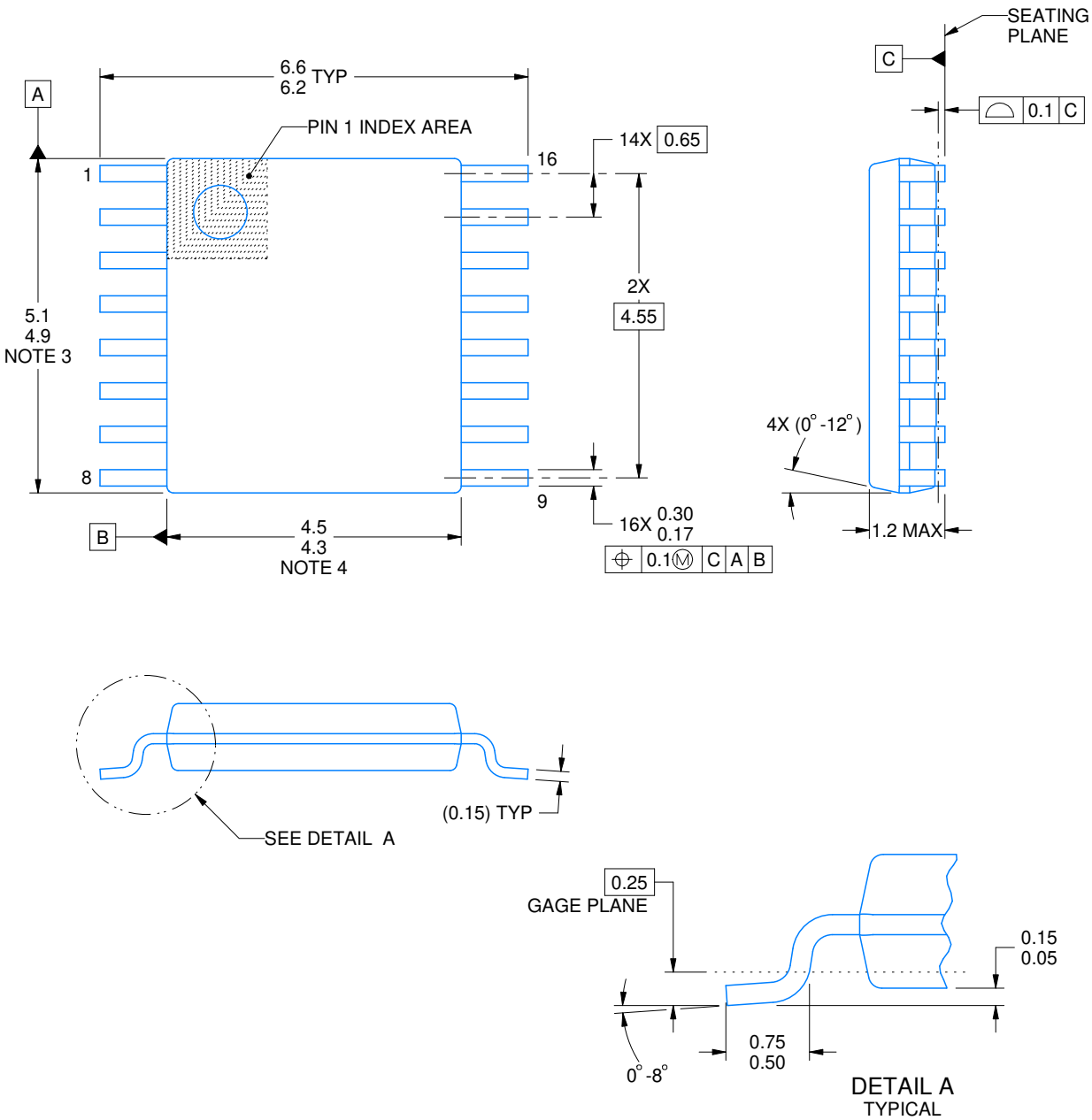
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

PW0016A

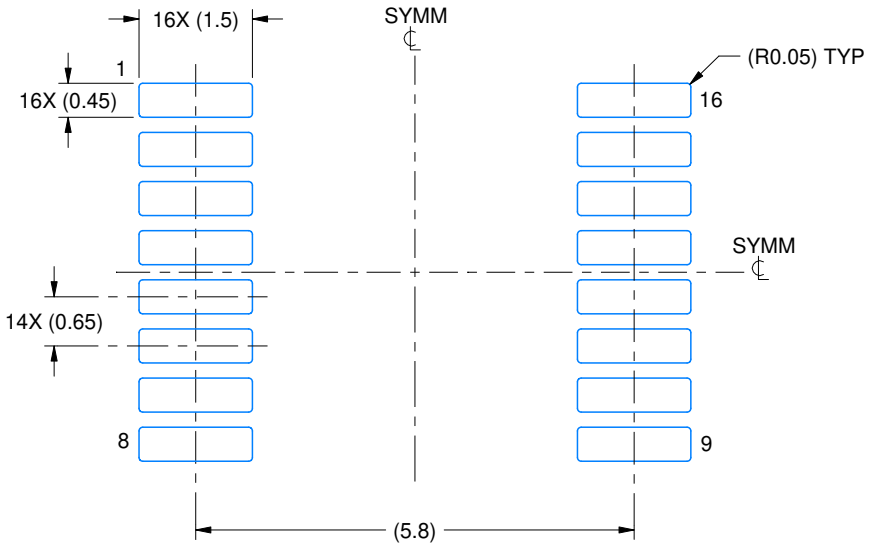
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

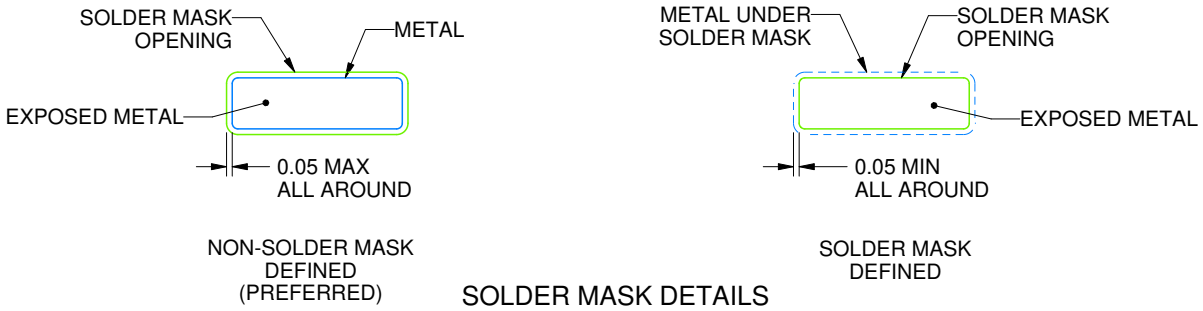


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

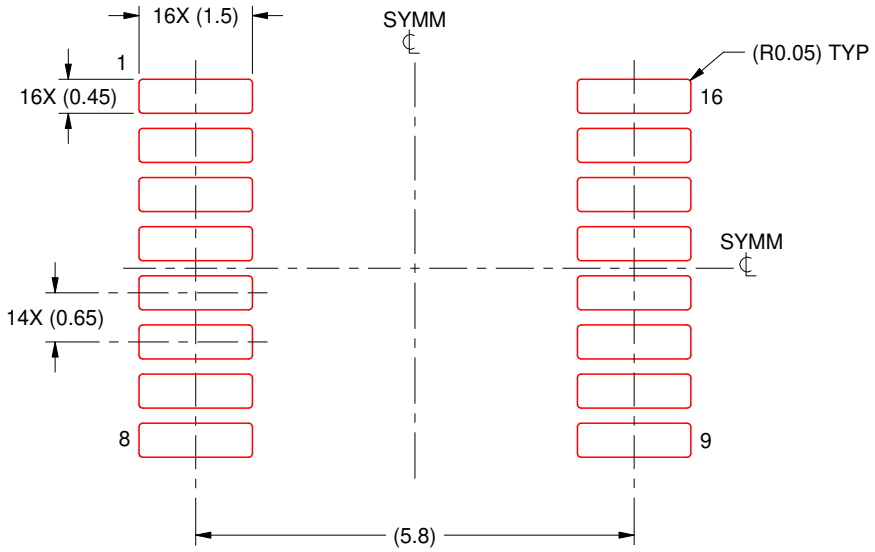


SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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