DAC161P997 Single-Wire 16-bit DAC for 4- to 20-mA Loops

1 Features

- 16-Bit Linearity
- Single-Wire Interface (SWIF), with Handshake
- Digital Data Transmission (No Loss of Fidelity)
- Pin Programmable Power-Up Condition
- Self Adjusting to Input Data Rate
- Loop Error Detection and Rreporting
- Programmable Output Current Error Level
- No External Precision Components
- Simple Interface to HART Modulator
- Small Package: WQFN-16 (4 x 4 mm, 0.5 mm Pitch)
- Key Specifications
  - Output Current TempCo: 29 ppmFS/°C (Max)
  - Long-Term Output Current Drift: 90 ppmFS (Typ)
  - INL: 3.3/−2.1 µA(Max)
  - Total Supply Current: 190 µA (Max)

2 Application

- Two-Wire, 4-20 mA Current Loop Transmitter
- Industrial Process Control
- Actuator Control
- Factory Automation
- Building Automation
- Precision Instruments
- Data Acquisition Systems
- Test Systems

3 Description

The DAC161P997 is a 16-bit ∑Δ digital-to-analog converter (DAC) for transmitting an analog output current over an industry standard 4-20 mA current loop. It offers 16-bit accuracy with a low output current temperature coefficient (29 ppm/°C) and excellent long-term output current drift (90 ppmFS) while consuming less than 190 µA.

The data link to the DAC161P997 is a Single Wire Interface (SWIF) which allows sensor data to be transferred in digital format over an isolation boundary using a single isolation component. The DAC161P997's digital input is compatible with standard isolation transformers and opto-couplers. Error detection and handshaking features within the SWIF protocol ensure error free communication across the isolation boundary. For applications where isolation is not required, the DAC161P997 interfaces directly to a microcontroller.

The loop drive of the DAC161P997 interfaces to a HART (Highway Addressable Remote Transducer) modulator, allowing injection of FSK modulated digital data into the 4-20 mA current loop. This combination of specifications and features makes the DAC161P997 ideal for 2- and 4-wire industrial transmitters.

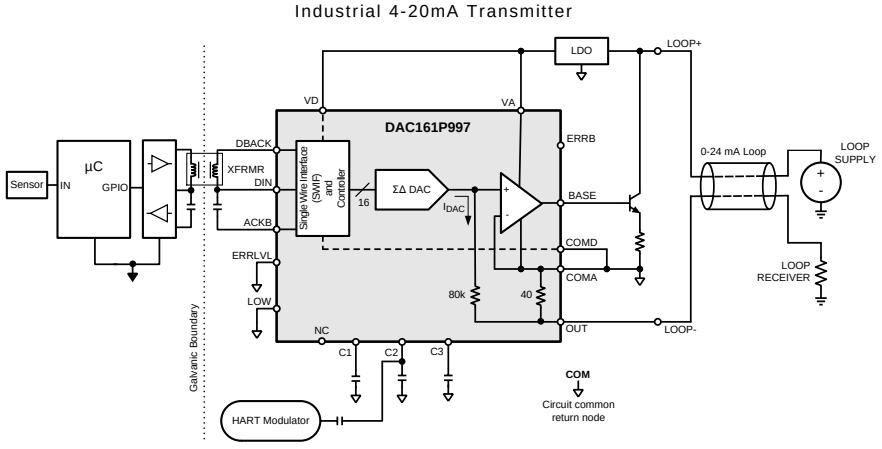
The DAC161P997 is available in a 16–lead WQFN package and is specified over the extended industrial temperature range of -40°C to 105°C.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DAC161P997	WQFN (16)	4.00 mm x 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Revision F (January 2013) to Revision G — **Page**

- Added *ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device* and *Documentation Support section,* and *Mechanical, Packaging,* and *Orderable Information section* ... 1
- Changed the second Thead to tbody/row and changed role to hdr in the Timing Requirements table ... 7
- Deleted the Related links subsection and checked for setting of single-part ... 31

Changes from Revision E (October 2013) to Revision F — **Page**

- Changed O to Ω in table ... 17

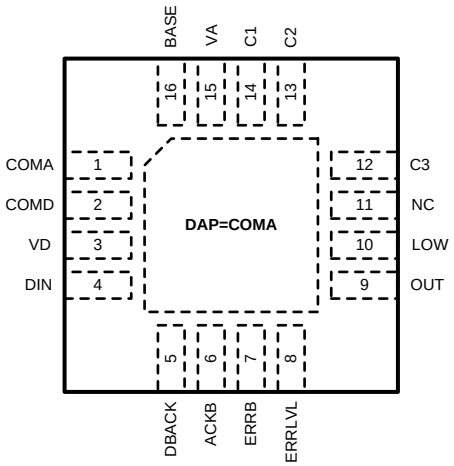
Changes from Revision D (March, 2013) to Revision E — **Page**

- Changed application circuit ... 26

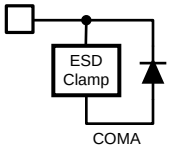
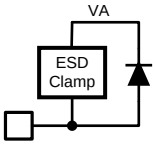
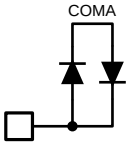
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5 Pin Configuration and Functions

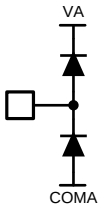
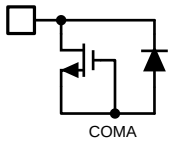
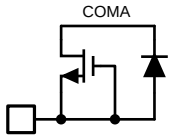
WQFN (RGH0016A)
16 pins
Top View



Pin Functions

PIN		DESCRIPTION	ESD PROTECTION
NAME	NO.		
VA	15	Analog block positive supply rail	
COMA	1	Analog block negative supply rail (local COMMMON)	
COMD	2	Digital block negative supply rail (local COMMON)	

Pin Functions (continued)

PIN		DESCRIPTION	ESD PROTECTION
NAME	NO.		
VD	3	Digital block positive supply rail	
DIN	4	SWIF input	
DBACK	5	SWIF input loop back	
ACKB	6	SWIF acknowledge output - open drain, active LOW	
ERRLVL	8	Sets the output current level at power-up	
LOW	10	Must be tied to COMA, COMD potential	
C1	14	External capacitor	
C2	13	External capacitor, HART Input	
C3	12	External capacitor	
BASE	16	External NPN base drive	
N.C.	11	User must not connect to this pin	
ERRB	7	Error flag output open drain, active LOW	
OUT	9	Loop output current source	
DAP	-	Die Attach Pad. For best thermal conductivity and best noise immunity DAP should be soldered to the PCB pad which is connected directly to circuit common node (COMA, COMD)	-

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
Supply relative to common (VA, VD to COMA, COMD)	−0.3	6	V
Voltage between any 2 pins (2)		6	V
Current IN or OUT of any pin - except OUT (2)		5	mA
Output current at OUT		50	mA
Junction Temperature			
Storage temperature range, T_{stg}	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) When the input voltage (VIN) at any pin exceeds power supplies (VIN < COMA or VIN > VA), the current at that pin must not exceed 5 mA, and the voltage (VIN) at that pin relative to any other pin must not exceed 6.0V. See *Pin Fuctions* for additional details of input structures.

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6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±5500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

	MIN	MAX	UNIT
Supply Voltage Range	2.7	3.6	V
(VA - VD)	0	0	V
(COMA - COMD)	0	0	V
BASE load to COMA	0	15	pF
OUT load to COMA	-	-	
Operating Temperature (T_A)	-40	105	°C

6.4 Thermal Information

THERMAL METRIC (1)		WQFN (16-PINS)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	35	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Unless otherwise noted, these specifications apply for VA = VD = 2.7 V to 3.6 V, T_A = 25°C, external bipolar transistor: 2N3904, R_E = 22Ω, C_1 = C_2 = C_3 = 2.2 nF.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
VA, VD	Supply Voltage	VA = VD	2.7		3.6	V
	VA Supply Current	DACCODE=0x0200 (1) -40 to 105°C			75	µA
	VD Supply Current				115	µA
	Total Supply Current				190	µA
VPOR	Power On Reset supply rail potential threshold		1.3		1.9	V
DC ACCURACY						
N	Resolution			16		Bits
INL	Integral Non-Linearity (2)	0x2AAA < DACCODE < 0xD555 (4mA < I_{LOOP} < 20 mA) -40 to 105°C	–2.1		3.3	µA
DNL	Differential Non-Linearity	See (3) -40 to 105°C	–0.2		0.2	
TUE	Total Unadjusted Error	0x2AAA < DACCODE < 0xD555	–0.23%		0.23%	FS
OE	Offset Error	See (4) -40 to 105°C	−9.16		9.16	µA
	Offset Error Temp. Coefficient				138	nA/°C

(1) At code 0x0200 the BASE current is minimal, i.e., device current contribution to power consumption is minimized. The SWIF link is inactive, i.e., after transmitting code 0x200 to the DAC161P997, there are no more transitions in the channel during the supply current measurement.
(2) INL is measured using “best fit” method in the output current range of 4 mA to 20 mA.
(3) Specified by design.
(4) Here offset is the y-intercept of the straight line defined by 4-mA and 20-mA points of the measured transfer characteristic.

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Electrical Characteristics (continued)

Unless otherwise noted, these specifications apply for VA = VD = 2.7 V to 3.6 V, T_A = 25°C, external bipolar transistor: 2N3904, R_E = 22Ω, C_1 = C_2 = C_3 = 2.2 nF.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GE	Gain Error	See (5) -40 to 105°C	−0.22%		0.22%	FS
	Gain Error Temp. Coefficient			5	29	ppmFS/°C
	4 mA Loop Current Error	DACCODE = 0x2AAA -40 to 105°C	−18		18	µA
	20 mA Loop Current Error	DACCODE = 0xD555 -40 to 105°C	−55		55	
IERRL	LOW ERROR Current	ERR_LOW = default -40 to 105°C	3361	3375	3391	
IERRH	HIGH ERROR Current	ERR_HIGH = default -40 to 105°C	21702	21750	21817	
LTD	Long Term Drift — mean shift of 12 mA output current after 1000 hrs at 150°C			90		ppmFS
LOOP CURRENT OUTPUT (OUT)						
	Output Current	Minimum tested at DACCODE = 0x01C2 (6) -40 to 105°C	0.18		24	mA
	Output Impedance		100			MΩ
	COMA to OUT voltage drop	I_{OUT} = 24 mA		960		mV
BASE OUTPUT						
	BASE short circuit output current	BASE forced to COMA potential		10		mA
DYNAMIC CHARACTERISTICS						
	Output Noise Density	1 kHz		20		nA/√Hz
	Integrated Output Noise	1 Hz to 1 kHz band		300		nA_{RMS}
SWIF I/O CHARACTERISTICS						
VIH	DIN	-40 to 105°C	0.7* VD			V
VIL	DIN	-40 to 105°C			0.3*VD	
CDIN	DIN input capacitance			10		pF
VOH	DBACK	I = 3 mA -40 to 105°C	2216			mV
		I = 5 mA -40 to 105°C	1783			
VOL	DBACK	I = 3 mA -40 to 105°C			547	
		I = 5 mA -40 to 105°C			1260	
TD	DIN to DBACK delay				8	ns
OPEN DRAIN OUTPUTS						
VOL	ACKB	I = 3 mA -40 to 105°C			550	mV
		I = 5 mA -40 to 105°C			1370	
VOL	ERRB	I = 300 µA -40 to 105°C			66	mV
		I = 3 mA -40 to 105°C			602	

(5) Here Gain Error is the difference in slope of the straight line defined by measured 4-mA and 20-mA points of transfer characteristic, and that of the ideal characteristic.
(6) This should be treated as the minimum LOOP current ensured specification.

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Electrical Characteristics (continued)

Unless otherwise noted, these specifications apply for VA = VD = 2.7 V to 3.6 V, T_A = 25°C, external bipolar transistor: 2N3904, R_E = 22Ω, C_1 = C_2 = C_3 = 2.2 nF.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IOZ	ACKB	Leakage current when output device is off -40 to 105°C			1	µA
	ERRB	Leakage current when output device is off -40 to 105°C			1	

6.6 Timing Requirements

		MIN	NOM	MAX	UNIT
SWIF TIMING, INTERNAL TIMER					
	Symbol rate: 1/TP	0.3		19.2	kHz
	“D” symbol duty cycle: THD/TP	7/16	1/2	9/16	
	“0” symbol duty cycle: TH0/TP	3/16	1/4	5/16	
	"1” symbol duty cycle: TH1/TP	11/16	3/4	13/16	
	ACKB assert: TA/TP	1/16	1/4	4/8	
	ACKB deassert: TB/TP	12/8	7/4	31/16	
TM	Timeout PeriodM	90	100	110	ms

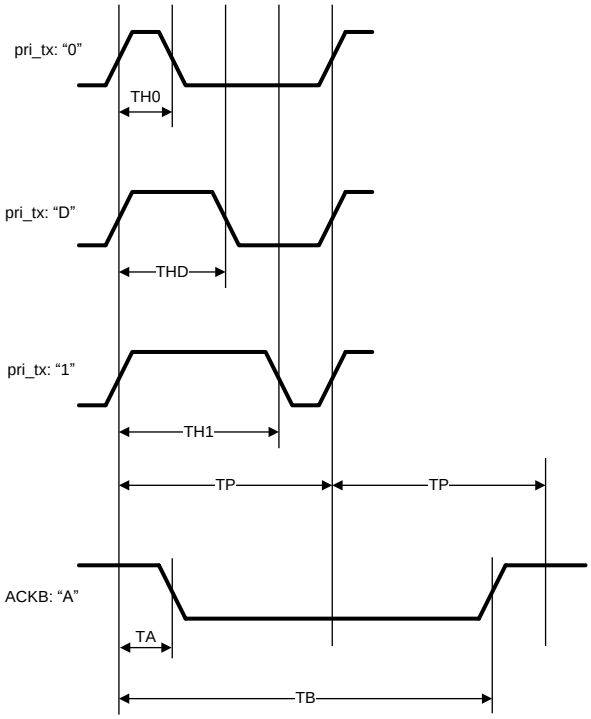


Figure 1. Single-Wire Interface (SWIF) Timing Diagram

6.7 Typical Characteristics

Unless otherwise noted, data presented here was collected under these conditions $V_A = V_D = 3.3V$, $T_A = 25°C$, external bipolar transistor: 2N3904, $R_E = 22\Omega$, $C_1 = C_2 = C_3 = 2.2$ nF.

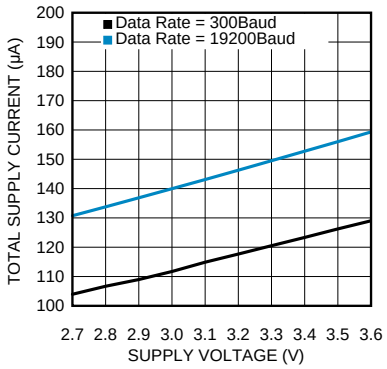


Figure 2. Supply Current vs Supply Voltage

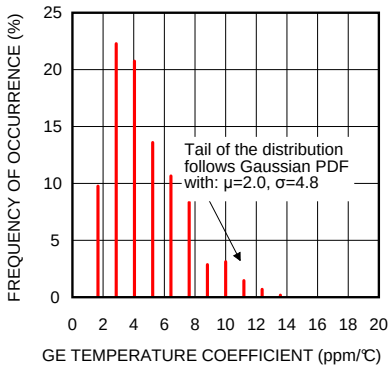


Figure 3. Gain Error TC Distribution

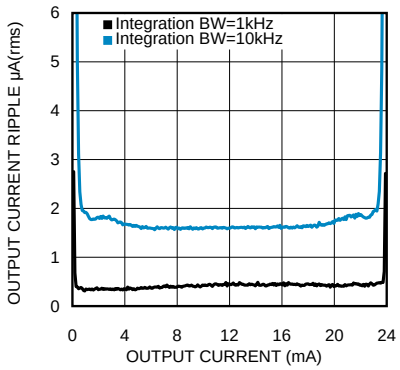


Figure 4. Integrated Noise vs I_{LOOP}

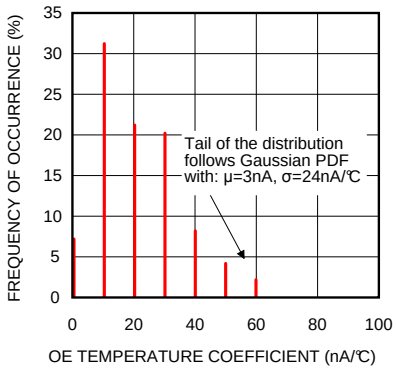


Figure 5. Offset Error TC Distribution

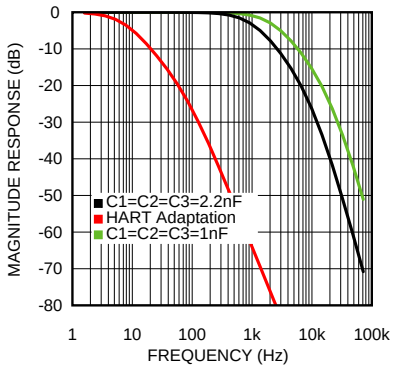


Figure 6. ΣΔ Modulator Filter Response

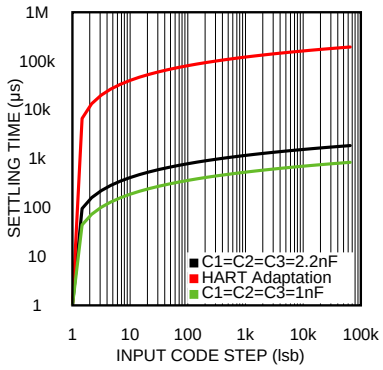


Figure 7. Settling Time vs Input Step Size

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Typical Characteristics (continued)

Unless otherwise noted, data presented here was collected under these conditions $V_A = V_D = 3.3V$, $T_A = 25°C$, external bipolar transistor: 2N3904, $R_E = 22Ω$, $C_1 = C_2 = C_3 = 2.2$ nF.

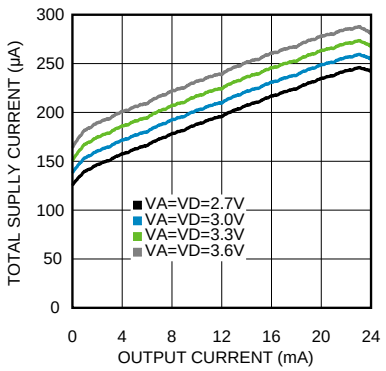


Figure 8. Supply Current vs I_{LOOP}

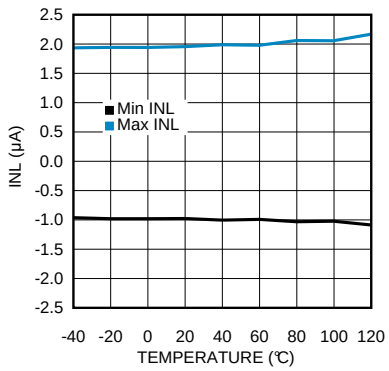


Figure 9. Output Linearity vs Temperature

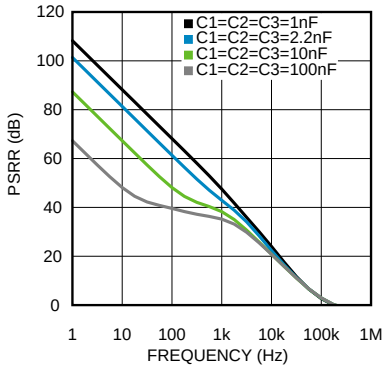


Figure 10. PSRR: I_{LOOP}=4 mA

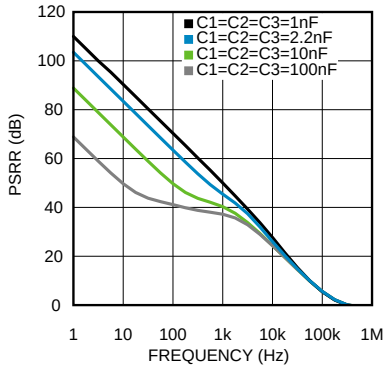


Figure 11. PSRR: I_{LOOP}=20 mA

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7 Detailed Description

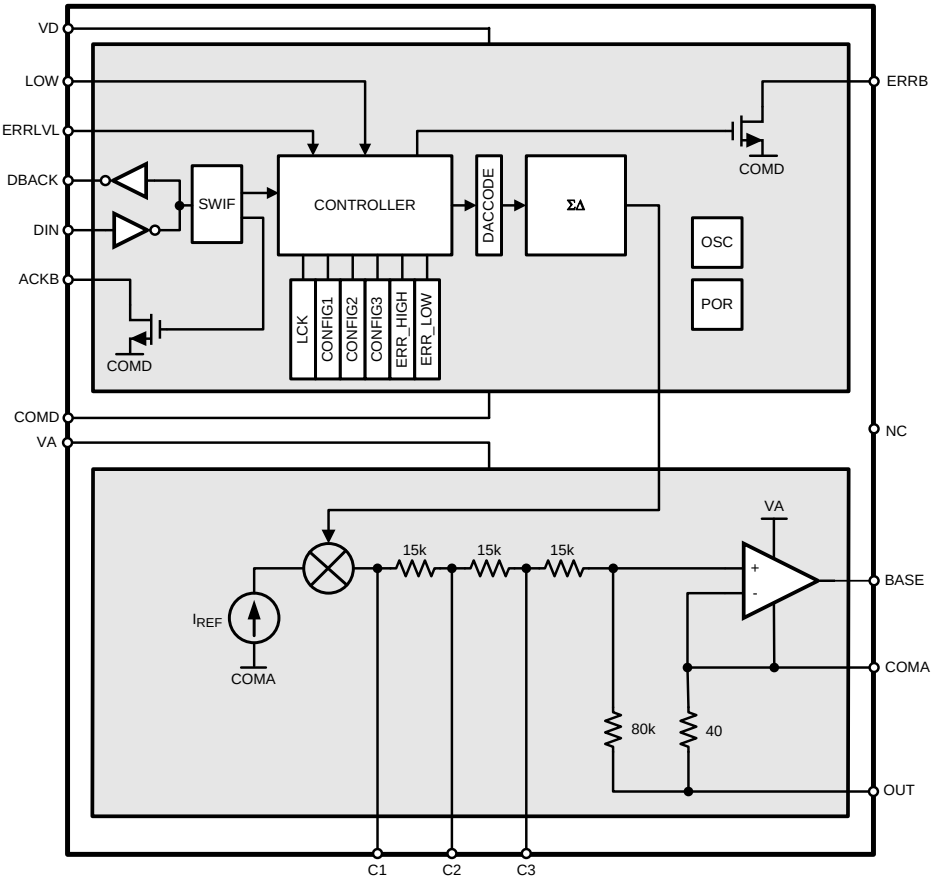
7.1 Overview

The DAC161P997 is a 16-bit DAC realized as a ∑Δ modulator. The DAC's output is a current pulse train that is filtered by the on-board low pass RC filter. The final output current is a multiplied copy of the filtered modulator output. This architecture ensures an excellent linearity performance, while minimizing power consumption of the device.

The DAC161P997 eases the design of robust, precise, long-term stable industrial systems by integrating all precision elements on-chip. Only a few external components are needed to realize a low-power, high-precision industrial 4-20 mA transmitter.

In case of a fault, or during initial power-up the DAC161P997 will output current in either upper or lower error current band. The choice of band is user selectable via a device pin. The error current value is user programmable via the SWIF link by the Master.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Error Detection and Reporting

The user can modify the CONFIG2:(LOOP | CHANNEL | PARITY | FRAME) bits to mask or enable the reporting of any of the detectable fault conditions. The DAC161P997 reports errors by asserting the ERRB signal, and by setting the current sourced by OUT to a value dictated by the state at ERRLVL pin and the contents of the ERR_HIGH and ERR_LOW registers. Once the condition causing the fault is removed the OUT will return to the last valid output level prior to the occurrence of the fault.

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Feature Description (continued)

Table 1 below summarizes the detectable faults, and means of reporting. The interval TM is governed by the internal timer and is specified in *Electrical Characteristics*.

Table 1. Error Detection and Reporting

ERROR	CAUSE	REPORTING	
		ERRB	Value used by the DAC to set OUT pin current
LOOP	The device cannot sustain the required output current at OUT pin, typically caused by drop in loop supply, or increased load impedance.	LOW	ERR_LOW
	The DAC161P997 automatically clears this fault after interval of TM and attempts to establish output current dictated by the value in the DACCODE register		
CHANNEL	no valid symbols have been received on DIN in last interval of TM	LOW	ERRLVL=1: ERR_HIGH
			ERRLVL=0: ERR_LOW
PARITY	SWIF received a valid data frame, but a bit error has been detected by parity check	LOW	ERRLVL=1: ERR_HIGH
			ERRLVL=0: ERR_LOW
FRAME	invalid symbol received, or an incorrect number of valid symbols were detected in the frame	LOW	ERRLVL=1: ERR_HIGH
			ERRLVL=0: ERR_LOW

7.3.2 Alarm Current

The DAC161P997 reports faults to the plant controller by forcing the OUT current into one of the error bands. The error current bands are defined as either above 20 mA, or below 4mA. The error band selection is done via the ERRLVL pin. The exact value of the output current used to indicate fault is dictated by the contents of ERR_HIGH and ERR_LOW registers. See *ERR_LOW* and *ERR_HIGH*.

The default settings for LOW ERROR CURRENT and HIGH ERROR CURRENT are specified in *Electrical Characteristics*

7.4 Device Functional Modes

SWIF is a versatile and robust solution for transmitting digital data over the galvanic isolation boundary using just one isolation element: a pulse transformer.

Digital data format achieves the information transmission without the loss of fidelity which usually afflicts transmissions employing PWM (Pulse Width Modulation) schemes. Digital transmission format also makes possible data differentiation: user can specify whether given data word is a DAC input to be converted to loop current, or it is a device configuration word.

SWIF was designed to use in conjunction with pulse transformer as an isolation element. The use of the transformers to cross the isolation boundary is typical in the legacy systems due to their robustness, low-power consumption, and low cost. However, system implementation is not limited to the transformer as a link since SWIF easily interfaces with opto-couplers, or it can be directly driven by a CMOS gate.

SWIF incorporates a number of features that address robustness aspect of the data link design:

Bidirectional signal flow the DAC161P997 can issue an ACKNOWLEDGE pulse back to the master transmitter, via the same physical channel, to confirm the reception of the valid data;

Error Detection SWIF protocol incorporates frame length detection and parity checks as a method of verifying the integrity of the received data;

Channel Activity Detection SWIF can monitor the data channel and raise an error flag should the expected activity drop below programmable threshold, due to , for example, damage to the physical channel.

In the typical system the Master is a micro controller. SWIF has been implemented on a number of popular micro controllers where it places minimum demands on the hardware or software resources even of the simple 8-bit devices.

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Device Functional Modes (continued)

SWIF gives the system designer flexibility is balancing the trade-offs between the data rate, activity monitoring functionality and the power consumption in the transformer coupled data channel. At lowest data rates, with long inactive inter-frame periods, the power consumed by SWIF is negligible. See *Inter-Frame Period*.

7.5 Programming

7.5.1 Single-Wire Interface (SWIF)

SWIF provides flexible and easy to implement digital data link between the Master (transmitter) and the Slave (receiver). The Master encodes the digital data into a square (NRZ) CMOS level waveform which can be generated using common microcontroller resources. The Slave (DAC161P997) translates the waveform back into a bit stream which is then interpreted as the output current update or configuration data.

SWIF can operate in both Simplex (unidirectional) and Half-Duplex (bidirectional) modes. In the DAC161P997's implementation of SWIF, an Acknowledge pulse constitutes the reverse data flowing from the Slave back to the Master.

In its simplest implementation, the waveform can be directly coupled to the DAC161P997 input. In typical systems, however, SWIF data is transmitted via the galvanic isolation element such as pulse transformer or an opto-coupler. The details of the circuit implementations are discussed in *Interface Circuit*.

Frame Format through *Symbol Set* describe the data encoding and the SWIF protocol.

7.5.1.1 Frame Format

A frame begins with a minimum of one idle symbol. There can be more than one and each has the effect of resetting the frame buffer of the DAC161P997. After idle symbol “D” a Tag Bit specifies the destination of the frame. If the tag is symbol ‘0’ then frame’s destination is the DACCODE register. If tag is a ‘1’ the destination is one of the configuration registers.

The following 16 symbols constitute the data payload. If current frame is a DAC frame, the entire payload is a single DACCODE word. If it is a configuration frame, the first byte is the register address and the second byte is the register data. Words are transmitted MSB first.

Two parity symbols follow the payload. The first parity symbol is determined by the bit parity of the tag bit and the first byte of payload (HIGH Slice) – a total of nine symbols. The second parity symbol corresponds to bit parity of the second byte of payload only (LOW Slice) – a total of 8 symbols.

P0 = [(Number of ones in LOW Slice) mod 2 == 0]

P1 = [(Number of ones in HIGH Slice) mod 2 == 0]

Symbol ‘D’ after the parity bits completes a valid frame.

The symbol “A” is optional, but if present it has to immediately follow the last “D” symbol of the frame. The duration of acknowledge symbol “A” is always twice the duration of P0 symbol preceding it. See Figure 12.

SWIF does not require that all symbols in valid frames are sent by the Master at a fixed Baud rate. Each symbol is evaluated individually and is recognized as valid as long as it conforms to the duration requirement (Tp) and its duty cycle falls outside of noise margins. (See Table 2 below.)

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Programming (continued)

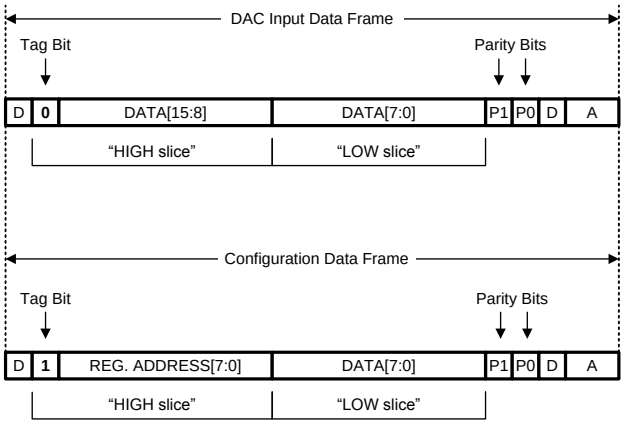


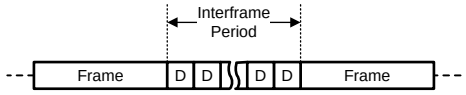
Figure 12. Data Frame Format

7.5.1.2 Inter-Frame Period

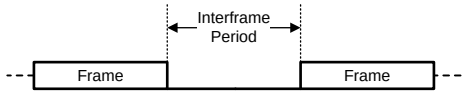
The fastest DAC update rate is achieved when Master sends the valid frames back to back, Continuous Mode, at the fastest Baud rate. This, however, results in the least power efficient implementation.



SWIF is designed to operate in the Burst Mode as well, where the valid frames are separated by the inter-frame periods that do not carry any data. The inter-frame period can be occupied by a stream of idle 'D' or 'L' symbols.



Sending the 'D' symbol in the inter-frame period provides continuous verification of integrity of the data link. The device by default monitors the activity of the SWIF link, and if the activity ceases the ERRB flag is asserted. See CONFIG2 and *Error Detection and Reporting*.



Sending the 'L' in the inter-frame period results in the transmission line being inactive (transition-free) except when the data frames are being transmitted. This is the most power efficient implementation of SWIF link, but it does not facilitate link integrity reporting. To avoid ERRB being asserted due to the channel inactivity, CONFIG2.CHANNEL should be cleared.

7.5.1.3 Symbol Set

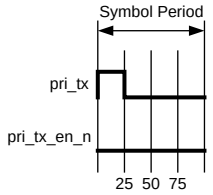
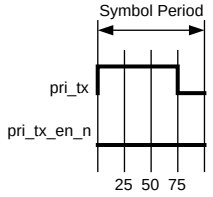
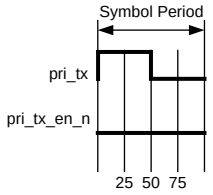
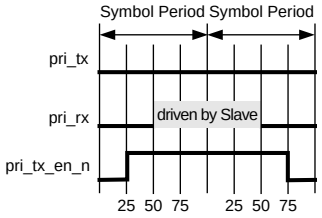
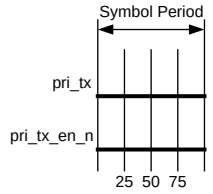
The digital data encoding scheme is outlined in the table below. The signal names in the table correspond to the nodes shown in Figure 27.

The signal waveforms due to a random symbol stream are shown in Figure 13.

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Programming (continued)

Table 2. Symbol Set Table

Character Mnemonic	SWIF Symbol	Comments
"0"		• Occupies one symbol period • Transmit from Master only • 25% duty-cycle square waveform • Terminates LOW
"1"		• Occupies one symbol period • Transmit from Master only • 75% duty-cycle square waveform • Terminates LOW
"D"		• Occupies one symbol period • Transmit from Master only • 50% duty-cycle square waveform • Terminates LOW
"A"		• Occupies **two** symbol periods • Master stops driving the SWIF and "listens" for acknowledge pulse from the Slave • Slave pulls ACKB LOW to reverse the direction of data flow through the transformer • Slave's DBACK will drive the SWIF pri_rx line between 50% points of the adjacent periods - in this interval Master must de-assert pri_tx_en_n • Terminates with pri_tx = LOW and pri_tx_en_n = LOW
"L"		• Occupies one symbol period, but can be repeated indefinitely • Transmit from Master only • Always LOW • Does not carry any meaningful information • Used as an inter-frame symbol, i.e., sent by the Master between valid data frames

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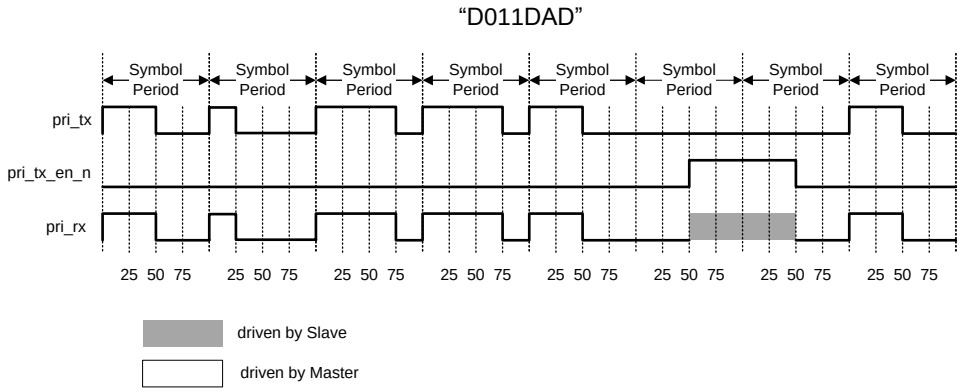


Figure 13. Symbol Stream Example

7.5.1.4 Interface Circuit

SWIF interface components are shown in Figure 14. The buffers A and B comprise a square waveform recovery circuit in applications where a pulse transformer is used to cross the galvanic isolation boundary, see *Transformer Coupled Interface - Data Flow to the DAC*. The ACKB output and its internal NMOS switch provide the means of reversing the direction of data flow through the coupling transformer see *Transformer Coupled Interface - Acknowledge Pulse*. In simple cases where the data link is DC coupled buffer A alone acts as a data receiver. The buffer C is provided for cases where improved noise immunity is required, see *DC-Coupled Interface*.

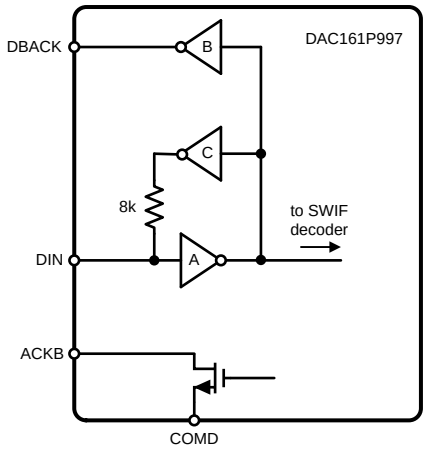


Figure 14. SWIF Front End

7.5.1.4.1 Transformer Coupled Interface - Data Flow to the DAC

In systems requiring galvanic isolation between the transmitter (micro-controller) and the receiver, the commonly used coupling element is a pulse transformer. Transformer passes only the AC components of the square input waveform resulting in an impulse train across the secondary winding. Buffers A and B form a latch circuit around the secondary winding that recovers the square waveform from the impulse train.

Figure 15 shows the details of the square waveform transmission from the primary side and recovery of the signal on the secondary side. Transmitter's DC component is blocked by the capacitor CP. The transmitter's output waveform VO results in the impulse train VP across the primary winding. Similar impulse train then appears across the secondary winding. If the magnitude of the impulse exceeds the threshold on the A buffer, the latch formed by A and B buffers will change state. The new latch state will persist until an opposite polarity impulse appears across the secondary winding.

Note that in Figure 15 the capacitor CS bottom plate floats, and thus does not affect the operation of this circuit.

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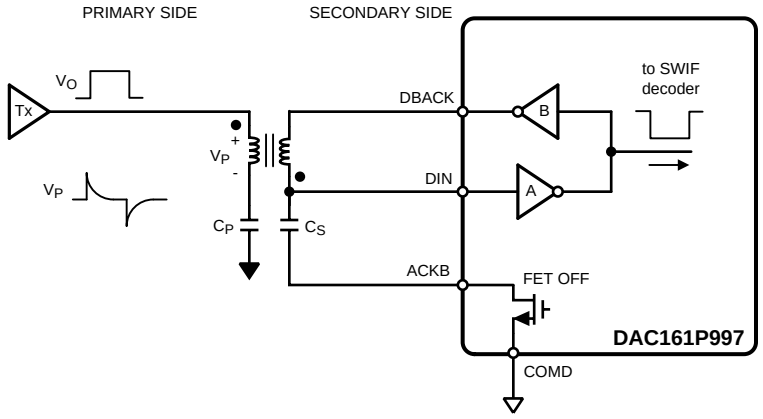


Figure 15. Transformer-Coupled SWIF Link With the DAC161P997 as Receiver

7.5.1.4.2 Transformer Coupled Interface - Acknowledge Pulse

Since the transformer is a symmetrical device (particularly one with 1:1 winding ratio), it is simple to reverse the data flow through it.

Figure 16 shows the SWIF interface circuit during the transmission of the Acknowledge pulse from the DAC161P997 on the secondary side back to the micro-controller on the primary side.

On the secondary side buffer B drives the square waveform across the transformer. Capacitor CS, whose bottom plate is now grounded via the ACKB pin, blocks the DC component of the square waveform. Buffer A is inactive.

On the primary side a square waveform recovery is performed by the now familiar latch.

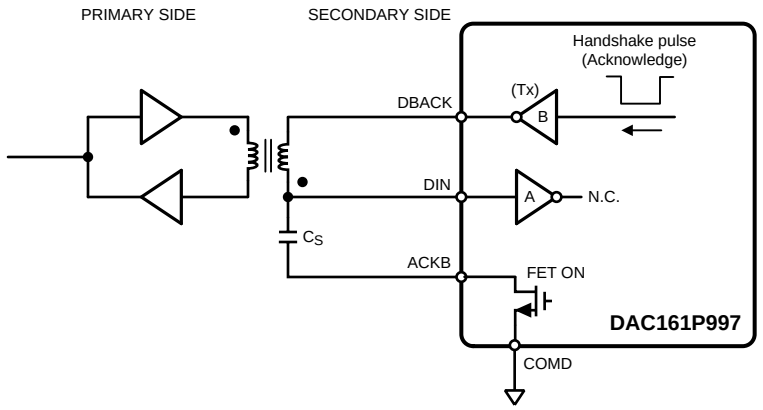


Figure 16. Transformer-Coupled SWIF Link With the DAC161P997 as Transmitter

7.5.1.4.3 DC-Coupled Interface

DC coupled signal path between the transmitter and the receiver is shown in Figure 17. Such circuit as the internal buffer A is sufficient for the signal recovery as the signal presented at the DIN input is a square CMOS level waveform.

In noisy environments it may be necessary to implement a Hysteresis loop around the DIN input to improve noise immunity of the input circuit. Presence of the buffer C and its output resistor facilitate this. The Hysteresis can be easily realized by inserting R_{IN} between the transmitter and DIN input.

Note that when R_{IN} = 0 the presence of the buffer C can be ignored.

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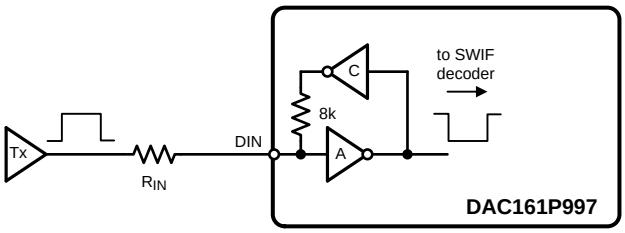


Figure 17. DC-Coupled SWIF Input

7.5.1.4.4 Transformer Selection and SWIF Data Link Circuit Design

In general, the transformers developed for T1/E1 telecom applications are well suited as the interface element for the DAC161P997 in the galvanically isolated industrial transmitter. The application circuit schematic utilizing T1/E1 transformer as the isolation element is shown in *Typical Application*. A number of suggested off the shelf transformers are listed in Table 3.

Table 3. Examples of Transformers Suitable in the DAC161P997 Applications

Manufacturer	P/N	L_M (mH)	L_{LP}/L_{LS} (µH)	R_P/R_S (Ω)	C_{WW} (pF)	Isolation Voltage (Vrms)
Pulse	TX1491	1.2	1.2	2.7	35	1500
Coilcraft	S5394–CLB	0.4	Not Specified	0.95	0.92	1500
Halo	TG02-1205	1.2	Not Specified	0.7	30	1500
XFMRS	XF7856-GD11	0.785	0.5	0.52	Not Specified	1500

Model suitable for simulating the behavior of the pulse transformer is shown in Figure 18. The model parameters are readily available in the datasheets provided by the transformer manufacturers, see Table 3 for examples.

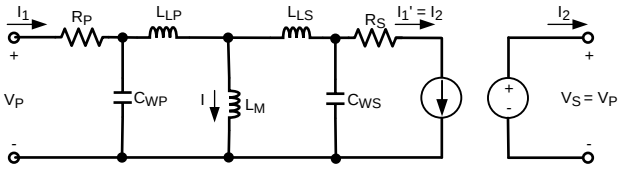


Figure 18. Pulse Transformer Model - Winding Ratio 1:1

Table 4. Transformer Model Parameters' Legend

Parameter	Description
L_M	Magnetizing inductance, in Data Sheets shown as OCL (open circuit inductance)
$L_{LP/S}$	Leakage inductance of the primary (secondary) winding
$C_{WP/S}$	Winding capacitance. Dominated by the CWW (winding to winding) component. Here it is assumed that CWS=CWP=½CWW
$R_{P/S}$	Winding resistance

The circuit behavior will be dominated by the DC blocking capacitance C_P and the magnetizing inductance L_M. In the example circuit shown in Figure 19 the rising edge of VO ultimately results in an impulse at the input DIN, see Figure 20. Once voltage at DIN is above VIH of the A buffer, the A buffer will change its state. However, the latch will acquire a new state only if the voltage at DIN persists above VIH for T_{PEAK} > TD.

The parasitic elements in the transformer model: L_{LS}, L_{SP}, C_{WS}, C_{WP} may result in the oscillating component superimposed on the dominant impulse response waveform shown in Figure 20. The oscillation should be controlled so that the condition T_{PEAK}> TD is maintained. The typical method for controlling this parasitic oscillation is to insert a damping element into the signal path. A small resistance in series with transformer winding is such damping element. The typical application example in *Typical Application* illustrates this.

The delay around the SWIF input latch, from DIN to DBACK, TD is specified in *Electrical Characteristics*.

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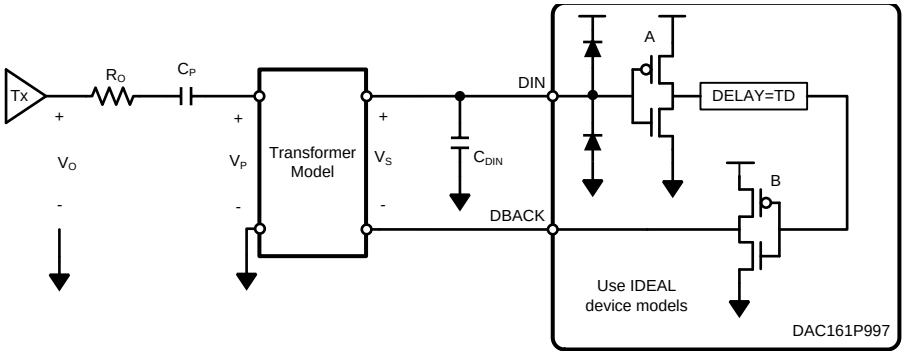


Figure 19. NRZ Waveform Transmission and Recovery Circuit Model

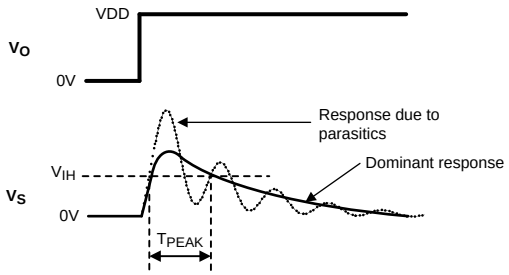


Figure 20. SWIF Link Circuit Response to Step-Input

7.6 Register Maps

7.6.1 LCK

Address=0x00; Default=0x00		
Bit Field	**Name**	**Description**
7:0		0x95 - registers unlocked 0x** - any value written locks registers A register lock prevents inadvertent changes to the configuration. The DAC output cannot be updated while software configuration registers are unlocked.

7.6.2 CONFIG1

Address=0x01; Default=0x08		
Bit Field	**Name**	**Description**
7:5		RESERVED. Always write 0.
4:3	SERR	0b00 - NOP 0b01 - set error 0b10 - clear error 0b11 - NOP Sets or clears the error condition. At power-on the error is set. Error is also cleared after reception of valid SWIF frame. These bits are self clearing. This functionality can be used for diagnostic purposes, e.g. Master can use SERR to force I_{LOOP} into an error band, and then return it to previously held output level.
2:1		RESERVED. Always write 0.
0	RST	0 - NOP 1- same as power-on reset. Once device is reset to default state the bit clears automatically

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7.6.3 CONFIG2

Address=0x02; Default=0x1F		
Bit Field	**Name**	**Description**
7:5		RESERVED. Always write 0.
4	ACK_EN	Set to enable ACK When enabled, an acknowledgement is indicated on the serial interface upon detection of each valid frame. See *Frame Format*.
3	FRAME	Set to enable framing error reporting. See table in *Error Detection and Reporting*.
2	PARITY	Set to enable parity error reporting. See table in *Error Detection and Reporting*.
1	CHANNEL	Set to enable channel-inactive reporting. See table in *Error Detection and Reporting*.
0	LOOP	Set to enable loop error reporting. See table in *Error Detection and Reporting*.

7.6.4 CONFIG3

Address=0x03; Default=0x08		
Bit Field	**Name**	**Description**
7:4		RESERVED. Always write 0.
3:0	RX_ERR_CNT	0 <= RX_ERR_CNT ≤ 15 Threshold = 1 + RX_ERR_CNT The slave enters the error state once 'Threshold' number of consecutive FRAME or PARITY errors are counted. The threshold is programmable to prevent occasional errors from being reported. See table in *Error Detection and Reporting*.

7.6.5 ERR_LOW

Address=0x04; Default=0x24		
Bit Field	**Name**	**Description**
7:0		8-bit value. If ERRLVL = LOW, the DAC will use the value stored in ERR_LOW register to set the output current sourced from OUT pin when reporting an error condition. The ERR_LOW value is used as the upper byte of the DACCODE, while the lower byte is forced to 0x00. At power up the ERR_LOW defaults to a value which forces IERRL output current. See *Electrical Characteristics*.

7.6.6 ERR_HIGH

Address=0x05; Default=0xE8		
Bit Field	**Name**	**Description**
7:0		If ERRLVL = HIGH, the DAC will use the value stored in ERR_HIGH register to set the output current sourced from OUT pin when reporting an error condition. The ERR_HIGH value is used as the upper byte of the DACCODE, while the lower byte is forced to 0x00. At power-up the ERR_HIGH defaults to a value which forces IERRH output current. See *Electrical Characteristics*.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 16-BIT DAC and Loop Drive

8.1.1.1 DC Characteristics

The DAC converts the 16-bit input code in the DACCODE register to an equivalent current output. The ∑Δ DAC output is a current pulse which is then filtered by a 3rd order RC low-pass filter and boosted to produce the loop current I_{LOOP} at the device OUT pin.

Figure 21 shows the principle of operation of the DAC161P997 in the Loop Powered Transmitter - the circuit details were omitted for clarity. In this figure I_D and I_A represent supply (quiescent) currents of the internal digital and analog blocks. I_{AUX} represents supply (quiescent) current of companion devices present in the system, such as the voltage regulator and the SWIF channel.

By observing that the control loop formed by the amplifier and the bipolar transistor forces the voltage across R_1 and R_2 to be equal, it can be shown that, under normal conditions, the I_{LOOP} is dependent only on I_{DAC} through the following relationship:

$$I_{LOOP} = \left(1 + \frac{R1}{R2}\right) I_{DAC}, \text{where } I_{DAC} = f(\text{DACCODE}) \quad (1)$$

While I_{LOOP} has a number of component currents, $I_{LOOP} = I_{DAC}+I_D+I_A+I_{AUX}+I_E$, it is only I_E that is regulated by the loop to maintain the relationship shown above.

Since it is only I_E's magnitude that is controlled, not its direction, there is a lower limit to I_{LOOP}. This limit is dependent on the fixed components I_A and I_D, and on system implementation through I_{AUX}.

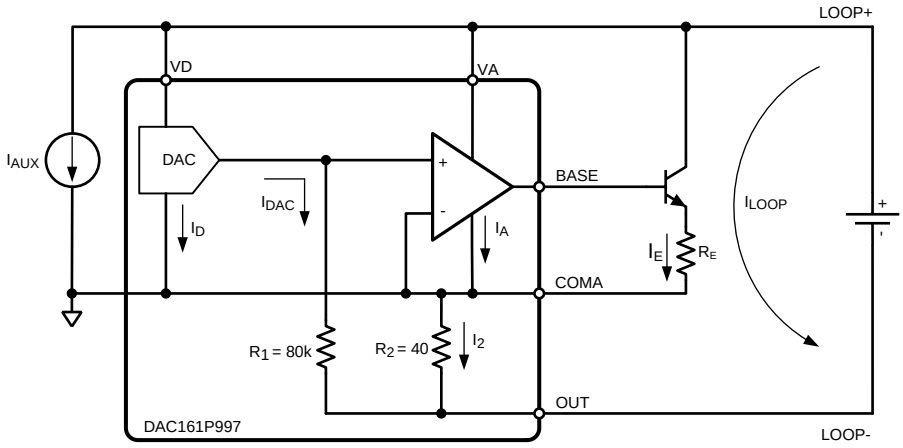


Figure 21. Loop-Powered Transmitter

Figure 22 shows the variant of the transmitter where the supply currents to the system blocks are provided by the local supply, and not the 4 - 20 mA loop Self-Powered Transmitter. Same basic relationship between the I_{LOOP} and I_{DAC} holds, but the component currents of I_{LOOP} are only I_{DAC} and I_E.

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Application Information (continued)

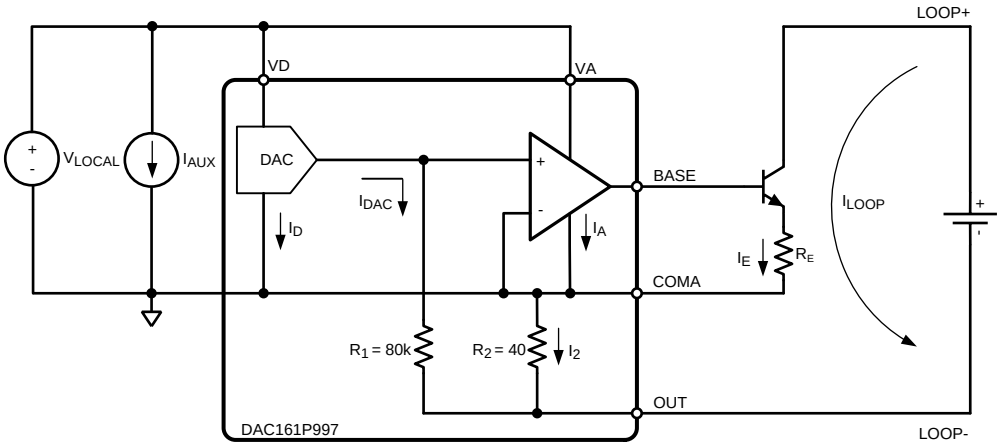


Figure 22. Self-Powered Transmitter

8.1.1.1.1 DC Input-Output Transfer Function

The output current sourced by the OUT pin of the device is expressed by:

$$I_{LOOP} = \left(\frac{DACCODE}{2^{16}}\right) 24mA \quad (2)$$

The valid DACCODE range is the full 16-bit code space (0x0000 to 0xFFFF), which results in the I_{DAC} range of 0 to approximately 12 µA. This, however, does not result in the I_{LOOP} range of 0 to 24 mA.

The maximum output current sourced out of OUT pin, I_{LOOP}, is 24 mA. The minimum output current is dependent on the system implementation. The minimum output current is the sum of supply currents of the DAC161P997 internal blocks, I_A, I_D, and companion devices present in the system, I_{AUX}. The last component current I_E can theoretically be controlled down to 0 but, due to the stability considerations of the control loop, it is advised not to allow the I_E to drop below 200 µA.

The graph in Figure 23 shows the DC transfer characteristic of the 4 - 20 mA transmitter, including minimum current limits. The minimum current limit for the Loop-Powered Transmitter is typically around 400 µA (I_D+I_A+I_{AUX}+I_E). The minimum current limit for the Self-Powered Transmitter is typically around 200 µA (I_E).

Typical values for I_D and I_A are listed in *Electrical Characteristics*. I_E depends on the BJT device used.

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Application Information (continued)

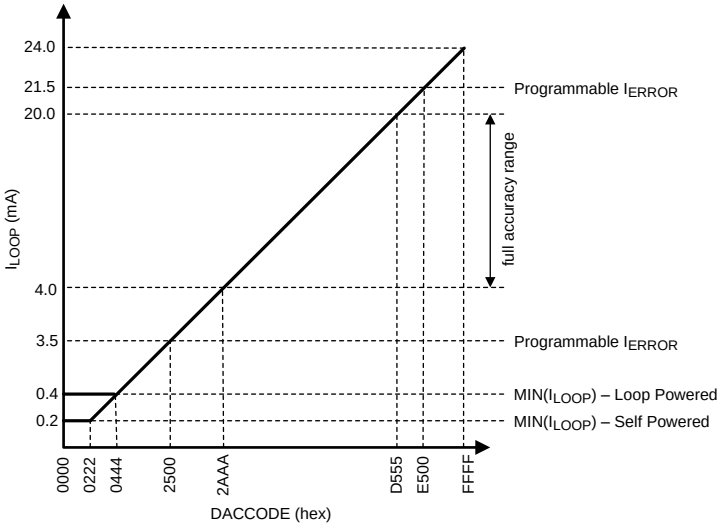


Figure 23. DAC-DC Transfer Function

8.1.1.1.2 Loop Interface

The DAC161P997 cannot directly interface to the typical 4 - 20 mA loop due to the excessive loop supply voltage. The loop interface has to provide the means of stepping down the LOOP Supply down to 3.6V. This can be accomplished with either a linear regulator (LDO) or switching regulator while keeping in mind that the regulator's quiescent current will have direct effect on the minimum achievable I_{LOOP} (see *DC Input-Output Transfer Function*).

The second component of the loop interface is the external NPN transistor (BJT). This device is part of the control circuit that regulates the transmitter's output current (I_{LOOP}). Since the BJT operates over the wide current range, spanning at least 4 - 20 mA, it is necessary to degenerate the emitter in order to stabilize transistor's transconductance (g_m). The degeneration resistor of 22Ω is suggested in typical applications. For circuit details, see *Typical Application*.

The NPN BJT should not be replaced with an N-channel FET (Field Effect Transistor) for the following reasons: discrete FET's typically have high threshold voltages (VT), in the order of 1.5 V to 2 V, which is beyond the BASE output maximum range; discrete FET's present higher load capacitance which may degrade system stability margins; and BASE output relies on the BJT's base current for biasing.

8.1.1.1.3 Loop Compliance

The maximum V(LOOP+,LOOP-) potential is limited by the choice of step-down regulator, and the external BJT's Collector Emitter breakdown voltage. For minimum V(LOOP+, LOOP−) potential consider Figure 22. Here, observe that V(LOOP+,LOOP−) ≅ min(V_{CE}) + $I_{LOOP}R_E$ + $I_{LOOP}R_2$ = min(V_{CE}) + 0.53V + 0.96V = 3.66V, at I_{LOOP} = 24mA. The voltage drop across internal R_2 is specified in *Electrical Characteristics*.

8.1.1.2 AC Characteristics

The approximate frequency dependent characteristics of the loop drive circuit can be analyzed using the circuit in Figure 24:

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Application Information (continued)

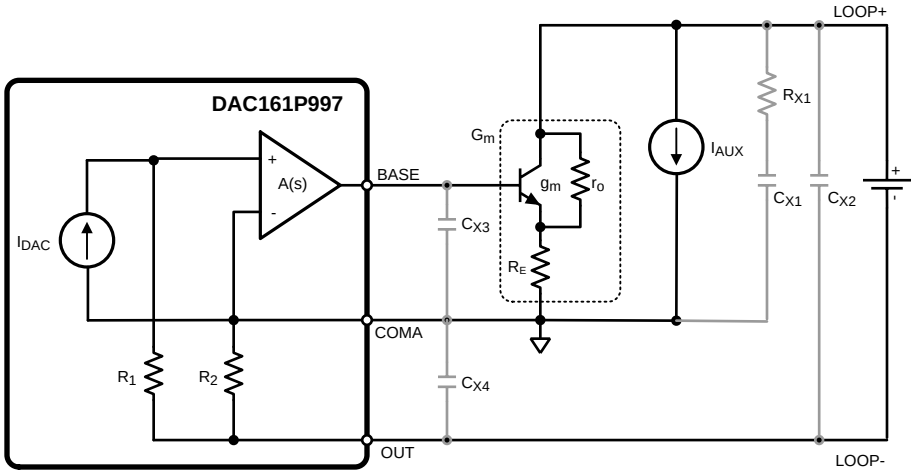


Figure 24. Capacitances Affecting Control Loop

Here it is assumed that the internal amplifier dominates the frequency response of the system, and it has a single pole response. The BJT's response, in the bandwidth of the control loop, is assumed to be frequency independent and is characterized by the transconductance g_m and the output resistance r_o.

As in previous sections I_{DAC} and I_{AUX} represent the filtered output of the ∑Δ modulator and the quiescent current of the companion devices.

The circuit in Figure 24 can be further simplified by omitting the on-board capacitances, whose effect will be discussed in *Stability*, and by combining the amplifier, the external transistor and resistor R_E into one G_m block. The resulting circuit is shown in Figure 25.

By assuming that the BJT's output resistance (r_o) is large, the loop current I_{LOOP} can be expressed as:

$$I_{LOOP} = I_{AUX} + A(s)\,G_m\,v_e \tag{3}$$

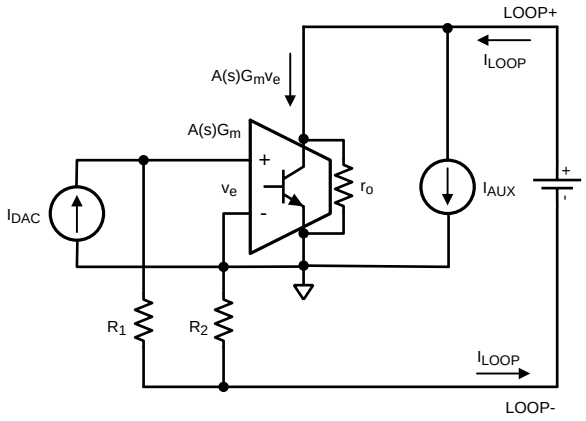


Figure 25. AC Analysis Model of a Transmitter

The sum of voltage drops around the path containing R_1, R_2 and v_e is:

$$v_e = I_{DAC}R_1 - \left[I_{AUX} + A(s)G_m v_e - I_{DAC}\right]R_2 \tag{4}$$

an assumption is made on the response of the internal amplifier::

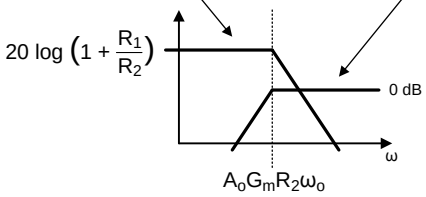
$$A(s) = \frac{A_o \omega_o}{s} \tag{5}$$

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Application Information (continued)

By combining the above the final expression for the I_{LOOP} as a function of 2 inputs I_{DAC} and I_{AUX} is:

$$I_{LOOP} = I_{DAC}\left(1 + \frac{R_1}{R_2}\right)\frac{A_o G_m R_2 \omega_o}{s + A_o G_m R_2 \omega_o} + I_{AUX}\frac{s}{s + A_o G_m R_2 \omega_o}$$



(6)

The result above reveals that there are 2 distinct paths from the inputs I_{DAC} and I_{AUX} to the output I_{LOOP}. I_{DAC} follows the low-pass, and the I_{AUX} follows the high-pass path.

In both cases the corner frequency is dependent on the effective transconductance, G_m, of the external transistor. This implies that control loop dynamics could vary with the output current I_{LOOP} if G_m were allowed to be just native device transconductance g_m. This undesirable behavior is mitigated by the degenerating resistor R_E which stabilizes G_m as follows:

$$G_m \cong \frac{1}{\frac{1}{g_m} + R_E} \cong \frac{1}{R_E} \tag{7}$$

This results in the frequency response which is largely independent of the output current I_{LOOP}:

$$I_{LOOP} = I_{DAC}\left(1 + \frac{R_1}{R_2}\right)\frac{A_o \frac{R_2}{R_E}\omega_o}{s + A_o \frac{R_2}{R_E}\omega_o} + I_{AUX}\frac{s}{s + A_o \frac{R_2}{R_E}\omega_o} \tag{8}$$

While the bandwidth of the I_{DAC} path may not be of great consequence given the low frequency nature of the 4-20 mA current loop systems, the location of the pole in the I_{AUX} path directly affects PSRR of the transmitter circuit. This is further discussed in *PSRR*.

8.1.1.2.1 Step Response

The transient input-output characteristics of the DAC161P997 are dominated by the response of the RC filter at the output of the ∑Δ DAC. Settling times due to step input are shown in *Typical Characteristics*.

8.1.1.2.2 Output Impedance

The output impedance is described as:

$$R_{OUT} = \frac{\Delta V_{LOOP}}{\Delta I_{LOOP}} \tag{9}$$

By considering the circuit in Figure 25, and setting $I_{DAC} = I_{AUX} = 0$, the following expression can be obtained:

$$R_{OUT}(s) = R_2 + \left[1 + A(s) G_m R_2\right] r_o \tag{10}$$

As in *AC Characteristics* an assumption can be made on the frequency response of the internal amplifier, and the effective transconductance G_m should be stabilized with external R_E leading to:

$$R_{OUT}(s) \approx \frac{A_o\left(\frac{R_2}{R_E}\right)\omega_o r_o}{s} \tag{11}$$

The output impedance of the transmitter is a product of the external BJT's output resistance r_o, and the frequency characteristics of the internal amplifier. At low frequencies this results in a large impedance that does not significantly affect the output current accuracy.

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Application Information (continued)

8.1.1.2.3 PSRR

Power Supply Rejection Ratio is defined as the ability of the current control loop to reject the variations in the supply current of the companion devices, I_{AUX}. Specifically:

$$PSRR = 20 \times \log_{10}\left(\frac{\Delta I_{LOOP}}{\Delta I_{AUX}}\right) \quad (12)$$

It was shown in *AC Characteristics* that the I_{AUX} affects I_{LOOP} via the high-pass path whose corner frequency is dependent on the effective Gm of the external BJT. If that dependence were not mitigated with the degenerating resistor R_E, the PSRR would be degraded at low output current I_{LOOP}.

The typical PSRR performance of the transmitter shown in *Typical Application* is shown in *Typical Characteristics*.

8.1.1.2.4 Stability

The current control loop's stability is affected by the impedances present in the system. Figure 24 shows the simplified diagram of the control loop, formed by the on-board amplifier and an external BJT, and the lumped capacitances C_{X1} through C_{X4} that model any other external elements.

C_{X1} typically represents a local step-down regulator, or LDO, and any other companion devices powered from the LOOP+. This capacitance reduces the stability margins of the control loop, and therefore it should be limited. RX1 can be used to isolate C_{X1} from LOOP+ node and thus remedy the stability margin reduction. If $R_{X1} = 0$, C_{X1} cannot exceed 10 nF. $R_{X1} = 200\Omega$ is recommended if it can be tolerated. Minimum $R_{X1} = 40\Omega$ if C_{X1} exceeds 10 nF.

C_{X3} also adversely affects stability of the loop and it must be limited to 20 pF. C_{X4} affects the control loop in the same way as C_{X1}, and it should be treated in the same way as C_{X1}. C_{X2} is the only capacitance that improves stability margins of the control loop. Its maximum size is limited only by the safety requirements.

Stability is a function of I_{LOOP} as well. Since I_{LOOP} is approximately equal to the collector current of the external BJT, G_m of the BJT, and thus loop dynamics, depend on I_{LOOP}. This dependence can be reduced by degenerating the emitter of the BJT with a small resistance as discussed in *Loop Interface*. Inductance in series with the LOOP+ and LOOP− do not significantly affect the control loop.

8.1.1.2.5 Noise and Ripple

The output of the DAC is a current pulse train. The transition density varies throughout the DAC input code range (I_{LOOP} range). At the extremes of the code range, the transition density is the lowest which results in low frequency components of the DAC output passing through the RC filter. Hence, the magnitude of the ripple present in I_{LOOP} is the highest at the ends of the transfer characteristic of the device (see *Typical Characteristics*).

It should be noted that at wide noise measurement bandwidth, it is the ripple due to the ∑Δ modulator that dominates the noise performance of the device throughout the entire code range of the DAC. This results in the "U" shaped noise characteristic as a function of output current. At narrow bandwidths, and particularly at mid-scale output currents, it is the amplifier driving the external BJT that starts to dominate as a noise source.

8.1.1.2.6 Digital Feedthrough

Digital feedthrough is indiscernible from the ripple induced by the ∑Δ modulator.

8.1.1.2.7 HART Signal Injection

The HART specification requires minimum suppression of the sensor signal in the HART signal band (1-2 kHz) of about 60 dB. The filter in Figure 26 below meets that requirement.

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Application Information (continued)

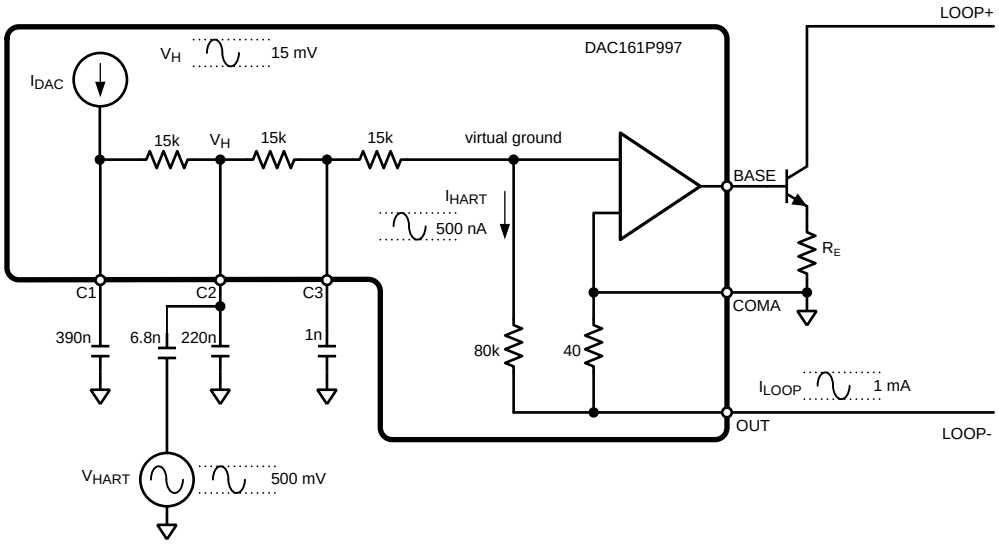
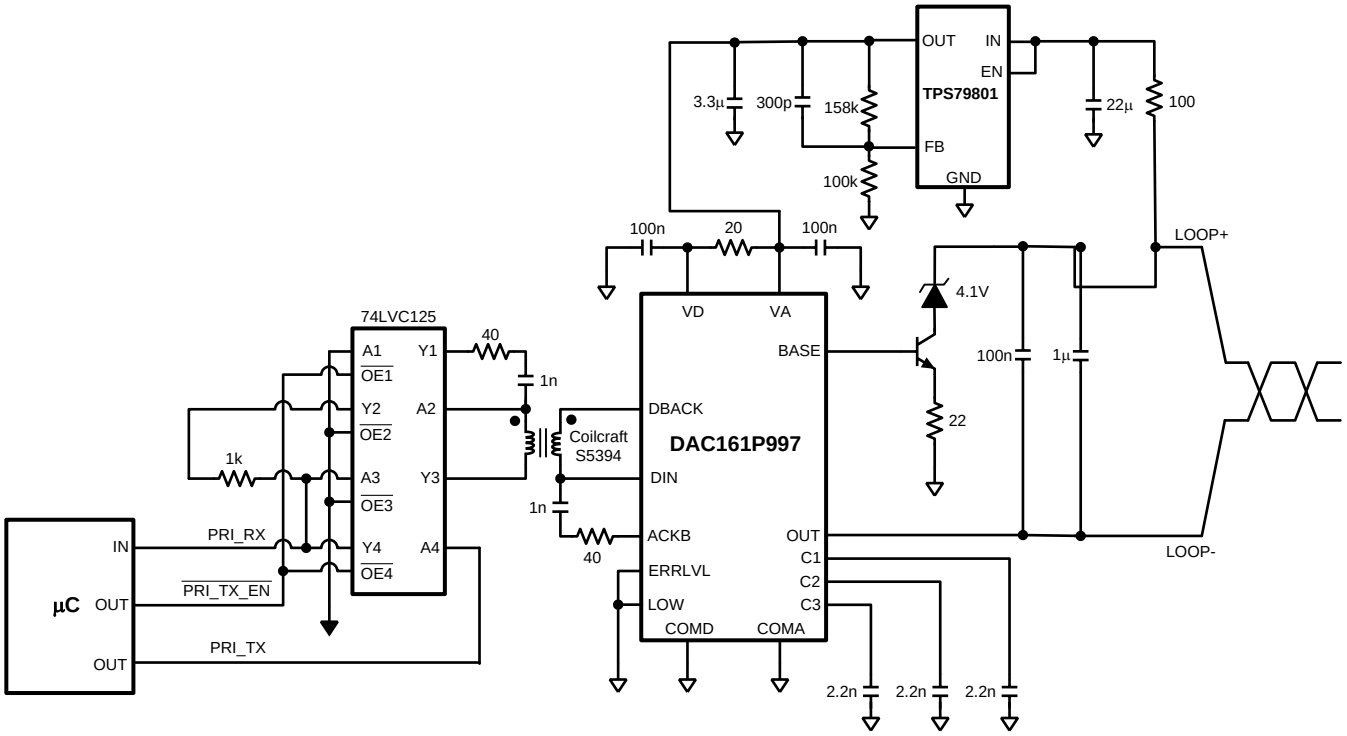


Figure 26. HART Signal Injection

8.1.1.2.8 RC Filter Limitation

In an effort to speed up the transient response of the device the user can reduce the capacitances associated with the low-pass filter at the output of the ∑Δ modulator. However, to maintain stability margins of the current control loop it is necessary to have at least $C_1 = C_2 = C_3 = 1nF$.

8.2 Typical Application



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Typical Application (continued)

8.2.1 Design Requirements

An example of implementation of the SWIF data link is shown in Detailed Design Procedure below. This implementation uses the components already present in the systems employing the standard methods for PWM signal transmission over an isolation boundary. Additional configuration examples show how the system can be expanded or simplified depneding on the requirements of hte system and capabilities of the Master controller.

8.2.2 Detailed Design Procedure

In this example Master uses 2 digital I/Os:

- One bidirectional port for transmitting encoded data to, and receiving the acknowledge signal from the slave – pri_tx/pri_rx.
- One output sourcing the pri_tx_en_n signal that governs the direction of the data flow over the SWIF link.

While transmitting, Master drives the pri_tx_en_n LOW and sources data stream onto the pri_tx. The circuit path is through buffer ‘a’, transformer primary winding, DC blocking capacitor to GND.

While receiving, Master drives the pri_tx_en_n HIGH and ‘listens’ for acknowledge signal pri_rx. In this mode the buffers ‘a’ and ‘b’ form the latch around the transformer winding, and buffer ‘c’ floats the DC blocking capacitor.

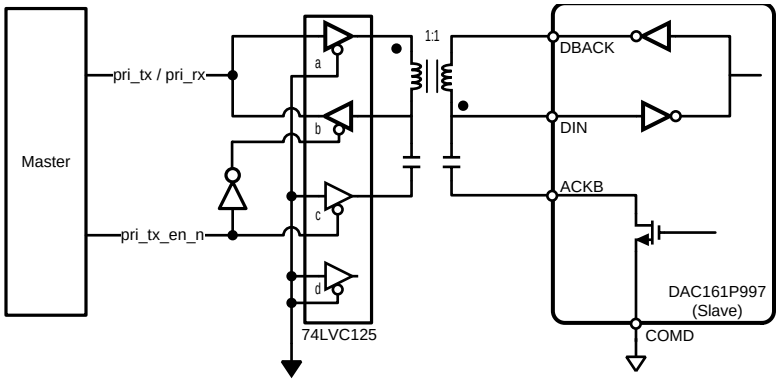


Figure 27. Typical SWIF Implementation

The interface implementation shown in Figure 27 can be expanded or simplified depending on the requirements of the system and capabilities of the Master controller. A number of other possible implementations are shown in the figures below.

Figure 28 shows the circuit analogous in its functionality to the circuit in Figure 27 but with fewer active components. Here instead of disabling ‘b’ buffer during data transmission, its output impedance is increased to the point where its drive is significant only during the data reception form the Slave.

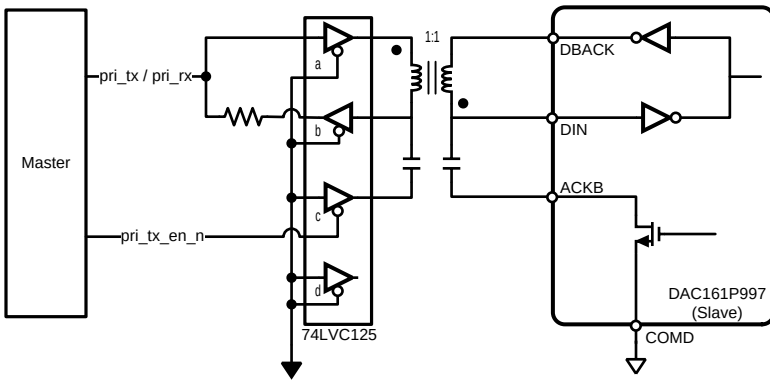


Figure 28. SWIF Link With Simplified Control

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Typical Application (continued)

Figure 29 shows the SWIF link circuit when the Master does not have a bidirectional I/O available. The Master output driving pri_tx is split away from the Master receiving pri_rx input by using a buffer 'd', until now unused, on 74LVC125.

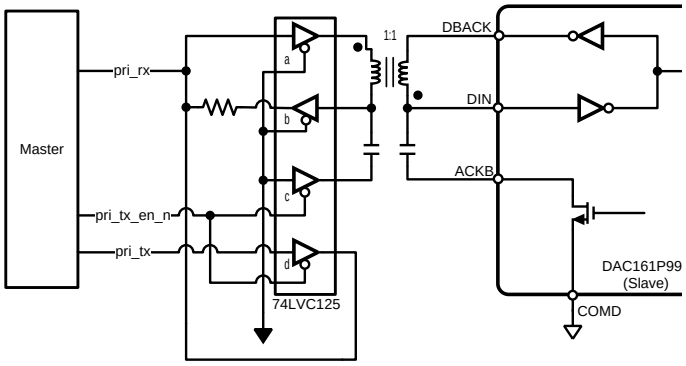


Figure 29. Master Without Bidirectional I/O

Figure 30 shows the trivial circuit realization of the SWIF link in simplex mode, unidirectional data flow.

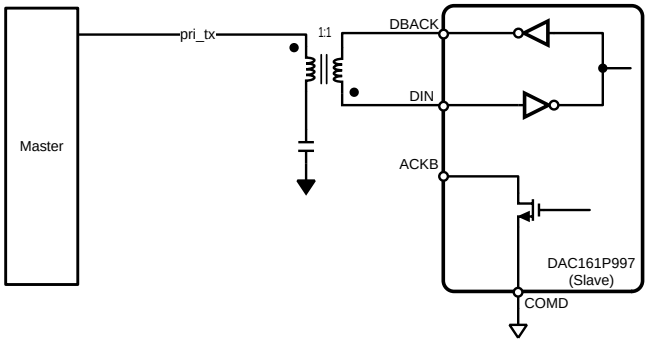


Figure 30. SWIF Without Acknowledge Capability

Figure 31 shows the DC coupled SWIF link realization. In this example ACKB output is used to generate the Acknowledge pulse. This is equivalent to the Acknowledge pulse generated at DBACK, since in transformer coupled application both ACKB and DBACK have to be pulsed to transmit back to the Master. Note that the pulse generated by ACKB is active LOW.

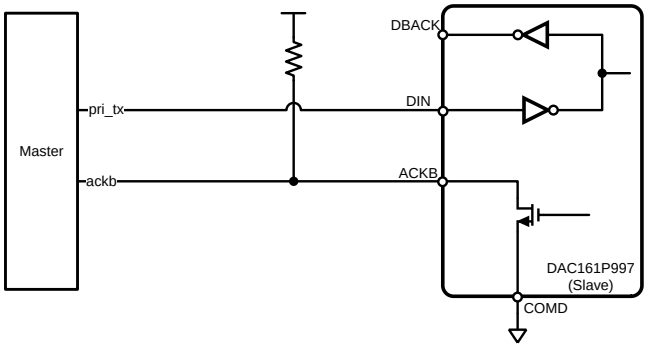


Figure 31. DC-Coupled SWIF Link

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Typical Application (continued)

The SWIF link realization using opto-couplers (opto-isolators) is shown in Figure 32. Points of note here are: the opto-couplers invert the SWIF symbol waveform, and there is increased power consumption due to the relatively large currents required to turn on the internal diodes and standing current in the pull-up resistors.

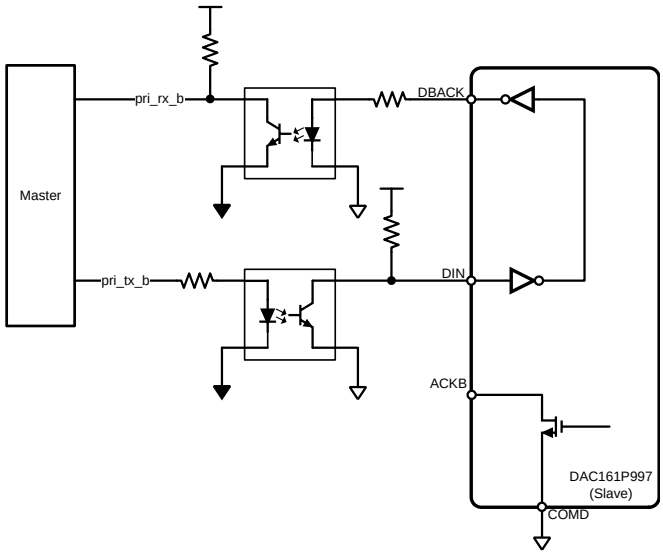


Figure 32. SWIF Link Realized With Octo-Couplers

8.2.3 Application Curve

Unless otherwise noted, these specifications apply for VA = VD = 3.3 V, COMA = COMD = 0 V, T_A= 25°C, external bipolar transistor: 2N3904, RE = 22 Ω, C1 = C2 = C3 = 2.2 nF.

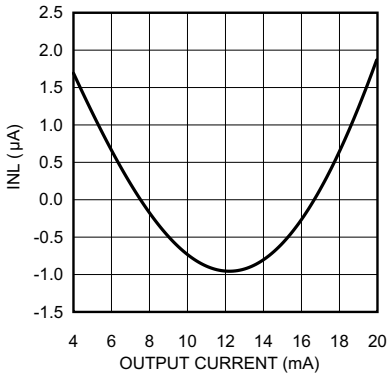


Figure 33. Linearity vs ILOOP

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9 Power Supply Recommendations

The DAC161P997 requires a voltage supply within 2.7 V and 3.6 V. Multilayer ceramic bypass X7R capacitors of 0.1µF between the VA and GND pins, and between the VD and GND pins are recommended. If the supply is located more than a few inches from the DAC161P997, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 10 µF or 22 µF is a typical choice

10 Layout

10.1 Layout Guidelines

To maximize the performance of the DAC161S997 in any application, good layout practices and proper circuit design must be followed. A few recommendations specific to the DAC161S997 are:

- Make sure that VD and VA have decoupling capacitors local to the respective terminals.
- Minimize trace length between the C1, C2, and C3 capacitors and the DAC161S997 pins.

10.2 Layout Example

Figure 34 and Figure 35 show the DAC161S997 evaluation module (EVM) layout

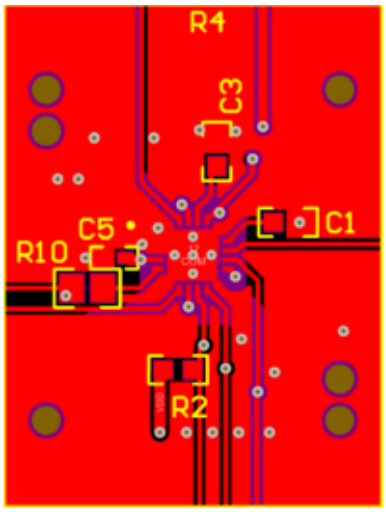


Figure 34. Example PCB layout: Top Layer

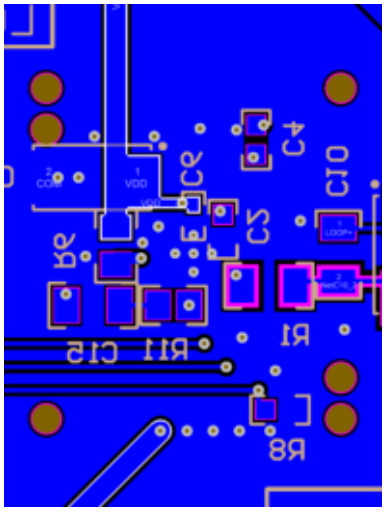


Figure 35. Example PCB layout: Bottom Layer

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11 Device and Documentation Support

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11.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DAC161P997CISQ/NO.A	Active	Production	WQFN (RGH) | 16	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 105	161P997
DAC161P997CISQ/NO.B	Active	Production	WQFN (RGH) | 16	1000 | SMALL T&R	-	Call TI	Call TI	-40 to 105	
DAC161P997CISQ/NOPB	Active	Production	WQFN (RGH) | 16	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 105	161P997
DAC161P997CISQX/NO.A	Active	Production	WQFN (RGH) | 16	4500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 105	161P997
DAC161P997CISQX/NO.B	Active	Production	WQFN (RGH) | 16	4500 | LARGE T&R	-	Call TI	Call TI	-40 to 105	
DAC161P997CISQX/NOPB	Active	Production	WQFN (RGH) | 16	4500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 105	161P997

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

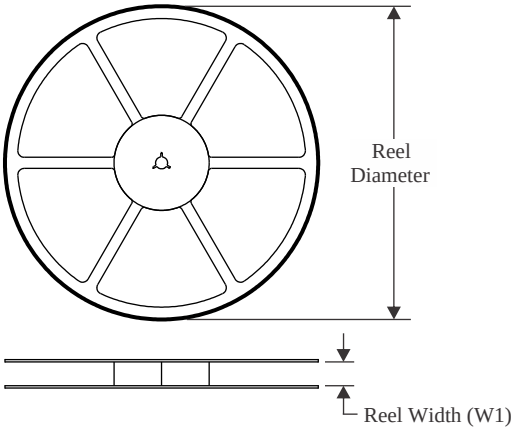
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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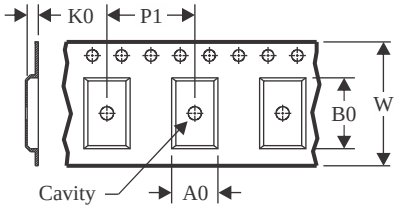
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

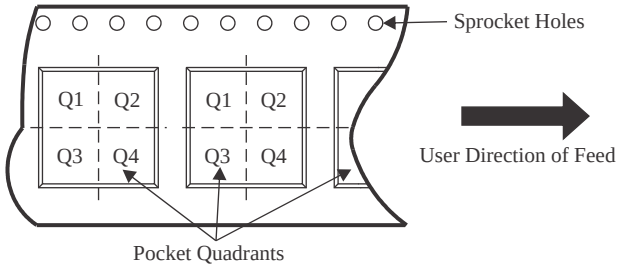


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

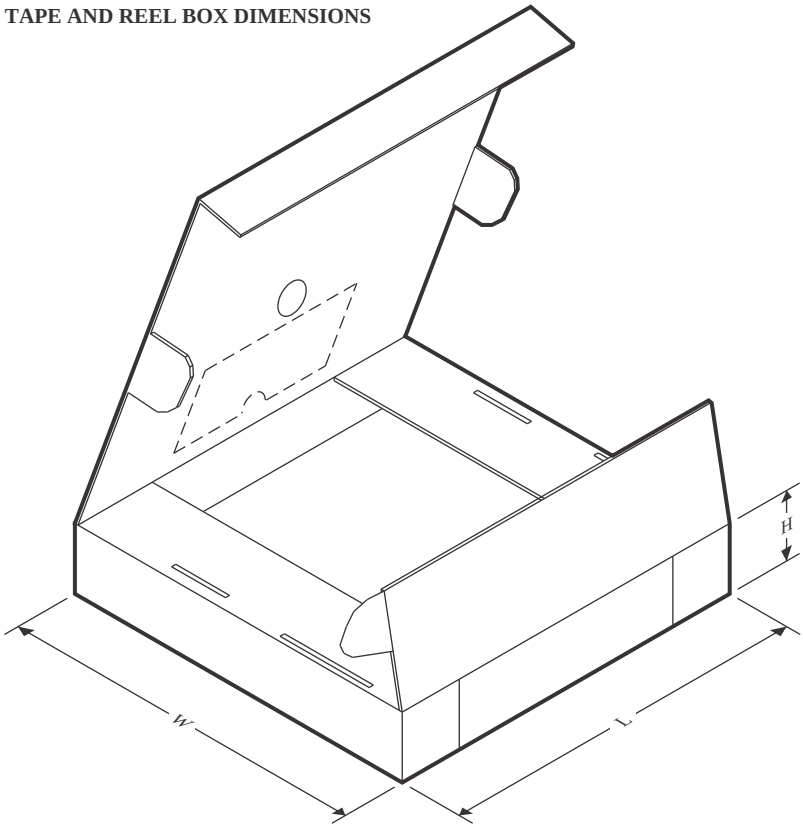
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC161P997CISQ/NOPB	WQFN	RGH	16	1000	177.8	12.4	4.3	4.3	1.3	8.0	12.0	Q1
DAC161P997CISQX/NOPB	WQFN	RGH	16	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

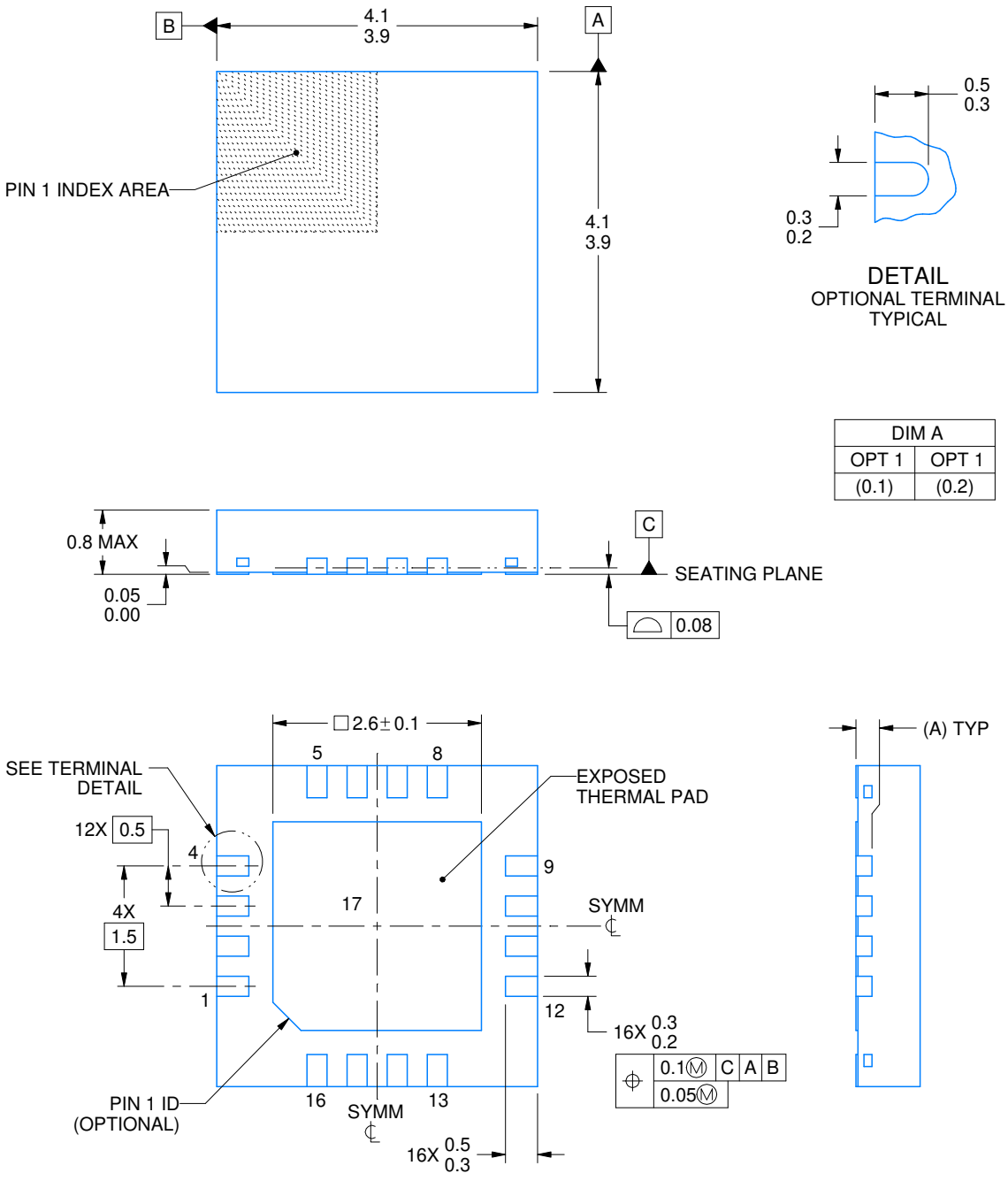
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC161P997CISQ/NOPB	WQFN	RGH	16	1000	367.0	367.0	35.0
DAC161P997CISQX/ NOPB	WQFN	RGH	16	4500	367.0	367.0	35.0

PACKAGE OUTLINE

RGH0016A

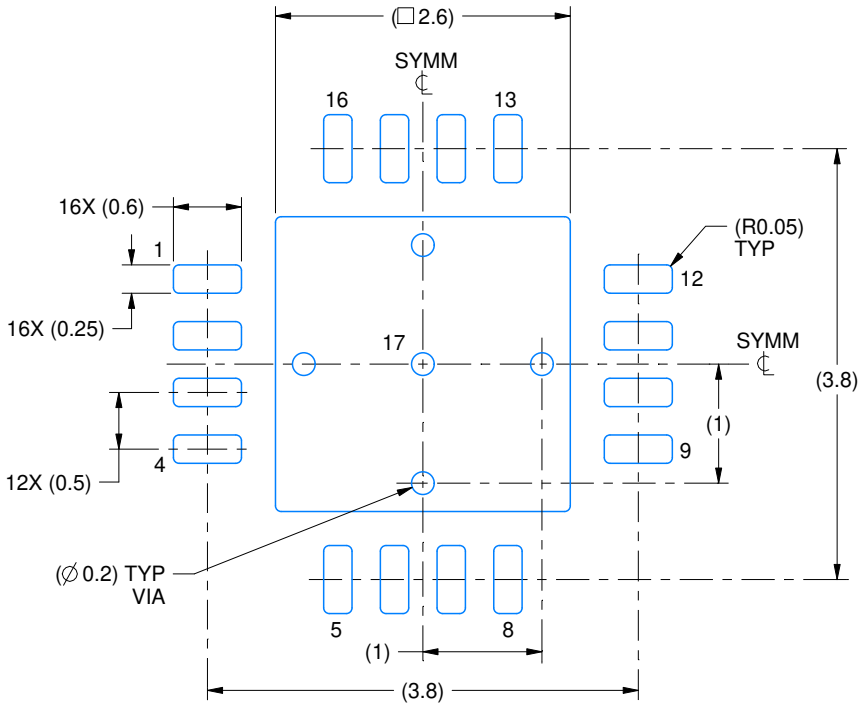
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

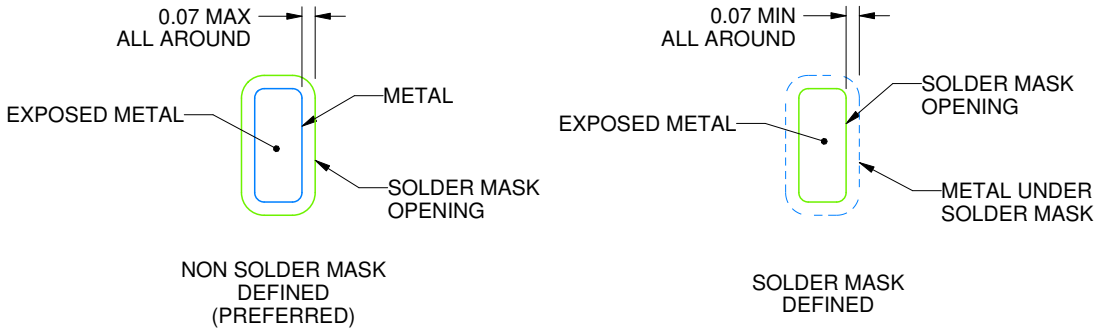


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

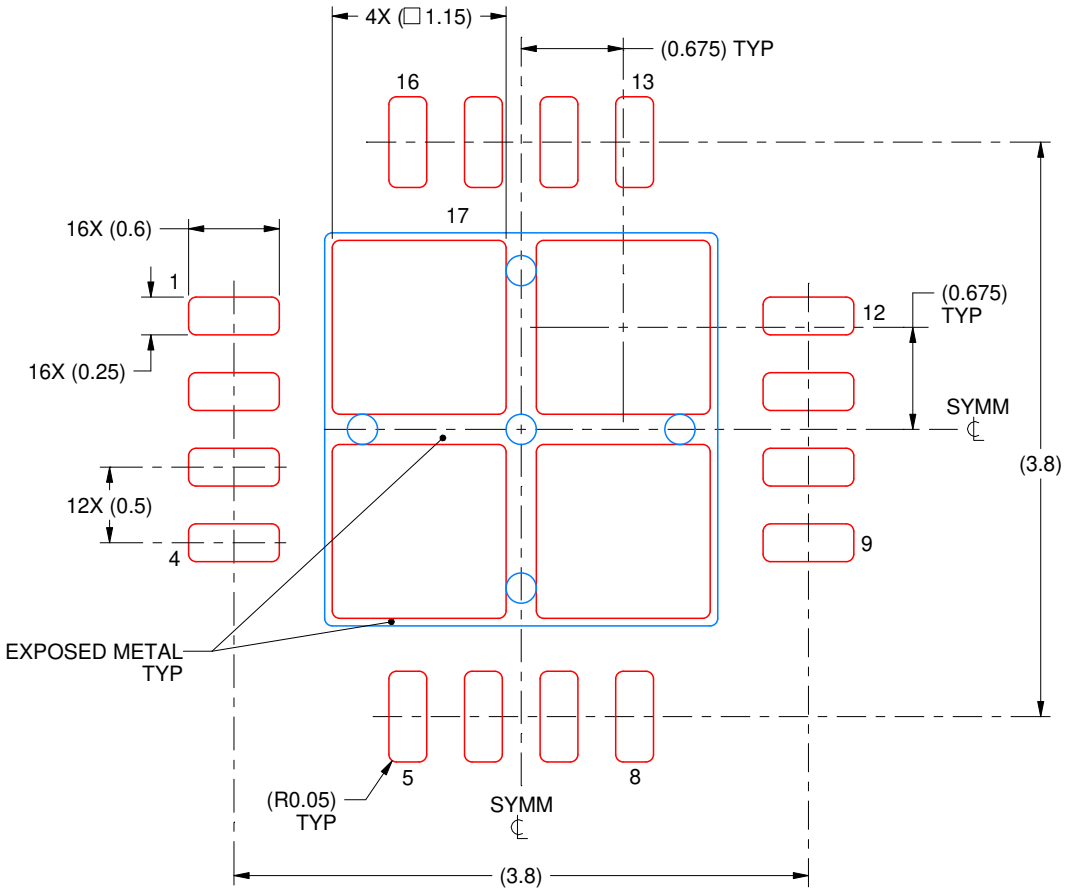


SOLDER MASK DETAILS

4214978/B 01/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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