DAC31x1 Single-Channel, 14-,12-, and 10-Bit, 500-MSPS, Digital-to-Analog Converters

1 Features

- Single Channel
- Resolution
  - DAC3151: 10-Bit
  - DAC3161: 12-Bit
  - DAC3171: 14-Bit
- Maximum Sample Rate: 500 MSPS
- Pin-Compatible Family
- Input Interface:
  - Parallel LVDS Inputs
  - Single or Dual DDR Data Clock
  - Internal FIFO
- Chip to Chip Synchronization
- Power Dissipation: 375 mW
- Spectral Performance at 20 MHz IF
  - SNR:
    - DAC3151: 62 dBFS
    - DAC3161: 72 dBFS
    - DAC3171: 76 dBFS
  - SFDR:
    - DAC3151: 76 dBc
    - DAC3161: 77 dBc
    - DAC3171: 78 dBc
- Current Sourcing DACs
- Compliance Range: –0.5 V to +1 V
- Package: 64-pin VQFN (9 mm × 9 mm)

2 Applications

- Wireless Infrastructure
  - PA Bias, Envelope Tracking, TX
- Radar
- Software-Defined Radios
- Signal and Waveform Generators
- Cable Head-End Equipment

3 Description

The DAC3151, DAC3161, and DAC3171 (DAC31x1) are a family of single-channel, 500-MSPS digital-to-analog converters (DACs). This family uses a 10-, 12-, or 14-bit wide LVDS digital bus with an input FIFO. The 14-bit DAC3171 also supports a DDR 7-bit LVDS interface mode. FIFO input and output pointers can be synchronized across multiple devices for precise signal synchronization. The DAC outputs are current sourcing, and terminate to GND with a compliance range of –0.5 V to +1 V. The DAC31x1 are pin compatible with the DAC31x4, dual-channel, 10-, 12-, and 14-bit, 500-MSPS digital-to-analog converters.

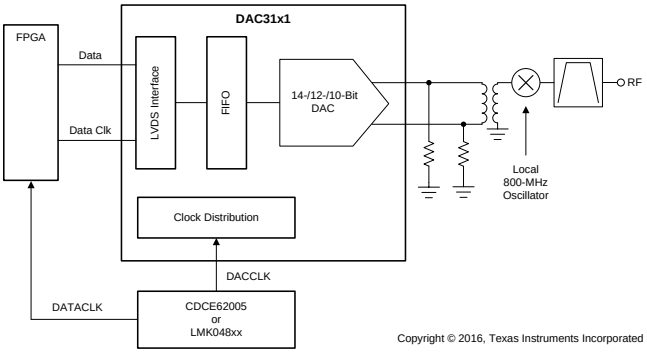
The DAC31x1 are available in a VQFN-64 package that is specified over the full industrial temperature range (–40°C to +85°C).

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DAC3151	VQFN (64)	9.00 mm × 9.00 mm
DAC3161		
DAC3171		

(1) For all available packages, see the package option addendum at the end of the data sheet.

DAC31x1 System Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (September 2016) to Revision D — **Page**

- Changed description for pins 1,2 from "and CLKVDD2" to "/ 2" in *Pin Functions: DAC3151* table ... 5
- Changed description for pins 1,2 from "and CLKVDD2" to "/ 2" in *Pin Functions: DAC3161* table ... 7
- Changed description for pins 1,2 from "and CLKVDD2" to "/ 2" in *Pin Functions: DAC3171 7-Bit Interface Mode* ... 9
- Changed description for pins 1,2 from "and CLKVDD2" to "/ 2" in *Pin Functions: DAC3171 14-Bit Interface Mode* ... 11
- Deleted all instances of sampling rates > 500 MSPS from Table 34 ... 52
- Changed VDDDA33 to VDDA33 (typo) in Table 34 ... 52
- Changed VDDA33 value from 0.9 V to 3.3 V in Table 34 ... 52

Changes from Revision B (January 2016) to Revision C — **Page**

- Added last sentence to RESETB pin description in *Pin Functions: DAC3151* table ... 4
- Added last sentence to RESETB pin description in *Pin Functions: DAC3161* table ... 6
- Added last sentence to RESETB pin description in *Pin Functions: DAC3171 7-Bit Interface Mode* table ... 8
- Added last sentence to RESETB pin description is *Pin Functions: DAC3171 14-Bit Interface Mode* table ... 10
- Changed *LVDS* to *LVPECL* in ALIGNP, ALIGNN amplifier in Figure 66 ... 30
- Changed *LVDS* to *LVPECL* in ALIGNP, ALIGNN amplifier in Figure 67 ... 31
- Changed *LVDS* to *LVPECL* in ALIGNP, ALIGNN amplifier in Figure 68 ... 32
- Added *Programming* section ... 38

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Changes from Revision A (August 2013) to Revision B **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. 1
- Added Simplified Schematic 1
- Changed the register default values and added missing electrical characteristics for LVPECL signal 15
- Changed Figure 66 30
- Changed Figure 67 31
- Changed Figure 68 32
- Changed Figure 69 33

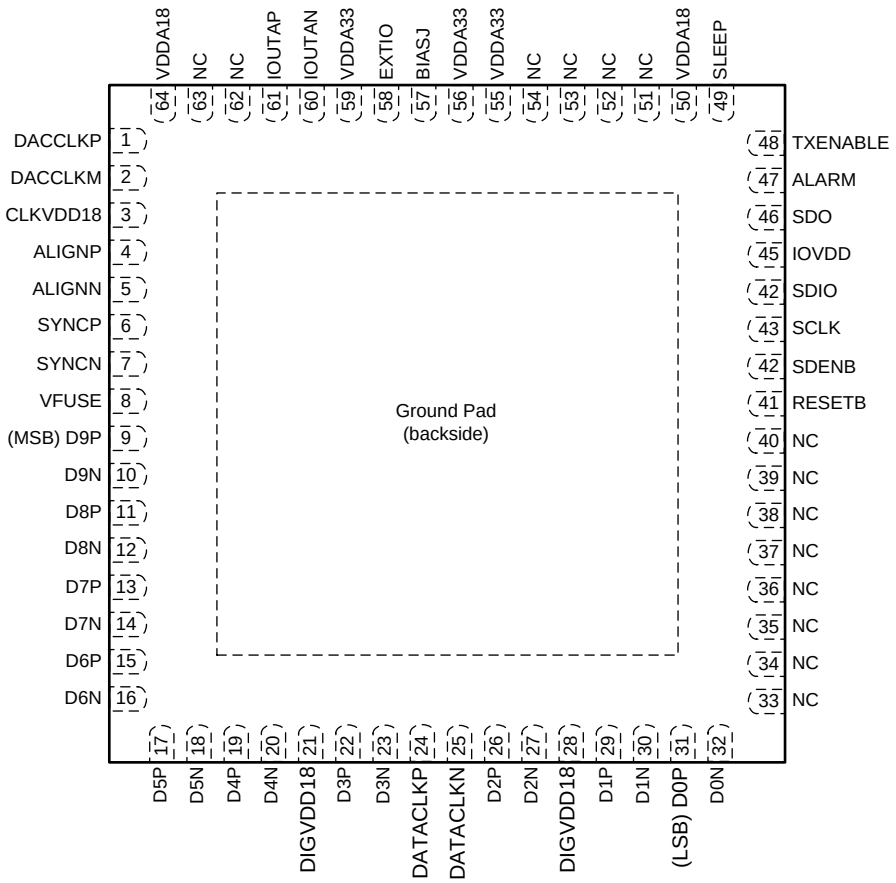
Changes from Original (August 2013) to Revision A **Page**

- Changed from Product Preview to Production Data 1

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5 Pin Configuration and Functions

RGC Package
64-Pin VQFN
Top View



Pin Functions: DAC3151

PIN		I/O	DESCRIPTION
NAME	NO.		
CONTROL OR SERIAL			
SCLK	43	I	Serial interface clock. Internal pulldown.
SDENB	42	I	Serial data enable. Internal pullup.
SDIO	44	I/O	Bi-directional serial data in 3 pin mode (default). In 4-pin interface mode (register sif4_ena (config 0, bit 9)), the SDIO pin in an input only. Internal pulldown.
SDO	46	O	Uni-directional serial interface data in 4 pin mode (register sif4_ena (config 0, bit 9)). The SDO pin is tri-stated in 3-pin interface mode (default). Internal pulldown.
RESETB	41	I	Serial interface reset input. Active low. Initialized internal registers during high to low transition. Asynchronous. Internal pullup. A reset event after every power cycle may be needed to reinitialize all SPI registers to their default values.
ALARM	47	O	CMOS output for ALARM condition.
TXENABLE	48	I	Transmit enable active high input. TXENABLE must be high for the DATA to the DAC to be enabled. When TXENABLE is low, the digital logic section is forced to all 0, and any input data is ignored. Internal pulldown.
SLEEP	49	I	Puts device in sleep, active high. Internal pulldown.

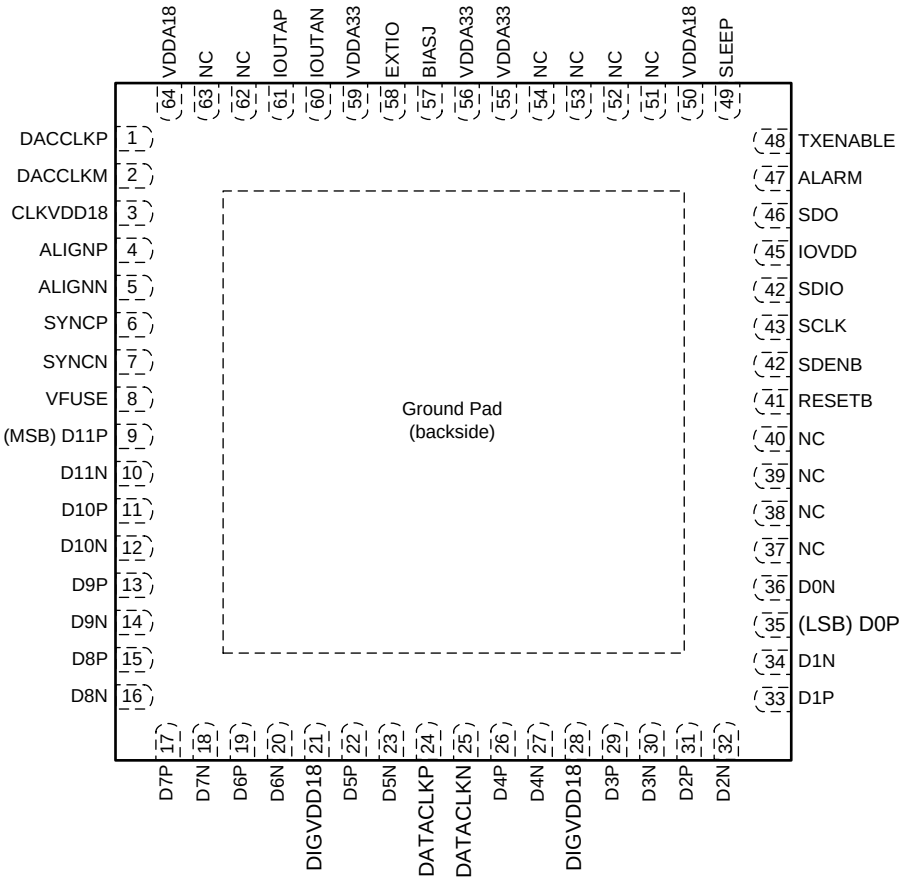
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Pin Functions: DAC3151 (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
DATA INTERFACE			
DATA[9:0]P, DATA[9:0]N	9, 10, 19, 20, 22, 23, 26, 27, 29, 30, 31, 32	I	LVDS input data bits for both channels. Each positive or negative LVDS pair has an internal 100-Ω termination resistor. The data format relative to DATACLKP and DATACLKN clock is Double Data Rate (DDR) with two data transfers per DATACKP and DATACKN clock cycle. The data format is interleaved with channel A (rising edge) and channel B (falling edge). In the default mode (reverse bus not enabled): DATA13P and DATA13N are most significant data bit (MSB) DATA0P and DATA0N are least significant data bit (LSB)
DATACLKP, DATACLKN	24, 25	I	DDR differential input data clock. Edge to center nominal timing. Channel A rising edge, channel B falling edge in multiplexed output mode.
SYNCP, SYNCN	6, 7	I	Reset the FIFO or to be used as a syncing source. These two functions are captured with the rising edge of DATACLKP and DATACLKN. The signal captured by the falling edge of DATACLKP and DATACLKN.
ALIGNP, ALIGNN	4, 5	I	LVPECL FIFO output synchronization. This positive and negative pair is captured with the rising edge of DACCLKP and DACCLKN. It is used to reset the clock dividers and for multiple DAC synchronization. If unused it can be left unconnected.
OUTPUT OR CLOCK			
DACCLKP, DACCLKN	1, 2	I	LVPECL clock input for DAC core with a self-bias of approximately CLKVDD18 / 2.
IOUTAP, IOUTAN	61, 60	O	A-channel DAC current output. An offset binary data pattern of 0x0000 at the DAC input results in a full scale current source and the most positive voltage on the IOUTAP pin. Similarly, a 0xFFFF data input results in a 0 mA current source and the least positive voltage on the IOUTAP pin.
REFERENCE			
EXTIO	58	I/O	Used as external reference input when internal reference is disabled. Requires a 0.1-µF decoupling capacitor to GND when used as reference output.
BIASJ	57	O	Full-scale output current bias. For 20-mA full-scale output current, connect a 960-Ω resistor to GND.
POWER SUPPLY			
IOVDD	45	I	Supply voltage for CMOS IO's. 1.8 V to 3.3 V.
CLKVDD18	3	I	1.8 V clock supply
DIGVDD18	21, 28	I	1.8 V digital supply. Also supplies LVDS receivers.
VDDA18	50, 64	I	Analog 1.8 V supply
VDDA33	55, 56, 59	I	Analog 3.3 V supply
VFUSE	8	I	Digital supply voltage. (1.8 V) This supply pin is also used for factory fuse programming. Connect to DVDD pins for normal operation.
NC	33, 34, 39, 40, 51, 52, 53, 54, 62, 63	–	Not used. These pins can be left open or tied to GROUND in actual application use. It is recommended to turn off pin 33-40 (register lvdsdata_ena) to save power.

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RGC Package
64-Pin VQFN
Top View



Pin Functions: DAC3161

PIN		I/O	DESCRIPTION
NAME	NO.		
CONTROL OR SERIAL			
SCLK	43	I	Serial interface clock. Internal pulldown.
SDENB	42	I	Serial data enable. Internal pullup.
SDIO	44	I/O	Bi-directional serial data in 3 pin mode (default). In 4-pin interface mode (register sif4_ena (config 0, bit 9)), the SDIO pin in an input only. Internal pulldown.
SDO	46	O	Uni-directional serial interface data in 4 pin mode (register sif4_ena (config 0, bit 9)). The SDO pin is tri-stated in 3-pin interface mode (default). Internal pulldown.
RESETB	41	I	Serial interface reset input. Active low. Initialized internal registers during high to low transition. Asynchronous. Internal pullup. A reset event after every power cycle may be needed to reinitialize all SPI registers to their default values.
ALARM	47	O	CMOS output for ALARM condition.
TXENABLE	48	I	Transmit enable active high input. TXENABLE must be high for the DATA to the DAC to be enabled. When TXENABLE is low, the digital logic section is forced to all 0, and any input data is ignored. Internal pulldown.
SLEEP	49	I	Puts device in sleep, active high. Internal pulldown.

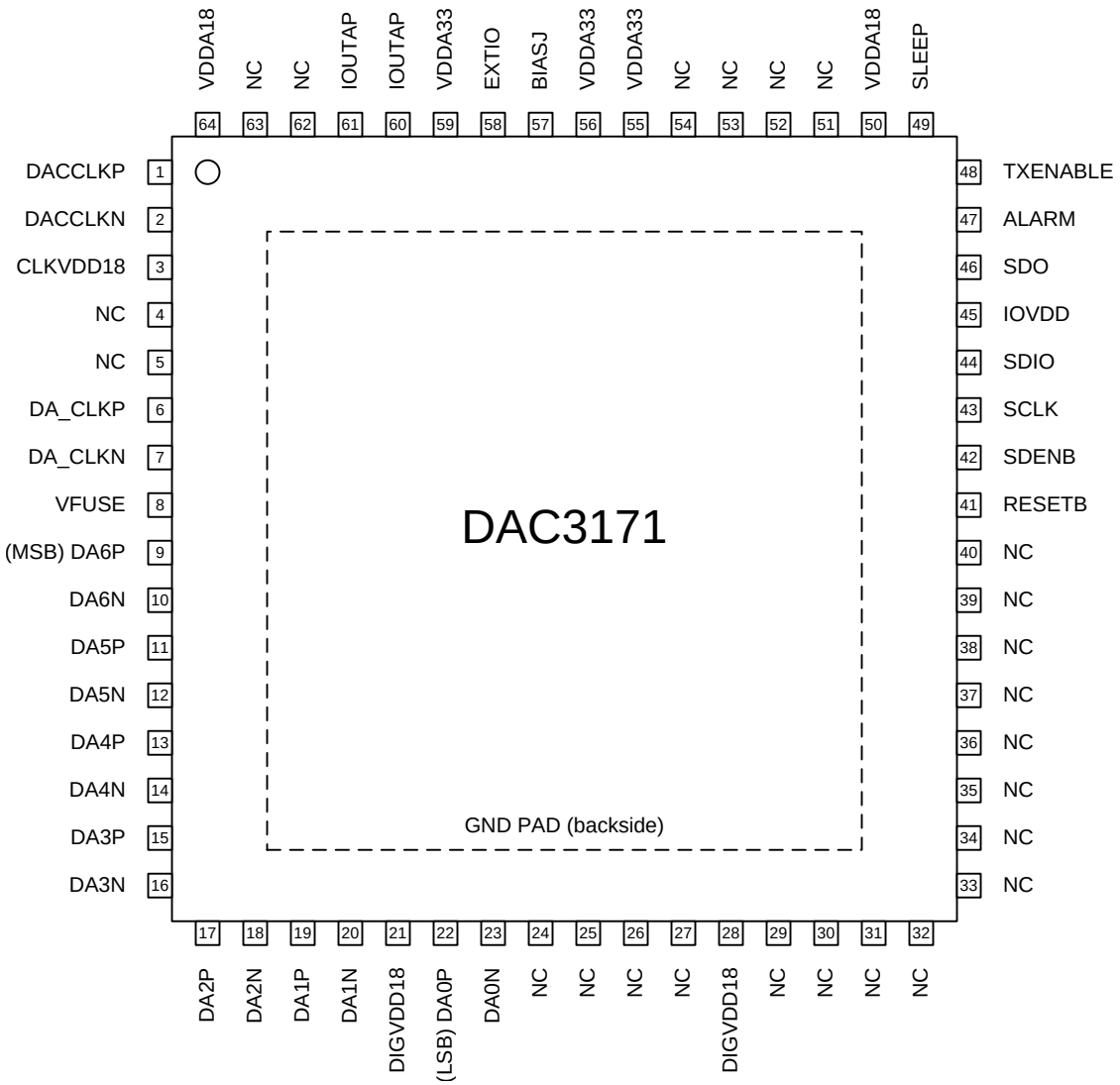
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Pin Functions: DAC3161 (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
DATA INTERFACE			
DATA[11:0]P, DATA[11:0]N	9, 10, 19, 20, 22, 23, 26, 27, 29, 30, 35, 36	I	LVDS input data bits for both channels. Each positive or negative LVDS pair has an internal 100-Ω termination resistor. The data format relative to DATACLKP and DATACLKN clock is Double Data Rate (DDR) with two data transfers per DATACKP and DATACKN clock cycle. The data format is interleaved with channel A (rising edge) and channel B (falling edge). In the default mode (reverse bus not enabled): DATA13P and DATA13N are most significant data bit (MSB) DATA0P and DATA0N are least significant data bit (LSB)
DATACLKP, DATACLKN	24, 25	I	DDR differential input data clock. Edge to center nominal timing. Channel A rising edge, channel B falling edge in multiplexed output mode.
SYNCP, SYNCN	6, 7	I	Reset the FIFO or to be used as a syncing source. These two functions are captured with the rising edge of DATACLKP and DATACLKN. The signal captured by the falling edge of DATACLKP and DATACLKN.
ALIGNP, ALIGNN	4, 5	I	LVPECL FIFO output synchronization. This positive or negative pair is captured with the rising edge of DACCLKP and DACCLKN. It is used to reset the clock dividers and for multiple DAC synchronization. If unused it can be left unconnected.
OUTPUT OR CLOCK			
DACCLKP, DACCLKN	1, 2	I	LVPECL clock input for DAC core with a self-bias of approximately CLKVDD18 / 2.
IOUTAP, IOUTAN	61, 60	O	A-channel DAC current output. An offset binary data pattern of 0x0000 at the DAC input results in a full scale current source and the most positive voltage on the IOUTAP pin. Similarly, a 0xFFFF data input results in a 0 mA current source and the least positive voltage on the IOUTAP pin.
REFERENCE			
EXTIO	58	I/O	Used as external reference input when internal reference is disabled. Requires a 0.1-µF decoupling capacitor to GND when used as reference output.
BIASJ	57	O	Full-scale output current bias. For 20-mA full-scale output current, connect a 960-Ω resistor to GND.
POWER SUPPLY			
IOVDD	45	I	Supply voltage for CMOS IO's. 1.8 V to 3.3 V.
CLKVDD18	3	I	1.8 V clock supply
DIGVDD18	21, 28	I	1.8 V digital supply. Also supplies LVDS receivers.
VDDA18	50, 64	I	Analog 1.8 V supply
VDDA33	55, 56, 59	I	Analog 3.3 V supply
VFUSE	8	I	Digital supply voltage. (1.8 V) This supply pin is also used for factory fuse programming. Connect to DVDD pins for normal operation.
NC	37, 38, 39, 40, 51, 52, 53, 54, 62, 63	–	Not used. These pins can be left open or tied to GROUND in actual application use. It is recommended to turn off pin 37-40 (register lvdsdata_ena) to save power.

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RGC Package
64-Pin VQFN
Top View



Pin Functions: DAC3171 7-Bit Interface Mode

PIN		I/O	DESCRIPTION
NAME	NO.		
CONTROL OR SERIAL			
SCLK	43	I	Serial interface clock. Internal pulldown.
SDENB	42	I	Serial data enable. Internal pullup.
SDIO	44	I/O	Bi-directional serial data in 3 pin mode (default). In 4-pin interface mode (register XYZ), the SDIO pin in an input only. Internal pulldown.
SDO	46	O	Uni-directional serial interface data in 4 pin mode (register XYZ). The SDO pin is tri-stated in 3-pin interface mode (default). Internal pulldown.
RESETB	41	I	Serial interface reset input. Active low. Initialized internal registers during high to low transition. Asynchronous. Internal pullup. A reset event after every power cycle may be needed to reinitialize all SPI registers to their default values.
ALARM	47	O	CMOS output for ALARM condition.

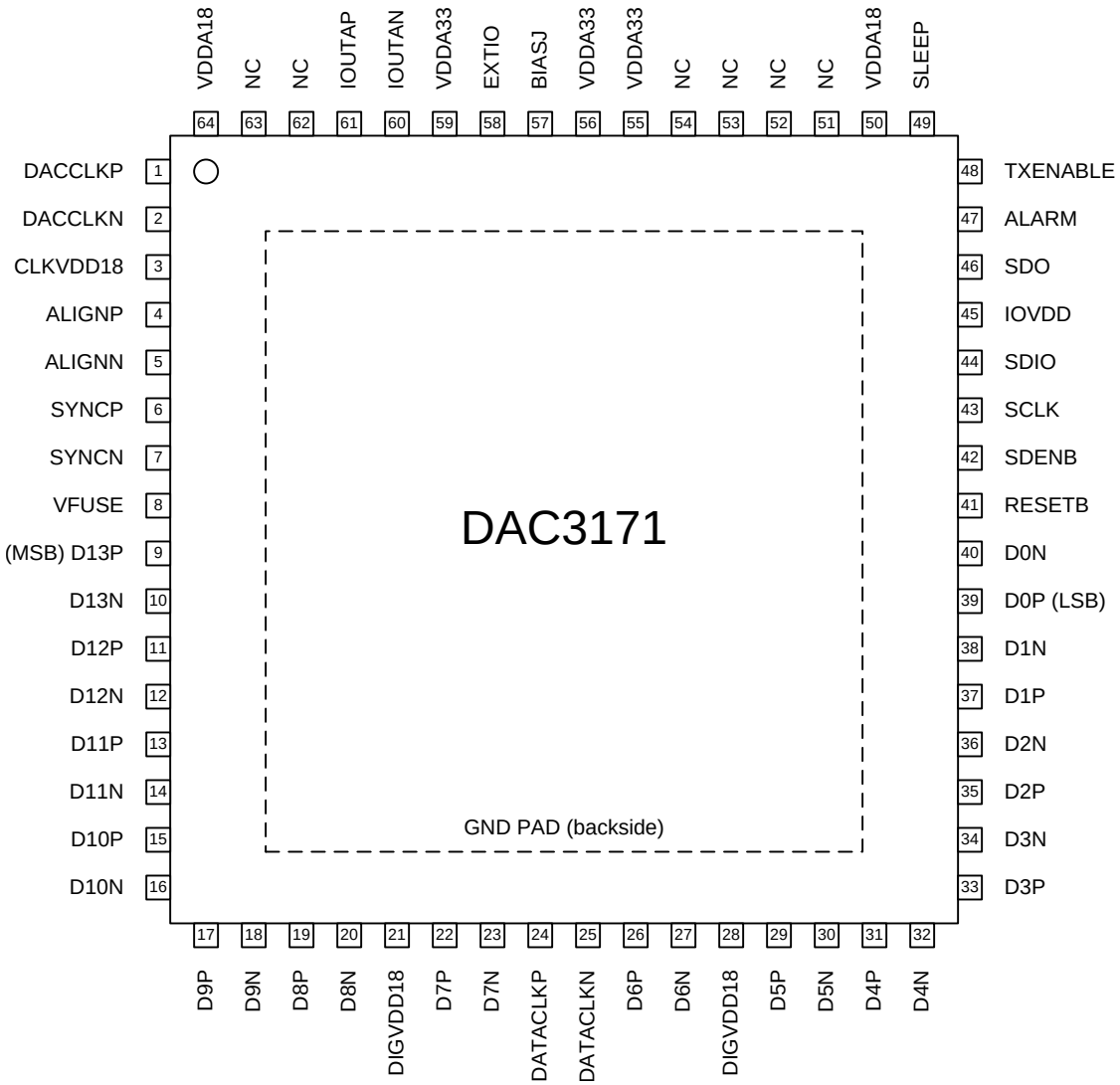
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Pin Functions: DAC3171 7-Bit Interface Mode (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
TXENABLE	48	I	Transmit enable active high input. TXENABLE must be high for the DATA to the DAC to be enabled. When TXENABLE is low, the digital logic section is forced to all 0, and any input data is ignored. Internal pulldown.
SLEEP	49	I	Puts device in sleep, active high. Internal pulldown.
DATA INTERFACE			
DA[6:0]P, DA[6:0]N	9, 10, 19, 20, 22, 23	I	LVDS positive input data bits for channel A. Each positive or negative LVDS pair has an internal 100-Ω termination resistor. The data format relative to DA_CLKP and DA_CLKN clock is Double Data Rate (DDR) with two data transfers per DA_CLKP and DA_CLKN clock cycle. The data format is 7 MSBs (rising edge) or 7 LSBs (falling edge). In the default mode (reverse bus not enabled): D6P and D6N are most significant data bit (MSB) D0P and D0N are least significant data bit (LSB)
DA_CLKP, DA_CLKN	6, 7	I	DDR differential input data clock for channel A. Edge to center nominal timing. Assumes SPI register field dual_ena (bit0 of Config3) is set. Otherwise, DA_CLKP and DA_CLKN will be on pins 24 or 25 as in DAC3171 14-bit Interface Mode.
OUTPUT OR CLOCK			
DACCLKP, DACCLKN	1, 2	I	LVPECL clock input for DAC core with a self-bias of approximately CLKVDD18 / 2.
IOUTAP, IOUTAN	61, 60	O	A-channel DAC current output. An offset binary data pattern of 0x0000 at the DAC input results in a full scale current source and the most positive voltage on the IOUTA1 pin. Similarly, a 0xFFFF data input results in a 0 mA current source and the least positive voltage on the IOUTA1 pin. The IOUTA2 pin is the complement of IOUTA1.
REFERENCE			
EXTIO	58	I/O	Used as external reference input when internal reference is disabled. Requires a 0.1-µF decoupling capacitor to GND when used as reference output.
BIASJ	57	O	Full-scale output current bias. For 20-mA full-scale output current, connect a 960-Ω resistor to GND.
POWER SUPPLY			
IOVDD	45	I	Supply voltage for CMOS IO's. 1.8 V to 3.3 V.
CLKVDD18	3	I	1.8 V clock supply
DIGVDD18	21, 28	I	1.8 V digital supply. Also supplies LVDS receivers.
VDDA18	50, 64	I	Analog 1.8 V supply
VDDA33	55, 56, 59	I	Analog 3.3 V supply
VFUSE	8	I	Digital supply voltage. (1.8 V) This supply pin is also used for factory fuse programming. Connect to DVDD pins for normal operation.
NC	4, 5, 24, 25, 26, 27, 29, 30-39, 40, 51, 52, 53, 62, 63	–	Not used. Pin 4 can be left open or tied to DIGVDD18, and other pins can be left open or tied to GROUND in actual application use. It is recommended to turn off pin 24, 25, 26, 27, 29, 30-39, and 40 (register lvdsdataclk_ena, lvdsdata_ena) to save power.

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RGC Package
64-Pin VQFN
Top View



Pin Functions: DAC3171 14-Bit Interface Mode

PIN		I/O	DESCRIPTION
NAME	NO.		
CONTROL OR SERIAL			
SCLK	43	I	Serial interface clock. Internal pulldown.
SDENB	42	I	Serial data enable. Internal pullup.
SDIO	44	I/O	Bi-directional serial data in 3 pin mode (default). In 4-pin interface mode (register sif4_ena (config 0, bit 9)), the SDIO pin in an input only. Internal pulldown.
SDO	46	O	Uni-directional serial interface data in 4 pin mode (register sif4_ena (config 0, bit 9)). The SDO pin is tri-stated in 3-pin interface mode (default). Internal pulldown.
RESETB	41	I	Serial interface reset input. Active low. Initialized internal registers during high to low transition. Asynchronous. Internal pullup. A reset event after every power cycle may be needed to reinitialize all SPI registers to their default values.
ALARM	47	O	CMOS output for ALARM condition.

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Pin Functions: DAC3171 14-Bit Interface Mode (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
TXENABLE	48	I	Transmit enable active high input. TXENABLE must be high for the DATA to the DAC to be enabled. When TXENABLE is low, the digital logic section is forced to all 0, and any input data is ignored. Internal pulldown.
SLEEP	49	I	Puts device in sleep, active high. Internal pulldown.
DATA INTERFACE			
DATA[13:0]P, DATA[13:0]N	9, 10-19, 20, 22, 23, 26, 27, 29, 30-39, 40	I	LVDS input data bits for both channels. Each positive or negative LVDS pair has an internal 100-Ω termination resistor. The data format relative to DATACLKP and DATACLKN clock is Double Data Rate (DDR) with two data transfers per DATACKP and DATACKN clock cycle. The data format is interleaved with channel A (rising edge) and channel B (falling edge). In the default mode (reverse bus not enabled): DATA13P and DATA13N are most significant data bit (MSB) DATA0P and DATA0N are least significant data bit (LSB)
DATACLKP, DATACLKN	24, 25	I	DDR differential input data clock. Edge to center nominal timing. Channel A rising edge, channel B falling edge in multiplexed output mode.
SYNCP, SYNCN	6, 7	I	Reset the FIFO or to be used as a syncing source. These two functions are captured with the rising edge of DATACLKP and DATACLKN. The signal captured by the falling edge of DATACLKP and DATACLKN.
ALIGNP, ALIGNN	4, 5	I	LVPECL FIFO output synchronization. This positive or negative pair is captured with the rising edge of DACCLKP and DACCLKN. It is used to reset the clock dividers and for multiple DAC synchronization. If unused it can be left unconnected.
OUTPUT OR CLOCK			
DACCLKP, DACCLKN	1, 2	I	LVPECL clock input for DAC core with a self-bias of approximately CLKVDD18 / 2.
IOUTAP, IOUTAN	61, 60	O	A-channel DAC current output. An offset binary data pattern of 0x0000 at the DAC input results in a full scale current source and the most positive voltage on the IOUTAP pin. Similarly, a 0xFFFF data input results in a 0 mA current source and the least positive voltage on the IOUTAP pin.
REFERENCE			
EXTIO	58	I/O	Used as external reference input when internal reference is disabled. Requires a 0.1-µF decoupling capacitor to GND when used as reference output.
BIASJ	57	O	Full-scale output current bias. For 20-mA full-scale output current, connect a 960-Ω resistor to GND.
POWER SUPPLY			
IOVDD	45	I	Supply voltage for CMOS IO's, 1.8 V to 3.3 V.
CLKVDD18	3	I	1.8 V clock supply
DIGVDD18	21, 28	I	1.8 V digital supply. Also supplies LVDS receivers.
VDDA18	50, 64	I	Analog 1.8 V supply
VDDA33	55, 56, 59	I	Analog 3.3 V supply
VFUSE	8	I	Digital supply voltage. (1.8 V) This supply pin is also used for factory fuse programming. Connect to DVDD pins for normal operation.
NC	51–54, 62, 63	–	Not used. These pins can be left open or tied to GROUND in actual application use.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	VDDA33 to GND	–0.5	4	V
	VDDA18 to GND	–0.5	2.3	V
	CLKVDD18 to GND	–0.5	2.3	V
	IOVDD to GND	–0.5	4	V
	DIGVDD18 to GND	–0.5	2.3	V
Pin voltage	CLKVDD18 to DIGVDD18	–0.5	0.5	V
	VDDA18 to DIGVDD18	–0.5	0.5	V
	DA[6:0]P, DA[6:0]N, D[13:0]P, D[13:0]N, DATACLKP, DATACLKN, DA_CLKP, DA_CLKPN, SYNCP, SYNCN to GND	–0.5	DIGVDD18 + 0.5	V
	DACCLKP, DACCLKN, ALIGNP, ALIGNN	–0.5	CLKVDD18 + 0.5	V
	TXENABLE, ALARM, SDO, SDIO, SCLK, SDENB, RESETB to GND	–0.5	IOVDD + 0.5	V
	IOUTAP, IOUTAN to GND	–0.7	1.4	V
	EXTIO, BIASJ to GND	–0.5	VDDA33 + 0.5	V
Temperature	Operating junction, T_J		125	°C
	Operating free-air temperature, T_A	–40	85	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
DIGVDD18	Digital power supply, 1.8 V	1.71	1.8	1.89	V
VFUSE	Digital power supply, fuse	1.71	1.8	1.89	V
VDDA18	Analog power supply, 1.8 V	1.71	1.8	1.89	V
CLKVDD18	Clock power supply, 1.8 V	1.71	1.8	1.89	V
VDDA33	Analog power supply, 3.3 V	3.15	3.3	3.45	V
IOVDD(1)	Input/output (IO) power supply	1.71		3.45	V
T_J	Operating junction temperature(2)			105	°C
T_A	Operating free-air temperature	–40	25	85	°C

(1) Sets CMOS IO voltage levels. Nominal 1.8 V, 2.5 V or 3.3 V.
(2) Prolonged use above this junction temperature may increase the device failure-in-time (FIT) rate.

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6.4 Thermal Information

THERMAL METRIC[1]		DAC31x1 RGC (VQFN) 64 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	23.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	7.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	2.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	2.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics: DC Specifications

full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, DAC sample rate = 500 MSPS, 50% clock duty cycle, VDDA33 and IOVDD = 3.3 V, VDDA18, CLKVDD18, and DIGVDD18 = 1.8 V, $IOUT_{FS}$ = 20 mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS	DAC3151			DAC3161			DAC3171			UNIT
			MIN	TYP[1]	MAX	MIN	TYP[1]	MAX	MIN	TYP[1]	MAX	
	Resolution		10			12			14			Bits
DC ACCURACY												
	DNL differential nonlinearity	1 LSB = $IOUT_{FS}$ / 2^{10} for DAC3151, 1 LSB = $IOUT_{FS}$ / 2^{12} for DAC3161, 1 LSB = $IOUT_{FS}$ / 2^{14} for DAC3171		±0.04			±0.2			±1		LSB
	INL integral nonlinearity			±0.15			±0.5			±2		LSB
ANALOG OUTPUTS												
	Coarse gain linearity			±0.4			±0.4			±0.4		LSB
	Offset error	Mid code offset		0.01%			0.01%			0.01%		FSR
	Gain error	With external reference		±2%			±2%			±2%		FSR
		With internal reference		±2%			±2%			±2%		
	Gain mismatch	With internal reference	–2%		2%	–2%		2%	–2%		2%	FSR
	Minimum full scale output current	Nominal full-scale current, $IOUT_{FS}$ = 16 × IBAIS current		2			2			2		mA
	Maximum full scale output current			20			20			20		
	Output compliance range	IOUTFS = 20 mA	–0.5		1	–0.5		1	–0.5		1	V
	Output resistance			300			300			300		kΩ
	Output capacitance				5			5		5		pF
REFERENCE OUTPUT												
V_{REF}	Reference output voltage		1.14	1.2	1.26	1.14	1.2	1.26	1.14	1.2	1.26	V
	Reference output current			100			100			100		nA
REFERENCE INPUT												
	VEXTIO input voltage range	External reference mode	0.1	1.2	1.25	0.1	1.2	1.25	0.1	1.2	1.25	V
	Input resistance			1			1			1		MΩ
	Small signal bandwidth			500			500			500		kHz
	Input capacitance			100			100			100		pF
TEMPERATURE COEFFICIENTS												
	Offset drift			±1			±1			±1		ppm of FSR/°C
	Gain drift	With external reference		±15			±15			±15		ppm/°C
		With internal reference		±30			±30			±30		
	Reference voltage drift			±8			±8			±8		ppm/°C

(1) Typical values at T_A = 25°C.

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Electrical Characteristics: DC Specifications (continued)

full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, DAC sample rate = 500 MSPS, 50% clock duty cycle, VDDA33 and IOVDD = 3.3 V, VDDA18, CLKVDD18, and DIGVDD18 = 1.8 V, $IOUT_{FS}$ = 20 mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS	DAC3151			DAC3161			DAC3171			UNIT
			MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
POWER CONSUMPTION												
I_{VDDA33}	3.3 V analog supply current	MODE 1 f_{DAC} = 491.52 MSPS, QMC on, IF = 20 MHz, input full word width		28			28			28	35	mA
$I_{CLKVDD18}$	1.8 V clock and analog supply current (CLKVDD18 and VDDA18)			47			47			47	56	mA
$I_{DIGVDD18}$	1.8 V digital supply current (DIGVDD18 and VFUSE)			110			110			110	125	mA
I_{IOVDD}	1.8 V IO supply current			0.002			0.002			0.002	0.015	mA
P_{dis}	Total power dissipation			375			375			375	442	mW
I_{VDDA33}	3.3 V analog supply current	MODE 2 f_{DAC} = 320 MSPS, QMC on, IF = 20 MHz, input full word width		28			28			28		mA
$I_{CLKVDD18}$	1.8 V clock and analog supply current (CLKVDD18 and VDDA18)			37			37			37		mA
$I_{DIGVDD18}$	1.8 V digital supply current (DIGVDD18 and VFUSE)			80			80			80		mA
I_{IOVDD}	1.8 V IO supply current			0.002			0.002			0.002		mA
P_{dis}	Total power dissipation			303			303			303		mW
I_{VDDA33}	3.3 V analog supply current	MODE 3 Sleep mode, f_{DAC} = 491.52 MSPS, DAC in sleep mode, input full word width		2.6			2.6			2.6		mA
$I_{CLKVDD18}$	1.8 V clock and analog supply current (CLKVDD18 and VDDA18)			43			43			43		mA
$I_{DIGVDD18}$	1.8 V digital supply current (DIGVDD18 and VFUSE)			106			106			106		mA
I_{IOVDD}	1.8 V IO supply current			0.003			0.003			0.003		mA
P_{dis}	Total power dissipation			277			277			277		mW
I_{VDDA33}	3.3 V analog supply current	MODE 4 Power-down mode, no clock, DAC in sleep mode, input full word width		1.6	4		1.6	4		1.6	4	mA
$I_{CLKVDD18}$	1.8 V clock and analog supply current (CLKVDD18 and VDDA18)			1.8	4		1.8	4		1.8	4	mA
$I_{DIGVDD18}$	1.8 V digital supply current (DIGVDD18 and VFUSE)			0.7	3		0.7	3		0.7	3	mA
I_{IOVDD}	1.8 V IO supply current			0.003	0.015		0.003	0.015		0.003	0.015	mA
P_{dis}	Total power dissipation			10	26		10	26		10	26	mW
PSRR	Power supply rejection ratio	DC tested	–0.4%		0.4%	–0.4%		0.4%	–0.4%		0.4%	FSR/V

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6.6 Electrical Characteristics: AC Specifications

full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, DAC sample rate = 500 MSPS, 50% clock duty cycle, VDDA33 and IOVDD = 3.3 V, VDDA18, CLKVDD18, and DIGVDD18 = 1.8 V, $IOUT_{FS}$ = 20 mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS	DAC3151			DAC3161			DAC3171			UNIT
			MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
ANALOG OUTPUT												
f_{DAC}	Maximum sample rate		500			500			500			MSPS
	Digital latency	Length of delay from DAC pin inputs to DATA at output pins. In normal operation mode including the latency of FIFO.		26			26			26		ns
AC PERFORMANCE												
SFDR	Spurious free dynamic range	f_{DAC} = 500 MSPS, f_{out} = 10.1 MHz		81			82			82		dBc
		f_{DAC} = 500 MSPS, f_{out} = 20.1 MHz		76			77			78		dBc
		f_{DAC} = 500 MSPS, f_{out} = 70.1 MHz		69			70			74		dBc
IMD3	Intermodulation distortion	f_{DAC} = 500 MSPS, f_{out} = 10.1 ± 0.5 MHz		82			83			84		dBc
		f_{DAC} = 500 MSPS, f_{out} = 20.1 ± 0.5 MHz		81			82			84		dBc
		f_{DAC} = 500 MSPS, f_{out} = 70.1 ± 0.5 MHz		73.5			74			75		dBc
		f_{DAC} = 500 MSPS, f_{out} = 150.1 ± 0.5 MHz		61			61			63		dBc
NSD	Noise spectral density	f_{DAC} = 500 MSPS, f_{out} = 10.1 MHz		147			158			160		dBc/Hz
		f_{DAC} = 500 MSPS, f_{out} = 20.1 MHz		146			156			157		dBc/Hz
		f_{DAC} = 500 MSPS, f_{out} = 70.1 MHz		146			153			155		dBc/Hz
ACLR	Adjacent channel leakage ratio	f_{DAC} = 491.52 MSPS, f_{out} = 30.72 MHz, WCDMA TM1		69			77			78		dBc
		f_{AC} = 491.52 MSPS, f_{out} = 153.6 MHz, WCDMA TM1		68			73			74		dBc

(1) Typical values at T_A = 25°C.

6.7 Electrical Characteristics: Digital Specifications

full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, DAC sample rate = 500 MSPS, 50% clock duty cycle, VDDA33 and IOVDD = 3.3 V, VDDA18, CLKVDD18, and DIGVDD18 = 1.8 V, $IOUT_{FS}$ = 20 mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS	DAC3151			DAC3161			DAC3171			UNIT
			MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
CMOS DIGITAL INPUTS (RESETB, SDENB, SCLK, SDIO, TXENABLE)												
V_{IH}	High-level input voltage	IOVDD = 3.3 V, 2.5 V, or 1.8 V	0.6 × IOVDD			0.6 × IOVDD			0.6 × IOVDD			V
V_{IL}	Low-level input voltage	IOVDD = 3.3 V, 2.5 V, or 1.8 V			0.25 × IOVDD			0.25 × IOVDD			0.25 × IOVDD	V
I_{IH}	High-level input current	IOVDD = 3.3 V, 2.5 V, or 1.8 V	-40		40				–40		40	µA
I_{IL}	Low-level input current	IOVDD = 3.3 V, 2.5 V, or 1.8 V	-40		40				–40		40	µA
CMOS DIGITAL OUTPUTS (SDOUT, SDIO)												
V_{OH}	High-level output voltage	IOVDD = 3.3 V, 2.5 V, or 1.8 V	0.85 × IOVDD			0.85 × IOVDD			0.85 × IOVDD			V
V_{OL}	Low-level output voltage	IOVDD = 3.3 V, 2.5 V, or 1.8 V			0.125 × IOVDD			0.125 × IOVDD			0.125 × IOVDD	V
LVPECL DIGITAL INPUTS (DACCLKP, DACCLKN, ALIGNP, ALIGNN)												
V_{com}	Input common mode voltage			0.5			0.5			0.5		V
V_{IDIFF}	Differential input peak-to-peak voltage		0.4	1.0		0.4	1.0		0.4	1.0		V
LVDS INTERFACE (D[x:0]P, D[x:0]N, DA[x:0]P, DA[x:0]N, DA_CLKP, DA_CLKN, DATACLKP, DATACLKN, SYNCP, SYNCN)												
$V_{A,B+}$	Logic high differential input voltage threshold		175			175			175			mV
$V_{A,B-}$	Logic low differential input voltage threshold				–175			–175			–175	mV
V_{COM}	Input Common Mode Range		1.0	1.2	2.0	1.0	1.2	2.0	1.0	1.2	2.0	V
Z_T	Internal termination		85	110	135	85	110	135	85	110	135	Ω
C_L	LVDS input capacitance			2			2			2		pF

(1) Typical values at T_A = 25°C.

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6.8 Timing Requirements

with nominal supplies and $IOUT_{FS}$ = 20 mA (unless otherwise noted)

				MIN	TYP(1)	MAX	UNIT
ANALOG OUTPUT							
$t_{s(DAC)}$	Output settling time to 0.1%	Transition: Code 0x0000 to 0x3FFF			11		ns
t_{PD}	Output propagation delay	Does not include digital latency			2		ns
$t_{r(IOUT)}$	Output rise time 10% to 90%				200		ps
$t_{f(IOUT)}$	Output fall time 90% to 10%				200		ps
SERIAL PORT TIMING							
$t_{s(SENDB)}$	Setup time, SDENB to rising edge of SCLK			20			ns
$t_{s(SDIO)}$	Setup time, SDIO to rising edge of SCLK			10			ns
$t_{h(SDIO)}$	Hold time, SDIO from rising edge of SCLK			5			ns
$t_{(SCLK)}$	Period of SCLK			100			ns
$t_{(SCLKH)}$	High time of SCLK			40			ns
$t_{(SCLKL)}$	Low time of SCLK			40			ns
$t_{d(DATA)}$	Data output delay after falling edge of SCLK				10		ns
T_{RESET}	Minimum RESTB pulse width				25		ns
LVDS INPUT TIMING							
			datadly	**clkdly**			
$t_{s(DATA)}$	Setup time(2)	D[x:0] valid to DATACLK rising for full word interface mode; DA[x:0] valid to DA_CLK rising or falling for 7-bit mode	0	0		–20	ps
			0	1		–120	ps
			0	2		–220	ps
			0	3		–310	ps
			0	4		–390	ps
			0	5		–480	ps
			0	6		–560	ps
			0	7		–630	ps
			1	0		70	ps
			2	0		150	ps
			3	0		230	ps
			4	0		330	ps
			5	0		430	ps
			6	0		530	ps
			7	0		620	ps

(1) Typical values at 25°C.
(2) Test conditions in config3 setting.

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Timing Requirements (continued)

with nominal supplies and $IOUT_{FS}$ = 20 mA (unless otherwise noted)

					MIN	TYP(1)	MAX	UNIT
$t_{h(DATA)}$	Hold time(2)	D[x:0] valid to DATACLK rising for full word interface mode; DA[x:0] valid to DA_CLK rising or falling for 7-bit bus mode	datadly	clkdly				
			0	0		310		ps
			0	1		390		ps
			0	2		480		ps
			0	3		560		ps
			0	4		650		ps
			0	5		740		ps
			0	6		850		ps
			0	7		930		ps
			1	0		200		ps
			2	0		100		ps
			3	0		20		ps
			4	0		–60		ps
			5	0		–140		ps
			6	0		–220		ps
			7	0		–290		ps

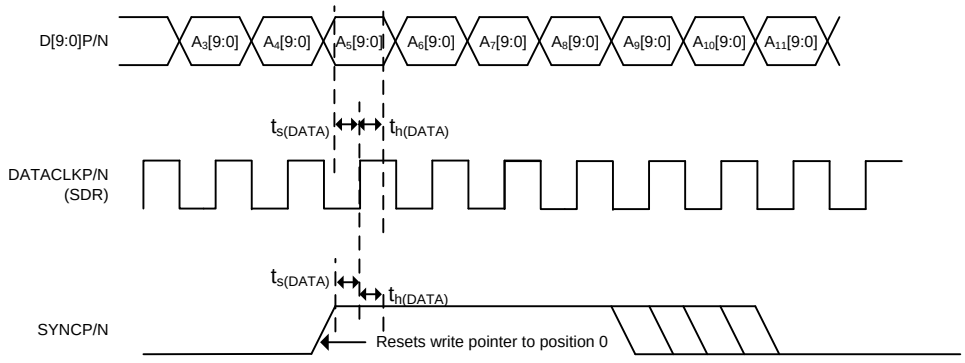


Figure 1. DAC3151 Input Data Timing Diagram

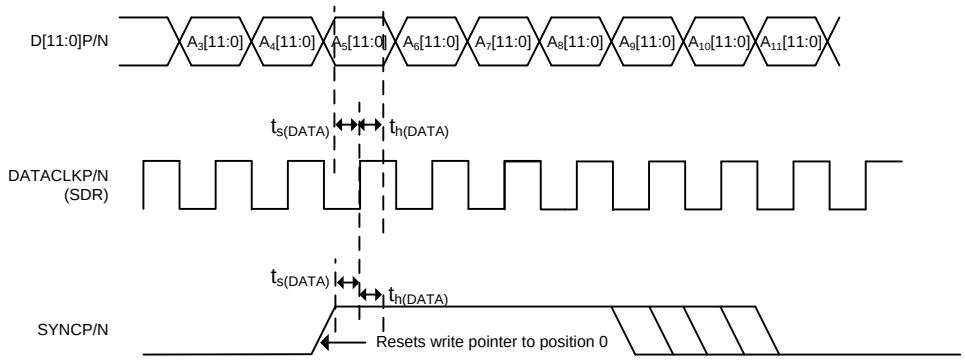


Figure 2. DAC3161 Input Data Timing Diagram

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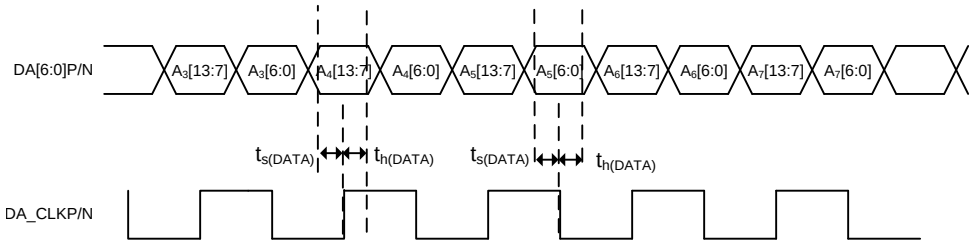


Figure 3. DAC3171 Input Data Timing Diagram for 7-Bit Interface Mode

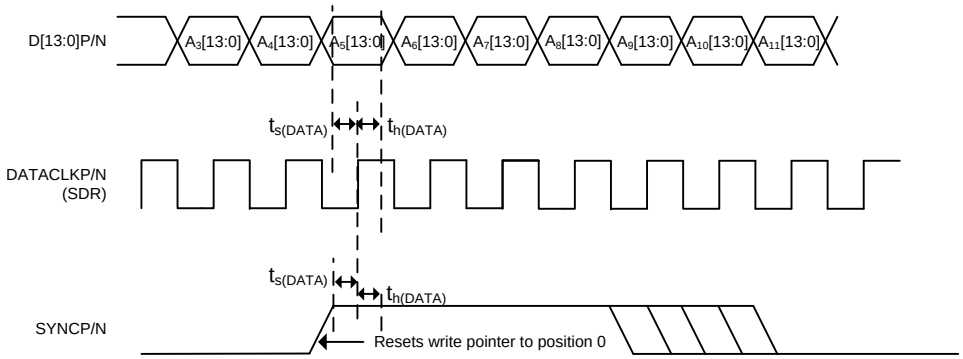


Figure 4. DAC3171 Input Data Timing for 14-Bit Interface Mode

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6.9 Typical Characteristics

all plots are at 25°C, nominal supply voltages, f_{DAC} = 500 MSPS, 50% clock duty cycle, 0-dBFS input signal and 20-mA full-scale output current (unless otherwise noted)

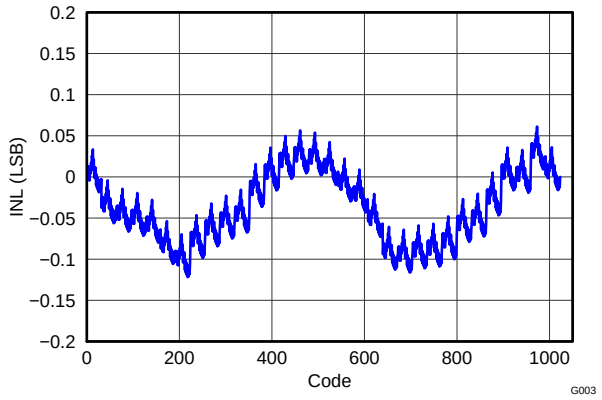


Figure 5. DAC3151 Integral Nonlinearity

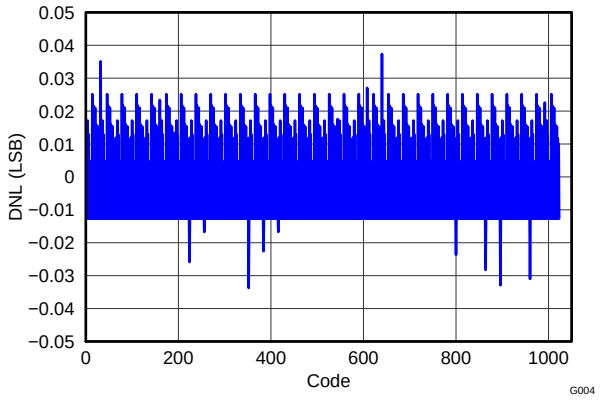


Figure 6. DAC3151 Differential Nonlinearity

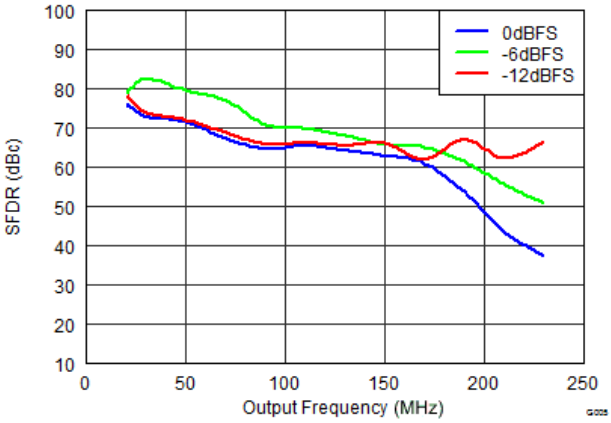


Figure 7. DAC3151 SFDR vs Output Frequency Over Input Scale

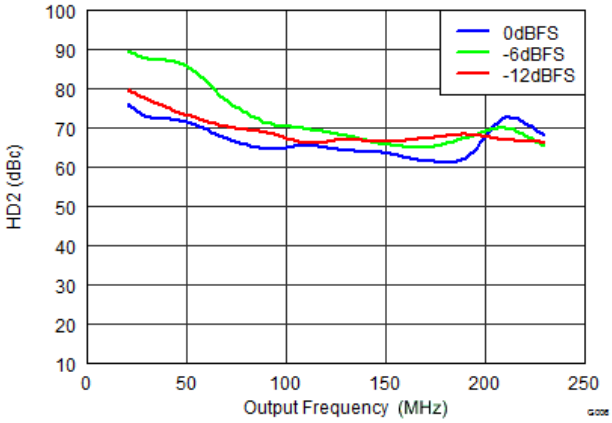


Figure 8. DAC3151 Second-Order Harmonic Distortion vs Output Frequency Over Input Scale

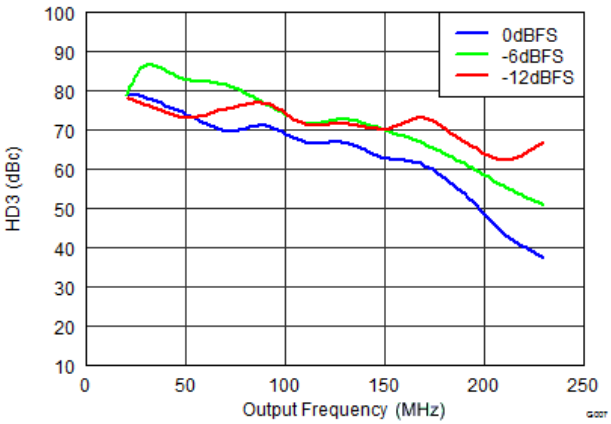


Figure 9. DAC3151 Third-Order Harmonic Distortion vs Output Frequency Over Input Scale

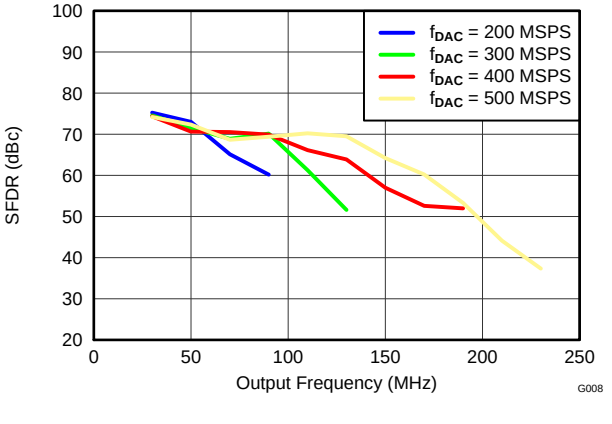


Figure 10. DAC3151 SFDR vs Output Frequency Over f_{DAC}

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Typical Characteristics (continued)

all plots are at 25°C, nominal supply voltages, f_{DAC} = 500 MSPS, 50% clock duty cycle, 0-dBFS input signal and 20-mA full-scale output current (unless otherwise noted)

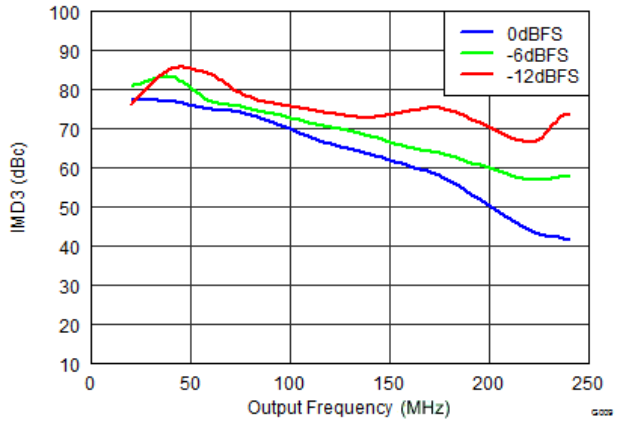


Figure 11. DAC3151 IMD3 vs Output Frequency Over Input Scale

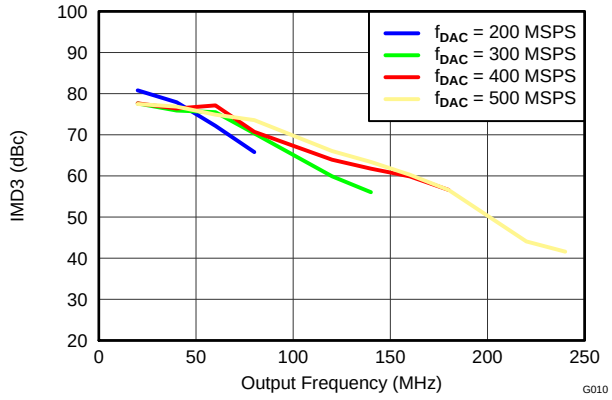


Figure 12. DAC3151 IMD3 vs Output Frequency Over f_{DAC}

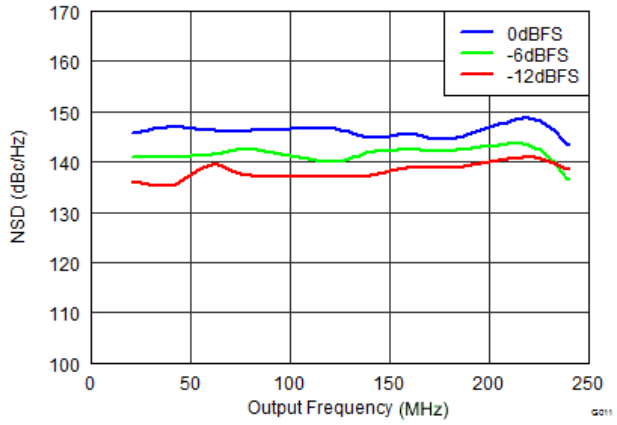


Figure 13. DAC3151 NSD vs Output Frequency Over Input Scale

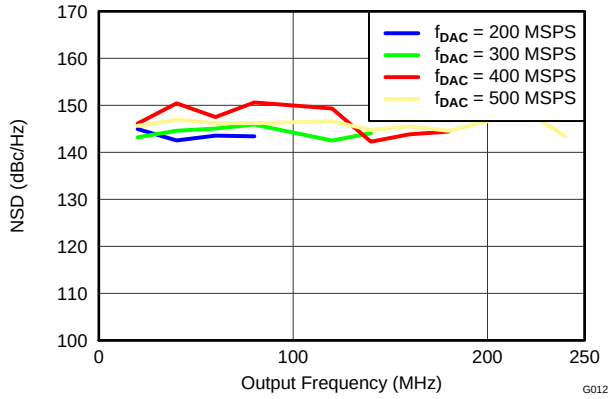


Figure 14. DAC3151 NSD vs Output Frequency Over f_{DAC}

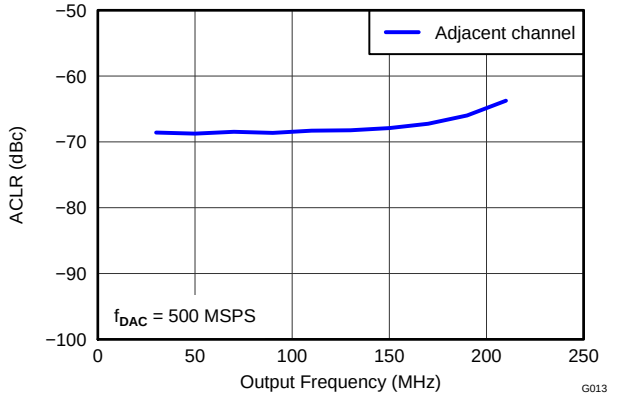


Figure 15. DAC3151 ACLR (Adjacent Channel) vs Output Frequency

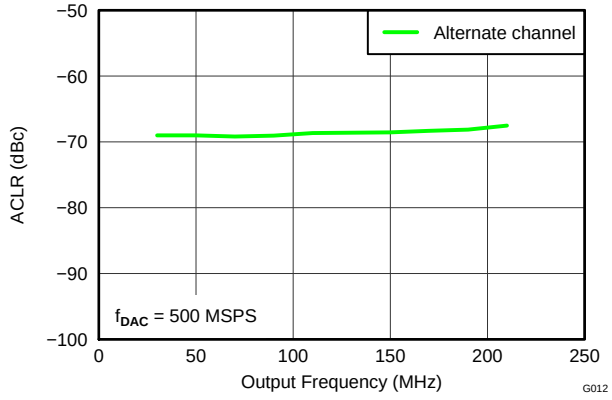


Figure 16. DAC3151 ACLR (Alternate Channel) vs Output Frequency

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Typical Characteristics (continued)

all plots are at 25°C, nominal supply voltages, f_{DAC} = 500 MSPS, 50% clock duty cycle, 0-dBFS input signal and 20-mA full-scale output current (unless otherwise noted)

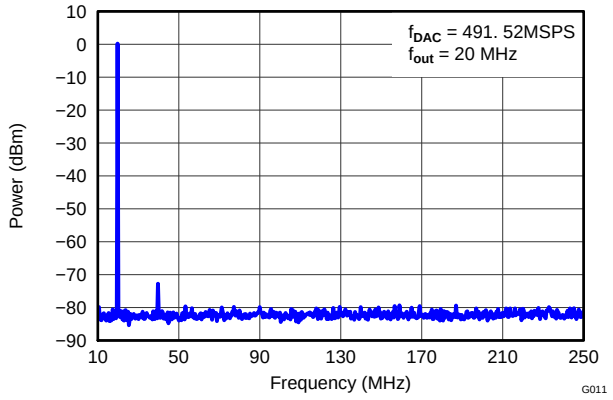


Figure 17. DAC3151 Single-Tone Spectral Plot (IF = 20 MHz)

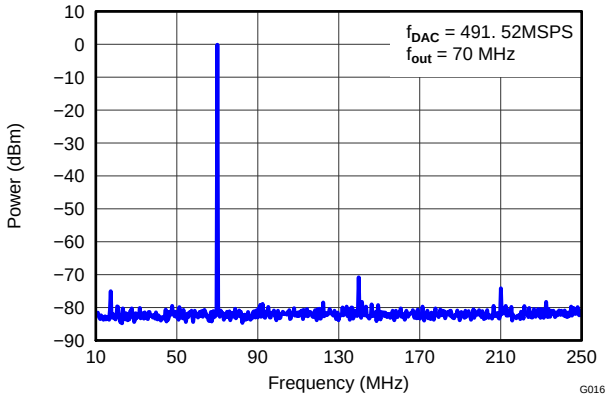


Figure 18. DAC3151 Single-Tone Spectral Plot (IF = 70 MHz)

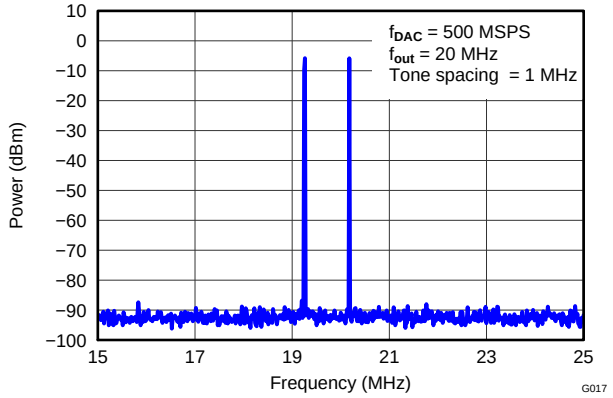


Figure 19. DAC3151 Two-Tone Spectral Plot (IF = 20 MHz)

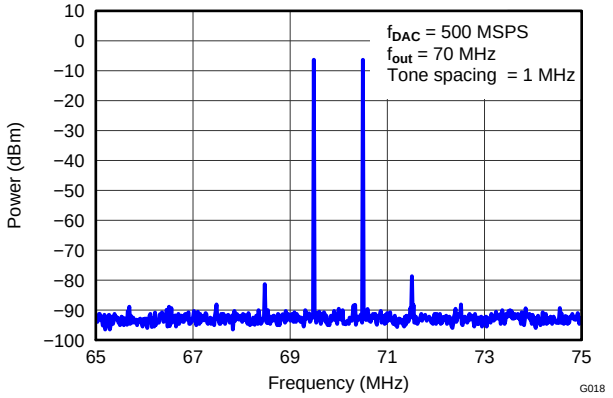


Figure 20. DAC3151 Two-Tone Spectral Plot (IF = 70 MHz)

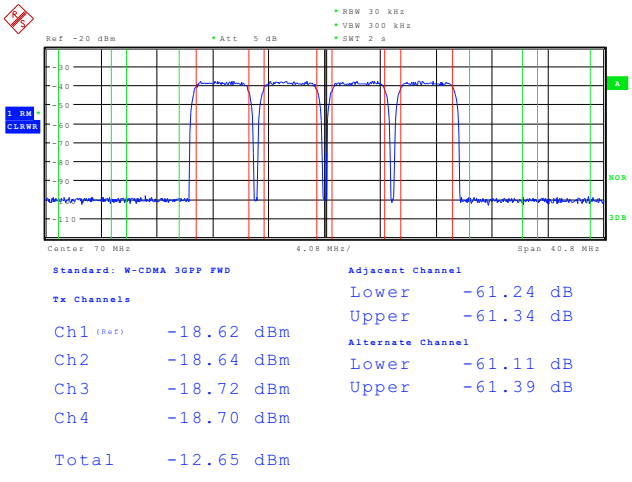


Figure 21. DAC3151 ACPR Four-Carrier WCDMA Test Mode 1

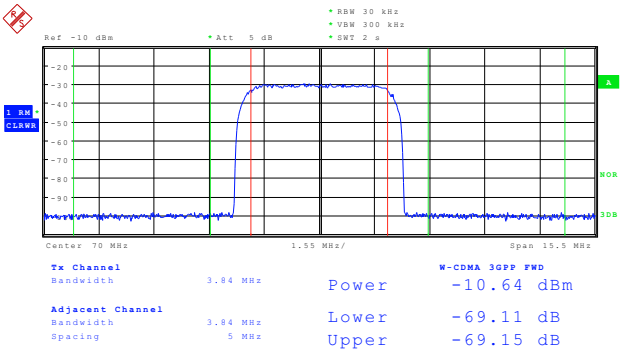


Figure 22. DAC3151 ACPR Single-Carrier WCDMA Test Mode 1

Typical Characteristics (continued)

all plots are at 25°C, nominal supply voltages, f_{DAC} = 500 MSPS, 50% clock duty cycle, 0-dBFS input signal and 20-mA full-scale output current (unless otherwise noted)

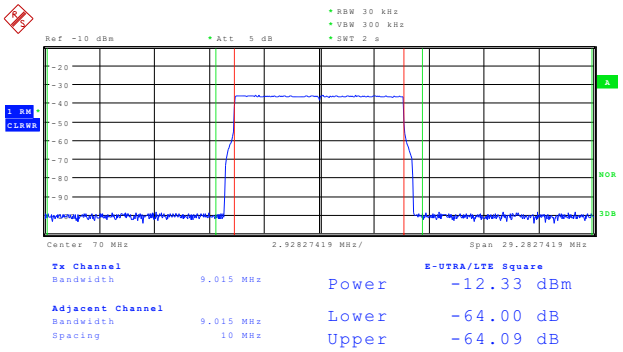


Figure 23. DAC3151 ACPR LTE 10-MHz FDD E-TM 1.1

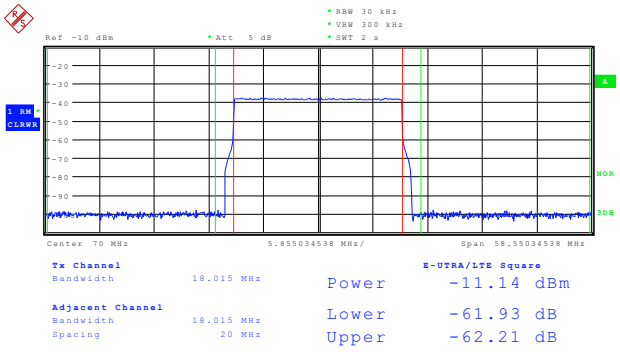


Figure 24. DAC3151 ACPR LTE 20-MHz FDD E-TM 1.1

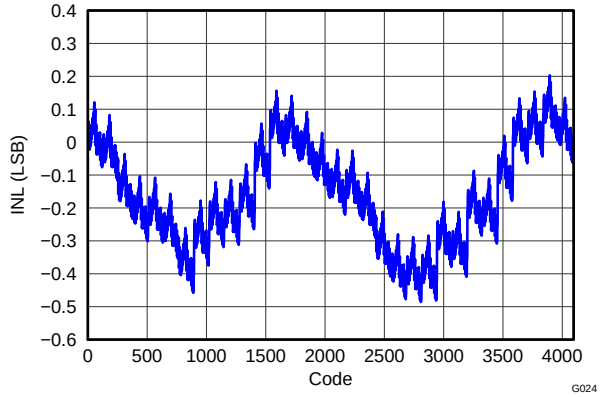


Figure 25. DAC3161 Integral Nonlinearity

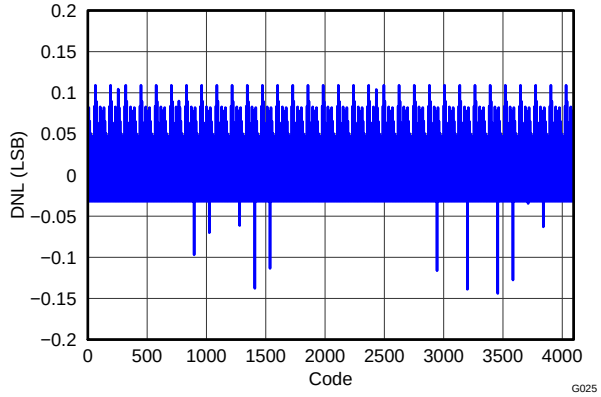


Figure 26. DAC3161 Differential Nonlinearity

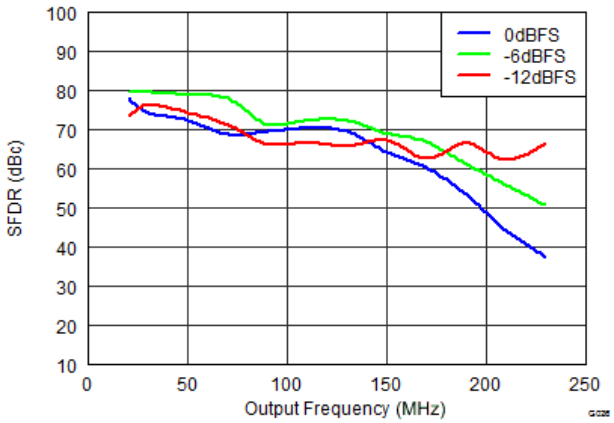


Figure 27. DAC3161 SFDR vs Output Frequency Over Input Scale

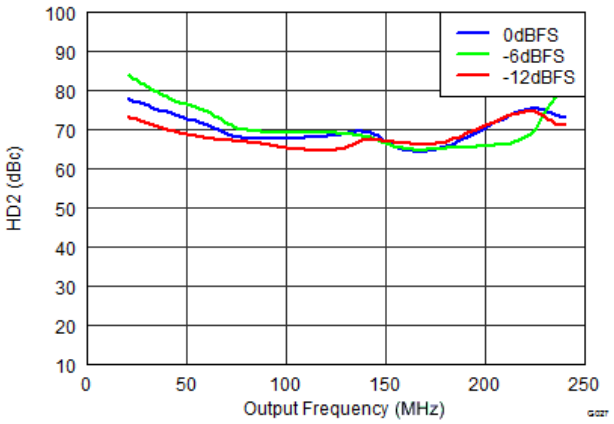


Figure 28. DAC3161 Second-Order Harmonic Distortion vs Output Frequency Over Input Scale

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Typical Characteristics (continued)

all plots are at 25°C, nominal supply voltages, f_{DAC} = 500 MSPS, 50% clock duty cycle, 0-dBFS input signal and 20-mA full-scale output current (unless otherwise noted)

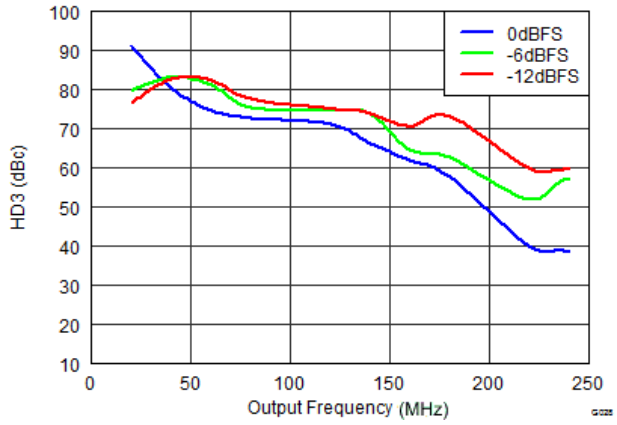


Figure 29. DAC3161 Third-Order Harmonic Distortion vs Output Frequency Over Input Scale

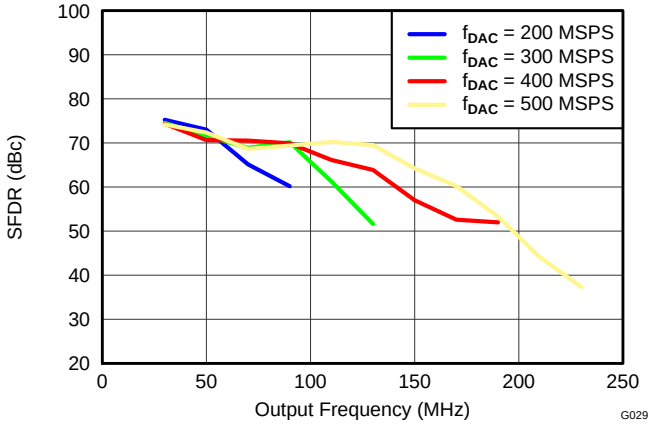


Figure 30. DAC3161 SFDR vs Output Frequency Over f_{DAC}

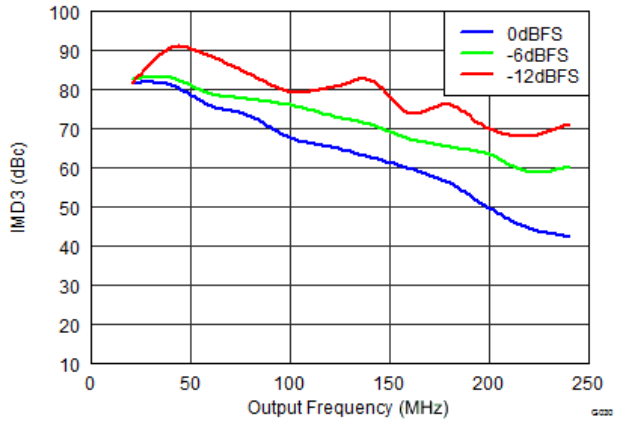


Figure 31. DAC3161 IMD3 vs Output Frequency Over Input Scale

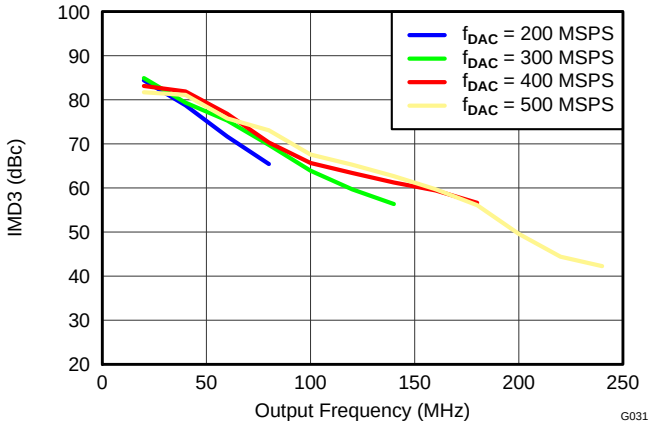


Figure 32. DAC3161 IMD3 vs Output Frequency Over f_{DAC}

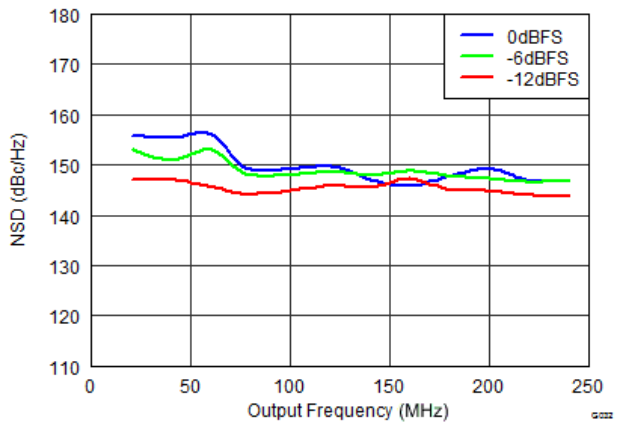


Figure 33. DAC3161 NSD vs Output Frequency Over Input Scale

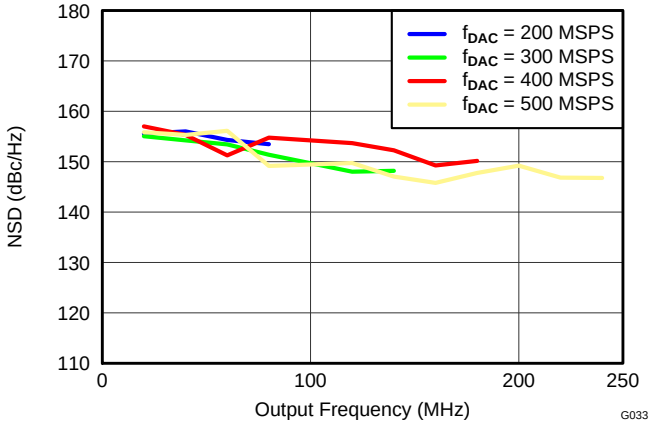


Figure 34. DAC3161 NSD vs Output Frequency Over f_{DAC}

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Typical Characteristics (continued)

all plots are at 25°C, nominal supply voltages, f_{DAC} = 500 MSPS, 50% clock duty cycle, 0-dBFS input signal and 20-mA full-scale output current (unless otherwise noted)

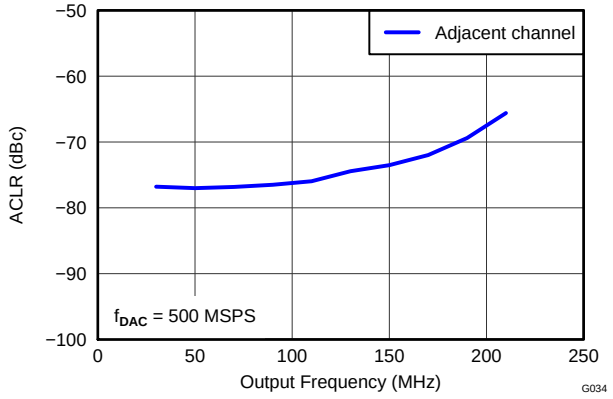


Figure 35. DAC3161 ACLR (Adjacent Channel) vs Output Frequency

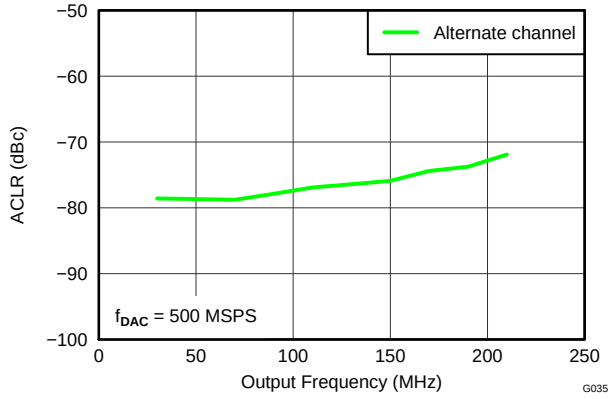


Figure 36. DAC3161 ACLR (Alternate Channel) vs Output Frequency

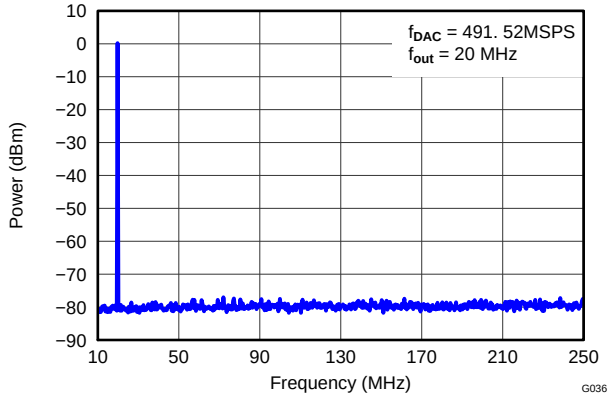


Figure 37. DAC3161 Single-Tone Spectral Plot (IF = 20 MHz)

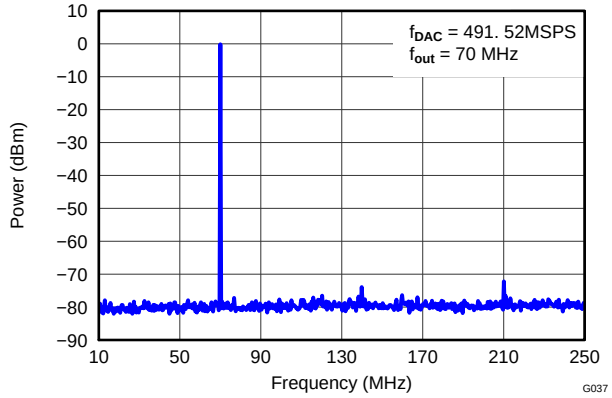


Figure 38. DAC3161 Single-Tone Spectral Plot (IF = 70 MHz)

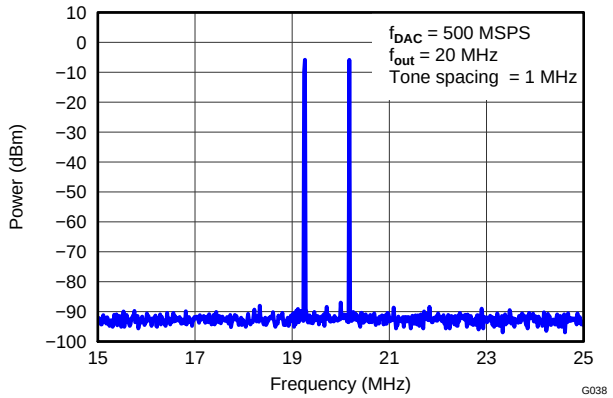


Figure 39. DAC3161 Two-Tone Spectral Plot (IF = 20 MHz)

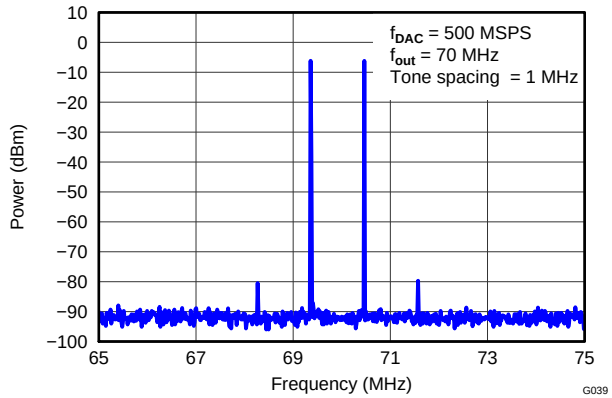


Figure 40. DAC3161 Two-Tone Spectral Plot (IF = 70 MHz)

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Typical Characteristics (continued)

all plots are at 25°C, nominal supply voltages, f_{DAC} = 500 MSPS, 50% clock duty cycle, 0-dBFS input signal and 20-mA full-scale output current (unless otherwise noted)

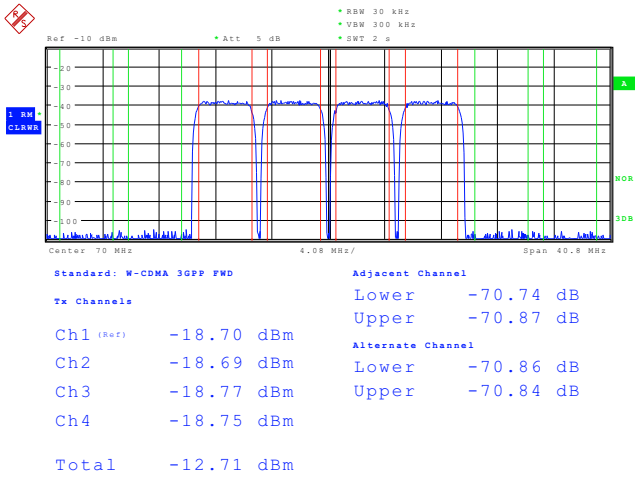


Figure 41. DAC3161 ACPR Four-Carrier WCDMA Test Mode 1

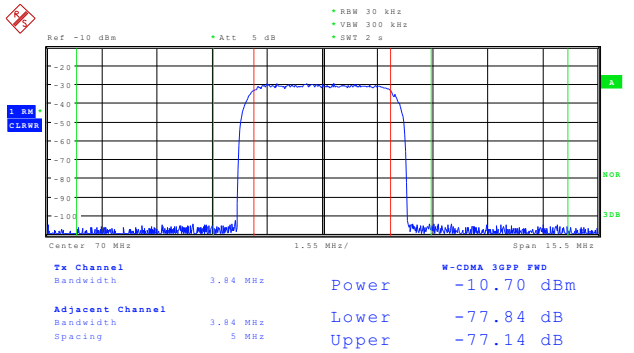


Figure 42. DAC3161 ACPR Single-Carrier WCDMA Test Mode 1

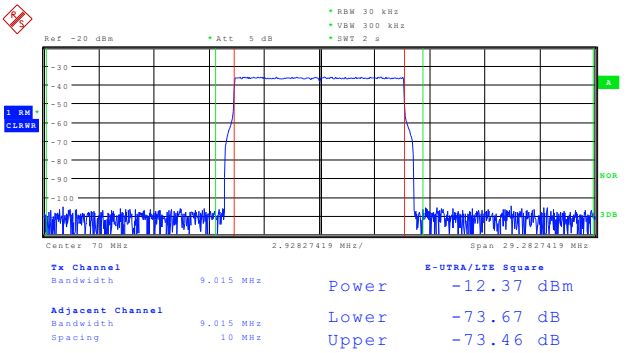


Figure 43. DAC3161 ACPR LTE 10-MHz FDD E-TM 1.1

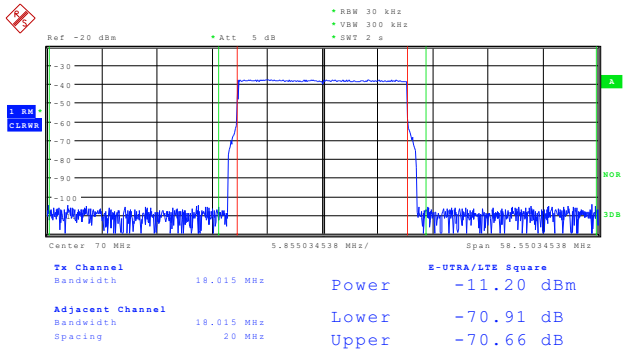


Figure 44. DAC3161 ACPR LTE 20-MHz FDD E-TM 1.1

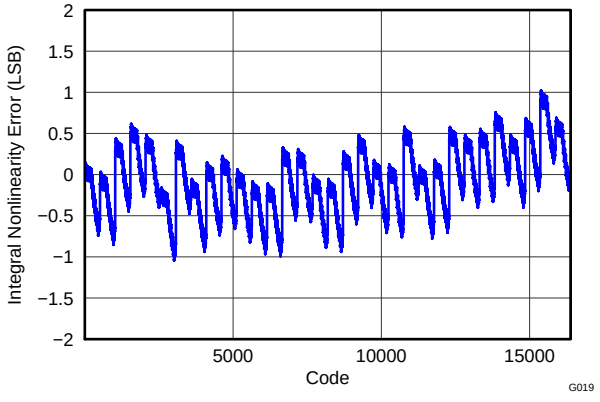


Figure 45. DAC3171 Integral Nonlinearity

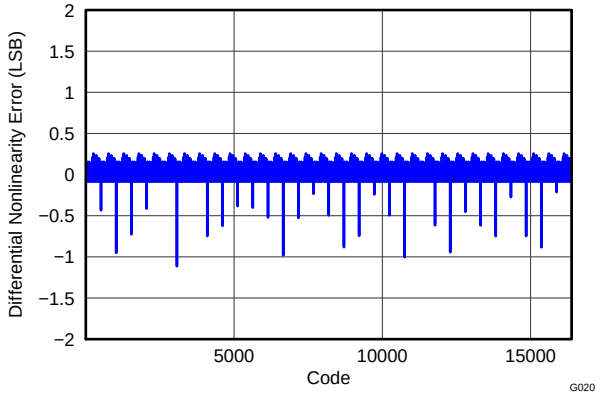


Figure 46. DAC3171 Differential Nonlinearity

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Typical Characteristics (continued)

all plots are at 25°C, nominal supply voltages, f_{DAC} = 500 MSPS, 50% clock duty cycle, 0-dBFS input signal and 20-mA full-scale output current (unless otherwise noted)

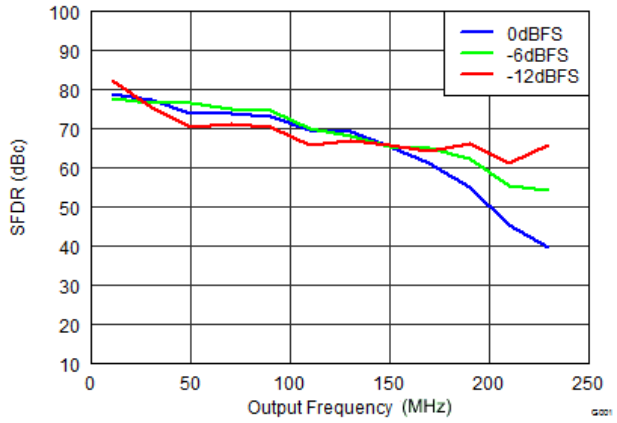


Figure 47. DAC3171 SFDR vs Output Frequency Over Input Scale

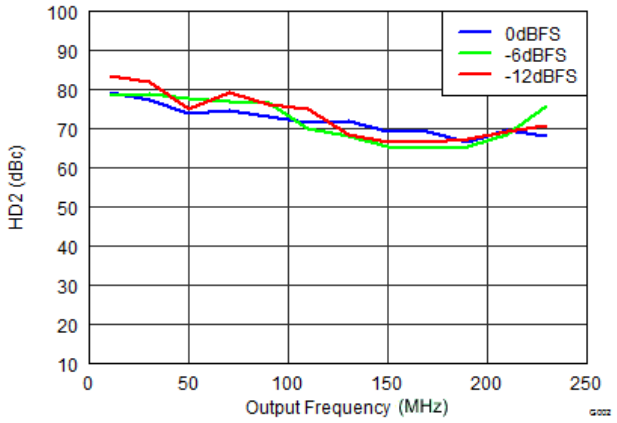


Figure 48. DAC3171 Second-Order Harmonic Distortion vs Output Frequency Over Input Scale

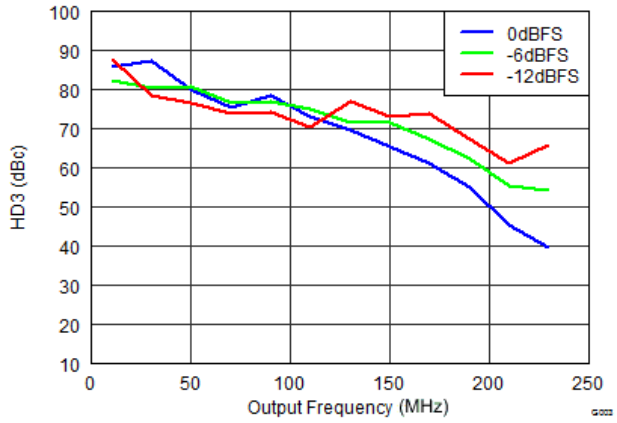


Figure 49. DAC3171 Third-Order Harmonic Distortion vs Output Frequency Over Input Scale

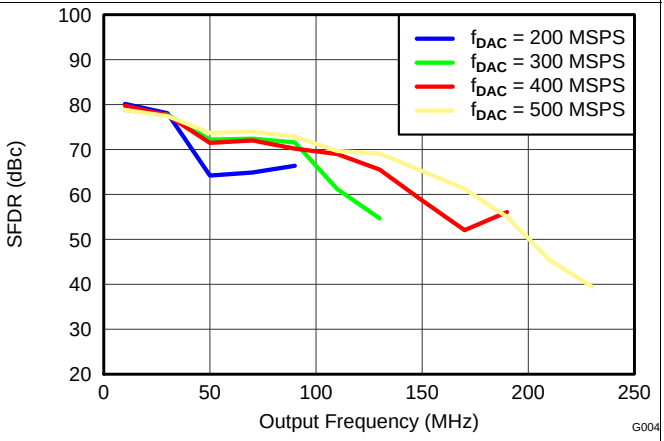


Figure 50. DAC3171 SFDR vs Output Frequency Over f_{DAC}

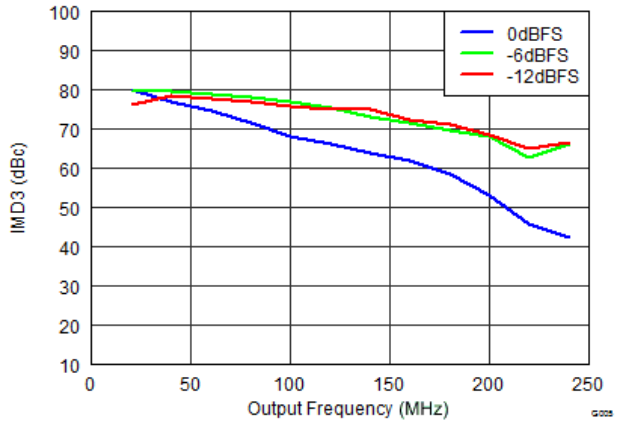


Figure 51. DAC3171 IMD3 vs Output Frequency Over Input Scale

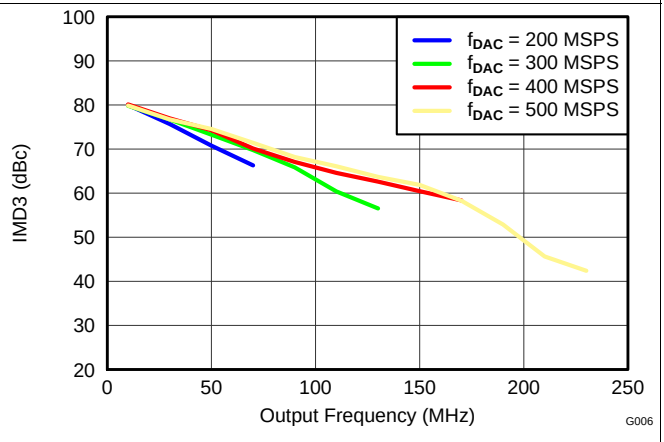


Figure 52. DAC3171 IMD3 vs Output Frequency Over f_{DAC}

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Typical Characteristics (continued)

all plots are at 25°C, nominal supply voltages, f_{DAC} = 500 MSPS, 50% clock duty cycle, 0-dBFS input signal and 20-mA full-scale output current (unless otherwise noted)

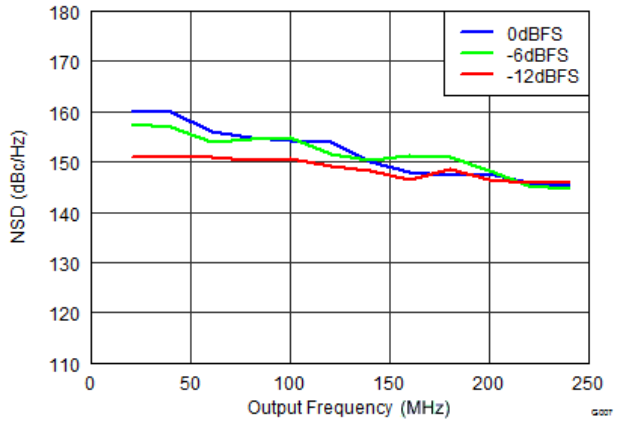


Figure 53. DAC3171 NSD vs Output Frequency Over Input Scale

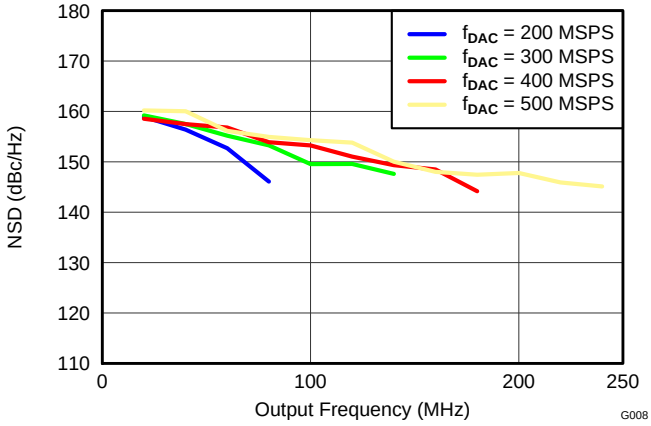


Figure 54. DAC3171 NSD vs Output Frequency Over f_{DAC}

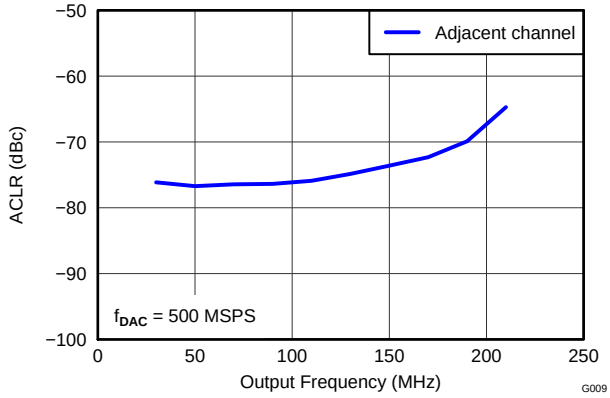


Figure 55. DAC3171 ACLR (Adjacent Channel) vs Output Frequency

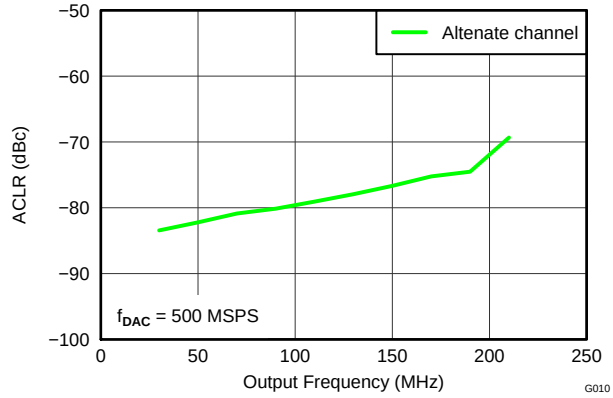


Figure 56. DAC3171 ACLR (Alternate Channel) vs Output Frequency

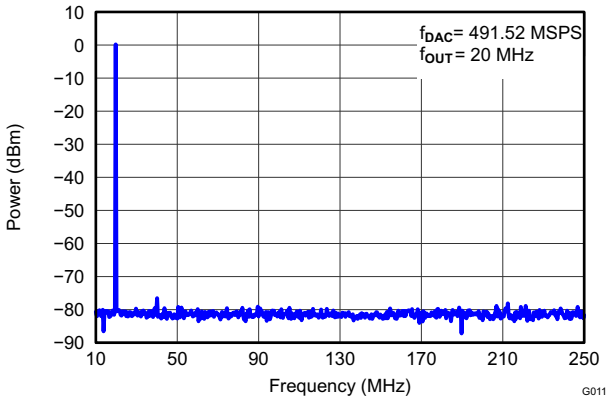


Figure 57. DAC3171 Single-Tone Spectral Plot (IF = 20 MHz)

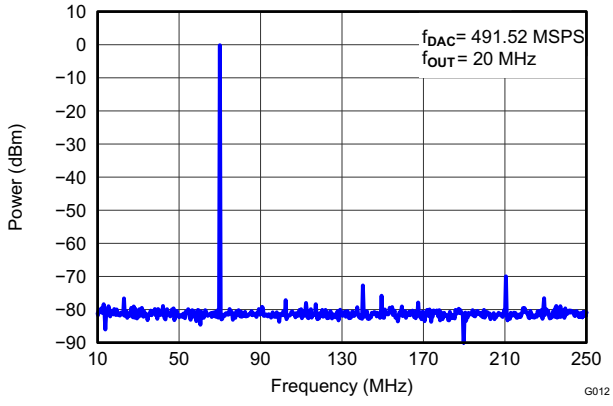


Figure 58. DAC3171 Single-Tone Spectral Plot (IF = 70 MHz)

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Typical Characteristics (continued)

all plots are at 25°C, nominal supply voltages, f_{DAC} = 500 MSPS, 50% clock duty cycle, 0-dBFS input signal and 20-mA full-scale output current (unless otherwise noted)

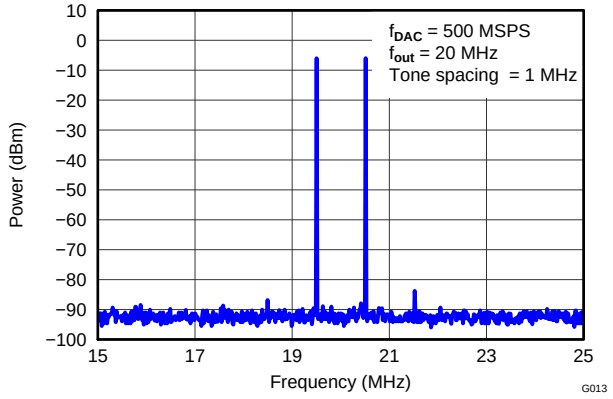


Figure 59. DAC3171 Two-Tone Spectral Plot (IF = 20 MHz)

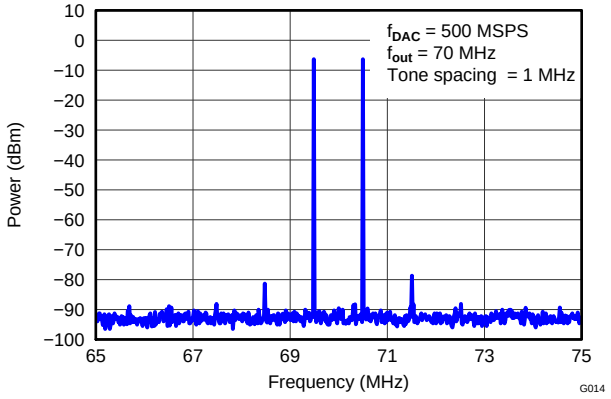


Figure 60. DAC3171 Two-Tone Spectral Plot (IF = 70 MHz)



Figure 61. DAC3171 Four-Carrier WCDMA Test Mode 1

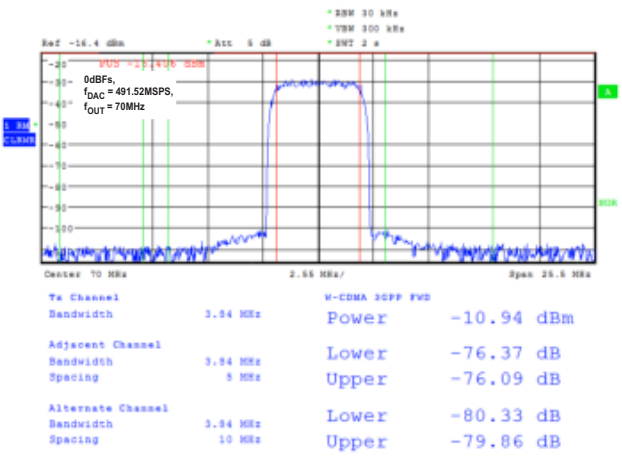


Figure 62. DAC3171 Single-Carrier WCDMA Test Mode 1

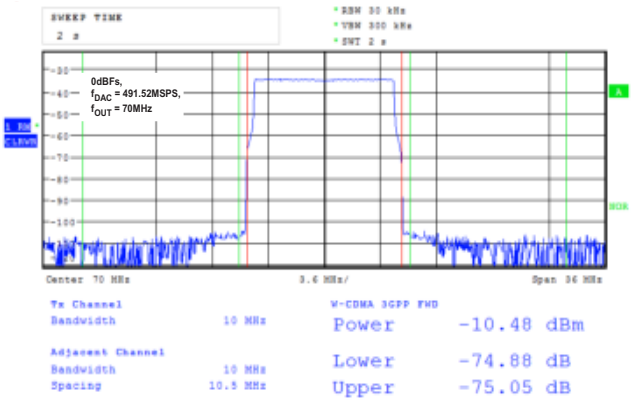


Figure 63. DAC3171 10-MHz Single-Carrier LTE Test Mode 3.1

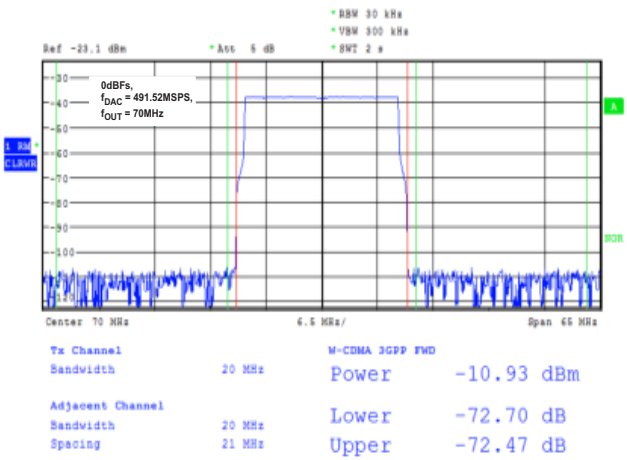


Figure 64. DAC3171 20-MHz Single-Carrier LTE Test Mode 3.1

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Typical Characteristics (continued)

all plots are at 25°C, nominal supply voltages, f_{DAC} = 500 MSPS, 50% clock duty cycle, 0-dBFS input signal and 20-mA full-scale output current (unless otherwise noted)

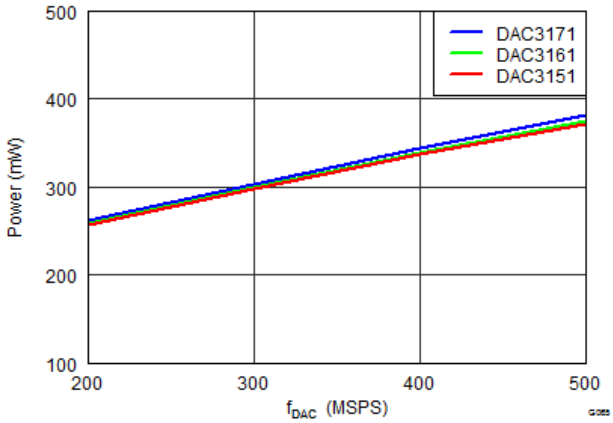


Figure 65. Power Consumption vs f_{DAC}

7 Detailed Description

7.1 Overview

The DAC3171 is a single channel, 14-bit, 500-MSPS, digital-to-analog converter and uses a 14-bit-wide LVDS digital bus with an input FIFO. The DAC3171 also supports a DDR 7-bit LVDS interface mode.

The DAC3161 is a single channel, 12-bit, 500-MSPS, digital-to-analog converter and uses a 12-bit-wide LVDS digital bus with an input FIFO.

The DAC3151 is a single channel, 10-bit, 500-MSPS, digital-to-analog converter and uses a 10-bit-wide LVDS digital bus with an input FIFO.

These devices (DAC31x1) have separate input data clock and output DAC clock. The FIFO input and output pointers can be synchronized across multiple devices for precise signal synchronization. The DAC outputs are current sourcing and terminate to GND with a compliance range of –0.5 V to +1 V. The DAC31x1 are pin compatible with the DAC31x4 family.

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7.2 Functional Block Diagrams

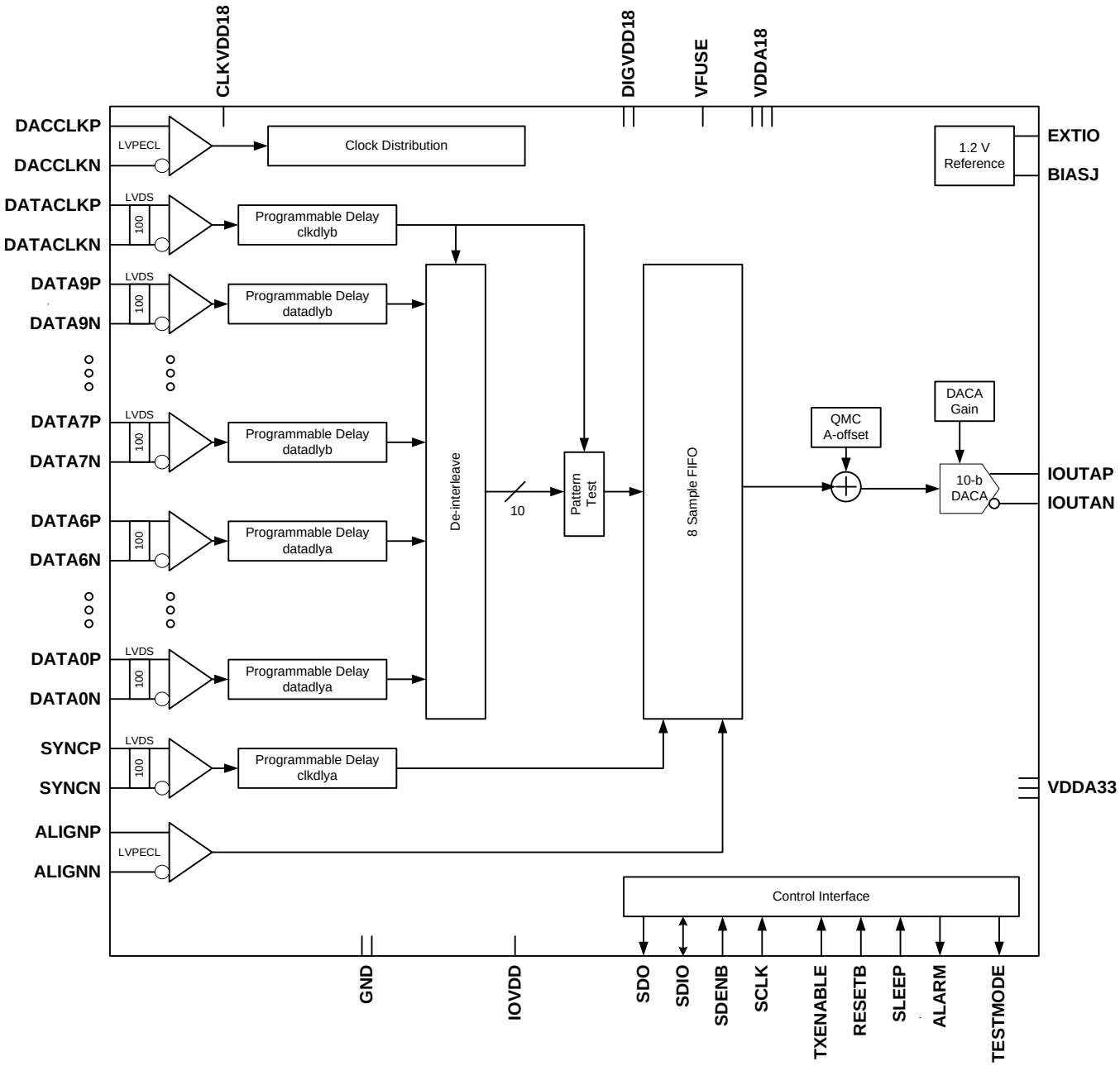


Figure 66. DAC3151 Functional Block Diagram

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Functional Block Diagrams (continued)

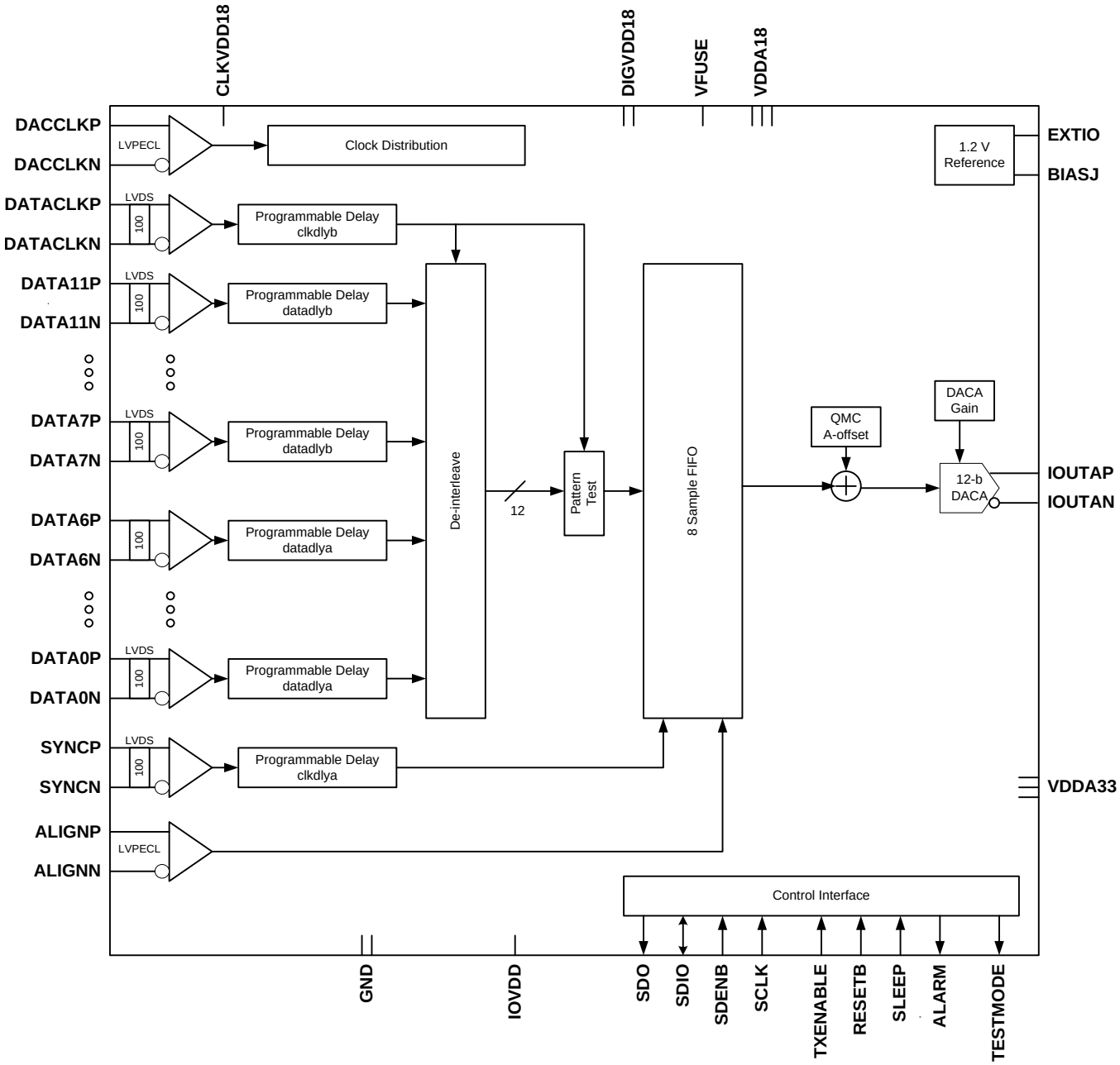


Figure 67. DAC3161 Functional Block Diagram

Functional Block Diagrams (continued)

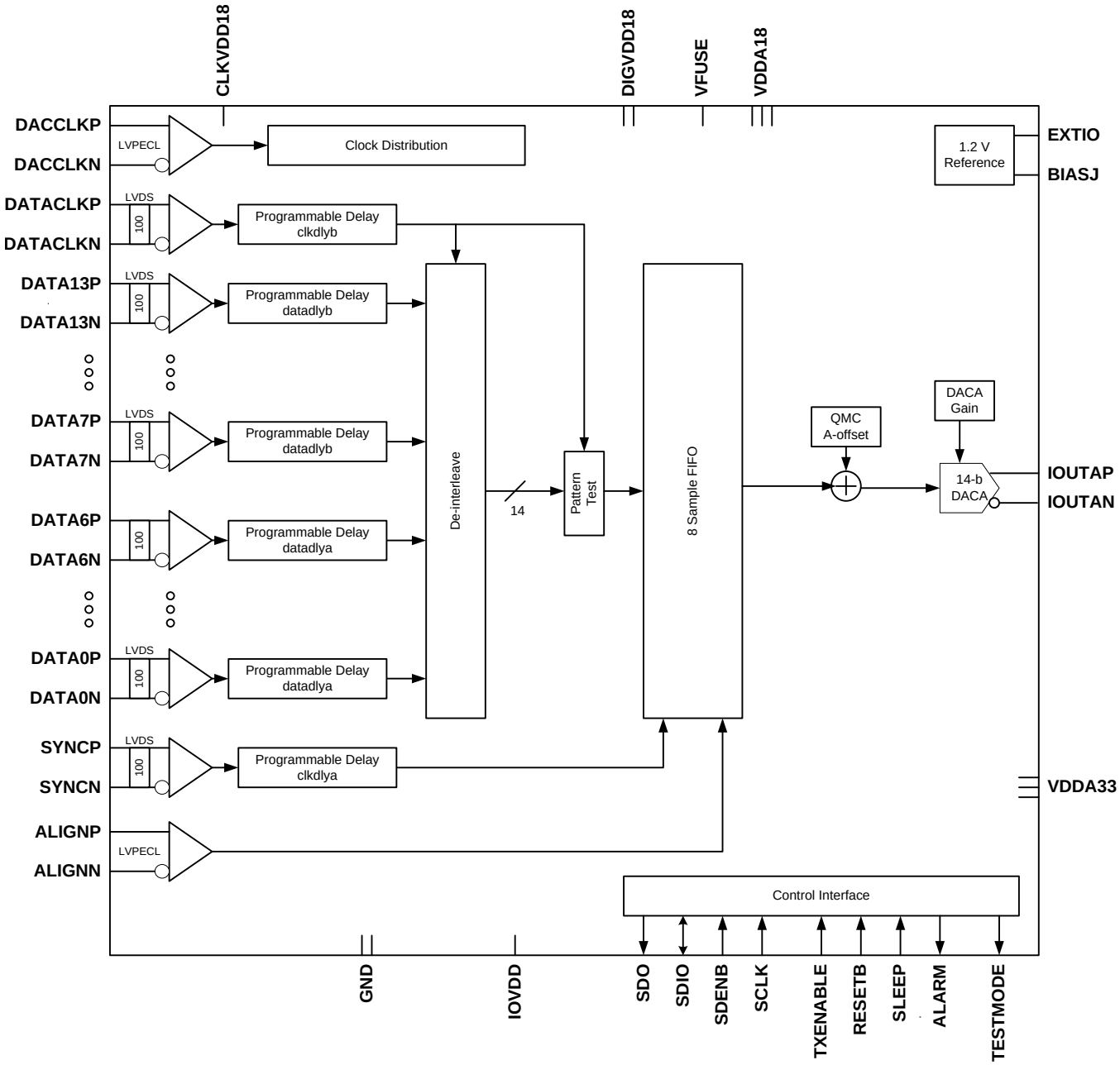


Figure 68. DAC3171 Functional Block Diagram

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Functional Block Diagrams (continued)

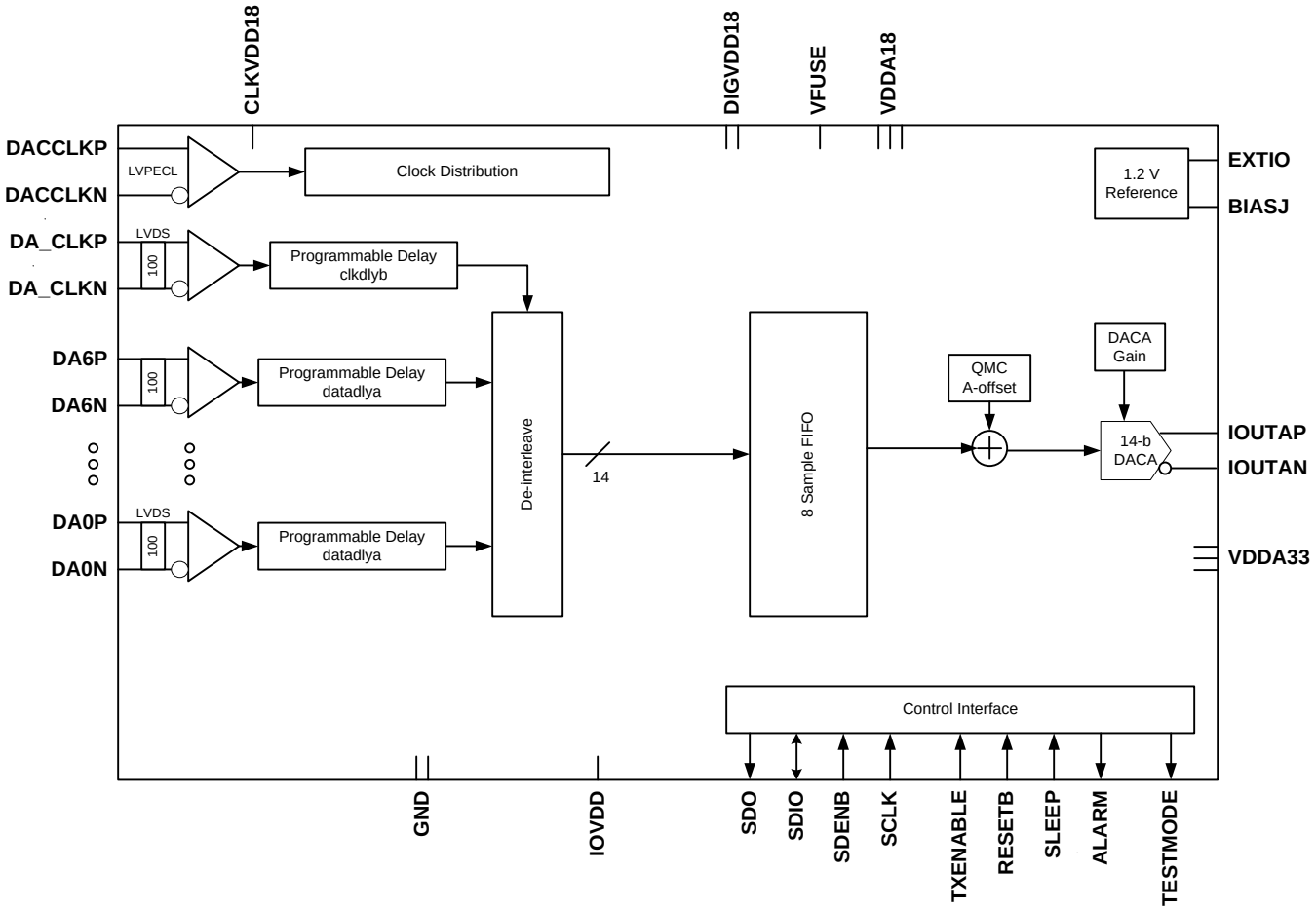


Figure 69. DAC3171 7-Bit Interface Mode

7.3 Feature Description

7.3.1 Data Input Formats

Table 1. DAC3151: 10-Bit Interface Mode

DIFFERENTIAL PAIR (P/N)	BITS	
	DATACLK RISING EDGE	DATACLK FALLING EDGE
D9	A9	–
D8	A8	–
D7	A7	–
D6	A6	–
D5	A5	–
D4	A4	–
D3	A3	–
D2	A2	–
D1	A1	–
D0	A0	–
SYNC	FIFO Write Reset	–

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Table 2. DAC3161: 12-Bit Interface Mode

DIFFERENTIAL PAIR (P/N)	BITS	
	DATACLK RISING EDGE	DATACLK FALLING EDGE
D11	A11	–
D10	A10	–
D9	A9	–
D8	A8	–
D7	A7	–
D6	A6	–
D5	A5	–
D4	A4	–
D3	A3	–
D2	A2	–
SYNC	FIFO Write Reset	–

Table 3. DAC3171: 7-Bit Interface Mode

DIFFERENTIAL PAIR (P/N)	BITS	
	DA_CLK RISING EDGE	DA_CLK FALLING EDGE
DA6	A13	A6
DA5	A12	A5
DA4	A11	A4
DA3	A10	A3
DA2	A9	A2
DA1	A8	A1
DA0	A7	A0

Table 4. DAC3171: 14-Bit Interface Mode

DIFFERENTIAL PAIR (P/N)	BITS	
	DATACLK RISING EDGE	DATACLK FALLING EDGE
D13	A13	–
D12	A12	–
D11	A11	–
D10	A10	–
D9	A9	–
D8	A8	–
D7	A7	–
D6	A6	–
D5	A5	–
D4	A4	–
D3	A3	–
D2	A2	–
D1	A1	–
D0	A0	–
SYNC	FIFO Write Reset	–

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7.3.2 Serial Interface

The serial port of the DAC31x1 is a flexible serial interface that communicates with industry-standard microprocessors and microcontrollers. The interface provides read and write access to all registers used to define the operating modes of DAC31x1. The interface is compatible with most synchronous transfer formats, and can be configured as a 3 or 4 pin interface by *sif4_ena* in register XYZ. In both configurations, SCLK is the serial interface input clock, and SDENB is serial interface enable. For 3-pin configuration, SDIO is a bidirectional pin for both data in and data out. For 4-pin configuration, SDIO is data in only, and SDO is data out only. Data are input into the device with the rising edge of SCLK. Data are output from the device on the falling edge of SCLK.

Each read and write operation is framed by the serial data enable bar signal (SDENB) asserted low. The first frame byte is the instruction cycle, which identifies the following data transfer cycle as read or write, as well as the 7-bit address to be accessed. Table 5 indicates the function of each bit in the instruction cycle, and is followed by a detailed description of each bit. The data transfer cycle consists of two bytes.

Table 5. Instruction Byte of the Serial interface

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Description	Read or Write	A6	A5	A4	A3	A2	A1	A0

Read or Write	Identifies the following data transfer cycle as a read or write operation. A high indicates a read operation from DAC31x1 and a low indicates a write operation to DAC31x1.
[A6:A0]	Identifies the address of the register to be accessed during the read or write operation.

Figure 70 shows the serial interface timing diagram for a DAC31x1 write operation. SCLK is the serial interface clock input to DAC31x1. Serial data enable SDENB is an active low input to DAC31x1. SDIO is serial data in. Input data to DAC31x1 is clocked on the rising edges of SCLK.

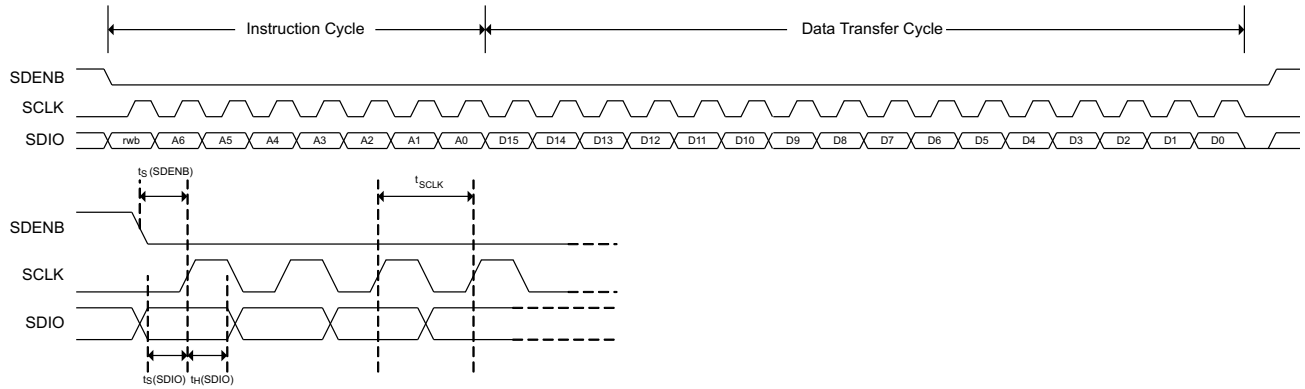


Figure 70. Serial Interface Write Timing Diagram

Figure 71 illustrates the serial interface timing diagram for a DAC31x1 read operation. SCLK is the serial interface clock input to DAC31x1. Serial data enable SDENB is an active low input to DAC31x1. SDIO is serial data in during the instruction cycle. In 3-pin configuration, SDIO is data out from the DAC31x1 during the data transfer cycle, while SDO is in a high-impedance state. In 4-pin configuration, both SDIO and SDO are data out from the DAC31x1 during the data transfer cycle. At the end of the data transfer, SDIO and SDO output low on the final falling edge of SCLK until the rising edge of SDENB when SDIO and SDO go to a high-impedance state.

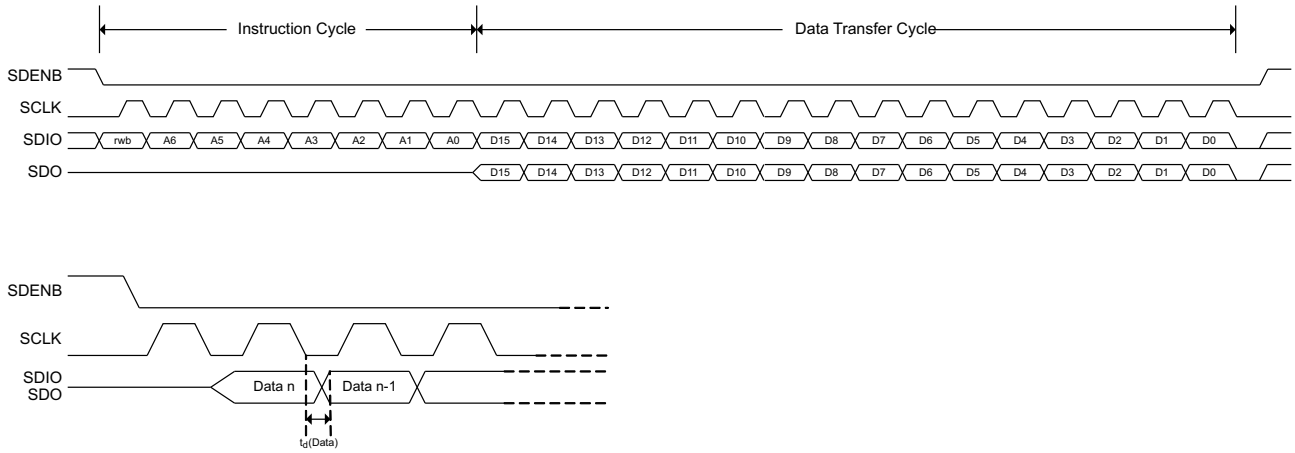


Figure 71. Serial Interface Read Timing Diagram

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7.4 Device Functional Modes

7.4.1 Synchronization Modes

There are three modes of syncing included in the DAC31x1: NORMAL Dual Sync, SYNC ONLY, and SIF_SYNC.

- NORMAL Dual Sync: The SYNC pin is used to align the input side of the FIFO (write pointers) with the A(0) sample. The ALIGN pin is used to reset the output side of the FIFO (read pointers) to the offset value. Multiple chip alignment can be accomplished with this kind of syncing.
- SYNC ONLY: In this mode only the SYNC pin is used to sync both the read and write pointers of the FIFO. There is an asynchronized handoff between the DATACLK and DACCLK when using this mode therefore, it is impossible to accurately align multiple chips closer than 2 T or 3 T.
- SIF_SYNC: When neither SYNC nor ALIGN are used, a programmable SYNC pulse can be used to sync the design. However, the same issues as ISTROBE ONLY apply. There is an asynchronized handoff between the serial clock domain and the two sides of the FIFO. As a result of of the asynchronous nature of the SIF_SYNC, it is impossible to align the sync up with any sample at the input. SIF_SYNC mode is the only synchronisation mode supported in the 7-bit interface mode.

NOTE

When ALIGNP or ALIGNN is not used, TI recommends clearing the alignrx_ena register (config1, bit 4), and tie ALIGNP to DIGVDD18 and ALIGNN to GROUND. When SYNCP or SYNCN is not used, clear the register lvdssyncrx_ena (config0, bit3), and the unused SYNCP or SYNCN pins can be left open or tied to GROUND.

7.4.2 Alarm Monitoring

The DAC31x1 includes flexible alarm monitoring that can be used to alert a possible malfunction scenario. All alarm events can be accessed either through the SIP registers or through the ALARM pin. After an alarm is set, the corresponding alarm bit in register config5 must be reset through the serial interface to allow further testing. The set of alarms includes: zero check alarm, FIFO alarms, clock alarms, and pattern checker alarm.

Zero check alarm:

- Alarm_from_zerochk occurs when the FIFO write pointer has an all zeros pattern. The write pointer is a shift register; therefore, all zeros cause the input point to be stuck until the next sync event. When this alarm triggers, a sync to the FIFO block is required.

FIFO alarms:

- alarm_from_fifo occurs when there is a collision in the FIFO pointers or a collision event is close.
- alarm_fifo_2away occurs when pointers are within two addresses of each other.
- alarm_fifo_1away occurs when pointers are within one address of each other.
- alarm_fifo_collision occurs when pointers are equal to each other.

Clock alarms:

- clock_gone occurs when either the DACCLK or DATACLOCK have been stopped.
- alarm_dacclk_gone occurs when the DACCLK has been stopped.
- alarm_dataclk_gone occurs when the DATACLK has been stopped.

Pattern checker alarm:

- alarm_from_iotest occurs when the input data pattern does not match the pattern key.

To prevent unexpected DAC outputs from propagating into the transmit channel chain, the DAC31x1 includes a feature that disables the outputs when a catastrophic alarm occurs. The catastrophic alarms include FIFO pointer collision, the loss DACCLK, or the loss of DATACLK. When any of these alarms occur, the internal TXenable signal is driven low, causing a zeroing of the data going to the DAC in < 10 T. One caveat is if both clocks stop, the circuit cannot determine clock loss, so no alarms are generated; therefore, no zeroing of output data occurs.

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7.5 Programming

7.5.1 Power-Up Sequence

The following startup sequence is recommended to power-up the DAC31x1:

1. Set TXENABLE low to prevent an unknown or undesirable output during the power-up sequence.
2. Supply all 1.8-V voltages (CLKVDD18, DIGVDD18, VDDA18, VFUSE, and possibly IOVDD) and all 3.3-V voltages (VDDA33 and possibly IOVDD). The 1.8-V and 3.3-V supplies can be powered up simultaneously or in any order. There are no specific requirements on the ramp rate for the supplies.
3. Provide all LVPECL inputs: DACCLKP, DACCLKN and the optional ALIGNP, ALIGNN. These inputs can also be provided after the SIF register programming.
4. Toggle the RESETB pin for a minimum of a 25-ns active low pulse duration.
5. Program the SIF registers.
6. Enable transmit of data by asserting the TXENABLE pin.

7.6 Register Map

In the SIF interface, there are three types of registers:

NORMAL: The NORMAL register type allows data to be written and read from. All 16-bits of the data are registered at the same time. There is no synchronizing with an internal clock thus all register writes are asynchronous with respect to internal clocks. There are three subtypes of NORMAL:

- **AUTOSYNC:** A NORMAL register that causes a sync to be generated after the write is finished. These registers are most commonly used for settings such as offset and phase, where there is a word or block setup that extends across multiple registers, and all of the registers must be programmed before any take effect on the circuit. Therefore, the design allows all the registers to be written. When the last register for this block is finished, an autosync is generated telling the mixer to grab all the new SIF values. The autosync occurs on a mixer clock cycle so that there are no metastability errors.
- **No RESET Value:** These are NORMAL registers, but for one reason or another reset value cannot be specified. The reason may be because the register has some read_only bits or some internal logic partially controls the bit values. An example is the SIF_CONFIG6 register, where the bits come from the temperature sensor and the fuses. Depending on which fuses are blown and the temperature of the die, the reset value will be different.
- **FUSE controlled:** While not a type of register, FUSE_controlled may be seen in the default-value column for the register. Fuses will change the default value, and the value shown in the default-value column is for when no fuses are blown.

READ_ONLY: Registers that are internal wires ANDed with the address bus, and then connected to the SIF output data bus.

WRITE_TO_CLEAR: These registers are just like NORMAL registers with one exception. These registers can be written and read; however, when the internal logic asynchronously sets a bit high in one of these registers, that bit stays high until it is written to 0. In this way, interrupts are captured and stay constant until cleared by the user.

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Table 6. Register Map

Name	Address	Default	Bit 15 (MSB)	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
config0	0x00	0x44FC	qmc_offset_ena	dual_ena	chipwidth (1:0)		rev	twos	sif4_ena	reserved	fifo_ena	alarm_out_ena	alarm_out_pol	alignrx_ena	lvdssyncrx_ena	lvdsdataclk_ena	reserved	synconly_ena
config1	0x01	0x600E	iotest_ena	reserved	fullword_interface_ena	64cnt_ena	dacclkgone_ena	dataclkgone_end	collision_ena	reserved	daca_compliment	reserved	sif_sync	sif_sync_ena	alarm_2away_ena	alarm_1away_ena	alarm_collision_ena	reserved
config2	0x02	0x3FFF	reserved	reserved	lvdsdata_ena (13:0)													
config3	0x03	0x0000	datadlya (2:0)		clkdlya (2:0)		datadlyb(2:0)				clkdlyb(2:0)				extref_ena	reserved		dual_ena
config4	0x04	0x0000	reserved		iotest_results (13:0)													
config5	0x05	0x0000	alarm_from_zerochka	reserved	alarms_from_fifoa (2:0)		reserved				alarm_dacclk_gone	alarm_dataclk_gone	clock_gone	alarm_from_iotesta	reserved	reserved		
config6	0x06	0x0000	tempdata (7:0)								fuse_cntl (5:0)						reserved	
config7	0x07	0xFFFF	alarms_mask (15:0)															
config8	0x08	0x6000	reserved		qmc_offseta (12:0)													
config9	0x09	0x8000	fifo_offset (2:0)		reserved													
config10	0x0A	0xF080	coarse_dac (3:0)				fuse_sleep	reserved	reserved	tsense_sleep	clkrecv_ena	sleepa	sleepb	reserved				reserved
config11	0x0B	0x1111	reserved				reserved				reserved				reservedspares_west (3:0)			
config12	0x0C	0x3A7A	reserved		iotest_pattern0 (13:0)													
config13	0x0D	0x36B6	reserved		iotest_pattern1 (13:0)													
config14	0x0E	0x2AEA	reserved		iotest_pattern2 (13:0)													
config15	0x0F	0x0545	reserved		iotest_pattern3 (13:0)													
config16	0x10	0x0585	reserved		iotest_pattern4 (13:0)													
config17	0x11	0x0949	reserved		iotest_pattern5 (13:0)													
config18	0x12	0x1515	reserved		iotest_pattern6 (13:0)													
config19	0x13	0x3ABA	reserved		iotest_pattern7 (13:0)													
config20	0x14	0x0000	sifdac_ena	reserved	sifdac (13:0)													
config21	0x15	0xFFFF	sleepcntl (15:0)															
config22	0x16	0x0000	fa002_data(15:0)															
config23	0x17	0x0000	fa002_data(31:16)															
config24	0x18	0x0000	fa002_data(47:32)															
config25	0x19	0x0000	fa002_data(63:48)															
config127	0x7F	0x0044	reserved		reserved		reserved		reserved		reserved	titest_voh	titest_vol	vendorid (1:0)		versionid (2:0)		

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7.6.1 Register Name: config0 – Address: 0x00, Default: 0x4FC

Table 7. Register Name: config0 – Address: 0x00, Default: 0x4FC

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
config0	0x00	15	qmc_offset_ena	Enable the offset function when asserted.	0
		14	dual_ena	Utilizes both DACs when asserted.	0 FUSE controlled
		13:12	chipwidth	Programmable bits for setting the input interface width. 00: all 14 bits are used 01: upper 12 bits are used 10: upper 10 bits are used 11: upper 10 bits are used	00
		11	rev	Reverses the input bits. When using the 7bit interface, this reverse each 7-bit input, however when using the 14-bit interface, all 14-bits are reversed as one word.	0
		10	twos	When asserted, this bit tells the chip to presume 2's complement data is arriving at the input. Otherwise offset binary is presumed.	1
		9	sif4_ena	When asserted the SIF interface becomes a 4 pin interface. This bit has a lower priority than the **dieid_ena** bit.	0
		8	reserved	reserved	0
		7	fifo_ena	When asserted, the FIFO is absorbing the difference between INPUT clock and DAC clock. If it is not asserted then the FIFO buffering is bypassed but the reversing of bits and handling of offset binary input is still available. **NOTE: When the FIFO is bypassed, the DACCCLK and DATACLK must be aligned or there may be timing errors; not recommended for actual application use.**	1
		6	alarm_out_ena	When asserted the pin alarm becomes an output instead of a tri-stated pin.	1
		5	alarm_out_pol	This bit changes the polarity of the ALARM signal. (0=negative logic, 1=positive logic)	1
		4	alignrx_ena	When asserted the ALIGN pin receiver is powered up. **NOTE: It is recommended to clear this bit when ALIGNP/N are not used (dual bus mode, and SYNC ONLY and SIF_SYNC modes in single bus mode).**	1
		3	lvdssyncrx_ena	When asserted the SYNC pin receiver is powered up. **NOTE: It is recommended to clear this bit when SYNCP/N are not used (dual bus mode, and SIF_SYNC mode in single bus mode.)**	1
		2	lvdsdataclk_ena	When asserted the DATACLK pin receiver is powered up.	1
		1	reserved	reserved	0
		0	synconly_ena	When asserted, the chip is put into the SYNC ONLY mode where the SYNC pin is used as the sync input for both the front and back of the FIFO.	0

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7.6.2 Register Name: config1 – Address: 0x01, Default: 0x600E

Table 8. Register Name: config1 – Address: 0x01, Default: 0x600E

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
config1	0x01	15	iotest_ena	Turns on the io-testing circuitry when asserted. This is the circuitry that will compare an 8 sample input pattern to SIF programmed registers to make sure the data coming into the chip meets setup and hold requirements. If this bit is a 0, then the clock to this circuitry is turned off for power savings. **NOTE: Sample 0 should be aligned with the rising edge of SYNC.**	0
		14	reserved	reserved	1
		13	fullwordinterface_ena	When asserted, the input interface is changed to use the full 14-bits for each word, instead of dual 8-bit buses for two half words. **Note: fixed to 1 for the DAC3151 and DAC3161.**	1
		12	64cnt_ena	This bit enables the resetting of the alarms after 64 good samples with the goal of removing unnecessary errors. For instance on a lab board, when checking the setup/hold through IO TEST, there may initially be errors, but once the test is up and running everything works. Setting this bit removes the need for a SIF write to clear the alarm register.	0
		11	dacclkgone_ena	This bit allows the DACCLK gone signal from the clock monitor to be used to shut the output off.	0
		10	dataclkgone_ena	This bit allows the DATACLK gone signal from the clock monitor to be used to shut the output off.	0
		9	collision_ena	This bit allows the collision alarm from the FIFO to shut the output off	0
		8	reserved	reserved.	0
		7	daca_compliment	When asserted, the output to the DACA is complimented. This setting allows the user of the chip to effectively change the + and – designations of the DAC output pins.	0
		6	reserved	reserved	0
		5	sif_sync	This bit is the SIF_SYNC signal. Whatever is programmed into this bit is used as the chip sync when SIF_SYNC mode is enabled. Design is sensitive to rising edges, so programming from 0 → 1 is when the sync pulse is generated. 1 → 0 has no effect.	0
		4	sif_sync_ena	When asserted, enable SIF_SYNC mode.	0
		3	alarm_2away_ena	When asserted, alarms from the FIFO that represent the pointers being 2 away are enabled	1
		2	alarm_1away_ena	When asserted, alarms from the FIFO that represent the pointers being 1 away are enabled	1
		1	alarm_collision_ena	When asserted, the collision of FIFO pointers causes an alarm to be generated	1
		0	reserved	reserved	0

7.6.3 Register Name: config2 – Address: 0x02, Default: 0x3FFF

Table 9. Register Name: config2 – Address: 0x02, Default: 0x3FFF

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
config2	0x02	15	reserved	reserved.	0
		14	reserved	reserved.	0
		13:0	lvdsdata_ena	These 14 bits are individual enables for the 14 input pin receivers. **Note: for the DAC3171 7-bit input interface mode, turn off bits(6:0).**	0x3FFF

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7.6.4 Register Name: config3 – Address: 0x03, Default: 0x0000

Table 10. Register Name: config3 – Address: 0x03, Default: 0x0000

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
config3	0x03	15:13	datadlya	Controls the delay of the D[13:7]P/N inputs through the LVDS receivers for single bus mode; controls the delay of the DA[6:0]P/N inputs through the LVDS receivers for dual bus mode (only applicable to DAC3171). 0= no additional delay and each LSB adds a nominal 80ps.	000
		12:10	clkdlya	Controls the delay of the SYNCP/N inputs through the LVDS receivers for single bus mode; controls the delay of the DA_CLKP/N inputs through the LVDS receivers for dual bus mode (only applicable to DAC3171). 0= no additional delay and each LSB adds a nominal 80ps.	000
		9:7	datadlyb	Controls the delay of the D[6:0]P/N inputs through the LVDS receivers for single bus mode; controls the delay of the DB[6:0]P/N inputs through the LVDS receivers for dual bus mode (only applicable to DAC3171).	000
		6:4	clkdlyb	Controls the delay of the DATACLKP/N inputs through the LVDS receivers for single bus mode; controls the delay of the DB_CLKP/N inputs through the LVDS receivers for dual bus mode (only applicable to DAC3171). 0= no additional delay and each LSB adds a nominal 80ps.	000
		3	extref_ ena	Enable external reference for the DAC when set.	0
		2:1	reserved	reserved	00
		0	dual_ena	When this bit is set, pins 6,7 become the DATACLK for the data into the FIFO while in 7-bit DDR mode for DAC3171. When this bit is not set, pins 24,25 become the DATACLK for the data into the FIFO. While in full-word interface mode, leave this bit at 0.	0

7.6.5 Register Name: config4 – Address: 0x04, Default: 0x0000

Table 11. Register Name: config4 – Address: 0x04, Default: 0x0000

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
config4 WRITE TO CLEAR/ No RESET value	0x04	15:14	reserved	reserved	00
		13:0	iotest_ results	The values of these bits tell which bit in the input word failed during the io-test pattern comparison.	0x0000

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7.6.6 Register Name: config5 – Address: 0x05, Default: 0x0000

Table 12. Register Name: config5 – Address: 0x05, Default: 0x0000

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
config5 WRITE TO CLEAR	0x05	15	alarm_from_ zerochka	When this bit is asserted the FIFOA write pointer has an all zeros pattern in it. Since this pointer is a shift register, all zeros will cause the input point to be stuck until the next sync. The result could be a repeated 8T pattern at the output if the mixer is off and no syncs occur. Check for this error will tell the user that another sync is necessary to restart the FIFO write pointer.	0
		14	reserved	reserved.	0
		13:11	alarms_from_ fifoa	These bits report the FIFO A pointer status. 000: All fine 001: Pointers are 2 away 01X: Pointers are 1 away 1XX: FIFO Pointer collision	000
		10:8	reserved	reserved	0
		7	alarm_dacclk_ gone	Bit gets asserted when the DACCLK has been stopped long for enough cycles to be caught. The number of cycles varies with interpolation.	0
		6	alarm_dataclk_ gone	Bit gets asserted when the DATACLK has been stopped long for enough cycles to be caught. The number of cycles varies with interpolation.	0
		5	clock_gone	This bit gets set when either alarm_dacclk_gone or alarm_dataclk_gone are asserted. It controls the output of the CDRV_SER block. When high, the CDRV_SER block will output 0x8000 for each output connected to a DAC. The bit must be written to ‘0’ for CDRV_SER outputs to resume normal operation.	0
		4	alarm_from_ iotesta	This is asserted when the input data pattern does not match the pattern in the iotest_pattern registers.	0
		3	reserved	reserved.	0
		2	reserved	reserved	0
		1	reserved	reserved	0
		0	reserved	reserved	0

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7.6.7 Register Name: config6 – Address: 0x06, Default: 0x0010(DAC3171); 0x0094(DAC3161); 0x0098(DAC3151)

Table 13. Register Name: config6 – Address: 0x06, Default: 0x0010(DAC3171); 0x0094(DAC3161); 0x0098(DAC3151)

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
config6 No RESET Value	0x06	15:8	tempdata	This the output from the chip temperature sensor. NOTE: when reading these bits the SIF interface must be exteremly slow, 1MHz range.	0x00
		7:2	fuse_cntl	These are the values of the blown fuses and are used to determine the available functionality in the chip. These bits are READ_ONLY, and allow the user to check what features have been disabled in the device. bit5 = 1: Forces Full Word interface bit4 = 0: reserved bit3 = 0: reserved bit2 = 1: Forces Single DAC mode. **Note: This does not force the channel B in sleep mode. In order to do so, user needs to program the sleepb SPI bit (config10, bit 5) to 1.** bit1:0 : Forces a different bits size: 00: 14 bit 01: 12 bit 10: 10 bit 11: 10 bit	0x10 for DAC3171; 0x94 for DAC3161; 0x98 for DAC3151; FUSE controlled
		1	reserved	reserved	0
		0	reserved	reserved	0

7.6.8 Register Name: config7 – Address: 0x07, Default: 0xFFFF

Table 14. Register Name: config7 – Address: 0x07, Default: 0xFFFF

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
config7	0x07	15:0	alarms_ mask	Each bit is used to mask an alarm. Assertion masks the alarm: bit15 = alarm_mask_zerochka bit14 = alarm_mask_zerochkb bit13 = alarm_mask_fifoa_collision bit12 = alarm_mask_fifoa_1away bit11 = alarm_mask_fifoa_2away bit10 = alarm_mask_fifob_collision bit9 = alarm_mask_fifob_1away bit8 = alarm_mask_fifob_2away bit7 = alarm_mask_dacclk_gone bit6 = alarm_mask_dataclk_gone bit5 = Masks the signal which turns off the DAC output when a clock or collision occurs. This bit has no effect on the PAD_ALARM output. bit4 = alarm_mask_iotesta bit3 = alarm_mask_iotestb bit2 = bit1 = bit0 =	0xFFFF

7.6.9 Register Name: config8 – Address: 0x08, Default: 0x6000

Table 15. Register Name: config8 – Address: 0x08, Default: 0x6000

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
config8	0x08	15:13	reserved	reserved	011
		12:0	qmc_ offseta	The DAC A offset correction. The offset is measured in DAC LSBs.	0x0000

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7.6.10 Register Name: config9 – Address: 0x09, Default: 0x8000

Table 16. Register Name: config9 – Address: 0x09, Default: 0x8000

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
config9 AUTO SYNC	0x09	15:13	fifo_ offset	This is the starting point for the READ_POINTER in the FIFO block. The READ_POINTER is set to this location when a sync occurs on the DACCLK side of the FIFO.	100
		12:0	reserved	reserved	0x0000

7.6.11 Register name: config10 – Address: 0x0A, Default: 0xF080

Table 17. Register Name: config10 – Address: 0x0A, Default: 0xF080

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
Config10	0x0A	15:12	coarse_ dac	Scales the output current is 16 equal steps. $\frac{VreflO}{Rbias} \times (mem_coarse_daca + 1)$	1111
		11	fuse_ sleep	Put the fuses to sleep when set high.	0
		10	reserved	reserved	0
		9	reserved	reserved	0
		8	tsense_ sleep	When asserted the temperature sensor is put to sleep.	0
		7	clkrecv_ ena	Turn on the DAC CLOCK receiver block when asserted.	1
		6	sleepa	When asserted DACA is put to sleep.	0
		5	sleepb	When asserted DACB is put to sleep. **Note: This bit needs to be programmed to 1 to save additional power.**	0
		4:0	reserved	reserved	00000

7.6.12 Register Name: config11 – Address: 0x0B, Default: 0x1111

Table 18. Register Name: config11 – Address: 0x0B, Default: 0x1111

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
config11	0x0B	15:12	reserved	reserved	0001
		11:8	reserved	reserved	0001
		7:4	reserved	reserved	0001
		3:0	reserved	reserved	0001

7.6.13 Register Name: config12 – Address: 0x0C, Default: 0x3A7A

Table 19. Register Name: config12 – Address: 0x0C, Default: 0x3A7A

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
config12	0x0C	15:14	reserved	reserved	00
		13:0	iotest_ pattern0	This is dataword0 in the IO test pattern. It is used with the seven other words to test the input data. (*** NOTE ***) This word should be aligned with the rising edge of SYNC when testing the IO interface.	0x3A7A

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7.6.14 Register Name: config13 – Address: 0x0D, Default: 0x36B6

Table 20. Register Name: config13 – Address: 0x0D, Default: 0x36B6

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
config13	0x0D	15:14	reserved	reserved	00
		13:0	iotest_ pattern1	This is dataword1 in the IO test pattern. It is used with the seven other words to test the input data.	0x36B6

7.6.15 Register Name: config14 – Address: 0x0E, Default: 0x2AEA

Table 21. Register name: config14 – Address: 0x0E, Default: 0x2AEA

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
config14	0x0E	15:14	reserved	reserved	00
		13:0	iotest_ pattern2	This is dataword2 in the IO test pattern. It is used with the seven other words to test the input data.	0x2AEA

7.6.16 Register name: config15 – Address: 0x0F, Default: 0x0545

Table 22. Register Name: config15 – Address: 0x0F, Default: 0x0545

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
config15	0x0F	15:14	reserved	reserved	00
		13:0	iotest_ pattern3	This is dataword3 in the IO test pattern. It is used with the seven other words to test the input data.	0x0545

7.6.17 Register Name: config16 – Address: 0x10, Default: 0x0585

Table 23. Register Name: config16 – Address: 0x10, Default: 0x0585

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
config16	0x10	15:14	reserved	reserved	00
		13:0	iotest_ pattern4	This is dataword4 in the IO test pattern. It is used with the seven other words to test the input data.	0x0585

7.6.18 Register Name: config17 – Address: 0x11, Default: 0x0949

Table 24. Register Name: config17 – Address: 0x11, Default: 0x0949

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
config17	0x11	15:14	reserved	reserved	00
		13:0	iotest_ pattern5	This is dataword5 in the IO test pattern. It is used with the seven other words to test the input data.	0x0949

7.6.19 Register Name: config18 – Address: 0x12, Default: 0x1515

Table 25. Register Name: config18 – Address: 0x12, Default: 0x1515

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
config18	0x12	15:14	reserved	reserved	00
		13:0	iotest_ pattern5	This is datawor6 in the IO test pattern. It is used with the seven other words to test the input data.	0x1515

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7.6.20 Register Name: config19 – Address: 0x13, Default: 0x3ABA

Table 26. Register Name: config19 – Address: 0x13, Default: 0x3ABA

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
config19	0x13	15:14	reserved	reserved	00
		13:0	iotest_ pattern7	This is dataword7 in the IO test pattern. It is used with the seven other words to test the input data.	0x3ABA

7.6.21 Register Name: config20– Address: 0x14, Default: 0x0000

Table 27. Register Name: config20– Address: 0x14, Default: 0x0000

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
config20	0x14	15	sifdac_ ena	When asserted the DAC output is set to the value in sifdac. This can be used for trim setting and other static tests.	0
		14	reserved	reserved	0
		13:0	sifdac	This is the value that is sent to the DACs when sifdac_ena is asserted.	0x0000

7.6.22 Register Name: config21– Address: 0x15, Default: 0xFFFF

Table 28. Register Name: config21– Address: 0x15, Default: 0xFFFF

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
config21	0x15	15:0	sleepcntl	This controls what blocks get sent a SLEEP signal when the PAD_SLEEP pin is asserted. Programming a '1' in a bit will pass the SLEEP signal to the appropriate block. bit15 = DAC A bit14 = DAC B bit13 = FUSE Sleep bit12 = Temperature Sensor bit11 = Clock Receiver bit10 = LVDS DATA Receivers bit9 = LVDS SYNC Receiver bit8 = PECL ALIGN Receiver bit7 = LVDS DATACLK Receiver bit6 = reserved bit5 = reserved bit4 = reserved bit3 = reserved bit2 = reserved bit1 = reserved bit0 = reserved	0xFFFF

7.6.23 Register Name: config22– Address: 0x16, Default: 0x0000

Table 29. Register Name: config22– Address: 0x16, Default: 0x0000

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
config22 READ ONLY	0x16	15:0	fa002_ data(15:0)	Lower 16 bits of the DIE ID word	

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7.6.24 Register Name: config23– Address: 0x17, Default: 0x0000

Table 30. Register Name: config23– Address: 0x17, Default: 0x0000

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
config23 READ ONLY	0x17	15:0	fa002_ data(31:16)	Lower middle 16 bits of the DIE ID word	

7.6.25 Register Name: config24– Address: 0x18, Default: 0x0000

Table 31. Register Name: config24– Address: 0x18, Default: 0x0000

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
config24 READ ONLY	0x18	15:0	fa002_ data(47:32)	Upper middle 16 bits of the DIE ID word	

7.6.26 Register Name: config25– Address: 0x19, Default: 0x0000

Table 32. Register Name: config25– Address: 0x19, Default: 0x0000

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
config25 READ ONLY	0x19	15:0	fa002_ data(63:48)	Upper 16 bits of the DIE ID word	

7.6.27 Register Name: config127– Address: 0x7F, Default: 0x0045

Table 33. Register Name: config127– Address: 0x7F, Default: 0x0045

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
config127 READ ONLY/No RESET Value	0x7F	15:14	reserved	reserved	00
		13:12	reserved	reserved	00
		11:10	reserved	reserved	00
		9:8	reserved	reserved	00
		7	reserved	reserved	0
		6	titest_voh	A fixed 1 that can be used to test the V_{OH} at the SIF output.	1
		5	titest_vol	A fixed 0 that can be used to test the V_{OL} at the SIF output.	0
		4:3	vendorid	Fixed at 01.	01
		2:0	versionid	Chip version	001

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DAC3171 is a single-channel, 14-bit, 500-MSPS DAC with a flexible input interface (full SDR 14-bit interface or DDR 7-bit interface). This device supports an independent input data clock and output DAC clock, and the FIFO can be used to absorb the timing difference of two clock domains. The DAC3171 has a wide use in many applications, such as real-IF transmitters for wireless infrastructure, arbitrary waveform generators, radar, cable head-end equipment, and more.

8.2 Typical Application

Figure 72 shows an example block diagram of the DAC31x1 used as a real IF transmitter to generate a modulated communication signal.

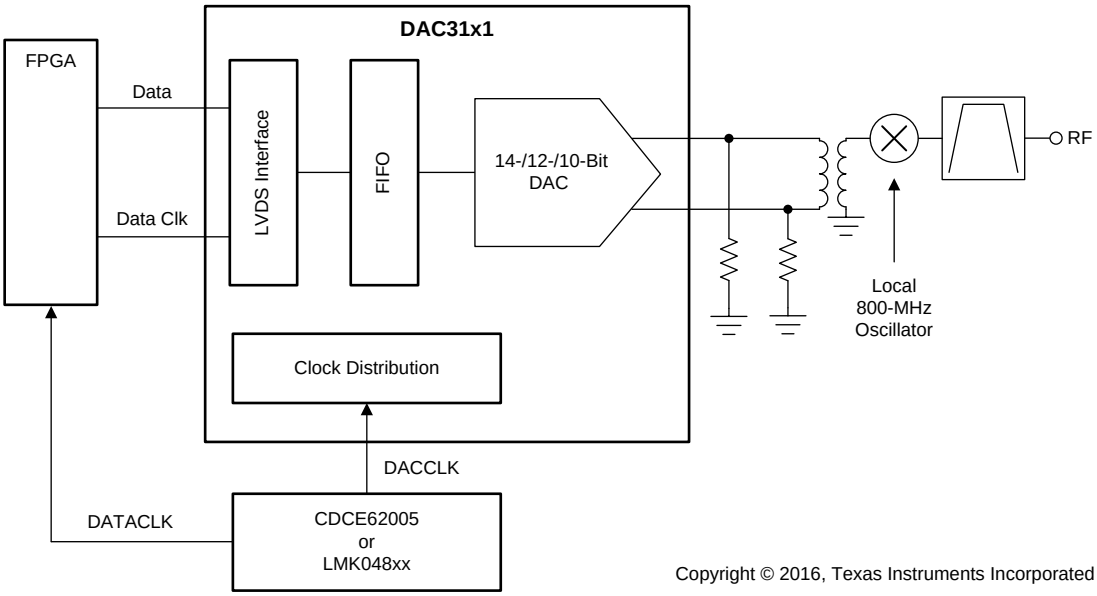


Figure 72. Real IF Transmitter

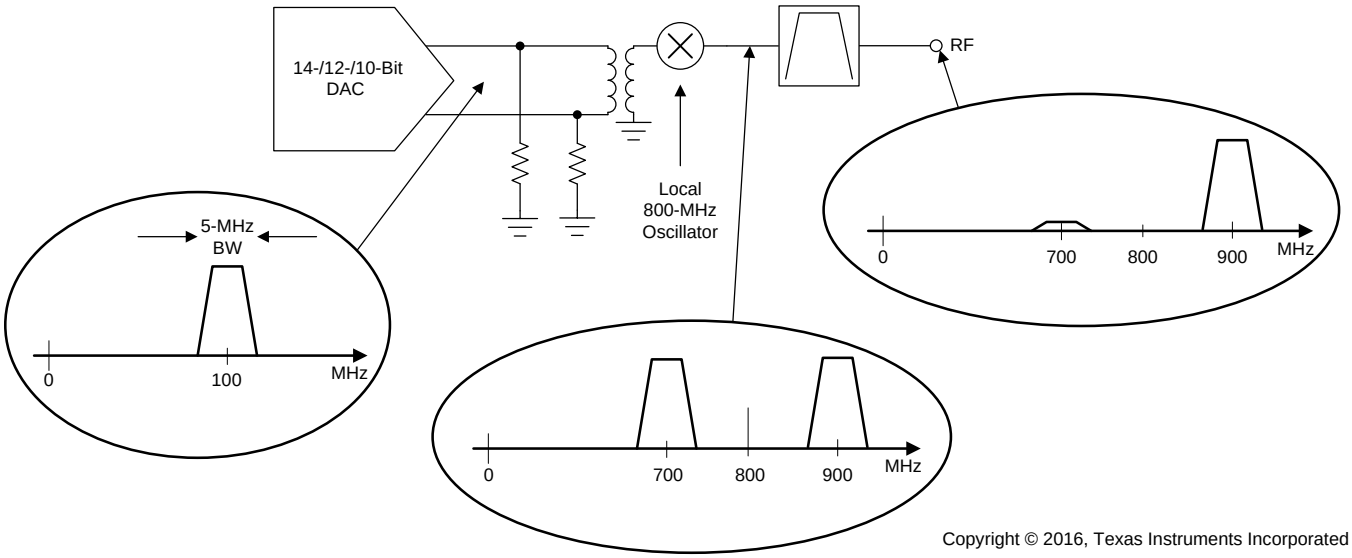
8.2.1 Design Requirements

A single-carrier WCDMA modulated waveform with a bandwidth of 5 MHz is to be created. The WCDMA signal is to be modulated up to a 900-MHz carrier. A real mixer will create two images of the signal about the carrier frequency and some bleedthrough of the local oscillator; therefore, a band-pass filter will be used to filter out the undesired image of the signal and the local oscillator.

Typical Application (continued)

8.2.2 Detailed Design Procedure

The data pattern file that represents the desired 5-MHz, single-carrier WCDMA signal is created with a pattern generation is clocked into the DAC31x1 by an FPGA as shown in the Figure 72. We choose to generate the data pattern file with the 5-MHz WCDMA signal centered at an intermediate frequency of 100 MHz and use a local oscillator of 800 MHz to upconvert the modulated signal to 900 MHz. The real mixer will create an image of the desired signal centered about 700 MHz, and there will also be local oscillator (LO) feedthrough observed at 800 MHz. A band-pass filter that follows the mixer is needed to remove the lower image of the signal and the local oscillator feedthrough, as shown in Figure 73.



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Figure 73. Signal Spectrum in a Real IF Transmitter

The choice of the intermediate frequency has an impact on the design of the 900-MHz band-pass filter. The band-pass filter is to pass the WCDMA signal image that is centered at 900 MHz, but provide significant attenuation of the local oscillator feedthrough and the signal image. The distance between the signal and the image is equal to twice the intermediate frequency. If the intermediate frequency is too low, the image gets too close to the signal, then a higher order band pass filter with steep roll-off is required. If the intermediate frequency is too high, the image would be further away from the signal, but the signal would be too far out towards the end of the Nyquist zone, and the SinX/X distortion would become an issue. Centering the DAC output signal at an intermediate frequency of 100 MHz is a good and balanced choice in this example, making the design of the band-pass filter reasonably easy.

The DAC31x1 does not have an interpolation option, so the data rate for the sample data will be the same rate as the sample rate to the DAC31x1. In this case, we choose a sample rate of 500 MSPS, the maximum sample rate for this device.

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Typical Application (continued)

8.2.3 Application Curve

The DAC output ACPR of a single-carrier, WCDMA modulated signal centered at an intermediate frequency of 100 MHz is shown in Figure 74.

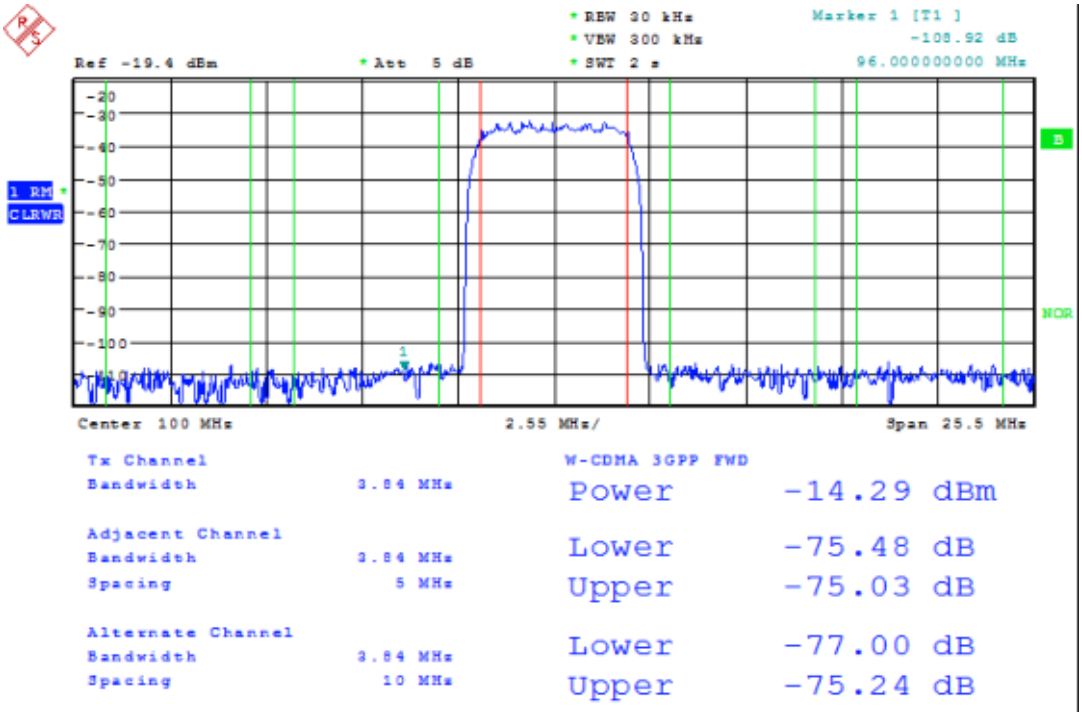


Figure 74. One Carrier WCDMA Signal ACPR at 100 MHz

9 Power Supply Recommendations

The DAC31x1 uses three different power supply voltages. Some of the DAC power supplies are noise sensitive. The table below is a summary of the various power supply of the DAC. See the evaluation module schematics for an example power supply implementation. Make certain to keep clean power-supply routing away from noisy digital supplies. Avoid placing digital supplies and clean supplies on adjacent board layers and use a ground layer between noisy and clean supplies if possible. All supplies pins should be decoupled as close to the pins as possible using small-value capacitors, with larger bulk capacitors placed further away.

Table 34. Power Supply Recommendations

POWER SUPPLY	VOLTAGE	NOISE SENSITIVE	RECOMMENDATION
IOVDD	1.8 V to 3.3 V	No	Digital supply, keep separated from noise sensitive supplies.
CLKVDD18	1.8 V (f_{DAC} ≤ 500 MSPS) 2.1 V	Yes	Provide clean voltage, avoid spurious noise
DIGVDD18	1.8 V (f_{DAC} ≤ 500 MSPS) 2.1 V	No	Digital supply, keep separated from noise sensitive supplies.
VDDA18	1.8 V (f_{DAC} ≤ 500 MSPS) 2.1 V	Yes	Provide clean voltage, avoid spurious noise
VDDA33	3.3 V	Yes	Provide clean voltage, avoid spurious noise
VFUSE	1.8 V (f_{DAC} ≤ 500 MSPS) 2.1 V	No	Digital supply, connect to DIGVDD18

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10 Layout

10.1 Layout Guidelines

- Place DAC output termination resistors as close to the output pins as possible in order to provide a dc path to ground and set the source impedance.
- Route the LVDS data signals as impedance-controlled, tightly-coupled, matched-length differential traces.
- Maintain a solid ground plane under the LVDS signals without any ground plane splits.
- Place a thermal ground pad under the device with adequate number of vias to the ground planes of the board.

10.2 Layout Example

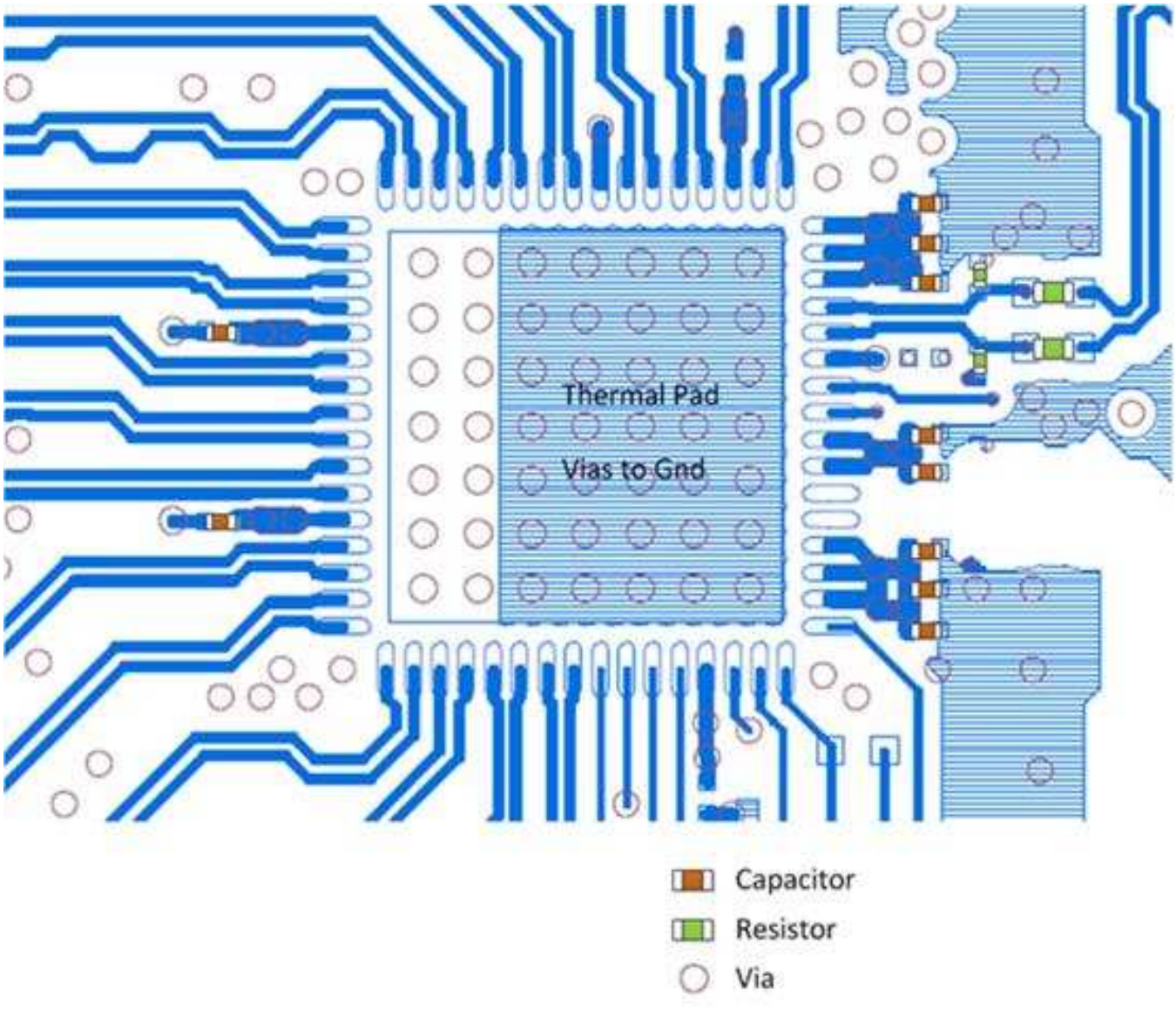


Figure 75. DAC31x1 Layout Example

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Definition of Specifications

Adjacent Carrier Leakage Ratio (ACLR): Defined as the ratio in decibles relative to the carrier (dBc) between the measured power within a channel and that of an adjacent channel.

Analog and Digital Power Supply Rejection Ratio (APSSR, DPSSR): Defined as the percentage error in the ratio of the delta IOUT and delta supply voltage normalized with respect to the ideal IOUT current.

Differential Nonlinearity (DNL): Defined as the variation in analog output associated with an ideal 1 LSB change in the digital input code.

Gain Drift: Defined as the maximum change in gain, in terms of ppm of full-scale range (FSR) per °C, from the value at ambient (25°C) to values over the full operating temperature range.

Gain Error: Defined as the percentage error (in FSR%) for the ratio between the measured full-scale output current and the ideal full-scale output current.

Integral Nonlinearity (INL): Defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero scale to full scale.

Intermodulation Distortion (IMD3): The two-tone IMD3 is defined as the ratio (in dBc) of the 3rd-order intermodulation distortion product to either fundamental output tone.

Offset Drift: Defined as the maximum change in DC offset, in terms of ppm of full-scale range (FSR) per °C, from the value at ambient (25°C) to values over the full operating temperature range.

Offset Error: Defined as the percentage error (in FSR%) for the ratio between the measured mid-scale output current and the ideal mid-scale output current.

Output Compliance Range: Defined as the minimum and maximum allowable voltage at the output of the current-output DAC. Exceeding this limit may result reduced reliability of the device or adversely affecting distortion performance.

Reference Voltage Drift: Defined as the maximum change of the reference voltage in ppm per degree Celsius from value at ambient (25°C) to values over the full operating temperature range.

Spurious Free Dynamic Range (SFDR): Defined as the difference (in dBc) between the peak amplitude of the output signal and the peak spurious signal.

Signal to Noise Ratio (SNR): Defined as the ratio of the RMS value of the fundamental output signal to the RMS sum of all other spectral components below the Nyquist frequency, including noise, but excluding the first six harmonics and dc.

11.2 Related Links

Table 35 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 35. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
DAC3151	Click here	Click here	Click here	Click here	Click here
DAC3161	Click here	Click here	Click here	Click here	Click here
DAC3171	Click here	Click here	Click here	Click here	Click here

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

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11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DAC3151IRGCR	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC3151I
DAC3151IRGCR.A	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC3151I
DAC3151IRGCT	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC3151I
DAC3151IRGCT.A	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC3151I
DAC3161IRGCR	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC3161I
DAC3161IRGCR.A	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC3161I
DAC3161IRGCT	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC3161I
DAC3161IRGCT.A	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC3161I
DAC3171IRGCR	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC3171I
DAC3171IRGCR.A	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC3171I
DAC3171IRGCT	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC3171I
DAC3171IRGCT.A	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC3171I

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

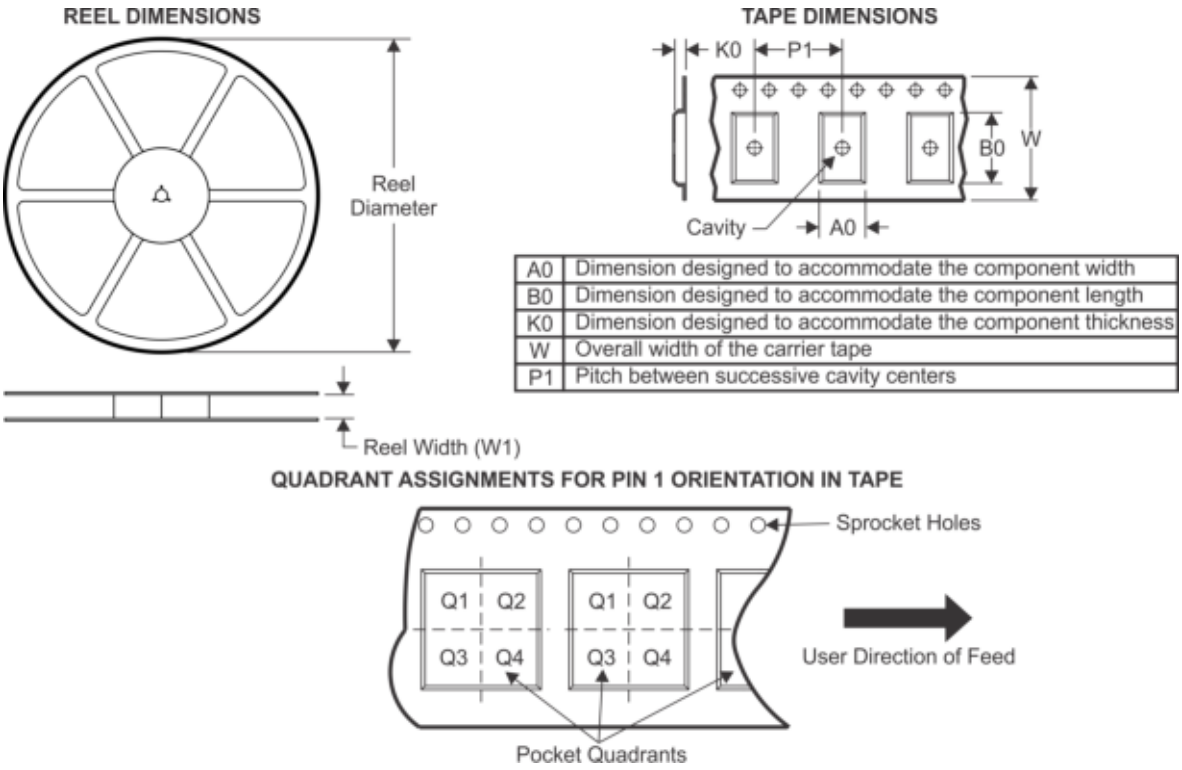
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

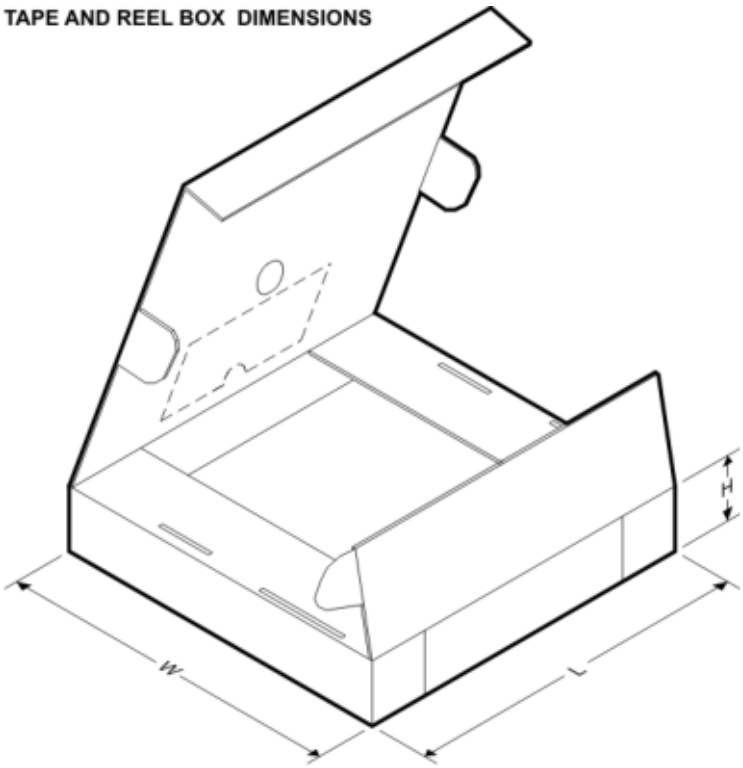


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC3151IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
DAC3151IRGCT	VQFN	RGC	64	250	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
DAC3161IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
DAC3161IRGCT	VQFN	RGC	64	250	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
DAC3171IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
DAC3171IRGCT	VQFN	RGC	64	250	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC3151IRGCR	VQFN	RGC	64	2000	336.6	336.6	28.6
DAC3151IRGCT	VQFN	RGC	64	250	367.0	367.0	38.0
DAC3161IRGCR	VQFN	RGC	64	2000	367.0	367.0	38.0
DAC3161IRGCT	VQFN	RGC	64	250	367.0	367.0	38.0
DAC3171IRGCR	VQFN	RGC	64	2000	336.6	336.6	28.6
DAC3171IRGCT	VQFN	RGC	64	250	367.0	367.0	38.0

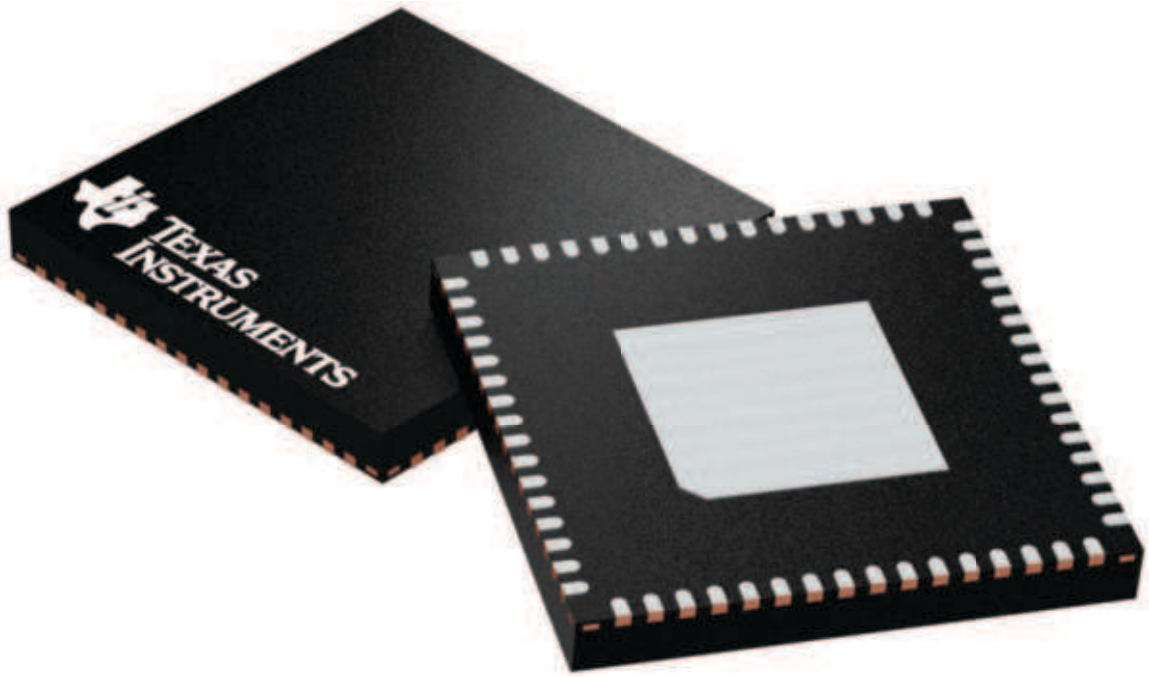
GENERIC PACKAGE VIEW

RGC 64

VQFN - 1 mm max height

9 x 9, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224597/A

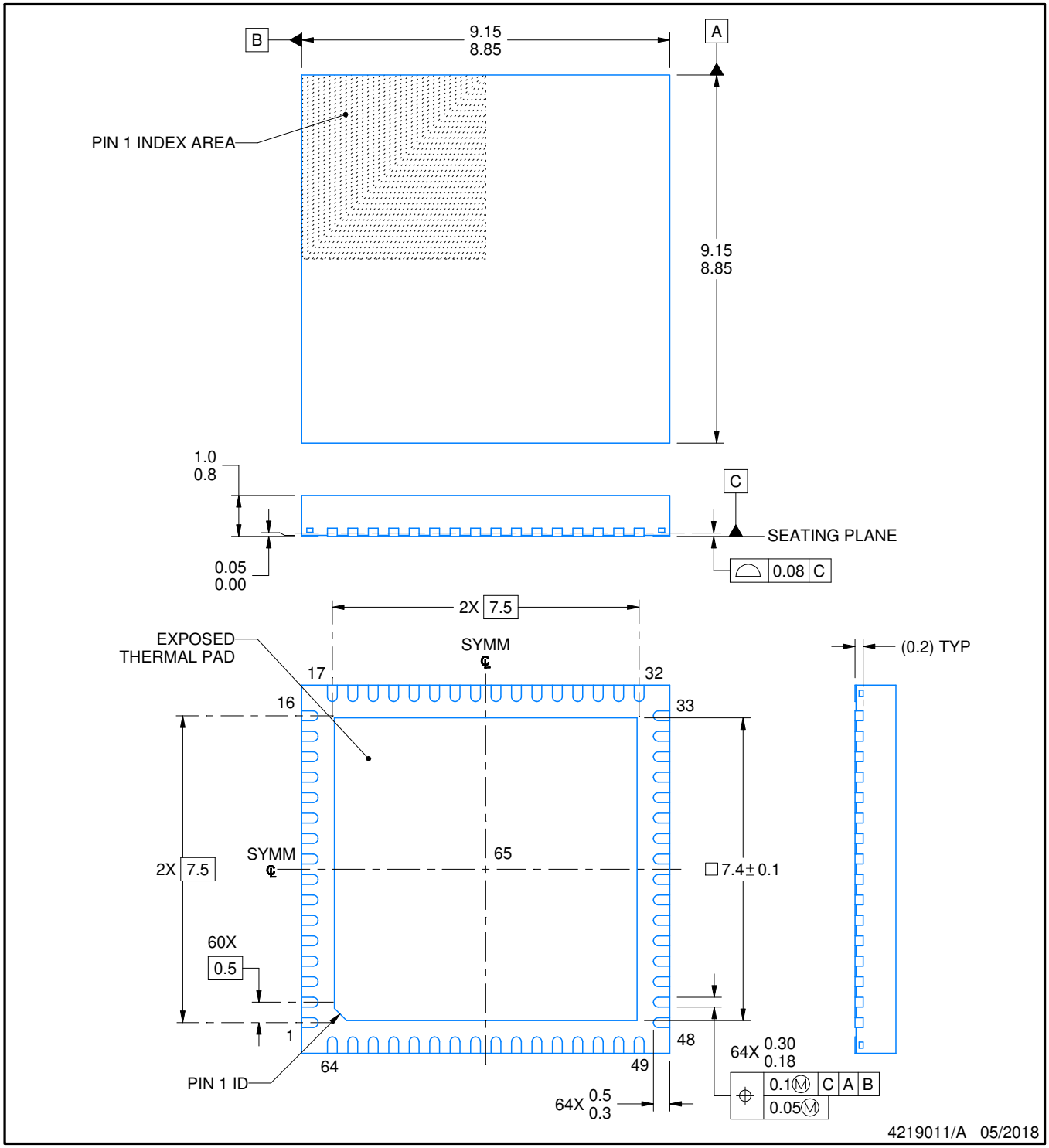
RGC0064H



PACKAGE OUTLINE

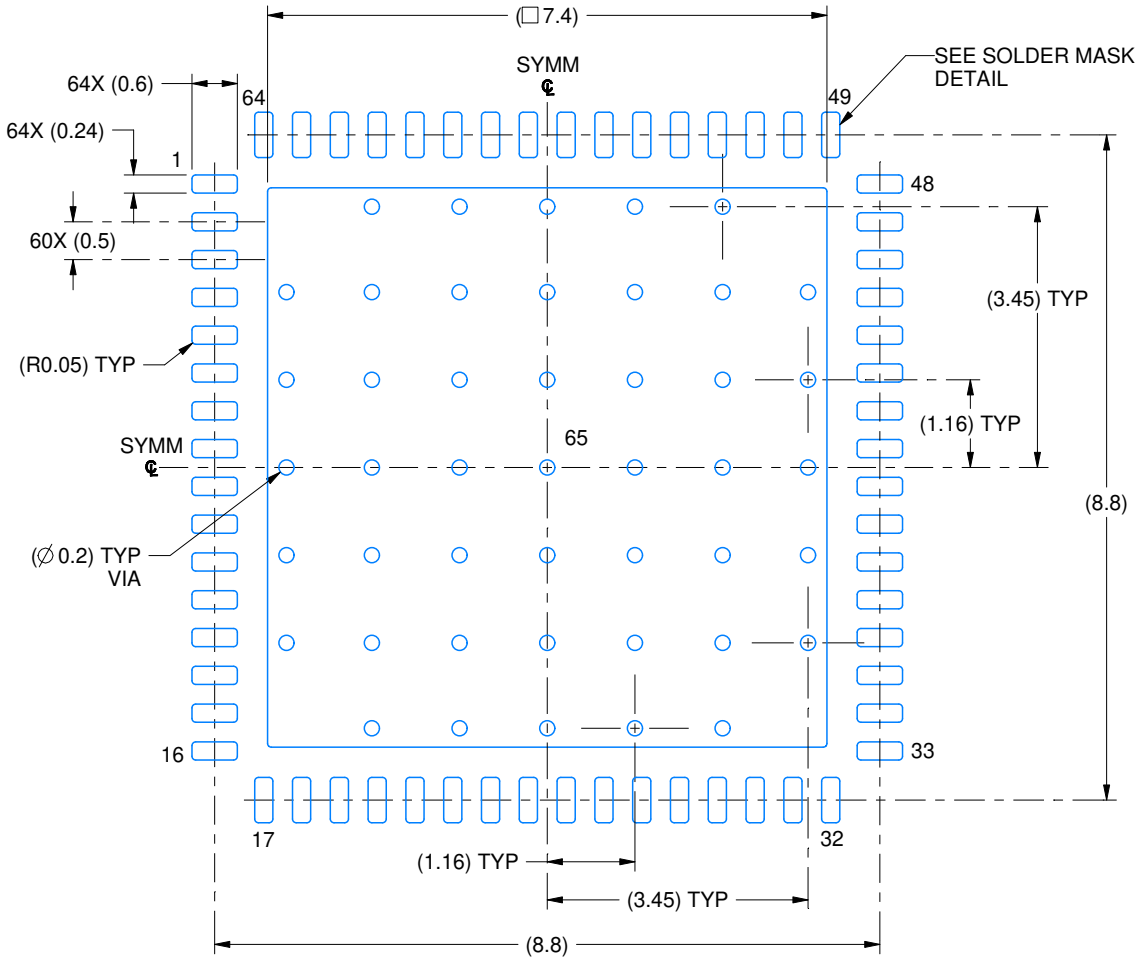
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

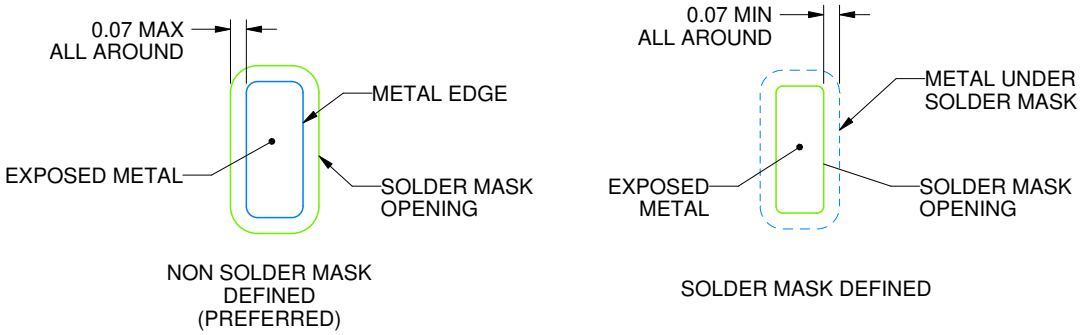


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

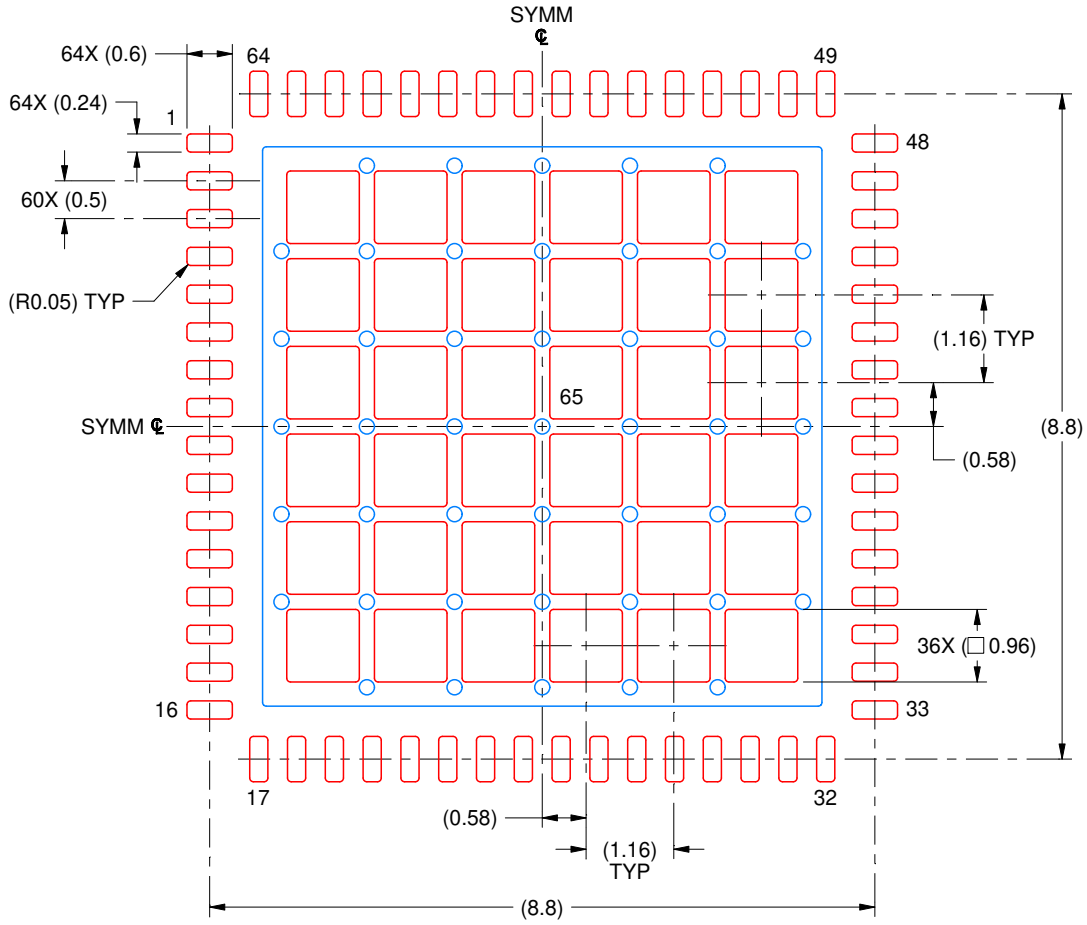


SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 65
61% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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