Burr-Brown Products
from Texas Instruments

DAC7714



Quad, Serial Input, 12-Bit, Voltage Output DIGITAL-TO-ANALOG CONVERTER

FEATURES

- LOW POWER: 250mW (max)
- UNIPOLAR OR BIPOLAR OPERATION
- SETTLING TIME: 10μs to 0.012%
- 12-BIT LINEARITY AND MONOTONICITY: –40°C to +85°C
- USER SELECTABLE RESET TO MID-SCALE OR ZERO-SCALE
- SECOND-SOURCE for DAC8420
- SMALL SO-16 PACKAGE

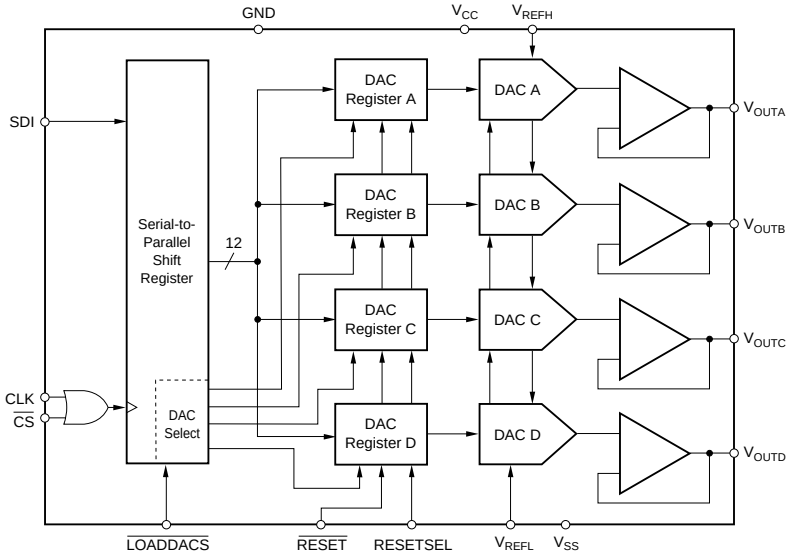
APPLICATIONS

- ATE PIN ELECTRONICS
- PROCESS CONTROL
- CLOSED-LOOP SERVO-CONTROL
- MOTOR CONTROL
- DATA ACQUISITION SYSTEMS

DESCRIPTION

The DAC7714 is a quad, serial input, 12-bit, voltage output Digital-to-Analog Converter (DAC) with guaranteed 12-bit monotonic performance over the –40°C to +85°C temperature range. An asynchronous reset clears all registers to either mid-scale (800_H) or zero-scale (000_H), selectable via the RESETSEL pin. The device can be powered from a single +15V supply or from dual +15V and –15V supplies.

Low power and small size makes the DAC7714 ideal for process control, data acquisition systems, and closed-loop servo-control. The device is available in a SO-16 package, and is guaranteed over the –40°C to +85°C temperature range.



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Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132
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SBAS119

SPECIFICATIONS (Dual Supply)

At T_A = –40°C to +85°C, V_{CC} = +15V, V_{SS} = –15V, V_{REFH} = +10V, V_{REFL} = –10V, unless otherwise noted.

PARAMETER	CONDITIONS	DAC7714U			DAC7714UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ACCURACY								
Linearity Error				±2			±1	LSB[1]
Linearity Matching[2]				±2			±1	LSB
Differential Linearity Error				±1			±1	LSB
Monotonicity	T_{MIN} to T_{MAX}	12			*			Bits
Zero-Scale Error	Code = 000_H			±2			*	LSB
Zero-Scale Drift			1			*		ppm/°C
Zero-Scale Matching[2]				±2			±1	LSB
Full-Scale Error	Code = FFF_H			±2			*	LSB
Full-Scale Matching[2]				±2			±1	LSB
Power Supply Sensitivity	At Full Scale		10			*		ppm/V
ANALOG OUTPUT								
Voltage Output[3]		V_{REFL}		V_{REFH}	*		*	V
Output Current		–5		+5	*		*	mA
Load Capacitance	No Oscillation		500			*		pF
Short-Circuit Current			±20			*		mA
Short-Circuit Duration	To V_{SS}, V_{CC}, or GND		Indefinite			*		
REFERENCE INPUT								
V_{REFH} Input Range		V_{REFL} +1.25		+10	*		*	V
V_{REFL} Input Range		–10		V_{REFH} – 1.25	*		*	V
Ref High Input Current		–0.5		3.0	*		*	mA
Ref Low Input Current		–3.5		0	*		*	mA
DYNAMIC PERFORMANCE								
Settling Time	To ±0.012%, 20V Output Step		8	10		*	*	µs
Channel-to-Channel Crosstalk	Full-Scale Step		0.25			*		LSB
Digital Feedthrough			2				*	nV-s
Output Noise Voltage	f = 10kHz		65			*		nV/√Hz
DIGITAL INPUT								
Logic Levels								
V_{IH}	$I_{IH} \leq \pm 10\mu A$	3.325			*			V
V_{IL}	$I_{IL} \leq \pm 10\mu A$			1.575			*	V
Data Format			Straight Binary			*		
POWER SUPPLY REQUIREMENTS								
V_{CC}		+14.25		+15.75	*		*	V
V_{SS}		–15.75		–14.25	*		*	V
I_{CC}			6	8.5		*	*	mA
I_{SS}		–8	–6		*	*		mA
Power Dissipation			180	250		*	*	mW
TEMPERATURE RANGE								
Specified Performance		–40		+85	*		*	°C

NOTES: (1) LSB means Least Significant Bit; if V_{REFH} equals +10V and V_{REFL} equals –10V, then one LSB equals 4.88mV. (2) All DAC outputs will match within the specified error band. (3) Ideal output voltage does not take into account zero or full-scale error.

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SPECIFICATIONS (Single Supply)

At T_A = –40°C to +85°C, V_{CC} = +15V, V_{SS} = GND, V_{REFH} = +10V, V_{REFL} = 0V, unless otherwise noted.

PARAMETER	CONDITIONS	DAC7714U			DAC7714UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ACCURACY								
Linearity Error[1]				±2			±1	LSB[2]
Linearity Matching[3]				±2			±1	LSB
Differential Linearity Error				±1			±1	LSB
Monotonicity	T_{MIN} to T_{MAX}	12			*			Bits
Zero-Scale Error	Code = 004_H			±4			*	LSB
Zero-Scale Drift			2			*		ppm/°C
Zero-Scale Matching[3]				±4			±2	LSB
Full-Scale Error	Code = FFF_H			±4			*	LSB
Full-Scale Matching[3]				±4			±2	LSB
Power Supply Sensitivity	At Full Scale		20			*		ppm/V
ANALOG OUTPUT								
Voltage Output[4]		V_{REFL}		V_{REFH}	*		*	V
Output Current		–5		+5	*			mA
Load Capacitance	No Oscillation		500			*		pF
Short-Circuit Current			±20			*		mA
Short-Circuit Duration	To V_{CC} or GND		Indefinite			*		
REFERENCE INPUT								
V_{REFH} Input Range		V_{REFL} +1.25		+10	*		*	V
V_{REFL} Input Range		0		V_{REFH} – 1.25	*		*	V
Ref High Input Current		–0.3		1.5	*		*	mA
Ref Low Input Current		–2.0		0	*		*	mA
DYNAMIC PERFORMANCE								
Settling Time[5]	To ±0.012%, 10V Output Step		8	10		*	*	µs
Channel-to-Channel Crosstalk			0.25			*		LSB
Digital Feedthrough			2				*	nV-s
Output Noise Voltage	f = 10kHz		65			*		nV/√Hz
DIGITAL INPUT/OUTPUT								
Logic Levels								
V_{IH}	$I_{IH} \leq \pm 10\mu A$	3.325			*			V
V_{IL}	$I_{IL} \leq \pm 10\mu A$			1.575			*	V
Data Format			Straight Binary			*		
POWER SUPPLY REQUIREMENTS								
V_{CC}		14.25		15.75	*		*	V
I_{CC}			3.0			*	*	mA
Power Dissipation			45			*		mW
TEMPERATURE RANGE								
Specified Performance		–40		+85	*		*	°C

NOTES: (1) If V_{SS} = 0V, specification applies at code 004_H and above. (2) LSB means Least Significant Bit; if V_{REFH} equals +10V and V_{REFL} equals 0V, then one LSB equals 2.44mV. (3) All DAC outputs will match within the specified error band. (4) Ideal output voltage does not take into account zero or full-scale error. (5) Full-scale positive 10V step and negative step from code FFF_H to 020_H.

ABSOLUTE MAXIMUM RATINGS[1]

V_{CC} to V_{SS}	–0.3V to +32V
V_{CC} to GND	–0.3V to +16V
V_{SS} to GND	+0.3V to –16V
$V_{REF}H$ to GND	–9V to +11V
$V_{REF}L$ to GND (V_{SS} = –15V)	–11V to +9V
$V_{REF}L$ to GND (V_{SS} = 0V)	–0.3V to +9V
V_{REFH} to V_{REFL}	–1V to +22V
Digital Input Voltage to GND	–0.3V to 5.8V
Digital Output Voltage to GND	–0.3V to 5.8V
Maximum Junction Temperature	+150°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

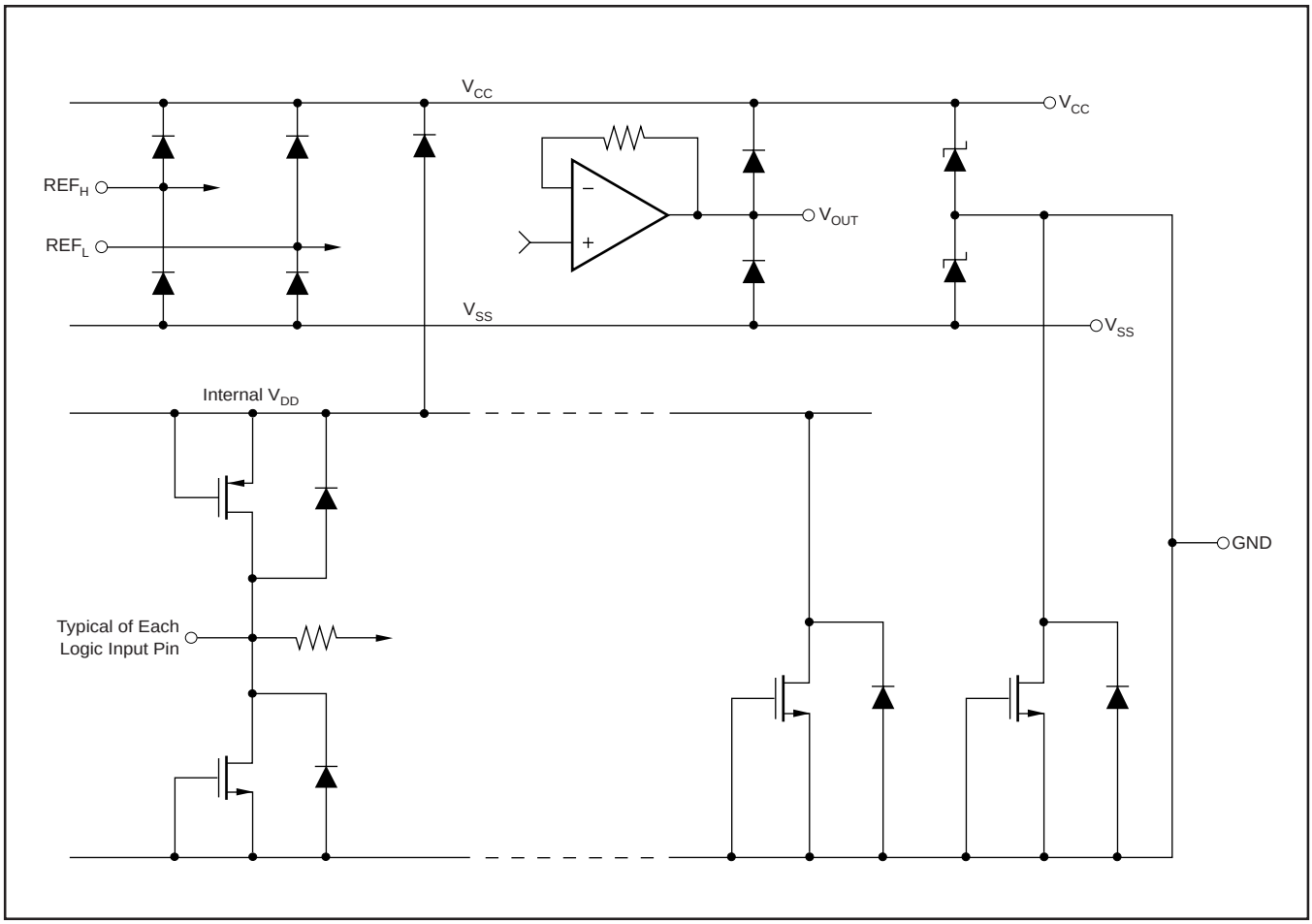
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

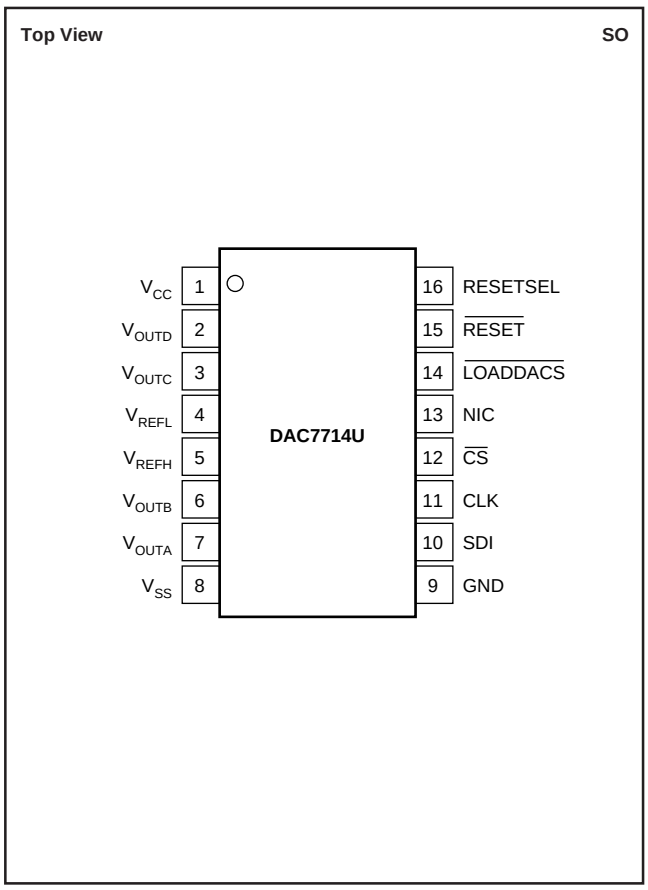
PRODUCT	MAXIMUM LINEARITY ERROR (LSB)	MAXIMUM DIFFERENTIAL LINEARITY (LSB)	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFICATION TEMPERATURE RANGE	ORDERING NUMBER[1]	TRANSPORT MEDIA
DAC7714U	±2	±1	SO-16	211	–40°C to +85°C	DAC7714U	Rails
"	"	"	"	"	"	DAC7714U/1K	Tape and Reel
DAC7714UB	±1	±1	SO-16	211	–40°C to +85°C	DAC7714UB	Rails
"	"	"	"	"	"	DAC7714UB/1K	Tape and Reel

NOTE: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /1K indicates 1000 devices per reel). Ordering 1000 pieces of "DAC7714UB/1K" will get a single 1000-piece Tape and Reel.

ESD PROTECTION CIRCUITS



PIN CONFIGURATION—U Package



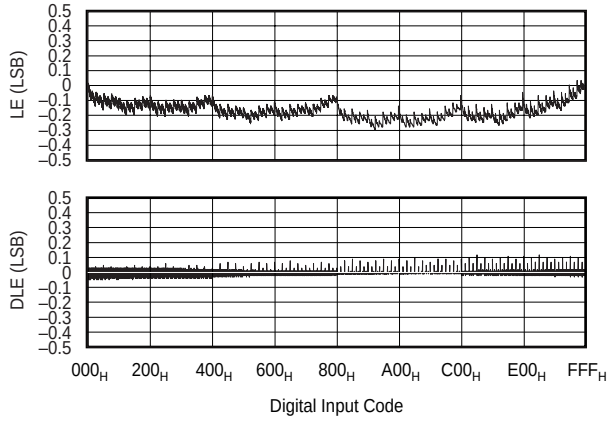
PIN DESCRIPTIONS—U Package

PIN	LABEL	DESCRIPTION
1	V_{CC}	Positive Analog Supply Voltage, +15V nominal.
2	V_{OUTD}	DAC D Voltage Output
3	V_{OUTC}	DAC C Voltage Output
4	V_{REFL}	Reference Input Voltage Low. Sets minimum output voltage for all DACs.
5	V_{REFH}	Reference Input Voltage High. Sets maximum output voltage for all DACs.
6	V_{OUTB}	DAC B Voltage Output
7	V_{OUTA}	DAC A Voltage Output
8	V_{SS}	Negative Analog Supply Voltage, 0V or –15V nominal.
9	GND	Ground
10	SDI	Serial Data Input
11	CLK	Serial Data Clock
12	$\overline{CS}$	Chip Select Input
13	NIC	Not Internally Connected
14	$\overline{LOADDACS}$	The selected DAC register becomes transparent when $\overline{LOADDACS}$ is LOW. It is in the latched state when $\overline{LOADDACS}$ is HIGH.
15	$\overline{RESET}$	Asynchronous Reset Input. Sets all DAC registers to either zero-scale (000_H) or mid-scale (800_H) when LOW. RESETSEL determines which code is active.
16	RESETSEL	When LOW, a LOW on $\overline{RESET}$ will cause all DAC registers to be set to code 000_H. When RESETSEL is HIGH, a LOW on $\overline{RESET}$ will set the registers to code 800_H.

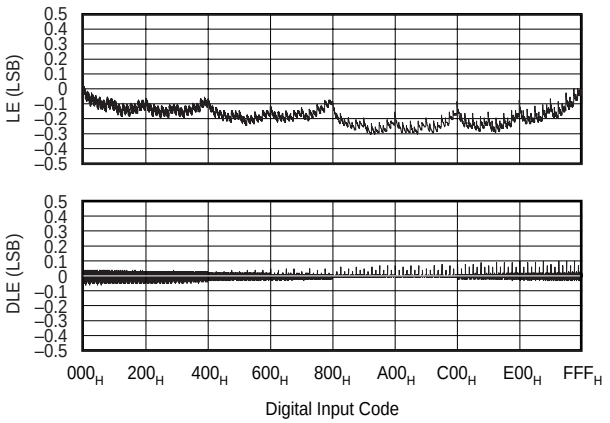
TYPICAL PERFORMANCE CURVES: V_{SS} = 0V

At T_A = +25°C, V_{CC} = +15V, V_{SS} = 0V, V_{REFH} = +10V, V_{REFL} = 0V, representative unit, unless otherwise specified.

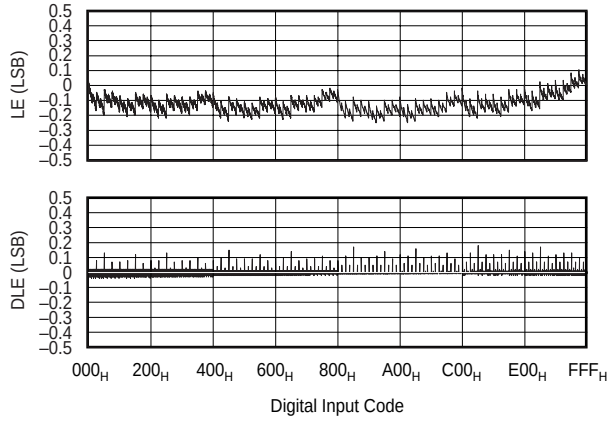
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
Single Channel 25°C
(Typical of Each Output Channel)



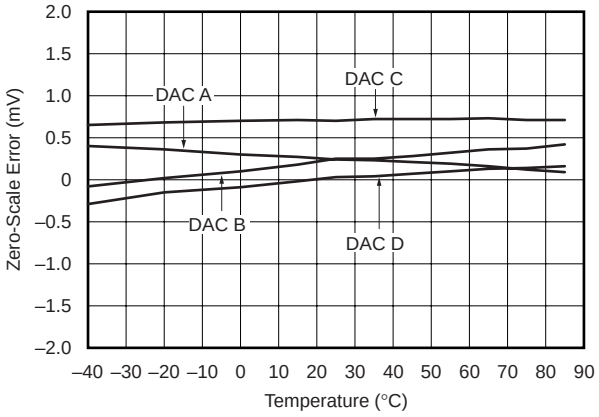
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
Single Channel 85°C
(Typical of Each Output Channel)



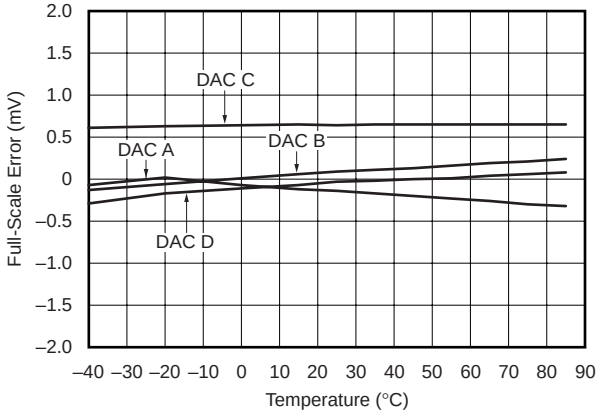
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
Single Channel –40°C
(Typical of Each Output Channel)



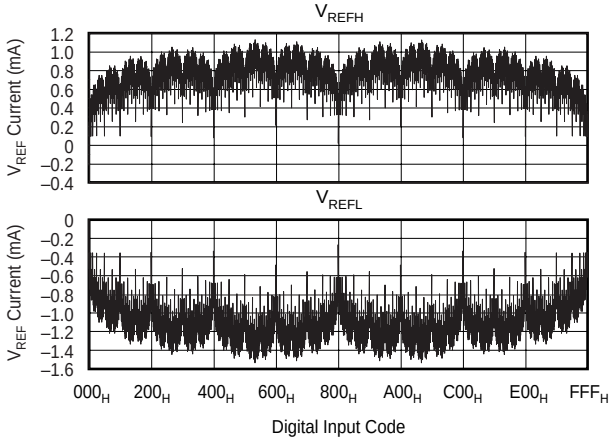
ZERO-SCALE ERROR vs TEMPERATURE
(Code 004_H)



FULL-SCALE ERROR vs TEMPERATURE
(Code FFF_H)



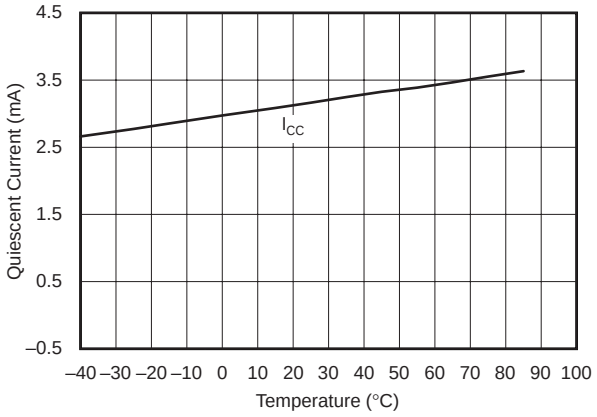
CURRENT vs CODE
All DACs Set to Indicated Code



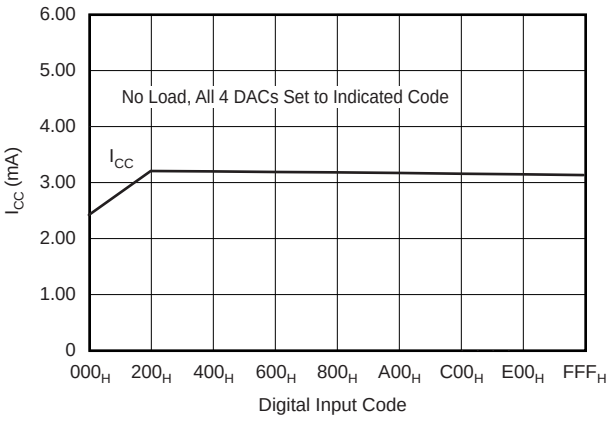
TYPICAL PERFORMANCE CURVES: V_{SS} = 0V (Cont.)

At T_A = +25°C, V_{CC} = +15V, V_{SS} = 0V, V_{REFH} = +10V, V_{REFL} = 0V, representative unit, unless otherwise specified.

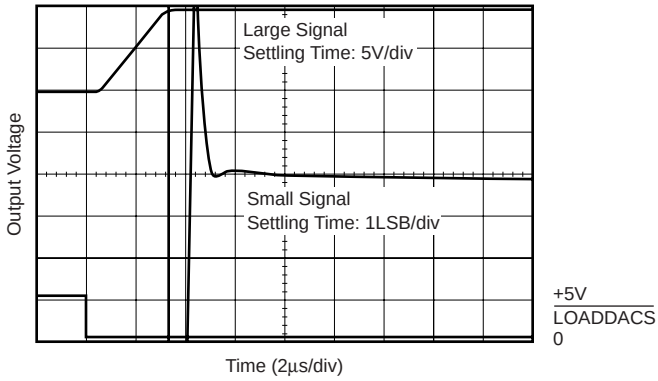
POWER SUPPLY CURRENT vs TEMPERATURE



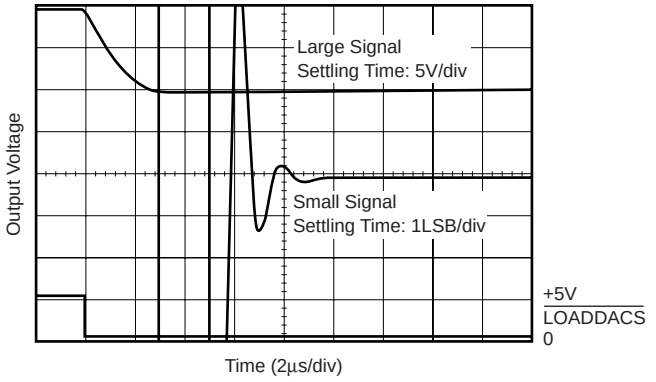
POSITIVE SUPPLY CURRENT
vs DIGITAL INPUT CODE



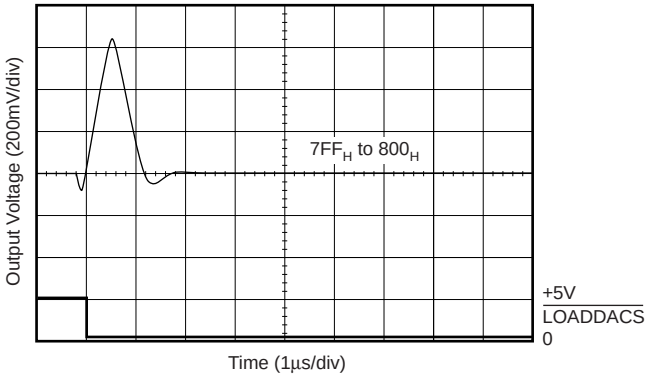
OUTPUT VOLTAGE vs SETTLING TIME
(0V to +10V)



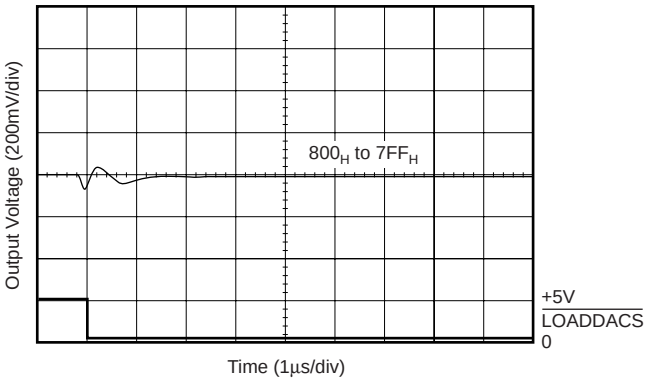
OUTPUT VOLTAGE vs SETTLING TIME
(+10V to Code 020_H)



OUTPUT VOLTAGE
MID-SCALE GLITCH PERFORMANCE



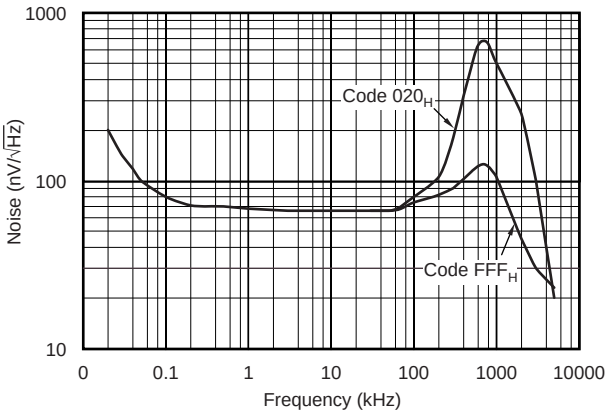
OUTPUT VOLTAGE
MID-SCALE GLITCH PERFORMANCE



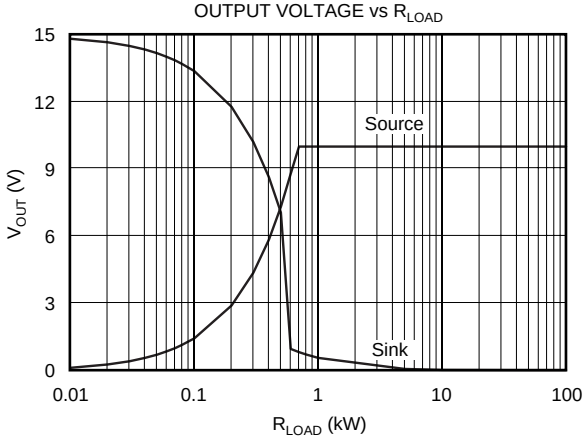
TYPICAL PERFORMANCE CURVES: V_{SS} = 0V (Cont.)

At T_A = +25°C, V_{CC} = +15V, V_{SS} = 0V, V_{REFH} = +10V, V_{REFL} = 0V, representative unit, unless otherwise specified.

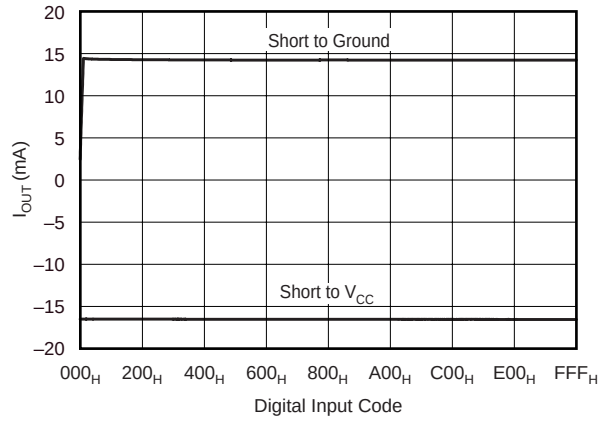
OUTPUT NOISE vs FREQUENCY



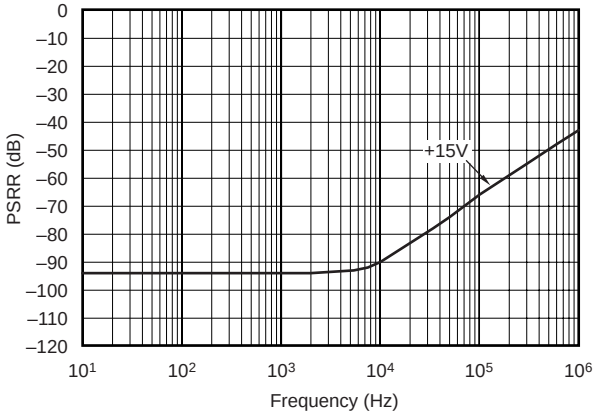
OUTPUT VOLTAGE vs R_{LOAD}



SINGLE SUPPLY CURRENT LIMIT vs INPUT CODE



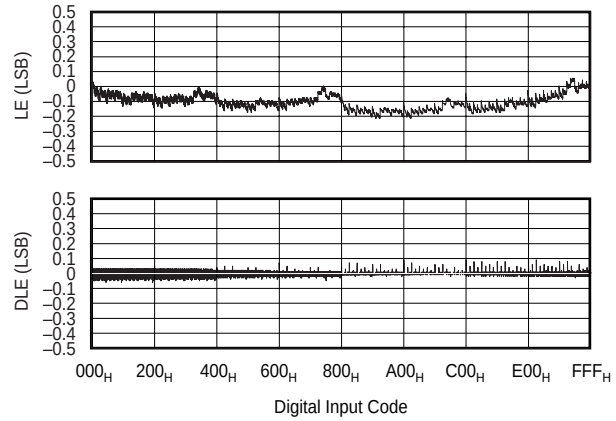
POWER SUPPLY REJECTION RATIO vs FREQUENCY



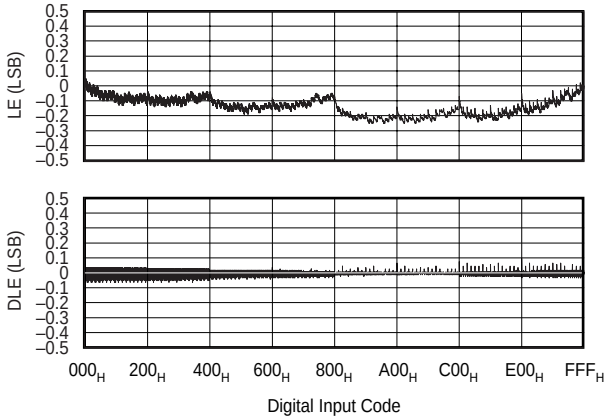
TYPICAL PERFORMANCE CURVES: V_{SS} = –15V

At T_A = +25°C, V_{CC} = +15V, V_{SS} = –15V, V_{REFH} = +10V, V_{REFL} = –10V, representative unit, unless otherwise specified.

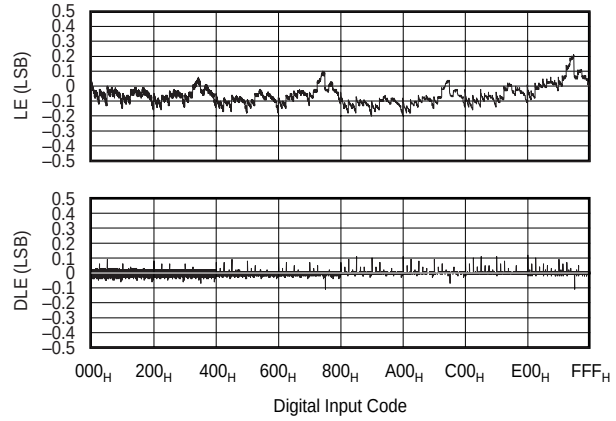
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
Single Channel 25°C
(Typical of Each Output Channel)



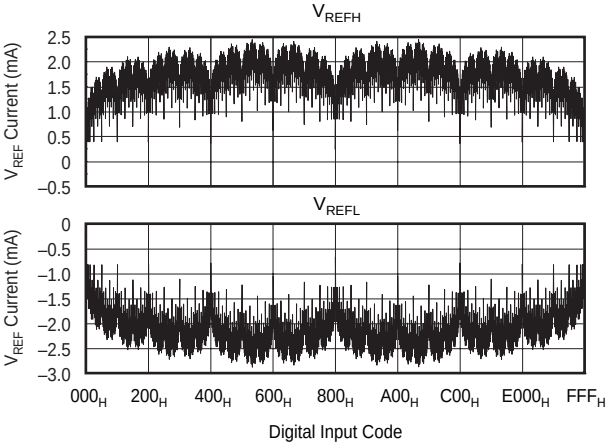
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
Single Channel 85°C
(Typical of Each Output Channel)



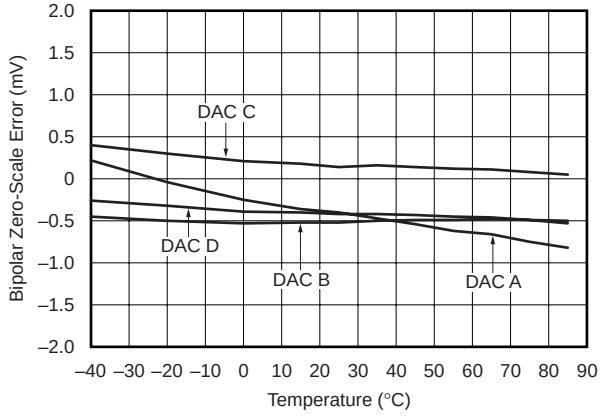
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
Single Channel –40°C
(Typical of Each Output Channel)



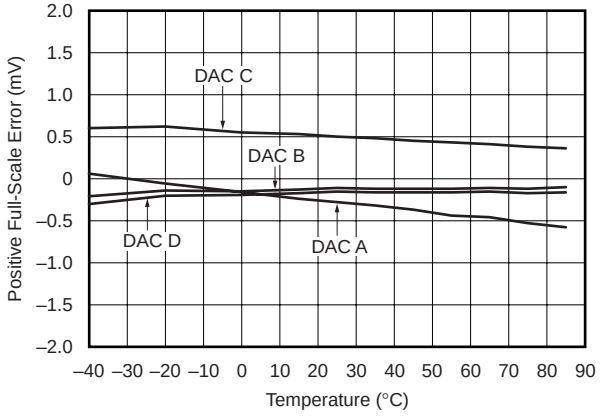
CURRENT vs CODE
All DACs Set to Indicated Code



BIPOLAR ZERO-SCALE ERROR vs TEMPERATURE
(Code 800_H)



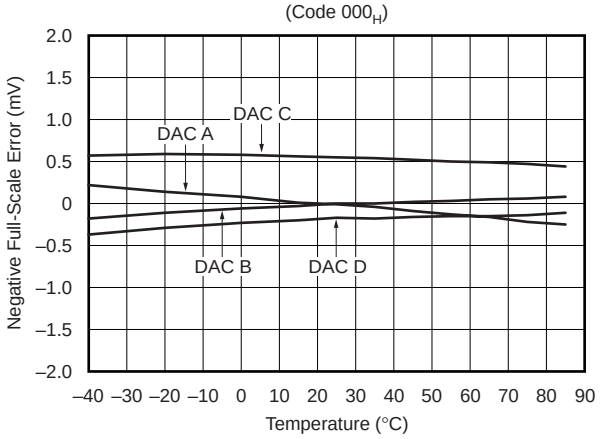
POSITIVE FULL-SCALE ERROR vs TEMPERATURE
(Code FFF_H)



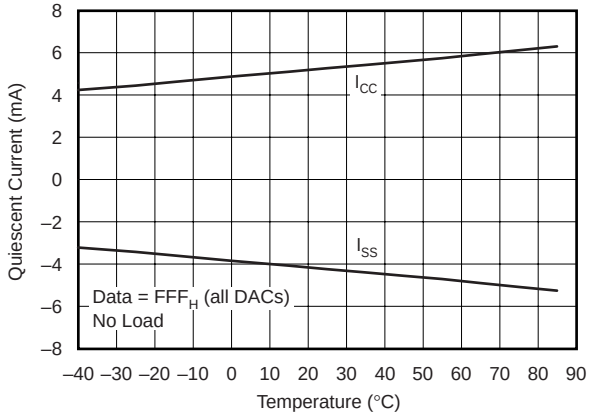
TYPICAL PERFORMANCE CURVES: V_{SS} = –15V (Cont.)

At T_A = +25°C, V_{CC} = +15V, V_{SS} = –15V, V_{REFH} = +10V, V_{REFL} = –10V, representative unit, unless otherwise specified.

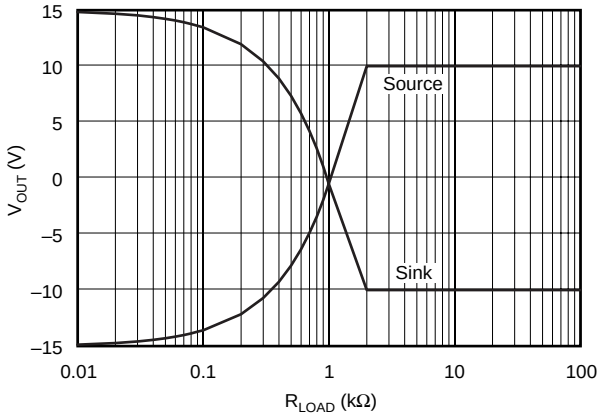
NEGATIVE FULL-SCALE ERROR vs TEMPERATURE
(Code 000_H)



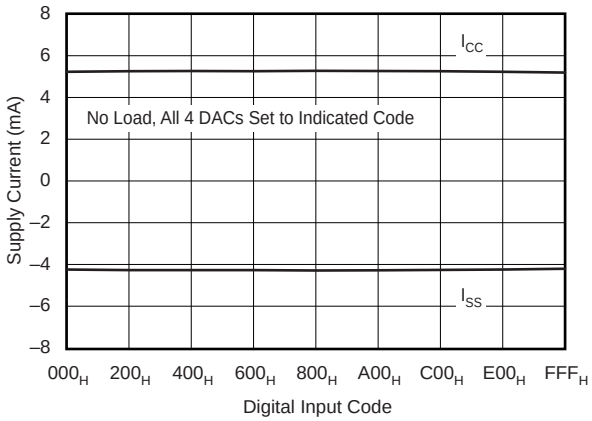
POWER SUPPLY CURRENT vs TEMPERATURE



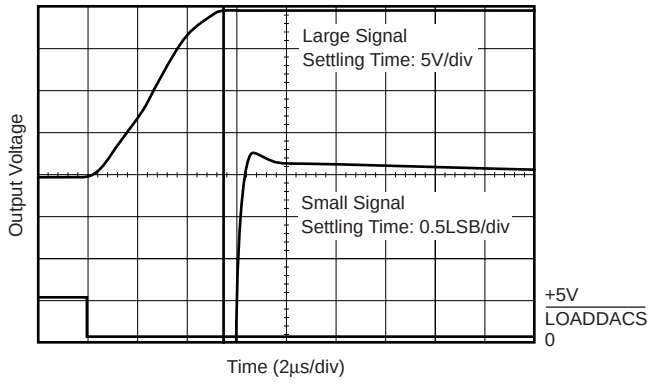
OUTPUT VOLTAGE vs R_{LOAD}



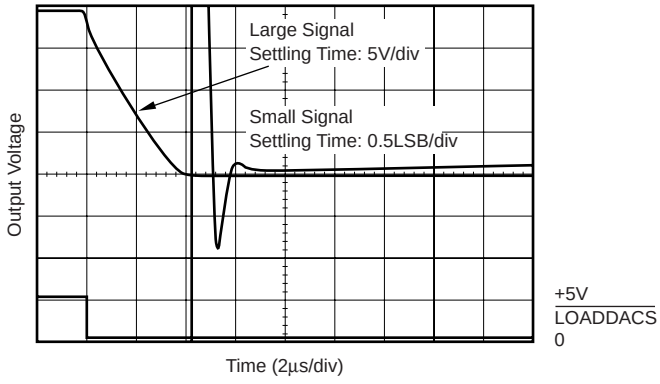
SUPPLY CURRENT vs CODE



OUTPUT VOLTAGE vs SETTLING TIME
(–10V to +10V)



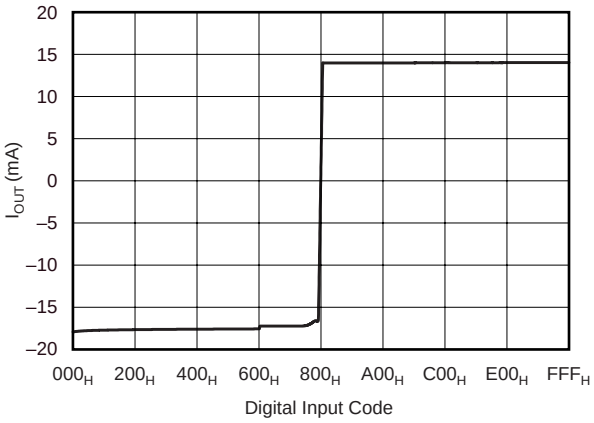
OUTPUT VOLTAGE vs SETTLING TIME
(+10V to –10V)



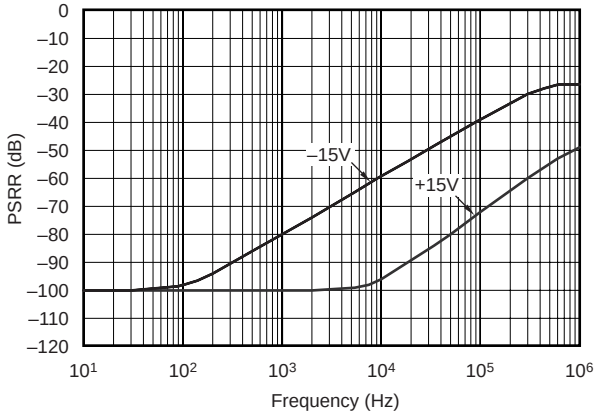
TYPICAL PERFORMANCE CURVES: V_{SS} = –15V (Cont.)

At T_A = +25°C, V_{CC} = +15V, V_{SS} = –15V, V_{REFH} = +10V, V_{REFL} = –10V, representative unit, unless otherwise specified.

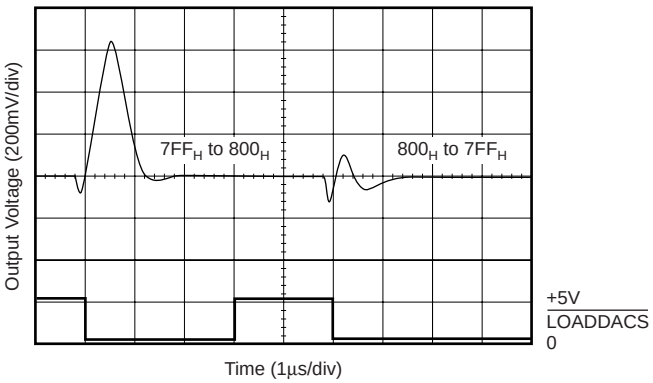
DUAL SUPPLY CURRENT LIMIT vs INPUT CODE
SHORT TO GROUND



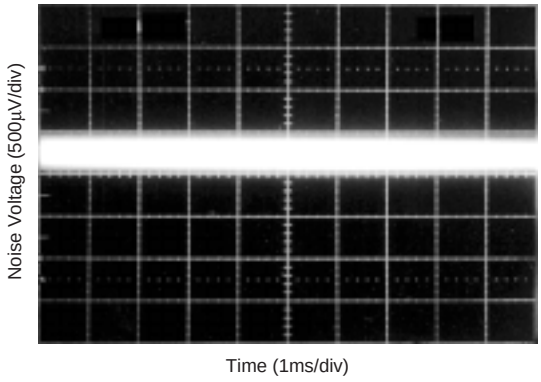
POWER SUPPLY REJECTION RATIO vs FREQUENCY



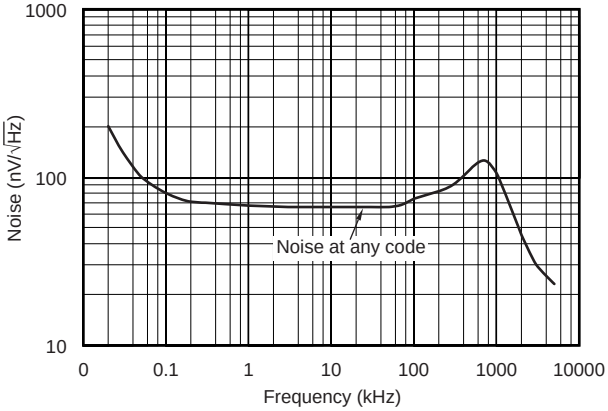
OUTPUT VOLTAGE
MID-SCALE GLITCH PERFORMANCE



BROADBAND NOISE



OUTPUT NOISE vs FREQUENCY



THEORY OF OPERATION

The DAC7714 is a quad, serial input, 12-bit, voltage output DAC. The architecture is a classic R-2R ladder configuration followed by an operational amplifier that serves as a buffer. Each DAC has its own R-2R ladder network and output op amp, but all share the reference voltage inputs, as shown in Figure 1. The minimum voltage output ("zero-scale") and maximum voltage output ("full-scale") are set by external voltage references (V_{REFL} and V_{REFH}, respectively). The digital input is a 16-bit serial word that contains the 12-bit DAC code and a 2-bit address code that selects one of the four DACs (the two remaining bits are unused). The converter can be powered from a single +15V supply or a dual ±15V supply. Each device offers a reset function which immediately sets all DAC output voltages and internal registers to either zero-scale (code 000_H) or mid-scale (code 800_H). The reset code is selected by the state of the RESETSEL pin (LOW = 000_H, HIGH = 800_H). Figures 2 and 3 show the basic operation of the DAC7714.

ANALOG OUTPUTS

When V_{SS} = –15V (dual supply operation), the output amplifier can swing to within 4V of the supply rails, over the –40°C to +85°C temperature range. With V_{SS} = 0V (single-supply operation), the output can swing to ground. Note that the settling time of the output op amp will be longer with voltages very near ground. Care must also be taken when measuring the zero-scale error when V_{SS} = 0V. If the output amplifier has a negative offset, the output voltage may not change for the first few digital input codes (000_H, 001_H, 002_H, etc.) since the output voltage cannot swing below ground.

At the negative offset limit of –4LSB (–9.76mV), for the single-supply case, the first specified output starts at code 004_H.

REFERENCE INPUTS

The reference inputs, V_{REFL} and V_{REFH}, can be any voltage between V_{SS} + 4V and V_{CC} – 4V provided that V_{REFH} is at least 1.25V greater than V_{REFL}. The minimum output of each D/A is equal to V_{REFL} – 1LSB plus a small offset voltage (essentially, the offset of the output op amp). The maximum output is equal to V_{REFH} plus a similar offset voltage. Note that V_{SS} (the negative power supply) must either be connected to ground or must be in the range of –14.75V to –15.75V. The voltage on V_{SS} sets several bias points within the converter. If V_{SS} is not in one of these two configurations, the bias values may be in error and proper operation of the device is not guaranteed.

The current into the reference inputs depends on the DAC output voltages and can vary from a few microamps to approximately 3mA. The reference input appears as a varying load to the reference. If the reference can sink or source the required current, a reference buffer is not required. See "Reference Current vs Code" in the Typical Performance Curves.

The analog supplies must come up before the reference power supplies, if they are separate. If the power supplies for the references come up first, then the V_{CC} and V_{SS} supplies will be powered from the reference via the ESD protection diodes (see page 4).

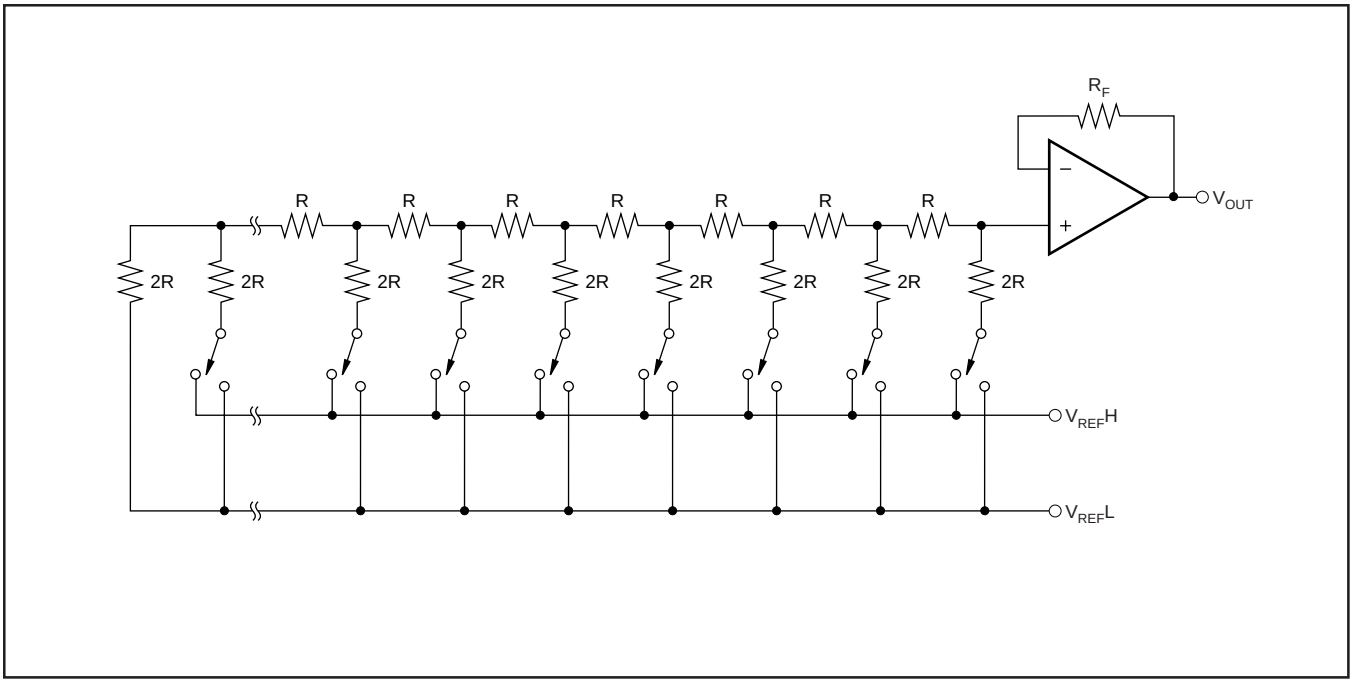


FIGURE 1. DAC7714 Architecture.

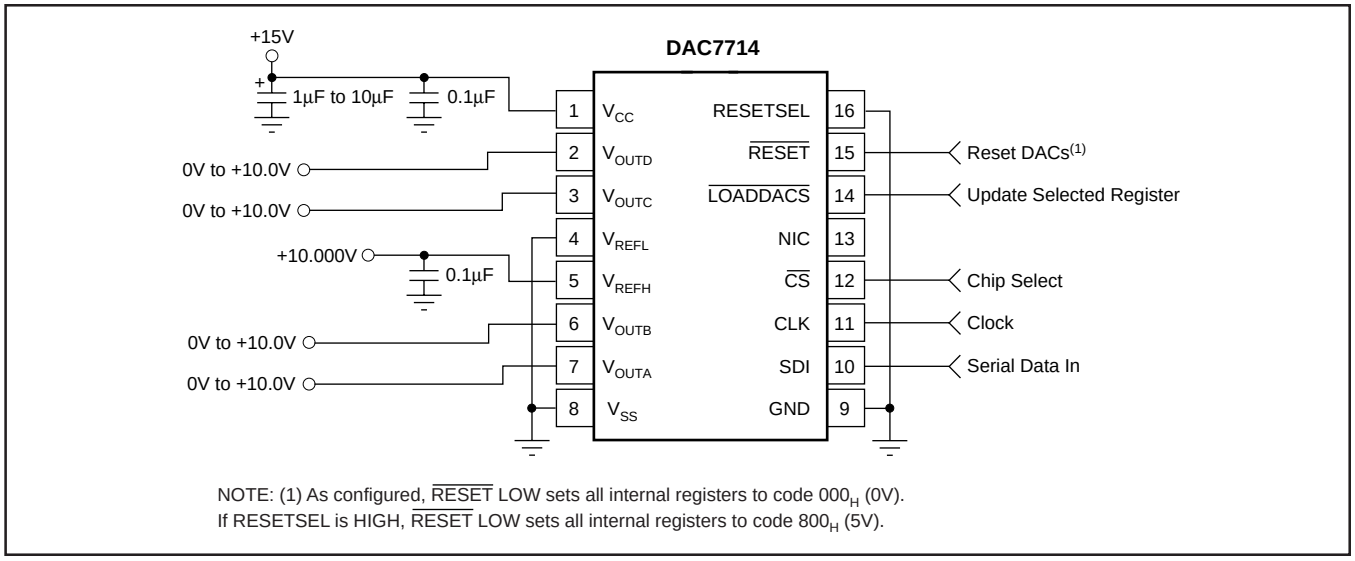


FIGURE 2. Basic Single-Supply Operation of the DAC7714.

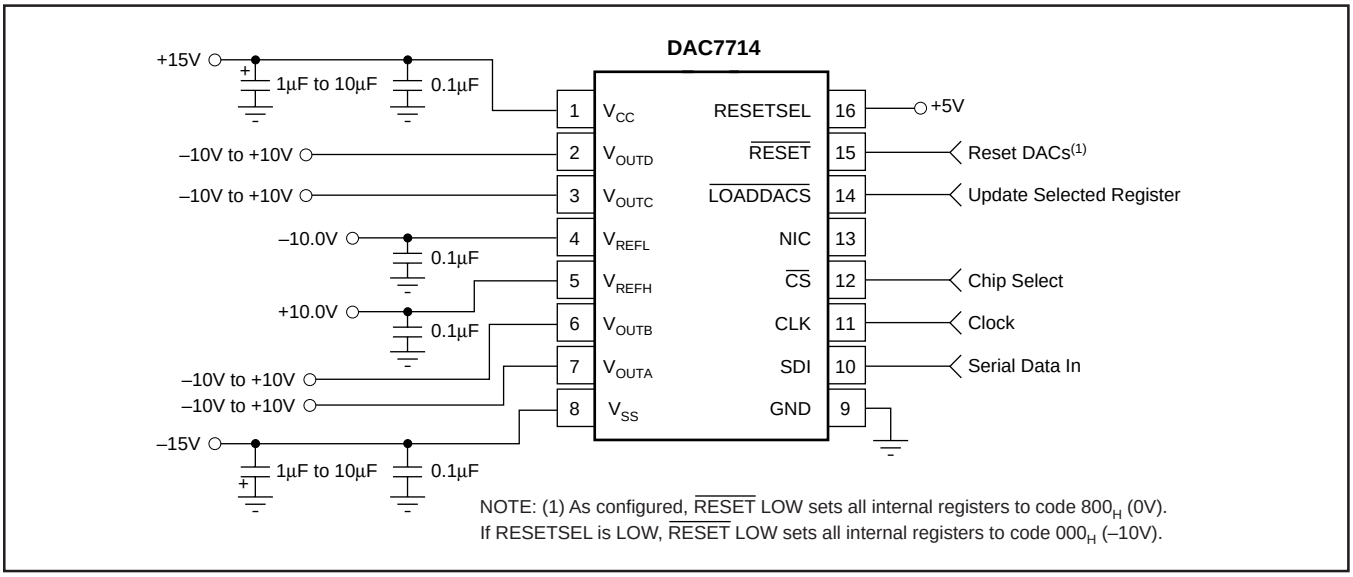


FIGURE 3. Basic Dual-Supply Operation of the DAC7714.

DIGITAL INTERFACE

Figure 4 and Table I provide the basic timing for the DAC7714. The interface consists of a serial clock (CLK), serial data (SDI), and a load DAC signal ($\overline{\text{LOADDACS}}$). In addition, a chip select ($\overline{\text{CS}}$) input is available to enable serial communication when there are multiple serial devices. An asynchronous reset input ($\overline{\text{RESET}}$) is provided to simplify start-up conditions, periodic resets, or emergency resets to a known state.

The DAC code and address are provided via a 16-bit serial interface (see Figure 4). The first two bits select the DAC register that will be updated when $\overline{\text{LOADDACS}}$ goes LOW (see Table II). The next two bits are not used. The last 12 bits is the DAC code which is provided, most significant bit first.

Note that $\overline{\text{CS}}$ and CLK are combined with an OR gate and the output controls the serial-to-parallel shift register internal to the DAC7714 (see the block diagram on the front of this data sheet). These two inputs are completely interchangeable. In addition, care must be taken with the state of CLK when $\overline{\text{CS}}$ rises at the end of a serial transfer. If CLK is LOW when $\overline{\text{CS}}$ rises, the OR gate will provide a rising edge to the shift register, shifting the internal data one additional bit. The result will be incorrect data and possible selection of the wrong DAC.

If both $\overline{\text{CS}}$ and CLK are used, then $\overline{\text{CS}}$ should rise only when CLK is HIGH. If not, then either $\overline{\text{CS}}$ or CLK can be used to operate the shift register. See Table III for more information.

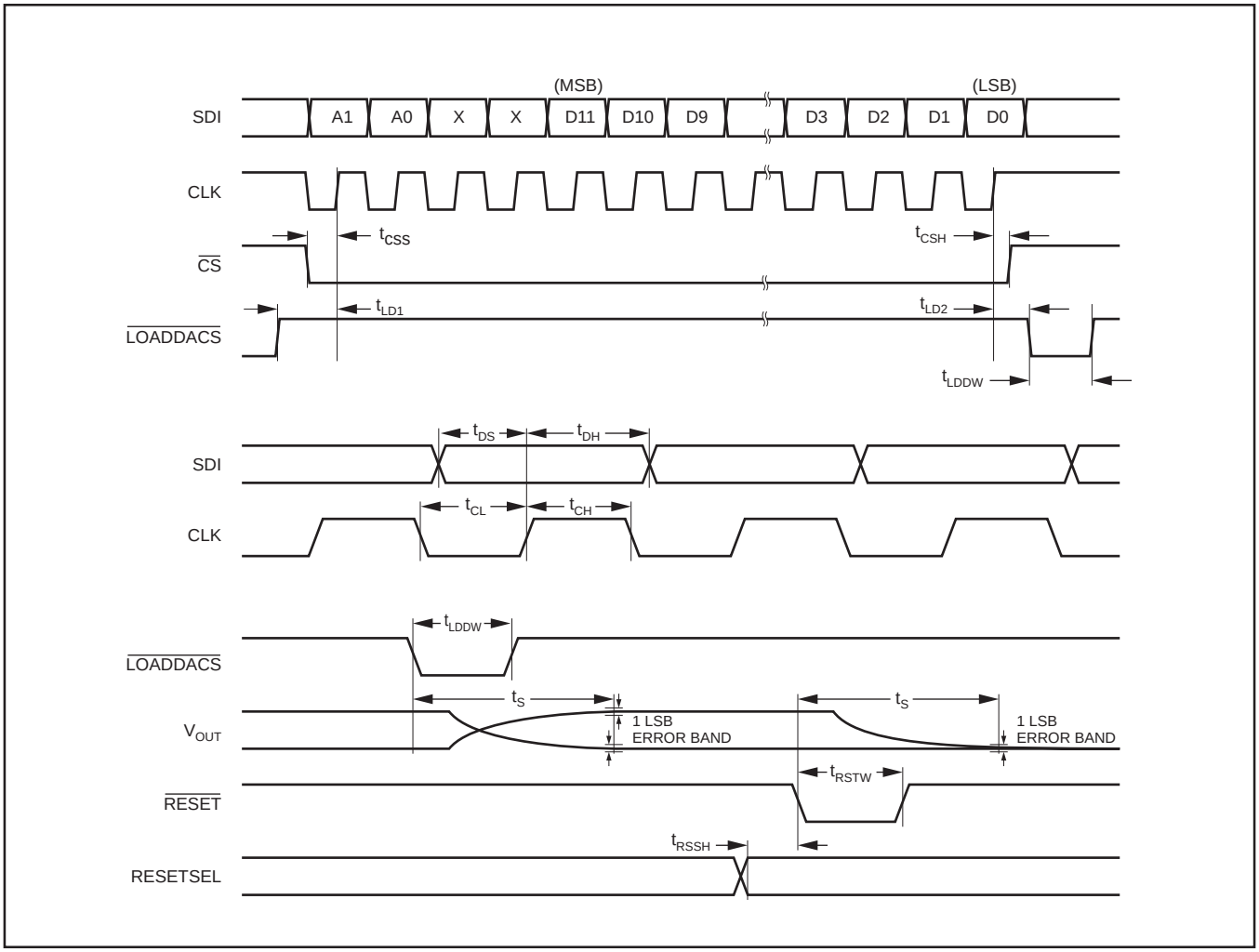


FIGURE 4. DAC7714 Timing.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{DS}	Data Valid to CLK Rising	25			ns
t_{DH}	Data Held Valid after CLK Rises	20			ns
t_{CH}	CLK HIGH	30			ns
t_{CL}	CLK LOW	50			ns
t_{CSS}	$\overline{CS}$ LOW to CLK Rising	55			ns
t_{CSH}	CLK HIGH to $\overline{CS}$ Rising	15			ns
t_{LD1}	$\overline{LOADDACS}$ HIGH to CLK Rising	40			ns
t_{LD2}	CLK Rising to $\overline{LOADDACS}$ LOW	15			ns
t_{LDDW}	$\overline{LOADDACS}$ LOW Time	45			ns
t_{RSSH}	RESETSEL Valid to $\overline{RESET}$ LOW	25			ns
t_{RSTW}	$\overline{RESET}$ LOW Time	70			ns
t_S	Settling Time	10			µs

TABLE I. Timing Specifications (T_A = –40°C to +85°C).

A1	A0	$\overline{LOADDACS}$	$\overline{RESET}$	SELECTED DAC REGISTER	STATE OF SELECTED DAC REGISTER
L(1)	L	L	H(2)	A	Transparent
L	H	L	H	B	Transparent
H	L	L	H	C	Transparent
H	H	L	H	D	Transparent
X(3)	X	H	H	NONE	(All Latched)
X	X	X	L	ALL	Reset(4)

NOTES: (1) L = Logic LOW. (2) H = Logic HIGH. (3) X = Don't Care. (4) Resets to either 000H or 800_H, per the RESETSEL state (LOW = 000_H, HIGH = 800_H). When $\overline{RESET}$ rises, all registers that are in their latched state retain the reset value.

TABLE II. Control Logic Truth Table.

$\overline{CS}$[1]	CLK[1]	$\overline{LOADDACS}$	$\overline{RESET}$	SERIAL SHIFT REGISTER
H[2]	X[3]	H	H	No Change
L[4]	L	H	H	No Change
L	↑[5]	H	H	Advanced One Bit
↑	L	H	H	Advanced One Bit
H[6]	X	L[7]	H	No Change
H[6]	X	H	L[8]	No Change

NOTES: (1) $\overline{CS}$ and CLK are interchangeable. (2) H = Logic HIGH. (3) X = Don't Care. (4) L = Logic LOW (5) = Positive Logic Transition. (6) A HIGH value is suggested in order to avoid a "false clock" from advancing the shift register and changing the shift register. (7) If data is clocked into the serial register while $\overline{LOADDACS}$ is LOW, the selected DAC register will change as the shift register bits "flow" through A1 and A0. This will corrupt the data in each DAC register that has been erroneously selected. (8) $\overline{RESET}$ LOW causes no change in the contents of the serial shift register.

TABLE III. Serial Shift Register Truth Table.

Digital Input Coding

The DAC7714 input data is in Straight Binary format. The output voltage is given by the following equation:

$$V_{OUT} = V_{REFL} + \frac{(V_{REFH} - V_{REFL}) \bullet N}{4096}$$

where N is the digital input code (in decimal). This equation does not include the effects of offset (zero-scale) or gain (full-scale) errors.

LAYOUT

A precision analog component requires careful layout, adequate bypassing, and clean, well-regulated power supplies. As the DAC7714 offers single-supply operation, it will often be used in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it will be to achieve good performance from the converter.

Because the DAC7714 has a single ground pin, all return currents, including digital and analog return currents, must flow through the GND pin. Ideally, GND would be connected directly to an analog ground plane. This plane would be separate from the ground connection for the digital components until they were connected at the power entry point of the system.

The power applied to V_{CC} (as well as V_{SS}, if not grounded) should be well regulated and low noise. Switching power supplies and DC/DC converters will often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes as their internal logic switches states. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DAC7714U	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC7714U
DAC7714U.A	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC7714U
DAC7714U/1K	Active	Production	SOIC (DW) | 16	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC7714U
DAC7714U/1K.A	Active	Production	SOIC (DW) | 16	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC7714U
DAC7714UB	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC7714U B
DAC7714UB.A	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC7714U B
DAC7714UB/1K	Active	Production	SOIC (DW) | 16	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC7714U B
DAC7714UB/1K.A	Active	Production	SOIC (DW) | 16	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC7714U B
DAC7714UBG4	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC7714U B

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

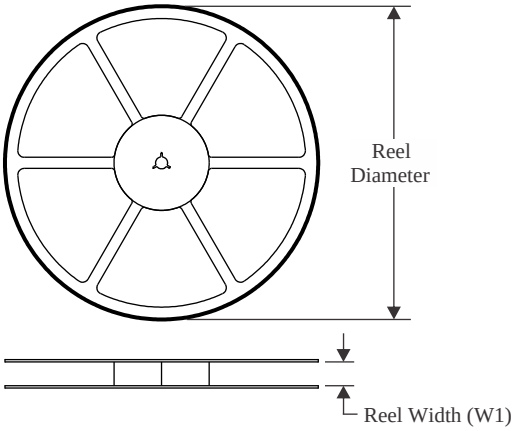
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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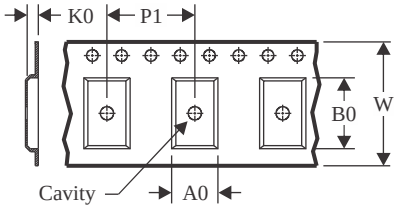
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

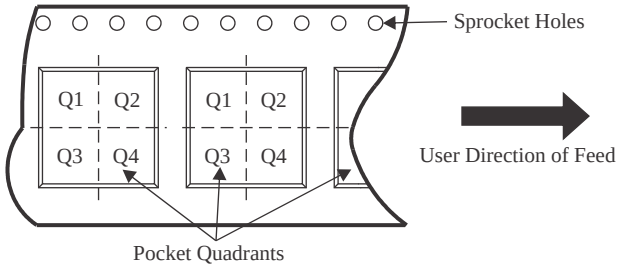


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

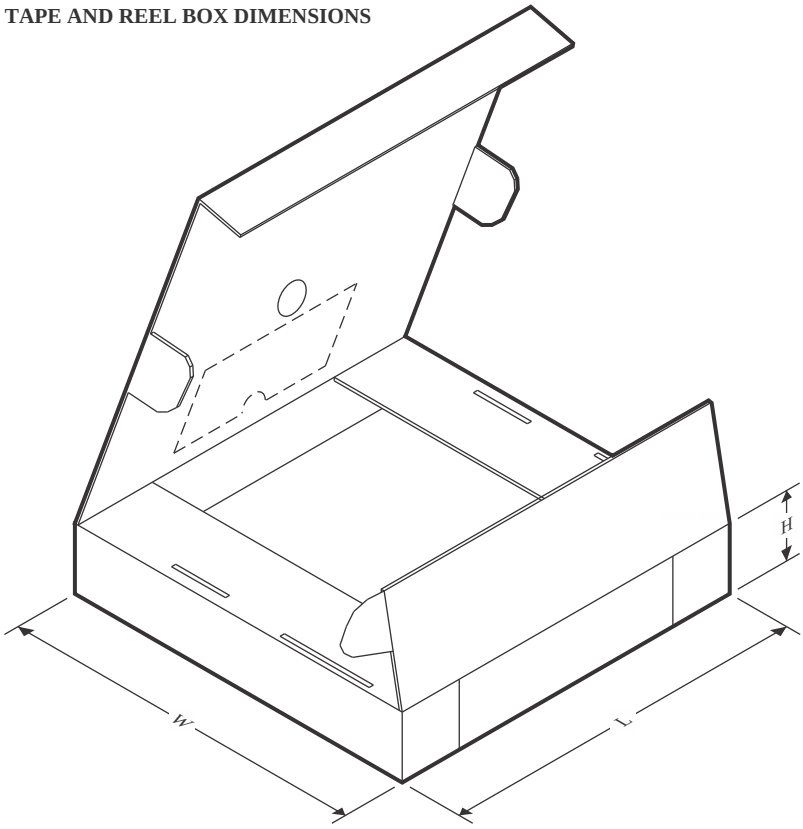
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC7714U/1K	SOIC	DW	16	1000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
DAC7714UB/1K	SOIC	DW	16	1000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

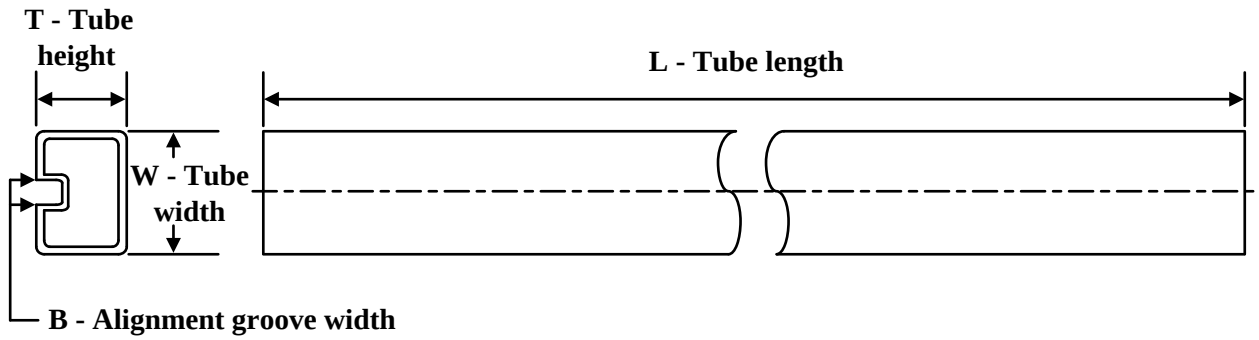
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC7714U/1K	SOIC	DW	16	1000	350.0	350.0	43.0
DAC7714UB/1K	SOIC	DW	16	1000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DAC7714U	DW	SOIC	16	40	506.98	12.7	4826	6.6
DAC7714U.A	DW	SOIC	16	40	506.98	12.7	4826	6.6
DAC7714UB	DW	SOIC	16	40	506.98	12.7	4826	6.6
DAC7714UB.A	DW	SOIC	16	40	506.98	12.7	4826	6.6
DAC7714UBG4	DW	SOIC	16	40	506.98	12.7	4826	6.6

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