# X9C102, X9C103, X9C104, X9C503

Digitally Controlled Potentiometer (XDCP™)

FN8222
Rev 4.00
Jan 11, 2019

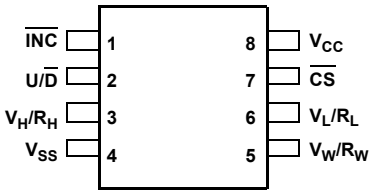
The X9C102, X9C103, X9C104, X9C503 are digitally controlled (XDCP) potentiometers. The device consists of a resistor array, wiper switches, a control section, and nonvolatile memory. The wiper position is controlled by a three-wire interface.

The potentiometer is implemented by a resistor array composed of 99 resistive elements and a wiper switching network. Between each element and at either end are tap points accessible to the wiper terminal. The position of the wiper element is controlled by the $\overline{CS}$, U/$\overline{D}$, and $\overline{INC}$ inputs. The position of the wiper can be stored in non-volatile memory and then be recalled upon a subsequent power-up operation.

The device can be used as a three-terminal potentiometer or as a two-terminal variable resistor in a wide variety of applications ranging from control to signal processing to parameter adjustment.

## Pinout

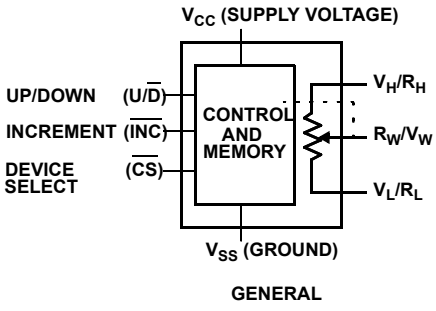
**X9C102, X9C103, X9C104, X9C503**
**(8 LD SOIC, 8 LD PDIP)**
TOP VIEW

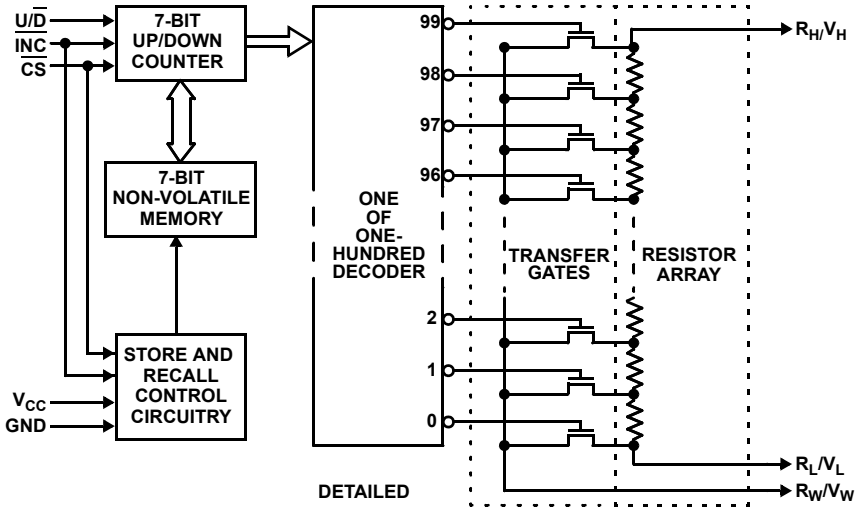



## Features

- Solid-State Potentiometer
- Three-Wire Serial Interface
- 100 Wiper Tap Points
  - Wiper Position Stored in Non-volatile Memory and Recalled on Power-up
- 99 Resistive Elements
  - Temperature Compensated
  - End-to-End Resistance, ±20%
  - Terminal Voltages, ±5V
- Low Power CMOS
  - $V_{CC}$ = 5V
  - Active Current, 3mA max.
  - Standby Current, 750µA max.
- High Reliability
  - Endurance, 100,000 Data Changes per Bit
  - Register Data Retention, 100 years
- X9C102 = 1kΩ
- X9C103 = 10kΩ
- X9C503 = 50kΩ
- X9C104 = 100kΩ
- Packages
  - 8 Ld SOIC
  - 8 Ld PDIP
- Pb-Free Available (RoHS Compliant)

## Block Diagram



## Ordering Information

| PART NUMBER | PART MARKING | $R_{TOTAL}$ (kΩ) | TEMP RANGE (°C) | PACKAGE (RoHS Compliant) | PACKAGE DWG. # |
|---|---|---|---|---|---|
| X9C102PZ (Notes 2, 3) | X9C102P Z | 1 | 0 to +70 | 8 Ld PDIP | MDP0031 |
| X9C102PIZ (Notes 2, 3) | X9C102P ZI | | -40 to +85 | 8 Ld PDIP | MDP0031 |
| X9C102SZ (Notes 1, 2) | X9C102S Z | | 0 to +70 | 8 Ld SOIC | M8.15E |
| X9C102SIZ (Notes 1, 2) | X9C102S ZI | | -40 to +85 | 8 Ld SOIC | M8.15E |
| X9C103PZ (Notes 2, 3) | X9C103P Z | 10 | 0 to +70 | 8 Ld PDIP | MDP0031 |
| X9C103PIZ (Notes 2, 3) | X9C103P ZI | | -40 to +85 | 8 Ld PDIP | MDP0031 |
| X9C103SZ (Notes 1, 2) | X9C103S Z | | 0 to +70 | 8 Ld SOIC | M8.15 |
| X9C103SIZ (Notes 1, 2) | X9C103S ZI | | -40 to +85 | 8 Ld SOIC | M8.15 |
| X9C503PZ (Notes 2, 3) | X9C503P Z | 50 | 0 to +70 | 8 Ld PDIP | MDP0031 |
| X9C503PIZ (Notes 2, 3) | X9C503P ZI | | -40 to +85 | 8 Ld PDIP | MDP0031 |
| X9C503SZ (Notes 1, 2) | X9C503S Z | | 0 to +70 | 8 Ld SOIC | M8.15E |
| X9C503SIZ (Notes 1, 2) | X9C503S ZI | | -40 to +85 | 8 Ld SOIC | M8.15E |
| X9C104PIZ (Notes 2, 3) | X9C104P ZI | 100 | -40 to +85 | 8 Ld PDIP | MDP0031 |
| X9C104SZ (Notes 1, 2) | X9C104S Z | | 0 to +70 | 8 Ld SOIC | M8.15E |
| X9C104SIZ (Notes 1, 2) | X9C104S ZI | | -40 to +85 | 8 Ld SOIC | M8.15E |

NOTES:

1. Add “T1” suffix for tape and reel. See TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. Pb-free PDIPs can be used for through-hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

## Pin Descriptions

| PIN NUMBER | PIN NAME | DESCRIPTION |
|---|---|---|
| 1 | $\overline{INC}$ | **INCREMENT** The $\overline{INC}$ input is negative-edge triggered. Toggling $\overline{INC}$ will move the wiper and either increment or decrement the counter in the direction indicated by the logic level on the U/$\overline{D}$ input. |
| 2 | U/$\overline{D}$ | **UP/DOWN** The U/$\overline{D}$ input controls the direction of the wiper movement and whether the counter is incremented or decremented. |
| 3 | $V_H/R_H$ | **$V_H/R_H$** The high ($V_H/R_H$) terminals of the X9C102, X9C103, X9C104, X9C503 are equivalent to the fixed terminals of a mechanical potentiometer. The minimum voltage is -5V and the maximum is +5V. The terminology of $V_H/R_H$ and $V_L/R_L$ references the relative position of the terminal in relation to wiper movement direction selected by the U/$\overline{D}$ input and not the voltage potential on the terminal. |
| 4 | $V_{SS}$ | **$V_{SS}$** |
| 5 | $V_W/R_W$ | **$V_W/R_W$** $V_W/R_W$ is the wiper terminal and is equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the control inputs. The wiper terminal series resistance is typically 40Ω. |
| 6 | $R_L/V_L$ | **$R_L/V_L$** The low ($V_L/R_L$) terminals of the X9C102, X9C103, X9C104, X9C503 are equivalent to the fixed terminals of a mechanical potentiometer. The minimum voltage is -5V and the maximum is +5V. The terminology of $V_H/R_H$ and $V_L/R_L$ references the relative position of the terminal in relation to wiper movement direction selected by the U/$\overline{D}$ input and not the voltage potential on the terminal. |
| 7 | $\overline{CS}$ | **$\overline{CS}$** The device is selected when the $\overline{CS}$ input is LOW. The current counter value is stored in non-volatile memory when $\overline{CS}$ is returned HIGH while the $\overline{INC}$ input is also HIGH. After the store operation is complete the X9C102, X9C103, X9C104, X9C503 device will be placed in the low power standby mode until the device is selected once again. |
| 8 | $V_{CC}$ | **$V_{CC}$** |

## Absolute Maximum Ratings

Voltage on $\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ and $V_{CC}$ with Respect to $V_{SS}$ . -1V to +7V
Voltage on $V_H/R_H$ and $V_L/R_L$ Referenced to $V_{SS}$ . . . . . -8V to +8V
$\Delta V = |V_H/R_H - V_L/R_L|$
X9C102 . . . . . .4V
X9C103, X9C104, and X9C503 . . . . . .10V
$I_W$ (10s) . . . . . .8.8mA
Power Rating
X9C102 . . . . . .16mW
X9C103 X0C104, and X9C503 . . . . . .10mW

## Thermal Information

Temperature Under Bias . . . . . .-65°C to +135°C
Storage Temperature . . . . . .-65°C to +150°C
Pb-Free Reflow Profile. . . . . TB493
*Pb-free PDIPs can be used for through-hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

## Recommended Operating Conditions

Commercial Temperature Range. . . . . 0°C to +70°C
Industrial Temperature Range . . . . . .-40°C to +85°C
Supply Voltage Range ($V_{CC}$) . . . . . 5V ±10%

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

## Electrical Specifications

Over recommended operating conditions unless otherwise stated.

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS MIN | LIMITS TYP (Note 7) | LIMITS MAX | UNIT |
|---|---|---|---|---|---|---|
| **POTENTIOMETER CHARACTERISTICS** | | | | | | |
| $R_{TOTAL}$ | End-to-End Resistance Variation | | -20 | | +20 | % |
| $V_{VH/RH}$ | $V_H$ Terminal Voltage | | -5 | | +5 | V |
| $V_{VL/RL}$ | $V_L$ Terminal Voltage | | -5 | | +5 | V |
| $I_W$ | Wiper Current | | -4.4 | | 4.4 | mA |
| $R_W$ | Wiper Resistance | Wiper Current = ±1mA | | 40 | 100 | Ω |
| | Resistor Noise (Note 8) | Ref 1kHz | | -120 | | dBV |
| | Charge Pump Noise (Note 8) | @ 850kHz | | 20 | | $mV_{RMS}$ |
| | Resolution | | | 1 | | % |
| | Absolute Linearity (Note 4) | $V_{W(n)(actual)} - V_{W(n)(EXPECTED)}$ | -1 | | +1 | MI (Note 6) |
| | Relative Linearity (Note 5) | $V_{W(n+1)(ACTUAL)} - [V_{W(n)} + MI]$ | -0.2 | | +0.2 | MI (Note 6) |
| | $R_{TOTAL}$ Temperature Coefficient | X9C103, X9C503, X9C104 | | ±300 (Note 8) | | ppm/°C |
| | $R_{TOTAL}$ Temperature Coefficient | X9C102 | | ±600 (Note 8) | | ppm/°C |
| | Ratiometric Temperature Coefficient | | | ±20 | | ppm/°C |
| $C_H/C_L/C_W$ (Note 8) | Potentiometer Capacitances | See “Circuit #3 SPICE Macro Model” on page 5. | | 10/10/25 | | pF |
| **DC OPERATING CHARACTERISTICS** | | | | | | |
| $I_{CC}$ | $V_{CC}$ Active Current | $\overline{CS}$ = $V_{IL}$, U/$\overline{D}$ = $V_{IL}$ or $V_{IH}$ and $\overline{INC}$ = 0.4V to 2.4V at Max $t_{CYC}$ | | 1 | 3 | mA |
| $I_{SB}$ | Standby Supply Current | $\overline{CS}$ = $V_{CC}$ - 0.3V, U/$\overline{D}$ and $\overline{INC}$ = $V_{SS}$ or $V_{CC}$ - 0.3V | | 200 | 750 | µA |
| $I_{LI}$ | $\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ Input Leakage Current | $V_{IN}$ = $V_{SS}$ to $V_{CC}$ | | | ±10 | µA |
| $V_{IH}$ | $\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ input HIGH Voltage | | 2 | | | V |
| $V_{IL}$ | $\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ input LOW Voltage | | | | 0.8 | V |
| $C_{IN}$ | $\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ Input Capacitance (Note 8) | $V_{CC}$ = 5V, $V_{IN}$ = $V_{SS}$, $T_A$ = +25°C, f = 1MHz | | 10 | | pF |

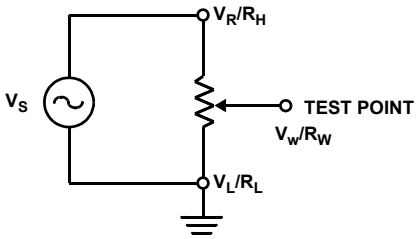
**Electrical Specifications** Over recommended operating conditions unless otherwise stated. **(Continued)**

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP (Note 7) | MAX | |
| **AC OPERATION CHARACTERISTICS** | | | | | | |
| $t_{CI}$ | $\overline{CS}$ to $\overline{INC}$ Setup | | 100 | | | ns |
| $t_{ID}$ | $\overline{INC}$ HIGH to U/$\overline{D}$ Change | | 100 | | | ns |
| $t_{DI}$ | U/$\overline{D}$ to $\overline{INC}$ Setup | | 2.9 | | | µs |
| $t_{IL}$ | $\overline{INC}$ LOW Period | | 1 | | | µs |
| $t_{IH}$ | $\overline{INC}$ HIGH Period | | 1 | | | µs |
| $t_{IC}$ | $\overline{INC}$ Inactive to $\overline{CS}$ Inactive | | 1 | | | µs |
| $t_{CPH}$ | $\overline{CS}$ Deselect Time (STORE) | | 20 | | | ms |
| $t_{CPH}$ | $\overline{CS}$ Deselect Time (NO STORE) | | 100 | | | ns |
| $t_{IW}$ (5) | $\overline{INC}$ to $V_{W/RW}$ Change | | | 100 | | µs |
| $t_{CYC}$ | $\overline{INC}$ Cycle Time | | 2 | | | µs |
| $t_{CYC}$ | $\overline{INC}$ Input Rise and Fall Time | | | | 500 | µs |
| $t_R$, $t_F$ | Power-up to Wiper Stable (Note 8) | | | 500 | | µs |
| $t_{PU}$ | $V_{CC}$ Power-up Rate (Note 8) | | 0.2 | | 50 | V/ms |

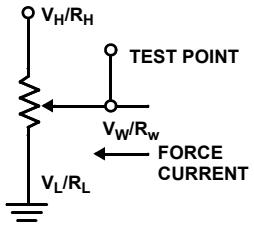
NOTES:

4. Absolute linearity is utilized to determine actual wiper voltage vs expected voltage = $[V_{W(n)(actual)} - V_{W(n)(expected)}]$ = ±1 MI Maximum.
5. Relative linearity is a measure of the error in step size between taps = $V_{W(n+1)} - [V_{W(n)+MI}]$ = +0.2 MI.
6. 1 MI = Minimum Increment = $R_{TOT}/99$.
7. Typical values are for $T_A$ = +25°C and nominal supply voltage.
8. This parameter is not 100% tested.

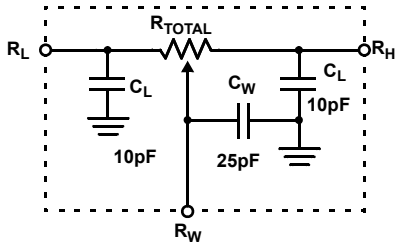
***Test Circuit #1***




***Test Circuit #2***




***Circuit #3 SPICE Macro Model***




### *Endurance and Data Retention*

| PARAMETER | MIN | UNIT |
|---|---|---|
| Medium Endurance | 100,000 | Data changes per bit per register |
| Data Retention | 100 | years |

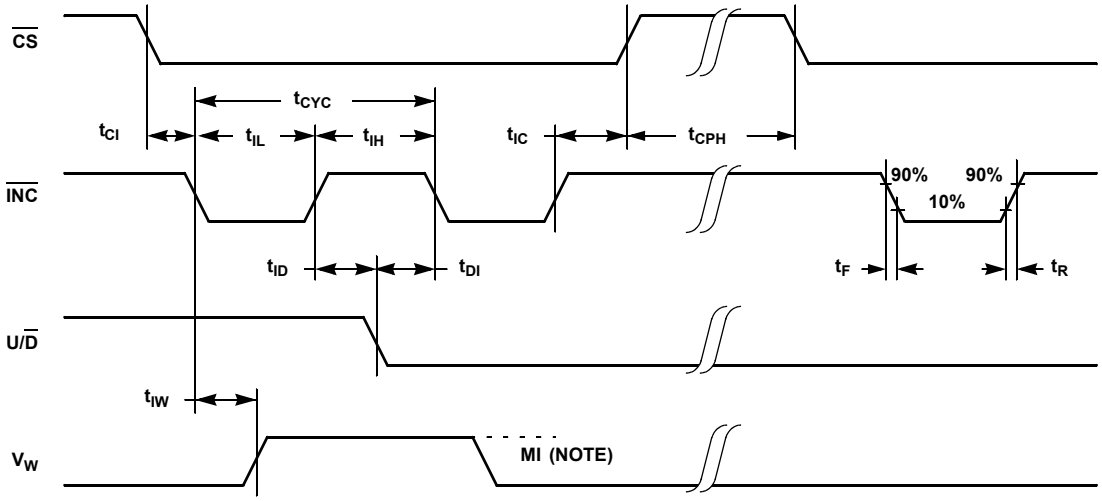
### *AC Conditions of Test*

| | |
|---|---|
| Input Pulse Levels | 0V to 3V |
| Input Rise and Fall Times | 10ns |
| Input Reference Levels | 1.5V |

## *Power-up and Down Requirements*

At all times, voltages on the potentiometer pins must be less than ±$V_{CC}$. The recall of the wiper position from non-volatile memory is not in effect until the $V_{CC}$ supply reaches its final value. The $V_{CC}$ ramp rate specification is always in effect.

## AC Timing Diagram




NOTE: MI REFERS TO THE MINIMUM INCREMENTAL CHANGE IN THE $V_W$ OUTPUT DUE TO A CHANGE IN THE WIPER POSITION.

## Pin Descriptions

### $R_H/V_H$ and $R_L/V_L$

The high ($V_H/R_H$) and low ($V_L/R_L$) terminals of the ISLX9C102, X9C103, X9C104, X9C503 are equivalent to the fixed terminals of a mechanical potentiometer. The minimum voltage is -5V and the maximum is +5V. The terminology of $V_H/R_H$ and $V_L/R_L$ references the relative position of the terminal in relation to wiper movement direction selected by the U/$\overline{D}$ input and not the voltage potential on the terminal.

### $R_W/V_W$

$V_W/R_W$ is the wiper terminal, and is equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the control inputs. The wiper terminal series resistance is typically 40Ω.

### Up/Down (U/$\overline{D}$)

The U/$\overline{D}$ input controls the direction of the wiper movement and whether the counter is incremented or decremented.

### Increment ($\overline{INC}$)

The $\overline{INC}$ input is negative-edge triggered. Toggling $\overline{INC}$ will move the wiper and either increment or decrement the counter in the direction indicated by the logic level on the U/$\overline{D}$ input.

### Chip Select ($\overline{CS}$)

The device is selected when the $\overline{CS}$ input is LOW. The current counter value is stored in non-volatile memory when $\overline{CS}$ is returned HIGH while the $\overline{INC}$ input is also HIGH. After the store operation is complete the ISLX9C102, X9C103, X9C104, X9C503 device will be placed in the low power standby mode until the device is selected once again.

## Principles of Operation

There are three sections of the X9C102, X9C103, ISL9C104 and ISL9C503: the input control, counter and decode section; the non-volatile memory; and the resistor array. The input control section operates just like an up/down counter. The output of this counter is decoded to turn on a single electronic switch connecting a point on the resistor array to the wiper output. Under the proper conditions, the contents of the counter can be stored in non-volatile memory and retained for future use. The resistor array is comprised of 99 individual resistors connected in series. At either end of the array and between each resistor is an electronic switch that transfers the potential at that point to the wiper.

The wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. That is, the counter does not wrap around when clocked to either extreme.

The electronic switches on the device operate in a “make-before-break” mode when the wiper changes tap positions. If the wiper is moved several positions, multiple taps are connected to the wiper for $t_{IW}$ ($\overline{INC}$ to $V_W/R_W$ change). The $R_{TOTAL}$ value for the device can temporarily be reduced by a significant amount if the wiper is moved several positions.

When the device is powered-down, the last wiper position stored will be maintained in the non-volatile memory. When power is restored, the contents of the memory are recalled and the wiper is reset to the value last stored.

The internal charge pump allows a wide range of voltages (from -5V to 5V) applied to XDCP terminals yet given a convenience of single power supply. The typical charge pump noise of 20mV at 850kHz should be taken in consideration when designing an application circuit.

### *Instructions and Programming*

The $\overline{INC}$, U/$\overline{D}$ and $\overline{CS}$ inputs control the movement of the wiper along the resistor array. With $\overline{CS}$ set LOW, the device is selected and enabled to respond to the U/$\overline{D}$ and $\overline{INC}$ inputs. HIGH to LOW transitions on $\overline{INC}$ will increment or decrement (depending on the state of the U/$\overline{D}$ input) a 7-bit counter. The output of this counter is decoded to select one of one-hundred wiper positions along the resistive array.

The value of the counter is stored in non-volatile memory whenever $\overline{CS}$ transitions HIGH while the $\overline{INC}$ input is also HIGH.

The system may select the X9Cxxx, move the wiper and deselect the device without having to store the latest wiper position in non-volatile memory. After the wiper movement is performed as previously described and once the new position is reached, the system must keep $\overline{INC}$ LOW while taking $\overline{CS}$ HIGH. The new wiper position will be maintained until changed by the system or until a power-down/up cycle recalled the previously stored data.

This procedure allows the system to always power-up to a pre-set value stored in non-volatile memory; then during system operation, minor adjustments could be made. The adjustments might be based on user preference, i.e.: system parameter changes due to temperature drift, etc.

The state of U/$\overline{D}$ may be changed while $\overline{CS}$ remains LOW. This allows the host system to enable the device and then move the wiper up and down until the proper trim is attained.

## *Mode Selection*

| $\overline{CS}$ | $\overline{INC}$ | U/$\overline{D}$ | MODE |
|---|---|---|---|
| L | ↘ | H | Wiper Up |
| L | ↘ | L | Wiper Down |
| ↗ | H | X | Store Wiper Position |
| H | X | X | Standby Current |
| ↗ | L | X | No Store, Return to Standby |
| ↘ | L | H | Wiper Up (not recommended) |
| ↘ | L | L | Wiper Down (not recommended) |

## *Symbol Table*

| WAVEFORM | INPUTS | OUTPUTS |
|---|---|---|
| | Must be steady | Will be steady |
| | May change from Low to High | Will change from Low to High |
| | May change from High to Low | Will change from High to Low |
| | Don't Care: Changes Allowed | Changing: State Not Known |
| | N/A | Center Line is High Impedance |

## *Performance Characteristics*

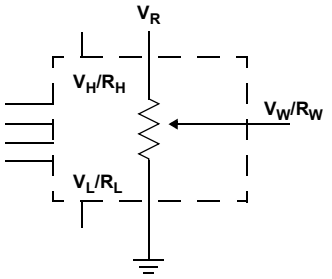
Contact the factory for more information.

## *Applications Information*

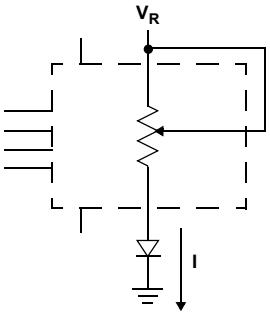
Electronic digitally controlled (XCDP) potentiometers provide three powerful application advantages:

1. The variability and reliability of a solid-state potentiometer.
2. The flexibility of computer-based digital controls.
3. The retentivity of non-volatile memory used for the storage of multiple potentiometer settings or data.

### *Basic Configurations of Electronic Potentiometers*

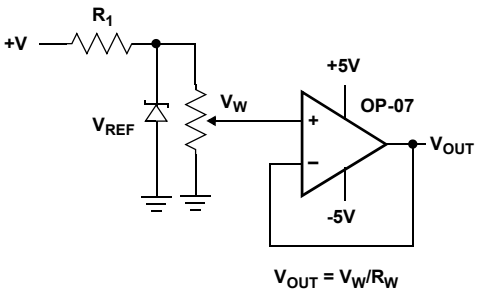



THREE TERMINAL POTENTIOMETER;
VARIABLE VOLTAGE DIVIDER

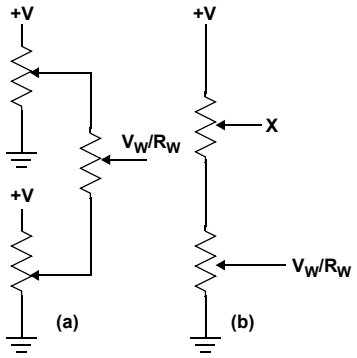



TWO TERMINAL VARIABLE RESISTOR;
VARIABLE CURRENT

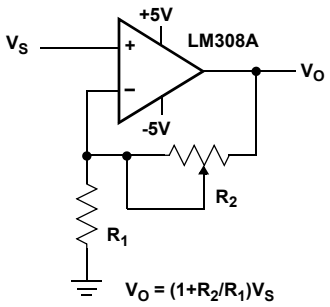
### *Basic Circuits*



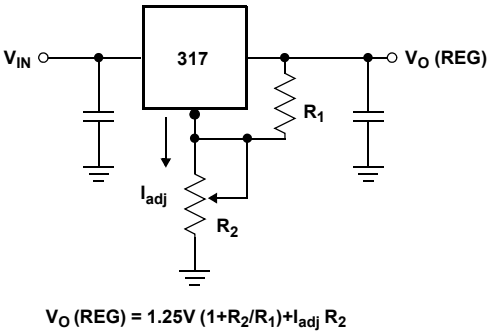

BUFFERED REFERENCE VOLTAGE



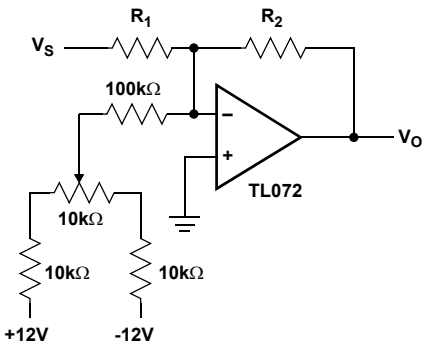

CASCADING TECHNIQUES



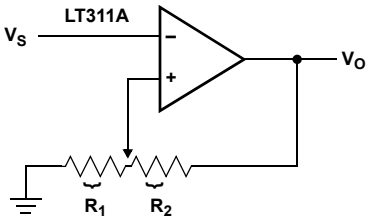

NONINVERTING AMPLIFIER




VOLTAGE REGULATOR




OFFSET VOLTAGE ADJUSTMENT




(FOR ADDITIONAL CIRCUITS SEE AN1145)

COMPARATOR WITH HYSTERESIS

## *Revision History*

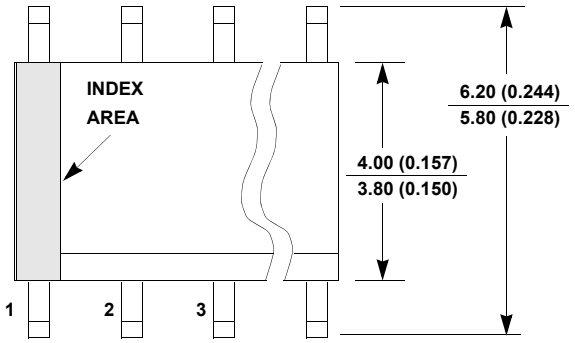
| Rev. | Date | Description |
|---|---|---|
| 4.00 | Jan 11, 2019 | Updated Ordering Information table to remove Obsolete and Retired parts.<br>Added Revision History.<br>Updated PODs for X9C102, X9C104, and X9C503 SOICs from: MDP0027 to: M8.15E and X9C103 SOIC from: MDP0027 to: M8.15, to include the Land Pattern design and convert dimensions from table to graphics.<br>Updated Intersil disclaimer to Renesas disclaimer. |

## *Package Outline Drawings*

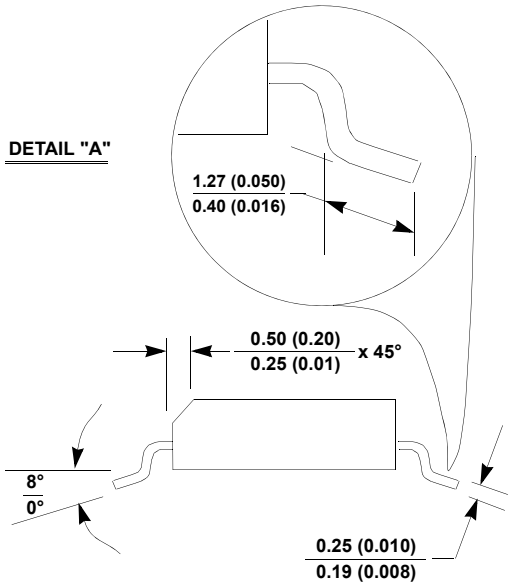
For the most recent package outline drawing, see M8.15.

### M8.15

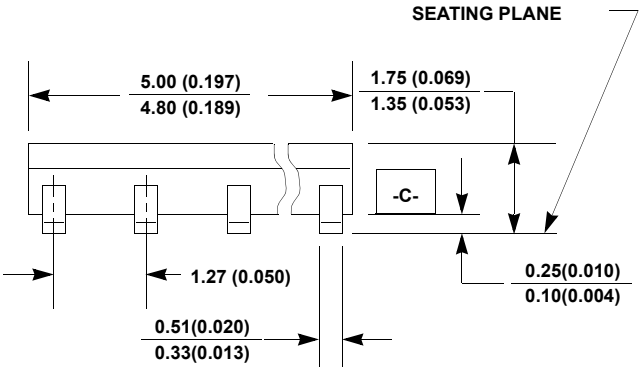
**8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE**
**Rev 4, 1/12**



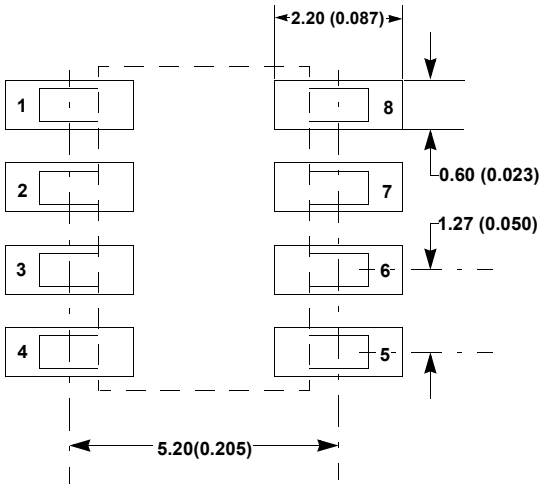

TOP VIEW




SIDE VIEW "B"




SIDE VIEW "A




TYPICAL RECOMMENDED LAND PATTERN

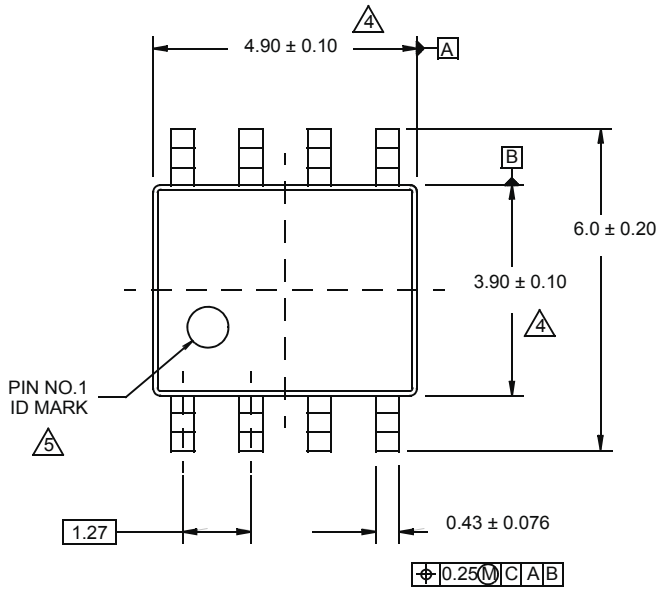
**NOTES:**

9. Dimensioning and tolerancing per ANSI Y14.5M-1994.
10. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
11. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
12. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
13. Terminal numbers are shown for reference only.
14. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
15. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
16. This outline conforms to JEDEC publication MS-012-AA ISSUE C.

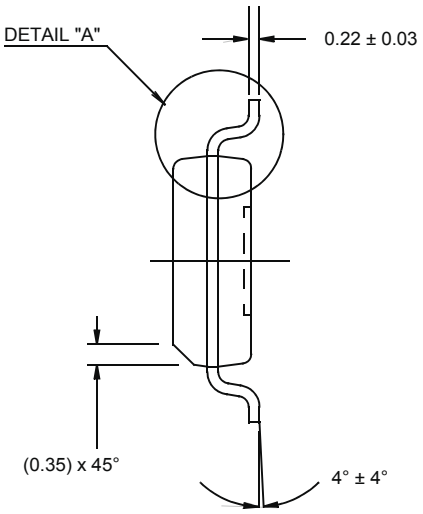
## M8.15E

**8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE**
**Rev 0, 08/09**

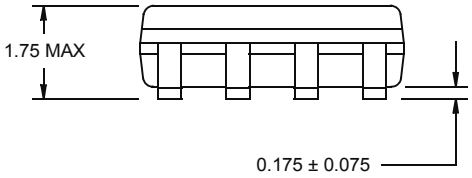
For the most recent package outline drawing, see M8.15E.



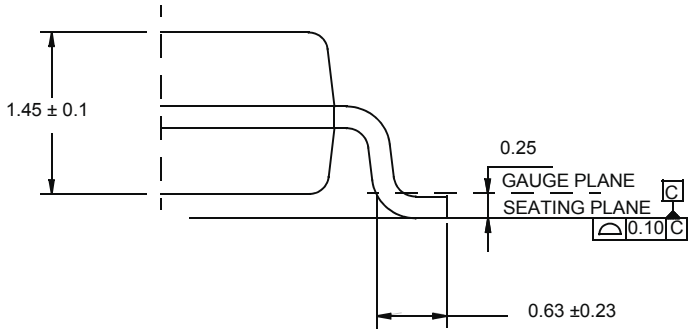

TOP VIEW



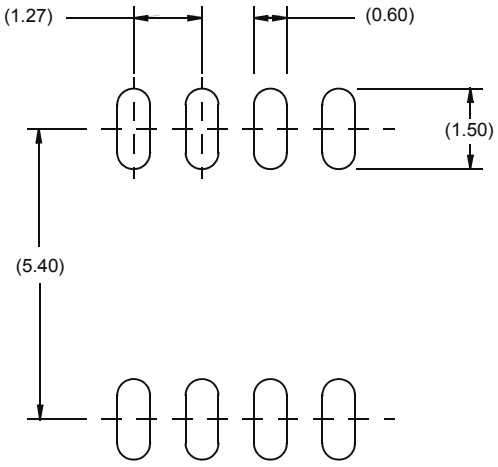

SIDE VIEW "B"




SIDE VIEW "A"




DETAIL "A"



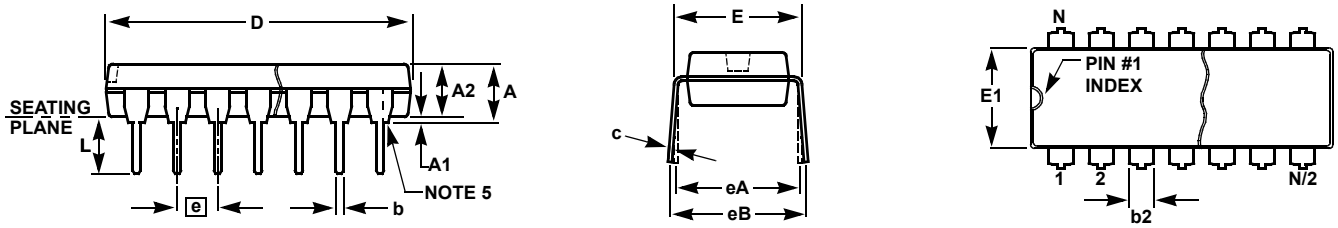

TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. Reference to JEDEC MS-012.

## *Plastic Dual-In-Line Packages (PDIP)*

For the most recent package outline drawing, see MDP0031.




### MDP0031

**PLASTIC DUAL-IN-LINE PACKAGE**

| SYMBOL | INCHES | | | | | TOLERANCE | NOTES |
|---|---|---|---|---|---|---|---|
| | PDIP8 | PDIP14 | PDIP16 | PDIP18 | PDIP20 | | |
| A | 0.210 | 0.210 | 0.210 | 0.210 | 0.210 | MAX | |
| A1 | 0.015 | 0.015 | 0.015 | 0.015 | 0.015 | MIN | |
| A2 | 0.130 | 0.130 | 0.130 | 0.130 | 0.130 | ±0.005 | |
| b | 0.018 | 0.018 | 0.018 | 0.018 | 0.018 | ±0.002 | |
| b2 | 0.060 | 0.060 | 0.060 | 0.060 | 0.060 | +0.010/-0.015 | |
| c | 0.010 | 0.010 | 0.010 | 0.010 | 0.010 | +0.004/-0.002 | |
| D | 0.375 | 0.750 | 0.750 | 0.890 | 1.020 | ±0.010 | 1 |
| E | 0.310 | 0.310 | 0.310 | 0.310 | 0.310 | +0.015/-0.010 | |
| E1 | 0.250 | 0.250 | 0.250 | 0.250 | 0.250 | ±0.005 | 2 |
| e | 0.100 | 0.100 | 0.100 | 0.100 | 0.100 | Basic | |
| eA | 0.300 | 0.300 | 0.300 | 0.300 | 0.300 | Basic | |
| eB | 0.345 | 0.345 | 0.345 | 0.345 | 0.345 | ±0.025 | |
| L | 0.125 | 0.125 | 0.125 | 0.125 | 0.125 | ±0.010 | |
| N | 8 | 14 | 16 | 18 | 20 | Reference | |

Rev. C 2/07

NOTES:

17. Plastic or metal protrusions of 0.010” maximum per side are not included.
18. Plastic interlead protrusions of 0.010” maximum per side are not included.
19. Dimensions E and eA are measured with the leads constrained perpendicular to the seating plane.
20. Dimension eB is measured with the lead tips unconstrained.
21. 8 and 16 lead packages have half end-leads as shown.

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