2.5V Single Data Rate 1:5 Clock Buffer Terabuffer™ Jr.

5T9050

DATA SHEET

FEATURES:

- Optimized for 2.5V LVTTL
- Guaranteed Low Skew < 25ps (max)
- Very low duty cycle distortion < 300 (max)
- High speed propagation delay < 1.8ns. (max)
- Up to 200MHz operation
- Very low CMOS power levels
- Hot insertable and over-voltage tolerant inputs
- 1:5 fanout buffer
- 2.5V V_{DD}
- Available in TSSOP package
- *For New Designs use functional replacement 8L30110*

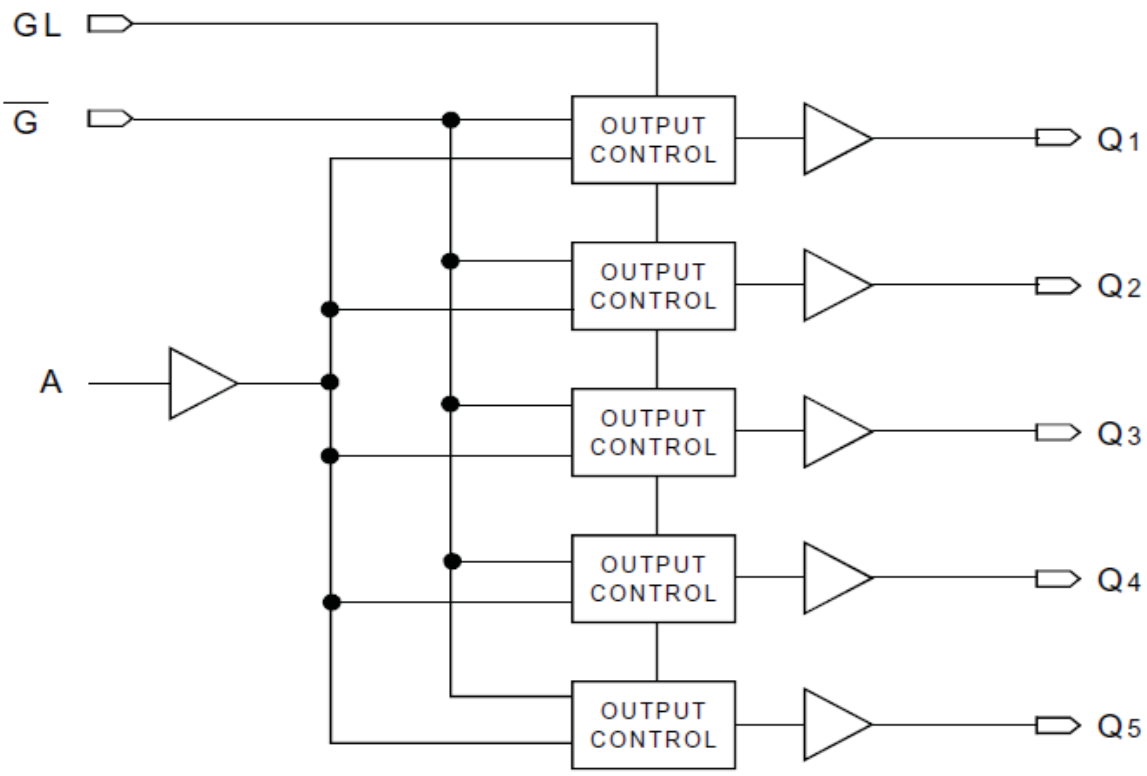
APPLICATIONS:

- Clock and signal distribution

DESCRIPTION:

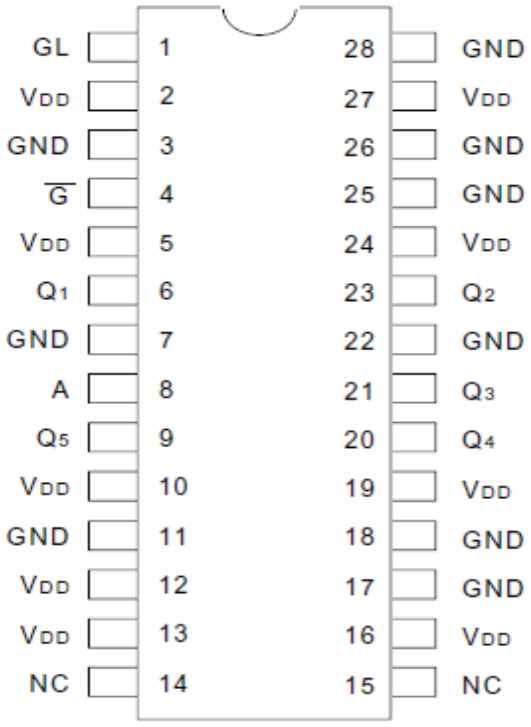
The 5T9050 2.5V single data rate (SDR) clock buffer is a single-ended input to five single-ended outputs buffer built on advanced metal CMOS technology. The SDR clock buffer fanout from a single input to five single-ended outputs reduces the loading on the preceding driver and provides an efficient clock distribution network. Multiple power and grounds reduce noise.

FUNCTIONAL BLOCK DIAGRAM



© 2019 Renesas Electronics Corporation

PIN CONFIGURATION



TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
V_{DD}	Power Supply Voltage	–0.5 to +3.6	V
V_I	Input Voltage	–0.5 to +3.6	V
V_O	Output Voltage	–0.5 to V_{DD} +0.5	V
T_{STG}	Storage Temperature	–65 to +165	°C
T_J	Junction Temperature	150	°C

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE(1) (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter	Min.	Typ.	Max.	Unit
C_{IN}	Input Capacitance	—	6	—	pF

NOTE:
1. This parameter is measured at characterization but not tested.

RECOMMENDED OPERATING RANGE

Symbol	Description	Min.	Typ.	Max.	Unit
T_A	Ambient Operating Temperature	–40	+25	+85	°C
V_{DD}	Internal Power Supply Voltage	2.3	2.5	2.7	V

PIN DESCRIPTION

Symbol	I/O	Type	Description
A	I	LVTTL	Clock input
$\overline{G}$	I	LVTTL	Gate control for Qn outputs. When $\overline{G}$ is LOW, these outputs are enabled. When $\overline{G}$ is HIGH, these outputs are asynchronously disabled to the level designated by GL(1).
GL	I	LVTTL	Specifies output disable level. If HIGH, the outputs disable HIGH. If LOW, the outputs disable LOW.
Qn	O	LVTTL	Clock outputs
V_{DD}		PWR	Power supply for the device core, inputs, and outputs
GND		PWR	Power supply return for power

NOTE:
1. Because the gate controls are asynchronous, runt pulses are possible. It is the user's responsibility to either time the gate control signals to minimize the possibility of runt pulses or be able to tolerate them in down stream circuitry.

© 2019 Renesas Electronics Corporation

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE(1)

Symbol	Parameter	Test Conditions	Min.	Typ.(4)	Max	Unit
I_{IH}	Input HIGH Current	V_{DD} = 2.7V V_I = V_{DD}/GND	—	—	±5	µA
I_{IL}	Input LOW Current	V_{DD} = 2.7V V_I = GND/V_{DD}	—	—	±5	
V_{IK}	Clamp Diode Voltage	V_{DD} = 2.3V, I_{IN} = -18mA	—	- 0.7	- 1.2	V
V_{IN}	DC Input Voltage		- 0.3		+3.6	V
V_{IH}	DC Input HIGH(2)		1.7		—	V
V_{IL}	DC Input LOW(3)		—		0.7	V
V_{OH}	Output HIGH Voltage	I_{OH} = -12mA	V_{DD} - 0.4		—	V
		I_{OH} = -100µA	V_{DD} - 0.1		—	V
V_{OL}	Output LOW Voltage	I_{OL} = 12mA	—		0.4	V
		I_{OL} = 100µA	—		0.1	V

NOTES:

1. See RECOMMENDED OPERATING RANGE table.
2. Voltage required to maintain a logic HIGH.
3. Voltage required to maintain a logic LOW.
4. Typical values are at V_{DD} = 2.5V, +25°C ambient.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions(1)	Typ.	Max	Unit
I_{DDQ}	Quiescent V_{DD} Power Supply Current	V_{DD} = Max., Reference Clock = LOW Outputs enabled, All outputs unloaded	1	1.5	mA
I_{DDD}	Dynamic V_{DD} Power Supply Current per Output	V_{DD} = Max., C_L = 0pF	100	150	µA/MHz
I_{TOT}	Total Power V_{DD} Supply Current	V_{DD} = 2.5V., $F_{REFERENCE\ CLOCK}$ = 100MHz, C_L = 15pF	50	65	mA
		V_{DD} = 2.5V., $F_{REFERENCE\ CLOCK}$ = 200MHz, C_L = 15pF	75	100	

NOTE:

1. The termination resistors are excluded from these measurements.

INPUT AC TEST CONDITIONS

Symbol	Parameter	Value	Units
V_{IH}	Input HIGH Voltage	V_{DD}	V
V_{IL}	Input LOW Voltage	0	V
V_{TH}	Input Timing Measurement Reference Level(1)	V_{DD}/2	V
t_R, t_F	Input Signal Edge Rate(2)	2	V/ns

NOTES:

1. A nominal 1.25V timing measurement reference level is specified to allow constant, repeatable results in an automatic test equipment (ATE) environment.
2. The input signal edge rate of 2V/ns or greater is to be maintained in the 10% to 90% range of the input waveform.

© 2019 Renesas Electronics Corporation

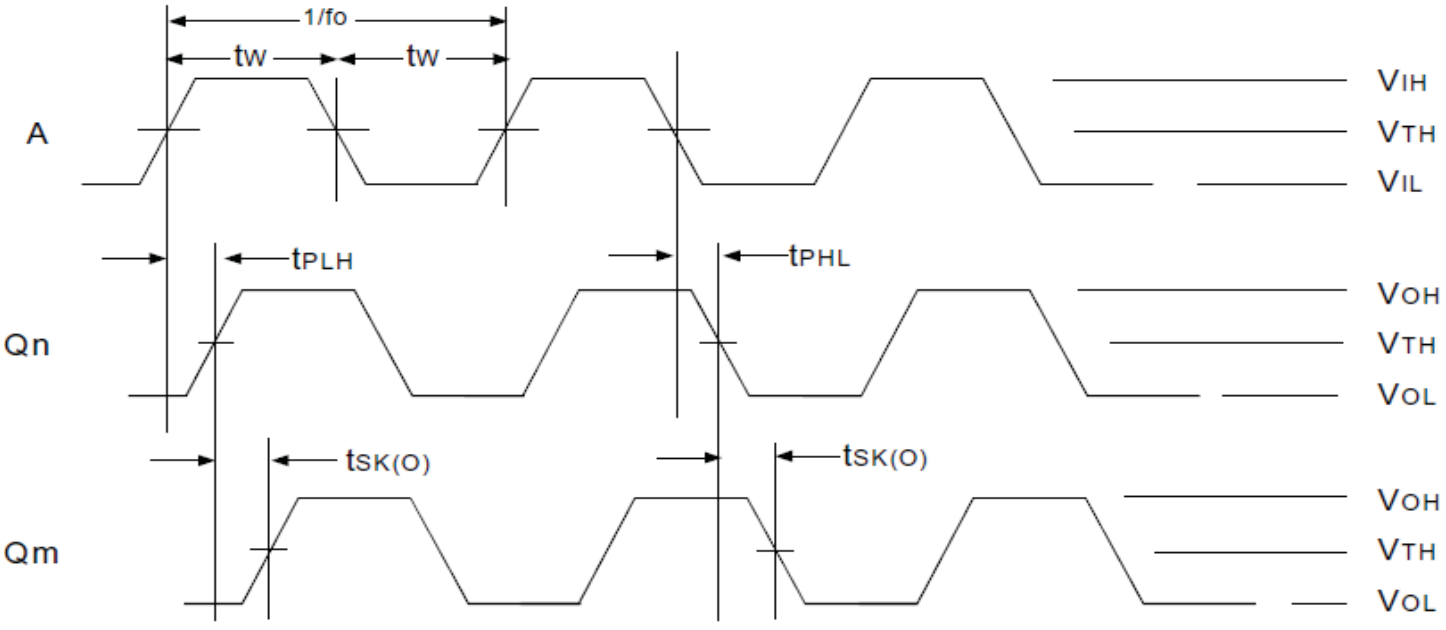
AC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE(4)

Symbol	Parameter	Min.	Typ.	Max	Unit
Skew Parameters					
$t_{SK(O)}$	Same Device Output Pin-to-Pin Skew(1)	—	—	25	ps
$t_{SK(P)}$	Pulse Skew(2)	—	—	300	ps
$t_{SK(PP)}$	Part-to-Part Skew(3)	—	—	300	ps
Propagation Delay					
t_{PLH} t_{PHL}	Propagation Delay A to Qn	—	—	1.8	ns
t_R	Output Rise Time (20% to 80%)	350	—	850	ps
t_F	Output Fall Time (20% to 80%)	350	—	850	ps
f_O	Frequency Range	—	—	200	MHz
Output Gate Enable/Disable Delay					
t_{PGE}	Output Gate Enable to Qn	—	—	3.5	ns
t_{PGD}	Output Gate Enable to Qn Driven to GL Designated Level	—	—	3	ns

NOTES:

1. Skew measured between all outputs under identical input and output transitions and load conditions on any one device.
2. Skew measured is the difference between propagation delay times t_{PHL} and t_{PLH} of any output under identical input and output transitions and load conditions on any one device.
3. Skew measured is the magnitude of the difference in propagation times between any outputs of two devices, given identical transitions and load conditions at identical V_{DD} levels and temperature.
4. Guaranteed by design.

AC TIMING WAVEFORMS



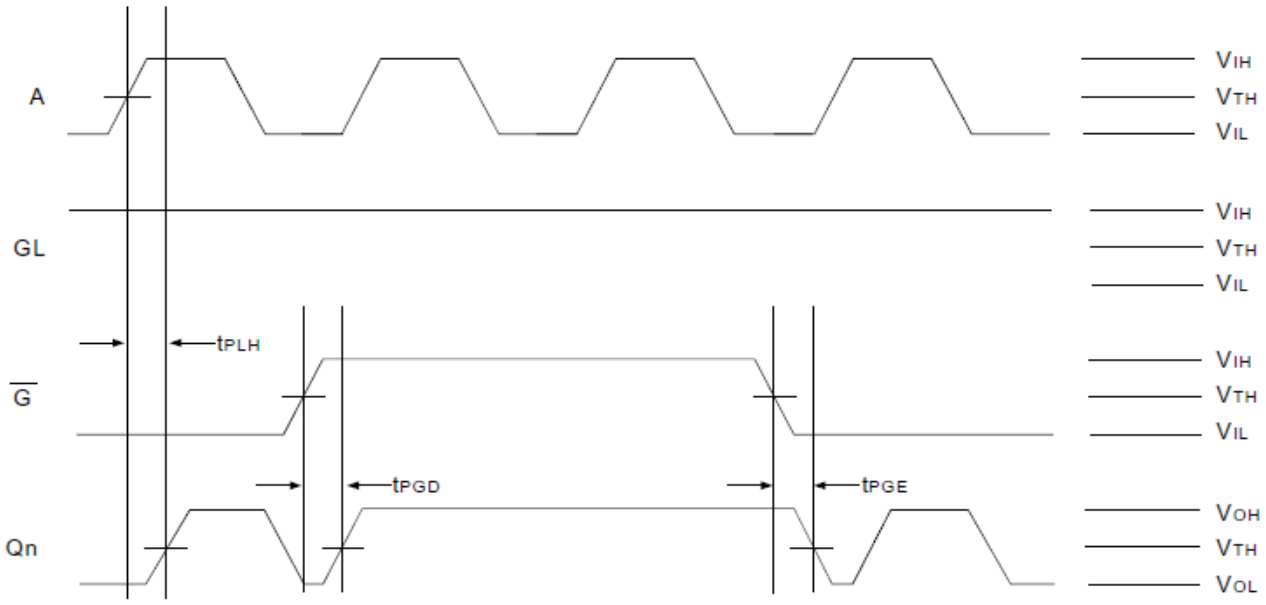
Propagation and Skew Waveforms

NOTE: Pulse Skew is calculated using the following expression:

$$t_{SK(P)} = | t_{PHL} - t_{PLH} |$$

where t_{PHL} and t_{PLH} are measured on the controlled edges of any one output from rising and falling edges of a single pulse. Please note that the t_{PHL} and t_{PLH} shown are not valid measurements for this calculation because they are not taken from the same pulse.

© 2019 Renesas Electronics Corporation



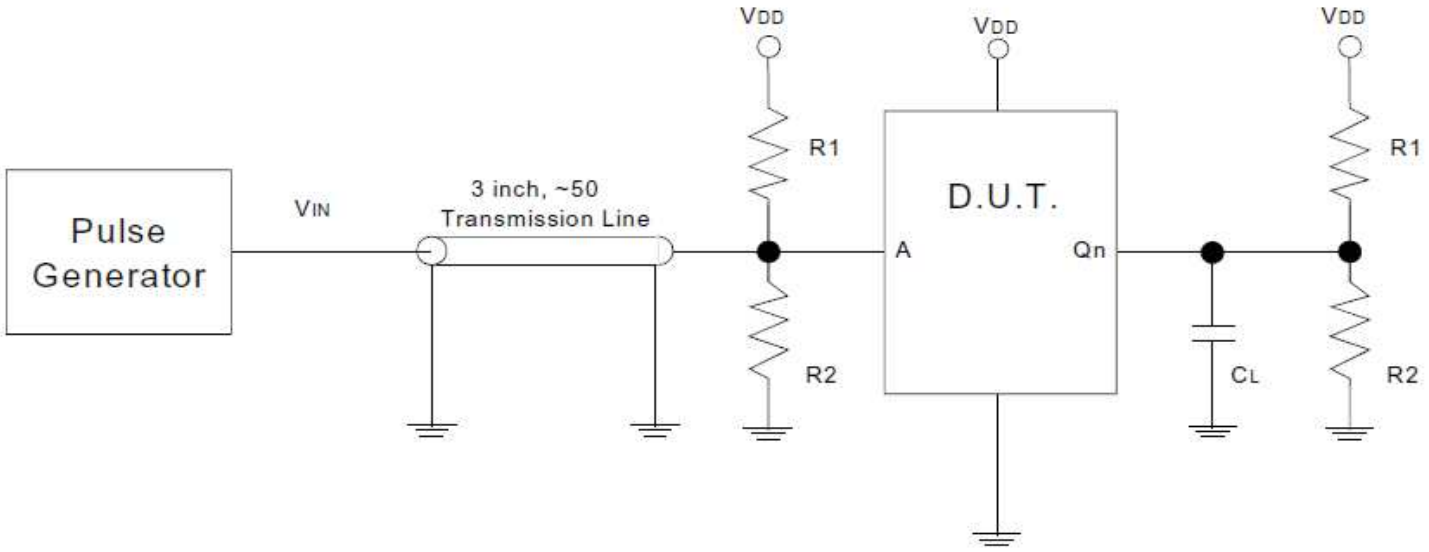
Gate Disable/Enable Showing Runt Pulse Generation

NOTE:

As shown, it is possible to generate runt pulses on gate disable and enable of the outputs. It is the user's responsibility to time their $\overline{G}$ signal to avoid this problem.

© 2019 Renesas Electronics Corporation

TEST CIRCUIT AND CONDITIONS



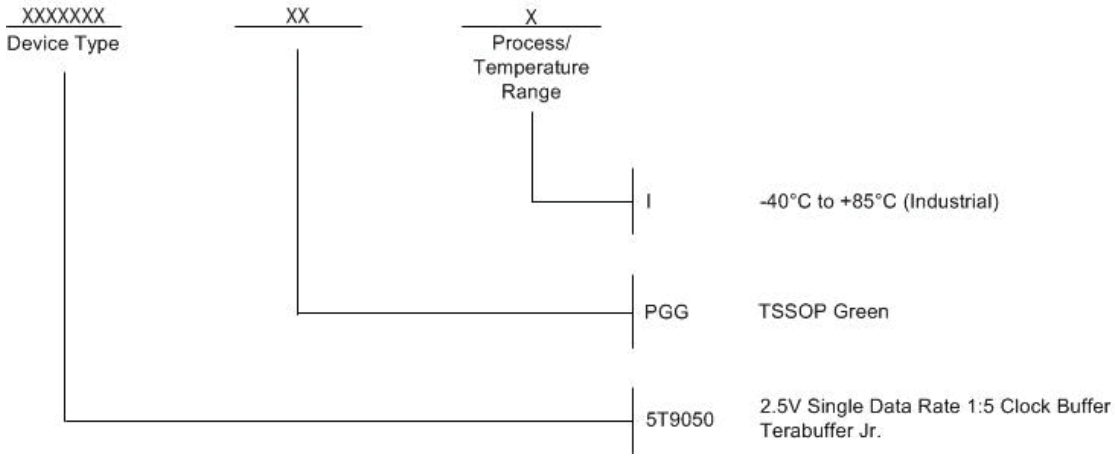
Test Circuit for Input/Output

INPUT/OUTPUT TEST CONDITIONS

Symbol	V_{DD} = 2.5V ± 0.2V	Unit
V_{TH}	V_{DD} / 2	V
R1	100	Ω
R2	100	Ω
C_L	15	pF

© 2019 Renesas Electronics Corporation

ORDERING INFORMATION



© 2019 Renesas Electronics Corporation

REVISION HISTORY

Rev	Table	Page	Discription of Change	Date
A		1	NRND - Not Recommended for New Designs	5/5/13
A		1	Product Discontinuation Notice - Last time buy expires 11/2/2016. PDN# CQ-15-05	11/2/15

© 2019 Renesas Electronics Corporation

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

© 2026 Renesas Electronics Corporation. All rights reserved.