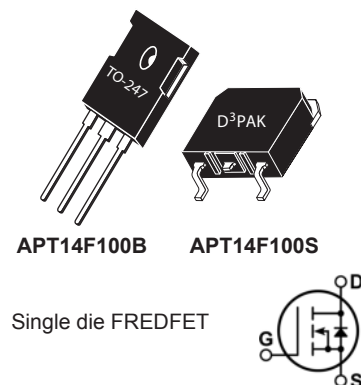


N-Channel FREDFET

Power MOS 8™ is a high speed, high voltage N-channel switch-mode power MOSFET. This 'FREDFET' version has a drain-source (body) diode that has been optimized for high reliability in ZVS phase shifted bridge and other circuits through reduced t_{rr} , soft recovery, and high recovery dv/dt capability. Low gate charge, high gain, and a greatly reduced ratio of C_{rss}/C_{iss} result in excellent noise immunity and low switching loss. The intrinsic gate resistance and capacitance of the poly-silicon gate structure help control di/dt during switching, resulting in low EMI and reliable paralleling, even when switching at very high frequency.



FEATURES

- Fast switching with low EMI
- Low t_{rr} for high reliability
- Ultra low C_{rss} for improved noise immunity
- Low gate charge
- Avalanche energy rated
- RoHS compliant 

TYPICAL APPLICATIONS

- ZVS phase shifted and other full bridge
- Half bridge
- PFC and other boost converter
- Buck converter
- Single and two switch forward
- Flyback

Absolute Maximum Ratings

Symbol	Parameter	Ratings	Unit
I_D	Continuous Drain Current @ $T_C = 25^\circ\text{C}$	14	A
	Continuous Drain Current @ $T_C = 100^\circ\text{C}$	9	
I_{DM}	Pulsed Drain Current ^①	56	
V_{GS}	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulse Avalanche Energy ^②	875	mJ
I_{AR}	Avalanche Current, Repetitive or Non-Repetitive	7	A

Thermal and Mechanical Characteristics

Symbol	Characteristic	Min	Typ	Max	Unit
P_D	Total Power Dissipation @ $T_C = 25^\circ\text{C}$			500	W
$R_{\theta JC}$	Junction to Case Thermal Resistance			0.25	$^\circ\text{C/W}$
$R_{\theta CS}$	Case to Sink Thermal Resistance, Flat, Greased Surface		0.11		
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55		150	$^\circ\text{C}$
T_L	Soldering Temperature for 10 Seconds (1.6mm from case)			300	
W_T	Package Weight		0.22		oz
			5.9		g
Torque	Mounting Torque (TO-247 Package), 6-32 or M3 screw			10	in·lbf
				1.1	N·m

Static Characteristics
 $T_J = 25^\circ\text{C}$ unless otherwise specified
APT14F100B S

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{BR(DSS)}$	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	1000			V
$\Delta V_{BR(DSS)}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	Reference to $25^\circ\text{C}, I_D = 250\mu A$		1.15		V/ $^\circ\text{C}$
$R_{DS(on)}$	Drain-Source On Resistance ^③	$V_{GS} = 10V, I_D = 7A$		0.82	0.98	Ω
$V_{GS(th)}$	Gate-Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 1mA$	2.5	4	5	V
$\Delta V_{GS(th)}/\Delta T_J$	Threshold Voltage Temperature Coefficient			-10		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 1000V$ $V_{GS} = 0V$			250	μA
		$T_J = 25^\circ\text{C}$ $T_J = 125^\circ\text{C}$			1000	
I_{GSS}	Gate-Source Leakage Current	$V_{GS} = \pm 30V$			± 100	nA

Dynamic Characteristics
 $T_J = 25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
g_{fs}	Forward Transconductance	$V_{DS} = 50V, I_D = 7A$		16		S
C_{iss}	Input Capacitance	$V_{GS} = 0V, V_{DS} = 25V$ $f = 1MHz$		3965		pF
C_{rss}	Reverse Transfer Capacitance			55		
C_{oss}	Output Capacitance			335		
$C_{o(cr)}^{④}$	Effective Output Capacitance, Charge Related	$V_{GS} = 0V, V_{DS} = 0V \text{ to } 667V$		135		
$C_{o(er)}^{⑤}$	Effective Output Capacitance, Energy Related			70		
Q_g	Total Gate Charge	$V_{GS} = 0 \text{ to } 10V, I_D = 7A,$ $V_{DS} = 500V$		120		nC
Q_{gs}	Gate-Source Charge			21		
Q_{gd}	Gate-Drain Charge			60		
$t_{d(on)}$	Turn-On Delay Time	Resistive Switching $V_{DD} = 667V, I_D = 7A$ $R_G = 4.7\Omega^{⑥}, V_{GG} = 15V$		28		ns
t_r	Current Rise Time			29		
$t_{d(off)}$	Turn-Off Delay Time			95		
t_f	Current Fall Time			26		

Source-Drain Diode Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_S	Continuous Source Current (Body Diode)	MOSFET symbol showing the integral reverse p-n junction diode (body diode)			14	A
I_{SM}	Pulsed Source Current (Body Diode) ^①				56	
V_{SD}	Diode Forward Voltage	$I_{SD} = 7A, T_J = 25^\circ\text{C}, V_{GS} = 0V$			1.2	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 7A^{②}$ $di_{SD}/dt = 100A/\mu s$ $V_{DD} = 100V$	$T_J = 25^\circ\text{C}$	205	240	ns
			$T_J = 125^\circ\text{C}$	355	430	
Q_{rr}	Reverse Recovery Charge		$T_J = 25^\circ\text{C}$	0.90		μC
			$T_J = 125^\circ\text{C}$	2.20		
I_{rrm}	Reverse Recovery Current		$T_J = 25^\circ\text{C}$	8.90		A
			$T_J = 125^\circ\text{C}$	12.90		
dv/dt	Peak Recovery dv/dt	$I_{SD} \leq 7A, di/dt \leq 1000A/\mu s, V_{DD} = 400V,$ $T_J = 125^\circ\text{C}$			25	V/ns

① Repetitive Rating: Pulse width and case temperature limited by maximum junction temperature.

② Starting at $T_J = 25^\circ\text{C}$, $L = 35.71mH$, $R_G = 25\Omega$, $I_{AS} = 7A$.

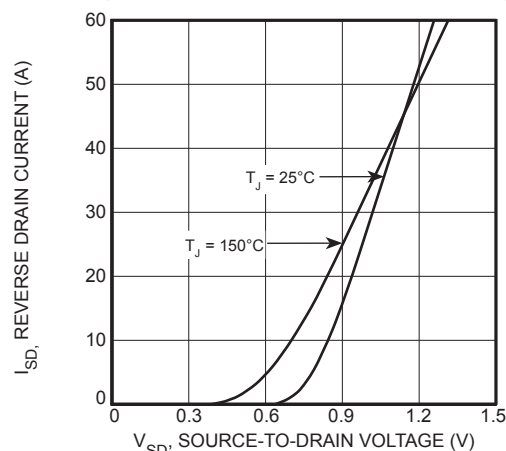
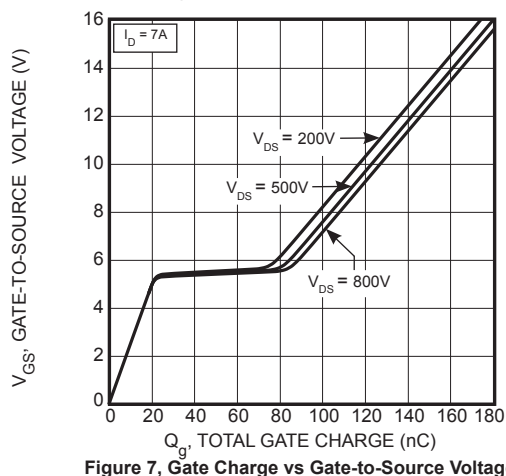
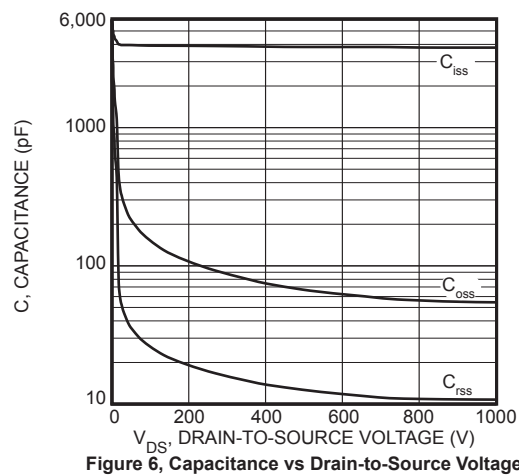
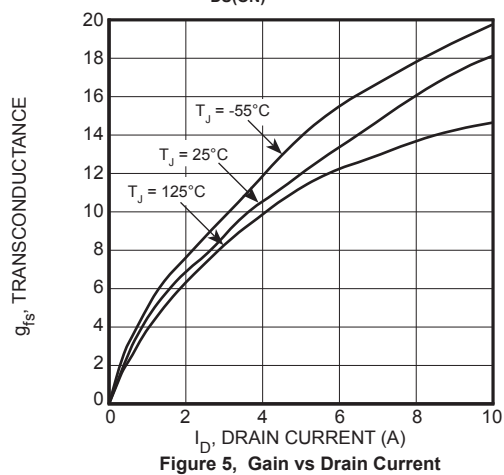
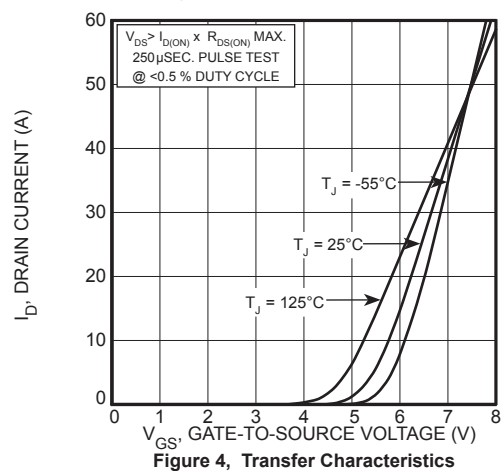
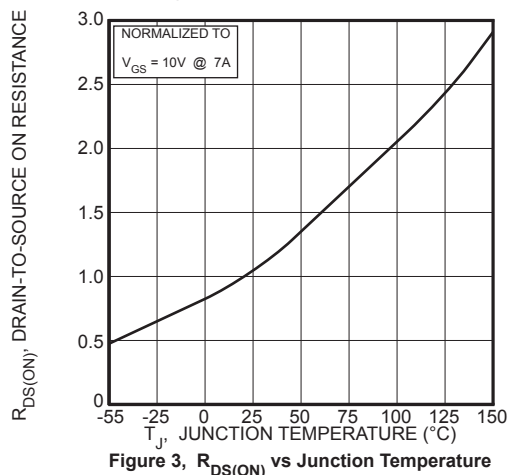
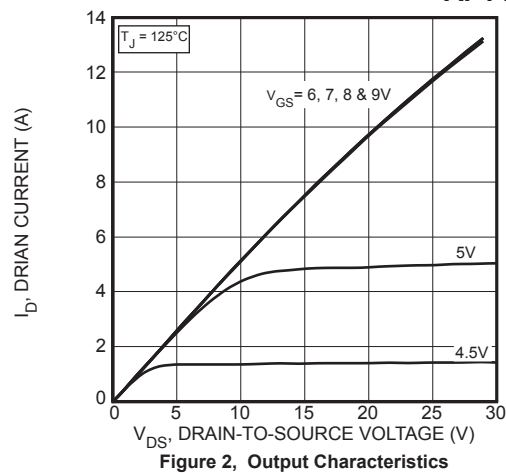
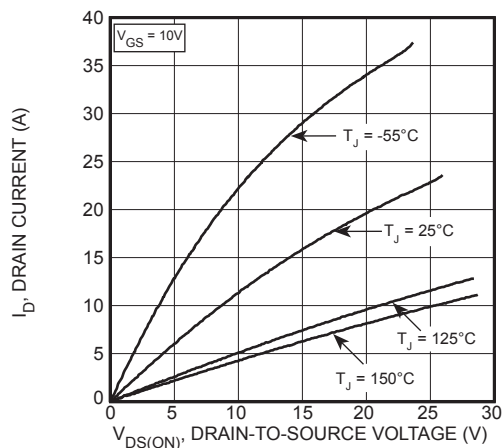
③ Pulse test: Pulse Width < 380 μs , duty cycle < 2%.

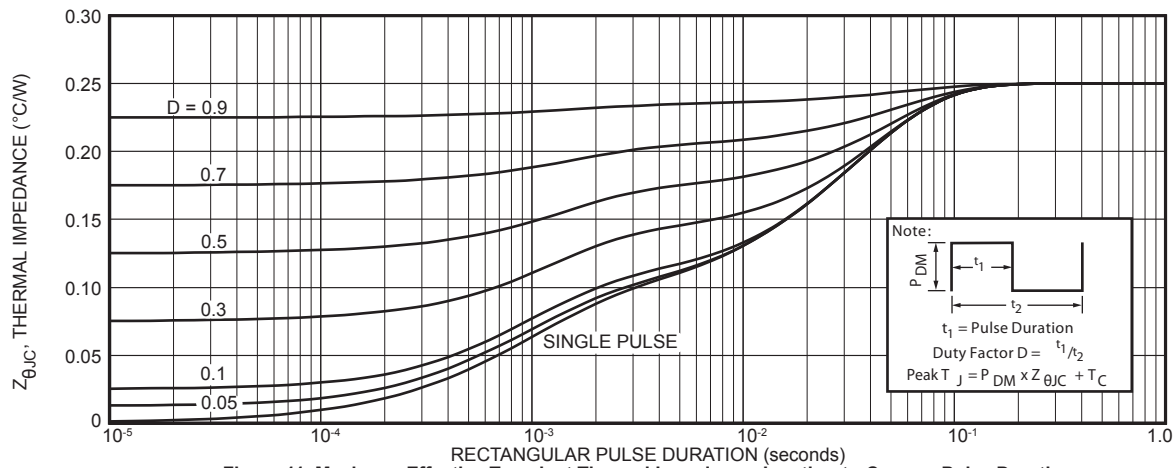
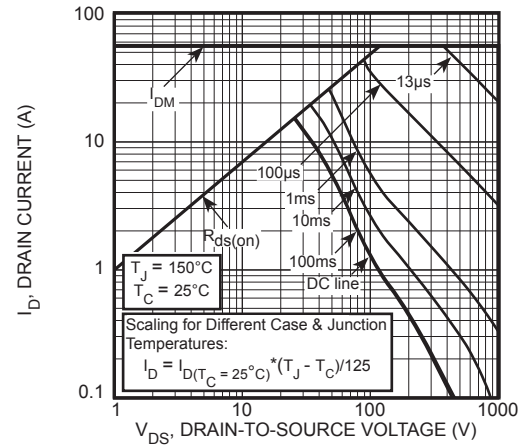
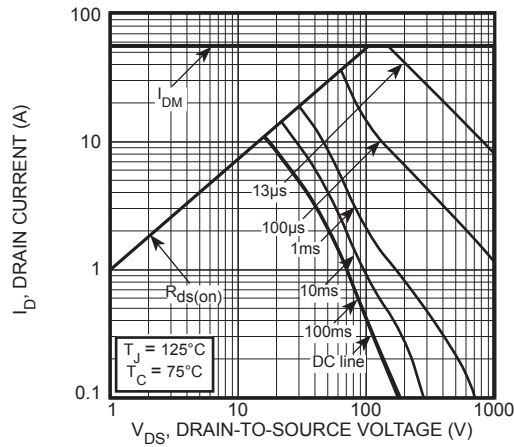
④ $C_{o(cr)}$ is defined as a fixed capacitance with the same stored charge as C_{OSS} with $V_{DS} = 67\%$ of $V_{(BR)DSS}$.

⑤ $C_{o(er)}$ is defined as a fixed capacitance with the same stored energy as C_{OSS} with $V_{DS} = 67\%$ of $V_{(BR)DSS}$. To calculate $C_{o(er)}$ for any value of V_{DS} less than $V_{(BR)DSS}$, use this equation: $C_{o(er)} = -1.15E-7/V_{DS}^2 + 2.03E-8/V_{DS} + 3.93E-11$.

⑥ R_G is external gate resistance, not including internal gate resistance or gate driver impedance. (MIC4452)

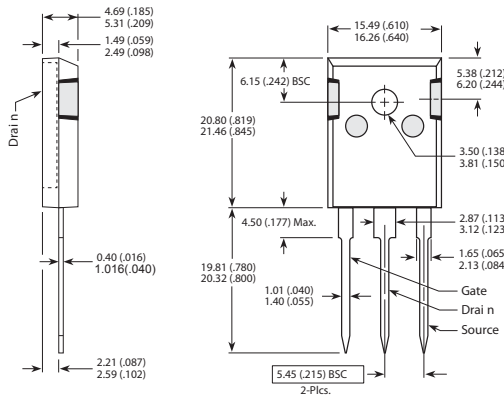
Microsemi reserves the right to change, without notice, the specifications and information contained herein.





TO-247 (B) Package Outline

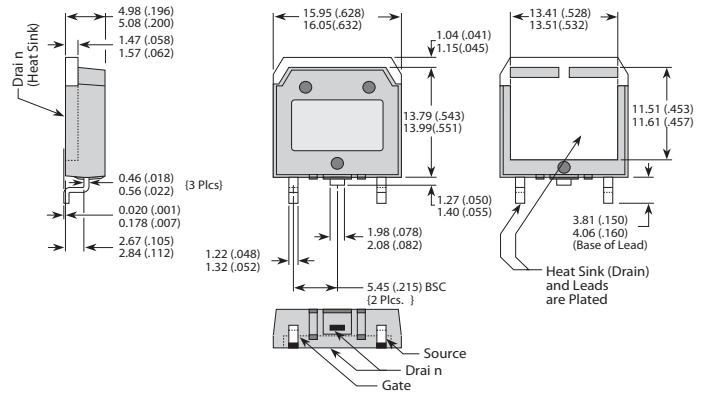
Ⓔ1 SAC: Tin, Silver, Copper



Dimensions in Millimeters (Inches)

D³PAK Package Outline

Ⓔ3 100% Sn Plated



Dimensions in Millimeters (Inches)