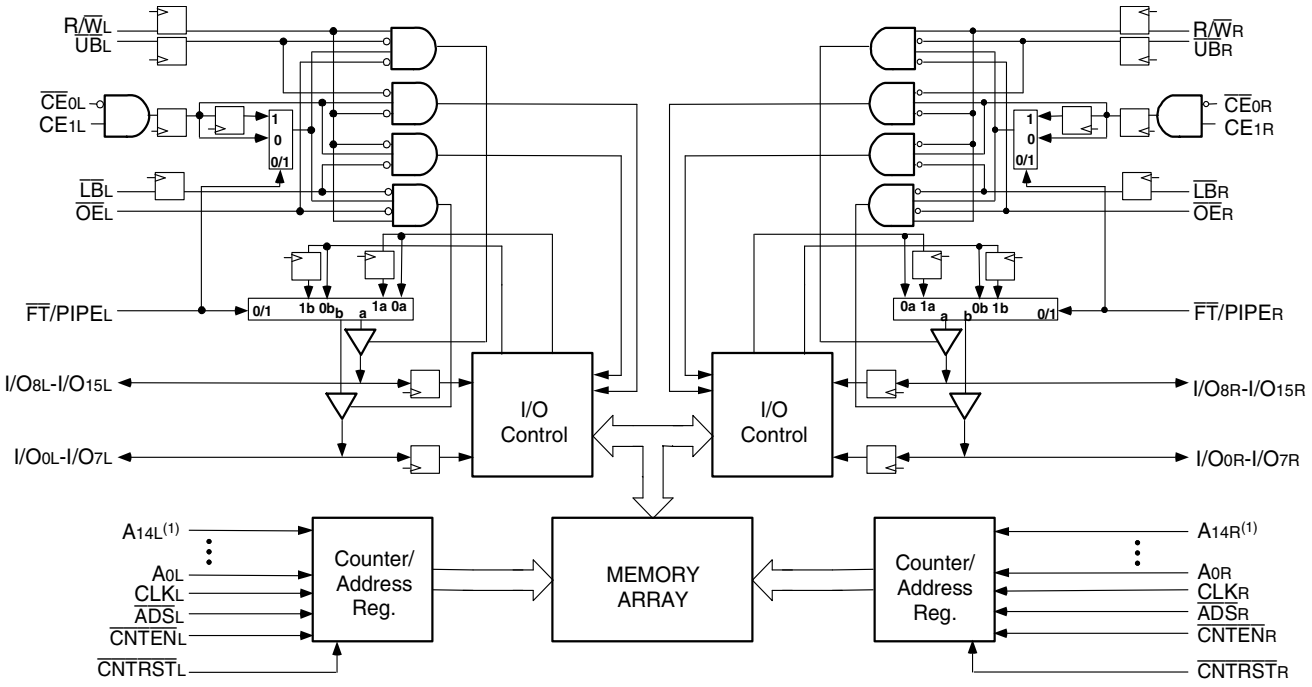
HIGH-SPEED 3.3V 32/16K x 16 SYNCHRONOUS DUAL-PORT STATIC RAM

70V9279/69S/L

Features:

- True Dual-Ported memory cells which allow simultaneous access of the same memory location
- High-speed clock to data access
  - *Commercial: 7.5/9ns (max.)*
  - *Industrial: 7.5ns (max.)*
- Low-power operation
  - *IDT70V9279/69L*
    Active: 429mW (typ.)
    Standby: 1.32mW (typ.)
- Flow-through or Pipelined output mode on either port via the $\overline{FT}$/PIPE pin
- Counter enable and reset features
- Dual chip enables allow for depth expansion without additional logic
- Full synchronous operation on both ports
  - *4ns setup to clock and 1ns hold on all control, data, and address inputs*
  - *Data input, address, and control registers*
  - *Fast 6.5ns clock to data out in the Pipelined output mode*
  - *Self-timed write allows fast cycle time*
  - *10ns cycle time, 100MHz operation in Pipelined output mode*
- Separate upper-byte and lower-byte controls for multiplexed bus and bus matching compatibility
- LVTTL- compatible, single 3.3V (±0.3V) power supply
- Industrial temperature range (–40°C to +85°C) is available for selected speeds
- Available in a 128-pin Thin Quad Flatpack (TQFP) package
- Green parts available, see ordering information

Functional Block Diagram



NOTE:
1. A_{14X} is a NC for IDT70V9269.

AUGUST 2019

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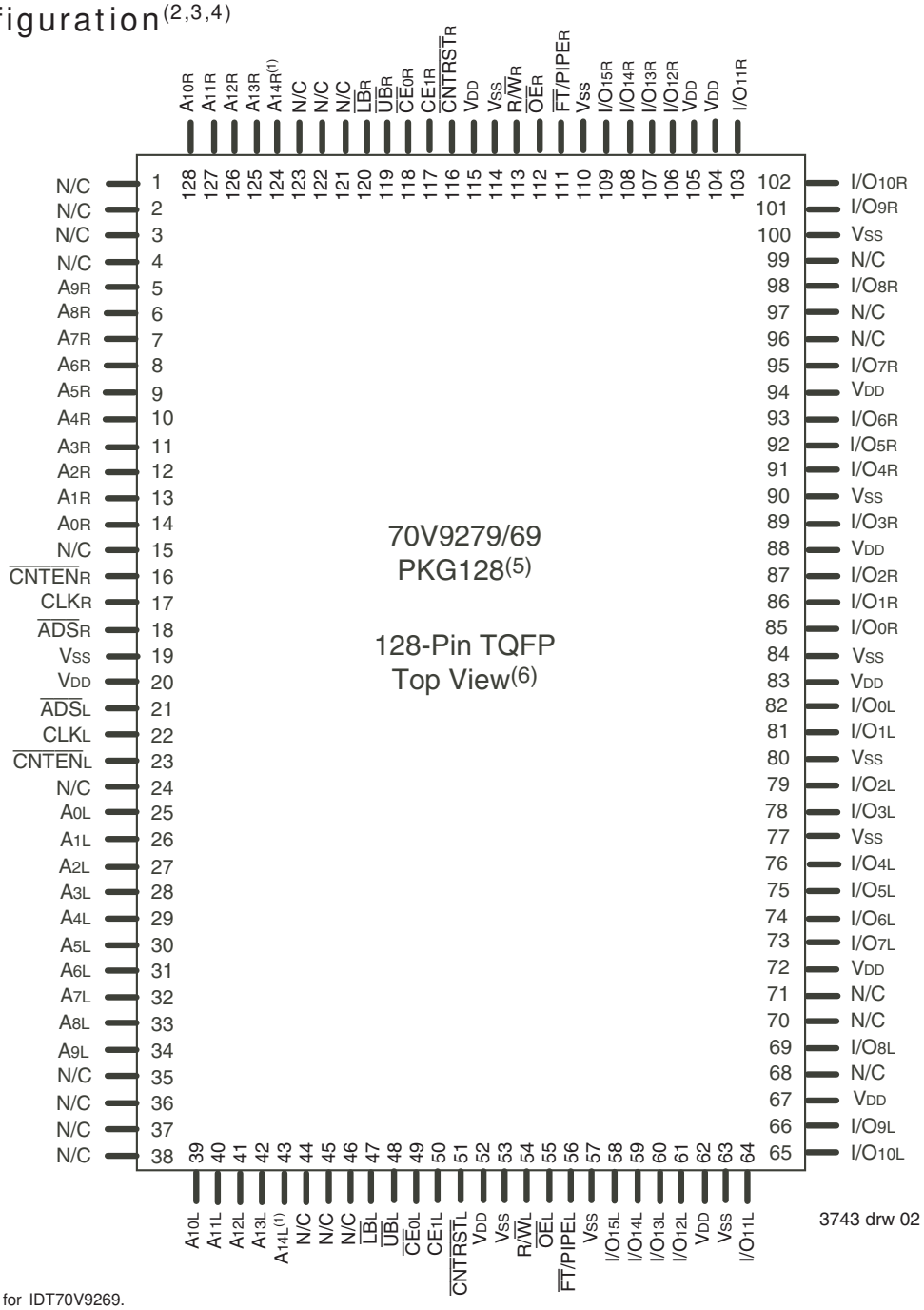
DSC 3743/13

Description:

The IDT70V9279/69 is a high-speed 32/16K x 16 bit synchronous Dual-Port RAM. The memory array utilizes Dual-Port memory cells to allow simultaneous access of any address from both ports. Registers on control, data, and address inputs provide minimal setup and hold times. The timing latitude provided by this approach allows systems to be designed with very short cycle times.

With an input data register, the IDT70V9279/69 has been optimized for applications having unidirectional or bidirectional data flow in bursts. An automatic power down feature, controlled by $\overline{CE}_0$ and CE_1, permits the on-chip circuitry of each port to enter a very low standby power mode. Fabricated using CMOS high-performance technology, these devices typically operate on only 429mW of power.

Pin Configuration[2,3,4]



NOTES:
1. A_{14X} is a NC for IDT70V9269.
2. All V_{DD} pins must be connected to power supply.
3. All V_{SS} pins must be connected to ground.
4. Package body is approximately 14mm x 20mm x 1.4mm.
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part-marking.

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Pin Names

Left Port	Right Port	Names
$\overline{CE}_{0L}$, CE_{1L}	$\overline{CE}_{0R}$, CE_{1R}	Chip Enables[3]
R/$\overline{W}_L$	R/$\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
A_{0L} - A_{14L}[1]	A_{0R} - A_{14R}[1]	Address
I/O_{0L} - I/O_{15L}	I/O_{0R} - I/O_{15R}	Data Input/Output
CLK_L	CLK_R	Clock
$\overline{UB}_L$	$\overline{UB}_R$	Upper Byte Select[2]
$\overline{LB}_L$	$\overline{LB}_R$	Lower Byte Select[2]
$\overline{ADS}_L$	$\overline{ADS}_R$	Address Strobe Enable
$\overline{CNTEN}_L$	$\overline{CNTEN}_R$	Counter Enable
$\overline{CNTRST}_L$	$\overline{CNTRST}_R$	Counter Reset
$\overline{FT}$/$PIPE_L$	$\overline{FT}$/$PIPE_R$	Flow-Through / Pipeline
V_{DD}		Power (3.3V)
V_{SS}		Ground (0V)

3743 tbl 01

NOTES:
1. Address A_{14X} is a NC for IDT70V9269.
2. $\overline{LB}$ and $\overline{UB}$ are single buffered regardless of state of $\overline{FT}$/PIPE.
3. $\overline{CE}_0$ and CE_1 are single buffered when $\overline{FT}$/PIPE = V_{IL}, $\overline{CE}_0$ and CE_1 are double buffered when $\overline{FT}$/PIPE = V_{IH}, i.e. the signals take two cycles to deselect.

Truth Table I—Read/Write and Enable Control[1,2,3]

$\overline{OE}$	CLK	$\overline{CE}_0$[5]	CE_1[5]	$\overline{UB}$[4]	$\overline{LB}$[4]	R/$\overline{W}$	Upper Byte I/O_{8-15}	Lower Byte I/O_{0-7}	MODE
X	↑	H	X	X	X	X	High-Z	High-Z	Deselected–Power Down
X	↑	X	L	X	X	X	High-Z	High-Z	Deselected–Power Down
X	↑	L	H	H	H	X	High-Z	High-Z	Both Bytes Deselected
X	↑	L	H	L	H	L	D_{IN}	High-Z	Write to Upper Byte Only
X	↑	L	H	H	L	L	High-Z	$DATA_{IN}$	Write to Lower Byte Only
X	↑	L	H	L	L	L	$DATA_{IN}$	$DATA_{IN}$	Write to Both Bytes
L	↑	L	H	L	H	H	$DATA_{OUT}$	High-Z	Read Upper Byte Only
L	↑	L	H	H	L	H	High-Z	$DATA_{OUT}$	Read Lower Byte Only
L	↑	L	H	L	L	H	$DATA_{OUT}$	$DATA_{OUT}$	Read Both Bytes
H	↑	L	H	L	L	X	High-Z	High-Z	Outputs Disabled

3743 tbl 02

NOTES:
1. "H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care.
2. $\overline{ADS}$, $\overline{CNTEN}$, $\overline{CNTRST}$ = X.
3. $\overline{OE}$ is an asynchronous input signal.
4 $\overline{LB}$ and $\overline{UB}$ are single buffered regardless of state of $\overline{FT}$/PIPE.
5. $\overline{CE}_0$ and CE_1 are single buffered when $\overline{FT}$/PIPE = V_{IL}. $\overline{CE}_0$ and CE_1 are double buffered when $\overline{FT}$/PIPE = V_{IH}, i.e. the signals take two cycles to deselect.

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Truth Table II—Address Counter Control(1,2,3)

External Address	Previous Internal Address	Internal Address Used	CLK	$\overline{ADS}$	$\overline{CNTEN}$	$\overline{CNTRST}$	I/O(3)	MODE
An	X	An	↑	L(4)	X	H	DI/O (n)	External Address Used
X	An	An + 1	↑	H	L(5)	H	DI/O(n+1)	Counter Enabled—Internal Address generation
X	An + 1	An + 1	↑	H	H	H	DI/O(n+1)	External Address Blocked—Counter disabled (An + 1 reused)
X	X	A0	↑	X	X	L(4)	DI/O(0)	Counter Reset to Address 0

3743 tbl 03

NOTES:
1. "H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care.
2. $\overline{CE_0}$, $\overline{LB}$, $\overline{UB}$, and $\overline{OE}$ = V_{IL}; CE_1 and R/$\overline{W}$ = V_{IH}.
3. Outputs configured in Flow-Through Output mode; if outputs are in Pipelined mode the data out will be delayed by one cycle.
4. $\overline{ADS}$ and $\overline{CNTRST}$ are independent of all other signals including $\overline{CE_0}$, CE_1, $\overline{UB}$ and $\overline{LB}$.
5. The address counter advances if $\overline{CNTEN}$ = V_{IL} on the rising edge of CLK, regardless of all other signals including $\overline{CE_0}$, CE_1, $\overline{UB}$ and $\overline{LB}$.

Recommended Operating Temperature and Supply Voltage(1,2)

Grade	Ambient Temperature	GND	VDD
Commercial	0°C to +70°C	0V	3.3V ± 0.3V
Industrial	-40°C to +85°C	0V	3.3V ± 0.3V

3743 tbl 04

NOTES:
1. Industrial temperature: for specific speeds, packages and powers contact your sales office.
2. This is the parameter TA. This is the "instant on" case temperature.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD	Supply Voltage	3.0	3.3	3.6	V
VSS	Ground	0	0	0	V
VIH	Input High Voltage	2.2	—	VDD+0.3V(2)	V
VIL	Input Low Voltage	-0.3(1)	—	0.8	V

3743 tbl 05

NOTES:
1. $V_{IL} \geq$ -1.5V for pulse width less than 10 ns.
2. VTERM must not exceed VDD + 0.3V.

Absolute Maximum Ratings(1)

Symbol	Rating	Commercial & Industrial	Unit
VTERM(2)	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
TBIAS(3)	Temperature Under Bias	-55 to +125	°C
TSTG	StorageTemperature	-65 to +150	°C
TJN	Junction Temperature	+150	°C
IOUT	DC Output Current	50	mA

3743 tbl 06

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VTERM must not exceed VDD + 0.3V for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of $V_{TERM} \geq V_{DD}$ + 0.3V.
3. Ambient Temperature Under DC Bias. No AC Conditions. Chip Deselected.

Capacitance(1)
(TA = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	9	pF
COUT(2)	Output Capacitance	VOUT = 0V	10	pF

3743 tbl 07

NOTES:
1. These parameters are determined by device characterization, but are not production tested.
2. COUT also references CI/O.

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DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{DD} = 3.3V ± 0.3V)

Symbol	Parameter	Test Conditions	70V9279/69S		70V9279/69L		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current[1]	V_{DD} = 3.6V, V_{IN} = 0V to V_{DD}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE0}$ = V_{IH} or CE_1 = V_{IL}, V_{OUT} = 0V to V_{DD}	—	10	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = +4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

3743 tbl 08

NOTE:
1. At V_{DD} ≤ 2.0V input leakages are undefined.

DC Electrical Characteristics Over the Operating Temperature Supply Voltage Range[3,6] (V_{DD} = 3.3V ± 0.3V)

Symbol	Parameter	Test Condition	Version		70V9279/69X6 Com'l Only		70V9279/69X7 Com'l & Ind		70V9279/69X9 Com'l Only		Unit
					Typ.[4]	Max.	Typ.[4]	Max.	Typ.[4]	Max.	
I_{DD}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}_L$ and $\overline{CE}_R$= V_{IL}, Outputs Disabled, f = f_{MAX}[1]	COM'L	S	220	395	200	335	180	260	mA
				L	220	350	200	290	180	225	
			IND	S	—	—	200	370	—	—	
				L	—	—	200	335	—	—	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ = $\overline{CE}_R$ = V_{IH} f = f_{MAX}[1]	COM'L	S	70	145	60	115	50	75	mA
				L	70	130	60	100	50	65	
			IND	S	—	—	60	130	—	—	
				L	—	—	60	115	—	—	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}$"A" = V_{IL} and $\overline{CE}$"B" = V_{IH}[5] Active Port Outputs Disabled, f=f_{MAX}[1]	COM'L	S	150	280	130	240	110	170	mA
				L	150	250	130	210	110	150	
			IND	S	—	—	130	265	—	—	
				L	—	—	130	240	—	—	
I_{SB3}	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{DD} - 0.2V, V_{IN} ≥ V_{DD} - 0.2V or V_{IN} ≤ 0.2V, f = 0[2]	COM'L	S	1.0	5	1.0	5	1.0	5	mA
				L	0.4	3	0.4	3	0.4	3	
			IND	S	—	—	1.0	20	—	—	
				L	—	—	0.4	15	—	—	
I_{SB4}	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}$"A" ≤ 0.2V and $\overline{CE}$"B" ≥ V_{DD} - 0.2V[5] V_{IN} ≥ V_{DD} - 0.2V or V_{IN} ≤ 0.2V, Active Port, Outputs Disabled, f = f_{MAX}[1]	COM'L	S	140	270	120	230	100	160	mA
				L	140	240	120	200	100	140	
			IND	S	—	—	120	255	—	—	
				L	—	—	120	230	—	—	

3743 tbl 09a

NOTES:
1. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of 1/t_{CYC}, using "AC TEST CONDITIONS" at input levels of V_{SS} to 3V.
2. f = 0 means no address, clock, or control lines change. Applies only to input at CMOS level standby.
3. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
4. V_{DD} = 3.3V, T_A = 25°C for Typ, and are not production tested. $I_{DD\,DC}$(f=0) = 90mA (Typ).
5. $\overline{CE}_X$ = V_{IL} means $\overline{CE}_{0X}$ = V_{IL} and CE_{1X} = V_{IH}
   $\overline{CE}_X$ = V_{IH} means $\overline{CE}_{0X}$ = V_{IH} or CE_{1X} = V_{IL}
   $\overline{CE}_X$ ≤ 0.2V means $\overline{CE}_{0X}$ ≤ 0.2V and CE_{1X} ≥ V_{DD} - 0.2V
   $\overline{CE}_X$ ≥ V_{DD} - 0.2V means $\overline{CE}_{0X}$ ≥ V_{DD} - 0.2V or CE_{1X} ≤ 0.2V
   'X' represents "L" for left port or "R" for right port.
6. 'X' in part numbers indicate power rating (S or L).

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DC Electrical Characteristics Over the Operating Temperature Supply Voltage Range(3,6) (V_{DD} = 3.3V ± 0.3V)(Cont'd)

Symbol	Parameter	Test Condition	Version		70V9279/69X12 Com'l Only Typ.(4)	70V9279/69X12 Com'l Only Max.	70V9279/69X15 Com'l Only Typ.(4)	70V9279/69X15 Com'l Only Max.	Unit
I_{DD}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}_L$ and $\overline{CE}_R$= V_{IL}, Outputs Disabled, f = f_{MAX}(1)	COM'L	S	150	240	130	220	mA
				L	150	205	130	185	
			IND	S	—	—	—	—	
				L	—	—	—	—	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ = $\overline{CE}_R$ = V_{IH} f = f_{MAX}(1)	COM'L	S	40	65	30	55	mA
				L	40	50	30	35	
			IND	S	—	—	—	—	
				L	—	—	—	—	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_{"A"}$ = V_{IL} and $\overline{CE}_{"B"}$ = V_{IH}(5) Active Port Outputs Disabled, f=f_{MAX}(1)	COM'L	S	100	160	90	150	mA
				L	100	140	90	130	
			IND	S	—	—	—	—	
				L	—	—	—	—	
I_{SB3}	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{DD} - 0.2V, V_{IN} ≥ V_{DD} - 0.2V or V_{IN} ≤ 0.2V, f = 0(2)	COM'L	S	1.0	5	1.0	5	mA
				L	0.4	3	0.4	3	
			IND	S	—	—	—	—	
				L	—	—	—	—	
I_{SB4}	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}_{"A"}$ ≤ 0.2V and $\overline{CE}_{"B"}$ ≥ V_{DD} - 0.2V(5) V_{IN} ≥ V_{DD} - 0.2V or V_{IN} ≤ 0.2V, Active Port, Outputs Disabled, f = f_{MAX}(1)	COM'L	S	90	150	80	140	mA
				L	90	130	80	120	
			IND	S	—	—	—	—	
				L	—	—	—	—	

3743 tbl 09b

NOTES:

1. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of 1/t_{CYC}, using "AC TEST CONDITIONS" at input levels of V_{SS} to 3V.
2. f = 0 means no address, clock, or control lines change. Applies only to input at CMOS level standby.
3. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
4. V_{DD} = 3.3V, T_A = 25°C for Typ, and are not production tested. $I_{DD\,DC}$(f=0) = 90mA (Typ).
5. $\overline{CE}_X$ = V_{IL} means $\overline{CE}_{0X}$ = V_{IL} and CE_{1X} = V_{IH}
   $\overline{CE}_X$ = V_{IH} means $\overline{CE}_{0X}$ = V_{IH} or CE_{1X} = V_{IL}
   $\overline{CE}_X$ ≤ 0.2V means $\overline{CE}_{0X}$ ≤ 0.2V and CE_{1X} ≥ V_{DD} - 0.2V
   $\overline{CE}_X$ ≥ V_{DD} - 0.2V means $\overline{CE}_{0X}$ ≥ V_{DD} - 0.2V or CE_{1X} ≤ 0.2V
   'X' represents "L" for left port or "R" for right port.
6. 'X' in part numbers indicate power rating (S or L).

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AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1, 2, and 3

7343 tbl 10

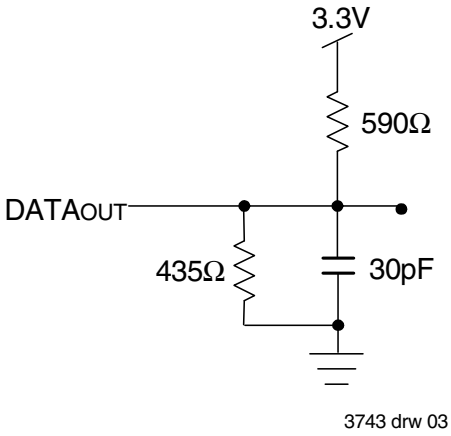


Figure 1. AC Output Test load.

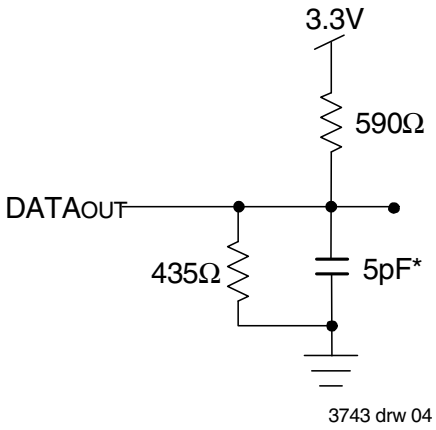


Figure 2. Output Test Load
(For t_{CKLZ}, t_{CKHZ}, t_{OLZ}, and t_{OHZ}).
*Including scope and jig.

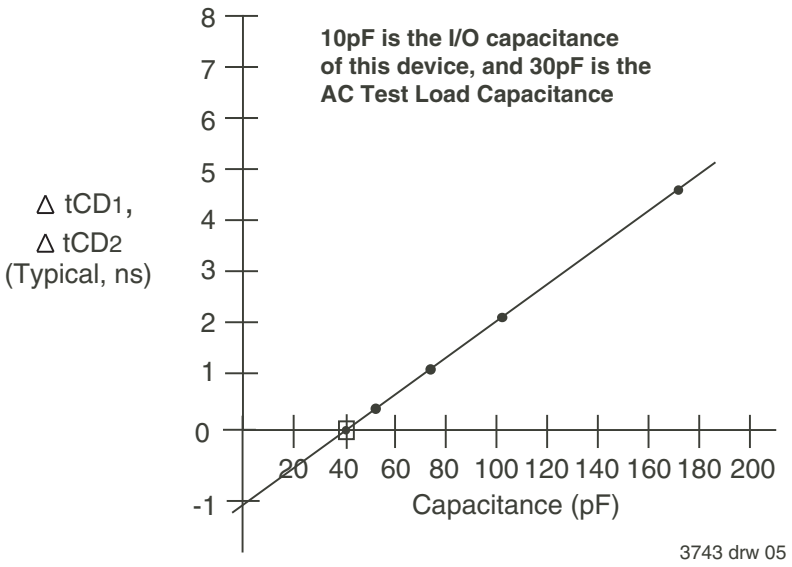


Figure 3. Typical Output Derating (Lumped Capacitive Load).

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AC Electrical Characteristics Over the Operating Temperature Range (Read and Write Cycle Timing)[3,4] (V_{DD} = 3.3V ± 0.3V, T_A = 0°C to +70°C)

		70V9279/69X6 Com'l Only		70V9279/69X7 Com'l & Ind		70V9279/69X9 Com'l Only		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{CYC1}	Clock Cycle Time (Flow-Through)[2]	19	—	22	—	25	—	ns
t_{CYC2}	Clock Cycle Time (Pipelined)[2]	10	—	12	—	15	—	ns
t_{CH1}	Clock High Time (Flow-Through)[2]	6.5	—	7.5	—	12	—	ns
t_{CL1}	Clock Low Time (Flow-Through)[2]	6.5	—	7.5	—	12	—	ns
t_{CH2}	Clock High Time (Pipelined)[2]	4	—	5	—	6	—	ns
t_{CL2}	Clock Low Time (Pipelined)[2]	4	—	5	—	6	—	ns
t_R	Clock Rise Time	—	3	—	3	—	3	ns
t_F	Clock Fall Time	—	3	—	3	—	3	ns
t_{SA}	Address Setup Time	3.5	—	4	—	4	—	ns
t_{HA}	Address Hold Time	0	—	0	—	1	—	ns
t_{SC}	Chip Enable Setup Time	3.5	—	4	—	4	—	ns
t_{HC}	Chip Enable Hold Time	0	—	0	—	1	—	ns
t_{SW}	R/W Setup Time	3.5	—	4	—	4	—	ns
t_{HW}	R/W Hold Time	0	—	0	—	1	—	ns
t_{SD}	Input Data Setup Time	3.5	—	4	—	4	—	ns
t_{HD}	Input Data Hold Time	0	—	0	—	1	—	ns
t_{SAD}	$\overline{ADS}$ Setup Time	3.5	—	4	—	4	—	ns
t_{HAD}	$\overline{ADS}$ Hold Time	0	—	0	—	1	—	ns
t_{SCN}	$\overline{CNTEN}$ Setup Time	3.5	—	4	—	4	—	ns
t_{HCN}	$\overline{CNTEN}$ Hold Time	0	—	0	—	1	—	ns
t_{SRST}	$\overline{CNTRST}$ Setup Time	3.5	—	4	—	4	—	ns
t_{HRST}	$\overline{CNTRST}$ Hold Time	0	—	0	—	1	—	ns
t_{OE}	Output Enable to Data Valid	—	6.5	—	7.5	—	9	ns
t_{OLZ}	Output Enable to Output Low-Z[1]	2	—	2	—	2	—	ns
t_{OHZ}	Output Enable to Output High-Z[1]	1	7	1	7	1	7	ns
t_{CD1}	Clock to Data Valid (Flow-Through)[2]	—	15	—	18	—	20	ns
t_{CD2}	Clock to Data Valid (Pipelined)[2]	—	6.5	—	7.5	—	9	ns
t_{DC}	Data Output Hold After Clock High	2	—	2	—	2	—	ns
t_{CKHZ}	Clock High to Output High-Z[1]	2	9	2	9	2	9	ns
t_{CKLZ}	Clock High to Output Low-Z[1]	2	—	2	—	2	—	ns
Port-to-Port Delay								
t_{CWDD}	Write Port Clock High to Read Data Delay	—	24	—	28	—	35	ns
t_{CCS}	Clock-to-Clock Setup Time	—	9	—	10	—	15	ns

3743 tbl 11a

NOTES:
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2). This parameter is guaranteed by device characterization, but is not production tested.
2. The Pipelined output parameters (t_{CYC2}, t_{CD2}) apply to either or both left and right ports when $\overline{FT}$/PIPE = V_{IH}. Flow-through parameters (t_{CYC1}, t_{CD1}) apply when $\overline{FT}$/PIPE = V_{IL} for that port.
3. All input signals are synchronous with respect to the clock except for the asynchronous Output Enable ($\overline{OE}$) and $\overline{FT}$/PIPE. $\overline{FT}$/PIPE should be treated as a DC signal, i.e. steady state during operation.
4. 'X' in part number indicates power rating (S or L).

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AC Electrical Characteristics Over the Operating Temperature Range (Read and Write Cycle Timing)[3,4] (V_{DD} = 3.3V ± 0.3V, T_A = 0°C to +70°C)(Cont'd)

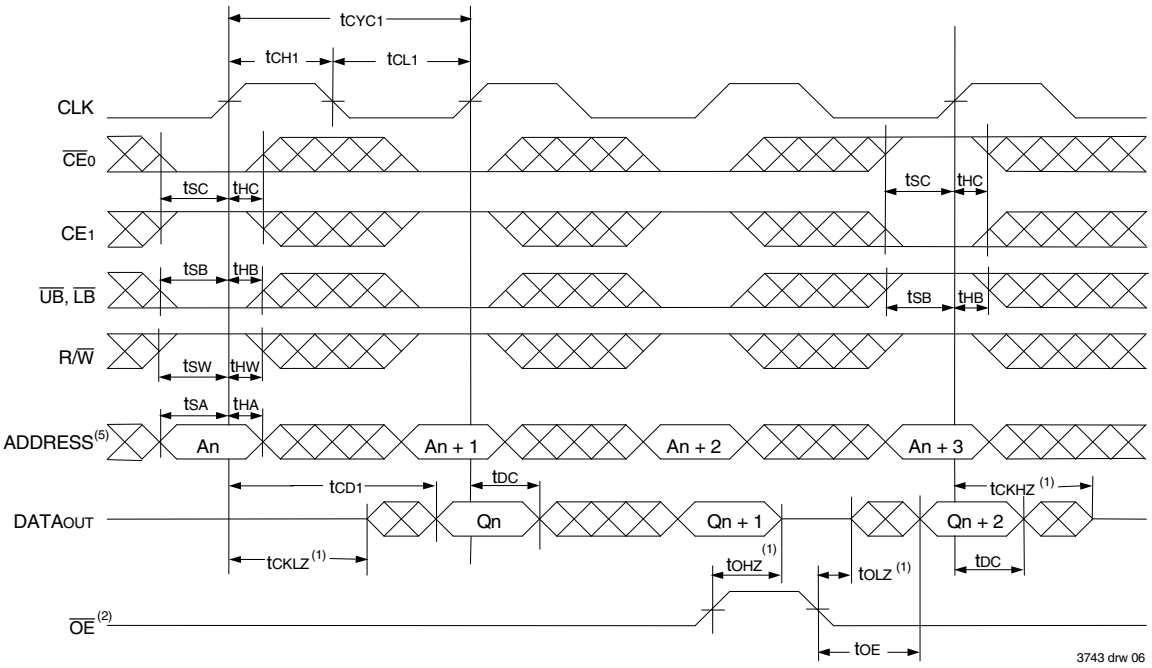
		70V9279/69X12 Com'l Only		70V9279/69X15 Com'l Only		
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
t_{CYC1}	Clock Cycle Time (Flow-Through)[2]	30	—	35	—	ns
t_{CYC2}	Clock Cycle Time (Pipelined)[2]	20	—	25	—	ns
t_{CH1}	Clock High Time (Flow-Through)[2]	12	—	12	—	ns
t_{CL1}	Clock Low Time (Flow-Through)[2]	12	—	12	—	ns
t_{CH2}	Clock High Time (Pipelined)[2]	8	—	10	—	ns
t_{CL2}	Clock Low Time (Pipelined)[2]	8	—	10	—	ns
t_R	Clock Rise Time	—	3	—	3	ns
t_F	Clock Fall Time	—	3	—	3	ns
t_{SA}	Address Setup Time	4	—	4	—	ns
t_{HA}	Address Hold Time	1	—	1	—	ns
t_{SC}	Chip Enable Setup Time	4	—	4	—	ns
t_{HC}	Chip Enable Hold Time	1	—	1	—	ns
t_{SW}	R/W Setup Time	4	—	4	—	ns
t_{HW}	R/W Hold Time	1	—	1	—	ns
t_{SD}	Input Data Setup Time	4	—	4	—	ns
t_{HD}	Input Data Hold Time	1	—	1	—	ns
t_{SAD}	$\overline{ADS}$ Setup Time	4	—	4	—	ns
t_{HAD}	$\overline{ADS}$ Hold Time	1	—	1	—	ns
t_{SCN}	$\overline{CNTEN}$ Setup Time	4	—	4	—	ns
t_{HCN}	$\overline{CNTEN}$ Hold Time	1	—	1	—	ns
t_{SRST}	$\overline{CNTRST}$ Setup Time	4	—	4	—	ns
t_{HRST}	$\overline{CNTRST}$ Hold Time	1	—	1	—	ns
t_{OE}	Output Enable to Data Valid	—	12	—	15	ns
t_{OLZ}	Output Enable to Output Low-Z[1]	2	—	2	—	ns
t_{OHZ}	Output Enable to Output High-Z[1]	1	7	1	7	ns
t_{CD1}	Clock to Data Valid (Flow-Through)[2]	—	25	—	30	ns
t_{CD2}	Clock to Data Valid (Pipelined)[2]	—	12	—	15	ns
t_{DC}	Data Output Hold After Clock High	2	—	2	—	ns
t_{CKHZ}	Clock High to Output High-Z[1]	2	9	2	9	ns
t_{CKLZ}	Clock High to Output Low-Z[1]	2	—	2	—	ns
Port-to-Port Delay						
t_{CWDD}	Write Port Clock High to Read Data Delay	—	40	—	50	ns
t_{CCS}	Clock-to-Clock Setup Time	—	15	—	20	ns

3743 tbl 11b

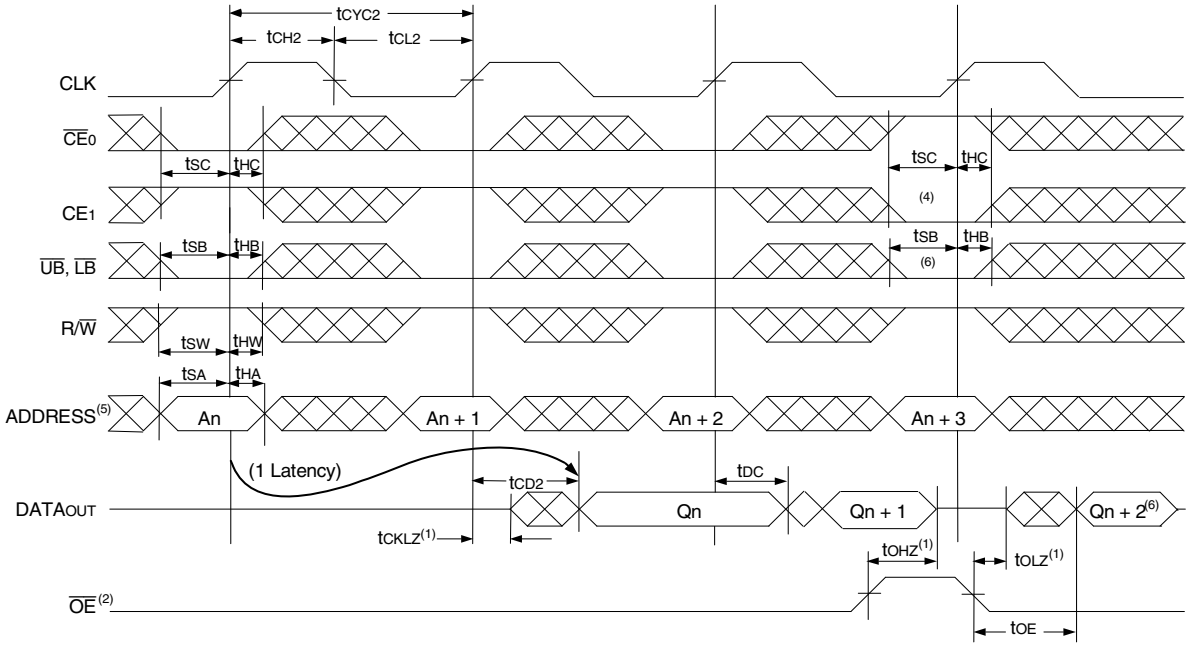
NOTES:
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2). This parameter is guaranteed by device characterization, but is not production tested.
2. The Pipelined output parameters (t_{CYC2}, t_{CD2}) apply to either or both left and right ports when $\overline{FT}$/PIPE = V_{IH}. Flow-through parameters (t_{CYC1}, t_{CD1}) apply when $\overline{FT}$/PIPE = V_{IL} for that port.
3. All input signals are synchronous with respect to the clock except for the asynchronous Output Enable ($\overline{OE}$) and $\overline{FT}$/PIPE. $\overline{FT}$/PIPE should be treated as a DC signal, i.e. steady state during operation.
4. 'X' in part number indicates power rating (S or L).

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Timing Waveform of Read Cycle for Flow-through Output ($\overline{FT}$/PIPE"X" = VIL)(3,7)



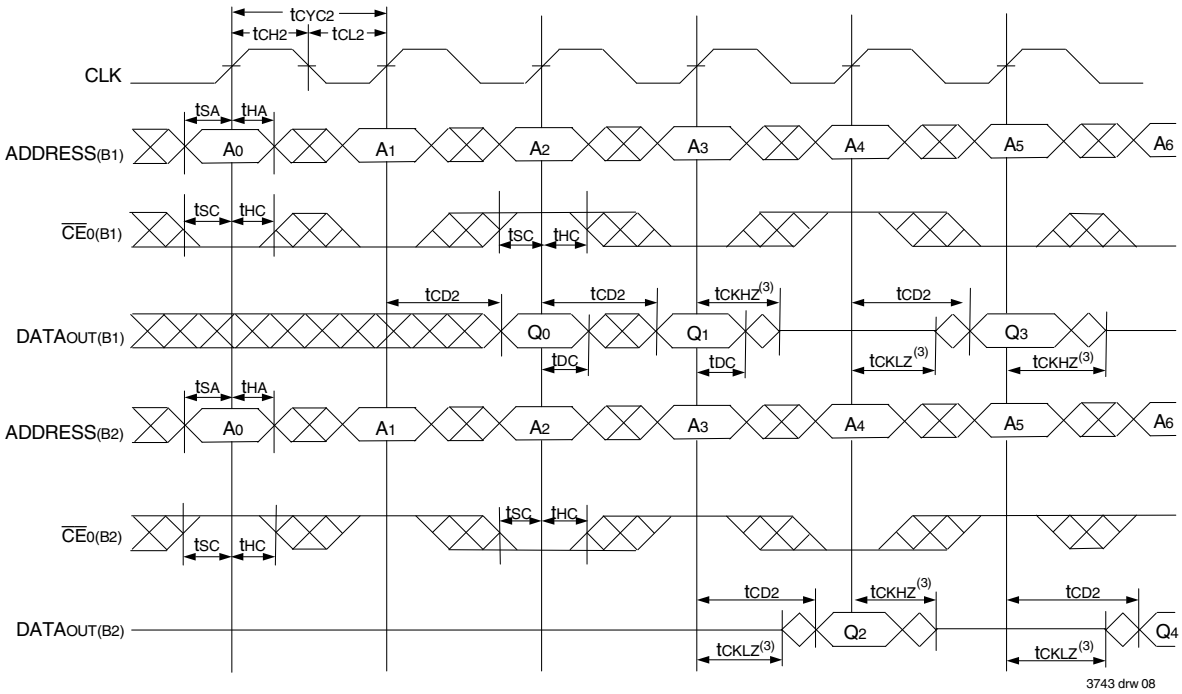
Timing Waveform of Read Cycle for Pipelined Output ($\overline{FT}$/PIPE"X" = VIH)(3,7)



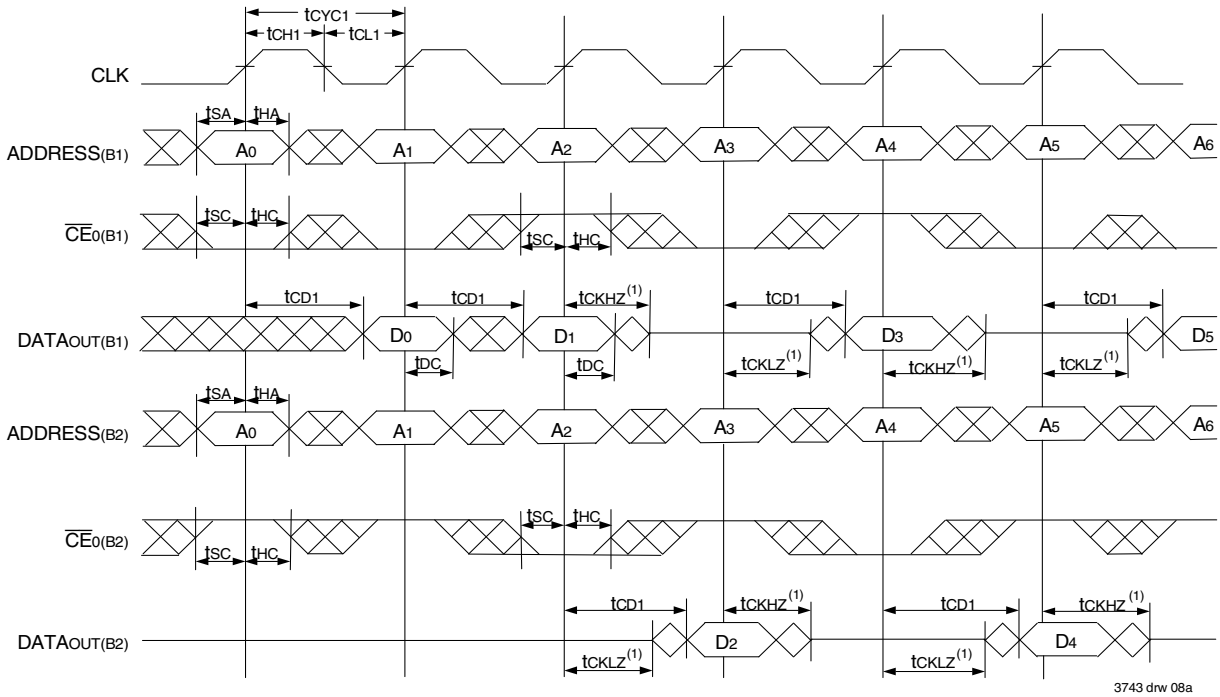
NOTES:
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. $\overline{OE}$ is asynchronously controlled; all other inputs are synchronous to the rising clock edge.
3. $\overline{ADS}$ = VIL, $\overline{CNTEN}$ and $\overline{CNTRST}$ = VIH.
4. The output is disabled (High-Impedance state) by $\overline{CE}_0$ = VIH or CE1 = VIL following the next rising edge of the clock. Refer to Truth Table 1.
5. Addresses do not have to be accessed sequentially since ADS = VIL constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
6. If $\overline{UB}$ or $\overline{LB}$ was HIGH, then the Upper Byte and/or Lower Byte of DATAOUT for Qn + 2 would be disabled (High-Impedance state).
7. "x" denotes Left or Right port. The diagram is with respect to that port.

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Timing Waveform of a Bank Select Pipelined Read(1,2)



Timing Waveform of a Bank Select Flow-Through Read(6)

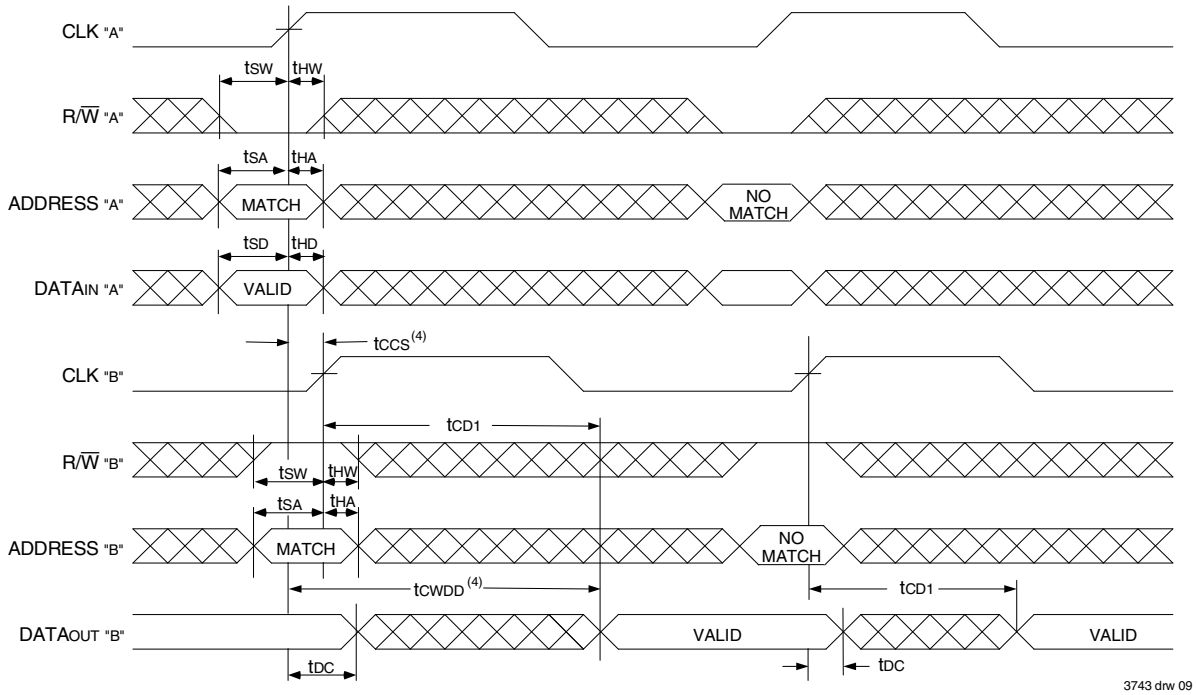


NOTES:

1. B1 Represents Bank #1; B2 Represents Bank #2. Each Bank consists of one IDT70V9279/69 for this waveform, and are setup for depth expansion in this example. ADDRESS(B1) = ADDRESS(B2) in this situation.
2. $\overline{UB}$, $\overline{LB}$, $\overline{OE}$, and $\overline{ADS}$ = V_{IL}; $CE_{1(B1)}$, $CE_{1(B2)}$, R/$\overline{W}$, $\overline{CNTEN}$, and $\overline{CNTRST}$ = V_{IH}.
3. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
4. $\overline{CE}_0$, $\overline{UB}$, $\overline{LB}$, and $\overline{ADS}$ = V_{IL}; CE_1, $\overline{CNTEN}$, and $\overline{CNTRST}$ = V_{IH}.
5. $\overline{OE}$ = V_{IL} for the Right Port, which is being read from. $\overline{OE}$ = V_{IH} for the Left Port, which is being written to.
6. If $t_{CCS} \leq$ maximum specified, then data from right port READ is not valid until the maximum specified for t_{CWDD}.
   If t_{CCS} > maximum specified, then data from right port READ is not valid until $t_{CCS} + t_{CD1}$. t_{CWDD} does not apply in this case.

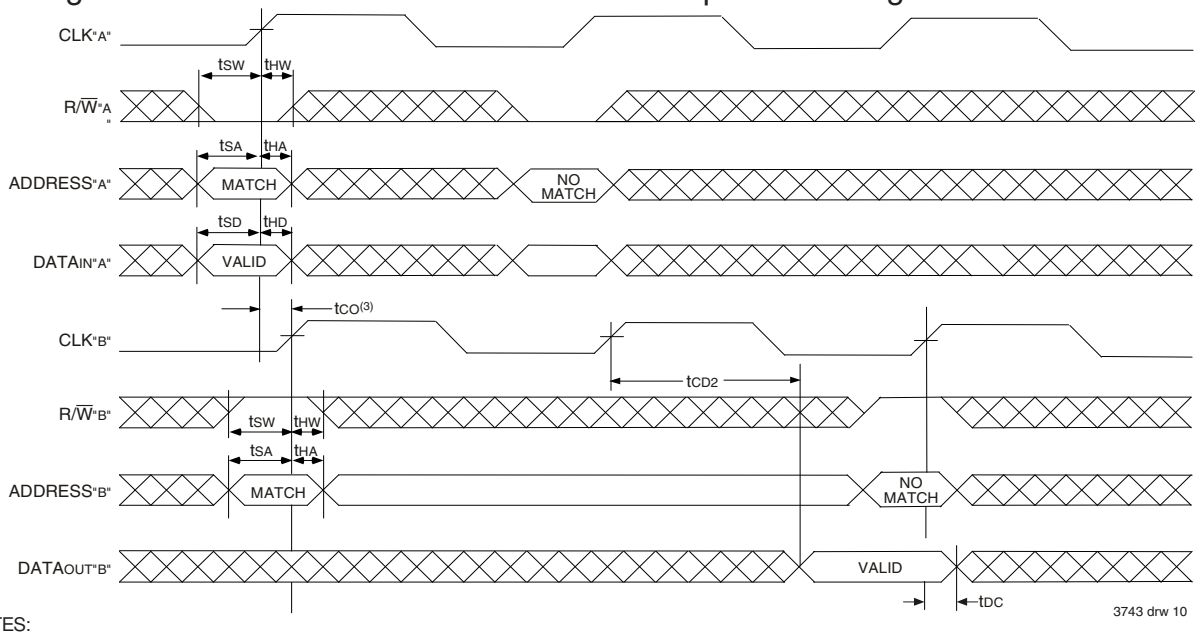
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Timing Waveform with Port-to-Port Flow-Through Read(1,2,3,5)



NOTES:
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. $\overline{CE_0}$, $\overline{UB}$, $\overline{LB}$, and $\overline{ADS}$ = V_{IL}; CE_1, $\overline{CNTEN}$, and $\overline{CNTRST}$ = V_{IH}.
3. $\overline{OE}$ = V_{IL} for the Right Port, which is being read from. $\overline{OE}$ = V_{IH} for the Left Port, which is being written to.
4. If $t_{CCS} \leq$ maximum specified, then data from right port READ is not valid until the maximum specified for t_{CWDD}.
   If t_{CCS} > maximum specified, then data from right port READ is not valid until $t_{CCS} + t_{CD1}$. t_{CWDD} does not apply in this case.
5. All timing is the same for both left and right ports. Port "A" may be either left or right port. Port "B" is the opposite of Port "A".

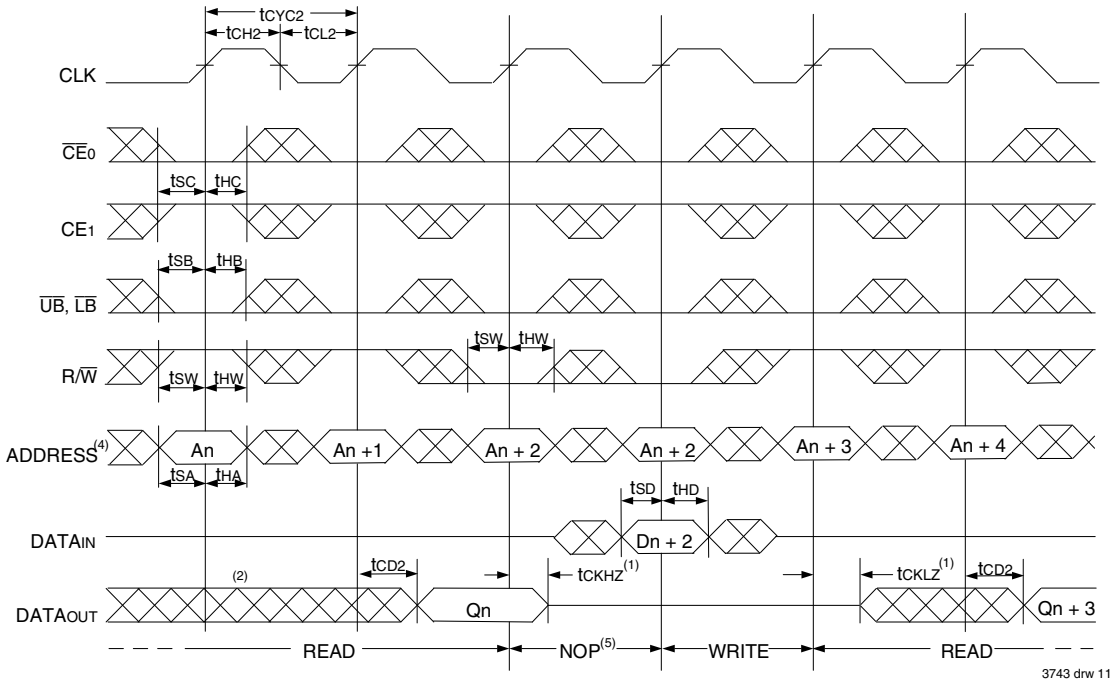
Timing Waveform of Left Port Write to Pipelined Right Port Read(1,2,4)



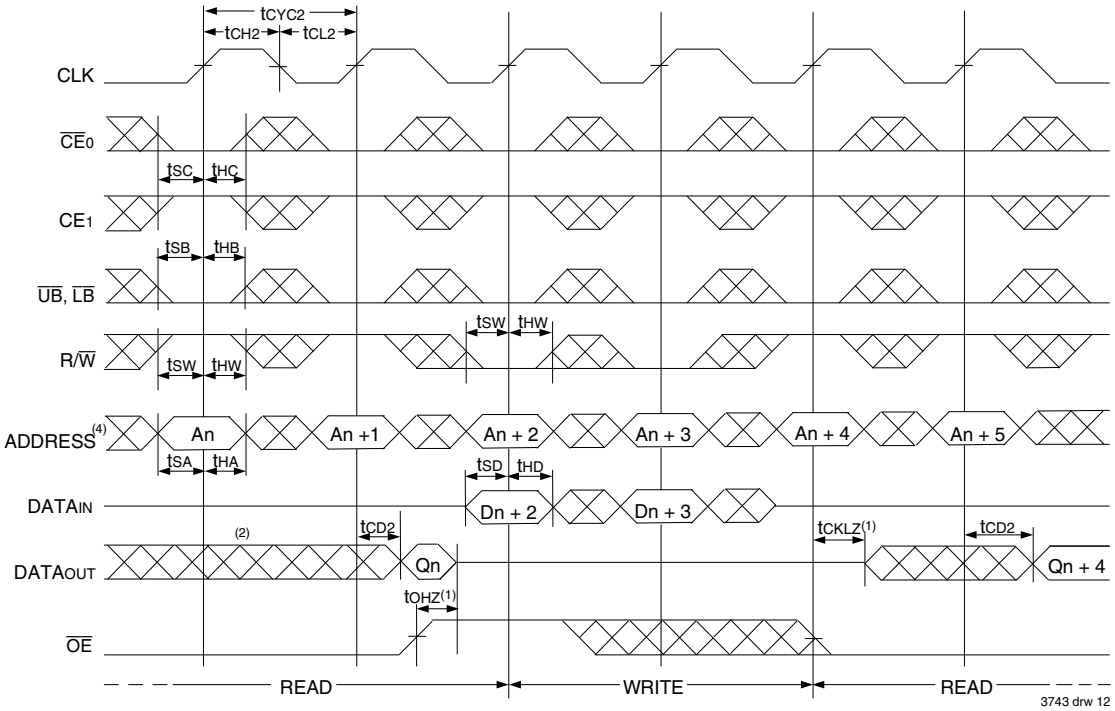
NOTES:
1. $\overline{CE_0}$, $\overline{BE_n}$, and $\overline{ADS}$ = V_{IL}; CE_1, $\overline{CNTEN}$, and $\overline{REPEAT}$ = V_{IH}.
2. $\overline{OE}$ = V_{IL} for Port "B", which is being read from. $\overline{OE}$ = V_{IH} for Port "A", which is being written to.
3. If $t_{CO} \leq$ minimum specified, then data from Port "B" read is not valid until following Port "B" clock cycle (ie, time from write to valid read on opposite port will be $t_{CO} + 2\ t_{CYC2} + t_{CD2}$). If t_{CO} > minimum, then data from Port "B" read is available on first Port "B" clock cycle (ie, time from write to valid read on opposite port will be $t_{CO} + t_{CYC2} + t_{CD2}$).
4. All timing is the same for Left and Right ports. Port "A" may be either Left or Right port. Port "B" is the opposite of Port "A"

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Timing Waveform of Pipelined Read-to-Write-to-Read ($\overline{OE}$ = VIL)(3)



Timing Waveform of Pipelined Read-to-Write-to-Read ($\overline{OE}$ Controlled)(3)

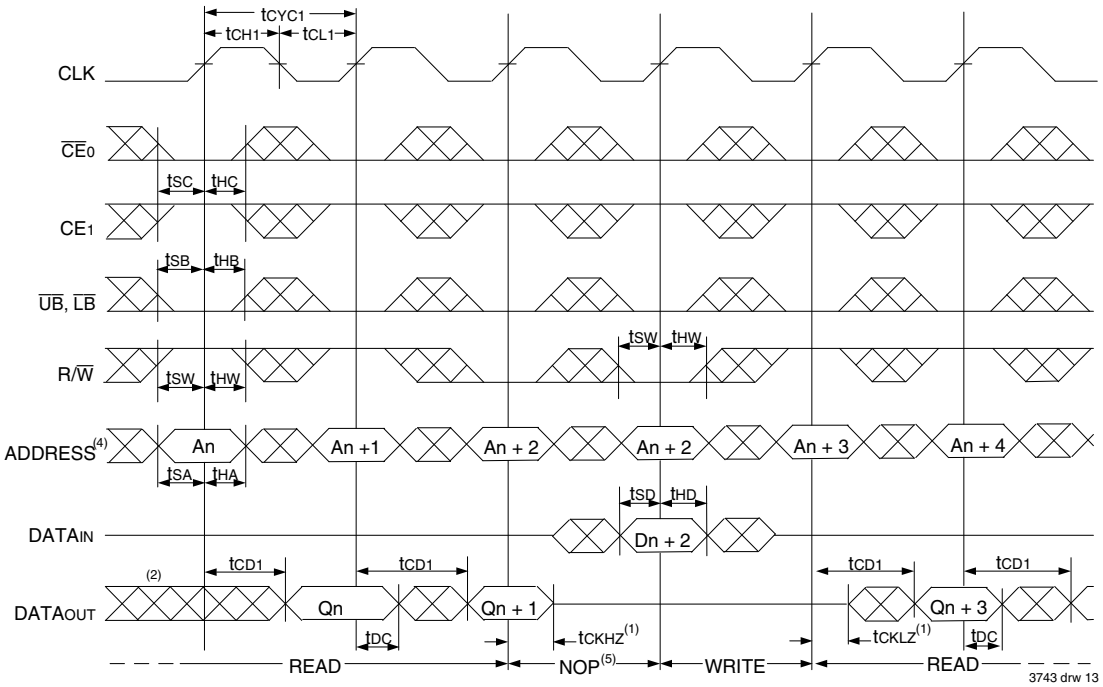


NOTES:

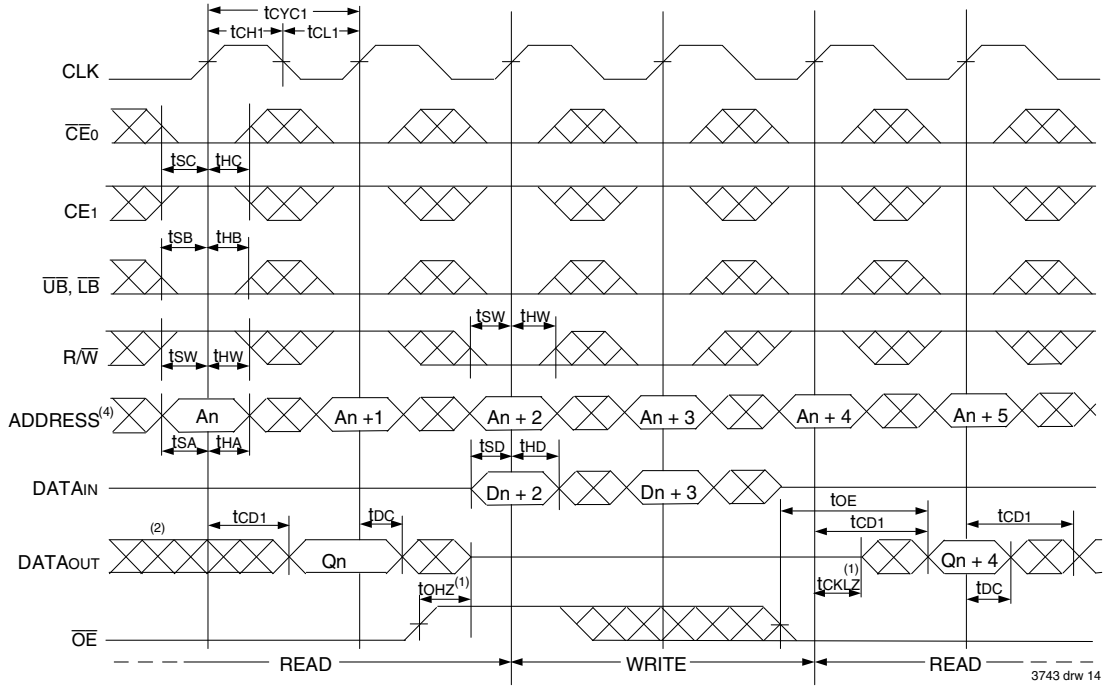
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
3. $\overline{CE}_0$, $\overline{UB}$, $\overline{LB}$, and $\overline{ADS}$ = VIL; CE1, $\overline{CNTEN}$, and $\overline{CNTRST}$ = VIH.
4. Addresses do not have to be accessed sequentially since ADS = VIL constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be rewritten to guarantee data integrity.

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Timing Waveform of Flow-Through Read-to-Write-to-Read ($\overline{OE}$ = VIL)(3)



Timing Waveform of Flow-Through Read-to-Write-to-Read ($\overline{OE}$ Controlled)(3)

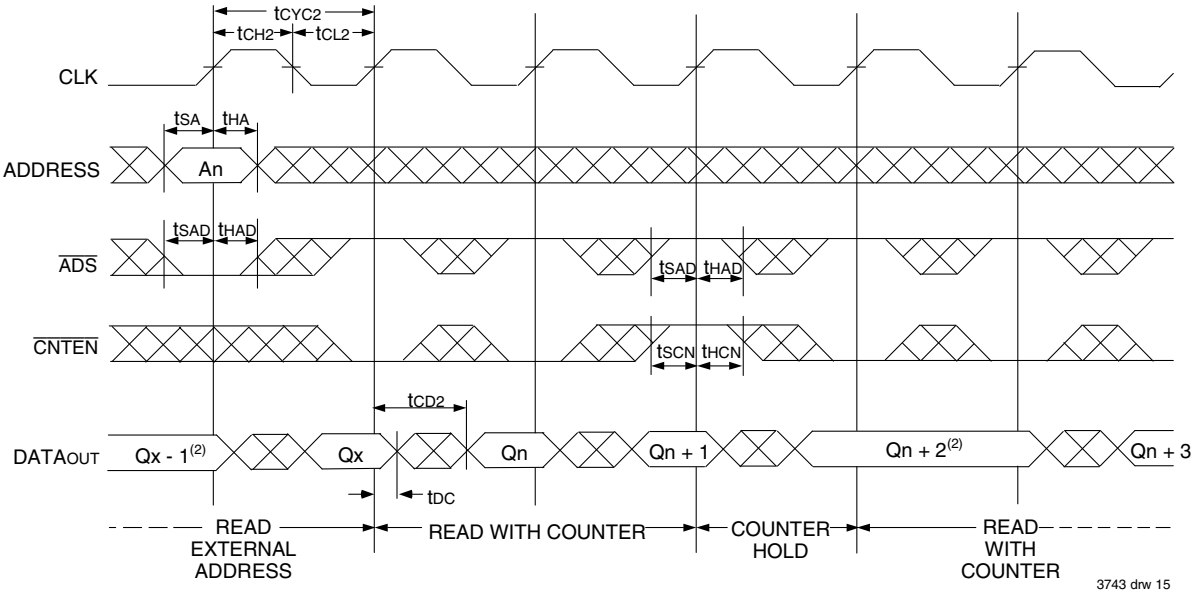


NOTES:

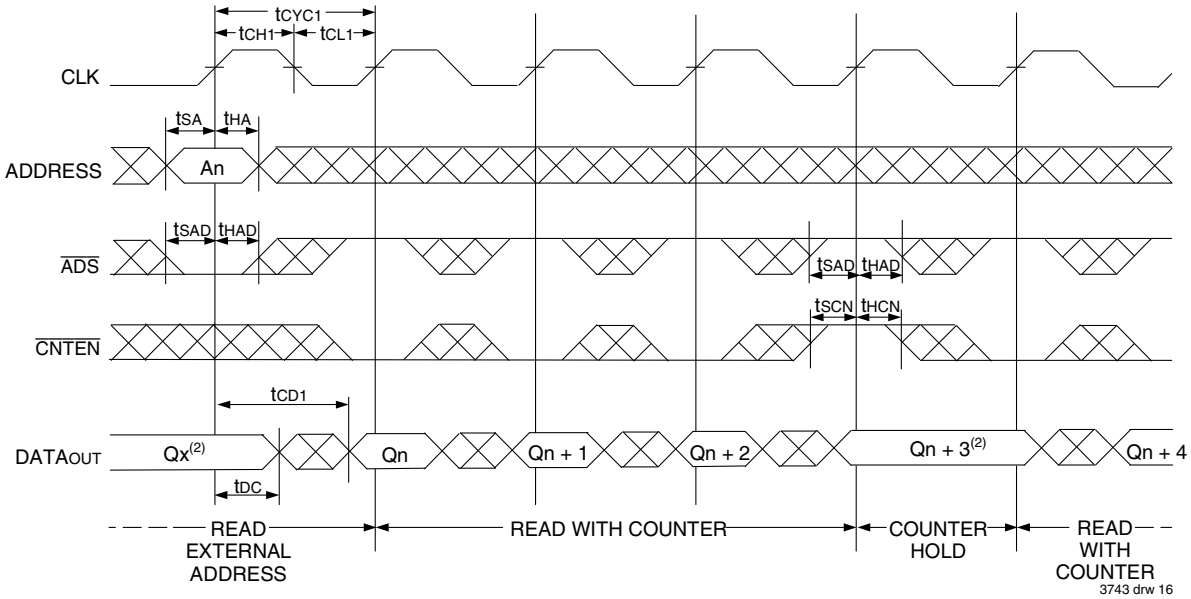
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
3. $\overline{CE_0}$, $\overline{UB}$, $\overline{LB}$, and $\overline{ADS}$ = VIL; CE1, $\overline{CNTEN}$, and $\overline{CNTRST}$ = VIH.
4. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = VIL constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be rewritten to guarantee data integrity.

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Timing Waveform of Pipelined Read with Address Counter Advance(1)



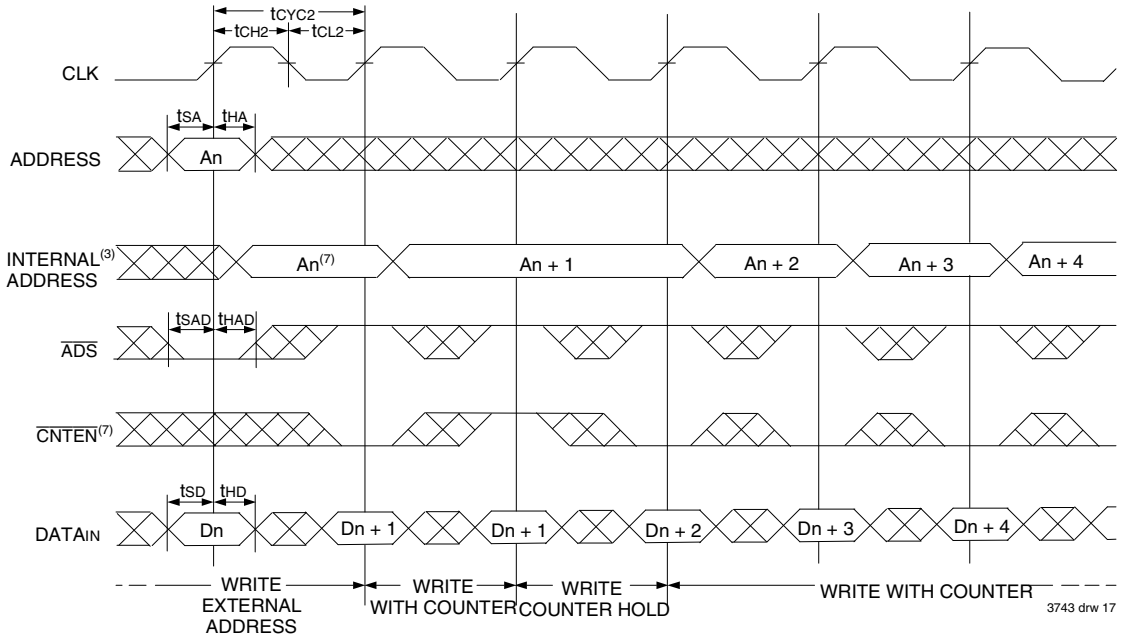
Timing Waveform of Flow-Through Read with Address Counter Advance(1)



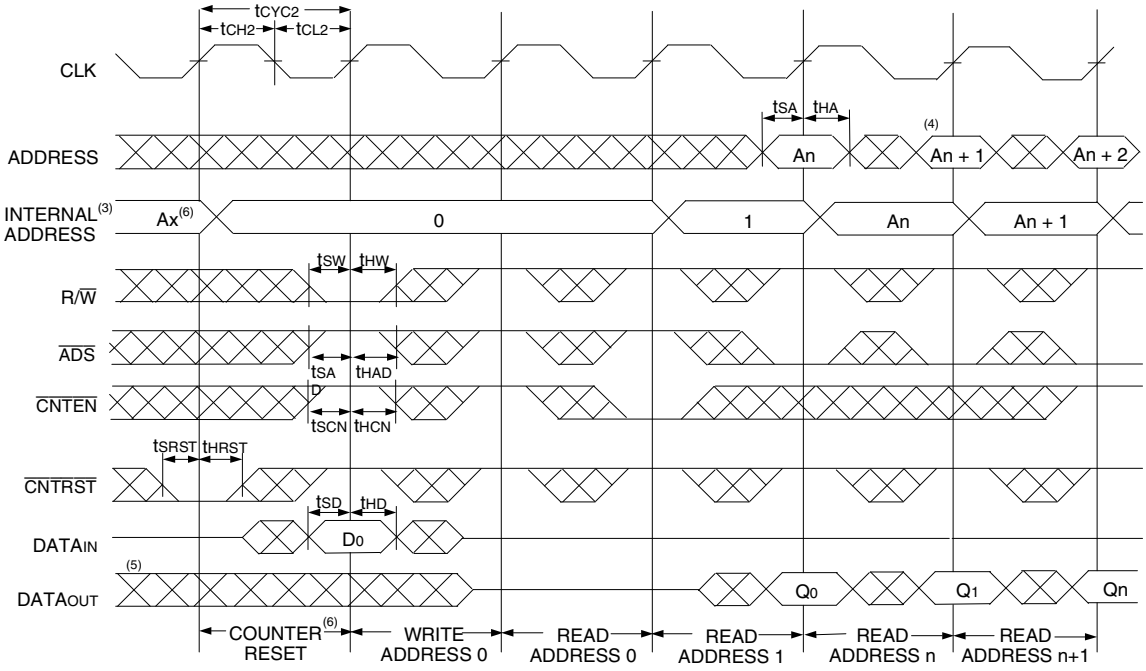
NOTES:
1. $\overline{CE_0}$, $\overline{OE}$, $\overline{UB}$, and $\overline{LB}$ = V_{IL}; CE_1, R/$\overline{W}$, and $\overline{CNTRST}$ = V_{IH}.
2. If there is no address change via $\overline{ADS}$ = V_{IL} (loading a new address) or $\overline{CNTEN}$ = V_{IL} (advancing the address), i.e. $\overline{ADS}$ = V_{IH} and $\overline{CNTEN}$ = V_{IH}, then the data output remains constant for subsequent clocks.

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Timing Waveform of Write with Address Counter Advance (Flow-Through or Pipelined Outputs)(1)



Timing Waveform of Counter Reset (Pipelined Outputs)(2)



NOTES:
1. $\overline{CE_0}$, $\overline{UB}$, $\overline{LB}$, and R/$\overline{W}$ = V_{IL}; CE_1 and $\overline{CNTRST}$ = V_{IH}.
2. $\overline{CE_0}$, $\overline{UB}$, $\overline{LB}$ = V_{IL}; CE_1 = V_{IH}.
3. The "Internal Address" is equal to the "External Address" when $\overline{ADS}$ = V_{IL} and equals the counter output when $\overline{ADS}$ = V_{IH}.
4. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = V_{IL} constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
6. No dead cycle exists during counter reset. A READ or WRITE cycle may be coincidental with the counter reset cycle. $ADDR_0$ will be accessed. Extra cycles are shown here simply for clarification.
7. $\overline{CNTEN}$ = V_{IL} advances Internal Address from 'An' to 'An +1'. The transition shown indicates the time required for the counter to advance. The 'An +1'Address is written to during this cycle.

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Functional Description

The IDT70V9279/69 provides a true synchronous Dual-Port Static RAM interface. Registered inputs provide minimal set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal, however, the self-timed internal write pulse is independent of the LOW to HIGH transition of the clock signal.

An asynchronous output enable is provided to ease asynchronous bus interfacing. Counter enable inputs are also provided to staff the operation of the address counters for fast interleaved memory applications.

A HIGH on $\overline{CE}_0$ or a LOW on CE_1 for one clock cycle will power down the internal circuitry to reduce static power consumption. Multiple chip enables allow easier banking of multiple IDT70V9279/69's for depth expansion configurations. When the Pipelined output mode is enabled, two cycles are required with $\overline{CE}_0$ LOW and CE_1 HIGH to reactivate the outputs.

Depth and Width Expansion

The IDT70V9279/69 features dual chip enables (refer to Truth Table I) in order to facilitate rapid and simple depth expansion with no requirements for external logic. Figure 4 illustrates how to control the various chip enables in order to expand two devices in depth.

The IDT70V9279/69 can also be used in applications requiring expanded width, as indicated in Figure 4. Since the banks are allocated at the discretion of the user, the external controller can be set up to drive the input signals for the various devices as required to allow for 32-bit or wider applications.

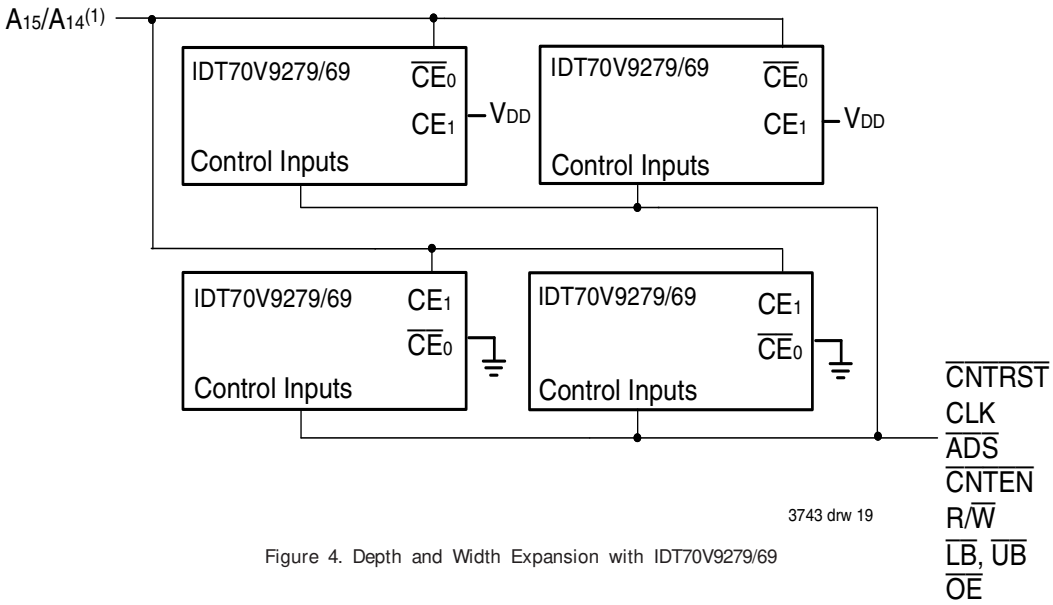
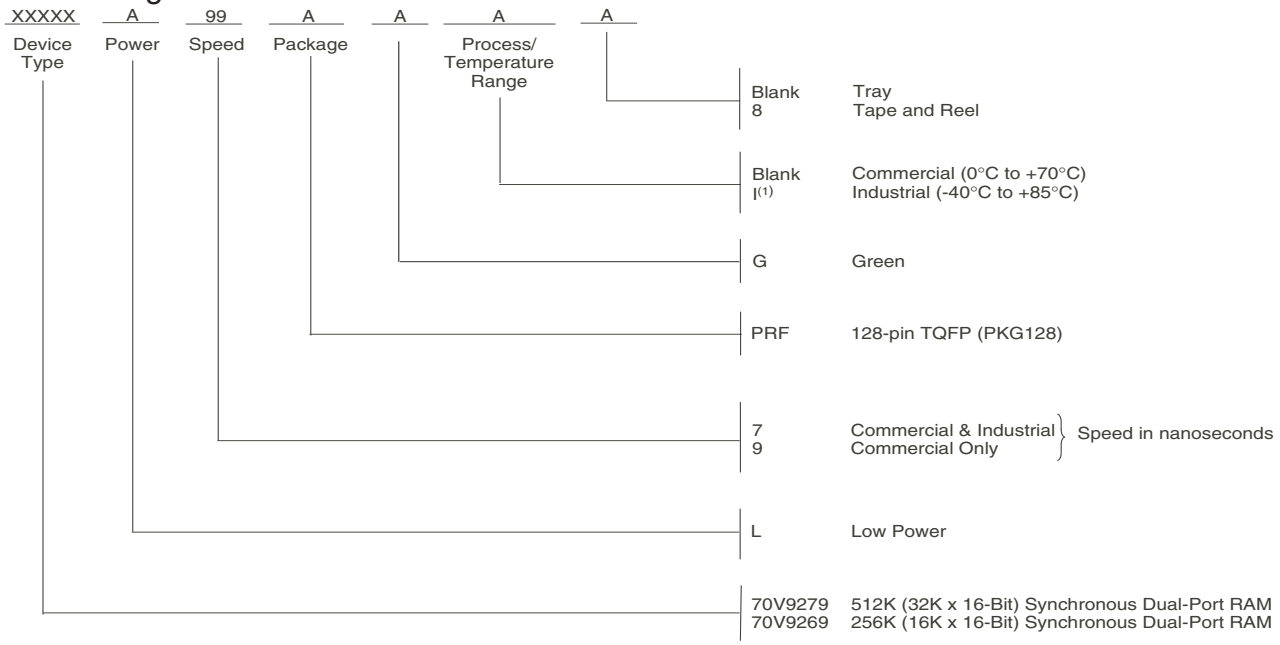


Figure 4. Depth and Width Expansion with IDT70V9279/69

NOTE:
1. A_{15} is for IDT70V9279. A_{14} is for IDT70V9269.

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Ordering Information



3743 drw 20

NOTES:

1. Contact your local sales office for industrial temp. range for other speeds, packages and powers.

LEAD FINISH (SnPb) parts are Obsolete. Product Discontinuation Notice - PDN# SP-17-02

Note that information regarding recently obsoleted parts are included in this datasheet for customer convenience.

Ordering Information for Flow-through Devices

Old Flow-through Part	New Combined Part
70V927S/L25	70V9279L7
70V927S/L30	70V9279L9

3743 tbl 12

IDT Clock Solution for IDT70V9279/69 Dual-Port

IDT Dual-Port Part Number	Dual-Port I/O Specitications		Clock Specifications				IDT PLL Clock Device	IDT Non-PLL Clock Device
	Voltage	I/O	Input Capacitance	Input Duty Cycle Requirement	Maximum Frequency	Jitter Tolerance		
70V9279/69	3.3	LVTTL	9pF	40%	100	150ps	2305 2308 2309	49FCT3805 49FCT3805D/E 74FCT3807 74FCT3807D/E

3743 tbl 13

Orderable Part Information

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
7	70V9279L7PRFG	PKG128	TQFP	C
	70V9279L7PRFG8	PKG128	TQFP	C
	70V9279L7PRFGI	PKG128	TQFP	I
	70V9279L7PRFGI8	PKG128	TQFP	I

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
9	70V9269L9PRFG	PKG128	TQFP	C
	70V9269L9PRFG8	PKG128	TQFP	C

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Datasheet Document History

01/12/99:		Initiated datasheet document history
		Converted to new format
		Cosmetic and typographical corrections
		Added additional notes to pin configurations
	Page 14	Added Depth & Width Expansion section
06/15/99:	Page 4	Deleted note 6 for Table II
09/29/99:	Page 7	Corrected typo in heading
11/10/99:		Replaced IDT logo
03/31/00:		Combined Pipelined 70V9279/69 family and Flow-through 70V927 family offerings into one data sheet
		Changed ±200mV in waveform notes to 0mV
		Added corresponding part chart with ordering information
01/017/01:	Page 4	Changed information in Truth Table II
		Increased storage temperature parameters
		Clarified T_A parameter
	Page 5	DC Electrical parameters–changed wording from "open" to "disabled"
		Removed Preliminary status
02/25/04:		Consolidated multiple devices into one datasheet
		Changed naming conventions from V_{CC} to V_{DD} and from GND to Vss
	Page 2	Added date revision for pin configuration
	Page 3	Added footnotes for $\overline{UB}$, $\overline{LB}$, $\overline{CE}_0$ and CE_1 buffer conditions when $\overline{FT}$ or PIPE
	Page 4	Added junction temperature to Absolute Maximum Ratings Table
		Added Ambient Temperature footnote
	Page 5	Added I-temp numbers for 9ns speed to DC Electrical Characteristics Table
		Added 6ns speed DC power numbers to the DC Electrical Characteristics Table
	Page 7	Added I-temp for 9ns speed to AC Electrical Characteristics Table
		Added 6ns speed AC timing numbers to the AC Electrical Characteristics Table
	Page 18	Added 6ns speed grade and 9ns I-temp to ordering information
		Added IDT Clock Solution Table
	Page 1 & 19	Updated IDT logo, replaced IDT™ logo with IDT® logo
05/04/04:	Page 1 & 18	Added 7ns speed grade to ordering information
	Page 5	Added 7ns speed DC power numbers to the DC Electrical Characteristics Table
	Page 8	Added 7ns speed AC timing numbers to the AC Electrical Characteristics Table
10/11/04:	Page 4	Updated Capacitance table
	Page 5	Added 7ns I-temp and removed 9ns I-temp DC power numbers from the DC Electrical Characteristics table
	Page 8	Added 7ns I-temp and removed 9ns I-temp from the AC Electrical Characteristics table
	Page 12	Added Timing Waveform of Left Port Write to Pipelined Right Port Read
	Page 18	Added 7ns I-temp and removed 9ns I-temp from ordering information
01/19/06:	Page 1	Added green availability to features
	Page 18	Added green indicator to ordering information
10/23/08:	Page18	Removed "IDT" from orderable part number
06/25/18:		Added Tape & Reel to Ordering Information
		Product Discontinuation Notice - PDN# SP-17-02
		Last time buy expires June 15, 2018
08/06/19:	Page 1 & 18	Deleted obsolete Commercial speed grades 6/12/15ns
	Page 2	Updated package code PK-128 to PKG128
	Page 18	Added Orderable Part Information table

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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