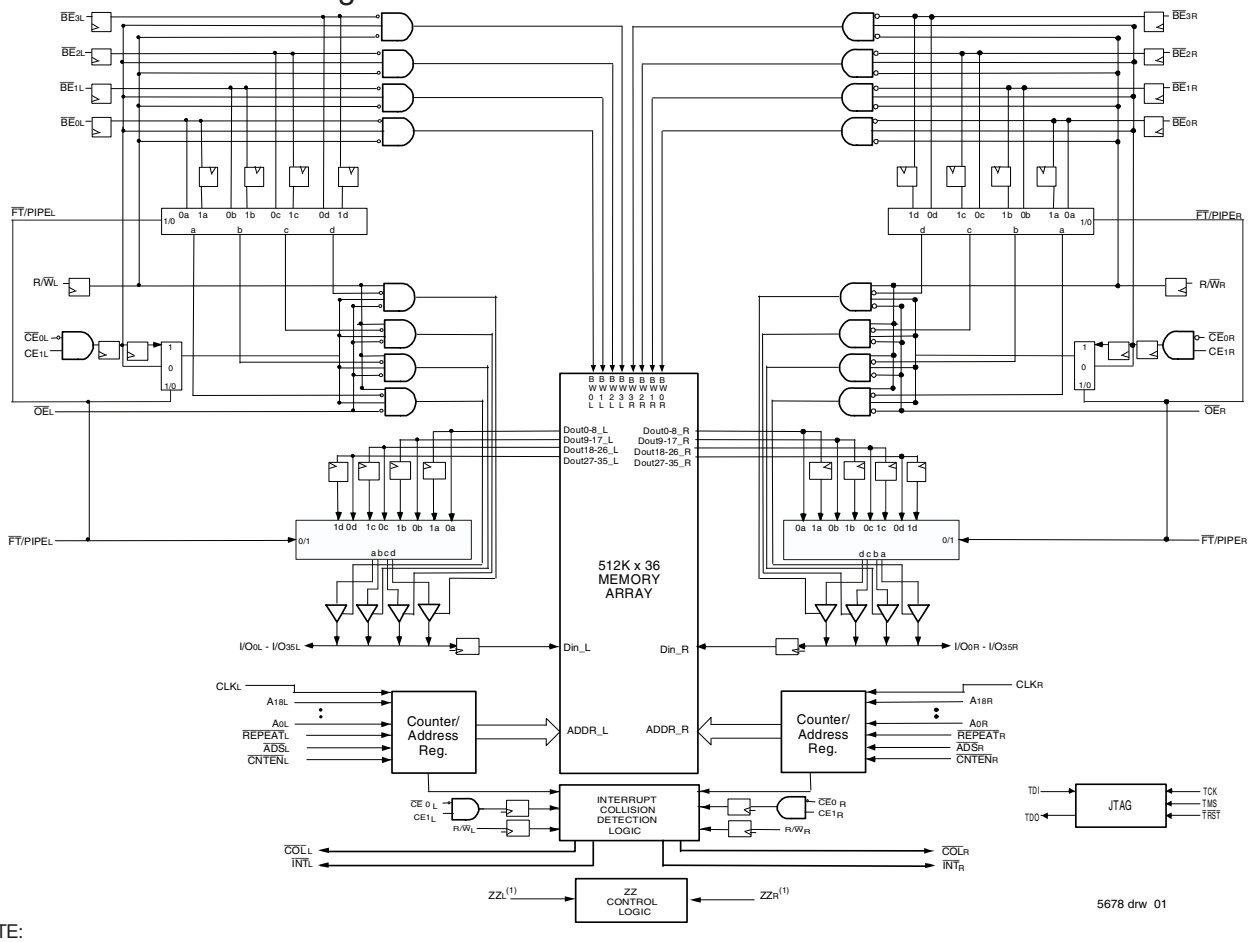
HIGH-SPEED 2.5V 512K x 36 SYNCHRONOUS DUAL-PORT STATIC RAM WITH 3.3V OR 2.5V INTERFACE

70T3539M

Features:

- True Dual-Port memory cells which allow simultaneous access of the same memory location
- High-speed data access
  - *Commercial: 3.6ns (166MHz)/4.2ns (133MHz)(max.)*
  - *Industrial: 4.2ns (133MHz) (max.)*
- Selectable Pipelined or Flow-Through output mode
- Counter enable and repeat features
- Dual chip enables allow for depth expansion without additional logic
- Interrupt and Collision Detection Flags
- Full synchronous operation on both ports
  - *6ns cycle time, 166MHz operation (12Gbps bandwidth)*
  - *Fast 3.6ns clock to data out*
  - *1.5ns setup to clock and 0.5ns hold on all control, data, and address inputs @ 166MHz*
  - *Data input, address, byte enable and control registers*
  - *Self-timed write allows fast cycle time*
- Separate byte controls for multiplexed bus and bus matching compatibility
- Dual Cycle Deselect (DCD) for Pipelined Output Mode
- 2.5V (±100mV) power supply for core
- LVTTL compatible, selectable 3.3V (±150mV) or 2.5V (±100mV) power supply for I/Os and control signals on each port
- Includes JTAG functionality
- Industrial temperature range (-40°C to +85°C) is available at 133MHz
- Available in a 256-pin Ball Grid Array (BGA)
- Green parts available, see ordering information

Functional Block Diagram



NOTE:

1. The sleep mode pin shuts off all dynamic inputs, except JTAG inputs, when asserted. All static inputs, i.e., PL/$\overline{FT}$x and OPTx and the sleep mode pins themselves (ZZx) are not affected during sleep mode.

JUNE 2019

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Description:

The IDT70T3539M is a high-speed 512K x 36 bit synchronous Dual-Port RAM. The memory array utilizes Dual-Port memory cells to allow simultaneous access of any address from both ports. Registers on control, data, and address inputs provide minimal setup and hold times. The timing latitude provided by this approach allows systems to be designed with very short cycle times. With an input data register, the IDT70T3539M has been optimized for applications having unidirectional or bidirectional data flow in bursts. An automatic power down feature, controlled by $\overline{CE}_0$ and CE_1, permits the on-chip circuitry of each port to enter a very low standby power mode.

The 70T3539M can support an operating voltage of either 3.3V or 2.5V on one or both ports, controllable by the OPT pins. The power supply for the core of the device (V_{DD}) is at 2.5V.

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Pin Configuration (1,2,3,4)

70T3539M
BC256(5)
BCG256(5)

256-Pin BGA
Top View(6)

10/07/03

A1 NC	A2 TDI	A3 NC	A4 A_{17L}	A5 A_{14L}	A6 A_{11L}	A7 A_{8L}	A8 $\overline{BE}_{2L}$	A9 CE_{1L}	A10 $\overline{OE}_L$	A11 $\overline{CNTEN}_L$	A12 A_{5L}	A13 A_{2L}	A14 A_{0L}	A15 NC	A16 NC
B1 I/O_{18L}	B2 NC	B3 TDO	B4 A_{18L}	B5 A_{15L}	B6 A_{12L}	B7 A_{9L}	B8 $\overline{BE}_{3L}$	B9 $\overline{CE}_{0L}$	B10 $R/\overline{W}_L$	B11 $\overline{REPEAT}_L$	B12 A_{4L}	B13 A_{1L}	B14 V_{DD}	B15 I/O_{17L}	B16 NC
C1 I/O_{18R}	C2 I/O_{19L}	C3 V_{SS}	C4 A_{16L}	C5 A_{13L}	C6 A_{10L}	C7 A_{7L}	C8 $\overline{BE}_{1L}$	C9 $\overline{BE}_{0L}$	C10 CLK_L	C11 $\overline{ADS}_L$	C12 A_{6L}	C13 A_{3L}	C14 OPT_L	C15 I/O_{17R}	C16 I/O_{16L}
D1 I/O_{20R}	D2 I/O_{19R}	D3 I/O_{20L}	D4 $PIPE/\overline{FT}_L$	D5 V_{DDQL}	D6 V_{DDQL}	D7 V_{DDQR}	D8 V_{DDQR}	D9 V_{DDQL}	D10 V_{DDQL}	D11 V_{DDQR}	D12 V_{DDQR}	D13 V_{DD}	D14 I/O_{15R}	D15 I/O_{15L}	D16 I/O_{16R}
E1 I/O_{21R}	E2 I/O_{21L}	E3 I/O_{22L}	E4 V_{DDQL}	E5 V_{DD}	E6 V_{DD}	E7 $\overline{INT}_L$	E8 V_{SS}	E9 V_{SS}	E10 V_{SS}	E11 V_{DD}	E12 V_{DD}	E13 V_{DDQR}	E14 I/O_{13L}	E15 I/O_{14L}	E16 I/O_{14R}
F1 I/O_{23L}	F2 I/O_{22R}	F3 I/O_{23R}	F4 V_{DDQL}	F5 V_{DD}	F6 NC	F7 $\overline{COL}_L$	F8 V_{SS}	F9 V_{SS}	F10 V_{SS}	F11 V_{SS}	F12 V_{DD}	F13 V_{DDQR}	F14 I/O_{12R}	F15 I/O_{13R}	F16 I/O_{12L}
G1 I/O_{24R}	G2 I/O_{24L}	G3 I/O_{25L}	G4 V_{DDQR}	G5 V_{SS}	G6 V_{SS}	G7 V_{SS}	G8 V_{SS}	G9 V_{SS}	G10 V_{SS}	G11 V_{SS}	G12 V_{SS}	G13 V_{DDQL}	G14 I/O_{10L}	G15 I/O_{11L}	G16 I/O_{11R}
H1 I/O_{26L}	H2 I/O_{25R}	H3 I/O_{26R}	H4 V_{DDQR}	H5 V_{SS}	H6 V_{SS}	H7 V_{SS}	H8 V_{SS}	H9 V_{SS}	H10 V_{SS}	H11 V_{SS}	H12 V_{SS}	H13 V_{DDQL}	H14 I/O_{9R}	H15 IO_{9L}	H16 I/O_{10R}
J1 I/O_{27L}	J2 I/O_{28R}	J3 I/O_{27R}	J4 V_{DDQL}	J5 ZZ_R	J6 V_{SS}	J7 V_{SS}	J8 V_{SS}	J9 V_{SS}	J10 V_{SS}	J11 V_{SS}	J12 ZZ_L	J13 V_{DDQR}	J14 I/O_{8R}	J15 I/O_{7R}	J16 I/O_{8L}
K1 I/O_{29R}	K2 I/O_{29L}	K3 I/O_{28L}	K4 V_{DDQL}	K5 V_{SS}	K6 V_{SS}	K7 V_{SS}	K8 V_{SS}	K9 V_{SS}	K10 V_{SS}	K11 V_{SS}	K12 V_{SS}	K13 V_{DDQR}	K14 I/O_{6R}	K15 I/O_{6L}	K16 I/O_{7L}
L1 I/O_{30L}	L2 I/O_{31R}	L3 I/O_{30R}	L4 V_{DDQR}	L5 V_{DD}	L6 NC	L7 $\overline{COL}_R$	L8 V_{SS}	L9 V_{SS}	L10 V_{SS}	L11 V_{SS}	L12 V_{DD}	L13 V_{DDQL}	L14 I/O_{5L}	L15 I/O_{4R}	L16 I/O_{5R}
M1 I/O_{32R}	M2 I/O_{32L}	M3 I/O_{31L}	M4 V_{DDQR}	M5 V_{DD}	M6 V_{DD}	M7 $\overline{INT}_R$	M8 V_{SS}	M9 V_{SS}	M10 V_{SS}	M11 V_{DD}	M12 V_{DD}	M13 V_{DDQL}	M14 I/O_{3R}	M15 I/O_{3L}	M16 I/O_{4L}
N1 I/O_{33L}	N2 I/O_{34R}	N3 I/O_{33R}	N4 $PIPE/\overline{FT}_R$	N5 V_{DDQR}	N6 V_{DDQR}	N7 V_{DDQL}	N8 V_{DDQL}	N9 V_{DDQR}	N10 V_{DDQR}	N11 V_{DDQL}	N12 V_{DDQL}	N13 V_{DD}	N14 I/O_{2L}	N15 I/O_{1R}	N16 I/O_{2R}
P1 I/O_{35R}	P2 I/O_{34L}	P3 TMS	P4 A_{16R}	P5 A_{13R}	P6 A_{10R}	P7 A_{7R}	P8 $\overline{BE}_{1R}$	P9 $\overline{BE}_{0R}$	P10 CLK_R	P11 $\overline{ADS}_R$	P12 A_{6R}	P13 A_{3R}	P14 I/O_{0L}	P15 I/O_{0R}	P16 I/O_{1L}
R1 I/O_{35L}	R2 NC	R3 $\overline{TRST}$	R4 A_{18R}	R5 A_{15R}	R6 A_{12R}	R7 A_{9R}	R8 $\overline{BE}_{3R}$	R9 $\overline{CE}_{0R}$	R10 $R/\overline{W}_R$	R11 $\overline{REPEAT}_R$	R12 A_{4R}	R13 A_{1R}	R14 OPT_R	R15 NC	R16 NC
T1 NC	T2 TCK	T3 NC	T4 A_{17R}	T5 A_{14R}	T6 A_{11R}	T7 A_{8R}	T8 $\overline{BE}_{2R}$	T9 CE_{1R}	T10 $\overline{OE}_R$	T11 $\overline{CNTEN}_R$	T12 A_{5R}	T13 A_{2R}	T14 A_{0R}	T15 NC	T16 NC

5678 drw 02d

NOTES:
1. All V_{DD} pins must be connected to 2.5V power supply.
2. All V_{DDQ} pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to V_{DD} (2.5V), and 2.5V if OPT pin for that port is set to V_{SS} (0V).
3. All V_{SS} pins must be connected to ground supply.
4. Package body is approximately 17mm x 17mm x 1.4mm, with 1.0mm ball-pitch.
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part-marking.

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Pin Names

Left Port	Right Port	Names
$\overline{CE}_{0L}$, CE_{1L}	$\overline{CE}_{0R}$, CE_{1R}	Chip Enables (Input)[5]
R/$\overline{W}_L$	R/$\overline{W}_R$	Read/Write Enable (Input)
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable (Input)
A_{0L} - A_{18L}	A_{0R} - A_{18R}	Address (Input)
I/O_{0L} - I/O_{35L}	I/O_{0R} - I/O_{35R}	Data Input/Output
CLK_L	CLK_R	Clock (Input)
PL/$\overline{FT}_L$	PL/$\overline{FT}_R$	Pipeline/Flow-Through (Input)
$\overline{ADS}_L$	$\overline{ADS}_R$	Address Strobe Enable (Input)
$\overline{CNTEN}_L$	$\overline{CNTEN}_R$	Counter Enable (Input)
$\overline{REPEAT}_L$	$\overline{REPEAT}_R$	Counter Repeat[3]
$\overline{BE}_{0L}$ - $\overline{BE}_{3L}$	$\overline{BE}_{0R}$ - $\overline{BE}_{3R}$	Byte Enables (9-bit bytes) (Input)[5]
V_{DDQL}	V_{DDQR}	Power (I/O Bus) (3.3V or 2.5V)[1] (Input)
OPT_L	OPT_R	Option for selecting V_{DDQX}[1,2] (Input)
ZZ_L	ZZ_R	Sleep Mode pin[4] (Input)
V_{DD}		Power (2.5V)[1] (Input)
V_{SS}		Ground (0V) (Input)
TDI		Test Data Input
TDO		Test Data Output
TCK		Test Logic Clock (10MHz) (Input)
TMS		Test Mode Select (Input)
$\overline{TRST}$		Reset (Initialize TAP Controller) (Input)
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag (Output)
$\overline{COL}_L$	$\overline{COL}_R$	Collision Alert (Output)

5678 tbl 01

NOTES:
1. V_{DD}, OPT_X, and V_{DDQX} must be set to appropriate operating levels prior to applying inputs on the I/Os and controls for that port.
2. OPT_X selects the operating voltage levels for the I/Os and controls on that port. If OPT_X is set to V_{DD} (2.5V), then that port's I/Os and controls will operate at 3.3V levels and V_{DDQX} must be supplied at 3.3V. If OPT_X is set to V_{SS} (0V), then that port's I/Os and address controls will operate at 2.5V levels and V_{DDQX} must be supplied at 2.5V. The OPT pins are independent of one another—both ports can operate at 3.3V levels, both can operate at 2.5V levels, or either can operate at 3.3V with the other at 2.5V.
3. When $\overline{REPEAT}_X$ is asserted, the counter will reset to the last valid address loaded via $\overline{ADS}_X$.
4. The sleep mode pin shuts off all dynamic inputs, except JTAG inputs, when asserted. All static inputs, i.e., PL/$\overline{FT}_X$ and OPT_X and the sleep mode pins themselves (ZZ_X) are not affected during sleep mode. It is recommended that boundry scan not be operated during sleep mode.
5. Chip Enables and Byte Enables are double buffered when PL/$\overline{FT}$ = V_{IH}, i.e., the signals take two cycles to deselect.

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Truth Table I—Read/Write and Enable Control (1,2,3,4)

$\overline{OE}$	CLK	$\overline{CE}_0$	CE_1	$\overline{BE}_3$	$\overline{BE}_2$	$\overline{BE}_1$	$\overline{BE}_0$	R/$\overline{W}$	ZZ	Byte 3 I/O_{27-35}	Byte 2 I/O_{18-26}	Byte 1 I/O_{9-17}	Byte 0 I/O_{0-8}	MODE
X	↑	H	X	X	X	X	X	X	L	High-Z	High-Z	High-Z	High-Z	Deselected–Power Down
X	↑	X	L	X	X	X	X	X	L	High-Z	High-Z	High-Z	High-Z	Deselected–Power Down
X	↑	L	H	H	H	H	H	X	L	High-Z	High-Z	High-Z	High-Z	All Bytes Deselected
X	↑	L	H	H	H	H	L	L	L	High-Z	High-Z	High-Z	D_{IN}	Write to Byte 0 Only
X	↑	L	H	H	H	L	H	L	L	High-Z	High-Z	D_{IN}	High-Z	Write to Byte 1 Only
X	↑	L	H	H	L	H	H	L	L	High-Z	D_{IN}	High-Z	High-Z	Write to Byte 2 Only
X	↑	L	H	L	H	H	H	L	L	D_{IN}	High-Z	High-Z	High-Z	Write to Byte 3 Only
X	↑	L	H	H	H	L	L	L	L	High-Z	High-Z	D_{IN}	D_{IN}	Write to Lower 2 Bytes Only
X	↑	L	H	L	L	H	H	L	L	D_{IN}	D_{IN}	High-Z	High-Z	Write to Upper 2 bytes Only
X	↑	L	H	L	L	L	L	L	L	D_{IN}	D_{IN}	D_{IN}	D_{IN}	Write to All Bytes
L	↑	L	H	H	H	H	L	H	L	High-Z	High-Z	High-Z	D_{OUT}	Read Byte 0 Only
L	↑	L	H	H	H	L	H	H	L	High-Z	High-Z	D_{OUT}	High-Z	Read Byte 1 Only
L	↑	L	H	H	L	H	H	H	L	High-Z	D_{OUT}	High-Z	High-Z	Read Byte 2 Only
L	↑	L	H	L	H	H	H	H	L	D_{OUT}	High-Z	High-Z	High-Z	Read Byte 3 Only
L	↑	L	H	H	H	L	L	H	L	High-Z	High-Z	D_{OUT}	D_{OUT}	Read Lower 2 Bytes Only
L	↑	L	H	L	L	H	H	H	L	D_{OUT}	D_{OUT}	High-Z	High-Z	Read Upper 2 Bytes Only
L	↑	L	H	L	L	L	L	H	L	D_{OUT}	D_{OUT}	D_{OUT}	D_{OUT}	Read All Bytes
H	↑	X	X	X	X	X	X	X	L	High-Z	High-Z	High-Z	High-Z	Outputs Disabled
X	X	X	X	X	X	X	X	X	H	High-Z	High-Z	High-Z	High-Z	Sleep Mode

5678 tbl 02

NOTES:
1. "H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care.
2. $\overline{ADS}$, $\overline{CNTEN}$, $\overline{REPEAT}$ = X.
3. $\overline{OE}$ and ZZ are asynchronous input signals.
4. It is possible to read or write any combination of bytes during a given access. A few representative samples have been illustrated here.

Truth Table II—Address Counter Control (1,2)

Address	Previous Internal Address	Internal Address Used	CLK	$\overline{ADS}$	$\overline{CNTEN}$	$\overline{REPEAT}$(6)	I/O(3)	MODE
An	X	An	↑	L(4)	X	H	$D_{I/O}$ (n)	External Address Used
X	An	An + 1	↑	H	L(5)	H	$D_{I/O}$(n+1)	Counter Enabled—Internal Address generation
X	An + 1	An + 1	↑	H	H	H	$D_{I/O}$(n+1)	External Address Blocked—Counter disabled (An + 1 reused)
X	X	An	↑	X	X	L(4)	$D_{I/O}$(n)	Counter Set to last valid $\overline{ADS}$ load

5678 tbl 03

NOTES:
1. "H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care.
2. Read and write operations are controlled by the appropriate setting of R/$\overline{W}$, $\overline{CE}_0$, CE_1, $\overline{BE}$n and $\overline{OE}$.
3. Outputs configured in flow-through output mode: if outputs are in pipelined mode the data out will be delayed by one cycle.
4. $\overline{ADS}$ and $\overline{REPEAT}$ are independent of all other memory control signals including $\overline{CE}_0$, CE_1 and $\overline{BE}$n
5. The address counter advances if $\overline{CNTEN}$ = V_{IL} on the rising edge of CLK, regardless of all other memory control signals including $\overline{CE}_0$, CE_1, $\overline{BE}$n.
6. When $\overline{REPEAT}$ is asserted, the counter will reset to the last valid address loaded via $\overline{ADS}$. This value is not set at power-up: a known location should be loaded via $\overline{ADS}$ during initialization if desired. Any subsequent $\overline{ADS}$ access during operations will update the $\overline{REPEAT}$ address location.

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Recommended Operating Temperature and Supply Voltage (1)

Grade	Ambient Temperature	GND	V_{DD}
Commercial	0°C to +70°C	0V	2.5V ± 100mV
Industrial	-40°C to +85°C	0V	2.5V ± 100mV

5678 tbl 04

NOTES:
1. This is the parameter TA. This is the "instant on" case temperature.

Recommended DC Operating Conditions with V_{DDQ} at 2.5V

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Core Supply Voltage	2.4	2.5	2.6	V
V_{DDQ}	I/O Supply Voltage(3)	2.4	2.5	2.6	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Volltage (Address, Control & Data I/O Inputs)(3)	1.7	—	V_{DDQ} + 100mV(2)	V
V_{IH}	Input High Voltage – JTAG	1.7	—	V_{DD} + 100mV(2)	V
V_{IH}	Input High Voltage - ZZ, OPT, PIPE/$\overline{FT}$	V_{DD} - 0.2V	—	V_{DD} + 100mV(2)	V
V_{IL}	Input Low Voltage	-0.3(1)	—	0.7	V
V_{IL}	Input Low Voltage - ZZ, OPT, PIPE/$\overline{FT}$	-0.3(1)	—	0.2	V

5678 tbl 05a

NOTES:
1. V_{IL} (min.) = -1.0V for pulse width less than t_{CYC}/2 or 5ns, whichever is less.
2. V_{IH} (max.) = V_{DDQ} + 1.0V for pulse width less than t_{CYC}/2 or 5ns, whichever is less.
3. To select operation at 2.5V levels on the I/Os and controls of a given port, the OPT pin for that port must be set to V_{ss}(0V), and V_{DDQX} for that port must be supplied as indicated above.

Recommended DC Operating Conditions with V_{DDQ} at 3.3V

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Core Supply Voltage	2.4	2.5	2.6	V
V_{DDQ}	I/O Supply Voltage(3)	3.15	3.3	3.45	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage (Address, Control &Data I/O Inputs)(3)	2.0	—	V_{DDQ} + 150mV(2)	V
V_{IH}	Input High Voltage – JTAG	1.7	—	V_{DD} + 100mV(2)	V
V_{IH}	Input High Voltage - ZZ, OPT, PIPE/$\overline{FT}$	V_{DD} - 0.2V	—	V_{DD} + 100mV(2)	V
V_{IL}	Input Low Voltage	-0.3(1)	—	0.8	V
V_{IL}	Input Low Voltage - ZZ, OPT, PIPE/$\overline{FT}$	-0.3(1)	—	0.2	V

5678 tbl 05b

NOTES:
1. V_{IL} (min.) = -1.0V for pulse width less than t_{CYC}/2, or 5ns, whichever is less.
2. V_{IH} (max.) = V_{DDQ} + 1.0V for pulse width less than t_{CYC}/2 or 5ns, whichever is less.
3. To select operation at 3.3V levels on the I/Os and controls of a given port, the OPT pin for that port must be set to V_{DD} (2.5V), and V_{DDQX} for that port must be supplied as indicated above.

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Absolute Maximum Ratings (1)

Symbol	Rating	Commercial & Industrial	Unit
V_{TERM} (V_{DD})	V_{DD} Terminal Voltage with Respect to GND	-0.5 to 3.6	V
V_{TERM}(2) (V_{DDQ})	V_{DDQ} Terminal Voltage with Respect to GND	-0.3 to V_{DDQ} + 0.3	V
V_{TERM}(2) (INPUTS and I/O's)	Input and I/O Terminal Voltage with Respect to GND	-0.3 to V_{DDQ} + 0.3	V
T_{BIAS}(3)	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
T_{JN}	Junction Temperature	+150	°C
I_{OUT}(For V_{DDQ} = 3.3V)	DC Output Current	50	mA
I_{OUT}(For V_{DDQ} = 2.5V)	DC Output Current	40	mA

5678 tbl 06

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This is a steady-state DC parameter that applies after the power supply has reached its nominal operating value. Power sequencing is not necessary; however, the voltage on any Input or I/O pin cannot exceed V_{DDQ} during power supply ramp up.
3. Ambient Temperature under DC Bias. No AC Conditions. Chip Deselected.

Capacitance (1)

(T_A = +25°C, F = 1.0MHz) BGA ONLY

Symbol	Parameter	Conditions(2)	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	15	pF
C_{OUT}(3)	Output Capacitance	V_{OUT} = 0V	10.5	pF

5678 tbl 07

NOTES:
1. These parameters are determined by device characterization, but are not production tested.
2. C_{OUT} also references $C_{I/O}$.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{DD} = 2.5V ± 100mV)

Symbol	Parameter	Test Conditions	70T3539MS		Unit
			Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current(1)	V_{DDQ} = Max., V_{IN} = 0V to V_{DDQ}	—	10	µA
$\|I_{LI}\|$	JTAG & ZZ Input Leakage Current(1,2)	V_{DD} = Max., V_{IN} = 0V to V_{DD}	—	±30	µA
$\|I_{LO}\|$	Output Leakage Current(1,3)	$\overline{CE}_0$ = V_{IH} or CE_1 = V_{IL}, V_{OUT} = 0V to V_{DDQ}	—	10	µA
V_{OL} (3.3V)	Output Low Voltage(1)	I_{OL} = +4mA, V_{DDQ} = Min.	—	0.4	V
V_{OH} (3.3V)	Output High Voltage(1)	I_{OH} = -4mA, V_{DDQ} = Min.	2.4	—	V
V_{OL} (2.5V)	Output Low Voltage(1)	I_{OL} = +2mA, V_{DDQ} = Min.	—	0.4	V
V_{OH} (2.5V)	Output High Voltage(1)	I_{OH} = -2mA, V_{DDQ} = Min.	2.0	—	V

5678 tbl 08

NOTES:
1. V_{DDQ} is selectable (3.3V/2.5V) via OPT pins. Refer to p.5 for details.
2. Applicable only for TMS, TDI and $\overline{TRST}$ inputs.
3. Outputs tested in tri-state mode.

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DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (3) (V_{DD} = 2.5V ± 100mV)

Symbol	Parameter	Test Condition	Version		70T3539MS166 Com'l Only Typ.(4)	70T3539MS166 Com'l Only Max.	70T3539MS133 Com'l & Ind Typ.(4)	70T3539MS133 Com'l & Ind Max.	Unit
I_{DD}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}_L$ and $\overline{CE}_R$= V_{IL}, Outputs Disabled, f = f_{MAX}(1)	COM'L	S	640	900	520	740	mA
			IND	S	—	—	520	900	
I_{SB1}(6)	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ = $\overline{CE}_R$ = V_{IH} f = f_{MAX}(1)	COM'L	S	350	460	280	380	mA
			IND	S	—	—	280	470	
I_{SB2}(6)	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_{"A"}$ = V_{IL} and $\overline{CE}_{"B"}$ = V_{IH}(5) Active Port Outputs Disabled, f=f_{MAX}(1)	COM'L	S	500	650	400	500	mA
			IND	S	—	—	400	620	
I_{SB3}	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{DDQ}$ - 0.2V, $V_{IN} \geq V_{DDQ}$ - 0.2V or $V_{IN} \leq$ 0.2V, f = 0(2)	COM'L	S	12	20	12	20	mA
			IND	S	—	—	12	25	
I_{SB4}(6)	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}_{"A"} \leq$ 0.2V and $\overline{CE}_{"B"} \geq V_{DDQ}$ - 0.2V(5) $V_{IN} \geq V_{DDQ}$ - 0.2V or $V_{IN} \leq$ 0.2V Active Port, Outputs Disabled, f = f_{MAX}(1)	COM'L	S	500	650	400	500	mA
			IND	S	—	—	400	620	
I_{ZZ}	Sleep Mode Current (Both Ports - TTL Level Inputs)	ZZ_L = ZZ_R = V_{IH} f=f_{MAX}(1)	COM'L	S	12	20	12	20	mA
			IND	S	—	—	12	25	

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NOTES:
1. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of 1/t_{CYC}, using "AC TEST CONDITIONS".
2. f = 0 means no address, clock, or control lines change. Applies only to input at CMOS level standby.
3. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
4. V_{DD} = 2.5V, T_A = 25°C for Typ, and are not production tested. $I_{DD\,DC}$(f=0) = 30mA (Typ).
5. $\overline{CE}_X$ = V_{IL} means $\overline{CE}_{0X}$ = V_{IL} and CE_{1X} = V_{IH}
   $\overline{CE}_X$ = V_{IH} means $\overline{CE}_{0X}$ = V_{IH} or CE_{1X} = V_{IL}
   $\overline{CE}_X \leq$ 0.2V means $\overline{CE}_{0X} \leq$ 0.2V and $CE_{1X} \geq V_{DDQ}$ - 0.2V
   $\overline{CE}_X \geq V_{DDQ}$ - 0.2V means $\overline{CE}_{0X} \geq V_{DDQ}$ - 0.2V or CE_{1X} - 0.2V
   "X" represents "L" for left port or "R" for right port.
6. I_{SB1}, I_{SB2} and I_{SB4} will all reach full standby levels (I_{SB3}) on the appropriate port(s) if ZZ_L and/or ZZ_R = V_{IH}.

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AC Test Conditions (V_{DDQ} - 3.3V/2.5V)

Input Pulse Levels (Address & Controls)	GND to 3.0V/GND to 2.4V
Input Pulse Levels (I/Os)	GND to 3.0V/GND to 2.4V
Input Rise/Fall Times	2ns
Input Timing Reference Levels	1.5V/1.25V
Output Reference Levels	1.5V/1.25V
Output Load	Figure 1

5678 tbl 10

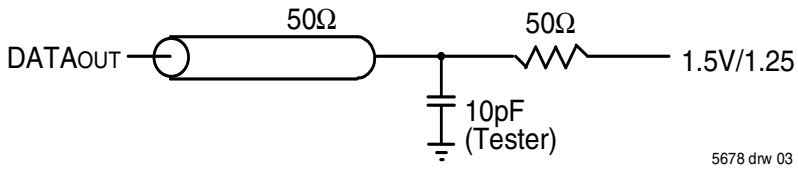
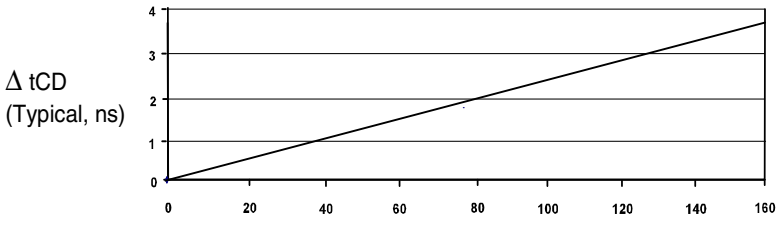


Figure 1. AC Output Test load.



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AC Electrical Characteristics Over the Operating Temperature Range (Read and Write Cycle Timing) [2,3] (V_{DD} = 2.5V ± 100mV, T_A = 0°C to +70°C)

		70T3539MS166 Com'l Only		70T3539MS133 Com'l & Ind		
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
t_{CYC1}	Clock Cycle Time (Flow-Through)[1]	20	—	25	—	ns
t_{CYC2}	Clock Cycle Time (Pipelined)[1]	6	—	7.5	—	ns
t_{CH1}	Clock High Time (Flow-Through)[1]	8	—	10	—	ns
t_{CL1}	Clock Low Time (Flow-Through)[1]	8	—	10	—	ns
t_{CH2}	Clock High Time (Pipelined)[2]	2.4	—	3	—	ns
t_{CL2}	Clock Low Time (Pipelined)[1]	2.4	—	3	—	ns
t_{SA}	Address Setup Time	1.7	—	1.8	—	ns
t_{HA}	Address Hold Time	0.5	—	0.5	—	ns
t_{SC}	Chip Enable Setup Time	1.7	—	1.8	—	ns
t_{HC}	Chip Enable Hold Time	0.5	—	0.5	—	ns
t_{SB}	Byte Enable Setup Time	1.7	—	1.8	—	ns
t_{HB}	Byte Enable Hold Time	0.5	—	0.5	—	ns
t_{SW}	R/W Setup Time	1.7	—	1.8	—	ns
t_{HW}	R/W Hold Time	0.5	—	0.5	—	ns
t_{SD}	Input Data Setup Time	1.7	—	1.8	—	ns
t_{HD}	Input Data Hold Time	0.5	—	0.5	—	ns
t_{SAD}	$\overline{ADS}$ Setup Time	1.7	—	1.8	—	ns
t_{HAD}	$\overline{ADS}$ Hold Time	0.5	—	0.5	—	ns
t_{SCN}	$\overline{CNTEN}$ Setup Time	1.7	—	1.8	—	ns
t_{HCN}	$\overline{CNTEN}$ Hold Time	0.5	—	0.5	—	ns
t_{SRPT}	$\overline{REPEAT}$ Setup Time	1.7	—	1.8	—	ns
t_{HRPT}	$\overline{REPEAT}$ Hold Time	0.5	—	0.5	—	ns
t_{OE}	Output Enable to Data Valid	—	4.4	—	4.6	ns
t_{OLZ}[6]	Output Enable to Output Low-Z	1	—	1	—	ns
t_{OHZ}[6]	Output Enable to Output High-Z	1	3.6	1	4.2	ns
t_{CD1}	Clock to Data Valid (Flow-Through)[1]	—	12	—	15	ns
t_{CD2}	Clock to Data Valid (Pipelined)[1]	—	3.6	—	4.2	ns
t_{DC}	Data Output Hold After Clock High	1	—	1	—	ns
t_{CKHZ}[6]	Clock High to Output High-Z	1	3.6	1	4.2	ns
t_{CKLZ}[6]	Clock High to Output Low-Z	1	—	1	—	ns
t_{INS}	Interrupt Flag Set Time	—	7	—	7	ns
t_{INR}	Interrupt Flag Reset Time	—	7	—	7	ns
t_{COLS}	Collision Flag Set Time	—	3.6	—	4.2	ns
t_{COLR}	Collision Flag Reset Time	—	3.6	—	4.2	ns
t_{ZZSC}	Sleep Mode Set Cycles	2	—	2	—	cycles
t_{ZZRC}	Sleep Mode Recovery Cycles	3	—	3	—	cycles
Port-to-Port Delay						
t_{CO}	Clock-to-Clock Offset	5	—	6	—	ns
t_{OFS}	Clock-to-Clock Offset for Collision Detection	Please refer to Collision Detection Timing Table on Page 19				

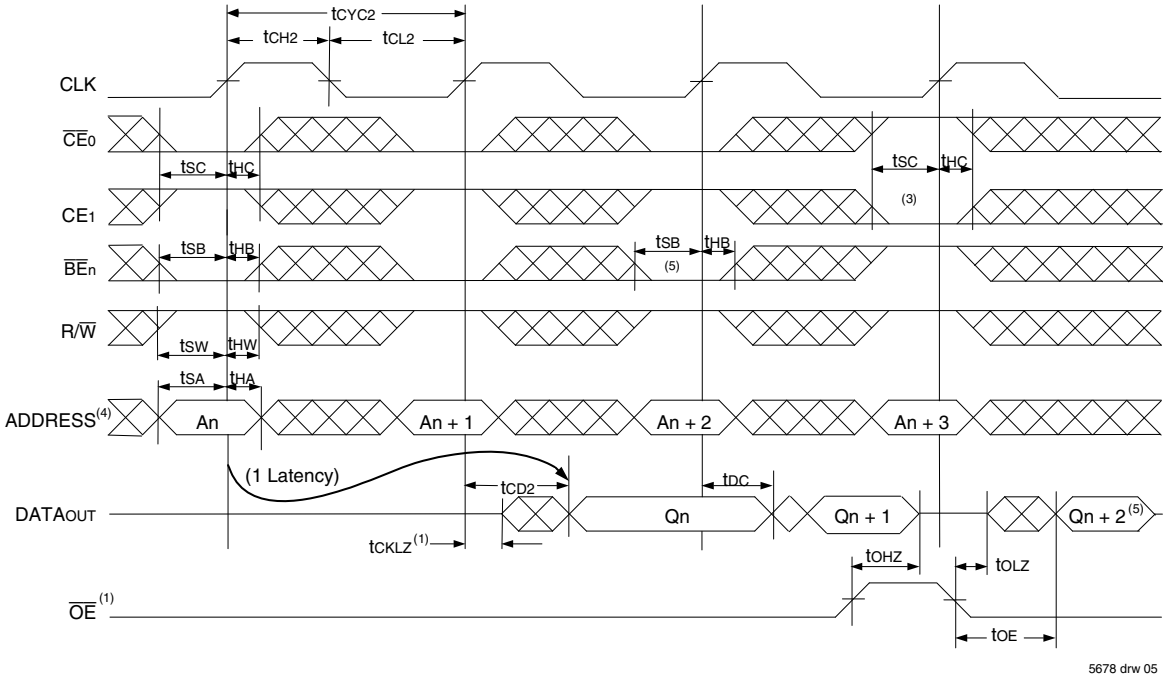
5678 tbl 11

NOTES:

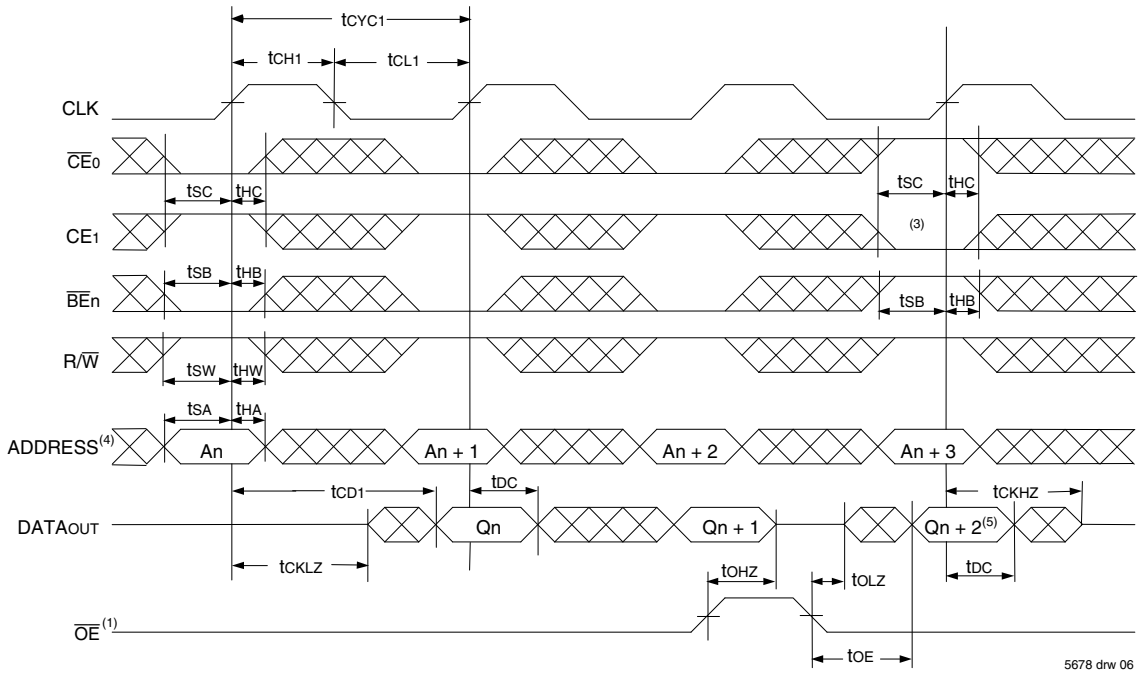
1. The Pipelined output parameters (t_{CYC2}, t_{CD2}) apply to either or both left and right ports when $\overline{FT}$/PIPEx = V_{DD} (2.5V). Flow-through parameters (t_{CYC1}, t_{CD1}) apply when $\overline{FT}$/PIPE = V_{SS} (0V) for that port.
2. All input signals are synchronous with respect to the clock except for the asynchronous Output Enable ($\overline{OE}$), $\overline{FT}$/PIPE and OPT. $\overline{FT}$/PIPE and OPT should be treated as DC signals, i.e. steady state during operation.
3. These values are valid for either level of V_{DDQ} (3.3V/2.5V). See page 6 for details on selecting the desired operating voltage levels for each port.
4. Guaranteed by design (not production tested).

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Timing Waveform of Read Cycle for Pipelined Operation ($\overline{FT}$/PIPE'X' = VIH)(1,2)



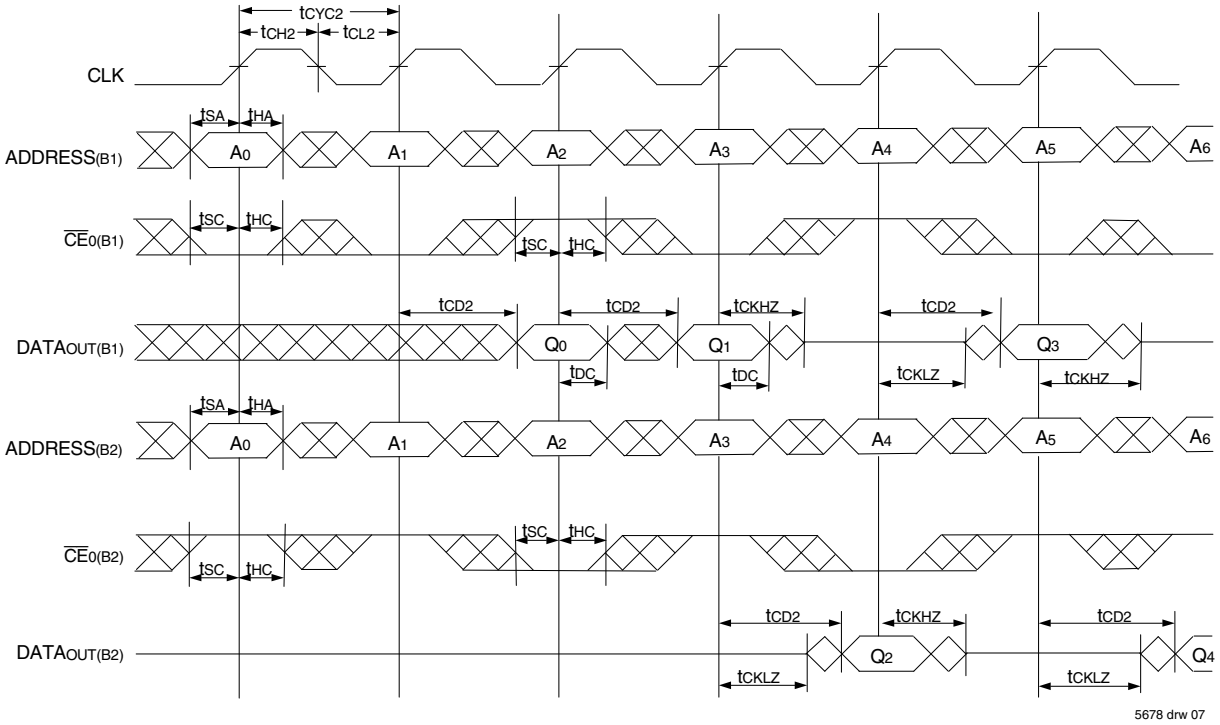
Timing Waveform of Read Cycle for Flow-through Output ($\overline{FT}$/PIPE"X" = VIL)(1,2,6)



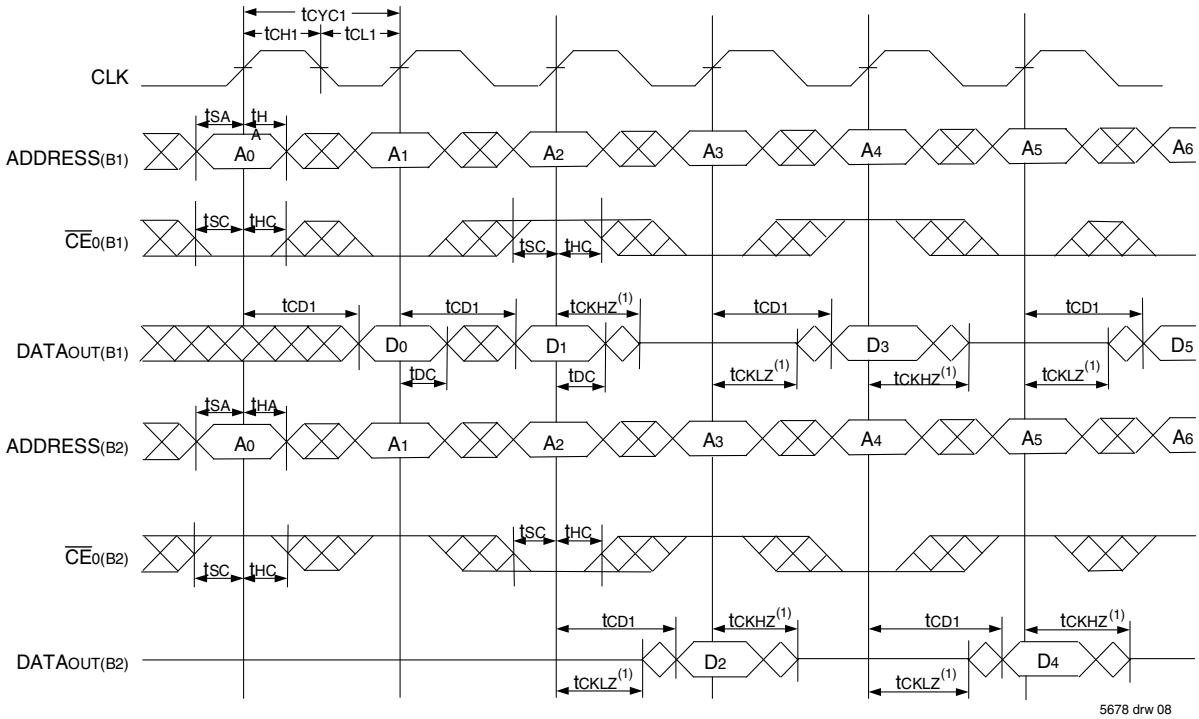
NOTES:
1. $\overline{OE}$ is asynchronously controlled; all other inputs depicted in the above waveforms are synchronous to the rising clock edge.
2. $\overline{ADS}$ = VIL, $\overline{CNTEN}$ and $\overline{REPEAT}$ = VIH.
3. The output is disabled (High-Impedance state) by $\overline{CE}_0$ = VIH, CE1 = VIL, $\overline{BE}_n$ = VIH following the next rising edge of the clock. Refer to Truth Table 1.
4. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = VIL constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. If $\overline{BE}_n$ was HIGH, then the appropriate Byte of DATAOUT for Qn + 2 would be disabled (High-Impedance state).
6. "x" denotes Left or Right port. The diagram is with respect to that port.

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Timing Waveform of a Multi-Device Pipelined Read(1,2)



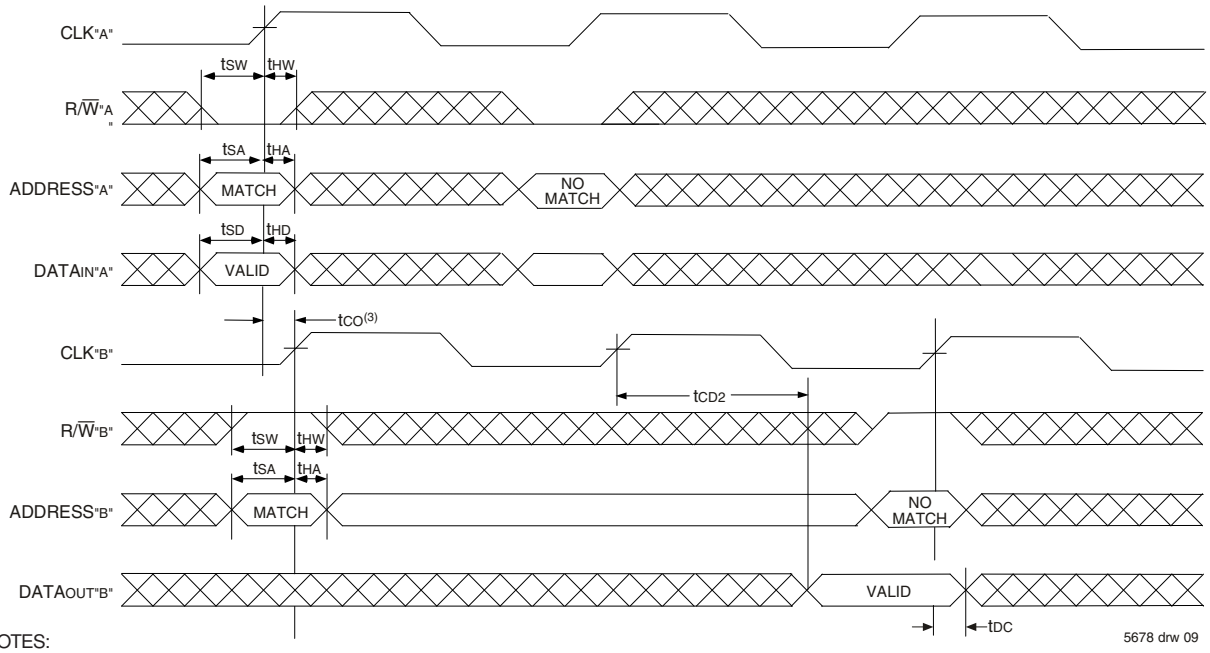
Timing Waveform of a Multi-Device Flow-Through Read(1,2)



NOTES:
1. B1 Represents Device #1; B2 Represents Device #2. Each Device consists of one IDT70T3539M for this waveform, and are setup for depth expansion in this example. ADDRESS(B1) = ADDRESS(B2) in this situation.
2. $\overline{BE}_n$, $\overline{OE}$, and $\overline{ADS}$ = V_{IL}; $CE_{1(B1)}$, $CE_{1(B2)}$, R/$\overline{W}$, $\overline{CNTEN}$, and $\overline{REPEAT}$ = V_{IH}.

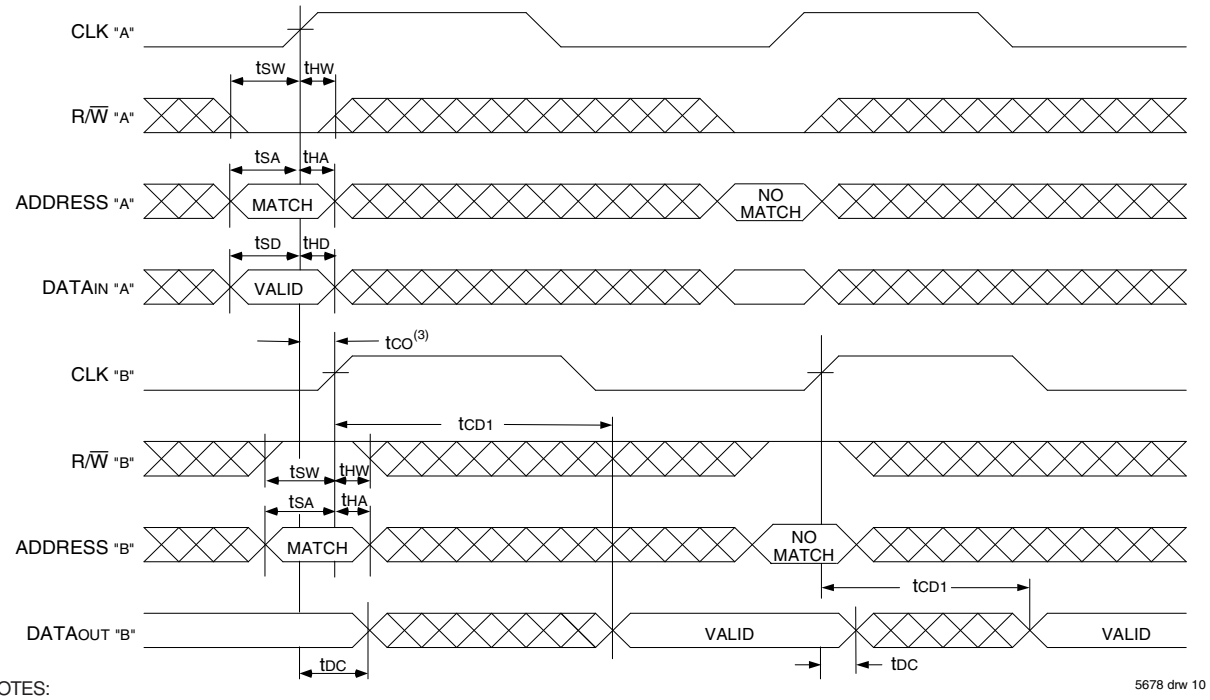
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Timing Waveform of Left Port Write to Pipelined Right Port Read(1,2,4)



NOTES:
1. $\overline{CE_0}$, $\overline{BE_n}$, and $\overline{ADS}$ = V_{IL}; CE_1, $\overline{CNTEN}$, and $\overline{REPEAT}$ = V_{IH}.
2. $\overline{OE}$ = V_{IL} for Port "B", which is being read from. $\overline{OE}$ = V_{IH} for Port "A", which is being written to.
3. If $t_{CO} \leq$ minimum specified, then data from Port "B" read is not valid until following Port "B" clock cycle (ie, time from write to valid read on opposite port will be t_{CO} + 2 t_{CYC2} + t_{CD2}). If t_{CO} > minimum, then data from Port "B" read is available on first Port "B" clock cycle (ie, time from write to valid read on opposite port will be t_{CO} + t_{CYC2} + t_{CD2}).
4. All timing is the same for Left and Right ports. Port "A" may be either Left or Right port. Port "B" is the opposite of Port "A"

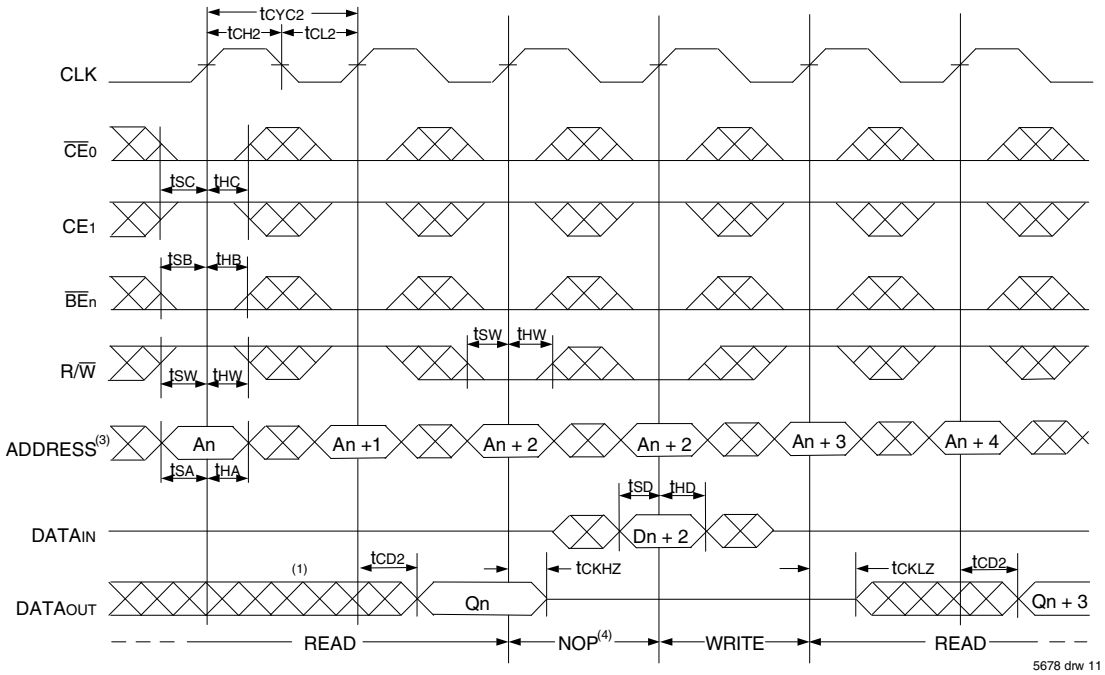
Timing Waveform with Port-to-Port Flow-Through Read(1,2,4)



NOTES:
1. $\overline{CE_0}$, $\overline{BE_n}$, and $\overline{ADS}$ = V_{IL}; CE_1, $\overline{CNTEN}$, and $\overline{REPEAT}$ = V_{IH}.
2. $\overline{OE}$ = V_{IL} for the Right Port, which is being read from. $\overline{OE}$ = V_{IH} for the Left Port, which is being written to.
3. If $t_{CO} \leq$ minimum specified, then data from Port "B" read is not valid until following Port "B" clock cycle (i.e., time from write to valid read on opposite port will be t_{CO} + t_{CYC} + t_{CD1}). If t_{CO} > minimum, then data from Port "B" read is available on first Port "B" clock cycle (i.e., time from write to valid read on opposite port will be t_{CO} + t_{CD1}).
4. All timing is the same for both left and right ports. Port "A" may be either left or right port. Port "B" is the opposite of Port "A".

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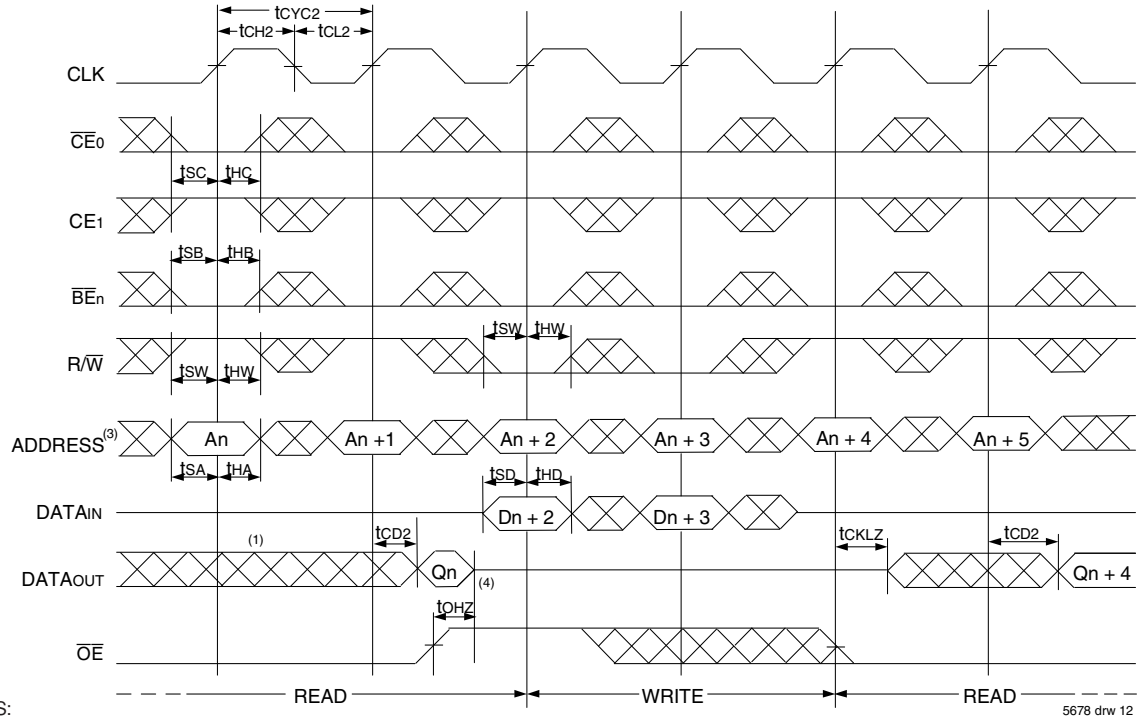
Timing Waveform of Pipelined Read-to-Write-to-Read ($\overline{OE}$ = VIL)(2)



NOTES:

1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2. $\overline{CE_0}$, $\overline{BE_n}$, and $\overline{ADS}$ = VIL; CE1, $\overline{CNTEN}$, and $\overline{REPEAT}$ = VIH. "NOP" is "No Operation".
3. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = VIL constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

Timing Waveform of Pipelined Read-to-Write-to-Read ($\overline{OE}$ Controlled)(2)

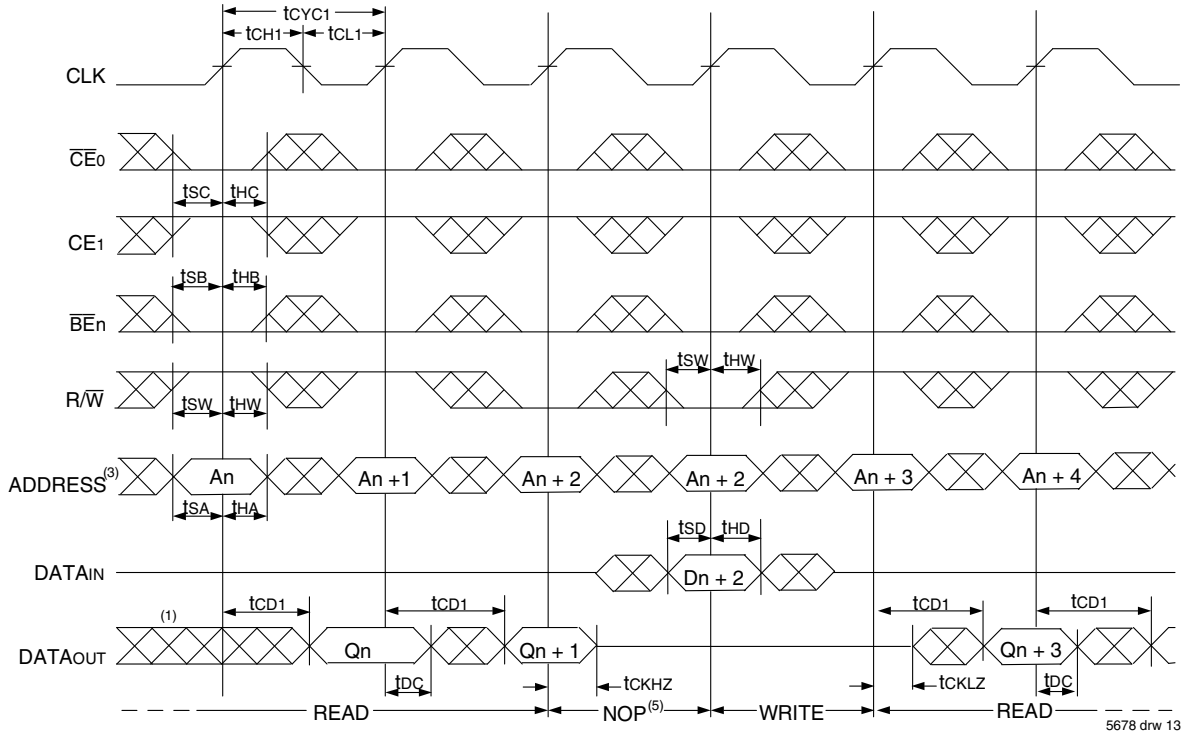


NOTES:

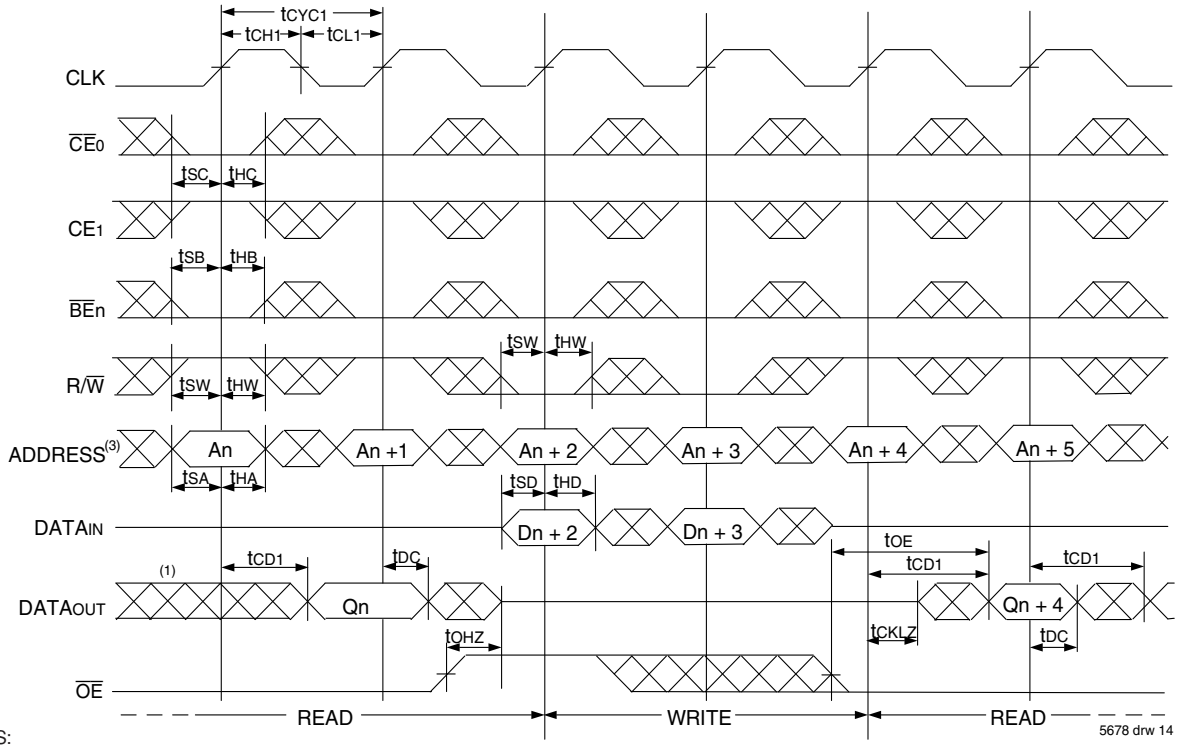
1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2. $\overline{CE_0}$, $\overline{BE_n}$, and $\overline{ADS}$ = VIL; CE1, $\overline{CNTEN}$, and $\overline{REPEAT}$ = VIH.
3. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = VIL constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. This timing does not meet requirements for fastest speed grade. This waveform indicates how logically it could be done if timing so allows.

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Timing Waveform of Flow-Through Read-to-Write-to-Read ($\overline{OE}$ = VIL)(2)



Timing Waveform of Flow-Through Read-to-Write-to-Read ($\overline{OE}$ Controlled)(2)

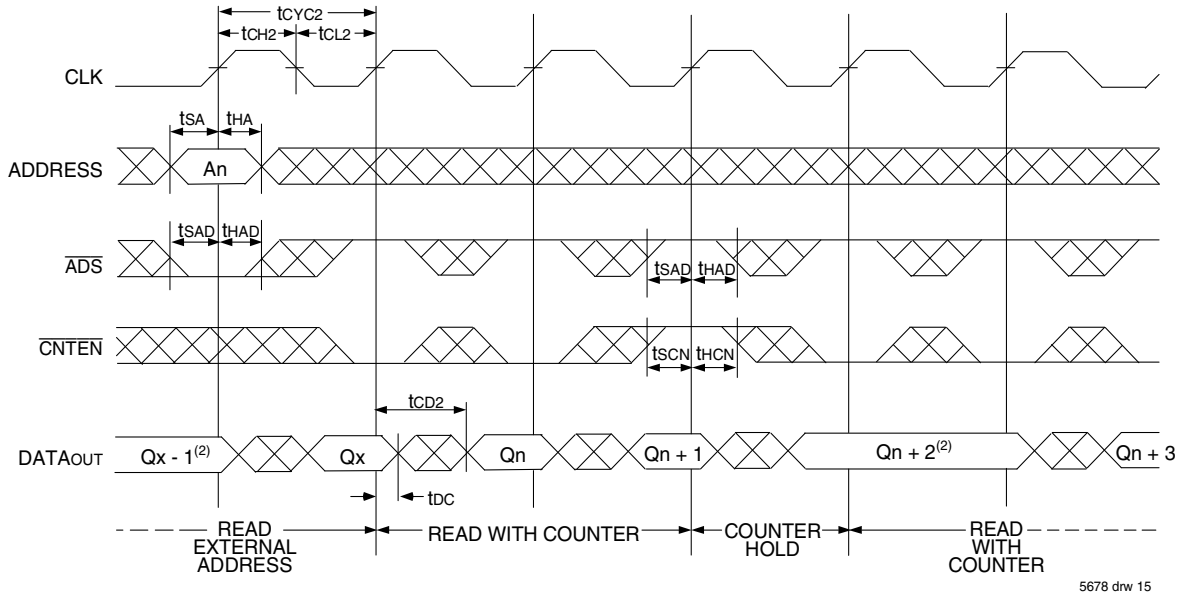


NOTES:

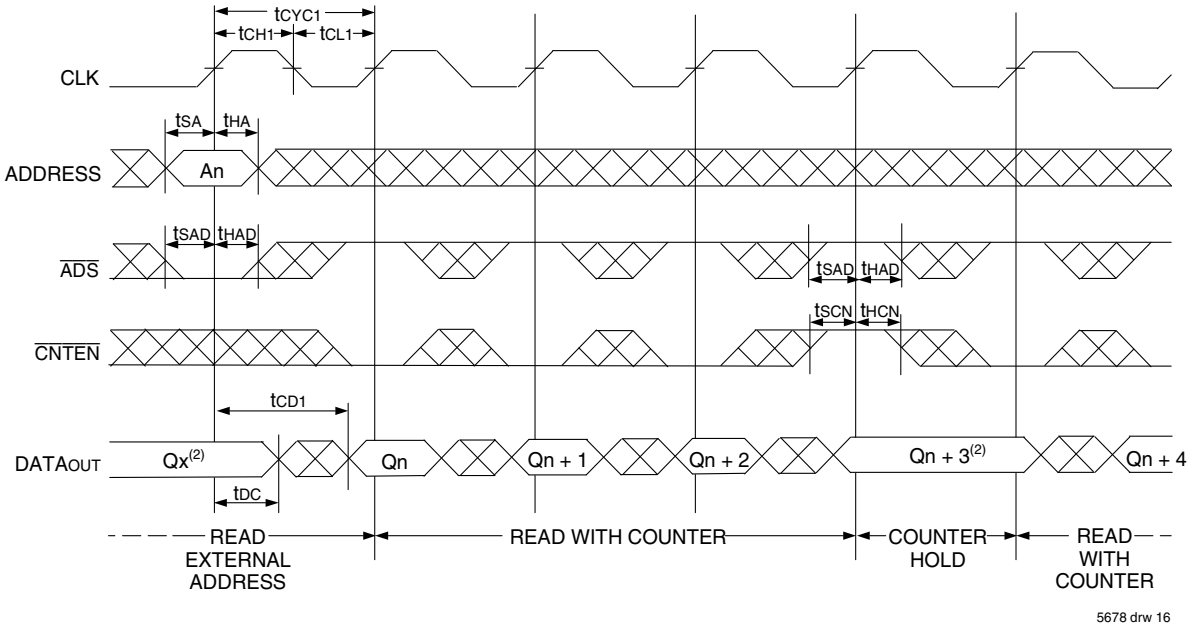
1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2. $\overline{CE_0}$, $\overline{BE}n$, and $\overline{ADS}$ = VIL; CE1, $\overline{CNTEN}$, and $\overline{REPEAT}$ = VIH.
3. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = VIL constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

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Timing Waveform of Pipelined Read with Address Counter Advance(1)



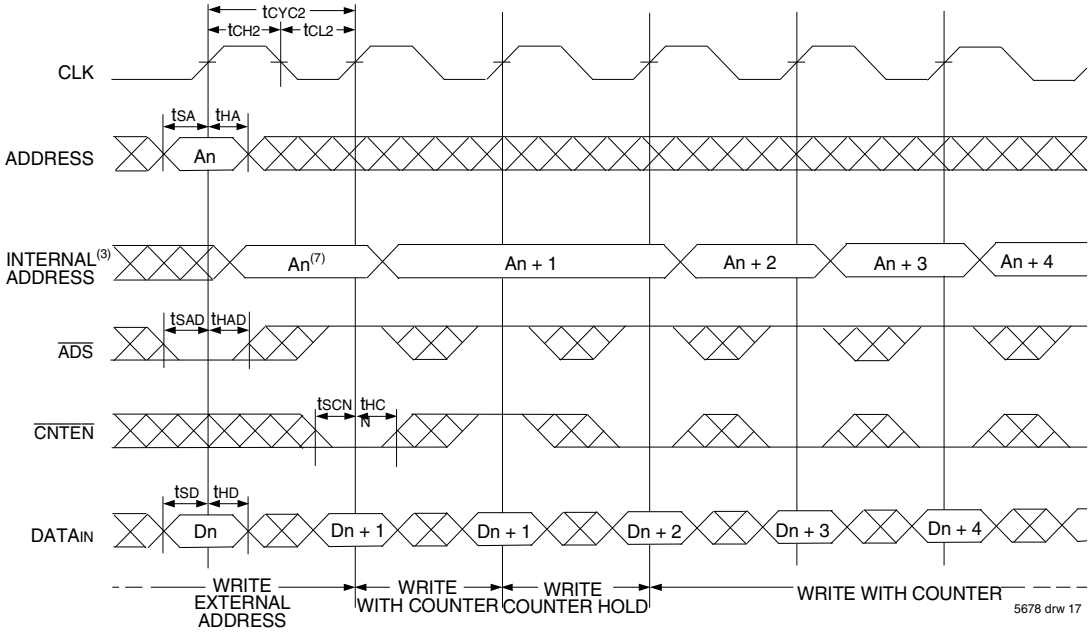
Timing Waveform of Flow-Through Read with Address Counter Advance(1)



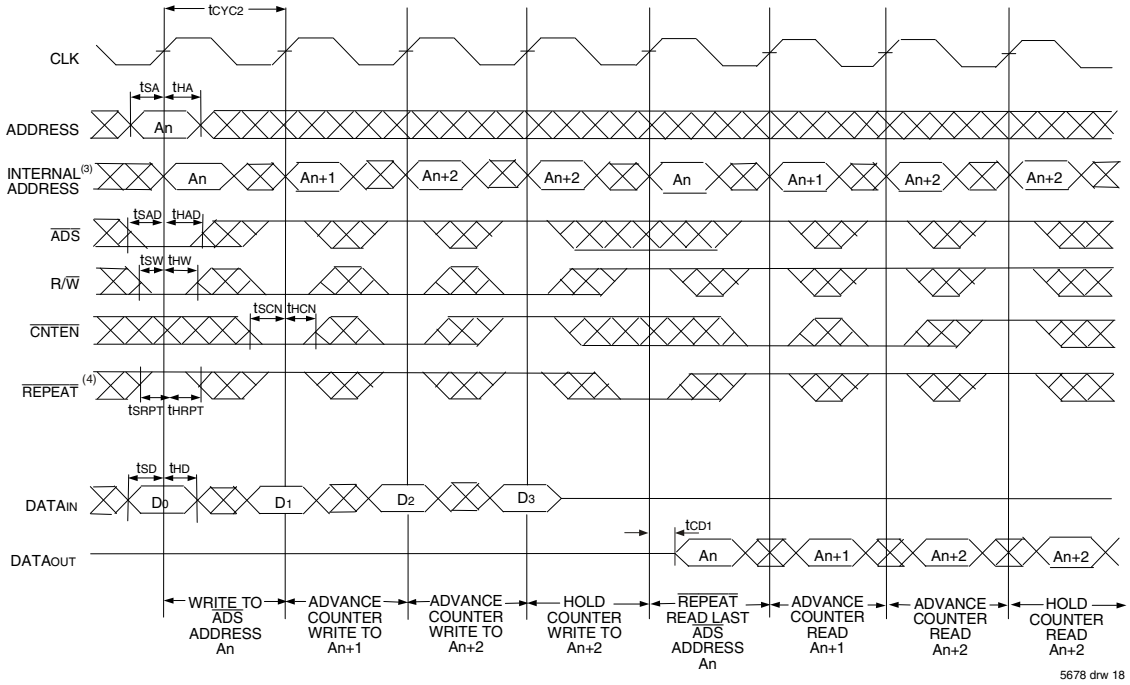
NOTES:
1. $\overline{CE_0}$, $\overline{OE}$, $\overline{BE_n}$ = V_{IL}; CE_1, R/$\overline{W}$, and $\overline{REPEAT}$ = V_{IH}.
2. If there is no address change via $\overline{ADS}$ = V_{IL} (loading a new address) or $\overline{CNTEN}$ = V_{IL} (advancing the address), i.e. $\overline{ADS}$ = V_{IH} and $\overline{CNTEN}$ = V_{IH}, then the data output remains constant for subsequent clocks.

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Timing Waveform of Write with Address Counter Advance (Flow-through or Pipelined Inputs)(1)



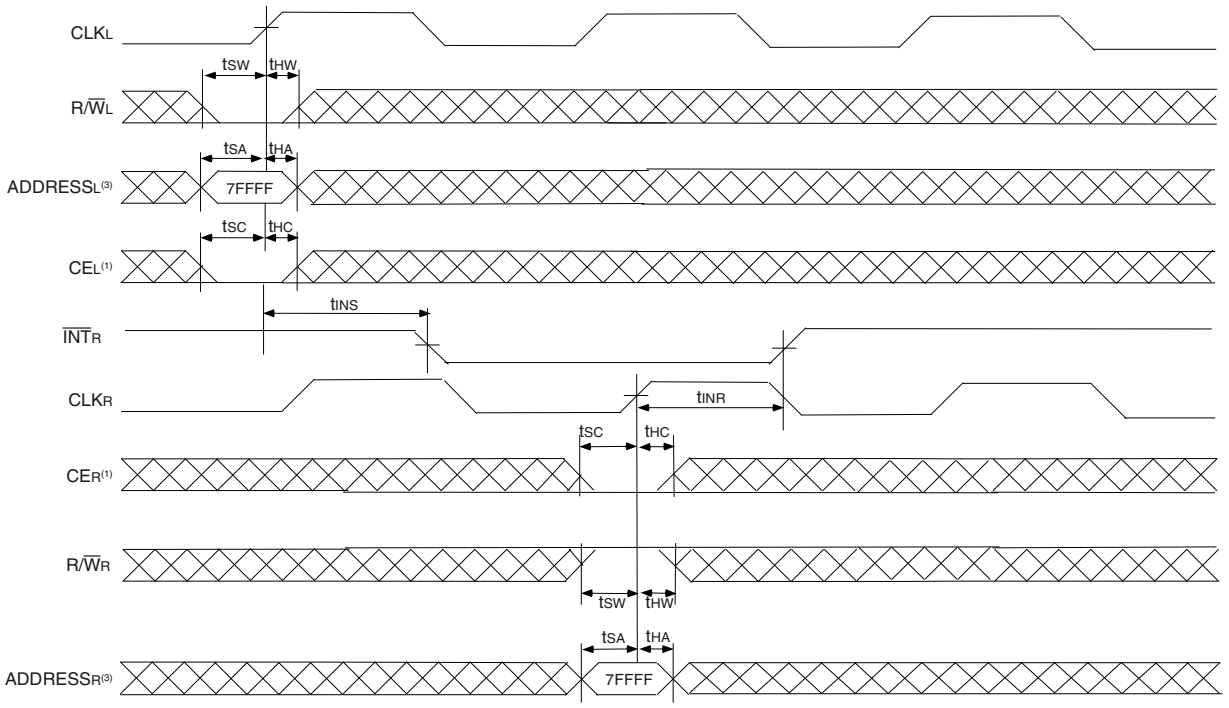
Timing Waveform of Counter Repeat(2,6)



NOTES:
1. $\overline{CE_0}$, $\overline{BE_n}$, and R/$\overline{W}$ = V_{IL}; CE_1 and $\overline{REPEAT}$ = V_{IH}.
2. $\overline{CE_0}$, $\overline{BE_n}$ = V_{IL}; CE_1 = V_{IH}.
3. The "Internal Address" is equal to the "External Address" when $\overline{ADS}$ = V_{IL} and equals the counter output when $\overline{ADS}$ = V_{IH}.
4. No dead cycle exists during $\overline{REPEAT}$ operation. A READ or WRITE cycle may be coincidental with the counter $\overline{REPEAT}$ cycle: Address loaded by last valid $\overline{ADS}$ load will be accessed. For more information on $\overline{REPEAT}$ function refer to Truth Table II.
5. $\overline{CNTEN}$ = V_{IL} advances Internal Address from 'An' to 'An +1'. The transition shown indicates the time required for the counter to advance. The 'An +1'Address is written to during this cycle.
6. For Pipelined Mode user should add 1 cycle latency for outputs as per timing waveform of read cycle for pipelined operations.

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Waveform of Interrupt Timing(2)



5678 drw 19

NOTES:
1. $\overline{CE}_0$ = V_{IL} and CE_1 = V_{IH}
2. All timing is the same for Left and Right ports.
3. Address is for internal register, not the external bus, i.e., address needs to be qualified by one of the Address counter control signals.

Truth Table III — Interrupt Flag(1)

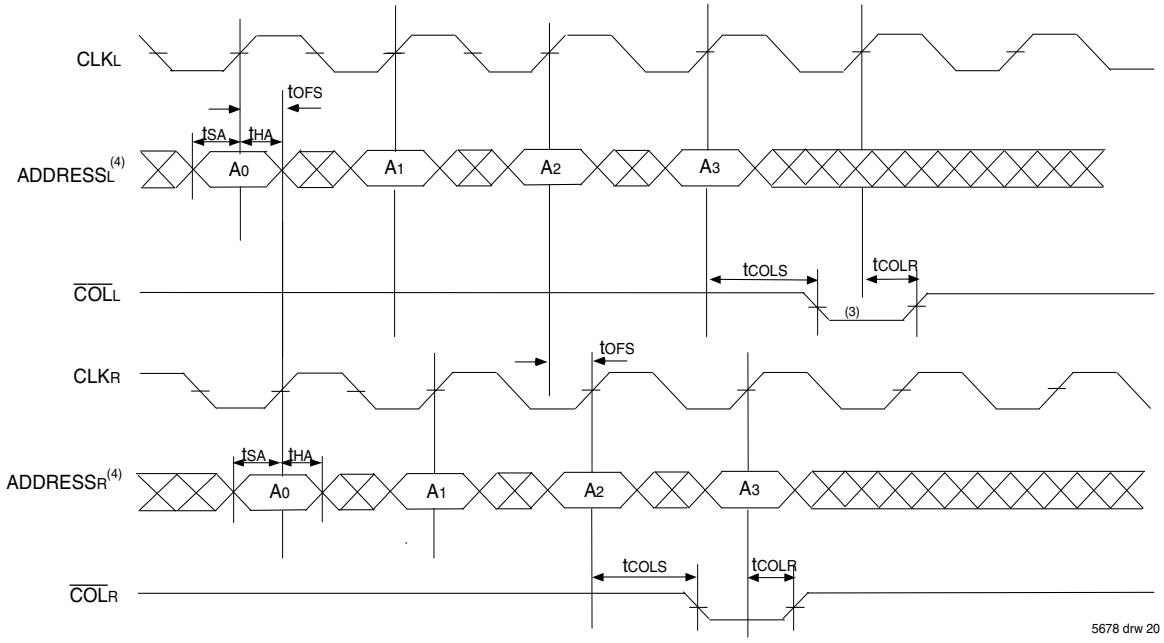
Left Port					Right Port					
CLKL	R/$\overline{W}$L(2)	$\overline{CE}$L(2)	A18L-A0L	$\overline{INT}$L	CLKR	R/$\overline{W}$R(2)	$\overline{CE}$R(2)	A18R-A0R	$\overline{INT}$R	Function
↑	L	L	7FFFF	X	↑	X	X	X	L	Set Right $\overline{INT}$R Flag
↑	X	X	X	X	↑	H	L	7FFFF	H	Reset Right $\overline{INT}$R Flag
↑	X	X	X	L	↑	L	L	7FFFE	X	Set Left $\overline{INT}$L Flag
↑	H	L	7FFFE	H	↑	X	X	X	X	Reset Left $\overline{INT}$L Flag

5678 tbl 12

NOTES:
1. $\overline{INT}_L$ and $\overline{INT}_R$ must be initialized at power-up by Resetting the flags.
2. $\overline{CE}_0$ = V_{IL} and CE_1 = V_{IH}. R/$\overline{W}$ and CE are synchronous with respect to the clock and need valid set-up and hold times.
3. Address is for internal register, not the external bus, i.e., address needs to be qualified by one of the Address counter control signals.

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Waveform of Collision Timing(1,2)



NOTES:
1. $\overline{CE}_0$ = V_{IL}, CE_1 = V_{IH}.
2. For reading port, $\overline{OE}$ is a Don't care on the Collision Detection Logic. Please refer to Truth Table IV for specific cases.
3. Leading Port Output flag might output $3t_{CYC2} + t_{COLS}$ after Address match.
4. Address is for internal register, not the external bus, i.e., address needs to be qualified by one of the Address counter control signals.

Collision Detection Timing(3,4)

Cycle Time	t_{OFS} (ns)	
	Region 1 (ns) (1)	Region 2 (ns) (2)
5ns	0 - 2.8	2.81 - 4.6
6ns	0 - 3.8	3.81 - 5.6
7.5ns	0 - 5.3	5.31 - 7.1

5678 tbl 13

NOTES:
1. Region 1
   Both ports show collision after 2nd cycle for Addresses 0, 2, 4 etc.
2. Region 2
   Leading port shows collision after 3rd cycle for addresses 0, 3, 6, etc. while trailing port shows collision after 2nd cycle for addresses 0, 2, 4 etc.
3. All the production units are tested to midpoint of each region.
4. These ranges are based on characterization of a typical device.

Truth Table IV — Collision Detection Flag

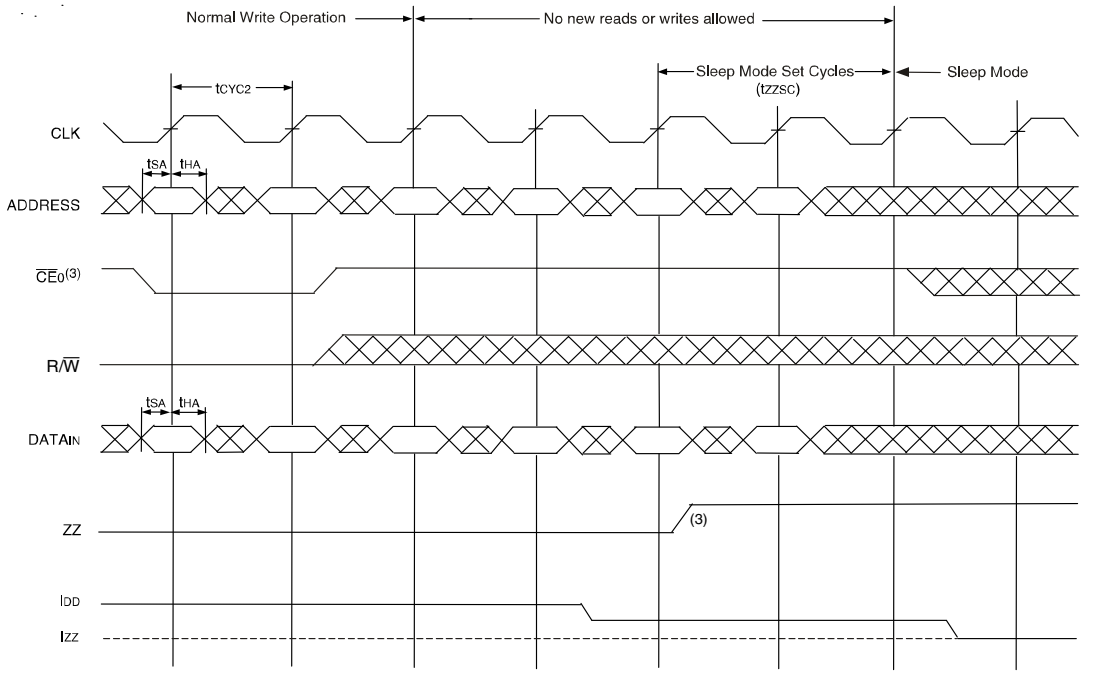
Left Port					Right Port					Function
CLK_L	$R/\overline{W}_L$(1)	CE_L(1)	A_{18L}-A_{0L}(2)	$\overline{COL}_L$	CLK_R	$R/\overline{W}_R$(1)	CE_R(1)	A_{18R}-A_{0R}(2)	$\overline{COL}_R$	
↑	H	L	MATCH	H	↑	H	L	MATCH	H	Both ports reading. Not a valid collision. No flag output on either port.
↑	H	L	MATCH	L	↑	L	L	MATCH	H	Left port reading, Right port writing. Valid collision, flag output on Left port.
↑	L	L	MATCH	H	↑	H	L	MATCH	L	Right port reading, Left port writing. Valid collision, flag output on Right port.
↑	L	L	MATCH	L	↑	L	L	MATCH	L	Both ports writing. Valid collision. Flag output on both ports.

5678 tbl 14

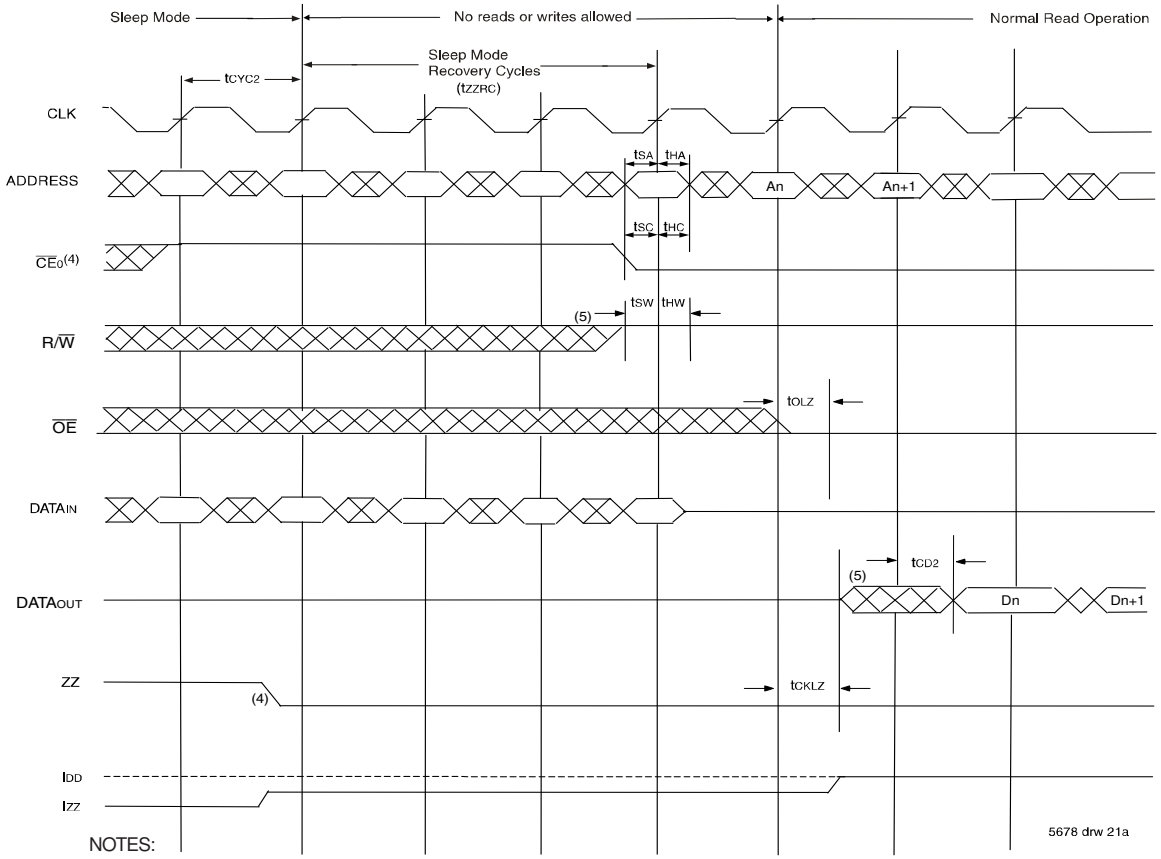
NOTES:
1. $\overline{CE}_0$ = V_{IL} and CE_1 = V_{IH}. $R/\overline{W}$ and CE are synchronous with respect to the clock and need valid set-up and hold times.
2. Address is for internal register, not the external bus, i.e., address needs to be qualified by one of the Address counter control signals.

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Timing Waveform - Entering Sleep Mode (1,2)



Timing Waveform - Exiting Sleep Mode (1,2)



NOTES:

1. $CE_1 = V_{IH}$.
2. All timing is same for Left and Right ports.
3. $\overline{CE}_0$ has to be deactivated ($\overline{CE}_0 = V_{IH}$) three cycles prior to asserting ZZ ($ZZ_x = V_{IH}$) and held for two cycles after asserting ZZ ($ZZ_x = V_{IH}$).
4. $\overline{CE}_0$ has to be deactivated ($\overline{CE}_0 = V_{IH}$) one cycle prior to de-asserting ZZ ($ZZ_x = V_{IL}$) and held for three cycles after de-asserting ZZ ($ZZ_x = V_{IL}$).
5. The device must be in Read Mode ($R/\overline{W}$ High) when exiting sleep mode. Outputs are active but data is not valid until the following cycle.

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Functional Description

The IDT70T3539M provides a true synchronous Dual-Port Static RAM interface. Registered inputs provide minimal set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal, however, the self-timed internal write pulse width is independent of the cycle time.

An asynchronous output enable is provided to ease asynchronous bus interfacing. Counter enable inputs are also provided to stall the operation of the address counters for fast interleaved memory applications.

A HIGH on $\overline{CE}_0$ or a LOW on CE_1 for one clock cycle will power down the internal circuitry to reduce static power consumption. Multiple chip enables allow easier banking of multiple IDT70T3539Ms for depth expansion configurations. Two cycles are required with $\overline{CE}_0$ LOW and CE_1 HIGH to re-activate the outputs.

Interrupts

If the user chooses the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is asserted when the right port writes to memory location 7FFFE (HEX), where a write is defined as $\overline{CE}_R$ = R/$\overline{W}_R$ = V_{IL} per the Truth Table. The left port clears the interrupt through access of address location 7FFFE when $\overline{CE}_L$ = V_{IL} and R/$\overline{W}$L = V_{IH}. Likewise, the right port interrupt flag ($\overline{INT}_R$) is asserted when the left port writes to memory location 7FFFF (HEX) and to clear the interrupt flag ($\overline{INT}_R$), the right port must read the memory location 7FFFF. The message (36 bits) at 7FFFE or 7FFFF is user-defined since it is an addressable SRAM location. If the interrupt function is not used, address locations 7FFFE and 7FFFF are not used as mail boxes, but as part of the random access memory. Refer to Truth Table III for the interrupt operation.

Collision Detection

Collision is defined as an overlap in access between the two ports resulting in the potential for either reading or writing incorrect data to a specific address. For the specific cases: (a) Both ports reading - no data is corrupted, lost, or incorrectly output, so no collision flag is output on either port. (b) One port writing, the other port reading - the end result of the write will still be valid. However, the reading port might capture data that is in a state of transition and hence the reading port's collision flag is output. (c) Both ports writing - there is a risk that the two ports will interfere with each other, and the data stored in memory will not be a valid write from either port (it may essentially be a random combination of the two). Therefore, the collision flag is output on both ports. Please refer to Truth Table IV for all of the above cases.

The alert flag ($\overline{COL}_x$) is asserted on the 2nd or 3rd rising clock edge of the affected port following the collision, and remains low for one cycle. Please refer to Collision Detection Timing Table on Page 19. During that next cycle, the internal arbitration is engaged in resetting the alert flag (this avoids a specific requirement on the part of the user to reset the alert flag). If two collisions occur on subsequent clock cycles, the second collision may not generate the appropriate alert flag. A third collision will generate the alert flag as appropriate. In the event that a user initiates a burst access on both ports with the same starting address on both ports and one or both ports writing during each access (i.e., imposes a long string of collisions on contiguous clock cycles), the alert flag will be asserted and cleared every other cycle. Please refer to the Collision Detection timing waveform on Page 19.

Collision detection on the IDT70T3539M represents a significant advance in functionality over current sync multi-ports, which have no such capability. In addition to this functionality the IDT70T3539M sustains the key features of bandwidth and flexibility. The collision detection function is very useful in the case of bursting data, or a string of accesses made to sequential addresses, in that it indicates a problem within the burst, giving the user the option of either repeating the burst or continuing to watch the alert flag to see whether the number of collisions increases above an acceptable threshold value. Offering this function on chip also allows users to reduce their need for arbitration circuits, typically done in CPLD's or FPGA's. This reduces board space and design complexity, and gives the user more flexibility in developing a solution.

Sleep Mode

The IDT70T3539M is equipped with an optional sleep or low power mode on both ports. The sleep mode pin on both ports is asynchronous and active high. During normal operation, the ZZ pin is pulled low. When ZZ is pulled high, the port will enter sleep mode where it will meet lowest possible power conditions. The sleep mode timing diagram shows the modes of operation: Normal Operation, No Read/Write Allowed and Sleep Mode.

For normal operation all inputs must meet setup and hold times prior to sleep and after recovering from sleep. Clocks must also meet cycle high and low times during these periods. Three cycles prior to asserting ZZ (ZZx = V_{IH}) and three cycles after de-asserting ZZ (ZZx = V_{IL}), the device must be disabled via the chip enable pins. If a write or read operation occurs during these periods, the memory array may be corrupted. Validity of data out from the RAM cannot be guaranteed immediately after ZZ is asserted (prior to being in sleep). When exiting sleep mode, the device must be in Read mode (R/$\overline{W}$x = V_{IH})when chip enable is asserted, and the chip enable must be valid for one full cycle before a read will result in the output of valid data.

During sleep mode the RAM automatically deselects itself. The RAM disconnects its internal clock buffer. The external clock may continue to run without impacting the RAMs sleep current (I_{ZZ}). All outputs will remain in high-Z state while in sleep mode. All inputs are allowed to toggle. The RAM will not be selected and will not perform any reads or writes.

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Depth and Width Expansion

The IDT70T3539M features dual chip enables (refer to Truth Table I) in order to facilitate rapid and simple depth expansion with no requirements for external logic. Figure 4 illustrates how to control the various chip enables in order to expand two devices in depth.

The IDT70T3539M can also be used in applications requiring expanded width, as indicated in Figure 4. Through combining the control signals, the devices can be grouped as necessary to accommodate applications needing 72-bits or wider.

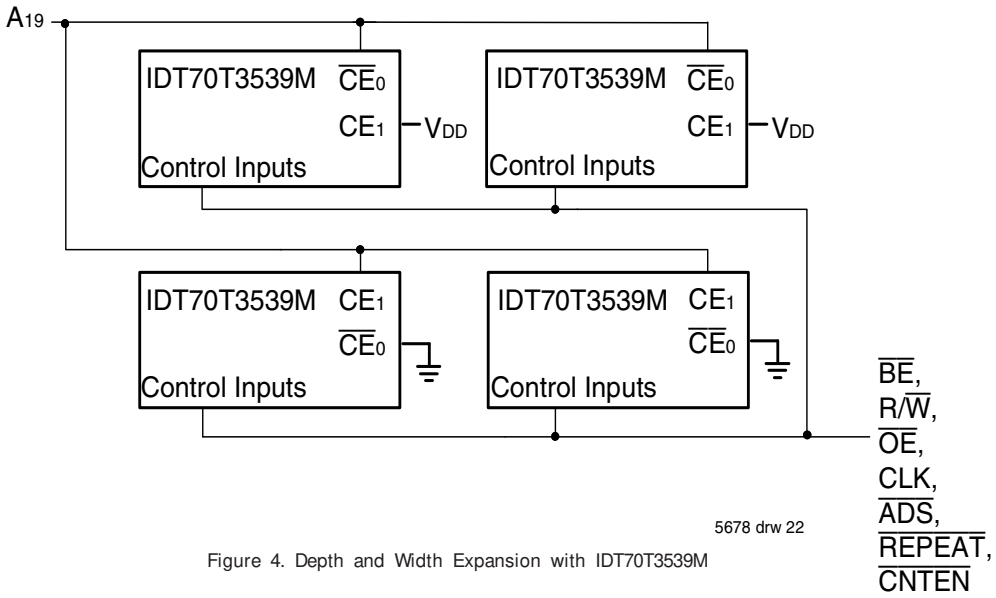


Figure 4. Depth and Width Expansion with IDT70T3539M

JTAG Functionality and Configuration

The IDT70T3539M is composed of two independent memory arrays, and thus cannot be treated as a single JTAG device in the scan chain. The two arrays (A and B) each have identical characteristics and commands but must be treated as separate entities in JTAG operations. Please refer to Figure 5.

JTAG signaling must be provided serially to each array and utilize the information provided in the Identification Register Definitions, Scan Register Sizes, and System Interface Parameter tables. Specifically, commands for Array B must precede those for Array A in any JTAG operations sent to the IDT70T3539M. Please reference Application Note AN-411, "JTAG Testing of Multichip Modules" for specific instructions on performing JTAG testing on the IDT70T3539M. AN-411 is available at www.idt.com.

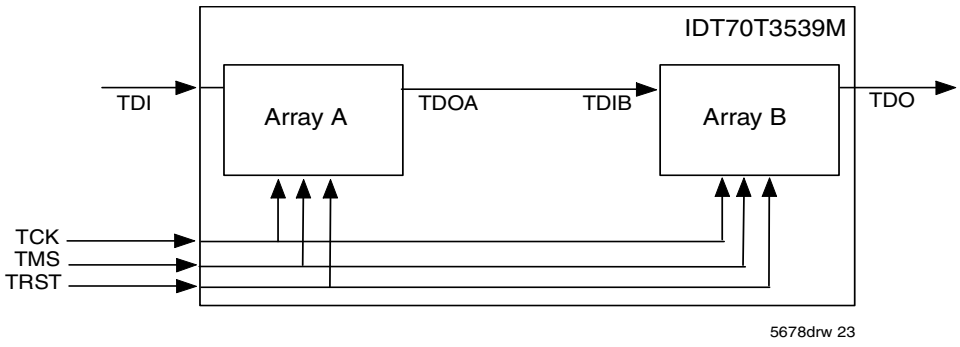


Figure 5. JTAG Configuration for IDT70T3539M

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JTAG Timing Specifications

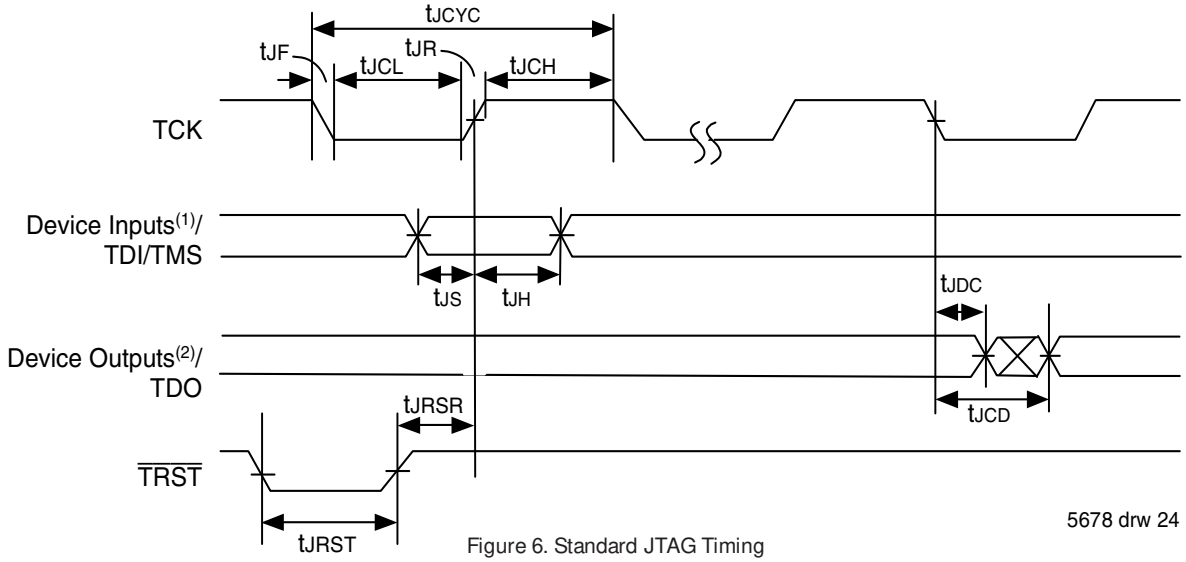


Figure 6. Standard JTAG Timing

NOTES:
1. Device inputs = All device inputs except TDI, TMS, and TRST.
2. Device outputs = All device outputs except TDO.

JTAG AC Electrical Characteristics (1,2,3,4)

Symbol	Parameter	70T3539M		
		Min.	Max.	Units
tJCYC	JTAG Clock Input Period	100	—	ns
tJCH	JTAG Clock HIGH	40	—	ns
tJCL	JTAG Clock Low	40	—	ns
tJR	JTAG Clock Rise Time	—	3(1)	ns
tJF	JTAG Clock Fall Time	—	3(1)	ns
tJRST	JTAG Reset	50	—	ns
tJRSR	JTAG Reset Recovery	50	—	ns
tJCD	JTAG Data Output	—	25	ns
tJDC	JTAG Data Output Hold	0	—	ns
tJS	JTAG Setup	15	—	ns
tJH	JTAG Hold	15	—	ns

5678 tbl 15

NOTES:
1. Guaranteed by design.
2. 30pF loading on external output signals.
3. Refer to AC Electrical Test Conditions stated earlier in this document.
4. JTAG operations occur at one speed (10MHz). The base device may run at any speed specified in this datasheet.

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Identification Register Definitions

Instruction Field Array B	Value Array B	Instruction Field Array A	Value Array A	Description
Revision Number (31:28)	0x0	Revision Number (63:60)	0x0	Reserved for Version number
IDT Device ID (27:12)	0x333	IDT Device ID (59:44)	0x333	Defines IDT Part number
IDT JEDEC ID (11:1)	0x33	IDT JEDEC ID (43:33)	0x33	Allows unique identification of device vendor as IDT
ID Register Indicator Bit (Bit 0)	1	ID Register Indicator Bit (Bit 32)	1	Indicates the presence of an ID Register

5678 tbl 16

Scan Register Sizes

Register Name	Bit Size Array A	Bit Size Array B	Bit Size 70T3539M
Instruction (IR)	4	4	8
Bypass (BYR)	1	1	2
Identification (IDR)	32	32	64
Boundary Scan (BSR)	Note (3)	Note (3)	Note (3)

5678 tbl 17

System Interface Parameters

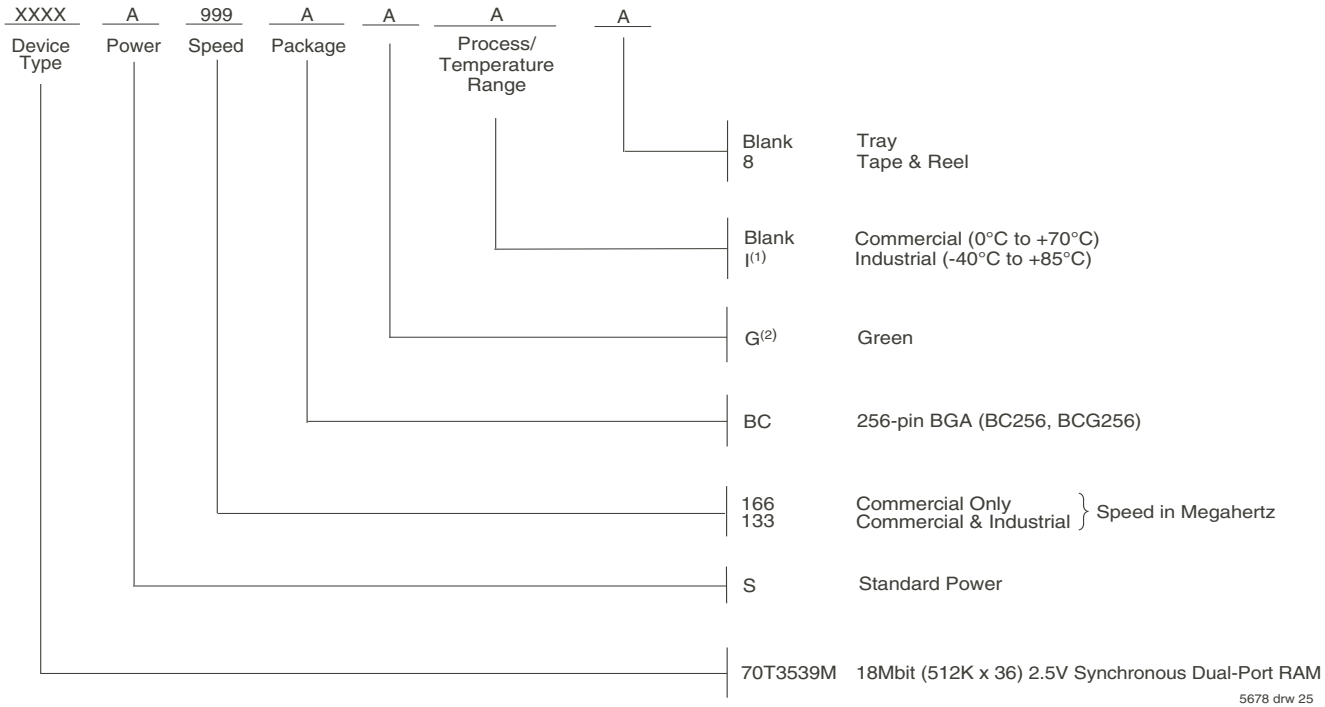
Instruction	Code	Description
EXTEST	00000000	Forces contents of the boundary scan cells onto the device outputs[1]. Places the boundary scan register (BSR) between TDI and TDO.
BYPASS	11111111	Places the bypass register (BYR) between TDI and TDO.
IDCODE	00100010	Loads the ID register (IDR) with the vendor ID code and places the register between TDI and TDO.
HIGHZ	01000100	Places the bypass register (BYR) between TDI and TDO. Forces all device output drivers except $\overline{INT}$x and $\overline{COL}$x to a High-Z state.
CLAMP	00110011	Uses BYR. Forces contents of the boundary scan cells onto the device outputs. Places the bypass register (BYR) between TDI and TDO.
SAMPLE/PRELOAD	00010001	Places the boundary scan register (BSR) between TDI and TDO. SAMPLE allows data from device inputs[2] to be captured in the boundary scan cells and shifted serially through TDO. PRELOAD allows data to be input serially into the boundary scan cells via the TDI.
RESERVED	01010101, 01110111, 10001000, 10011001, 10101010, 10111011, 11001100	Several combinations are reserved. Do not use codes other than those identified above.
PRIVATE	01100110,11101110, 11011101	For internal use only.

5678 tbl 18

NOTES:
1. Device outputs = All device outputs except TDO.
2. Device inputs = All device inputs except TDI, TMS, and $\overline{TRST}$.
3. The Boundary Scan Descriptive Language (BSDL) file for this device is available on the IDT website (www.idt.com), or by contacting your local IDT sales representative.

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Ordering Information



NOTES:

1. Contact your local sales office for industrial temp range for other speeds, packages and powers.
2. Green parts available. For specific speeds, packages and powers contact your sales office.

Orderable Part Information

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
133	70T3539MS133BC	BC256	CABGA	C
	70T3539MS133BC8	BC256	CABGA	C
	70T3539MS133BCG	BCG256	CABGA	C
	70T3539MS133BCGI	BCG256	CABGA	I
	70T3539MS133BCI	BC256	CABGA	I
	70T3539MS133BCI8	BC256	CABGA	I
166	70T3539MS166BC	BC256	CABGA	C
	70T3539MS166BC8	BC256	CABGA	C
	70T3539MS166BCG	BCG256	CABGA	C

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Datasheet Document History:

10/08/03:	Initial Datasheet
10/20/03:	Page 1 Added "Includes JTAG functionality" to features
	Page 25 Added IDT Clock Solution Table
12/04/03:	Page 10 Added t_{OFS} symbol and parameter to AC Electrical Characteristics table
	Page 19 Updated Collision Timing waveform
	Page 19 Added Collision Detection Timing table and footnotes
	Page 22 Added JTAG Configuration and JTAG Functionality descriptions
02/02/04:	Page 8 Changed I_{SB3} and I_{ZZ} in the DC Electrical Characteristics table
04/08/04:	Page 20 & 21 Clarified Sleep Mode Text and Waveform
	Page 22 Added an Application Note, AN-411, reference to the JTAG Functionality and Configuration text
	Page 4 Added another sentence to footnote 4 to recommend that boundary scan not be operated during sleep mode
05/28/04:	Removed "Preliminary" status
07/25/08:	Page 8 Corrected a typo in the footnotes of the DC Chars table
01/29/09:	Page 25 Removed "IDT" from orderable part number
02/04/10:	Page 7 Corrected the Capacitance Table Title
05/15/15:	Page 1 Added Green parts availability to features
	Page 26 Added Tape and Reel and Green indicators with their footnote annotations to the Ordering Information
02/13/18:	Product Discontinuation Notice - PDN# SP-17-02
	Last time buy expires June 15, 2018
06/13/19:	Removed erroneous note PDN#SP-17-02
	Page 3 & 25 The package code BC-256 changed to BC256 and BCG256 to match standard package code
	Page 25 Removed IDT Clock Solutions table
	Page 25 Added Orderable Part Information

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