PS9402

R08DS0014EJ0100
Rev.1.00
Jun 22, 2012

2.5 A OUTPUT CURRENT, HIGH CMR, IGBT, POWER MOS FET GATE DRIVE, 16-PIN SSOP PHOTOCOUPLER

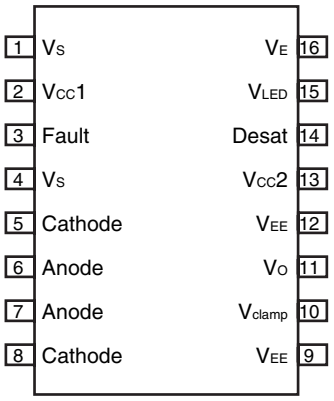
DESCRIPTION

The PS9402 is an optically coupled isolator containing a GaAlAs LED on the input side and a photo diode, a signal processing circuit and a power output transistor on the output side on one chip.
The PS9402 is designed specifically for high common mode transient immunity (CMR), high output current and high switching speed.
The PS9402 includes desaturation detection and active miller clamping functions.
The PS9402 is suitable for driving IGBTs and Power MOS FETs.
The PS9402 is in a 16-pin plastic SSOP (Shrink Small Outline Package). And the PS9402 is able to high-density (surface) mounting.

FEATURES

- Long creepage distance (8 mm MIN.)
- Large peak output current (2.5 A MAX., 2.0 A MIN.)
- High speed switching (t_{PLH}, t_{PHL} = 200 ns MAX.)
- UVLO (Under Voltage Lock Out) protection with hysteresis
- Desaturation detection
- Miller clamping
- High common mode transient immunity ($|CM_H|$, $|CM_L|$ = 25 kV/μs MIN.)
- Embossed tape product: PS9402-E3: 850 pcs/reel
- Pb-Free product
- <R> Safety standards
  - UL approved: No. E72422
  - CSA approved: No. CA 101391 (CA5A, CAN/CSA-C22.2 60065, 60950)
  - DIN EN60747-5-2 (VDE0884 Part2) approved: No. 40024069 (Option)

PIN CONNECTION
(Top View)

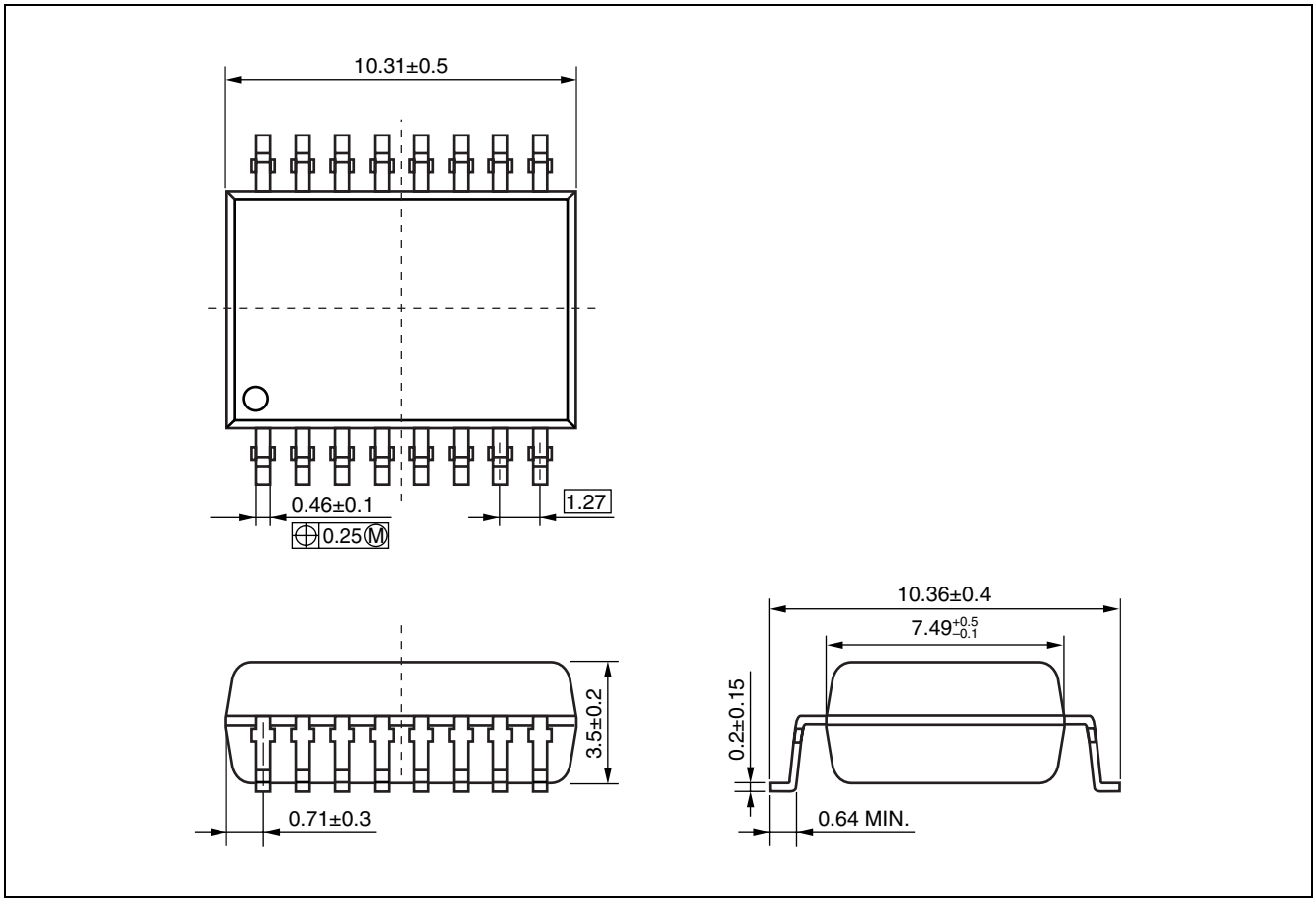


APPLICATIONS

- IGBT, Power MOS FET Gate Driver
- Industrial inverter
- Uninterruptible Power Supply (UPS)

The mark <R> shows major revised points.
The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

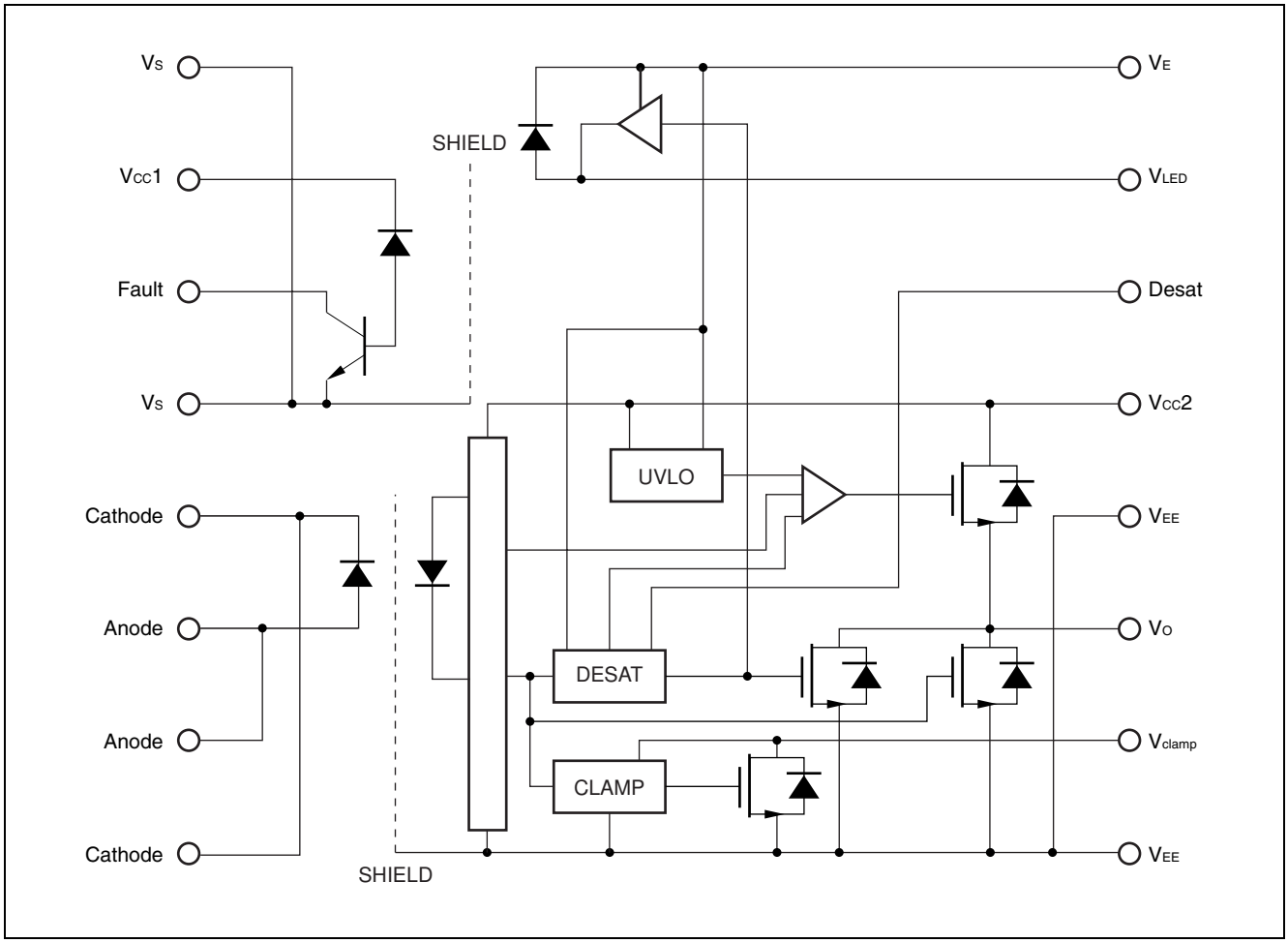
PACKAGE DIMENSIONS (UNIT: mm)



PHOTOCOUPLER CONSTRUCTION

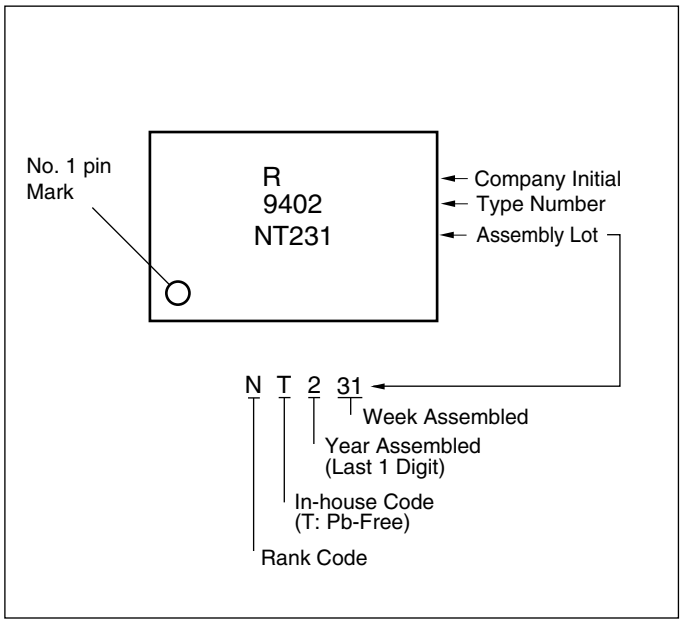
Parameter	Unit (MIN.)
Air Distance	8 mm
Outer Creepage Distance	8 mm
Isolation Distance	0.4 mm

BLOCK DIAGRAM (UNIT: mm)



	I_F	UVLO ($V_{CC}2 - V_{EE}$)	DESAT (Pin 14: DESAT pin input)	FAULT (Pin 3: FAULT pin output)	V_O
<R>	OFF	Not Active (> V_{UVLO+})	Not active	High	Low
<R>	ON	Not Active (> V_{UVLO+})	Low (< $V_{DESATth}$)	High	High
<R>	ON	Not Active (> V_{UVLO+})	High (> $V_{DESATth}$)	Low (FAULT)	Low
<R>	ON	Active (< V_{UVLO-})	Not Active	High	Low
<R>	OFF	Active (< V_{UVLO-})	Not Active	High	Low

<R> MARKING EXAMPLE



ORDERING INFORMATION

Part Number	Order Number	Solder Plating Specification	Packing Style	Safety Standard Approval	Application Part Number*1
PS9402	PS9402-AX	Pb-Free (Ni/Pd/Au)	10 pcs (Tape 10 pcs cut)	Standard products (UL and CSA Approved)	PS9402
<R> PS9402-E3	PS9402-E3-AX		Embossed Tape 850 pcs/reel		
PS9402-V	PS9402-V-AX		10 pcs (Tape 10 pcs cut)	DIN EN60747-5-2 (VDE0884 Part2) Approved (Option)	
<R> PS9402-V-E3	PS9402-V-E3-AX		Embossed Tape 850 pcs/reel		

Note: *1. For the application of the Safety Standard, following part number should be used.

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Ratings	Unit
<R> Forward Current *1	I_F	25	mA
Peak Transient Forward Current (Pulse Width < 1 μs)	$I_{F\ (TRAN)}$	1.0	A
Reverse Voltage	V_R	5	V
Input Supply Voltage	$V_{CC}1$	0 to 5.5	V
Input IC Power Dissipation *2	P_I	80	mW
High Level Peak Output Current *3	$I_{OH\ (PEAK)}$	2.5	A
Low Level Peak Output Current *3	$I_{OL\ (PEAK)}$	2.5	A
FAULT Output Current	I_{FAULT}	8	mA
FAULT Pin Voltage	V_{FAULT}	0 to $V_{CC}1$	V
Total Output Supply Voltage	($V_{CC}2 - V_{EE}$)	0 to 33	V
Negative Output Supply Voltage	($V_E - V_{EE}$)	0 to 15	V
Output Voltage	V_O	0 to $V_{CC}2$	V
Peak Clamping Sinking Current	I_{Clamp}	1.7	A
Miller Clamping Pin Voltage	V_{Clamp}	0 to $V_{CC}2$	V
DESAT Voltage	V_{DESAT}	V_E to V_E + 10	V
Output IC Power Dissipation *4	P_O	300	mW
Isolation Voltage *5	BV	5 000	Vr.m.s.
Operating Ambient Temperature	T_A	−40 to +110	°C
Storage Temperature	T_{stg}	−55 to +125	°C

<R> Notes: *1. Reduced to 0.52 mA/°C at T_A = 85°C or more.

*2. Reduced to 1.6 mW/°C at T_A = 75°C or more.

<R> *3. Maximum pulse width = 10 μs, Maximum duty cycle = 0.2%

*4. Reduced to 5.5 mW/°C at T_A = 70°C or more.

*5. AC voltage for 1 minute at T_A = 25°C, RH = 60% between input and output. Pins 1-8 shorted together, 9-16 shorted together.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	MIN.	MAX.	Unit
Total Output Supply Voltage	($V_{CC}2 - V_{EE}$)	15	30	V
Negative Output Supply Voltage	($V_E - V_{EE}$)	0	15	V
Positive Output Supply Voltage	($V_{CC}2 - V_E$)	15	30 − ($V_E - V_{EE}$)	V
Forward Current (ON)	$I_{F\ (ON)}$	8	12	mA
Forward Voltage (OFF)	$V_{F\ (OFF)}$	−2	0.8	V
Operating Ambient Temperature	T_A	−40	110	°C

<R> **ELECTRICAL CHARACTERISTICS (DC) (at RECOMMENDED OPERATING CONDITIONS, V_{EE} = V_E = GND, unless otherwise specified)**

Parameter	Symbol	Conditions	MIN.	TYP. *1	MAX.	Unit
FAULT Logic Low Output Voltage	V_{FAULTL}	I_{FAULT} = 1.1 mA, $V_{CC}1$ = 5.5 V		0.1		V
FAULT Logic High Output Current	I_{FAULTH}	V_{FAULT} = 5.5 V, $V_{CC}1$ = 5.5 V, T_A = 25°C			0.5	μA
High Level Output Current	I_{OH}	V_O = ($V_{CC}2$ – 4 V) *2	–0.5	–1.5		A
		V_O = ($V_{CC}2$ – 15 V) *3	–2.0			
Low Level Output Current	I_{OL}	V_O = (V_{EE} + 2.5 V) *2	0.5	1.5		A
		V_O = (V_{EE} + 15 V) *3	2.0			
Low Level Output Current During Fault Condition	I_{OLF}	V_O – V_{EE} = 14 V	90	140	230	mA
High Level Output Voltage	V_{OH}	I_O = 100 mA *4	$V_{CC}2$ – 3.0	$V_{CC}2$ – 1.3		V
		I_O = –650 μA *4	$V_{CC}2$ – 2.5	$V_{CC}2$ – 0.8		
Low Level Output Voltage	V_{OL}	I_O = 100 mA		0.15	0.5	V
Clamp Pin Threshold Voltage	V_{tClamp}			2.0		V
Clamp Low Level Sinking Current	I_{CL}	V_{tClamp} = V_{EE} + 2.5 V	0.35	1.5		A
High Level Supply Current	$I_{CC}2_H$	I_O = 0 mA		2	3	mA
Low Level Supply Current	$I_{CC}2_L$	I_O = 0 mA		2	3	mA
Blanking Capacitor Charging Current	I_{CHG}	V_{DESAT} = 2 V	–0.13	–0.24	–0.33	mA
Blanking Capacitor Discharging Current	I_{DSCHG}	V_{DESAT} = 7 V	10	30		mA
DESAT Threshold	$V_{DESATth}$	$V_{CC}2$ – V_E > V_{UVLO-}, V_O < 5 V	6.0	6.9	7.5	V
UVLO Threshold	V_{UVLO+}	V_O > 5 V	11.0	12.6	13.5	V
	V_{UVLO-}	V_O < 5 V	9.8	11.3	12.3	
UVLO Hysteresis	$UVLO_{HYS}$	(V_{UVLO+}) – (V_{UVLO-})	0.4	1.3		V
Threshold Input Current (L → H)	I_{FLH}	I_O = 0 mA, V_O > 5 V		1.5	5	mA
Threshold Input Voltage (H → L)	V_{FHL}	I_O = 0 mA, V_O < 5 V	0.8			V
Input Forward Voltage	V_F	I_F = 10 mA, T_A = 25°C	1.2	1.56	1.8	V
Input Reverse Current	I_R	V_R = 3 V, T_A = 25°C			10	μA
Input Capacitance	C_{IN}	f = 1 MHz, V_F = 0 V		30		pF

Notes: *1. Typical values at T_A = 25°C.

*2. Maximum pulse width = 50 μs, Maximum duty cycle = 0.5%

*3. Maximum pulse width = 10 μs, Maximum duty cycle = 0.2%

*4. V_{OH} is measured with the DC load current in this testing (Maximum pulse width = 1 ms, Maximum duty cycle = 20%).

<R> **SWITCHING CHARACTERISTICS (AC) (at RECOMMENDED OPERATING CONDITIONS, V_{EE} = V_E = GND, unless otherwise specified)**

Parameter	Symbol	Conditions	MIN.	TYP. *1	MAX.	Unit
Propagation Delay Time (L → H)	t_{PLH}	R_g = 10 Ω, C_g = 10 nF,	50	90	200	ns
Propagation Delay Time (H → L)	t_{PHL}	f = 10 kHz,	50	110	200	ns
Pulse Width Distortion (PWD)	$\|t_{PHL}-t_{PLH}\|$	Duty Cycle = 50% *2,		20	100	ns
Propagation Delay Time (Difference Between Any Two Products)	$t_{PHL}-t_{PLH}$	I_F = 10 mA, $V_{CC}2$ = 30 V	−100		100	ns
Rise Time	t_r			50		ns
Fall Time	t_f			50		ns
Common Mode Transient Immunity at High Level Output *3	CM_H	T_A = 25°C, I_F = 10 mA, $V_{CC}2$ = 30 V, V_{CM} = 1.5 kV, C_{DESAT} = 100 pF, R_F = 2.1 kΩ, $V_{CC}1$ = 5 V	25			kV/μs
Common Mode Transient Immunity at Low Level Output *4	CM_L	T_A = 25°C, V_F = 0 V, $V_{CC}2$ = 30 V, V_{CM} = 1.5 kV, R_F = 2.1 kΩ, $V_{CC}1$ = 5 V			−25	kV/μs
DESAT Sense to 90% V_O Delay	t_{DESAT} (90%)	C_{DESAT} = 100 pF, R_F = 2.1 kΩ,		250	500	ns
DESAT Sense to 10% V_O Delay	t_{DESAT} (10%)	R_g = 10 Ω, C_g = 10 nF $V_{CC}2$ = 30 V	1.5	2	3	μs
DESAT Sense to Low Level FAULT Signal Delay	t_{DESAT} (FAULT)			400	800	ns
DESAT Sense to DESAT Low Propagation Delay	t_{DESAT} (LOW)			250		ns
DESAT Input Mute *5	t_{DESAT} (MUTE)		5			μs
RESET to High Level FAULT Signal Delay	t_{RESET} (FAULT)	$V_{CC}1$ = 5.5 V	0.3	1.2	3.0	μs
		$V_{CC}1$ = 3.3 V	0.5	1.5	4.0	μs

Notes: *1. Typical values at T_A = 25°C.

*2. This load condition is equivalent to the IGBT load at 1 200 V/150 A.

*3. Common mode transient immunity in the high state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in the high state (i.e., V_O > 15 V or FAULT > 2 V). A 100 pF and a 2.1 kΩ pull-up resistor is needed in fault detection mode.

*4. Common mode transient immunity in the low state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in a low state (i.e., V_O < 1.0 V or FAULT < 0.8 V).

*5. During muting DESAT, even if LED (IF) input occurs, IGBT operates turn-off and Vo state is kept to low. After unmuting this DESAT, when LED is turned on, Vo/FAULT becomes high state (with automatic reset).

<R> TEST CIRCUIT 1

Fig. 1 V_{FAULTL} Test Circuit

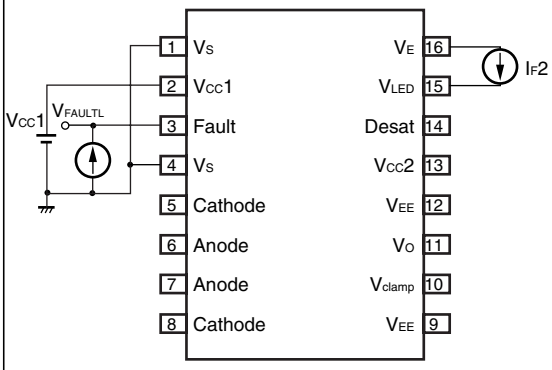


Fig. 2 I_{FAULTH} Test Circuit

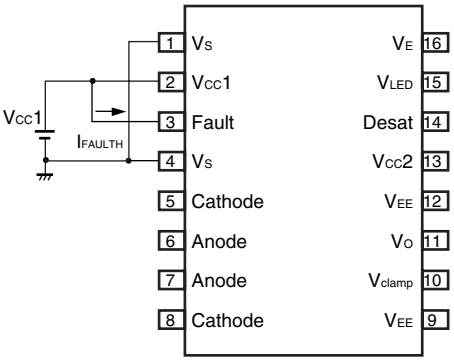


Fig. 3 I_{OH} Test Circuit

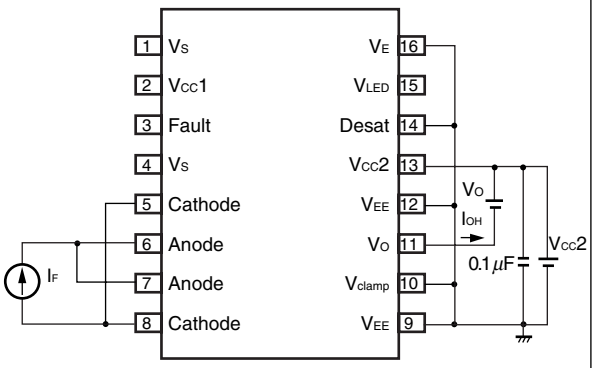


Fig. 4 I_{OL} Test Circuit

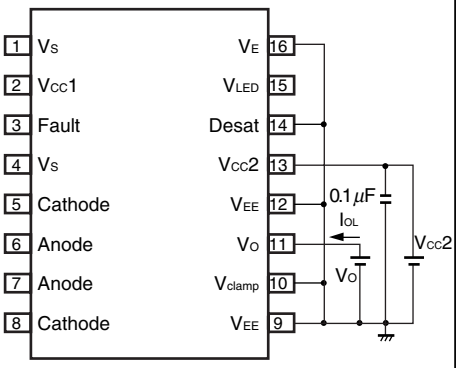


Fig. 5 V_{OH} Test Circuit

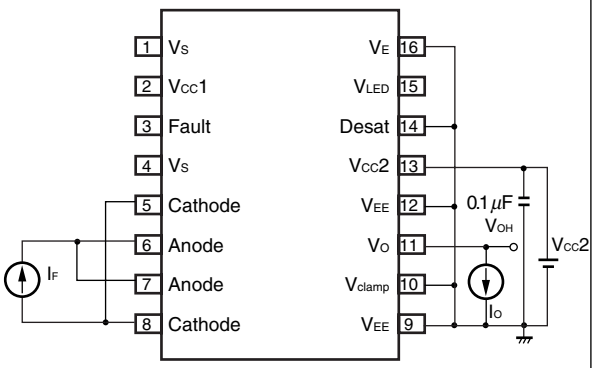
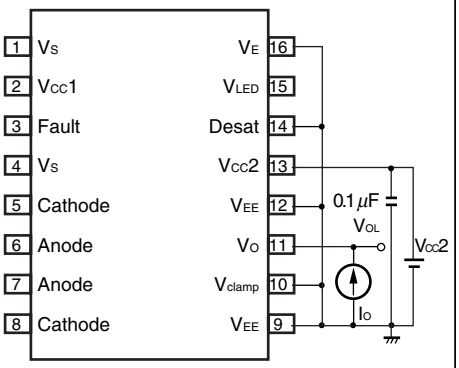


Fig. 6 V_{OL} Test Circuit



<R> TEST CIRCUIT 2

Fig. 7 I_{CC2H} Test Circuit

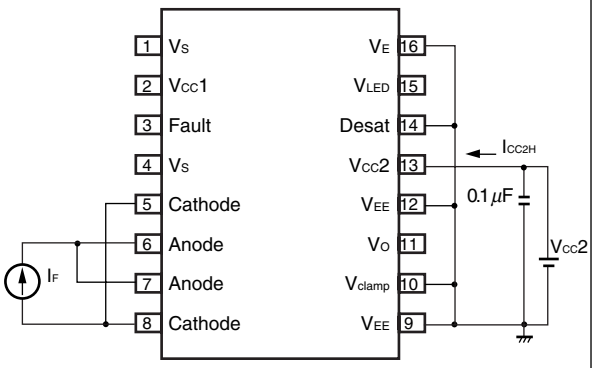


Fig. 8 I_{CC2L} Test Circuit

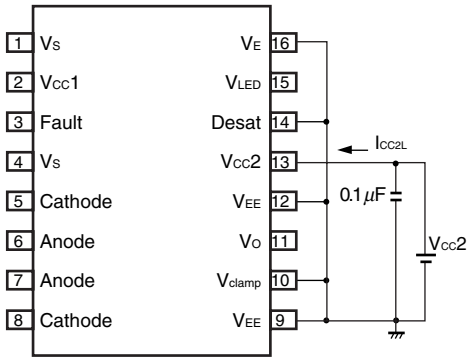


Fig. 9 I_{CHG} Test Circuit

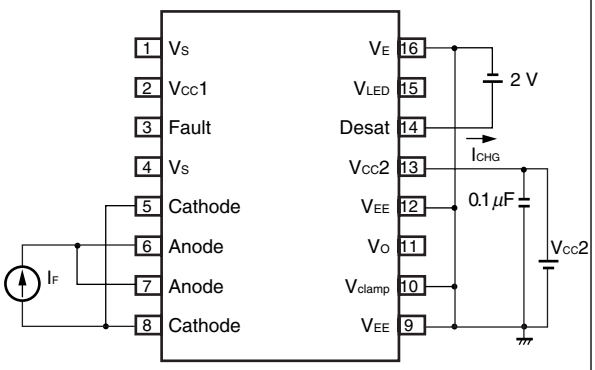


Fig. 10 I_{DSCHG} Test Circuit

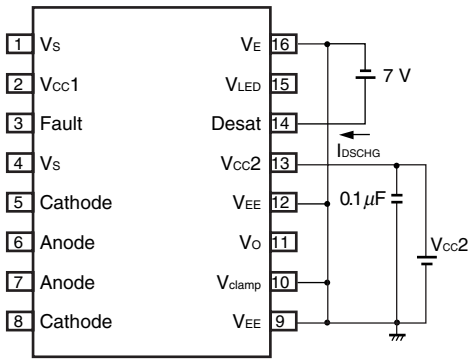


Fig. 11 I_{CL} Test Circuit

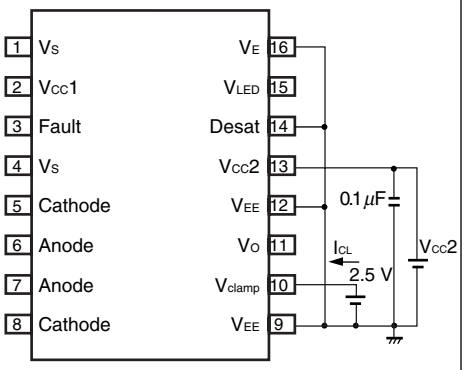
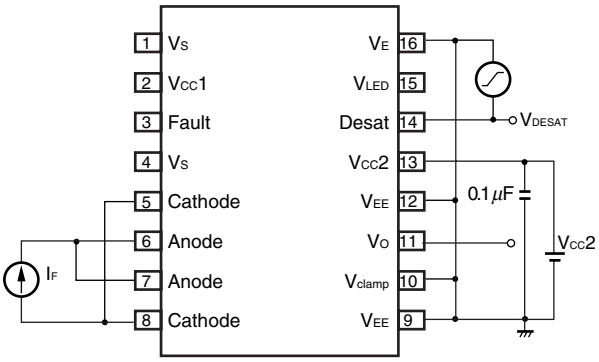


Fig. 12 V_{DESAT} Test Circuit



<R> TEST CIRCUIT 3

Fig. 13 V_{UVLO} Test Circuit

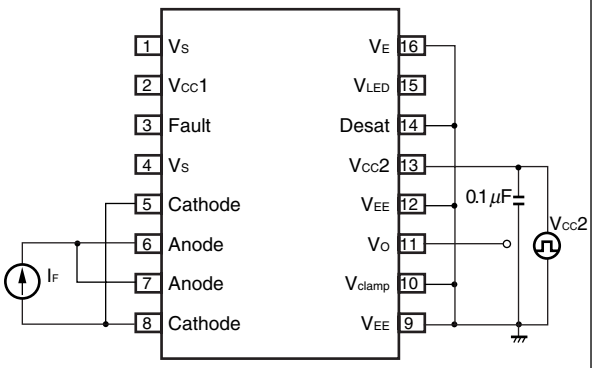


Fig. 14 I_{FLH} Test Circuit

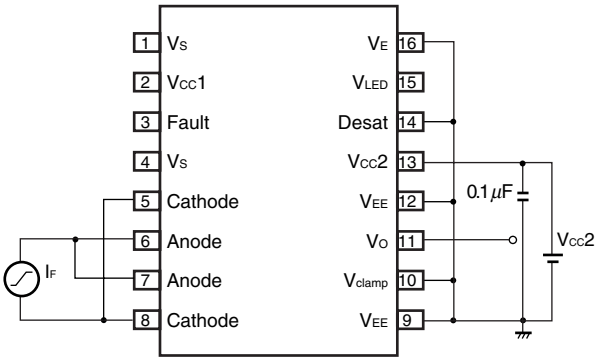


Fig. 15 t_{PLH}/t_{PHL} Test Circuit

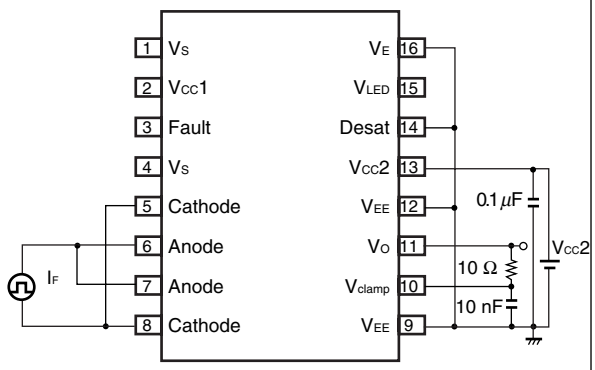


Fig. 17 t_{PLH}/t_{PHL} Test Wave Forms

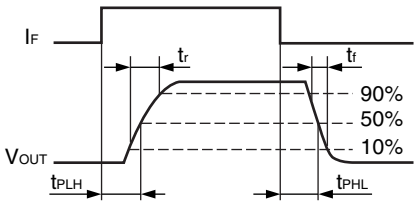


Fig. 17 t_{DESAT} Test Circuit

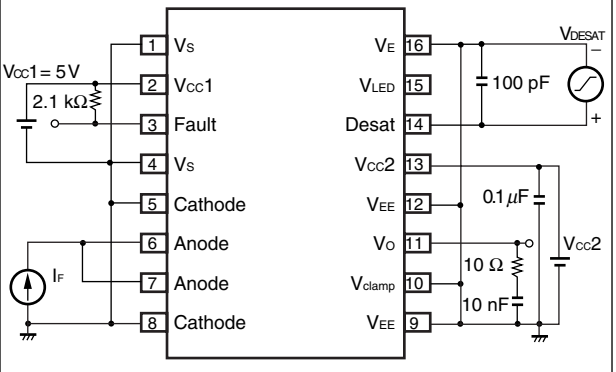
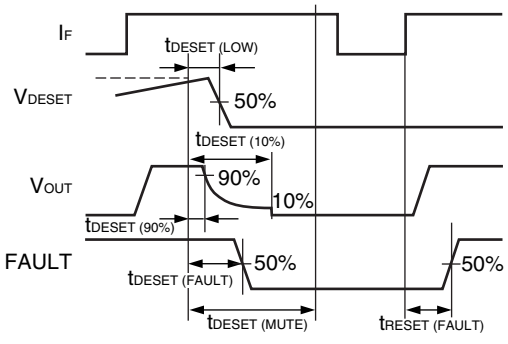


Fig. 18 t_{DESAT} Test Wave Forms



<R> TEST CIRCUIT 4

Fig. 19 CM_H Test Circuit (LED1 ON)

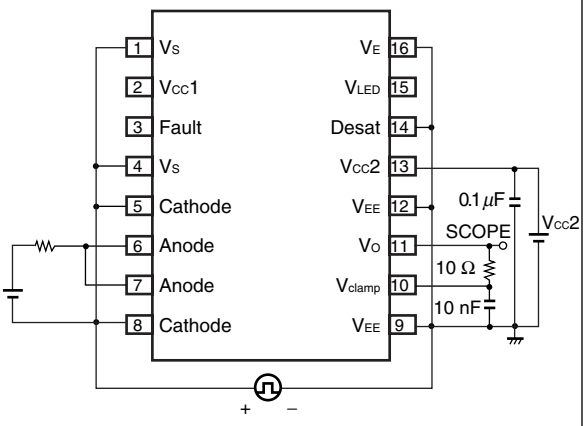


Fig. 20 CM_L Test Circuit (LED1 OFF)

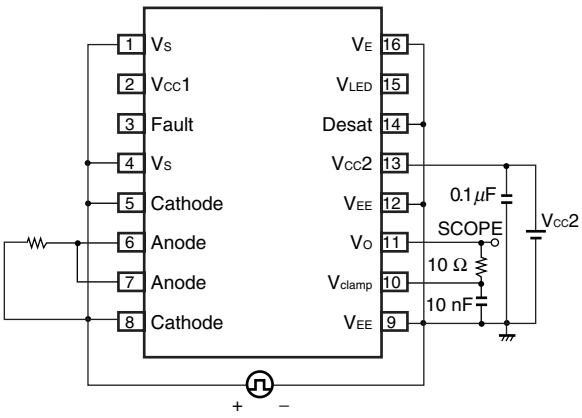


Fig. 21 CM_H Test Circuit (LED2 ON)

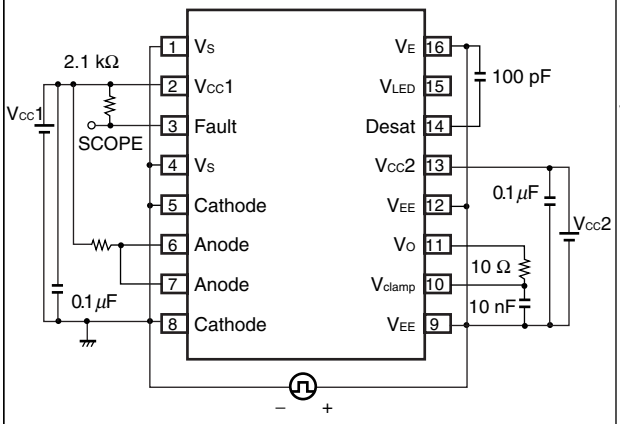


Fig. 22 CM_L Test Circuit (LED2 OFF)

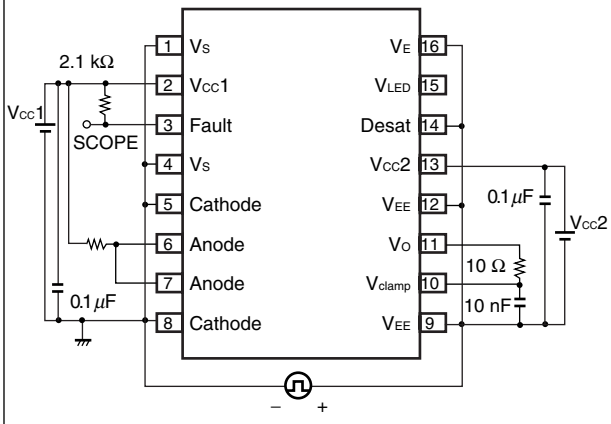


Fig. 23 CM_H, CM_L Test Wave Forms (LED1 ON, OFF)

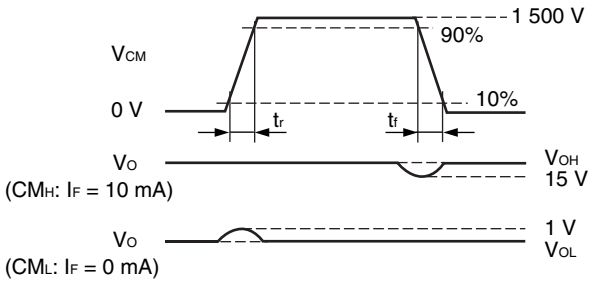
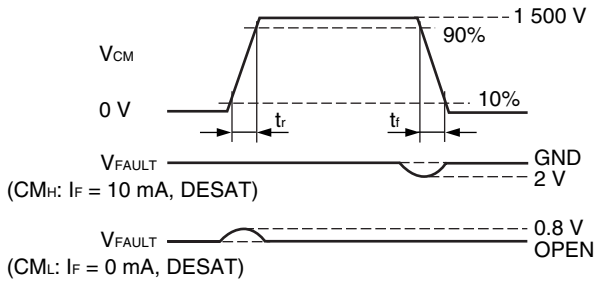
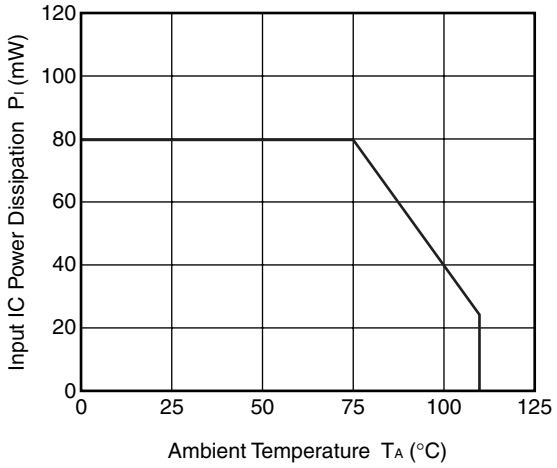


Fig. 24 CM_H, CM_L Test Wave Forms (LED2 ON, OFF)

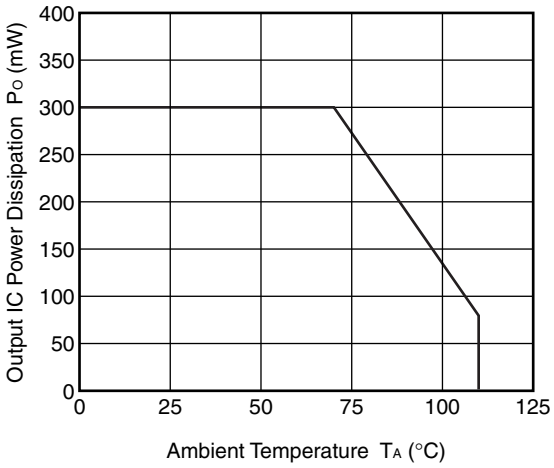


<R> TYPICAL CHARACTERISTICS (T_A = 25°C, unless otherwise specified)

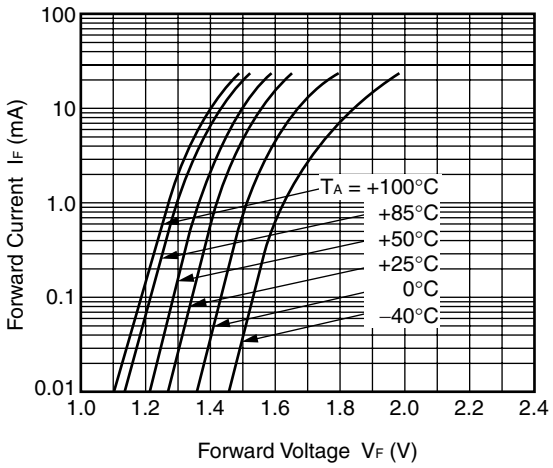
INPUT IC POWER DISSIPATION vs. AMBIENT TEMPERATURE



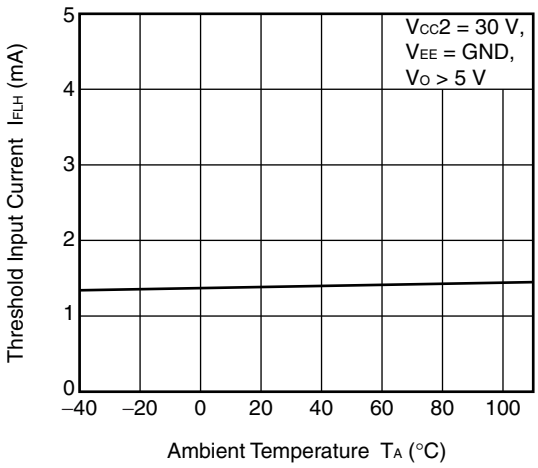
OUTPUT IC POWER DISSIPATION vs. AMBIENT TEMPERATURE



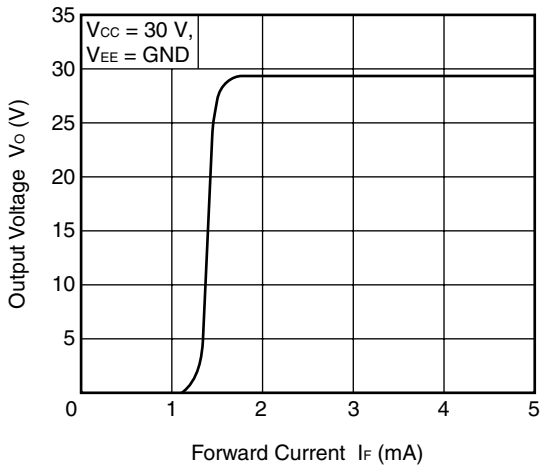
FORWARD CURRENT vs. FORWARD VOLTAGE



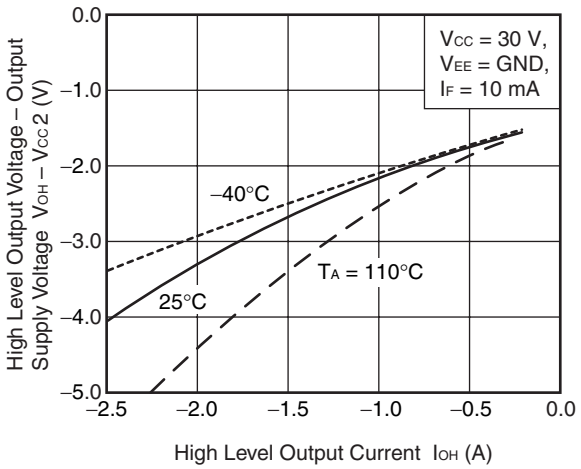
THRESHOLD INPUT CURRENT vs. AMBIENT TEMPERATURE



OUTPUT VOLTAGE vs. FORWARD CURRENT

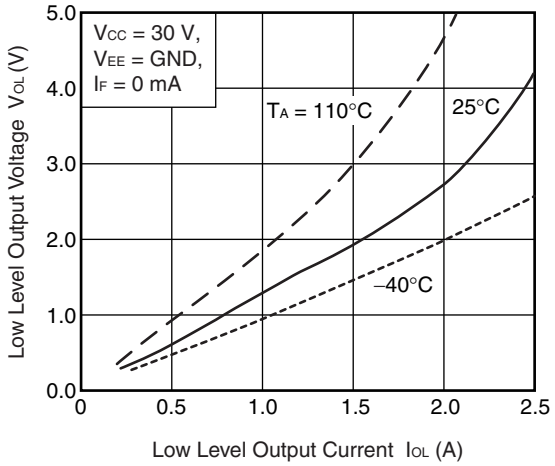


HIGH LEVEL OUTPUT VOLTAGE – OUTPUT SUPPLY VOLTAGE vs. HIGH LEVEL OUTPUT CURRENT

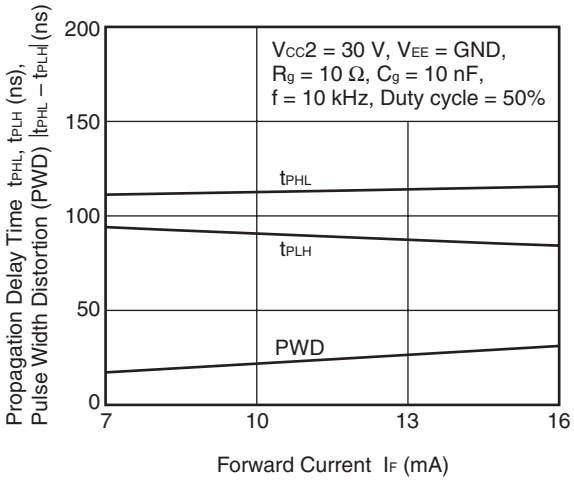


Remark The graphs indicate nominal characteristics.

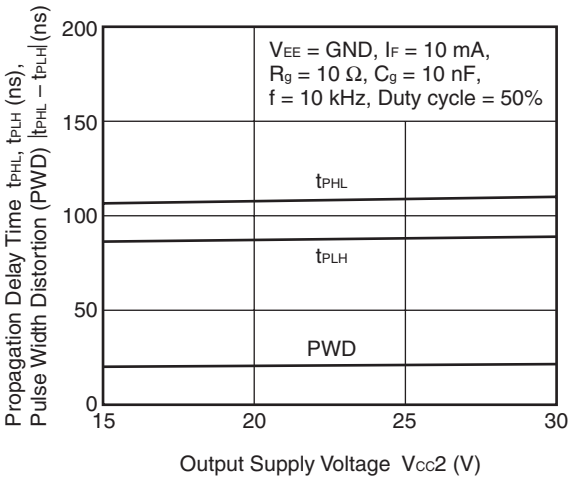
LOW LEVEL OUTPUT VOLTAGE vs.
LOW LEVEL OUTPUT CURRENT



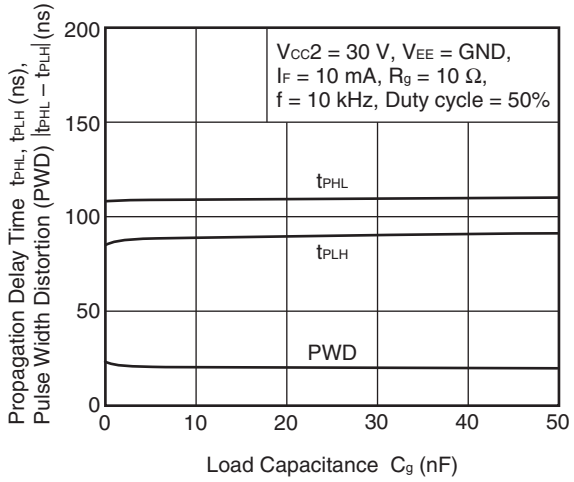
PROPAGATION DELAY TIME,
PULSE WIDTH DISTORTION
vs. FORWARD CURRENT



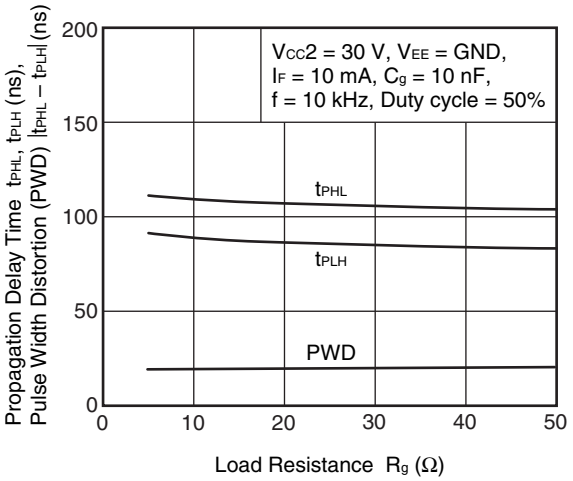
PROPAGATION DELAY TIME,
PULSE WIDTH DISTORTION
vs. OUTPUT SUPPLY VOLTAGE



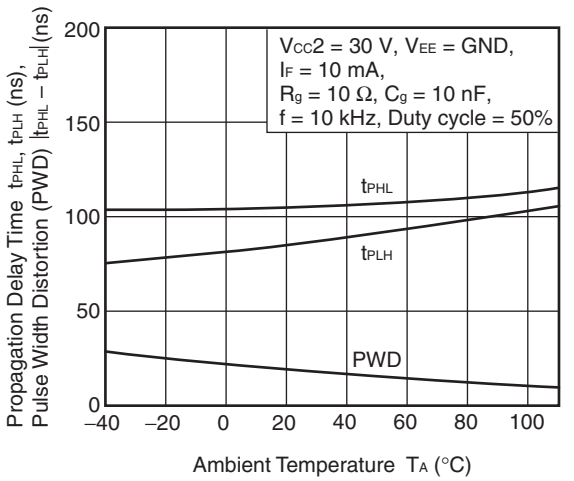
PROPAGATION DELAY TIME,
PULSE WIDTH DISTORTION
vs. LOAD CAPACITANCE



PROPAGATION DELAY TIME,
PULSE WIDTH DISTORTION
vs. LOAD RESISTANCE

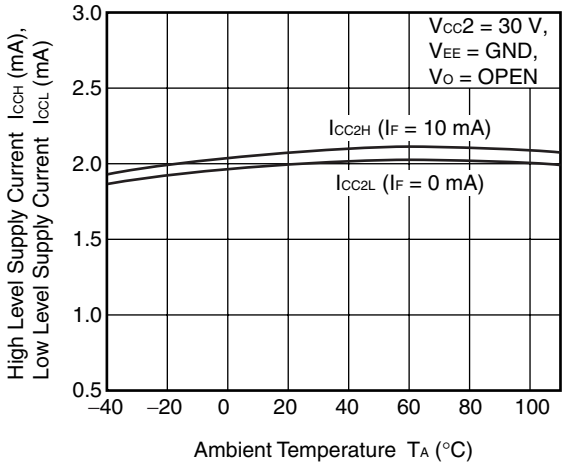


PROPAGATION DELAY TIME,
PULSE WIDTH DISTORTION
vs. AMBIENT TEMPERATURE

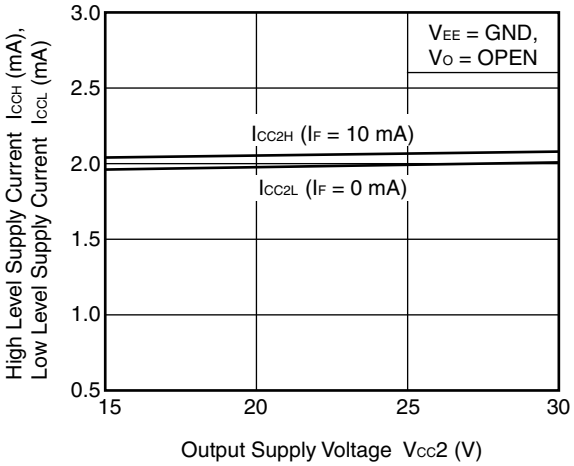


Remark The graphs indicate nominal characteristics.

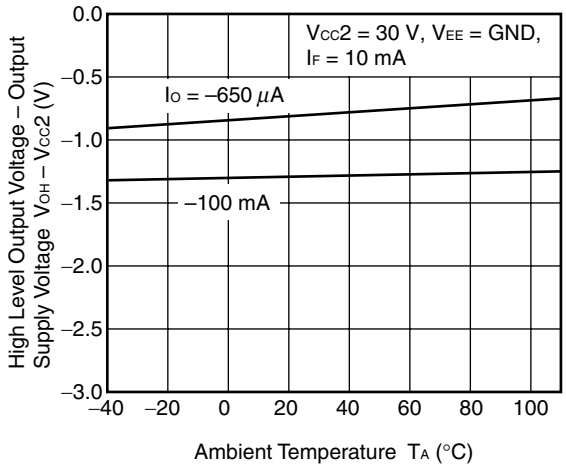
HIGH LEVEL SUPPLY CURRENT, LOW LEVEL SUPPLY CURRENT vs. AMBIENT TEMPERATURE



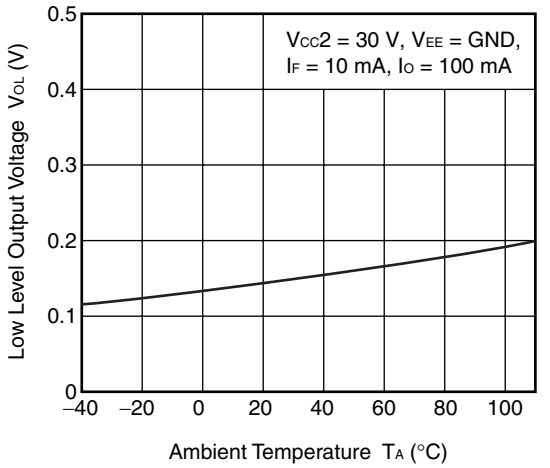
HIGH LEVEL SUPPLY CURRENT, LOW LEVEL SUPPLY CURRENT vs. OUTPUT SUPPLY VOLTAGE



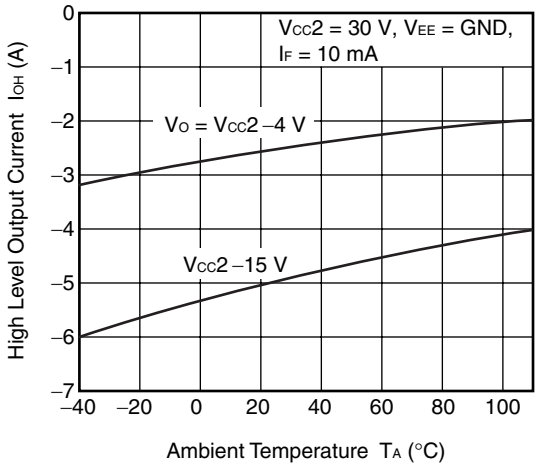
HIGH LEVEL OUTPUT VOLTAGE – OUTPUT SUPPLY VOLTAGE vs. AMBIENT TEMPERATURE



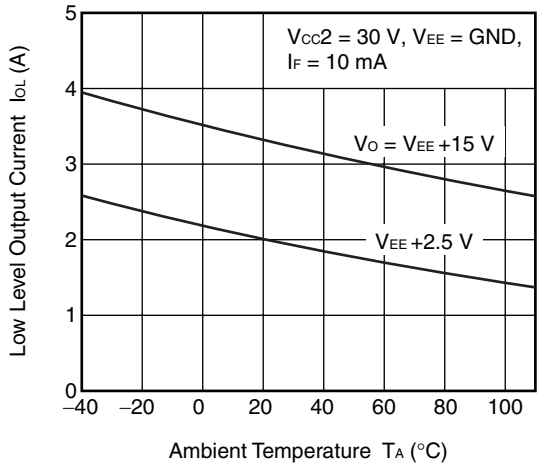
LOW LEVEL OUTPUT VOLTAGE vs. AMBIENT TEMPERATURE



HIGH LEVEL OUTPUT CURRENT vs. AMBIENT TEMPERATURE

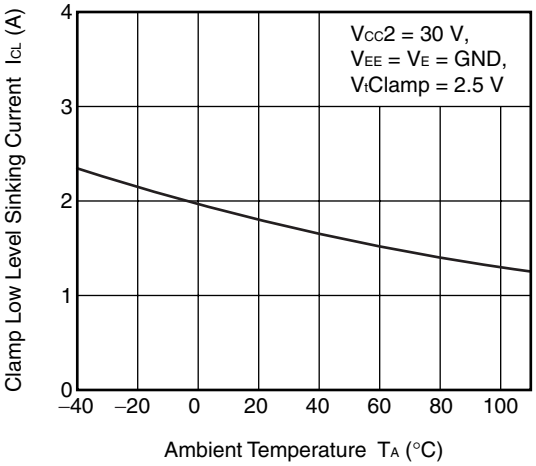


LOW LEVEL OUTPUT CURRENT vs. AMBIENT TEMPERATURE

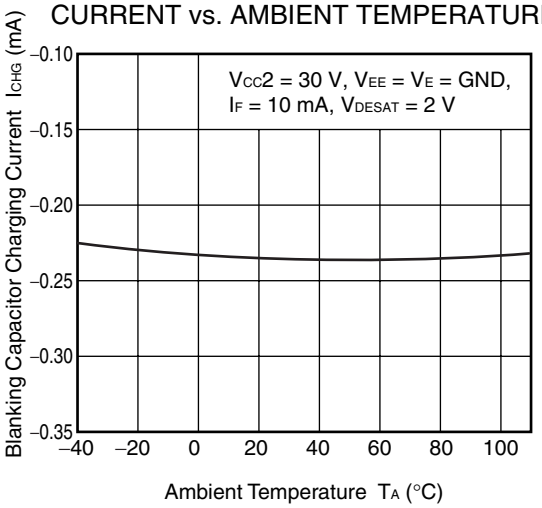


Remark The graphs indicate nominal characteristics.

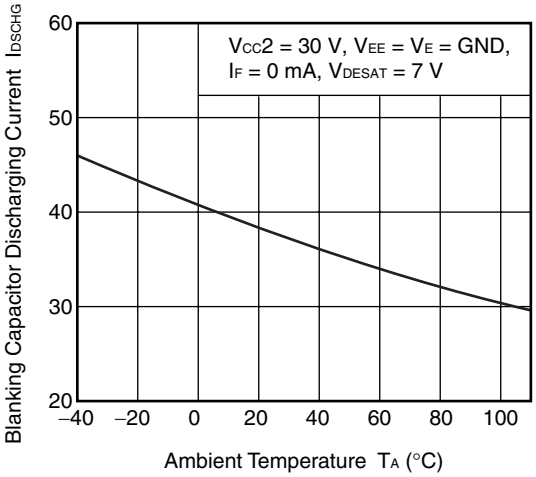
CLAMP LOW LEVEL SINKING CURRENT vs. AMBIENT TEMPERATURE



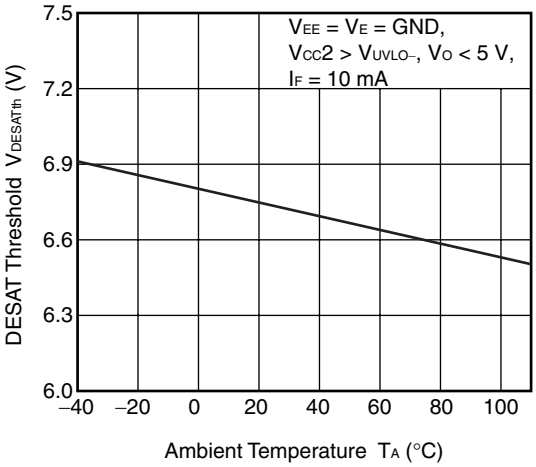
BLANKING CAPACITOR CHARGING CURRENT vs. AMBIENT TEMPERATURE



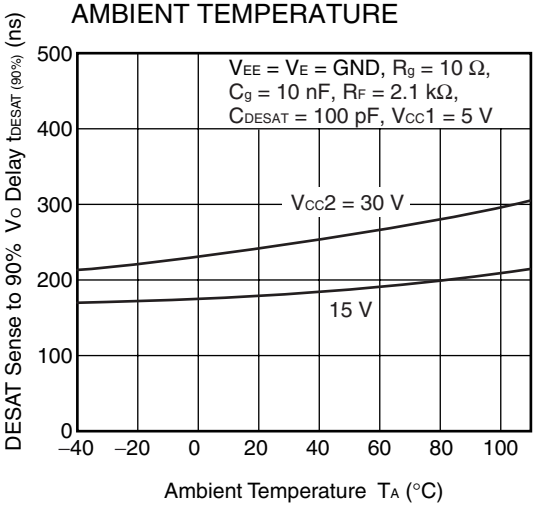
BLANKING CAPACITOR DISCHARGING CURRENT vs. AMBIENT TEMPERATURE



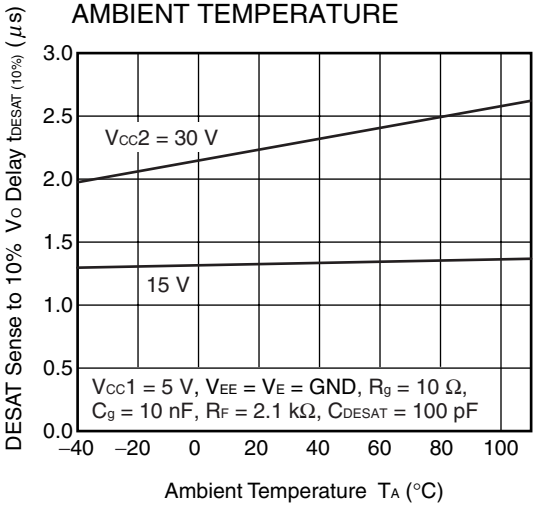
DESAT THRESHOLD vs. AMBIENT TEMPERATURE



DESAT SENSE TO 90% VO DELAY vs. AMBIENT TEMPERATURE

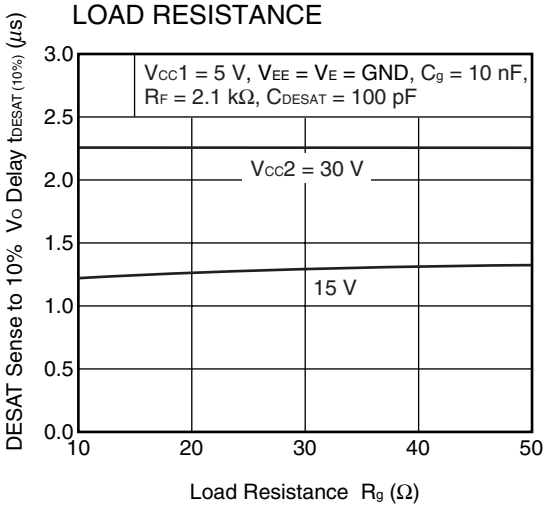


DESAT SENSE TO 10% VO DELAY vs. AMBIENT TEMPERATURE

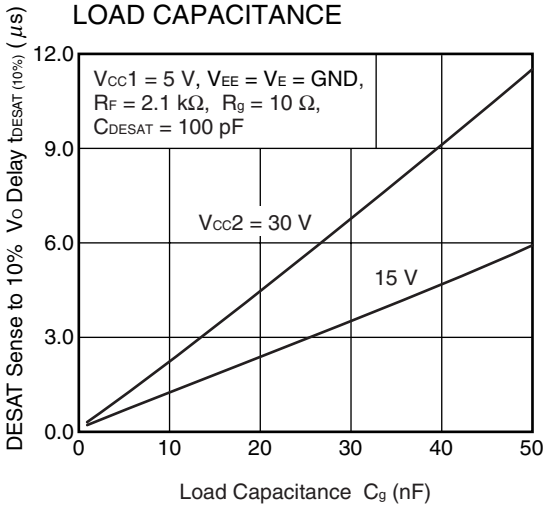


Remark The graphs indicate nominal characteristics.

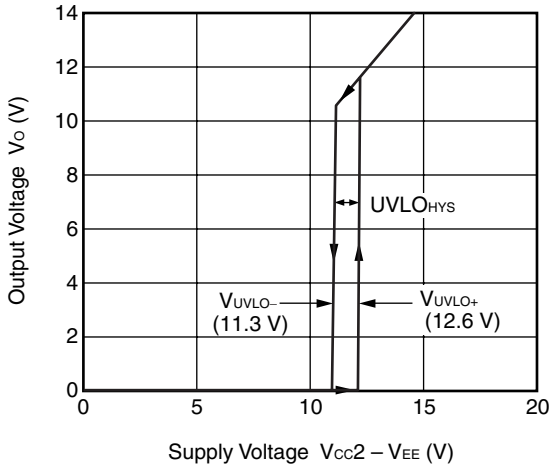
DESAT SENSE TO 10% V_O DELAY vs. LOAD RESISTANCE



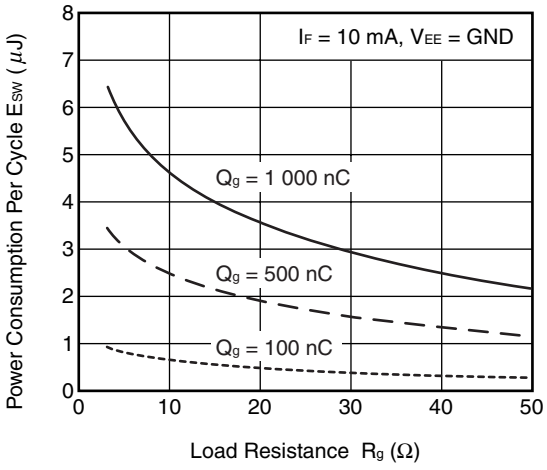
DESAT SENSE TO 10% V_O DELAY vs. LOAD CAPACITANCE



OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



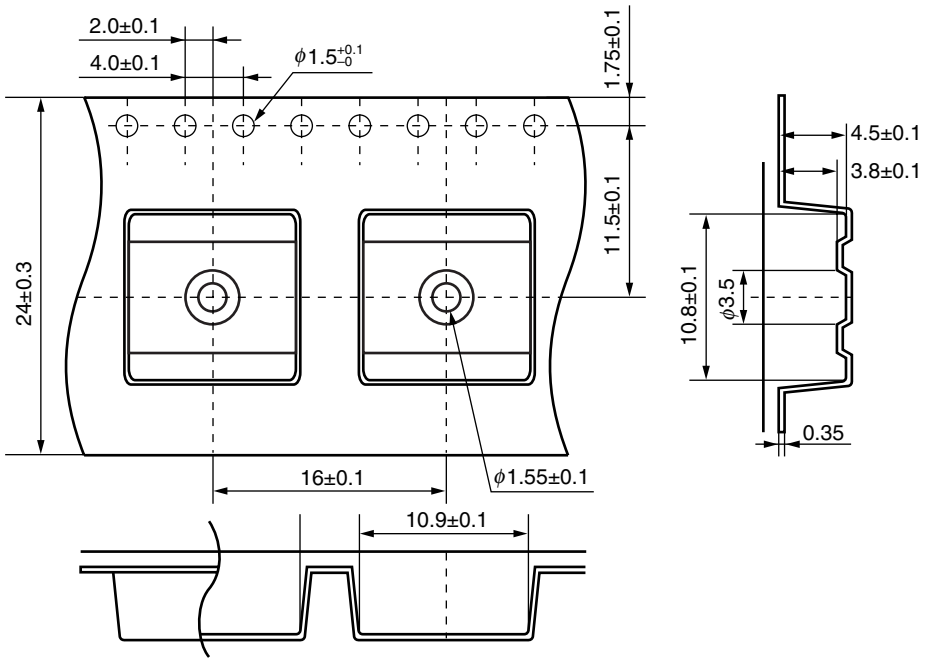
POWER CONSUMPTION PER CYCLE vs. LOAD RESISTANCE



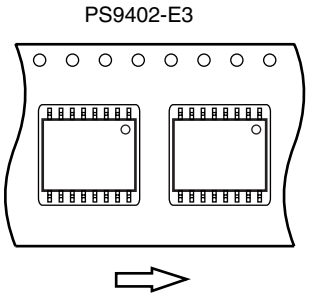
Remark The graphs indicate nominal characteristics.

TAPING SPECIFICATIONS (UNIT: mm)

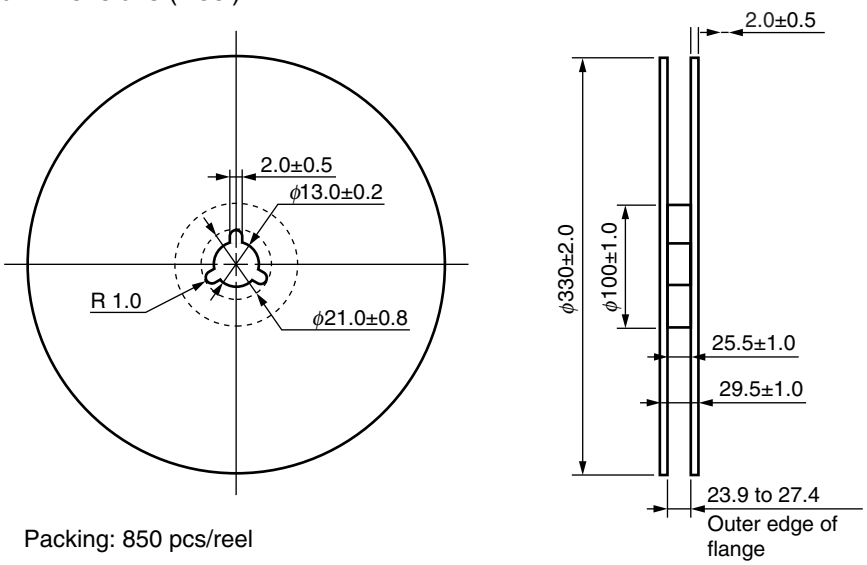
Outline and Dimensions (Tape)



Tape Direction

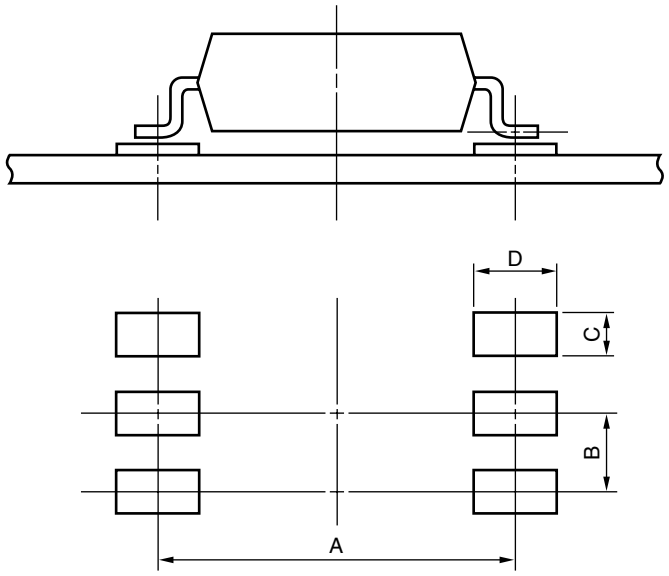


Outline and Dimensions (Reel)



Packing: 850 pcs/reel

<R> RECOMMENDED MOUNT PAD DIMENSIONS (UNIT: mm)



Part Number	Lead Bending	A	B	C	D
PS9402	lead bending type (Gull-wing) for surface mount	9.85	1.27	0.96	1.65

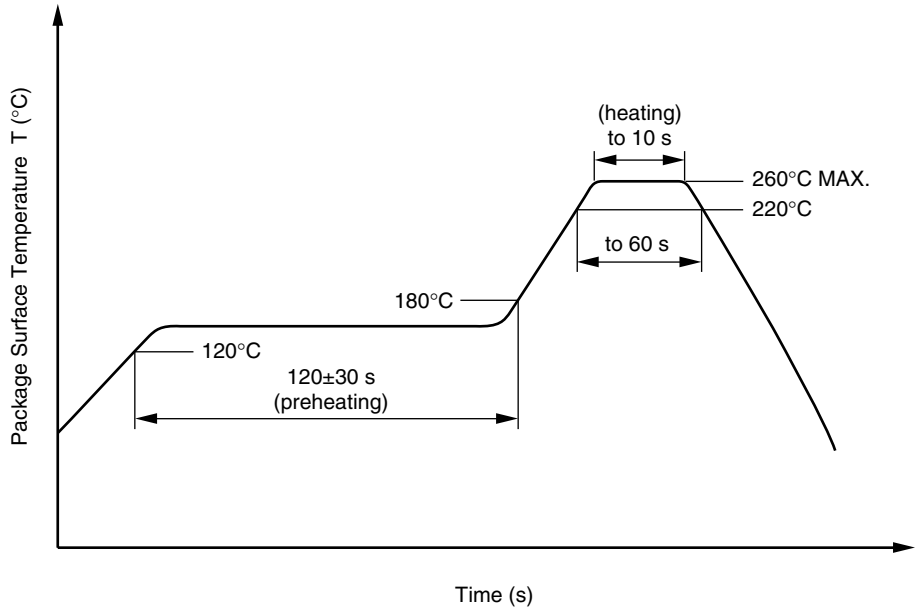
NOTES ON HANDLING

1. Recommended soldering conditions

(1) Infrared reflow soldering

- Peak reflow temperature — 260°C or below (package surface temperature)
- Time of peak reflow temperature — 10 seconds or less
- Time of temperature higher than 220°C — 60 seconds or less
- Time to preheat temperature from 120 to 180°C — 120±30 s
- Number of reflows — Three
- Flux — Rosin flux containing small amount of chlorine (The flux with a maximum chlorine content of 0.2 Wt% is recommended.)

Recommended Temperature Profile of Infrared Reflow



(2) Wave soldering

- Temperature — 260°C or below (molten solder temperature)
- Time — 10 seconds or less
- Preheating conditions — 120°C or below (package surface temperature)
- Number of times — One (Allowed to be dipped in solder including plastic mold portion.)
- Flux — Rosin flux containing small amount of chlorine (The flux with a maximum chlorine content of 0.2 Wt% is recommended.)

(3) Soldering by Soldering Iron

- Peak Temperature (lead part temperature) — 350°C or below
- Time (each pins) — 3 seconds or less
- Flux — Rosin flux containing small amount of chlorine (The flux with a maximum chlorine content of 0.2 Wt% is recommended.)

(a) Soldering of leads should be made at the point 1.5 to 2.0 mm from the root of the lead

(4) Cautions

- Fluxes — Avoid removing the residual flux with freon-based and chlorine-based cleaning solvent.

2. Cautions regarding noise

Be aware that when voltage is applied suddenly between the photocoupler's input and output at startup, the output transistor may enter the on state, even if the voltage is within the absolute maximum ratings.

USAGE CAUTIONS

1. This product is weak for static electricity by designed with high-speed integrated circuit so protect against static electricity when handling.
2. Board designing
   (1) By-pass capacitor of more than 0.1 μF is used between V_{CC} and GND near device. Also, ensure that the distance between the leads of the photocoupler and capacitor is no more than 10 mm.
<R> (2) When designing the printed wiring board, ensure that the pattern of the IGBT collectors/emitters is not too close to the input block pattern of the photocoupler.
   If the pattern is too close to the input block and coupling occurs, a sudden fluctuation in the voltage on the IGBT output side might affect the photocoupler's LED input, leading to malfunction or degradation of characteristics. (If the pattern needs to be close to the input block, to prevent the LED from lighting during the off state due to the abovementioned coupling, design the input-side circuit so that the bias of the LED is reversed, within the range of the recommended operating conditions, and be sure to thoroughly evaluate operation.)
3. Make sure the rise/fall time of the forward current is 0.5 μs or less.
<R> 4. In order to avoid malfunctions, make sure the rise/fall slope of the $V_{CC}2$ is 3 V/μs or less.
5. Avoid storage at a high temperature and high humidity.

<R> SPECIFICATION OF VDE MARKS LICENSE DOCUMENT

Parameter	Symbol	Spec.	Unit
Climatic test class (IEC 60068-1/DIN EN 60068-1)		40/110/21	
Dielectric strength maximum operating isolation voltage Test voltage (partial discharge test, procedure a for type test and random test) U_{pr} = 1.6 × $U_{IORM.}$, P_d < 5 pC	 U_{IORM} U_{pr}	 1 130 1 808	 V_{peak} V_{peak}
Test voltage (partial discharge test, procedure b for all devices) U_{pr} = 1.875 × $U_{IORM.}$, P_d < 5 pC	U_{pr}	2 119	V_{peak}
Highest permissible overvoltage	U_{TR}	8 000	V_{peak}
Degree of pollution (DIN EN 60664-1 VDE0110 Part 1)		2	
Comparative tracking index (IEC 60112/DIN EN 60112 (VDE 0303 Part 11))	CTI	175	
Material group (DIN EN 60664-1 VDE0110 Part 1)		III a	
Storage temperature range	T_{stg}	–55 to +125	°C
Operating temperature range	T_A	–40 to +110	°C
Isolation resistance, minimum value V_{IO} = 500 V dc at T_A = 25°C V_{IO} = 500 V dc at T_A MAX. at least 100°C	 Ris MIN. Ris MIN.	 10^{12} 10^{11}	 Ω Ω
Safety maximum ratings (maximum permissible in case of fault, see thermal derating curve) Package temperature Current (input current I_F, Psi = 0) Power (output or total power dissipation) Isolation resistance V_{IO} = 500 V dc at T_A = Tsi	 Tsi Isi Psi Ris MIN.	 175 400 700 10^9	 °C mA mW Ω

Caution GaAs Products	This product uses gallium arsenide (GaAs). GaAs vapor and powder are hazardous to human health if inhaled or ingested, so please observe the following points. • Follow related laws and ordinances when disposing of the product. If there are no applicable laws and/or ordinances, dispose of the product as recommended below. 1. Commission a disposal company able to (with a license to) collect, transport and dispose of materials that contain arsenic and other such industrial waste materials. 2. Exclude the product from general industrial waste and household garbage, and ensure that the product is controlled (as industrial waste subject to special control) up until final disposal. • Do not burn, destroy, cut, crush, or chemically dissolve the product. • Do not lick the product or in any way allow it to enter the mouth.

Revision History	PS9402 Data Sheet

Rev.	Date	Description	
		Page	Summary
0.01	May 09, 2011	–	First edition issued
1.00	Jun 22, 2012	Throughout	Preliminary Data Sheet - > Data Sheet
		Throughout	Safety standards approved
		p.3	Modification of **BLOCK DIAGRAM**
		p.4	Modification of **MARKING EXAMPLE**
		p.5	Modification of **ABSOLUTE MAXIMUM RATINGS**
		p.6	Modification of **ELECTRICAL CHARACTERISTICS (DC)**
		p.7	Modification of **SWITCHING CHARACTERISTICS (AC)**
		pp.8 to 11	Modification of **TEST CIRCUIT**
		pp.12 to 16	Addition of **TYPICAL CHARACTERISTICS**
		p.18	Addition of **RECOMMENDED MOUNT PAD DIMENSIONS**
		p.20	Modification of **USAGE CAUTIONS**
		p.21	Addition of **SPECIFICATION OF VDE MARKS LICENSE DOCUMENT**

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