ISL8323, ISL8324, ISL8325

Low-Voltage, Single Supply, Dual SPST Analog Switches

FN6023
Rev 2.00
October 7, 2015

The Intersil ISL8323–ISL8325 devices are precision, dual analog switches designed to operate from a single +2.7V to +12V supply. Targeted applications include battery powered equipment that benefit from the devices' low power consumption (5µW), low leakage currents (100pA max), and fast switching speeds. Excellent R_{ON} matching and flatness maintain signal fidelity over the whole input range.

The ISL8323/ISL8324/ISL8325 are dual single-pole/single-throw (SPST) devices. The ISL8323 has two normally open (NO) switches; the ISL8324 has two normally closed (NC) switches; the ISL8325 has one NO and one NC switch and can be used as an SPDT. Table 1 summarizes the performance of this family. For higher performance, pin compatible versions, or SOT-23 packaged devices, see the ISL5120-23 data sheet.

TABLE 1. SUMMARY OF FEATURES

	ISL8323	ISL8324 No Longer Available or Supported	ISL8325 No Longer Available or Supported
Number of Switches	2	2	2
SW 1 / SW 2	NO / NO	NC / NC	NO / NC
3.3V R_{ON} (Max)	175Ω	175Ω	175Ω
3.3V t_{ON} / t_{OFF} (Max)	400 / 125ns	400 / 125ns	400 / 125ns
5V R_{ON} (Max)	60Ω	60Ω	60Ω
5V t_{ON} / t_{OFF} (Max)	150 / 100ns	150 / 100ns	150 / 100ns
Packages	8 Ld SOIC		

Related Literature

- Technical Brief TB363 *Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)*

Features

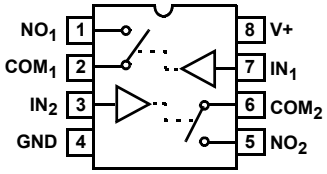
- Drop-in Replacements for MAX323 - MAX325 in Single Supply Applications up to 12V.
- ON Resistance (R_{ON}) . . . . . 60Ω (Max)
- R_{ON} Matching Between Channels. . . . . 2Ω (Max)
- Low Charge Injection . . . . . 5pC (Max)
- Single Supply Operation. . . . . +2.7V to +12V
- Low Power Consumption (P_D) . . . . . <5µW
- Low Leakage Current (Max at 85°C) 5nA
- Fast Switching Action
  - t_{ON} . . . . . 150ns (Max)
  - t_{OFF} . . . . . 100ns (Max)
- Guaranteed Break-Before-Make (ISL8325 only)
- Minimum 2000V ESD Protection per Method 3015.7
- TTL, CMOS Compatible
- Pb-free available

Applications

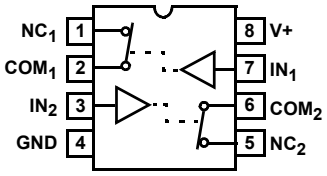
- Battery Powered, Handheld, and Portable Equipment
  - Cellular/Mobile Phones
  - Pagers
  - Laptops, Notebooks, Palmtops
- Communications Systems
  - Military Radios
  - PBX, PABX
- Test Equipment
  - Ultrasound
  - Electrocardiograph
- Heads-Up Displays
- Audio and Video Switching
- Various Circuits
  - +3V/+5V DACs and ADCs
  - Sample and Hold Circuits
  - Digital Filters
  - Operational Amplifier Gain Switching Networks
  - High Frequency Analog Switching
  - High Speed Multiplexing
  - Integrator Reset Circuits

Pinouts (Note 1)

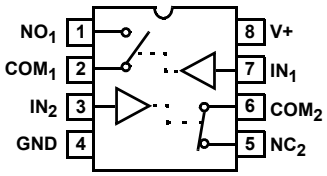
ISL8323 (SOIC)
TOP VIEW



ISL8324 (SOIC)
TOP VIEW



ISL8325 (SOIC)
TOP VIEW



NOTE:

1. Switches Shown for Logic “0” Input.

Truth Table

LOGIC	ISL8323	ISL8324	ISL8325	
	SW 1,2	SW 1,2	SW 1	SW 2
0	OFF	ON	OFF	ON
1	ON	OFF	ON	OFF

NOTE: Logic “0” ≤ 0.8V. Logic “1” ≥ 2.4V.

Pin Descriptions

PIN	FUNCTION
V+	System Power Supply Input (+2.7V to +12V)
GND	Ground Connection
IN	Digital Control Input
COM	Analog Switch Common Pin
NO	Analog Switch Normally Open Pin
NC	Analog Switch Normally Closed Pin

Ordering Information

PART NO. (BRAND) (Notes 2, 3)	TEMP. RANGE (^{O}C)	PACKAGE RoHS Compliant	PKG. DWG. #
ISL8323IBZ	-40 to 85	8 Ld SOIC	M8.15
ISL8324IBZ (No longer available, recommended replacement: ISL8323IBZ)	-40 to 85	8 Ld SOIC	M8.15
ISL8325IBZ (No longer available, recommended replacement: ISL8323IBZ)	-40 to 85	8 Ld SOIC	M8.15

NOTES:

2. Add “-T” suffix to part number for tape and reel packaging.
3. Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which is compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J Std-020B.

Absolute Maximum Ratings

V+ to GND . . . . . -0.3 to15V
Input Voltages
IN, NO, NC, COM (Note 2) . . . . . -0.3 to ((V+) + 0.3V)
Continuous Current (NO, NC, or COM) 30mA
Peak Current NO, NC, or COM
(Pulsed 1ms, 10% Duty Cycle, Max) 100mA
ESD Rating (Per MIL-STD-883 Method 3015). . . . . >2kV

Operating Conditions

Temperature Range
ISL832XIX . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 5) θ_{JA} (°C/W)
8 LD SOIC Package 170
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Moisture Sensitivity (See Technical Brief TB363)
All Packages . . . . . Level 1
Maximum Storage Temperature Range. . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

4. Signals on NC, NO, COM, or IN exceeding V+ or GND are clamped by internal diodes. Limit forward diode current to maximum current ratings.
5. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications - 5V Supply

Test Conditions: V+ = +4.5V to +5.5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Note 6), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (NOTE 7)	TYP	MAX (NOTE 7)	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	V+	V
ON Resistance, R_{ON}	V+ = 4.5V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 3.5V, See Figure 5	25	-	-	60	Ω
		Full	-	-	75	Ω
R_{ON} Matching Between Channels, ΔR_{ON}	V+ = 5V, I_{COM} = 1.0mA, V_{NO} or V_{NC}= 3V	25	-	0.8	2	Ω
		Full	-	-	4	Ω
R_{ON} Flatness, $R_{FLAT(ON)}$	V+ = 5V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 1V, 2V, 3V	Full	-	7	8	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 5.5V, V_{COM} = 1V, 4.5V, V_{NO} or V_{NC} = 4.5V, 1V, Note 8	25	-0.1	-	0.1	nA
		Full	-5	-	5	nA
COM OFF Leakage Current, $I_{COM(OFF)}$	V+ = 5.5V, V_{COM} = 4.5V, 1V, V_{NO} or V_{NC} = 1V, 4.5V, Note 8	25	-0.1	-	0.1	nA
		Full	-5	-	5	nA
COM ON Leakage Current, $I_{COM(ON)}$	V+ = 5.5V, V_{COM} = 5V, or V_{NO} or V_{NC} = 5V, Note 8	25	-0.2	-	0.2	nA
		Full	-10	-	10	nA
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V_{NO} or V_{NC} = 3V, R_L =1kΩ, C_L = 35pF, V_{IN} = 0 to 3V, See Figure 1	25	-	-	150	ns
		Full	-	-	240	ns
Turn-OFF Time, t_{OFF}	V_{NO} or V_{NC} = 3V, R_L =1kΩ, C_L = 35pF, V_{IN} = 0 to 3V, See Figure 1	25	-	-	100	ns
		Full	-	-	150	ns
Break-Before-Make Time Delay (ISL8325), t_D	R_L = 300Ω, C_L = 35pF, V_{NO} = V_{NC} = 3V, V_{IN} = 0 to 3V, See Figure 3	Full	2	10	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω, See Figure 2	25	-	-	5	pC
OFF Isolation	R_L = 50Ω, C_L = 5pF, f = 1MHz, See Figure 4	25	-	72	-	dB
Crosstalk (Channel-to-Channel)	R_L = 50Ω, C_L = 5pF, f = 1MHz, See Figure 6	25	-	-85	-	dB
NO or NC OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V, See Figure 7	25	-	9	-	pF
COM OFF Capacitance, $C_{COM(OFF)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V, See Figure 7	25	-	9	-	pF
COM ON Capacitance, $C_{COM(ON)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V, See Figure 7	25	-	22	-	pF
POWER SUPPLY CHARACTERISTICS						
Power Supply Range		Full	2.7		12	V
Positive Supply Current, I+	V+ = 5.5V, V_{IN} = 0V or V+, all channels on or off	Full	-1	0.0001	1	µA

Electrical Specifications - 5V Supply

Test Conditions: V+ = +4.5V to +5.5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Note 6), Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (^oC)	MIN (NOTE 7)	TYP	MAX (NOTE 7)	UNITS
DIGITAL INPUT CHARACTERISTICS						
Input Voltage Low, V_{INL}		Full	-	-	0.8	V
Input Voltage High, V_{INH}		Full	2.4	-	-	V

NOTES:

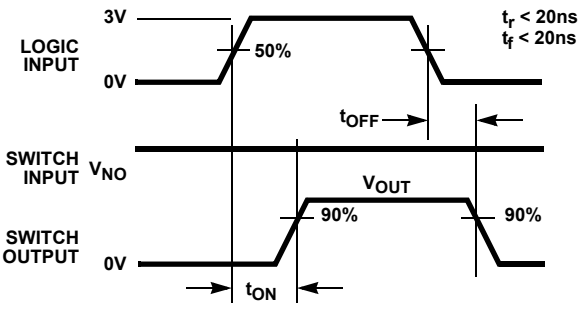
6. V_{IN} = input voltage to perform proper function.
7. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
8. Leakage parameter is 100% tested at high temp, and guaranteed by correlation at 25^{o}C.

Electrical Specifications - 3.3V Supply

Test Conditions: V+ = +3.0V to +3.6V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Note 6), Unless Otherwise Specified

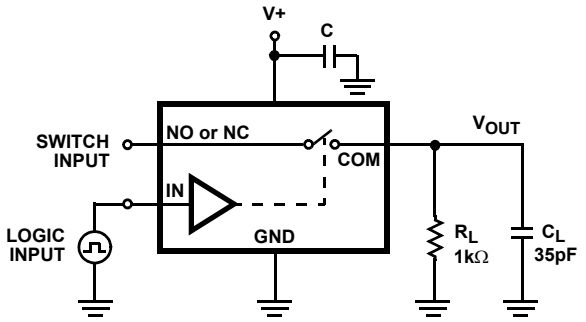
PARAMETER	TEST CONDITIONS	TEMP (^oC)	MIN (NOTE 7)	TYP	MAX (NOTE 7)	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	V+	V
ON Resistance, R_{ON}	V+ = 3V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 1.5V	25	-	-	175	Ω
		Full	-	-	275	Ω
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V_{NO} or V_{NC} = 1.5V, R_L =1kΩ, C_L = 35pF, V_{IN} = 0 to 3V	25	-	-	400	ns
		Full			500	ns
Turn-OFF Time, t_{OFF}	V_{NO} or V_{NC} = 1.5V, R_L =1kΩ, C_L = 35pF, V_{IN} = 0 to 3V	25	-	-	125	ns
		Full	-	-	175	ns
Break-Before-Make Time Delay (ISL8325), t_D	R_L = 300Ω, C_L = 35pF, V_{NO} or V_{NC} = 1.5V, V_{IN} = 0 to 3V	Full	2	-	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω	25	-	-	5	pC
POWER SUPPLY CHARACTERISTICS						
Positive Supply Current, I+	V+ = 3.6V, V_{IN} = 0V or V+, all channels on or off	Full	-1	-	1	µA

Test Circuits and Waveforms



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1A. MEASUREMENT POINTS



Repeat test for all switches. C_L includes fixture and stray capacitance.

$$V_{OUT} = V_{(NO\ or\ NC)} \frac{R_L}{R_L + R_{(ON)}}$$

FIGURE 1B. TEST CIRCUIT

FIGURE 1. SWITCHING TIMES

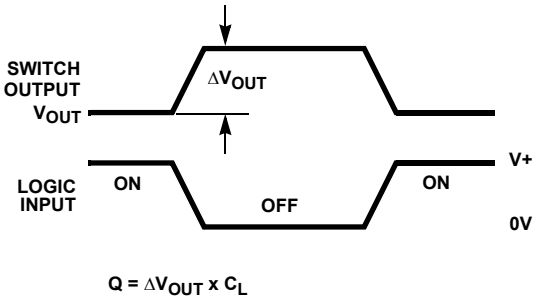


FIGURE 2A. MEASUREMENT POINTS

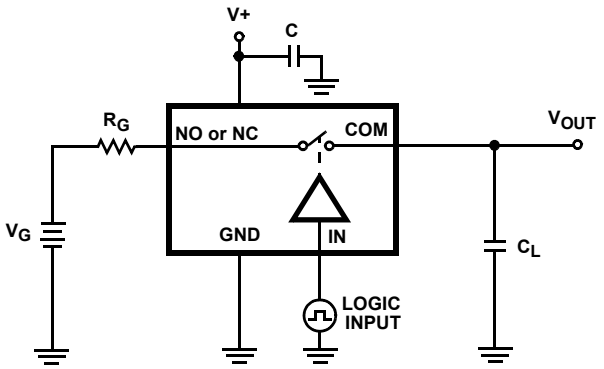


FIGURE 2B. TEST CIRCUIT

FIGURE 2. CHARGE INJECTION

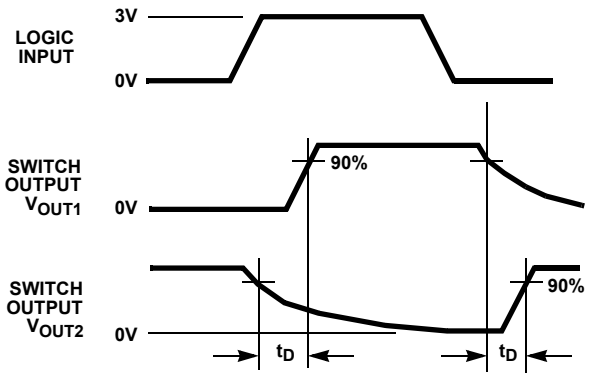
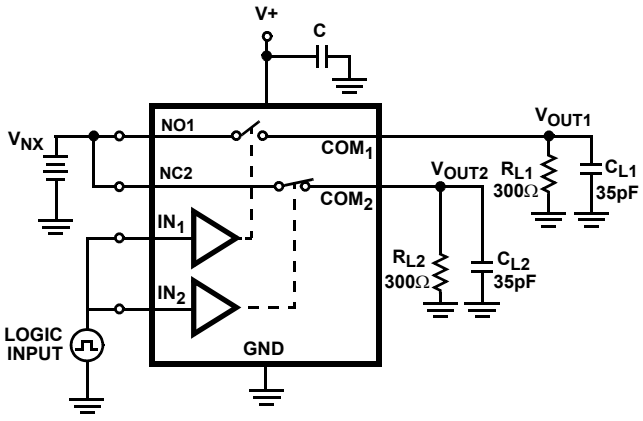


FIGURE 3A. MEASUREMENT POINTS (ISL8325 ONLY)



C_L includes fixture and stray capacitance.

FIGURE 3B. TEST CIRCUIT (ISL8325 ONLY)

FIGURE 3. BREAK-BEFORE-MAKE TIME

Test Circuits and Waveforms (Continued)

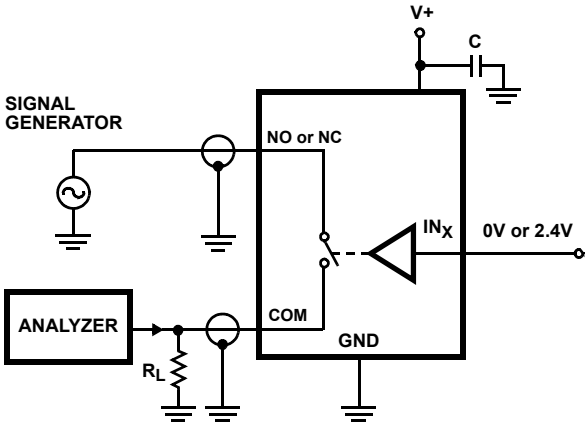


FIGURE 4. OFF ISOLATION TEST CIRCUIT

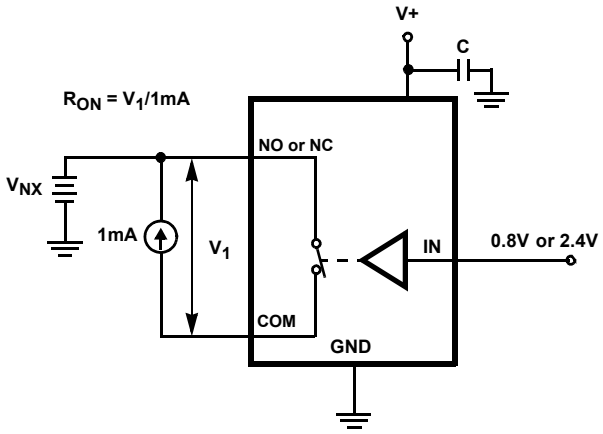


FIGURE 5. R_{ON} TEST CIRCUIT

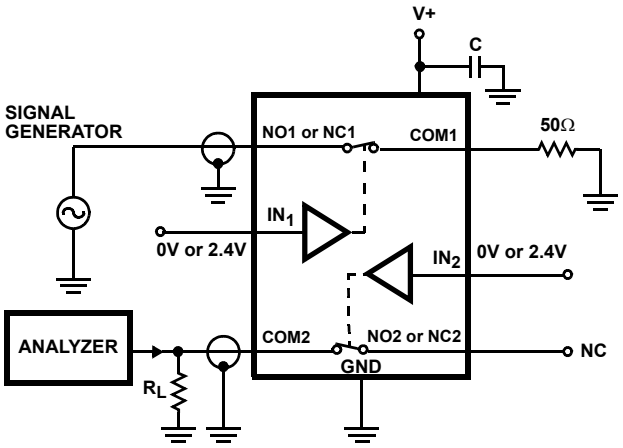


FIGURE 6. CROSSTALK TEST CIRCUIT

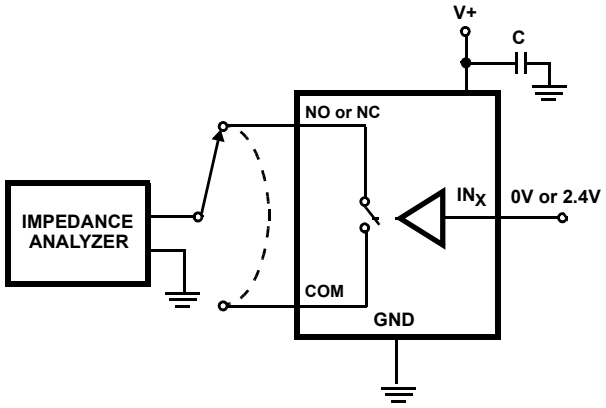


FIGURE 7. CAPACITANCE TEST CIRCUIT

Detailed Description

The ISL8323–ISL8325 dual analog switches offer precise switching capability from a single 2.7V to 12V supply with low on-resistance and high speed operation. The devices are especially well suited to portable battery powered equipment thanks to the low operating supply voltage (2.7V), low power consumption (5µW), low leakage currents (100pA max), and the small SOIC packaging. High frequency applications also benefit from the wide bandwidth, and the very high off isolation and crosstalk rejection.

Supply Sequencing And Overvoltage Protection

With any CMOS device, proper power supply sequencing is required to protect the device from excessive input currents which might permanently damage the IC. All I/O pins contain ESD protection diodes from the pin to V+ and to GND (see Figure 8). To prevent forward biasing these diodes, V+ must be applied before any input signals, and input signal voltages must remain between V+ and GND. If these conditions cannot be guaranteed, then one of the following two protection methods should be employed.

Logic inputs can easily be protected by adding a 1kΩ resistor in series with the input (see Figure 8). The resistor limits the input current below the threshold that produces permanent damage, and the sub-microamp input current produces an insignificant voltage drop during normal operation.

Adding a series resistor to the switch input defeats the purpose of using a low R_{ON} switch, so two small signal diodes can be added in series with the supply pins to provide overvoltage protection for all pins (see Figure 8). These additional diodes limit the analog signal from 1V below V+ to 1V above GND. The low leakage current performance is unaffected by this approach, but the switch resistance may increase, especially at low supply voltages.

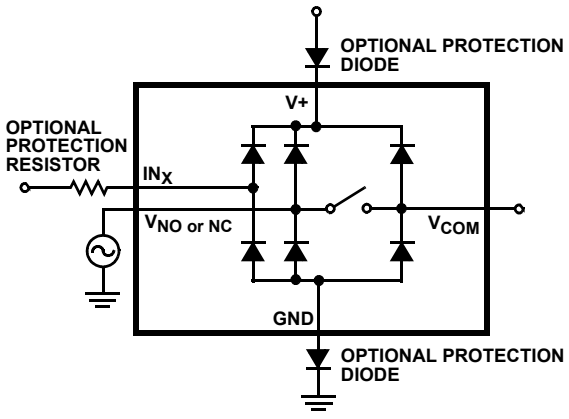


FIGURE 8. OVERVOLTAGE PROTECTION

Power-Supply Considerations

The ISL832X construction is typical of most CMOS analog switches, except that they have only two supply pins: V+ and GND. V+ and GND drive the internal CMOS switches and set their analog voltage limits. Unlike switches with a 13V maximum supply voltage, the ISL832X 15V maximum supply voltage provides plenty of room for the 10% tolerance of 12V supplies, as well as room for overshoot and noise spikes.

The minimum recommended supply voltage is 2.7V. It is important to note that the input signal range, switching times, and on-resistance degrade at lower supply voltages. Refer to the electrical specification tables and *Typical Performance* curves for details.

V+ and GND also power the internal logic and level shifters. The level shifters convert the logic levels to switched V+ and GND signals to drive the analog switch gate terminals.

This family of switches cannot be operated with bipolar supplies, because the input switching point becomes negative in this configuration.

Logic-Level Thresholds

This switch family is TTL compatible (0.8V and 2.4V) over a supply range of 3V to 11V (see Figure 12). At 12V the V_{IH} level is about 2.5V. This is still below the TTL guaranteed high output minimum level of 2.8V, but noise margin is reduced. For best results with a 12V supply, use a logic family the provides a V_{OH} greater than 3V.

The digital input stages draw supply current whenever the digital input voltage is not at one of the supply rails. Driving the digital input signals from GND to V+ with a fast transition time minimizes power dissipation.

Leakage Considerations

Reverse ESD protection diodes are internally connected between each analog-signal pin and both V+ and GND. One of these diodes conducts if any analog signal exceeds V+ or GND.

Virtually all the analog leakage current comes from the ESD diodes to V+ or GND. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or GND and the analog signal. This means their leakages will vary as the signal varies. The difference in the two diode leakages to the V+ and GND pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of the same or opposite polarity. There is no connection between the analog-signal paths and V+ or GND.

Typical Performance Curves $T_A = 25^oC$, Unless Otherwise Specified

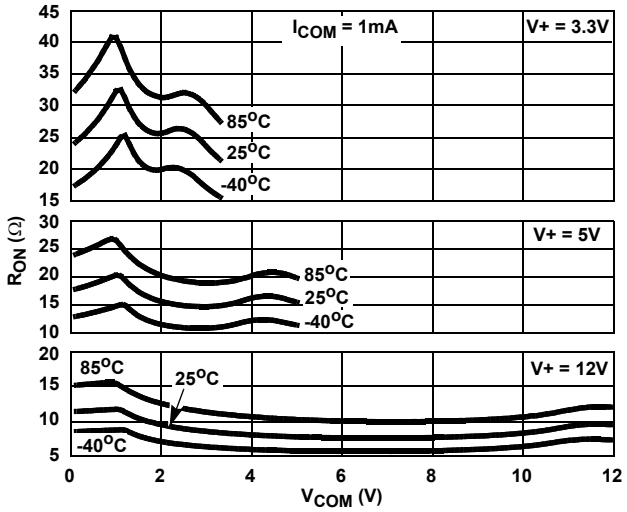


FIGURE 9. ON RESISTANCE vs SWITCH VOLTAGE

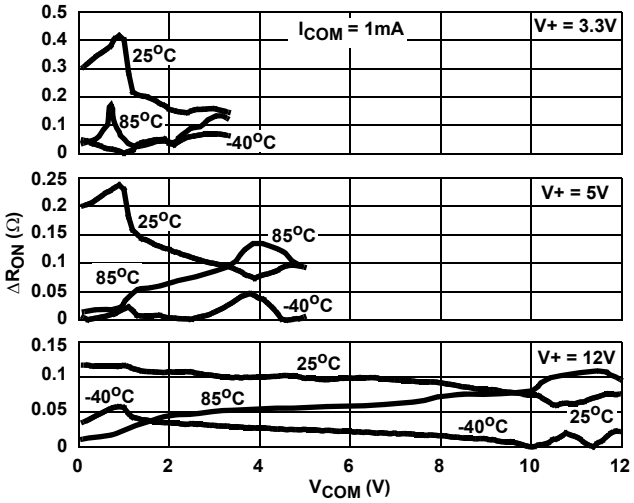


FIGURE 10. R_{ON} MATCH vs SWITCH VOLTAGE

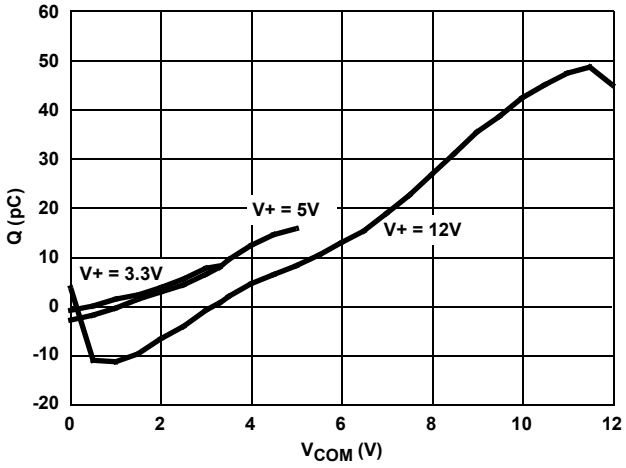


FIGURE 11. CHARGE INJECTION vs SWITCH VOLTAGE

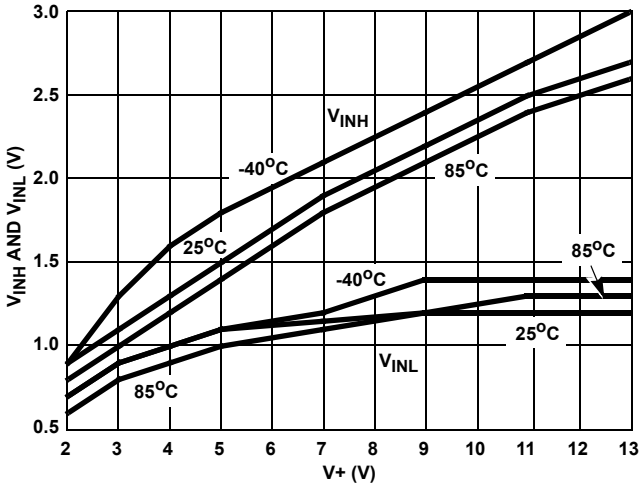


FIGURE 12. DIGITAL SWITCHING POINT vs SUPPLY VOLTAGE

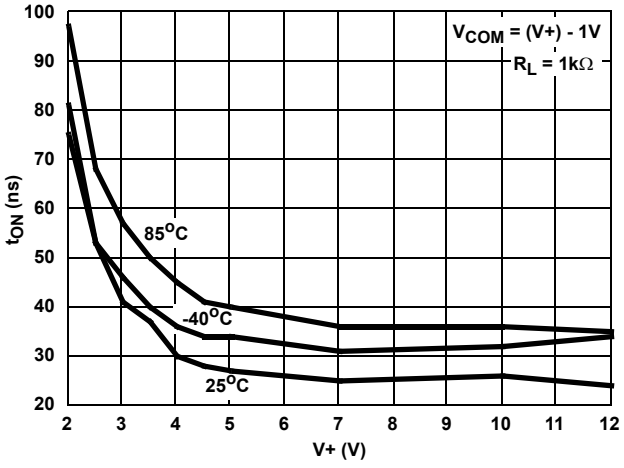


FIGURE 13. TURN - ON TIME vs SUPPLY VOLTAGE

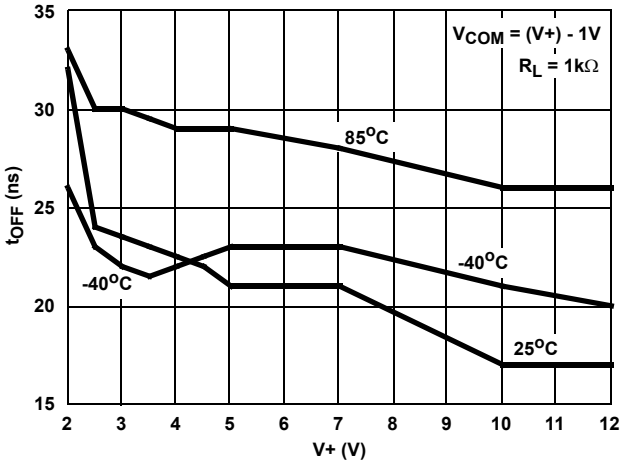


FIGURE 14. TURN - OFF TIME vs SUPPLY VOLTAGE

Die Characteristics

DIE DIMENSIONS:

ISL832X:
54 mils x 28 mils (1370µm x 710µm)

METALLIZATION:

Type: Metal 1: AlSi(1%)
Thickness: Metal 1: 8kÅ
Type: Metal 2: AlSi (1%)
Thickness: Metal 2: 10kÅ

SUBSTRATE POTENTIAL (POWERED UP):

GND

PASSIVATION:

Type: Silox
Thickness: 13kÅ

TRANSISTOR COUNT:

ISL8323: 66
ISL8324: 66
ISL8325: 66

PROCESS:

Si Gate CMOS

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
October 7, 2015	FN6023.1	Updated the Ordering Information table on page page 2. Added Revision History and About Intersil sections. Updated Package Outline Drawing M8.15 to the latest revision. Changes are as follows: -New Revision. Remove "u" symbol from drawing (overlaps the "a" on Side View). -Updated to new POD format by removing table and moving dimensions onto drawing and adding land pattern. -Changed in Typical Recommended Land Pattern the following: 2.41(0.095) to 2.20(0.087) 0.76 (0.030) to 0.60(0.023) 0.200 to 5.20(0.205) -Changed Note 1 "1982" to "1994".

About Intersil

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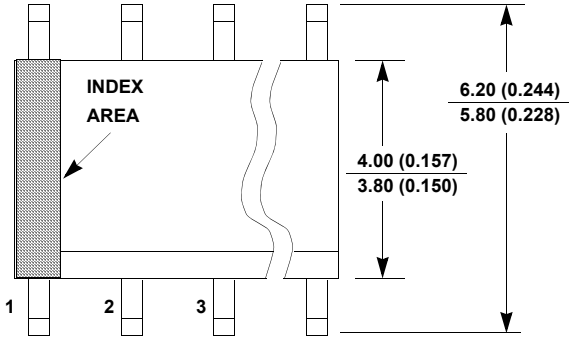
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Package Outline Drawing

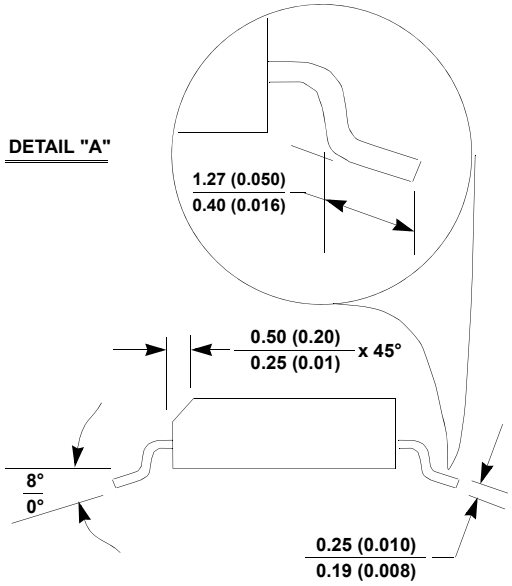
M8.15

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

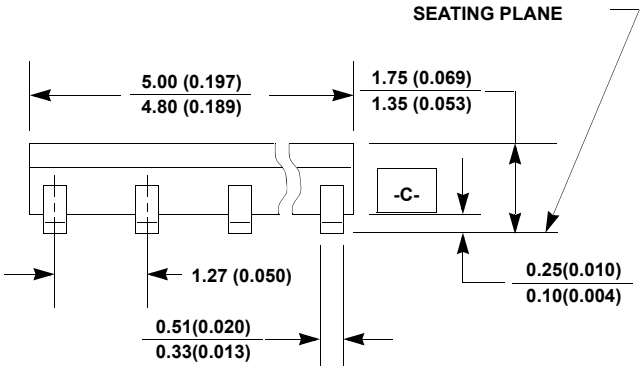
Rev 4, 1/12



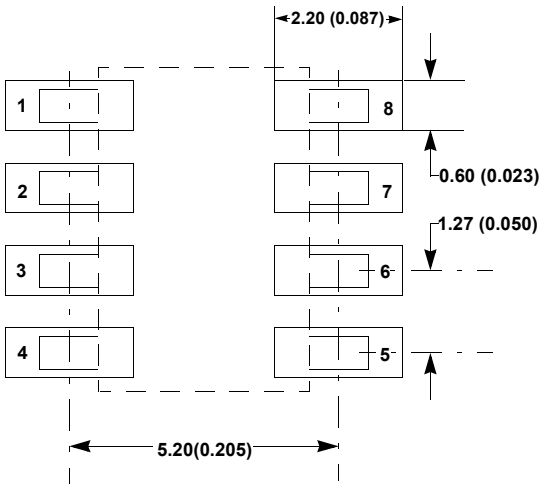
TOP VIEW



SIDE VIEW "B"



SIDE VIEW "A"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensioning and tolerancing per ANSI Y14.5M-1994.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.