8-Lane 5-Port PCI Express® Switch

89HPES8T5A
Data Sheet

Device Overview

The 89HPES8T5A is a member of IDT's PRECISE™ family of PCI Express switching solutions. The PES8T5A is an 8-lane, 5-port peripheral chip that performs PCI Express Base switching. It provides connectivity and switching functions between a PCI Express upstream port and up to four downstream ports and supports switching between downstream ports.

Features

- High Performance PCI Express Switch
  - *Eight 2.5Gbps PCI Express lanes*
  - *Five switch ports*
  - *Upstream port is x4*
  - *Downstream ports are x1*
  - *Low-latency cut-through switch architecture*
  - *Support for Max Payload Sizes up to 256 bytes*
  - *One virtual channel*
  - *Eight traffic classes*
  - *PCI Express Base Specification Revision 1.1 compliant*
- Flexible Architecture with Numerous Configuration Options
  - *Automatic lane reversal on all ports*
  - *Automatic polarity inversion on all lanes*
  - *Ability to load device configuration from serial EEPROM*
- Legacy Support
  - *PCI compatible INTx emulation*
  - *Bus locking*
- Highly Integrated Solution
  - *Requires no external components*
  - *Incorporates on-chip internal memory for packet buffering and queueing*
  - *Integrates eight 2.5 Gbps embedded SerDes with 8B/10B encoder/decoder (no separate transceivers needed)*
- Reliability, Availability, and Serviceability (RAS) Features
  - *Internal end-to-end parity protection on all TLPs ensures data integrity even in systems that do not implement end-to-end CRC (ECRC)*
  - *Supports ECRC and Advanced Error Reporting*
  - *Supports PCI Express Native Hot-Plug, Hot-Swap capable I/O*
  - *Compatible with Hot-Plug I/O expanders used on PC motherboards*
- Power Management
  - *Utilizes advanced low-power design techniques to achieve low typical power consumption*
  - *Supports PCI Power Management Interface specification (PCI-PM 1.2)*
  - *Unused SerDes are disabled.*
  - *Supports Advanced Configuration and Power Interface Specification, Revision 2.0 (ACPI) supporting active link state*
- Testability and Debug Features
  - *Built in Pseudo-Random Bit Stream (PRBS) generator*
  - *Numerous SerDes test modes*
  - *Ability to read and write any internal register via the SMBus*
  - *Ability to bypass link training and force any link into any mode*
  - *Provides statistics and performance counters*

Block Diagram

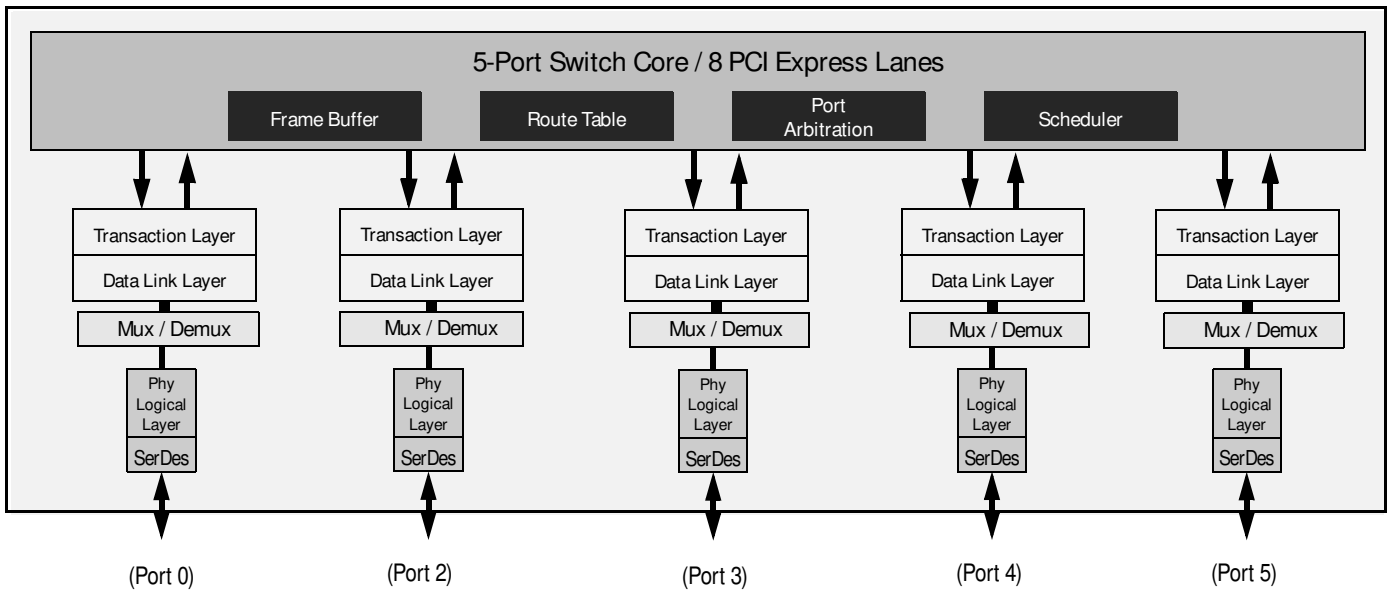

Figure 1 Internal Block Diagram

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- 11 General Purpose Input/Output Pins
  - *Each pin may be individually configured as an input or output*
  - *Each pin may be individually configured as an interrupt input*
  - *Some pins have selectable alternate functions*
- Packaged in a 15mm x 15mm 196-ball BGA with 1mm ball spacing

Product Description

Utilizing standard PCI Express interconnect, the PES8T5A provides the most efficient I/O connectivity solution for applications requiring high throughput, low latency, and simple board layout with a minimum number of board layers. It provides 3 GBps (24 Gbps) of aggregated, full-duplex switching capacity through 6 integrated serial lanes, using proven and robust IDT technology. Each lane provides 2.5 Gbps of bandwidth in both directions and is fully compliant with PCI Express Base specification revision 1.1.

The PES8T5A is based on a flexible and efficient layered architecture. The PCI Express layer consists of SerDes, Physical, Data Link and Transaction layers in compliance with PCI Express Base specification Revision 1.1. The PES8T5A can operate either as a store and forward or cut-through switch and is designed to switch memory and I/O transactions. It supports eight Traffic Classes (TCs) and one Virtual Channel (VC) with sophisticated resource management to allow efficient switching for applications requiring additional narrow port connectivity.

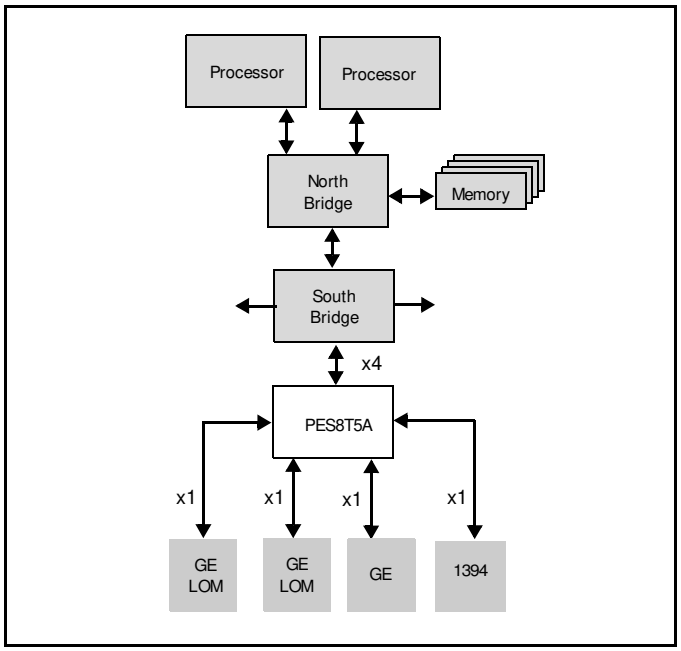

Figure 2 I/O Expansion Application

SMBus Interface

The PES8T5A contains two SMBus interfaces. The slave interface provides full access to the configuration registers in the PES8T5A, allowing every configuration register in the device to be read or written by an external agent. The master interface allows the default configuration register values of the PES8T5A to be overridden following a reset with values programmed in an external serial EEPROM. The master interface is also used by an external Hot-Plug I/O expander.

Six pins make up each of the two SMBus interfaces. These pins consist of an SMBus clock pin, an SMBus data pin, and 4 SMBus address pins. In the slave interface, these address pins allow the SMBus address to which the device responds to be configured. In the master interface, these address pins allow the SMBus address of the serial configuration EEPROM from which data is loaded to be configured. The SMBus address is set up on negation of PERSTN by sampling the corresponding address pins. When the pins are sampled, the resulting address is assigned as shown in Table 1.

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Bit	Slave SMBus Address	Master SMBus Address
1	SSMBADDR[1]	MSMBADDR[1]
2	SSMBADDR[2]	MSMBADDR[2]
3	SSMBADDR[3]	MSMBADDR[3]
4	0	MSMBADDR[4]
5	SSMBADDR[5]	1
6	1	0
7	1	1

Table 1 Master and Slave SMBus Address Assignment

As shown in Figure 3, the master and slave SMBuses may be used in a unified or split configuration. In the unified configuration, shown in Figure 3(a), the master and slave SMBuses are tied together and the PES8T5A acts both as a SMBus master as well as a SMBus slave on this bus. This requires that the SMBus master or processor that has access to PES8T5A registers supports SMBus arbitration. In some systems, this SMBus master interface may be implemented using general purpose I/O pins on a processor or micro controller, and may not support SMBus arbitration. To support these systems, the PES8T5A may be configured to operate in a split configuration as shown in Figure 3(b).

In the split configuration, the master and slave SMBuses operate as two independent buses and thus multi-master arbitration is never required. The PES8T5A supports reading and writing of the serial EEPROM on the master SMBus via the slave SMBus, allowing in system programming of the serial EEPROM.

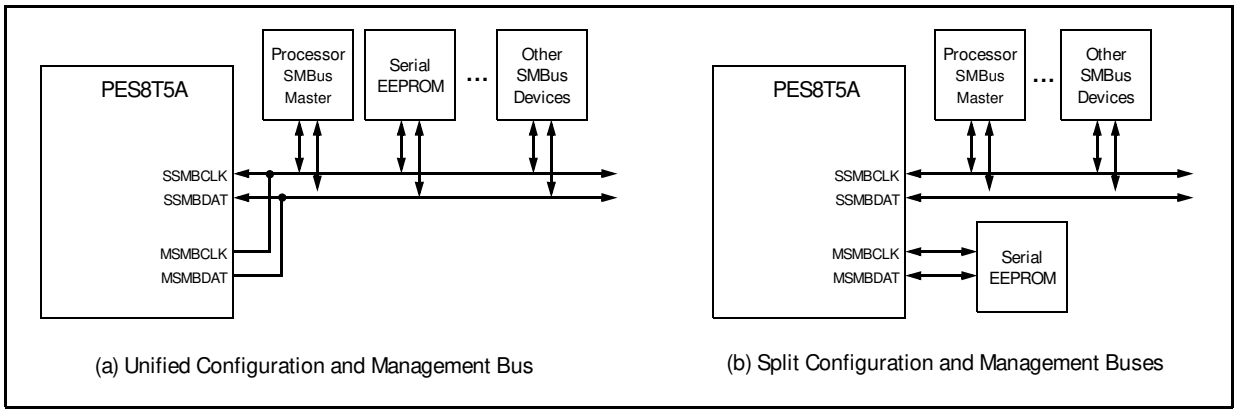

Figure 3 SMBus Interface Configuration Examples

Hot-Plug Interface

The PES8T5A supports PCI Express Hot-Plug on each downstream port. To reduce the number of pins required on the device, the PES8T5A utilizes an external I/O expander, such as that used on PC motherboards, connected to the SMBus master interface. Following reset and configuration, whenever the state of a Hot-Plug output needs to be modified, the PES8T5A generates an SMBus transaction to the I/O expander with the new value of all of the outputs. Whenever a Hot-Plug input changes, the I/O expander generates an interrupt which is received on the IOEXPINTN input pin (alternate function of GPIO) of the PES8T5A. In response to an I/O expander interrupt, the PES8T5A generates an SMBus transaction to read the state of all of the Hot-Plug inputs from the I/O expander.

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General Purpose Input/Output

The PES8T5A provides 11 General Purpose Input/Output (GPIO) pins that may be used by the system designer as bit I/O ports. Each GPIO pin may be configured independently as an input or output through software control. Some GPIO pins are shared with other on-chip functions. These alternate functions may be enabled via software, SMBus slave interface, or serial configuration EEPROM.

Pin Description

The following tables lists the functions of the pins provided on the PES8T5A. Some of the functions listed may be multiplexed onto the same pin. The active polarity of a signal is defined using a suffix. Signals ending with an “N” are defined as being active, or asserted, when at a logic zero (low) level. All other signals (including clocks, buses, and select lines) will be interpreted as being active, or asserted, when at a logic one (high) level.

Signal	Type	Name/Description
PE0RP[3:0] PE0RN[3:0]	I	PCI Express Port 0 Serial Data Receive. Differential PCI Express receive pairs for port 0.
PE0TP[3:0] PE0TN[3:0]	O	PCI Express Port 0 Serial Data Transmit. Differential PCI Express transmit pairs for port 0.
PE2RP[0] PE2RN[0]	I	PCI Express Port 2 Serial Data Receive. Differential PCI Express receive pair for port 2.
PE2TP[0] PE2TN[0]	O	PCI Express Port 2 Serial Data Transmit. Differential PCI Express transmit pair for port 2.
PE3RP[0] PE3RN[0]	I	PCI Express Port 3 Serial Data Receive. Differential PCI Express receive pair for port 3.
PE3TP[0] PE3TN[0]	O	PCI Express Port 3 Serial Data Transmit. Differential PCI Express transmit pair for port 3.
PE4RP[0] PE4RN[0]	I	PCI Express Port 4 Serial Data Receive. Differential PCI Express receive pair for port 4.
PE4TP[0] PE4TN[0]	O	PCI Express Port 4 Serial Data Transmit. Differential PCI Express transmit pair for port 4.
PE5RP[0] PE5RN[0]	I	PCI Express Port 5 Serial Data Receive. Differential PCI Express receive pair for port 5.
PE5TP[0] PE5TN[0]	O	PCI Express Port 5 Serial Data Transmit. Differential PCI Express transmit pair for port 5.
PEREFCLKP PEREFCLKN	I	PCI Express Reference Clock. Differential reference clock pair input. This clock is used as the reference clock by on-chip PLLs to generate the clocks required for the system logic and on-chip SerDes. The frequency of the differential reference clock is determined by the REFCLKM signal.
REFCLKM	I	PCI Express Reference Clock Mode Select. This signal selects the frequency of the reference clock input. 0x0 - 100 MHz 0x1 - 125 MHz

Table 2 PCI Express Interface Pins

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Signal	Type	Name/Description
MSMBADDR[4:1]	I	Master SMBus Address. These pins determine the SMBus address of the serial EEPROM from which configuration information is loaded.
MSMBCLK	I/O	Master SMBus Clock. This bidirectional signal is used to synchronize transfers on the master SMBus.
MSMBDAT	I/O	Master SMBus Data. This bidirectional signal is used for data on the master SMBus.
SSMBADDR[5,3:1]	I	Slave SMBus Address. These pins determine the SMBus address to which the slave SMBus interface responds.
SSMBCLK	I/O	Slave SMBus Clock. This bidirectional signal is used to synchronize transfers on the slave SMBus.
SSMBDAT	I/O	Slave SMBus Data. This bidirectional signal is used for data on the slave SMBus.

Table 3 SMBus Interface Pins

Signal	Type	Name/Description
GPIO[0]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: P2RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 2
GPIO[1]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: P4RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 4
GPIO[2]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN0 Alternate function pin type: Input Alternate function: I/O Expander interrupt 0 input
GPIO[3]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN1 Alternate function pin type: Input Alternate function: I/O Expander interrupt 1 input
GPIO[4]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN2 Alternate function pin type: Input Alternate function: I/O Expander interrupt 2 input
GPIO[5]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin.
GPIO[6]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin.

Table 4 General Purpose I/O Pins (Part 1 of 2)

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Signal	Type	Name/Description
GPIO[7]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: GPEN Alternate function pin type: Output Alternate function: General Purpose Event (GPE) output
GPIO[8]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin.
GPIO[9]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: P3RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 3
GPIO[10]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: P5RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 5

Table 4 General Purpose I/O Pins (Part 2 of 2)

Signal	Type	Name/Description
APWRDISN	I	Auxiliary Power Disable Input. When this pin is active, it disables the device from using auxiliary power supply.
CCLKDS	I	Common Clock Downstream. The assertion of this pin indicates that all downstream ports are using the same clock source as that provided to downstream devices.This bit is used as the initial value of the Slot Clock Configuration bit in all of the Link Status Registers for downstream ports. The value may be override by modifying the SCLK bit in the downstream port's PCIELSTS register.
CCLKUS	I	Common Clock Upstream. The assertion of this pin indicates that the upstream port is using the same clock source as the upstream device. This bit is used as the initial value of the Slot Clock Configuration bit in the Link Status Register for the upstream port. The value may be overridden by modifying the SCLK bit in the PA_PCIELSTS register.
MSMBSMODE	I	Master SMBus Slow Mode. The assertion of this pin indicates that the master SMBus should operate at 100 KHz instead of 400 kHz. This value may not be overridden.
PERSTN	I	Fundamental Reset. Assertion of this signal resets all logic inside the PES8T5A and initiates a PCI Express fundamental reset.

Table 5 System Pins (Part 1 of 2)

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Signal	Type	Name/Description
RSTHALT	I	**Reset Halt.** When this signal is asserted during a PCI Express fundamental reset, the PES8T5A executes the reset procedure and remains in a reset state with the Master and Slave SMBuses active. This allows software to read and write registers internal to the device before normal device operation begins. The device exits the reset state when the RSTHALT bit is cleared in the PA_SWCTL register by an SMBus master.
SWMODE[2:0]	I	**Switch Mode.** These configuration pins determine the PES8T5A switch operating mode. 0x0 - Normal switch mode 0x1 - Normal switch mode with Serial EEPROM initialization 0x2 - through 0xF Reserved
WAKEN	I/O	**Wake Input/Output.** The WAKEN signal is an input or output. The WAKEN signal input/output selection can be made through the WAKEDIR bit setting in the WAKEUPCNTL register.

Table 5 System Pins (Part 2 of 2)

Signal	Type	Name/Description
JTAG_TCK	I	**JTAG Clock.** This is an input test clock used to clock the shifting of data into or out of the boundary scan logic or JTAG Controller. JTAG_TCK is independent of the system clock with a nominal 50% duty cycle.
JTAG_TDI	I	**JTAG Data Input.** This is the serial data input to the boundary scan logic or JTAG Controller.
JTAG_TDO	O	**JTAG Data Output.** This is the serial data shifted out from the boundary scan logic or JTAG Controller. When no data is being shifted out, this signal is tri-stated.
JTAG_TMS	I	**JTAG Mode.** The value on this signal controls the test mode select of the boundary scan logic or JTAG Controller.
JTAG_TRST_N	I	**JTAG Reset.** This active low signal asynchronously resets the boundary scan logic and JTAG TAP Controller. An external pull-up on the board is recommended to meet the JTAG specification in cases where the tester can access this signal. However, for systems running in functional mode, one of the following should occur: 1) actively drive this signal low with control logic 2) statically drive this signal low with an external pull-down on the board

Table 6 Test Pins

Signal	Type	Name/Description
V_{DD}CORE	I	**Core VDD.** Power supply for core logic.
V_{DD}IO	I	**I/O VDD.** LVTTL I/O buffer power supply.
V_{DD}PE	I	**PCI Express Digital Power.** PCI Express digital power used by the digital power of the SerDes.
V_{DD}APE	I	**PCI Express Analog Power.** PCI Express analog power used by the PLL and bias generator.
V_{TT}PE	I	**PCI Express Termination Power.**
V_{SS}	I	**Ground.**

Table 7 Power and Ground Pins

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Pin Characteristics

Note: Some input pads of the PES8T5A do not contain internal pull-ups or pull-downs. Unused inputs should be tied off to appropriate levels. This is especially critical for unused control signal inputs which, if left floating, could adversely affect operation. Also, any input pin left floating can cause a slight increase in power consumption.

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor	Notes
PCI Express Interface	PE0RN[1:0]	I	CML	Serial Link		
	PE0RP[1:0]	I				
	PE0TN[1:0]	O				
	PE0TP[1:0]	O				
	PE2RN[0]	I				
	PE2RP[0]	I				
	PE2TN[0]	O				
	PE2TP[0]	O				
	PE3RN[0]	I				
	PE3RP[0]	I				
	PE3TN[0]	O				
	PE3TP[0]	O				
	PE4RN[0]	I				
	PE4RP[0]	I				
	PE4TN[0]	O				
	PE4TP[0]	O				
	PE5RN[0]	I				
	PE5RP[0]	I				
	PE5TN[0]	O				
	PE5TP[0]	O				
	PEREFCLKN	I	LVPECL/ CML	Diff. Clock Input		Refer to Table 9
	PEREFCLKP	I				
	REFCLKM	I	LVTTL	Input	pull-down	
SMBus	MSMBADDR[4:1]	I	LVTTL	Input	pull-up	
	MSMBCLK	I/O		STI[1]		
	MSMBDAT	I/O		STI		
	SSMBADDR[5,3:1]	I		Input	pull-up	
	SSMBCLK	I/O		STI		
	SSMBDAT	I/O		STI		
General Purpose I/O	GPIO[10:0]	I/O	LVTTL	High Drive	pull-up	

Table 8 Pin Characteristics (Part 1 of 2)

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Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor	Notes
System Pins	APWRDISN	I	LVTTL	Input	pull-down	
	CCLKDS	I			pull-up	
	CCLKUS	I			pull-up	
	MSMBSMODE	I			pull-down	
	PERSTN	I			pull-up	
	RSTHALT	I			pull-down	
	SWMODE[2:0]	I			pull-down	
	WAKEN	I/O			open-drain	
EJTAG / JTAG	JTAG_TCK	I	LVTTL	STI	pull-up	
	JTAG_TDI	I		STI	pull-up	
	JTAG_TDO	O				
	JTAG_TMS	I		STI	pull-up	
	JTAG_TRST_N	I		STI	pull-up	

Table 8 Pin Characteristics (Part 2 of 2)

1. Schmitt Trigger Input (STI).

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Logic Diagram — PES8T5A

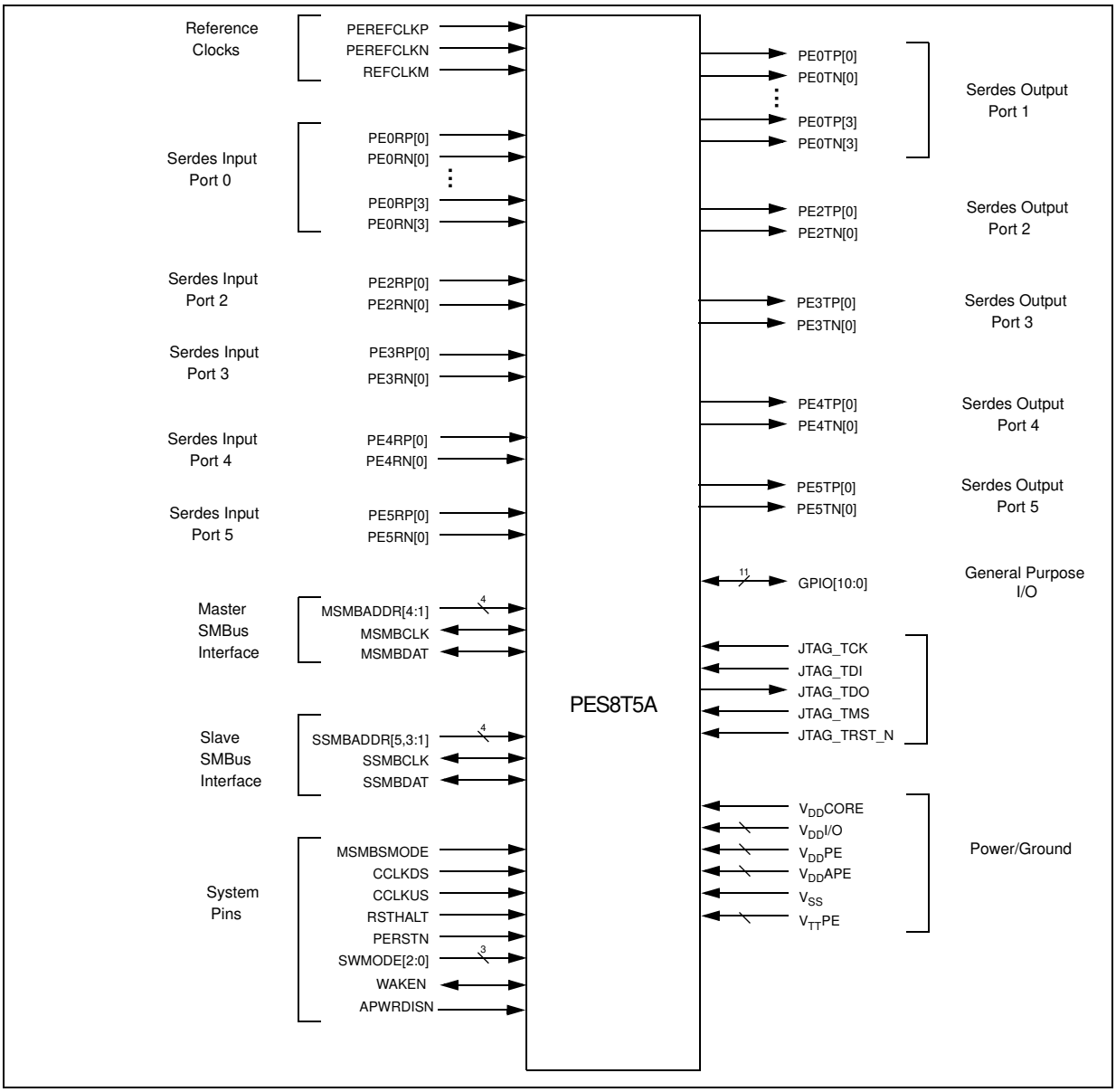

Figure 4 PES8T5A Logic Diagram

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System Clock Parameters

Values based on systems running at recommended supply voltages and operating temperatures, as shown in Tables 13 and 14.

Parameter	Description	Min	Typical	Max	Unit
PEREFCLK					
$Refclk_{FREQ}$	Input reference clock frequency range	100		125[1]	MHz
$Refclk_{DC}$[2]	Duty cycle of input clock	40	50	60	%
T_R, T_F	Rise/Fall time of input clocks			0.2*RCUI	RCUI[3]
V_{SW}	Differential input voltage swing[4]	0.6		1.6	V
T_{jitter}	Input clock jitter (cycle-to-cycle)			125	ps

Table 9 Input Clock Requirements

1. The input clock frequency will be either 100 or 125 MHz depending on signal REFCLKM.
2. ClkIn must be AC coupled. Use 0.01 — 0.1 µF ceramic capacitors.
3. RCUI (Reference Clock Unit Interval) refers to the reference clock period.
4. AC coupling required.

AC Timing Characteristics

Parameter	Description	Min[1]	Typical[1]	Max[1]	Units
PCIe Transmit					
UI	Unit Interval	399.88	400	400.12	ps
T_{TX-EYE}	Minimum Tx Eye Width	0.7	.9		UI
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median			0.15	UI
$T_{TX-RISE}$, $T_{TX-FALL}$	D+ / D- Tx output rise/fall time	50	90		ps
$T_{TX- IDLE-MIN}$	Minimum time in idle	50			UI
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid Idle after sending an Idle ordered set			20	UI
$T_{TX-IDLE-TO-DIFF-DATA}$	Maximum time to transition from valid idle to diff data			20	UI
$T_{TX-SKEW}$	Transmitter data skew between any 2 lanes		500	1300	ps
T_{BTEn}	Time from asserting Beacon TxEn to beacon being transmitted on the lane		30	80	ns
PCIe Receive					
UI	Unit Interval	399.88	400	400.12	ps
T_{RX-EYE} (with jitter)	Minimum Receiver Eye Width (jitter tolerance)	0.4			UI

Table 10 PCIe AC Timing Characteristics (Part 1 of 2)

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Parameter	Description	Min[1]	Typical[1]	Max[1]	Units
$T_{RX-EYE-MEDIUM\ TO\ MAX\ JITTER}$	Max time between jitter median & max deviation			0.3	UI
$T_{RX-IDLE-DET-DIFF-ENTER\ TIME}$	Unexpected Idle Enter Detect Threshold Integration Time			10	ms
$T_{RX-SKEW}$	Lane to lane input skew			20	ns

Table 10 PCIe AC Timing Characteristics (Part 2 of 2)

1. Minimum, Typical, and Maximum values meet the requirements under PCI Specification 1.1

Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
GPIO						
GPIO[10:0][1]	Tpw_13b[2]	None	50	—	ns	See Figure 5.

Table 11 GPIO AC Timing Characteristics

1. GPIO signals must meet the setup and hold times if they are synchronous or the minimum pulse width if they are asynchronous.

2. The values for this symbol were determined by calculation, not by testing.

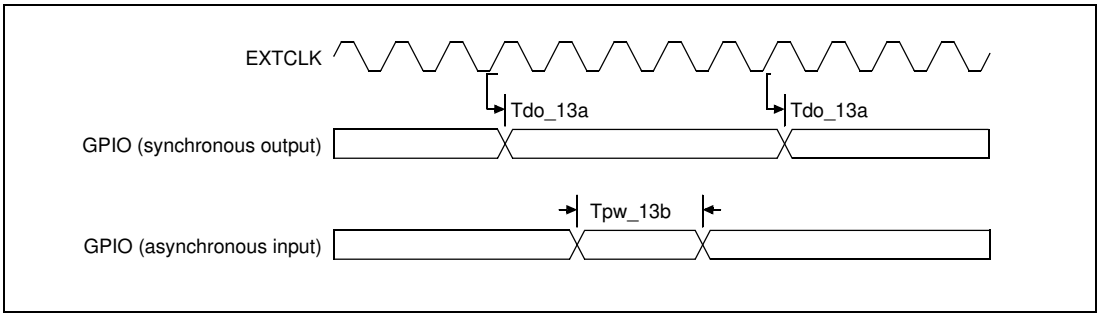

Figure 5 GPIO AC Timing Waveform

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Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
JTAG						
JTAG_TCK	Tper_16a	none	25.0	50.0	ns	See Figure 6.
	Thigh_16a, Tlow_16a		10.0	25.0	ns	
JTAG_TMS[1], JTAG_TDI	Tsu_16b	JTAG_TCK rising	2.4	—	ns	
	Thld_16b		1.0	—	ns	
JTAG_TDO	Tdo_16c	JTAG_TCK falling	—	11.3	ns	
	Tdz_16c[2]		—	11.3	ns	
JTAG_TRST_N	Tpw_16d[2]	none	25.0	—	ns	

Table 12 JTAG AC Timing Characteristics

1. The JTAG specification, IEEE 1149.1, recommends that JTAG_TMS should be held at 1 while the signal applied at JTAG_TRST_N changes from 0 to 1. Otherwise, a race may occur if JTAG_TRST_N is deasserted (going from low to high) on a rising edge of JTAG_TCK when JTAG_TMS is low, because the TAP controller might go to either the Run-Test/Idle state or stay in the Test-Logic-Reset state.

2. The values for this symbol were determined by calculation, not by testing.

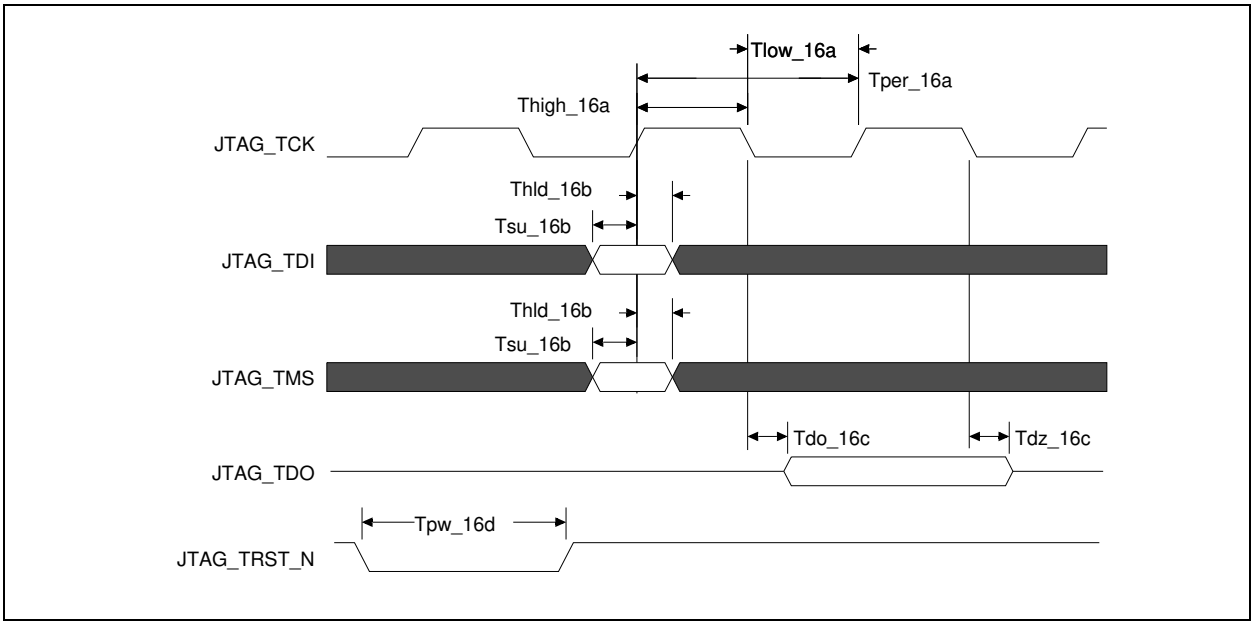

Figure 6 JTAG AC Timing Waveform

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Recommended Operating Supply Voltages

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{DD}CORE	Internal logic supply	0.9	1.0	1.1	V
V_{DD}I/O	I/O supply except for SerDes LVPECL/CML	3.135	3.3	3.465	V
V_{DD}PE	PCI Express Digital Power	0.9	1.0	1.1	V
V_{DD}APE	PCI Express Analog Power	0.9	1.0	1.1	V
V_{TT}PE	PCI Express Serial Data Transmit Termination Voltage	1.425	1.5	1.575	V
V_{SS}	Common ground	0	0	0	V

Table 13 PES8T5A Operating Voltages

Power-Up/Power-Down Sequence

This section describes the sequence in which various voltages must be applied to the part during power-up to ensure proper functionality. For the PES8T5A, the power-up sequence must be as follows:

1. V_{DD}I/O — 3.3V
2. V_{DD}Core, V_{DD}PE, V_{DD}APE — 1.0V
3. V_{TT}PE — 1.5V

When powering up, each voltage level must ramp and stabilize prior to applying the next voltage in the sequence to ensure internal latch-up issues are avoided. There are no maximum time limitations in ramping to valid power levels.

The power-down sequence must be in the reverse order of the power-up sequence.

Recommended Operating Temperature

Grade	Temperature
Commercial	0°C to +70°C Ambient
Industrial	-40°C to +85°C Ambient

Table 14 PES8T5A Operating Temperatures

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Power Consumption

Typical power is measured under the following conditions: 25°C Ambient, 35% total link usage on all ports, typical voltages defined in Table 13.

Maximum power is measured under the following conditions: 70°C Ambient, 85% total link usage on all ports, maximum voltages defined in Table 13.

All power measurements assume that the part is mounted on a 10 layer printed circuit board with 0 LFM airflow.

Number of Connected Lanes		Core Supply		PCIe Digital Supply		PCIe Analog Supply		PCIe Termination Supply		I/O Supply		Total	
		Typ 1.0V	Max 1.1V	Typ 1.0V	Max 1.1V	Typ 1.0V	Max 1.1V	Typ 1.5V	Max 1.575V	Typ 3.3V	Max 3.465V	Typ Power	Max Power
4/1/1/1/1	mA	308	495	327	440	130	187	161	222	3	3.3		
	Watts	0.31	0.54	0.33	0.48	0.13	0.21	0.24	0.35	0.01	0.01	1.02	1.60

Table 15 PES8T5A Power Consumption

Thermal Considerations

This section describes thermal considerations for the PES8T5A (15mm^2 BCG196 package). The data in Table 16 below contains information that is relevant to the thermal performance of the PES8T5A switch.

Symbol	Parameter	Value	Units	Conditions
$T_{J(max)}$	Junction Temperature	125	°C	Maximum
$T_{A(max)}$	Ambient Temperature	70	°C	Maximum for commercial-rated products
$T_{A(max)}$	Ambient Temperature	85	°C	Maximum for industrial-rated products
$\theta_{JA(effective)}$	Effective Thermal Resistance, Junction-to-Ambient	33.3	°C/W	Zero air flow
		29	°C/W	1 m/S air flow
		26.6	°C/W	2 m/S air flow
θ_{JB}	Thermal Resistance, Junction-to-Board	18.7	°C/W	
θ_{JC}	Thermal Resistance, Junction-to-Case	9.8	°C/W	
P	Power Dissipation of the Device	1.60	Watts	Maximum

Table 16 Thermal Specifications for PES8T5A, 15x15mm BCG196 Package

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DC Electrical Characteristics

Values based on systems running at recommended supply voltages, as shown in Table 13.

Note: See Table 8, Pin Characteristics, for a complete I/O listing.

I/O Type	Parameter	Description	Min[1]	Typ[1]	Max[1]	Unit	Conditions
Serial Link	PCIe Transmit						
	$V_{TX-DIFFp-p}$	Differential peak-to-peak output voltage	800		1200	mV	
	$V_{TX-DE-RATIO}$	De-emphasized differential output voltage	-3		-4	dB	
	$V_{TX-DC-CM}$	DC Common mode voltage	-0.1	1	3.7	V	
	$V_{TX-CM-ACP}$	RMS AC peak common mode output voltage			20	mV	
	$V_{TX-CM-DC-active-idle-delta}$	Abs delta of DC common mode voltage between L0 and idle			100	mV	
	$V_{TX-CM-DC-line-delta}$	Abs delta of DC common mode voltage between D+ and D-			25	mV	
	$V_{TX-Idle-DiffP}$	Electrical idle diff peak output			20	mV	
	$V_{TX-RCV-Detect}$	Voltage change during receiver detection			600	mV	
	$RL_{TX-DIFF}$	Transmitter Differential Return loss	12			dB	
	RL_{TX-CM}	Transmitter Common Mode Return loss	6			dB	
	$Z_{TX-DEFF-DC}$	DC Differential TX impedance	80	100	120	Ω	
	Z_{OSE}	Single ended TX Impedance	40	50	60	Ω	
	Transmitter Eye Diagram	TX Eye Height (De-emphasized bits)	505	650		mV	
	Transmitter Eye Diagram	TX Eye Height (Transition bits)	800	950		mV	
	PCIe Receive						
	$V_{RX-DIFFp-p}$	Differential input voltage (peak-to-peak)	175		1200	mV	
	$V_{RX-CM-AC}$	Receiver common-mode voltage for AC coupling			150	mV	
	$RL_{RX-DIFF}$	Receiver Differential Return Loss	15			dB	
	RL_{RX-CM}	Receiver Common Mode Return Loss	6			dB	
	$Z_{RX-DIFF-DC}$	Differential input impedance (DC)	80	100	120	Ω	
	$Z_{RX-COMM-DC}$	Single-ended input impedance	40	50	60	Ω	
	$Z_{RX-COMM-HIGH-Z-DC}$	Powered down input common mode impedance (DC)	200k	350k		Ω	
	$V_{RX-IDLE-DET-DIFFp-p}$	Electrical idle detect threshold	65		175	mV	
PCIe REFCLK							
	C_{IN}	Input Capacitance	1.5	—		pF	

Table 17 DC Electrical Characteristics (Part 1 of 2)

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I/O Type	Parameter	Description	Min[1]	Typ[1]	Max[1]	Unit	Conditions
Other I/Os							
LOW Drive Output	I_{OL}		—	2.5	—	mA	V_{OL} = 0.4v
	I_{OH}		—	-5.5	—	mA	V_{OH} = 1.5V
High Drive Output	I_{OL}		—	12.0	—	mA	V_{OL} = 0.4v
	I_{OH}		—	-20.0	—	mA	V_{OH} = 1.5V
Schmitt Trigger Input (STI)	V_{IL}		-0.3	—	0.8	V	—
	V_{IH}		2.0	—	V_{DD}IO + 0.5	V	—
Input	V_{IL}		-0.3	—	0.8	V	—
	V_{IH}		2.0	—	V_{DD}IO + 0.5	V	—
Capacitance	C_{IN}		—	—	8.5	pF	—
Leakage	Inputs		—	—	± 10	µA	V_{DD}I/O (max)
	$I/O_{LEAK\ W/O}$ Pull-ups/downs		—	—	± 10	µA	V_{DD}I/O (max)
	$I/O_{LEAK\ WITH}$ Pull-ups/downs		—	—	± 80	µA	V_{DD}I/O (max)

Table 17 DC Electrical Characteristics (Part 2 of 2)

[1] Minimum, Typical, and Maximum values meet the requirements under PCI Specification 1.1.

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Package Pinout — 196-BGA Signal Pinout for PES8T5A

The following table lists the pin numbers and signal names for the PES8T5A device.

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
A1	V_{SS}		C7	V_{DD}APE		E13	V_{DD}CORE		H5	V_{SS}	
A2	PE0RP03		C8	V_{DD}APE		E14	V_{SS}		H6	V_{DD}CORE	
A3	V_{SS}		C9	V_{TT}PE		F1	MSMBDAT		H7	V_{DD}CORE	
A4	PE0TN03		C10	CCLKDS		F2	SSMBADDR_2		H8	V_{SS}	
A5	PE0TP02		C11	V_{SS}		F3	SSMBADDR_5		H9	V_{SS}	
A6	V_{SS}		C12	V_{DD}IO		F4	V_{DD}IO		H10	V_{DD}CORE	
A7	PE0RN02		C13	V_{SS}		F5	V_{SS}		H11	V_{DD}CORE	
A8	PE0RN01		C14	SWMODE_0		F6	V_{DD}CORE		H12	GPIO_05	
A9	V_{SS}		D1	SSMBCLK		F7	V_{DD}CORE		H13	GPIO_03	1
A10	PE0TP01		D2	SSMBDAT		F8	V_{SS}		H14	GPIO_02	
A11	PE0TN00		D3	V_{SS}		F9	V_{DD}CORE		J1	JTAG_TDO	
A12	V_{SS}		D4	V_{DD}IO		F10	V_{DD}CORE		J2	JTAG_TRST_N	
A13	PE0RP00		D5	V_{DD}CORE		F11	V_{DD}IO		J3	JTAG_TMS	
A14	V_{SS}		D6	V_{DD}CORE		F12	GPIO_00	1	J4	V_{DD}CORE	
B1	V_{SS}		D7	V_{DD}PE		F13	PERSTN		J5	V_{SS}	
B2	PE0RN03		D8	V_{DD}PE		F14	V_{SS}		J6	V_{DD}CORE	
B3	V_{SS}		D9	V_{DD}CORE		G1	MSMBADDR_4		J7	V_{SS}	
B4	PE0TP03		D10	V_{DD}IO		G2	MSMBCLK		J8	V_{DD}CORE	
B5	PE0TN02		D11	V_{DD}CORE		G3	V_{DD}IO		J9	V_{DD}CORE	
B6	V_{SS}		D12	V_{SS}		G4	V_{SS}		J10	V_{SS}	
B7	PE0RP02		D13	SWMODE_2		G5	V_{DD}CORE		J11	V_{DD}IO	
B8	PE0RP01		D14	SWMODE_1		G6	V_{SS}		J12	V_{DD}IO	
B9	V_{SS}		E1	SSMBADDR_1		G7	V_{SS}		J13	GPIO_06	
B10	PE0TN01		E2	SSMBADDR_3		G8	V_{DD}CORE		J14	GPIO_04	1
B11	PE0TP00		E3	V_{DD}IO		G9	V_{SS}		K1	JTAG_TDI	
B12	V_{SS}		E4	V_{DD}CORE		G10	V_{SS}		K2	V_{DD}IO	
B13	PE0RN00		E5	V_{SS}		G11	V_{SS}		K3	V_{DD}APE	
B14	V_{SS}		E6	V_{SS}		G12	V_{DD}IO		K4	V_{SS}	
C1	WAKEN		E7	V_{SS}		G13	GPIO_01	1	K5	V_{DD}CORE	
C2	APWRDISN		E8	V_{SS}		G14	RSTHALT		K6	V_{SS}	
C3	CCLKUS		E9	V_{SS}		H1	MSMBADDR_1		K7	V_{SS}	
C4	V_{SS}		E10	V_{DD}CORE		H2	MSMBADDR_2		K8	V_{SS}	
C5	V_{SS}		E11	V_{SS}		H3	MSMBADDR_3		K9	V_{SS}	
C6	V_{TT}PE		E12	V_{DD}IO		H4	V_{DD}CORE		K10	V_{SS}	

Table 18 PES8T5A 196-pin Signal Pin-Out (Part 1 of 2)

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Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
K11	V_{DD}CORE		L12	V_{SS}		M13	MSMBSMODE		N14	PE5RN00	
K12	V_{SS}		L13	GPIO_10	1	M14	V_{SS}		P1	PEREFCLKP	
K13	GPIO_08		L14	GPIO_09	1	N1	PEREFCLKN		P2	V_{SS}	
K14	GPIO_07	1	M1	V_{SS}		N2	V_{SS}		P3	PE2RP00	
L1	JTAG_TCK		M2	V_{DD}CORE		N3	PE2RN00		P4	V_{SS}	
L2	V_{SS}		M3	V_{DD}CORE		N4	V_{SS}		P5	PE2TN00	
L3	V_{SS}		M4	V_{SS}		N5	PE2TP00		P6	PE3TP00	
L4	V_{DD}IO		M5	V_{DD}IO		N6	PE3TN00		P7	V_{SS}	
L5	V_{DD}CORE		M6	V_{TT}PE		N7	V_{SS}		P8	PE3RP00	
L6	V_{DD}CORE		M7	V_{DD}APE		N8	PE3RN00		P9	PE4RN00	
L7	V_{DD}PE		M8	V_{DD}APE		N9	PE4RP00		P10	V_{SS}	
L8	V_{DD}PE		M9	V_{TT}PE		N10	V_{SS}		P11	PE4TP00	
L9	V_{DD}CORE		M10	V_{DD}IO		N11	PE4TN00		P12	PE5TN00	
L10	V_{DD}CORE		M11	V_{DD}IO		N12	PE5TP00		P13	V_{SS}	
L11	V_{SS}		M12	REFCLKM		N13	V_{SS}		P14	PE5RP00	

Table 18 PES8T5A 196-pin Signal Pin-Out (Part 2 of 2)

Alternate Signal Functions

Pin	GPIO	Alternate
F12	GPIO_00	P2RSTN
G13	GPIO_01	P4RSTN
H14	GPIO_02	IOEXPINTN0
H13	GPIO_03	IOEXPINTN1
J14	GPIO_04	IOEXPINTN2
K14	GPIO_07	GPEN
L14	GPIO_09	P3RSTN
L13	GPIO_10	P5RSTN

Table 19 PES8T5A Alternate Signal Functions

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Power Pins

V_{DD}Core	V_{DD}Core	V_{DD}IO	V_{DD}PE	V_{DD}APE	V_{TT}PE
D5	H10	C12	D7	C7	C6
D6	H11	D4	D8	C8	C9
D9	J4	D10	L7	K3	M6
D11	J6	E3	L8	M7	M9
E4	J8	E12		M8	
E10	J9	F4			
E13	K5	F11			
F6	K11	G3			
F7	L5	G12			
F9	L6	J11			
F10	L9	J12			
G5	L10	K2			
G8	M2	L4			
H4	M3	M5			
H6		M10			
H7		M11			

Table 20 PES8T5A Power Pins

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Ground Pins

V_{ss}	V_{ss}	V_{ss}	V_{ss}
A1	D3	G10	L3
A3	D12	G11	L11
A6	E5	H5	L12
A9	E6	H8	M1
A12	E7	H9	M4
A14	E8	J5	M14
B1	E9	J7	N2
B3	E11	J10	N4
B6	E14	K4	N7
B9	F5	K6	N10
B12	F8	K7	N13
B14	F14	K8	P2
C4	G4	K9	P4
C5	G6	K10	P7
C11	G7	K12	P10
C13	G9	L2	P13

Table 21 PES8T5A Ground Pins

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Signals Listed Alphabetically

Signal Name	I/O Type	Location	Signal Category
APWRDISN	I	C2	System
CCLKDS	I	C10	
CCLKUS	I	C3	
GPIO_00	I/O	F12	General Purpose Input/Output
GPIO_01	I/O	G13	
GPIO_02	I/O	H14	
GPIO_03	I/O	H13	
GPIO_04	I/O	J14	
GPIO_05	I/O	H12	
GPIO_06	I/O	J13	
GPIO_07	I/O	K14	
GPIO_08	I/O	K13	
GPIO_09	I/O	L14	
GPIO_10	I/O	L13	
JTAG_TCK	I	L1	JTAG
JTAG_TDI	I	K1	
JTAG_TDO	O	J1	
JTAG_TMS	I	J3	
JTAG_TRST_N	I	J2	
MSMBADDR_1	I	H1	SMBus
MSMBADDR_2	I	H2	
MSMBADDR_3	I	H3	
MSMBADDR_4	I	G1	
MSMBCLK	I/O	G2	
MSMBDAT	I/O	F1	
MSMBSMODE	I	M13	System
PE0RN00	I	B13	PCI Express
PE0RN01	I	A8	
PE0RN02	I	A7	
PE0RN03	I	B2	
PE0RP00	I	A13	
PE0RP01	I	B8	
PE0RP02	I	B7	
PE0RP03	I	A2	

Table 22 PES8T5A Alphabetical Signal List (Part 1 of 3)

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Signal Name	I/O Type	Location	Signal Category
PE0TN00	O	A11	PCI Express (cont.)
PE0TN01	O	B10	
PE0TN02	O	B5	
PE0TN03	O	A4	
PE0TP00	O	B11	
PE0TP01	O	A10	
PE0TP02	O	A5	
PE0TP03	O	B4	
PE2RN00	I	N3	
PE2RP00	I	P3	
PE2TN00	O	P5	
PE2TP00	O	N5	
PE3RN00	I	N8	
PE3RP00	I	P8	
PE3TN00	O	N6	
PE3TP00	O	P6	
PE4RN00	I	P9	
PE4RP00	I	N9	
PE4TN00	O	N11	
PE4TP00	O	P11	
PE5RN00	I	N14	
PE5RP00	I	P14	
PE5TN00	O	P12	
PE5TP00	O	N12	
PEREFCLKN	I	N1	
PEREFCLKP	I	P1	
PERSTN	I	F13	System
REFCLKM	I	M12	PCI Express
RSTHALT	I	G14	System
SSMBADDR_1	I	E1	SMBus
SSMBADDR_2	I	F2	
SSMBADDR_3	I	E2	
SSMBADDR_5	I	F3	
SSMBCLK	I/O	D1	SMBus
SSMBDAT	I/O	D2	

Table 22 PES8T5A Alphabetical Signal List (Part 2 of 3)

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Signal Name	I/O Type	Location	Signal Category
SWMODE_0	I	C14	System
SWMODE_1	I	D14	
SWMODE_2	I	D13	
WAKEN	I/O	C1	
V_{DD}CORE, V_{DD}APE, V_{DD}IO, V_{DD}PE, V_{TT}PE	See Table 20 for a listing of power pins.		
V_{SS}	See Table 21 for a listing of ground pins.		

Table 22 PES8T5A Alphabetical Signal List (Part 3 of 3)

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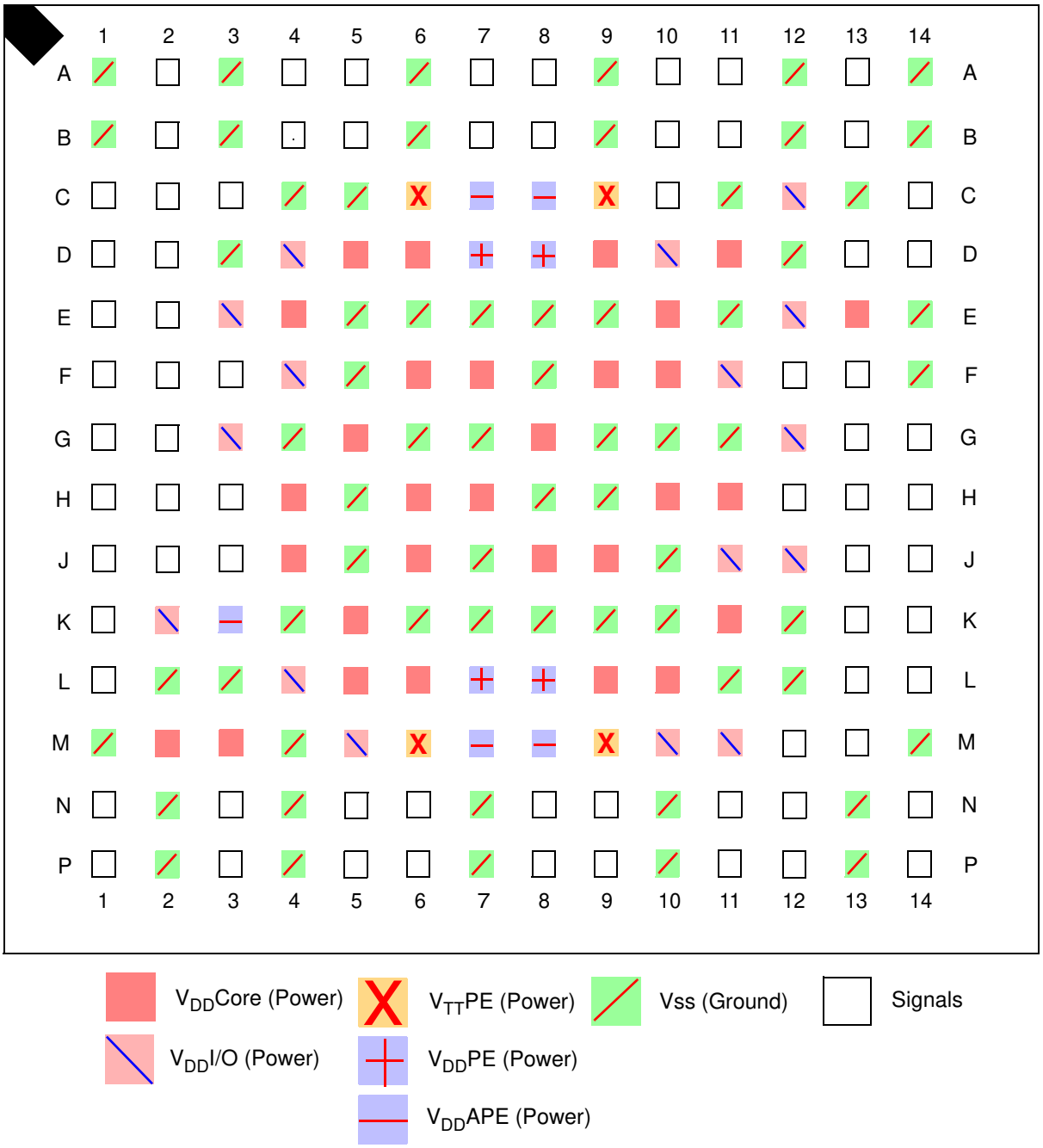
PES8T5A Pinout — Top View



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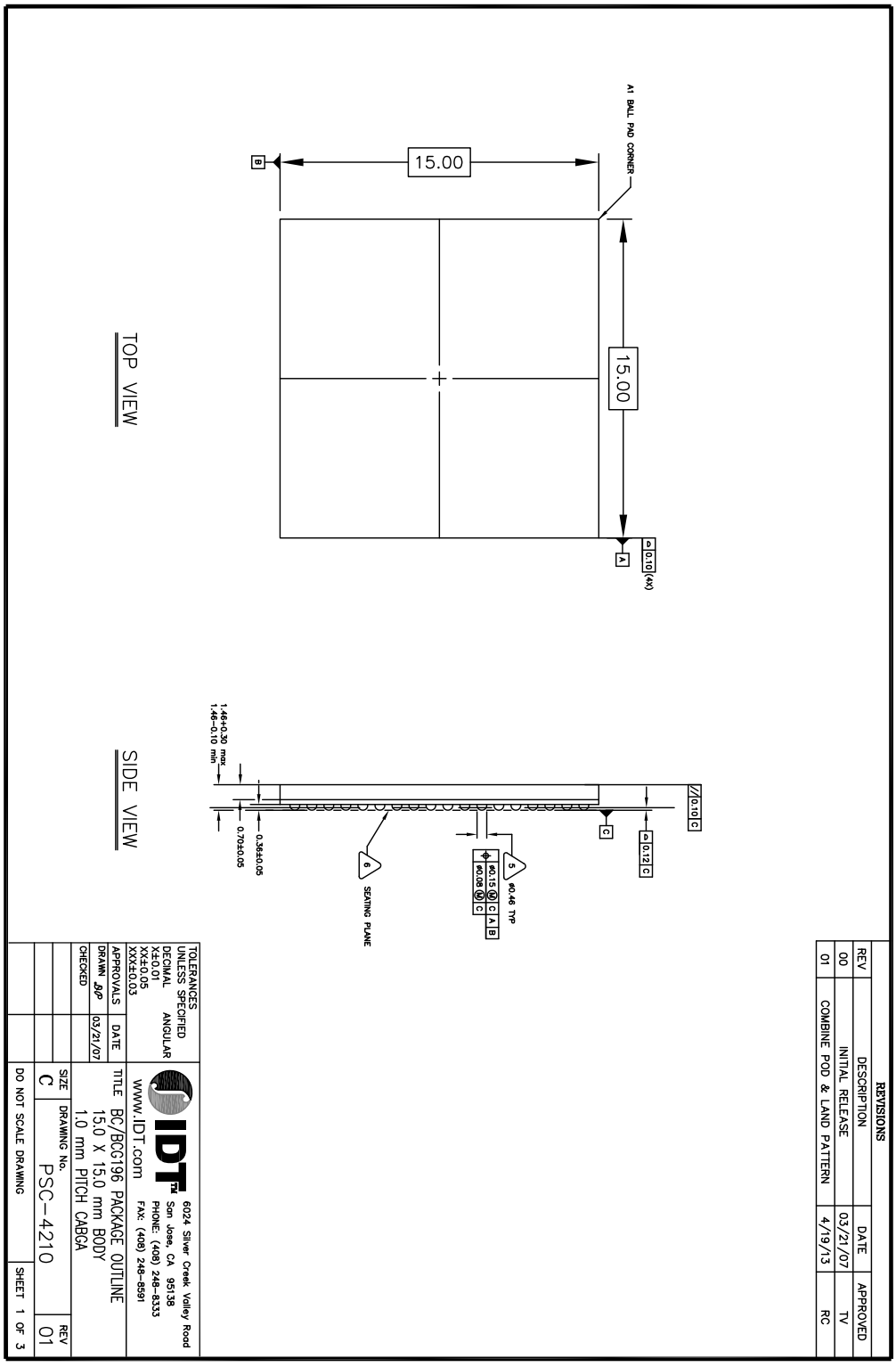
PES8T5A Package Drawing — 196-Pin BC196/BCG196



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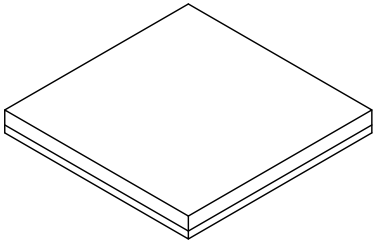
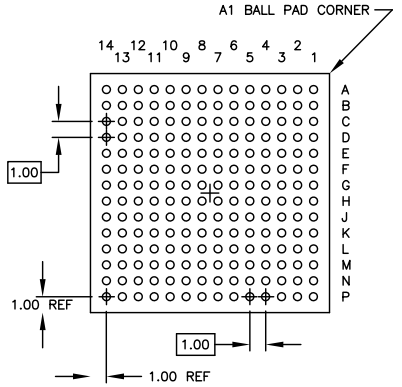
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	03/21/07	TV
01	COMBINE POD & LAND PATTERN	4/19/13	RC





BOTTOM VIEW
196 SOLDER BALLS

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994.
2. THE BASIC SOLDER BALL GRID PITCH IS 1.00mm.
3. THE MAXIMUM SOLDER BALL MATRIX SIZE IS 14 X 14.
4. THE MAXIMUM ALLOWABLE NUMBER OF SOLDER BALLS IS 196.
5. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
6. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
7. "A1" ID CORNER MUST BE IDENTIFIED. IDENTIFICATION MAY BE BY MEANS OF CHAMFER, METALLIZED OR INK MARK, INDENTATION OR OTHER FEATURE OF THE PACKAGE BODY.
8. THIS DRAWING CONFORMS TO THE JEDEC REGISTERED OUTLINE MS–034/A, VARIATION AAG–1 EXCEPT FOR A1, b, AND aaa DIMENSIONS.

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR X± XX± XXX±		IDT™ www.IDT.com	6024 Silver Creek Valley Road San Jose, CA 95138 PHONE: (408) 248–8333 FAX: (408) 248–8591
APPROVALS	DATE	TITLE	BC/BCG 196 PACKAGE OUTLINE 15.0 x 15.0 mm BODY 1.0 mm PITCH CABGA
DRAWN BJP	03/21/07		
CHECKED			
		SIZE C	DRAWING No. PSC–4210 REV 01
		DO NOT SCALE DRAWING	SHEET 2 OF 3

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Revision History

March 31, 2008: Publication of final data sheet.

August 6, 2008: Added industrial temperature information to Tables 14 and 16 and to Ordering Information section.

May 7, 2009: Revised labels in Table 15, Power Consumption, for greater clarification.

June 18, 2014: Changed the height dimension for the side view in PES8T5A Package Drawing — 196-Pin BC196/BCG196 to match the package's characteristics.

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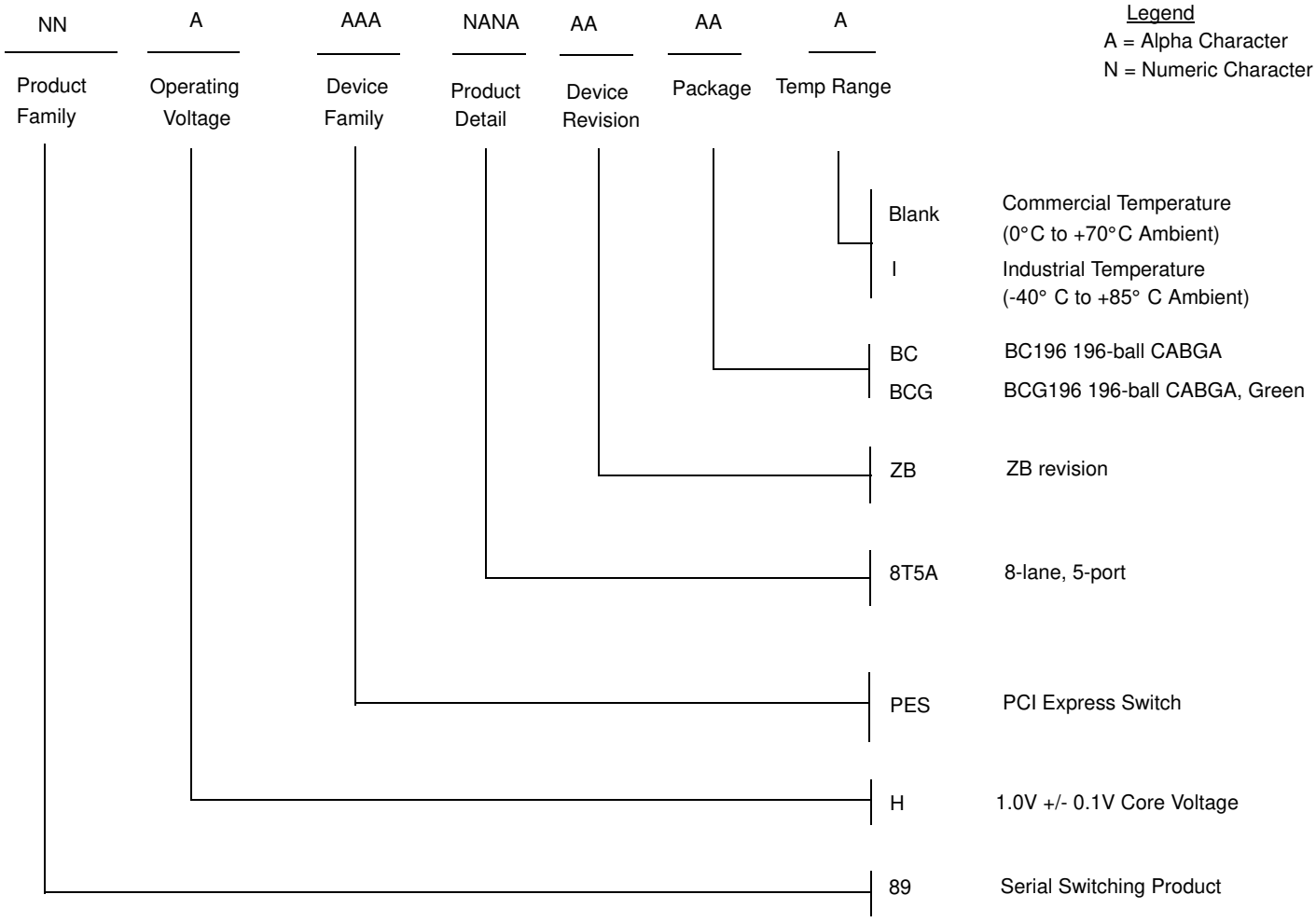
Ordering Information



Valid Combinations

89HPES8T5AZBBC	196-pin BC196 package, Commercial Temperature
89HPES8T5AZBBCG	196-pin Green BCG196 package, Commercial Temperature
89HPES8T5AZBBCI	196-pin BC196 package, Industrial Temperature
89HPES8T5AZBBCGI	196-pin Green BCG196 package, Industrial Temperature

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