# USER CONFIGURABLE CLOCK 525-01/02

## Description

The ICS525-01/02 are the most flexible way to generate a high-quality, high-accuracy, high-frequency clock output from an inexpensive crystal or clock input. The user can configure the device to produce nearly any output frequency from any input frequency by grounding or floating the select pins. Neither microcontroller, software, nor device programmer are needed to set the frequency. Using Phase-Locked Loop (PLL) techniques, the device accepts a standard fundamental mode, inexpensive crystal to produce output clocks up to 250MHz. It can also produce a highly accurate output clock from a given input clock, keeping them frequency locked together.

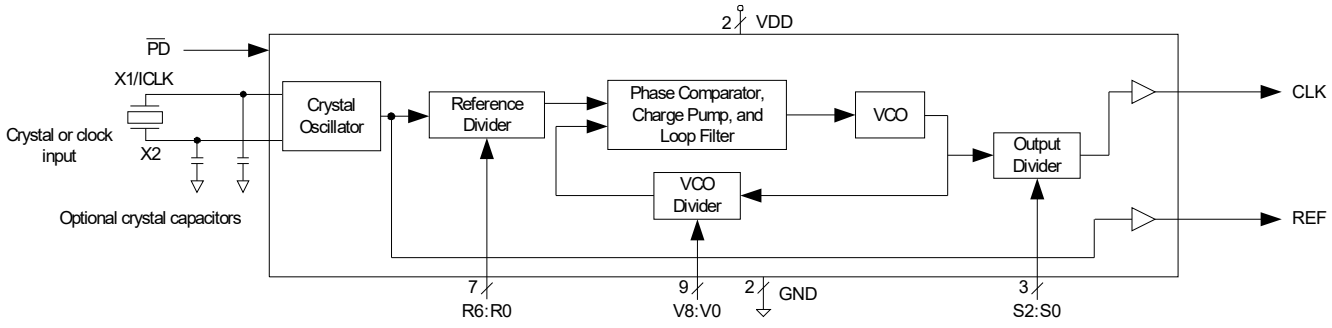
For similar capability with a serial interface, use the 307. For simple multipliers to produce common frequencies, refer to the 50x family of parts, which are smaller and more cost effective.

These products are intended for clock generation. They have low output jitter (variation in the output period), but input to output skew and jitter are not defined nor guaranteed. For applications which require defined input to output timing, use the 527-01.

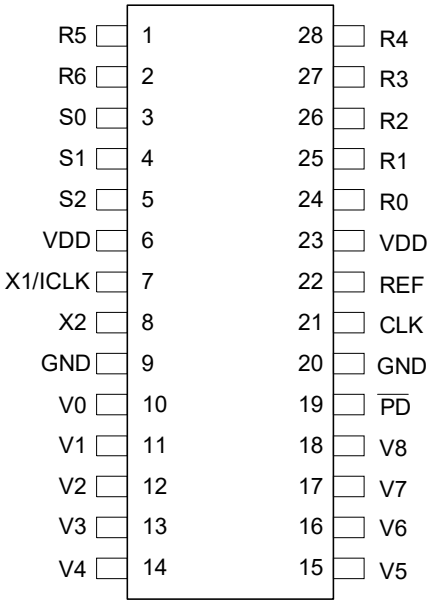
## Features

- Packaged in 28-pin SSOP (150 mil body) or 28-pin VFQFPN (4x4mm body)
- Industrial and commercial versions available in Pb (lead) free package
- User determines the output frequency by setting all internal dividers
- Eliminates need for custom oscillators
- No software needed
- Online calculator determines register settings
- Pull-ups on all select inputs
- Input crystal frequency of 5 – 27 MHz
- Input clock frequency of 2 – 50 MHz
- Very low jitter
- Duty cycle of 45/55 up to 200MHz
- Operating voltage of 3.0V or 5.5V
- Ideal for oscillator replacement
- Industrial temperature version available
- For Zero Delay, refer to the 527

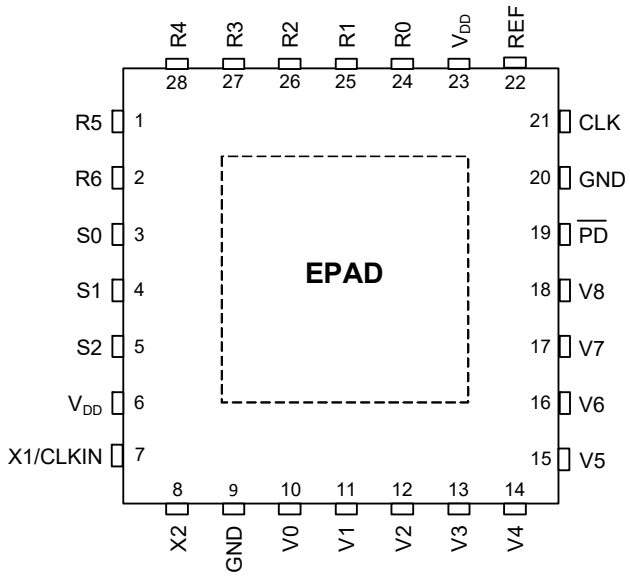
## Block Diagram



## Pin Assignments




**28-pin SSOP**




**28-pin VFQFPN**

## Pin Descriptions

| Pin Number | Pin Name | Pin Type | Pin Description |
|---|---|---|---|
| 1, 2, 24-28 | R5, R6, R0-R4 | I(PU) | Reference divider word input pins determined by user. Forms a binary number from 0 to 127. |
| 3, 4, 5 | S0, S1, S2 | I(PU) | Select pins for output divider determined by user. See table on page 3. |
| 6, 23 | VDD | Power | Connect to VDD. |
| 7 | X1/ICLK | X1 | Crystal connection. Connect to a parallel resonant fundamental crystal or input clock. |
| 8 | X2 | X2 | Crystal connection. Connect to a crystal or leave unconnected for clock. |
| 9, 20 | GND | Power | Connect to ground. |
| 10 - 18 | V0 - V8 | I(PU) | VCO divider word input pins determined by user. Forms a binary number from 0 to 511. |
| 19 | $\overline{PD}$ | Input | Power-down. Active low. Turns off entire chip when low. Clock outputs tri-stated. |
| 21 | CLK | Output | Output clock determined by status of R0-R6, V-V8, S0-S2, and input frequency. |
| 22 | REF | Output | Reference output. Buffered crystal oscillator (or clock ) output. |

KEY: I(PU) = Input with internal pull-up resistor; X1, X2 = crystal connections

## 525-01 Output Frequency and Output Divider Table

| S2 Pin 5 | S1 Pin 4 | S0 Pin 3 | CLK Output Divider | Output Frequency Range (MHz) | | | |
|---|---|---|---|---|---|---|---|
| | | | | VDD = 5 V | | VDD = 3.3 V | |
| | | | | 0 - 70°C | -40 to +85°C | 0 - 70°C | -40 to +85°C |
| 0 | 0 | 0 | 10 | 3–26 | 3–23 | 3–18 | 3–16 |
| 0 | 0 | 1 | 2 | 15–160 | 15–140 | 15–100 | 15–90 |
| 0 | 1 | 0 | 8 | 3.75–40 | 3.75–36 | 3.75–25 | 3.75–22 |
| 0 | 1 | 1 | 4 | 7.5–80 | 7.5–72 | 7.5–50 | 7.5–45 |
| 1 | 0 | 0 | 5 | 6–50 | 6–45 | 6–34 | 6–30 |
| 1 | 0 | 1 | 7 | 4–40 | 4–36 | 4–26 | 4–23 |
| 1 | 1 | 0 | 9 | 3.3–33.3 | 3.3–30 | 3.3–20 | 3.3–18 |
| 1 | 1 | 1 | 6 | 5–53 | 5–47 | 5–27 | 5–24 |

## 525-02 Output Frequency and Output Divider Table

| S2 Pin 5 | S1 Pin 4 | S0 Pin 3 | CLK Output Divider | Output Frequency Range (MHz) | |
|---|---|---|---|---|---|
| | | | | VDD = 5 V | VDD = 3.3 V |
| | | | | -40 to +85°C | -40 to +85°C |
| 0 | 0 | 0 | 6 | 5–67 | 5–40 |
| 0 | 0 | 1 | 2 | 15–200 | 15–120 |
| 0 | 1 | 0 | 8 | 3.75–50 | 3.75–30 |
| 0 | 1 | 1 | 4 | 7.5–100 | 7.5–60 |
| 1 | 0 | 0 | 5 | 6–80 | 6–48 |
| 1 | 0 | 1 | 7 | 4–57 | 4–34 |
| 1 | 1 | 0 | 1 | 30–250 | 30–200 |
| 1 | 1 | 1 | 3 | 10–133 | 10–80 |

# External Components/Crystal Selection

## Decoupling Capacitors

The ICS525-01/02 requries two 0.01µF decoupling capacitors to be connected between VDD and GND, one on each side of the chip. The capacitor must be connected close to the device to minimize lead inductance.

## External Resistors

A 33Ω series termination resistor should be used on the CLK and REF pins.

## Crystal Load Capacitors

The approximate total on-chip capacitance for a crystal is 16 pF, so a parallel resonant, fundamental mode crystal with this value of load (correlation) capacitance should be used. For crystals with a specified load capacitance greater than 16 pF, crystal capacitors may be connected from each of the pins X1 and X2 to Ground as shown in the block diagram. The value (in pF) of these crystal caps should be (CL -16)*2, where CL is the crystal load capacitance in pF. These external capacitors are only required for applications where the exact frequency is critical. For a clock input, connect to X1 and leave X2 unconnected (no capacitors on either).

## Determining the Output Frequency

Users have full control in setting the desired output frequency over the range shown in the tables on pages 3-4. To replace a standard oscillator, users should connect the divider select input pins directly to ground (or VDD, although this is not required because of internal pull-ups) during Printed Circuit Board layout. The 525 will automatically produce the correct frequency when all components are soldered. It is also possible to connect the inputs to parallel I/O ports to switch frequencies. By choosing divides carefully, the number of inputs which need to be changed can be minimized. Observe the restrictions on allowed values of VDW and RDW.

## Configuration Pin Settings

The output of the 525 can be determined by the following simple equation:

$$\text{CLK Frequency} = \text{Input Frequency} \times 2x\frac{(VDW + 8)}{(RDW + 2) \bullet OD}$$

Where:

Reference Divider Word (RDW) = 0 to 127 (0 not permitted for 525-01)

VCO Divider Word (VDW) = 0 to 511 (0, 1, 2, 3 not permitted for 525-01)

Output Divider (OD) = values on pages 3-4

Also, the following operating ranges should be observed:

1. The output frequency must be in the ranges listed on pages 3-4.

2. The phase detector frequency must be above 200 kHz.

$$200\text{kHz} < \frac{\text{InputFrequency}}{(RDW + 2)}$$

Since all of the inputs have pull-up resistors, it is only necessary to ground the pins that need to be set to zero.

## Which Part to Use?

The 525-01 is the original configurable clock.

The 525-02 has a higher maximum output frequency and a slightly different set of output dividers.

To determine the best combination of VCO, reference, and output divide, use the Calculator on our web site.

## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS525-01/02. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item | Rating |
|---|---|
| Supply Voltage, VDD | 7 V |
| All Inputs and Outputs | -0.5 V to VDD+0.5 V |
| Ambient Operating Temperature, Commercial | 0 to +70°C |
| Ambient Operating Temperature, Industrial | -40 to +85°C |
| Storage Temperature | -65°C to 150°C |
| Junction Temperature | 125°C |
| Soldering Temperature | 260°C (max. of 10 seconds) |

## DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V**

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Operating Voltage | VDD | | 3.0 | | 5.5 | V |
| Operating Supply Current | IDD | 60 MHz out, no load, 15 MHz crystal, 525-01/02 only | | 8 | | mA |
| Operating Supply Current, Power-down | IDD | Pin 19 = 0, Note 1 | | 4 | | µA |
| Input High Voltage | $V_{IH}$ | | 2 | | | V |
| Input Low Voltage | $V_{IL}$ | | | | 0.8 | V |
| Input High Voltage, X1/ICLK only | $V_{IH}$ | ICLK (pin7) | VDD/2+1 | VDD/2 | | V |
| Input Low Voltage, X1/ICLK only | $V_{IL}$ | ICLK (pin7) | | VDD/2 | VDD/2-1 | V |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -12 mA | VDD-0.4 | | | V |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 12 mA | | | 0.4 | V |
| Short Circuit Current | | CLK and REF outputs | | ±55 | | mA |
| Input Capacitance | $C_{IN}$ | V, R, S pins and pin 19 | | 4 | | pF |
| On-chip Pull-up Resistor | $R_{PU}$ | V, R, S pins and pin 19 | | 270 | | kΩ |

## AC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V**

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Input Frequency | $F_{IN}$ | Crystal input | 5 | | 27 | MHz |
| | | Clock input | 2 | | 50 | MHz |
| Output Clock Rise Time | | 0.8 to 2.0 V | | 1 | | ns |
| Output Clock Fall Time | | 2.0 to 0.8 V | | 1 | | ns |
| Output Clock Duty Cycle, OD = 2, 4, 6, 8, or 10 | | At VDD/2 | 45 | 49 to 51 | 55 | % |
| Output Clock Duty Cycle, OD = 3, 5, 7, or 9 | | At VDD/2 | 40 | | 60 | % |
| Output Clock Duty Cycle, OD = 1 (-02 only) | | At VDD/2 | 35 | | 65 | |
| Power-down Time, PD low to clocks stopped | | | | | 50 | ns |
| Power-up Time, PD high to clocks stable | | | | | 10 | ms |
| Absolute Clock Period Jitter, 525-01, Note 2 | $t_{ja}$ | Deviation from mean | | ±140 | | ps |
| One Sigma Clock Period Jitter, 525-01, Note 2 | $t_{js}$ | One Sigma | | 45 | | ps |
| Absolute Clock Period Jitter, 525-02, Note 2 | $t_{ja}$ | Deviation from mean | | ±85 | | ps |
| One Sigma Clock Period Jitter, 525-02, Note 2 | $t_{js}$ | One Sigma | | 30 | | ps |

NOTE 1: Phase relationship between input and output can change at power-up. For a fixed phase relationship, see the 527.

NOTE 2: For 16 MHz, 100 MHz output. Use the -02 for lowest jitter.

## Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see Ordering Information for POD links). The package information is the most current data available and is subject to change without revision of this document.

## Ordering Information

| Part / Order Number | Marking | Shipping Packaging | Package | Temperature |
|---|---|---|---|---|
| 525-01RLF | ICS525-01RLF | Tubes | 28-pin SSOP | 0 to +70°C |
| 525-01RLFT | ICS525-01RLF | Tape and Reel | 28-pin SSOP | 0 to +70°C |
| 525-01RILF | ICS525-01RILF | Tubes | 28-pin SSOP | -40 to +85°C |
| 525-01RILFT | ICS525-01RILF | Tape and Reel | 28-pin SSOP | -40 to +85°C |
| 525R-02LF | ICS525R-02LF | Tubes | 28-pin SSOP | 0 to +70°C |
| 525R-02LFT | ICS525R-02LF | Tape and Reel | 28-pin SSOP | 0 to +70°C |
| 525R-02ILF | ICS525R-02ILF | Tubes | 28-pin SSOP | -40 to +85°C |
| 525R-02ILFT | ICS525R-02ILF | Tape and Reel | 28-pin SSOP | -40 to +85°C |
| 525NQG-01 | 525NQG-01 | Tubes | 28-pin VFQFPN | 0 to +70°C |
| 525NQG-01T | 525NQG-01 | Tape and Reel | 28-pin VFQFPN | 0 to +70°C |
| 525NQG-01I | 525NQG-01I | Tubes | 28-pin VFQFPN | -40 to +85°C |
| 525NQG-01IT | 525NQG-01I | Tape and Reel | 28-pin VFQFPN | -40 to +85°C |
| 525NQG-02 | 525NQG-02 | Tubes | 28-pin VFQFPN | 0 to +70°C |
| 525NQG-02T | 525NQG-02 | Tape and Reel | 28-pin VFQFPN | 0 to +70°C |
| 525NQG-02I | 525NQG-02I | Tubes | 28-pin VFQFPN | -40 to +85°C |
| 525NQG-02IT | 525NQG-02I | Tape and Reel | 28-pin VFQFPN | -40 to +85°C |

## Revision History

Rev. March 30, 2015
1. removed -11 and -12 references/parts from datasheet. The devices are obsolete.
2. Added VFQFPN packaging note to Features.
3. Updated POD with latest drawing
4. Updated Ordering Information.

Rev. August 23, 2021
1. Rebranded to Renesas.
2. Updated “Which Part to Use?” section to include updated link to calculators page.
3. Updated Package Outline Drawings section and Ordering Information table.

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