Description

The 5PB12xx is a high-performance TCXO/LVCMOS clock fanout buffer family with individual OE pin for each output. The CLKIN pin can accept either a square wave (LVCMOS) or clipped sine wave (such as TCXO clipped sine wave output) as input.

There are 3 different fan-out versions available: 1:3, 1:4 and 1:6.

The 5PB12xx has industry-leading low jitter and extremely low current consumption, making it ideal for smart mobile devices.

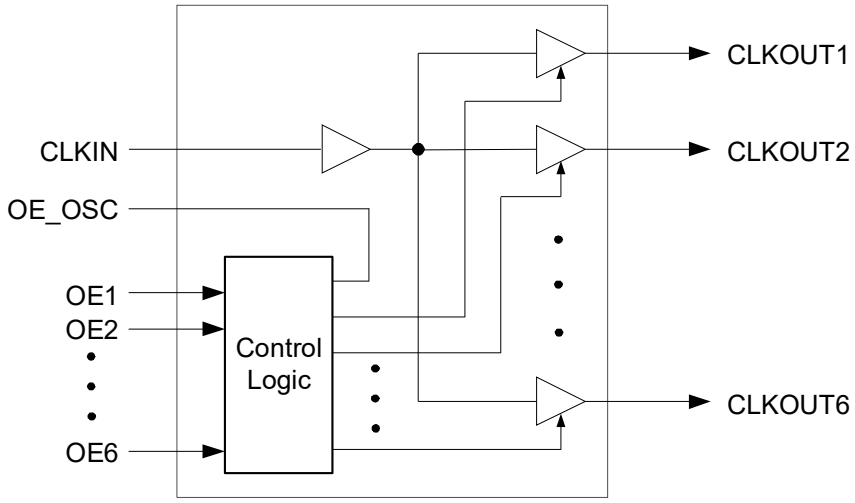
Typical Applications

- Smart Mobile Handsets
- RF and baseband peripheral clock distribution
- Automotive

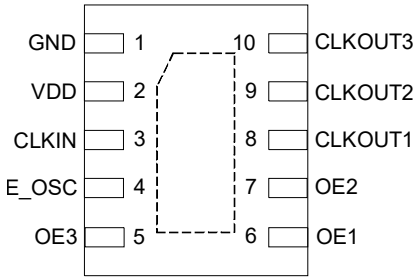
Features

- Extremely low operating and standby current consumption
- Low RMS additive phase jitter
- Family supports 1.8V to 3.3V power supply voltage:
  - For 1.8V supply: 5PB1203, 5PB1204, 5PB1206
  - For 2.5V / 3.3V supply: 5PB1213, 5PB1214, 5PB1216
- Three, four, and six outputs with individual Output Enable pin
- One input
- OE_OSC control pin to enable/disable reference TCXO/XO
- Small 10-pin, 16-pin and 20-pin packages available
- Industrial -40º to +105ºC temperature range

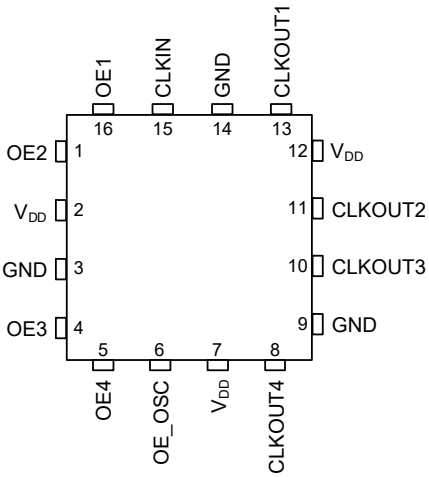
Block Diagram



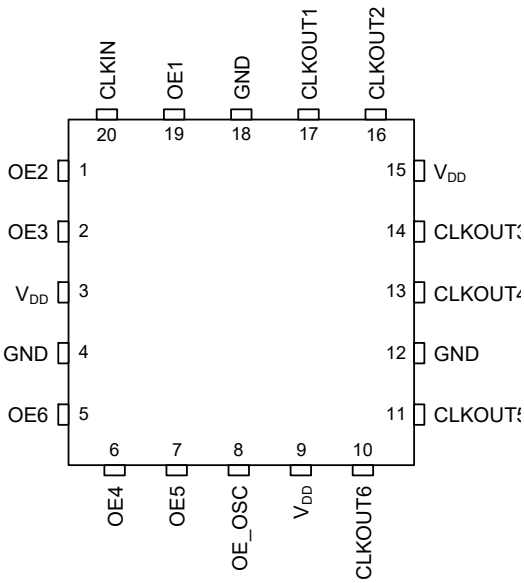
Pin Assignments



5PB1203 / 5PB1213
10-pin 2mm x 2mm DFN



5PB1204 / 5PB1214
16-pin, 2.5mm x 2.5mm VFQFPN



5PB1206 / 5PB1216
20-pin, 3mm x 3mm VFQFPN

Pin Descriptions

Pin Name	Pin Number			Pin Type	Pin Description
	5PB1203 5PB1213	5PB1204 5PB1214	5PB1206 5PB1216		
VDD	2	2, 7, 12	3, 9, 15	Power	Connect 1.8V to 5PB1203/5PB1204/5PB1206. Connect 2.5V or 3.3V to 5PB1213/5PB1214/5PB1216.
GND	1	3, 9, 14	4, 12, 18	Power	Power supply ground.
CLKIN	3	15	20	Input	Single-ended clock input. Typically connected to a single-ended clock output.
OE_OSC	4	6	8	Output	Status pin to indicate that all OE pins are low (all outputs disabled). This pin may be used to disable an external oscillator when all outputs are disabled. Refer to Enable Function Truth Table for additional details. 0 = All OE pins indicate disabled (off) 1 = At least one OE pin indicates enabled (on)
OE1	6	16	19	Input	Output Enable pin for CLKOUT1. Active High. Internal 120kΩ pull-down.
OE2	7	1	1	Input	Output Enable pin for CLKOUT2. Active High. Internal 120kΩ pull-down.
OE3	5	4	2	Input	Output Enable pin for CLKOUT3. Active High. Internal 120kΩ pull-down.
OE4	—	5	6	Input	Output Enable pin for CLKOUT4. Active High. Internal 120kΩ pull-down.
OE5	—	—	7	Input	Output Enable pin for CLKOUT5. Active High. Internal 120kΩ pull-down.
OE6	—	—	5	Input	Output Enable pin for CLKOUT6. Active High. Internal 120kΩ pull-down.
CLKOUT1	8	13	17	Output	Clock Output 1. Same frequency as CLKIN.
CLKOUT2	9	11	16	Output	Clock Output 2. Same frequency as CLKIN.
CLKOUT3	10	10	14	Output	Clock Output 3. Same frequency as CLKIN.
CLKOUT4	—	8	13	Output	Clock Output 4. Same frequency as CLKIN.
CLKOUT5	—	—	11	Output	Clock Output 5. Same frequency as CLKIN.
CLKOUT6	—	—	10	Output	Clock Output 6. Same frequency as CLKIN.

©2026 Renesas Electronics Corporation

Enable Function Truth Table

Input						Output						
OE1	OE2	OE3	OE4	OE5	OE6	OE_OSC	CLKOUT1	CLKOUT2	CLKOUT3	CLKOUT4	CLKOUT5	CLKOUT6
0	0	0	0	0	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
1	0	0	0	0	0	1	CLOCK	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
1	1	0	0	0	0	1	CLOCK	CLOCK	Hi-Z	Hi-Z	Hi-Z	Hi-Z
…	…	…	…	…	…	…	…	…	…	…	…	…
1	1	1	1	1	1	1	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK

External Components

A minimum number of external components are required for proper operation. A 0.01µF bypass capacitor should be used on each VDD pin. Use a separate ground via to the board ground plane for the capacitor. Use a separate ground via for each GND pin. Do not share the ground via. Route power from the via to the VDD plane through the bypass capacitor and then to the VDD pin. A 33Ω series termination resistor should be used on each clock output pin.

To achieve the low output skew that the 5PB12xx is capable of, careful attention must be paid to board layout. Essentially, all four outputs must have identical terminations, identical loads and identical trace geometries. If they do not, the output skew will be degraded. For example, using a 30Ω series termination on one output (with 33Ω on the others) will cause at least 15ps of skew.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 5PB12xx. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	3.8V
Output Enable and All Inputs/Outputs	-0.5 V to VDD + 0.5 V
Ambient Operating Temperature (extended)	-40 to +105°C
Storage Temperature	-65 to +150°C
Junction Temperature	125°C
Soldering Temperature	260°C

DC Electrical Characteristics

(VDD = 1.8V, 2.5V, 3.3V)

VDD = 1.8V ±5%, for **5PB1203 / 1204 / 1206**, ambient temperature -40° to +105°C, unless stated otherwise.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		1.71		1.89	V
Input High Voltage, CLKIN	V_{IH}	LVCMOS input. Note 1	VDD/2 + 200		VDD	mV
Input Low Voltage, CLKIN	V_{IL}	LVCMOS input. Note 1			VDD/2 - 200	mV
Input High Voltage, OE	V_{IH}		0.7xVDD		VDD	V
Input Low Voltage, OE	V_{IL}				0.3xVDD	V
Output High Voltage	V_{OH}	I_{OH} = -4mA	0.8xVDD			V
Output Low Voltage	V_{OL}	I_{OL} = 4mA			0.2xVDD	V
Nominal Output Impedance	Z_O			17		Ω
Input Capacitance	C_{IN}			5		pF
Operating Supply Current						
5PB1203	IDD	CLKIN = 26MHz, all outputs enabled		4.76	5.91	mA
		CLKIN = Low or High, all outputs disabled		0.01	0.01	
5PB1204		CLKIN = 26MHz, all outputs enabled		5.99	7.22	
		CLKIN = Low or High, all outputs disabled		0.01	0.01	
5PB1206		CLKIN = 26MHz, all outputs enabled		9.15	11.39	
		CLKIN = Low or High, all outputs disabled		0.01	0.01	

VDD = 2.5V ±5%, for **5PB1213 / 1214 / 1216**, ambient temperature -40° to +105°C, unless stated otherwise.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		2.375		2.625	V
Input High Voltage, CLKIN	V_{IH}	LVCMOS input. Note 1	VDD/2 + 200		VDD	mV
Input Low Voltage, CLKIN	V_{IL}	LVCMOS input. Note 1			VDD/2 - 200	mV
Input High Voltage, OE	V_{IH}		0.7xVDD		VDD	V
Input Low Voltage, OE	V_{IL}				0.3xVDD	V
Output High Voltage	V_{OH}	I_{OH} = -4mA	0.8xVDD			V
Output Low Voltage	V_{OL}	I_{OL} = 4mA			0.2xVDD	V
Nominal Output Impedance	Z_O			17		Ω
Input Capacitance	C_{IN}	ICLK, OE pin		5		pF
Operating Supply Current						
5PB1213	IDD	CLKIN = 26MHz, all outputs enabled		6.66	8.54	mA
		CLKIN = Low or High, all outputs disabled		0.01	0.02	
5PB1214		CLKIN = 26MHz, all outputs enabled		8.36	10.48	
		CLKIN = Low or High, all outputs disabled		0.01	0.03	
5PB1216		CLKIN = 26MHz, all outputs enabled		12.58	16.30	
		CLKIN = Low or High, all outputs disabled		0.01	0.04	

VDD = 3.3V ±5%, for **5PB1213 / 1214 / 1216**, ambient temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.135		3.465	V
Input High Voltage, CLKIN	V_{IH}	LVCMOS input. Note 1	VDD/2 + 200		VDD	mV
Input Low Voltage, CLKIN	V_{IL}	LVCMOS input. Note 1			VDD/2 - 200	mV
Input High Voltage, OE	V_{IH}		0.7xVDD		VDD	V
Input Low Voltage, OE	V_{IL}				0.3xVDD	V
Output High Voltage	V_{OH}	I_{OH} = -4mA	0.8xVDD			V
Output Low Voltage	V_{OL}	I_{OL} = 4mA			0.2xVDD	V
Nominal Output Impedance	Z_O			17		Ω
Input Capacitance	C_{IN}	ICLK, OE pin		5		pF
Operating Supply Current						
5PB1213	IDD	CLKIN = 26MHz, all outputs enabled		8.96	11.65	mA
		CLKIN = Low or High, all outputs disabled		0.14	0.45	
5PB1214		CLKIN = 26MHz, all outputs enabled		11.34	14.06	
		CLKIN = Low or High, all outputs disabled		0.20	0.63	
5PB1216		CLKIN = 26MHz, all outputs enabled		16.87	21.72	
		CLKIN = Low or High, all outputs disabled		0.22	0.70	

Notes: 1. Nominal switching threshold is VDD/2.

AC Electrical Characteristics

(VDD = 1.8V, 2.5V, 3.3V)

VDD = 1.8V ±5%; for **5PB1203 / 1204 / 1206**, ambient Temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency			0		200	MHz
Output Rise Time	t_{OR}	0.36 to 1.44V, C_L = 5pF		0.6	1.0	ns
Output Fall Time	t_{OF}	1.44 to 0.36V, C_L = 5pF		0.6	1.0	ns
Propagation Delay	Note 1	Note 1	1.5	2.0	2.5	ns
Buffer Additive Phase Jitter, RMS		26MHz TCXO clipped sine wave input, Integration Range: 12kHz to 20MHz		420		fs
		125MHz LVCMOS input, Integration Range: 12kHz to 20MHz		42		fs
Output to Output Skew	$t_{SKEWO-O}$	Note 2, Rising edges at VDD/2		20	50	ps
Device to Device Skew	$t_{SKEWD-D}$	Rising edges at VDD/2			200	ps
Output Enable/Disable time (OEx to CLKOUTx driven/Hi-Z)	t_{EN}/t_{DIS}	CL < 5pF			5.5	ns
Start-up Time	$t_{START-UP}$				2	ms
TCXO Clock Clipped Sine Wave Input Voltage Swing Level	VIN_{pp}	VDD = 1.8V, should connect to CLKIN through AC coupling and bias circuit		0.8		V

VDD = 2.5V ±5%; for **5PB1213 / 1214 / 1216**, ambient Temperature -40° to +105°C, unless stated otherwise

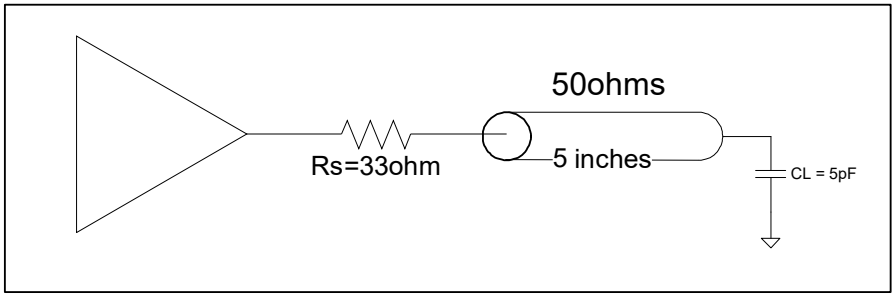
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency			0		200	MHz
Output Rise Time	t_{OR}	0.5 to 2.0V, C_L = 5pF		0.6	1.0	ns
Output Fall Time	t_{OF}	2.0 to 0.5V, C_L = 5pF		0.6	1.0	ns
Propagation Delay	Note 1	Note 1	1.7	2.2	2.7	ns
Buffer Additive Phase Jitter, RMS		26MHz TCXO clipped sine wave input, Integration Range: 12kHz to 20MHz		280		fs
		125MHz LVCMOS input, Integration Range: 12kHz to 20MHz		30		fs
Output to Output Skew	$t_{SKEWO-O}$	Note 2, Rising edges at VDD/2		20	50	ps
Device to Device Skew	$t_{SKEWD-D}$	Rising edges at VDD/2			200	ps
Output Enable/Disable time (OEx to CLKOUTx driven/Hi-Z)	t_{EN}/t_{DIS}	CL < 5pF			3.8	ns
Start-up Time	$t_{START-UP}$	Part start-up time for valid outputs after VDD ramp-up			2	ms
TCXO Clock Clipped Sine Wave Input Voltage Swing Level	VIN_{pp}	VDD = 2.5V, should connect to CLKIN through AC coupling and bias circuit		0.8		V

VDD = 3.3V ±5%; for **5PB1213 / 1214 / 1216**, ambient Temperature -40° to +105°C, unless stated otherwise

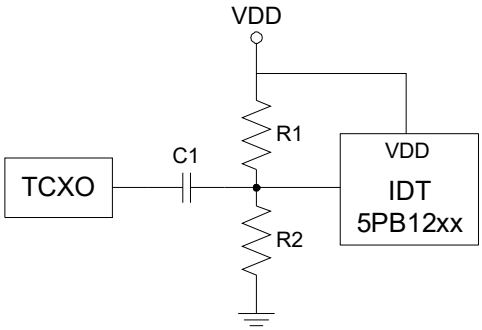
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency			0		200	MHz
Output Rise Time	t_{OR}	0.66 to 2.64V, C_L = 5pF		0.6	1.0	ns
Output Fall Time	t_{OF}	2.64 to 0.66V, C_L = 5pF		0.6	1.0	ns
Propagation Delay	Note 1	Note 1	1.4	1.9	2.4	ns
Buffer Additive Phase Jitter, RMS		26MHz TCXO clipped sine wave input, Integration Range: 12kHz to 20MHz		377		fs
		125MHz LVCMOS input, Integration Range: 12kHz to 20MHz		18		fs
Output to Output Skew	$t_{SKEWO-O}$	Note 2, Rising edges at VDD/2		20	50	ps
Device to Device Skew	$t_{SKEWD-D}$	Rising edges at VDD/2			200	ps
Output Enable/Disable time (OEx to CLKOUTx driven/Hi-Z)	t_{EN}/t_{DIS}	CL < 5pF			3.2	ns
Start-up Time	$t_{START-UP}$	Part start-up time for valid outputs after VDD ramp-up			2	ms
TCXO Clock Clipped Sine Wave Input Voltage Swing Level	VIN_{pp}	VDD = 3.3V, should connect to CLKIN through AC coupling and bias circuit		0.5		V

Notes:
1. With rail to rail input clock.
2. Between any 2 outputs with equal loading.
3. Duty cycle on outputs will match incoming clock duty cycle. Consult IDT for tight duty cycle clock generators.

Test Load and Circuit



AC Coupling and Bias Circuit



Component	Value
C1	0.1µF
R1	10k
R2	10k

Package Outline Drawings

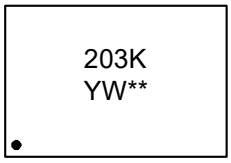
The package outline drawings are located at the end of this document and are accessible from the Renesas website (see Ordering Information for POD links). The package information is the most current data available and is subject to change without revision of this document.

Ordering Information

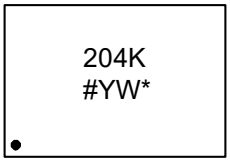
Part Number	Carrier	Package Description	Temp. Range
5PB1203NTGK	Cut Tape	10-pin DFN	-40 to +105°C
5PB1203NTGK8	Tape and Reel	10-pin DFN	-40 to +105°C
5PB1213NTGK	Cut Tape	10-pin DFN	-40 to +105°C
5PB1213NTGK8	Tape and Reel	10-pin DFN	-40 to +105°C
5PB1204CMGK	Cut Tape	16-pin VFQFPN	-40 to +105°C
5PB1204CMGK8	Tape and Reel	16-pin VFQFPN	-40 to +105°C
5PB1214CMGK	Cut Tape	16-pin VFQFPN	-40 to +105°C
5PB1214CMGK8	Tape and Reel	16-pin VFQFPN	-40 to +105°C
5PB1206NDGK	Tube	20-pin VFQFPN	-40 to +105°C
5PB1206NDGK8	Tape and Reel	20-pin VFQFPN	-40 to +105°C
5PB1216NDGK	Tube	20-pin VFQFPN	-40 to +105°C
5PB1216NDGK8	Tape and Reel	20-pin VFQFPN	-40 to +105°C

“G” after the two-letter package code denotes Pb-Free configuration, RoHS compliant.

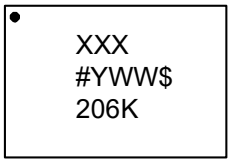
Marking Diagrams



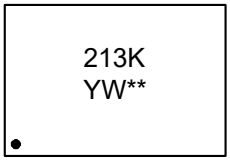
10-pin DFN



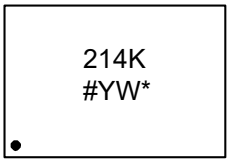
16-pin VFQFPN



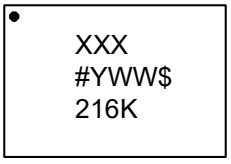
20-pin VFQFPN



10-pin DFN



16-pin VFQFPN



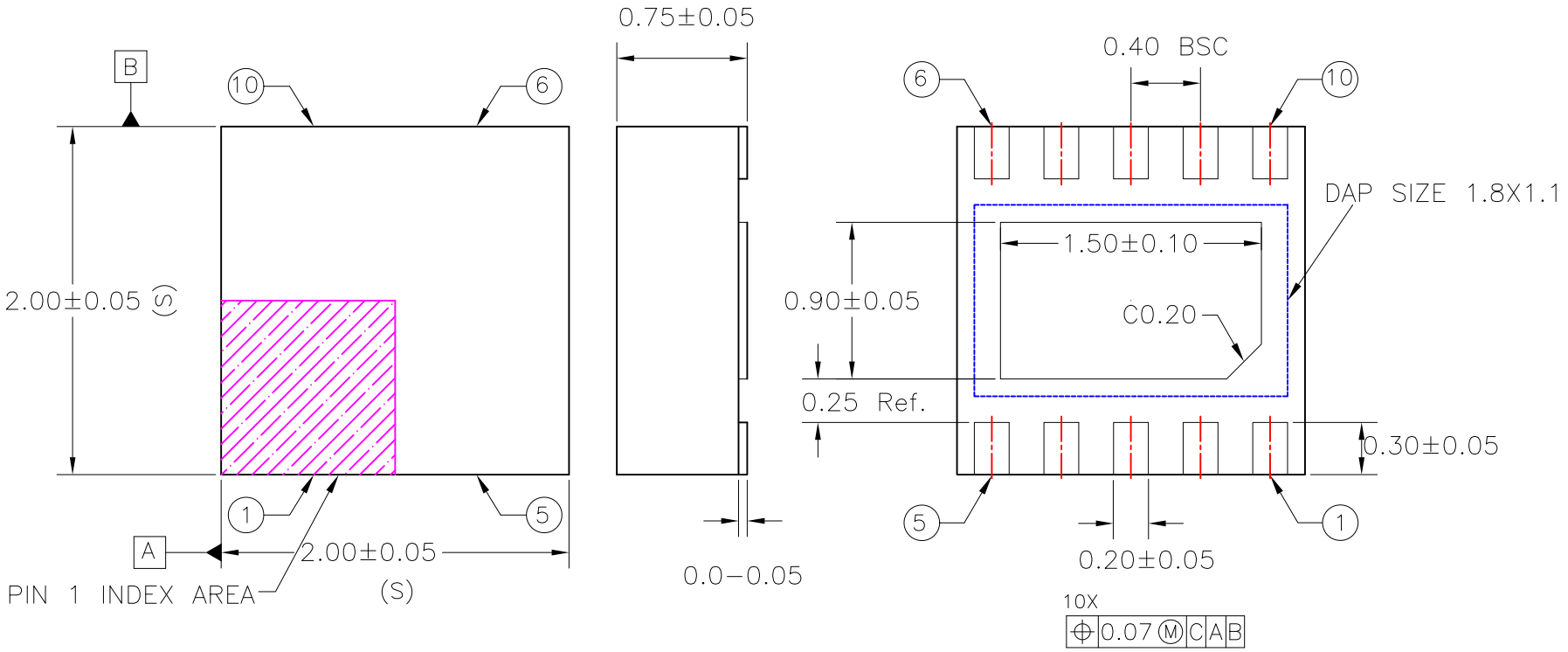
20-pin VFQFPN

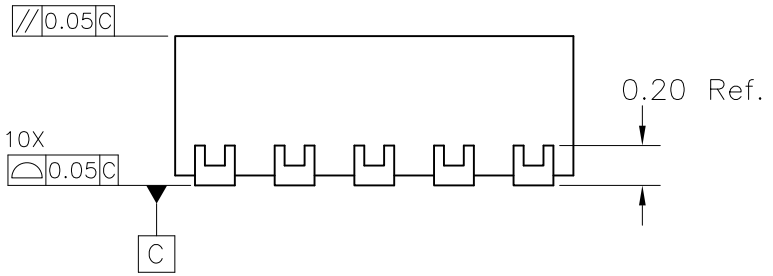
Notes:
1. “**” is the lot number.
2. “YWW”, “YW”, or “Y” are the last digit(s) of the year and week that the part was assembled.
3. “$” denotes mark location code.
4. “K” denotes extended temperature range device.
5. “XXX” denotes last three characters of Asm lot.
6. “#” denotes stepping number.

Revision History

Date	Description of Change
August 14, 2026	Updated Marking Diagrams.
June 7, 2022	▪ Updated pin 1 dot location for 20-pin VFQFPN Marking Diagrams. ▪ Updated Package Outline Drawings and Ordering Information section.
December 7, 2021	▪ Updated Pin Descriptions. ▪ Corrected Output Enable/Disable time (OEx to CLKOUTx driven/Hi-Z) enable/disable time for 1.8V, 2.5V, and 3.3V AC Electrical Characteristics.
January 15, 2021	Updated 1st paragraph text in External Components section.
February 3, 2020	▪ Updated the capacitor value for C1 in AC Coupling and Bias Circuit
November 22, 2019	▪ Updated “Operating Supply Current” data in DC Electrical Characteristics for VDD = 1.8V ±5%, VDD = 2.5V ±5%, and VDD = 3.3V ±5% ▪ Updated Package Outline Drawings; however, no mechanical changes
February 28, 2018	▪ Updated CLKIN input high and low voltage ratings in DC characterization tables. ▪ Updated Absolute Maximum supply voltage (VDD) from 3.465V to 3.8V.
April 10, 2017	▪ Updated Operating Supply Current and Operating Voltage values in DC electrical characteristics tables. ▪ Updated Propagation Delay and Output skew values in AC electrical characteristics tables. ▪ Updated package outline drawings. ▪ Updated legal disclaimer.
July 11, 2016	Initial release.

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	5/20/15	J.HUA



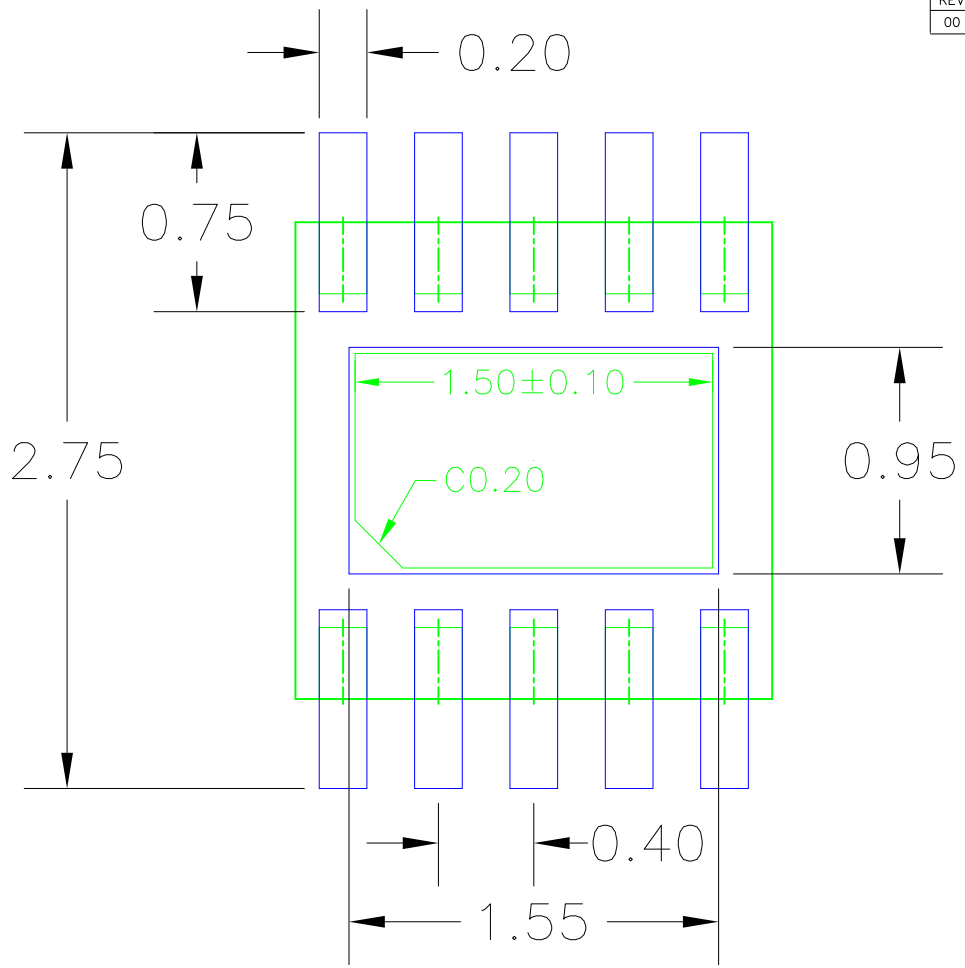


NOTES:

1. ALL DIMENSIONS IN MM.

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR XX± ± XXX± XXXX±		IDT™ www.IDT.com	6024 Silver Creek Valley Rd San Jose, CA 95138 PHONE: (408) 727-6116 FAX: (408) 492-8674
APPROVALS	DATE	TITLE	NTG10 PACKAGE OUTLINE 2.0 x 2.0 mm BODY 0.75 mm THICK
DRAWN RAC	5/20/15		
CHECKED		SIZE C	DRAWING No. PSC-4612 REV 00
		DO NOT SCALE DRAWING	SHEET 1 OF 2

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	5/20/15	J.HUA



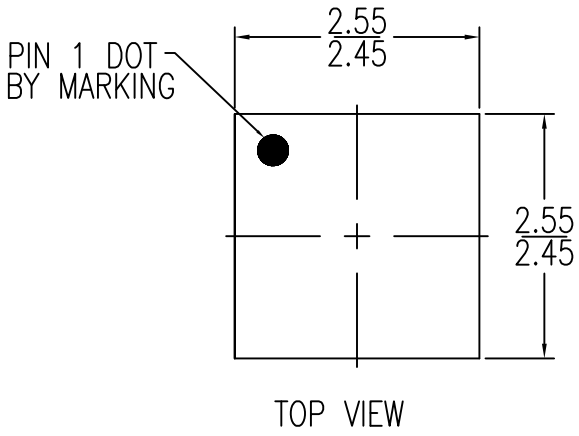
RECOMMENDED LAND PATTERN DIMENSION

NOTES:

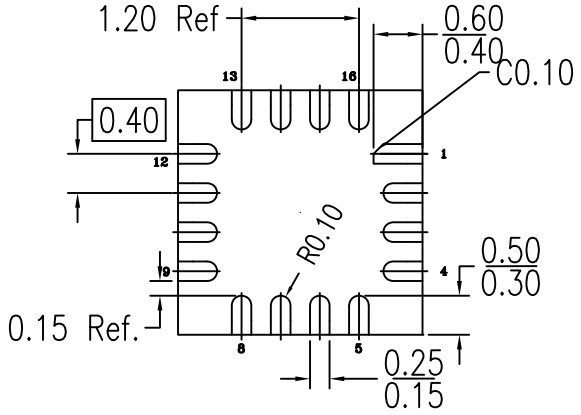
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW, AS VIEWED ON PCB.
3. COMPONENT OUTLINE IS SHOWN FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR XX± ± XXX± XXXX±		IDT™ www.IDT.com	6024 Silver Creek Valley Rd San Jose, CA 95138 PHONE: (408) 727-6116 FAX: (408) 492-8674
APPROVALS	DATE	TITLE	NTG10 PACKAGE OUTLINE 2.0 x 2.0 mm BODY 0.75 mm THICK
DRAWN RAC	5/20/15		
CHECKED			
		SIZE C	DRAWING No. PSC-4612 REV 00
		DO NOT SCALE DRAWING	SHEET 2 OF 2

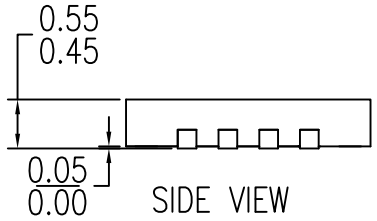
REVISIONS			
DATE CREATED	REV	DESCRIPTION	AUTHOR
4/3/14	00	INITIAL RELEASE	JH
12/11/14	01	ADD PIN1 CHAMFER	JH
4/5/18	02	CHANGE QFN TO VFQFPN, RECALCULATE LAND PATTERN	RC
NOE: REFER TO DCP FOR OFFICIAL RELEASE DATE			



TOP VIEW



BOTTOM VIEW

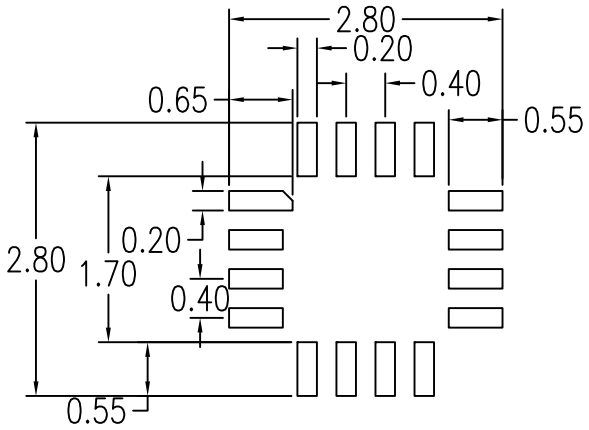


SIDE VIEW

NOTES:
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1982
2. ALL DIMENSIONS ARE IN MILLIMETERS.

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR X± ±1° XX± XXX±	IDT™ www.IDT.com	6024 Silver Creek Valley Road San Jose CA 95138 PHONE: (408) 284–8200 FAX: (408) 284–8591
DRAWN	TITLE: CMG16 Package Outline Drawing 2.5 x 2.5 x 0.5 mm Body 0.40mm Pitch VFQFPN	
	SIZE: C DRAWING No.: PSC–4478 REV: 02	
	DO NOT SCALE DRAWING	SHEET 1 OF 2

REVISIONS			
DATE CREATED	REV	DESCRIPTION	AUTHOR
4/3/14	00	INITIAL RELEASE	JH
12/11/14	01	ADD PIN1 CHAMFER	JH
4/5/18	02	CHANGE QFN TO VFQFPN, RECALCULATE LAND PATTERN	RC
NOE: REFER TO DCP FOR OFFICIAL RELEASE DATE			



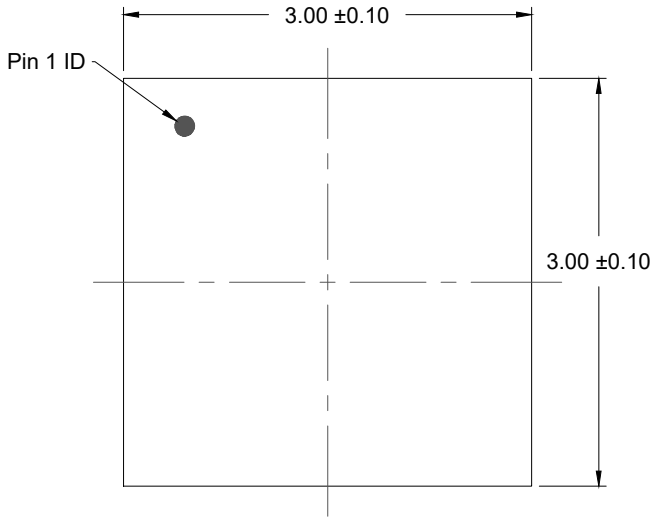
RECOMMENDED LAND PATTERN DIMENSION

NOTES:
1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW AS VIEWED ON PCB.
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

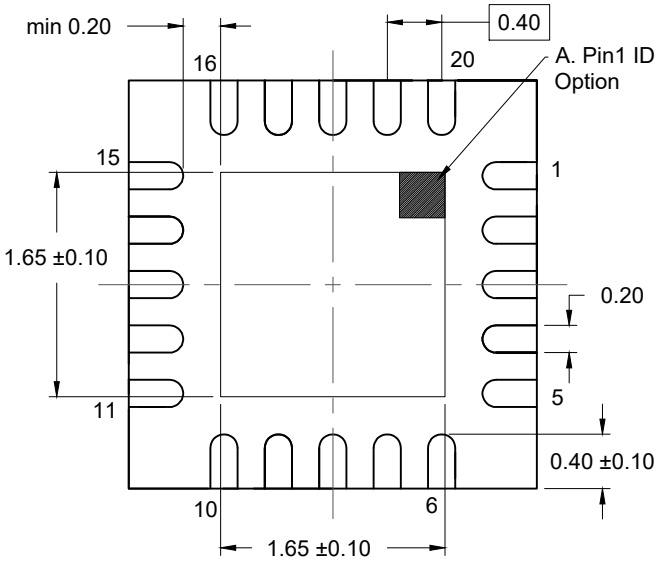
TOLERANCES UNLESS SPECIFIED DECIMAL X± XX± XXX± ANGULAR ±1°	IDT™ www.IDT.com 6024 Silver Creek Valley Road San Jose CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-8591
DRAWN	TITLE CMG16 Package Outline Drawing 2.5 x 2.5 x 0.5 mm Body 0.40mm Pitch VFQFPN
	SIZE C | DRAWING No. PSC-4478 | REV 02
	DO NOT SCALE DRAWING | SHEET 2 OF 2

Package Outline Drawing

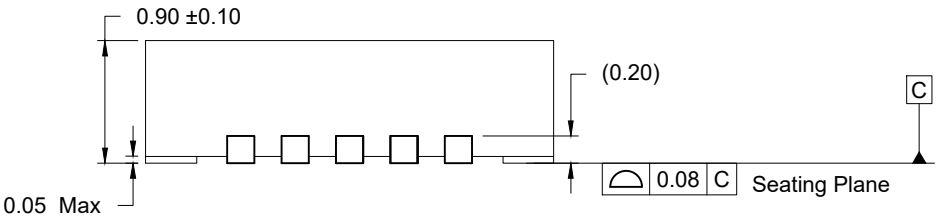
PSC-4179-02
NDG20P2
20-VFQFPN 3.0 x 3.0 x 0.9 mm Body, 0.4mm Pitch
Rev.03, May 5, 2025



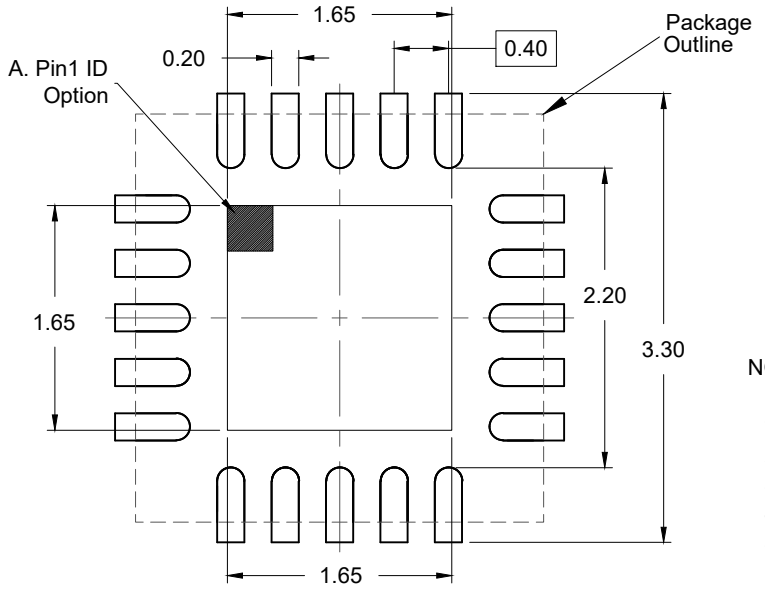
TOP VIEW



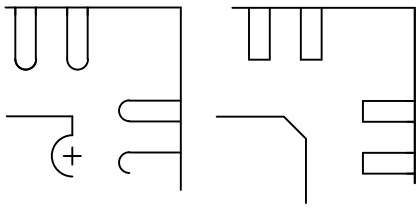
BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)



A. PIN1 ID OPTION DETAILS

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.
5. Pin#1 ID is identified by either chamfer or notch.

© Renesas Electronics Corporation

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

© 2026 Renesas Electronics Corporation. All rights reserved.