FAST CMOS BUFFER/CLOCK DRIVER

IDT49FCT805/A

FEATURES:

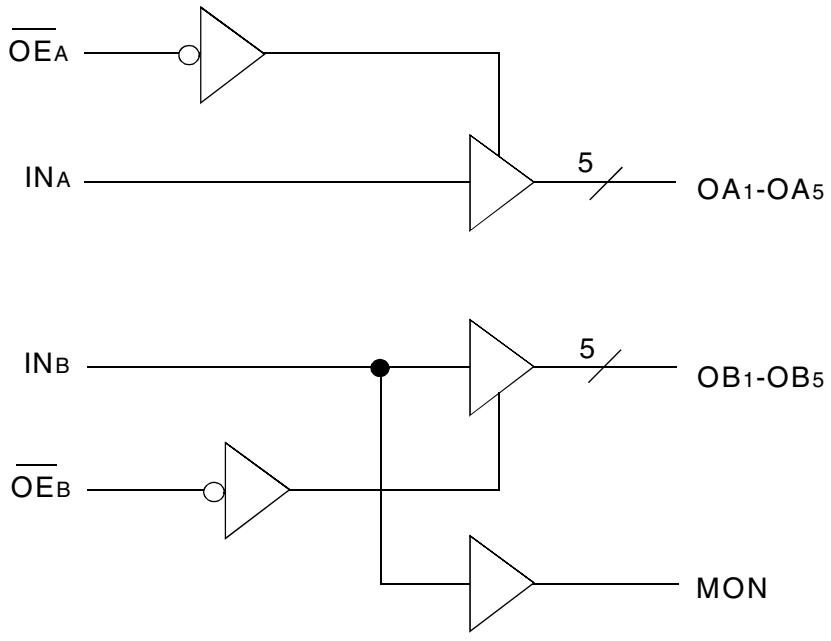
- 0.5 MICRON CMOS Technology
- Guaranteed low skew < 700ps (max.)
- Low duty cycle distortion < 1ns (max.)
- Low CMOS power levels
- TTL compatible inputs and outputs
- Rail-to-rail output voltage swing
- High drive: -24mA I_{OH}, +64mA I_{OL}
- Two independent output banks with 3-state control
- 1:5 fanout per bank
- "Heartbeat" monitor output
- Available in SSOP and SOIC packages

DESCRIPTION:

The 49FCT805 is a non-inverting buffer/clock driver built using advanced dual metal CMOS technology. Each bank consists of two banks of drivers. Each bank drives five output buffers from a standard TTL compatible input. These devices feature a "heart-beat" monitor for diagnostics and PLL driving. The MON output is identical to all other outputs and complies with the output specifications in this document.

The 49FCT805 offers low capacitance inputs and hysteresis. Rail-to-rail output swing improves noise margin and allows easy interface with CMOS inputs.

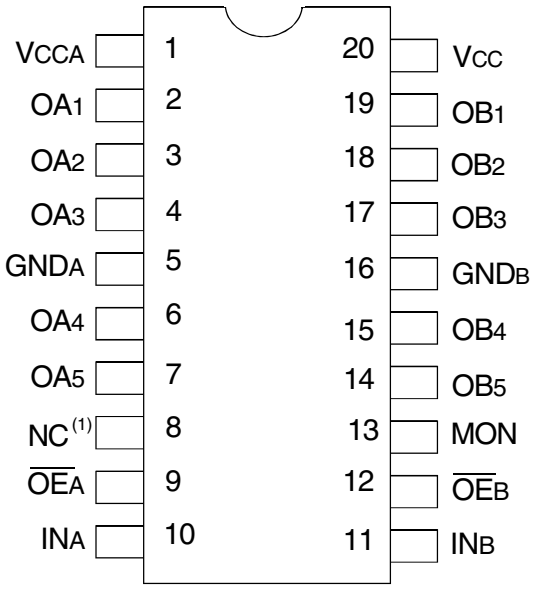
FUNCTIONAL BLOCK DIAGRAM



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PIN CONFIGURATION



SOIC/ SSOP
TOP VIEW

NOTE:
1. Pin 8 is not internally connected on devices with a "K" prefix in the date code. On older devices, pin 8 is internally connected to GND. To insure compatibility with all products, pin 8 should be connected to GND at the board level.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC}+0.5	V
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	DC Output Current	–60 to +60	mA

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Input and V_{CC} terminals.
3. Output and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8	pF

NOTE:
1. This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}_A$, $\overline{OE}_B$	3-State Output Enable Inputs (Active LOW)
IN_A, IN_B	Clock Inputs
OAn, OBn	Clock Outputs
MON	Monitor Output

FUNCTION TABLE(1)

Inputs		Outputs	
$\overline{OE}_A$, $\overline{OE}_B$	IN_A, IN_B	OAn, OBn	MON
L	L	L	L
L	H	H	H
H	L	Z	L
H	H	Z	H

NOTE:
1. H = HIGH
   L = LOW
   Z = High-Impedance

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DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C, Industrial: T_A = -40°C to +85°C, V_{CC} = 5V ± 5%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level		2	—	—	V
V_{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = 5.5V	—	—	±1	µA
I_{IL}	Input LOW Current	V_{CC} = Max.	V_I = GND	—	—	±1	µA
I_{OZH}	Off State (Hi-Z) Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	±1	µA
I_{OZL}			V_O = GND	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–60	–120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}	I_{OH} = –32µA	V_{HC}	V_{CC}	—	V
		V_{CC} = Min.	I_{OH} = –300µA	V_{HC}	V_{CC}	—	
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –15mA	3.6	4.3	—	
			I_{OH} = –24mA	2.4	3.8	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}	I_{OL} = 300µA	—	GND	V_{LC}	V
		V_{CC} = Min.	I_{OL} = 300mA	—	GND	V_{LC}	
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 64mA	—	0.3	0.55	
V_H	Input Hysteresis for all inputs	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	5	500	µA

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.

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POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	1	2.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE_A}$ = $\overline{OE_B}$ = GND 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.2	mA/MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_O = 10MHz	V_{IN} = V_{CC} V_{IN} = GND	—	1.5	2.5	mA
		50% Duty Cycle $\overline{OE_A}$ = $\overline{OE_B}$ = V_{CC} Mon. Output Toggling	V_{IN} = 3.4V V_{IN} = GND	—	2	3.8	
		V_{CC} = Max. Outputs Open f_O = 2.5MHz	V_{IN} = V_{CC} V_{IN} = GND	—	4.1	6[5]	
		50% Duty Cycle $\overline{OE_A}$ = $\overline{OE_B}$ = GND Eleven Outputs Toggling	V_{IN} = 3.4V V_{IN} = GND	—	5.1	8.5[5]	

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_C formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_O N_O)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_O = Output Frequency
   N_O = Number of Outputs at f_O
   All currents are in milliamps and all frequencies are in megahertz.

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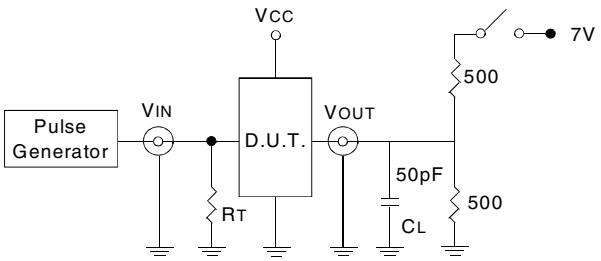
SWITCHING CHARACTERISTICS OVER OPERATING RANGE(1)

Symbol	Parameter	Conditions(2)	FCT805		FCT805A		Unit
			Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay IN_A to OA_n, IN_B to OB_n	C_L = 50pF R_L = 500Ω	1.5	5.6	1.5	5.3	ns
t_R	Output Rise Time		—	1.5	—	1.5	ns
t_F	Output Fall Time		—	1.5	—	1.5	ns
$t_{SK(O)}$	Output skew: skew between outputs of all banks of same package (inputs tied together)		—	0.7	—	0.7	ns
$t_{SK(P)}$	Pulse skew: skew between opposite transitions of same output ($\lvert t_{PHL} - t_{PLH} \rvert$)		—	1	—	1	ns
$t_{SK(PP)}$	Part-to-part skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade		—	1.5	—	1.5	ns
t_{PZL} t_{PZH}	Output Enable Time $\overline{OE}_A$ to OA_n, $\overline{OE}_B$ to OB_n		1.5	8	1.5	8	ns
t_{PLZ} t_{PHZ}	Output Disable Time $\overline{OE}_A$ to OA_n, $\overline{OE}_B$ to OB_n		1.5	7	1.5	7	ns

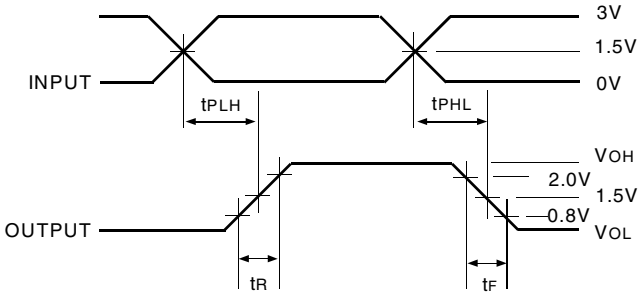
NOTES:
1. Propagation delay range indicated by Min. and Max. limit is due to V_{CC}, operating temperature and process parameters. These propagation delay limits do not imply skew.
2. See test circuits and waveforms.

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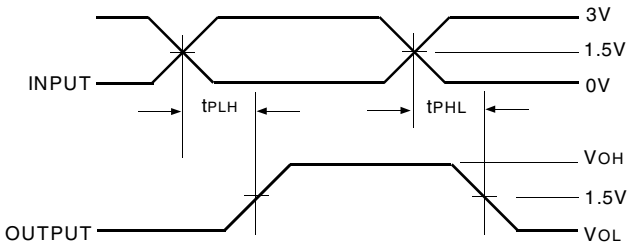
TEST CIRCUITS AND WAVEFORMS



Test Circuits for All Outputs

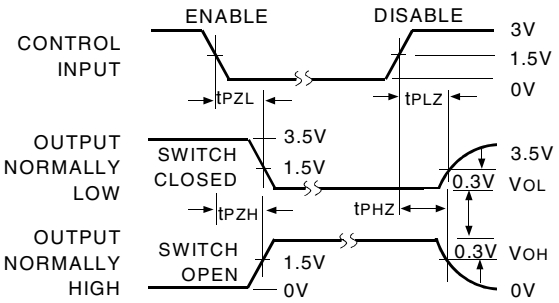


Package Delay



$t_{SK(p)} = |t_{PHL} - t_{PLH}|$

Pulse Skew - $t_{SK(P)}$



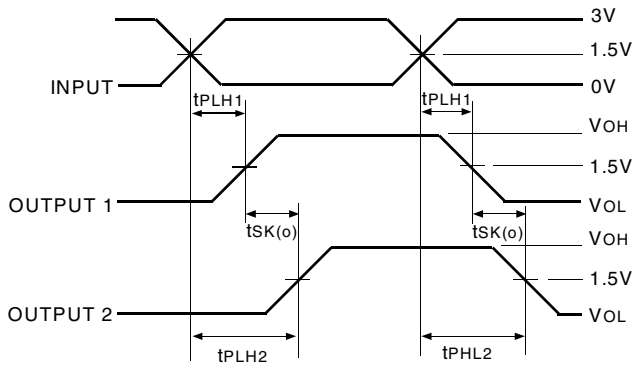
Enable and Disable Times

NOTES:
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤1.0MHz; t_F ≤2.5ns; t_R ≤2.5ns

SWITCH POSITION

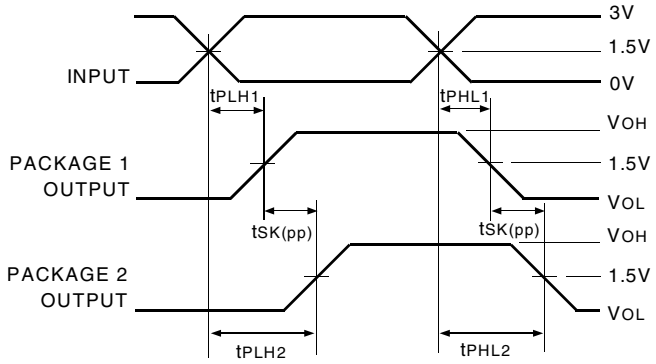
Test	Switch
Disable LOW Enable LOW	Closed
Disable HIGH Enable HIGH	GND

DEFINITIONS:
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.



$t_{SK(o)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

Output Skew



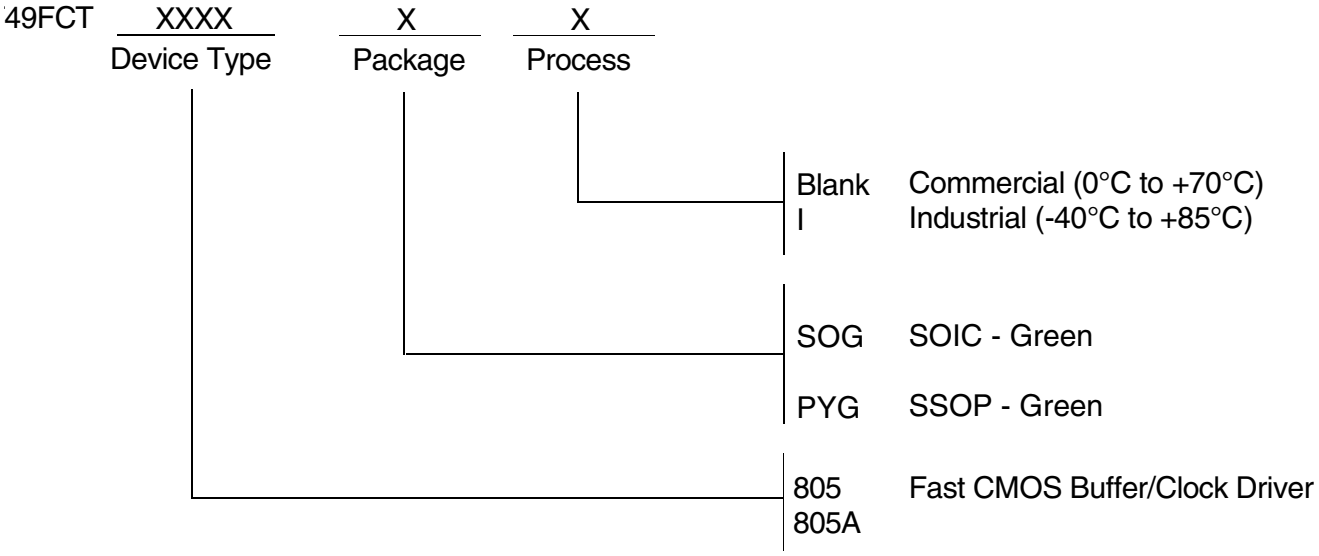
$t_{SK(pp)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

Part-to-Part Skew - $t_{SK(PP)}$

NOTE:
1. Package 1 and Package 2 are same device type and speed grade.

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