ICL7667

Dual Power MOSFET Driver

FN2853
Rev 7.00
September 4, 2015

The ICL7667 is a dual monolithic high-speed driver designed to convert TTL level signals into high current outputs at voltages up to 15V. Its high speed and current output enable it to drive large capacitive loads with high slew rates and low propagation delays. With an output voltage swing only millivolts less than the supply voltage and a maximum supply voltage of 15V, the ICL7667 is well suited for driving power MOSFETs in high frequency switched-mode power converters. The ICL7667's high current outputs minimize power losses in the power MOSFETs by rapidly charging and discharging the gate capacitance. The ICL7667's inputs are TTL compatible and can be directly driven by common pulse-width modulation control ICs.

Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ICL7667CBA* **(No longer available, recommended replacement: ICL7667CBAZA)**	7667 CBA	0 to 70	8 Ld SOIC (N)	M8.15
ICL7667CBAZA	7667 CBAZ	0 to 70	8 Ld SOIC (N) (Pb-Free)	M8.15
ICL7667CPA*	7667 CPA	0 to 70	8 Ld PDIP	E8.3
ICL7667CPAZ	7667 CPAZ	0 to 70	8 Ld PDIP** (Pb-Free)	E8.3

*Add "-T" suffix for tape and reel. Please refer to TB347 for details on reel specifications.

**Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

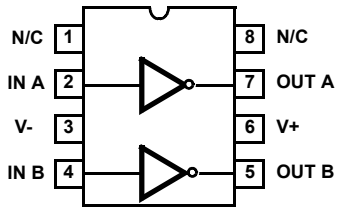
- Fast Rise and Fall Times
  - 30ns with 1000pF Load
- Wide 15V Supply Voltage Range
  - V+ = +4.5V to +15V
  - V- = -15V to Ground (0V)
- Low Power Consumption
  - 4mW with Inputs Low
  - 20mW with Inputs High
- TTL/CMOS Input Compatible Power Driver
  - R_{OUT} = 7Ω Typ
- Direct Interface with Common PWM Control ICs
- Pin Equivalent to DS0026/DS0056; TSC426
- Pb-Free Available (RoHS Compliant)

Applications

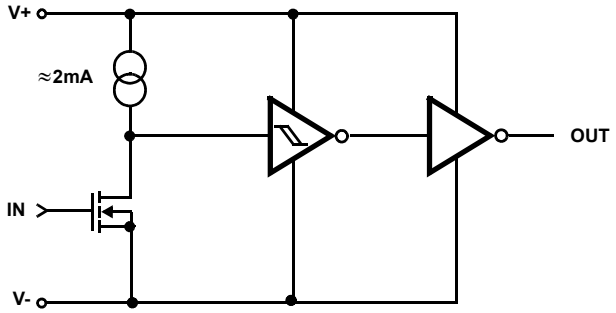
- Switching Power Supplies
- DC/DC Converters
- Motor Controllers

Pinout

ICL7667
(8 LD PDIP, SOIC)
TOP VIEW



Functional Diagram (Each Driver)



Absolute Maximum Ratings

Supply Voltage V+ to V- . . . . . ±18V
Input Voltage . . . . . V- -0.3V to V+ +0.3V
Package Dissipation, T_A +25°C 500mW

Operating Conditions

ICL7667C. . . . . 0° to +70°C
Supply Voltages: V+ = +4.5V to +15V; V- = Ground to -15V
Logic Inputs: Logic Low = V- < Vin < 0.8V ; Logic High = 2.0V< Vin < V+

Thermal Information

Thermal Resistance (Typical, Note 1, 2)	θ_{JA} (°C/W)	θ_{JC}(°C/W)
8 Ld PDIP Package	150	N/A
8 Ld SOIC Package	170	N/A

Maximum Storage Temperature Range . . . . . -65° to +150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)
Pb-Free Reflow Profile. . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp
Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

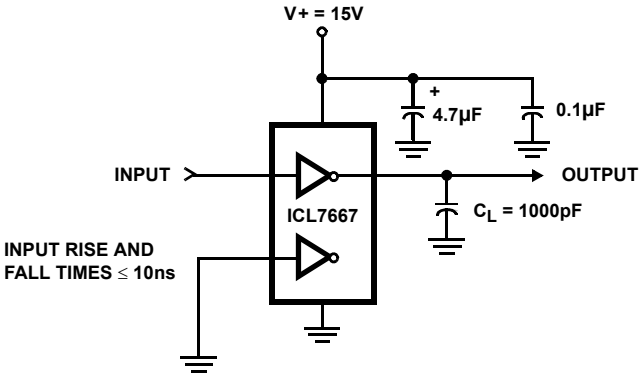
1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
2. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

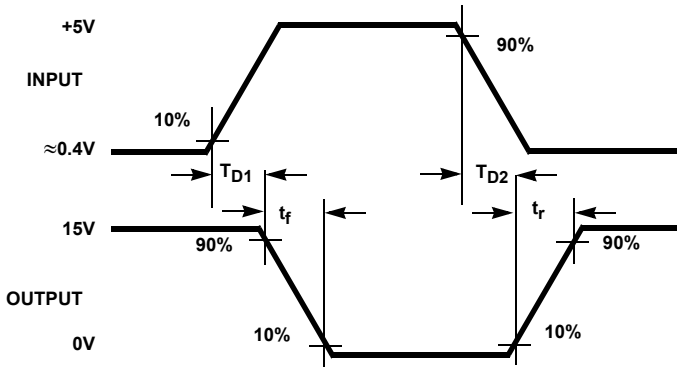
Electrical Specifications

Parameters with MIN and/or MAX limits are 100% tested at +25°C, V+ = 0V unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETER	SYMBOL	TEST CONDITIONS	ICL7667C, M T_A = +25°C			ICL7667M 0°C ≤ T_A ≤ +70°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
DC SPECIFICATIONS									
Logic 1 Input Voltage	V_{IH}	V+ = 4.5V	2.0	-	-	2.0	-	-	V
Logic 1 Input Voltage	V_{IH}	V+V+ = 15V	2.0	-	-	2.0	-	-	V
Logic 0 Input Voltage	V_{IL}	V+ = 4.5V	-	-	0.8	-	-	0.5	V
Logic 0 Input Voltage	V_{IL}	V+ = 15V	-	-	0.8	-	-	0.5	V
Input Current	I_{IL}	V+ = 15V, V_{IN} = 0V and 15V	-0.1	-	0.1	-0.1	-	0.1	µA
Output Voltage High	V_{OH}	V+ = 4.5V and 15V	V+ -0.05	V+	-	V+ -0.1	V+	-	V
Output Voltage Low	V_{OL}	V+ = 4.5V and 15V	-	0	0.05	-	-	0.1	V
Output Resistance	R_{OUT}	V_{IN} = V_{IL}, I_{OUT} = -10mA, V+ = 15V	-	7	10	-	-	12	Ω
Output Resistance	R_{OUT}	V_{IN} = V_{IH}, I_{OUT} = 10mA, V+ = 15V	-	8	12	-	-	13	Ω
Power Supply Current	I_{CC}	V+ = 15V, V_{IN} = 3V both inputs	-	5	7	-	-	8	mA
Power Supply Current	I_{CC}	V+ = 15V, V_{IN} = 0V both inputs	-	150	400	-	-	400	µA
SWITCHING SPECIFICATIONS									
Delay Time	T_{D2}	(Figure 3)	-	35	50	-	-	60	ns
Rise Time	T_R	(Figure 3)	-	20	30	-	-	40	ns
Fall Time	T_F	(Figure 3)	-	20	30	-	-	40	ns
Delay Time	T_{D1}	(Figure 3)	-	20	30	-	-	40	ns

Test Circuits





Typical Performance Curves

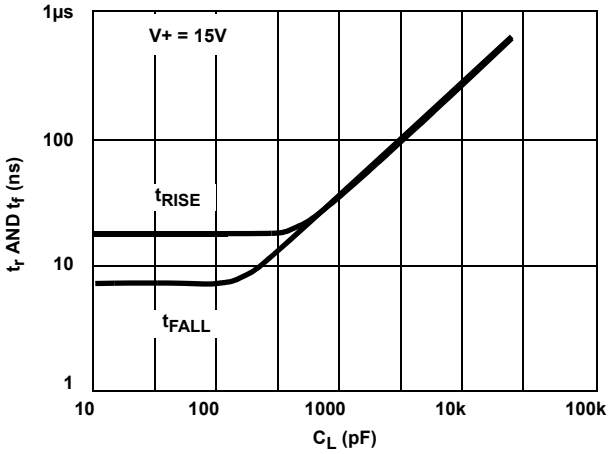


FIGURE 1. RISE AND FALL TIMES vs C_L

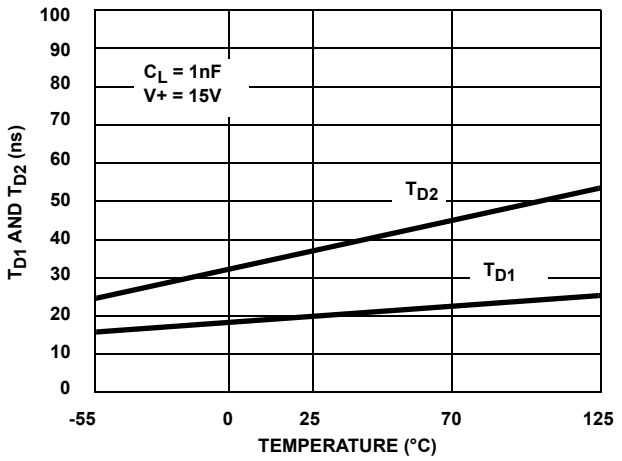


FIGURE 2. T_{D1}, T_{D2} vs TEMPERATURE

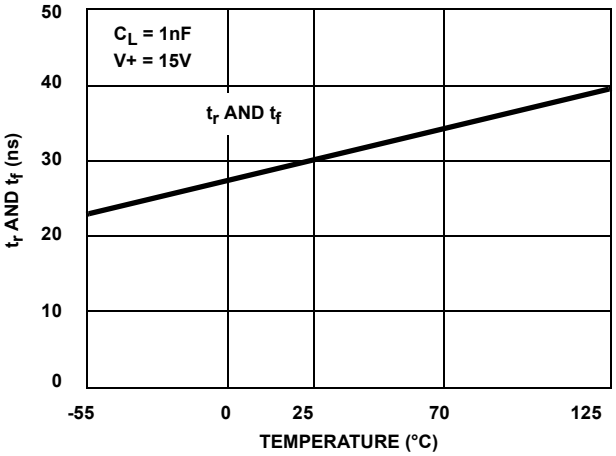


FIGURE 3. t_r, t_f vs TEMPERATURE

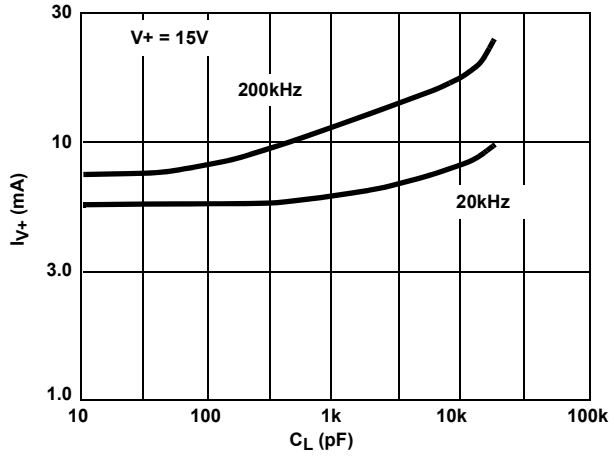


FIGURE 4. I_{V+} vs C_L

Typical Performance Curves (Continued)

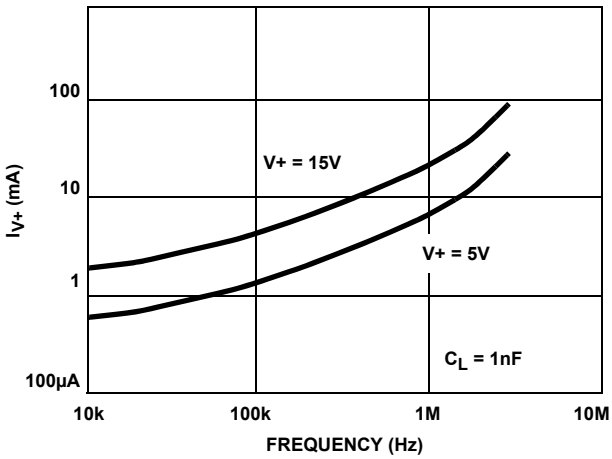


FIGURE 5. I_{V+} vs FREQUENCY

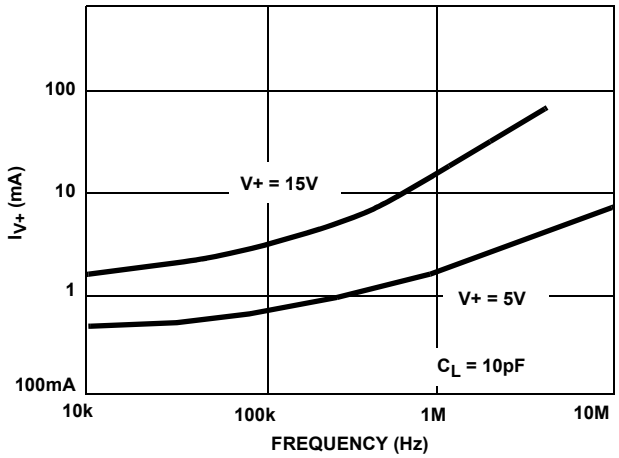


FIGURE 6. NO LOAD I_{V+} vs FREQUENCY

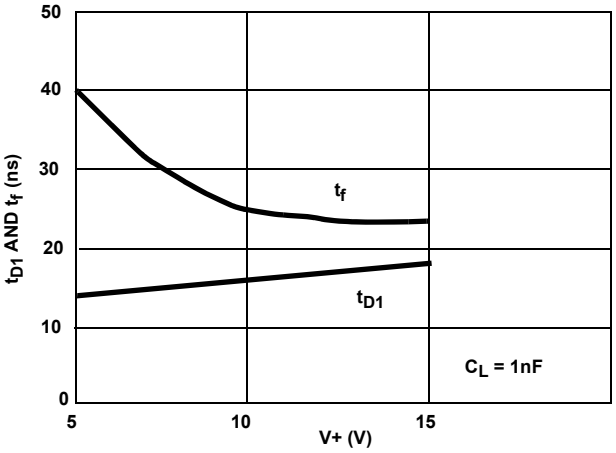


FIGURE 7. DELAY AND FALL TIMES vs V+

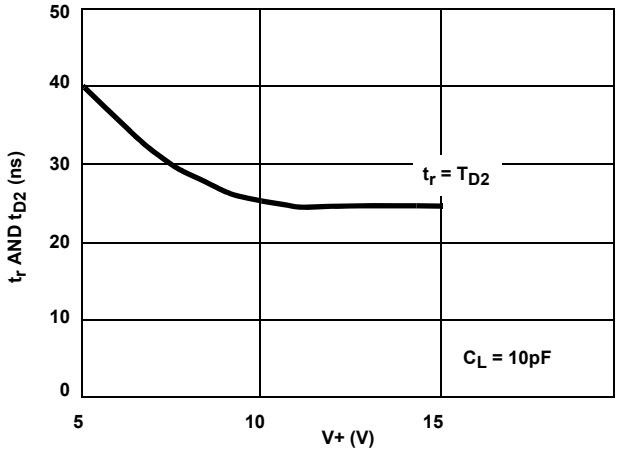


FIGURE 8. RISE TIME vs V+

Detailed Description

The ICL7667 is a dual high-power CMOS inverter whose inputs respond to TTL levels while the outputs can swing as high as 15V. Its high output current enables it to rapidly charge and discharge the gate capacitance of power MOSFETs, minimizing the switching losses in switchmode power supplies. Since the output stage is CMOS, the output will swing to within millivolts of both V- and V+ without any external parts or extra power supplies as required by the DS0026/56 family. Although most specifications are at
V+ = 15V, the propagation delays and specifications are almost independent of V+.

In addition to power MOS drivers, the ICL7667 is well suited for other applications such as bus, control signal, and clock drivers on large memory of microprocessor boards, where the load capacitance is large and low propagation delays are required. Other potential applications include peripheral power drivers and charge-pump voltage inverters.

Input Stage

The input stage is a large N-Channel FET with a P-Channel constant-current source. This circuit has a threshold of about 1.5V, relatively independent of the V+ voltage. This means that the inputs will be directly compatible with TTL over the entire 4.5V - 15V V+ range. Being CMOS, the inputs draw less than 1µA of current over the entire input voltage range of V- to V+. The quiescent current or no load supply current of the ICL7667 is affected by the input voltage, going to nearly zero when the inputs are at the 0 logic level and rising to 7mA maximum when both inputs are at the 1 logic level. A small amount of hysteresis, about 50mV to 100mV at the input, is generated by positive feedback around the second stage.

Output Stage

The ICL7667 output is a high-power CMOS inverter, swinging between V- and V+. At V+ = 15V, the output impedance of the inverter is typically 7Ω. The high peak current capability of the ICL7667 enables it to drive a 1000pF load with a rise time of

only 40ns. Because the output stage impedance is very low, up to 300mA will flow through the series N-Channel and P-Channel output devices (from V+ to V-) during output transitions. This crossover current is responsible for a significant portion of the internal power dissipation of the ICL7667 at high frequencies. It can be minimized by keeping the rise and fall times of the input to the ICL7667 below 1µs.

Application Notes

Although the ICL7667 is simply a dual level-shifting inverter, there are several areas to which careful attention must be paid.

Grounding

Since the input and the high current output current paths both include the V- pin, it is very important to minimize and common impedance in the ground return. Since the ICL7667 is an inverter, any common impedance will generate negative feedback, and will degrade the delay, rise and fall times. Use a ground plane if possible, or use separate ground returns for the input and output circuits. To minimize any common inductance in the ground return, separate the input and output circuit ground returns as close to the ICL7667 as is possible.

Bypassing

The rapid charging and discharging of the load capacitance requires very high current spikes from the power supplies. A parallel combination of capacitors that has a low impedance over a wide frequency range should be used. A 4.7µF tantalum capacitor in parallel with a low inductance 0.1µF capacitor is usually sufficient bypassing.

Output Damping

Ringing is a common problem in any circuit with very fast rise or fall times. Such ringing will be aggravated by long inductive lines with capacitive loads. Techniques to reduce ringing include:

- Reduce inductance by making printed circuit board traces as short as possible.
- Reduce inductance by using a ground plane or by closely coupling the output lines to their return paths.
- Use a 10Ω to 30Ω resistor in series with the output of the ICL7667. Although this reduces ringing, it will also slightly increase the rise and fall times.
- Use good by-passing techniques to prevent supply voltage ringing.

Power Dissipation

The power dissipation of the ICL7667 has three main components:

1. Input inverter current loss
2. Output stage crossover current loss
3. Output stage I^2R power loss

The sum of the above must stay within the specified limits for reliable operation.

As noted above, the input inverter current is input voltage dependent, with an I_{V+} of 0.1mA maximum with a logic 0 input and 6mA maximum with a logic 1 input.

The output stage crowbar current is the current that flows through the series N-Channel and P-Channel devices that form the output. This current, about 300mA, occurs only during output transitions. **Caution:** The inputs should never be allowed to remain between V_{IL} and V_{IH} since this could leave the output stage in a high current mode, rapidly leading to destruction of the device. If only one of the drivers is being used, be sure to tie the unused input to V- or ground. **NEVER** leave an input floating. The average supply current drawn by the output stage is frequency dependent, as can be seen in Figure 5 (I_{V+} vs Frequency graph in the Typical Characteristics Graphs).

The output stage I^2R power dissipation is nothing more than the product of the output current times the voltage drop across the output device. In addition to the current drawn by any resistive load, there will be an output current due to the charging and discharging of the load capacitance. In most high frequency circuits the current used to charge and discharge capacitance dominates, and the power dissipation is approximately:

$$P_{AC} = CV_V 2_f \quad \text{(EQ. 1)}$$

where C = Load Capacitance, f = Frequency

In cases where the load is a power MOSFET and the gate drive requirement are described in terms of gate charge, the ICL7667 power dissipation will be:

$$P_{AC} = QGV_V f \quad \text{(EQ. 2)}$$

where Q_G = Charge required to switch the gate, in Coulombs, f = Frequency.

Power MOS Driver Circuits

Power MOS Driver Requirements

Because it has a very high peak current output, the ICL7667 the at driving the gate of power MOS devices. The high current output is important since it minimizes the time the power MOS device is in the linear region. Figure 9 is a typical curve of Charge vs Gate voltage for a power MOSFET. The flat region is caused by the Miller capacitance, where the drain-to-gate capacitance is multiplied by the voltage gain of the FET. This increase in capacitance occurs while the power MOSFET is in the linear region and is dissipating significant amounts of power. The very high current output of the ICL7667 is able to rapidly overcome this high capacitance and quickly turns the MOSFET fully on or off.

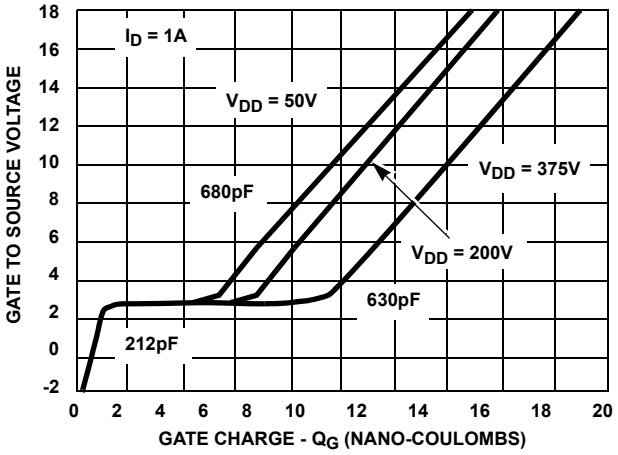


FIGURE 9. MOSFET GATE DYNAMIC CHARACTERISTICS

Direct Drive of MOSFETs

Figure 11 shows interfaces between the ICL7667 and typical switching regulator ICs. Note that unlike the DS0026, the ICL7667 does not need a dropping resistor and speedup capacitor between it and the regulator IC. The ICL7667, with its high slew rate and high voltage drive can directly drive the gate of the MOSFET. The SG1527 IC is the same as the SG1525 IC, except that the outputs are inverted. This inversion is needed since ICL7667 is an inverting buffer.

Transformer Coupled Drive of MOSFETs

Transformers are often used for isolation between the logic and control section and the power section of a switching regulator. The high output drive capability of the ICL7667 enables it to directly drive such transformers. Figure 11 shows a typical transformer coupled drive circuit. PWM ICs with either active high or active low output can be used in this circuit, since any inversion required can be obtained by reversing the windings on the secondaries.

Buffered Drivers for Multiple MOSFETs

In very high power applications which use a group of MOSFETs in parallel, the input capacitance may be very large and it can be difficult to charge and discharge quickly. Figure 13 shows a circuit which works very well with very large capacitance loads. When the input of the driver is zero, Q_1 is held in conduction by the lower half of the ICL7667 and Q_2 is clamped off by Q_1. When the input goes positive, Q_1 is turned off and a current pulse is applied to the gate of Q_2 by the upper half of the ICL7667 through the transformer, T_1. After about 20ns, T_1 saturates and Q_2 is held on by its own C_{GS} and the bootstrap circuit of C_1, D_1 and R_1. This bootstrap circuit may not be needed at frequencies greater than 10kHz since the input capacitance of Q_2 discharges slowly.

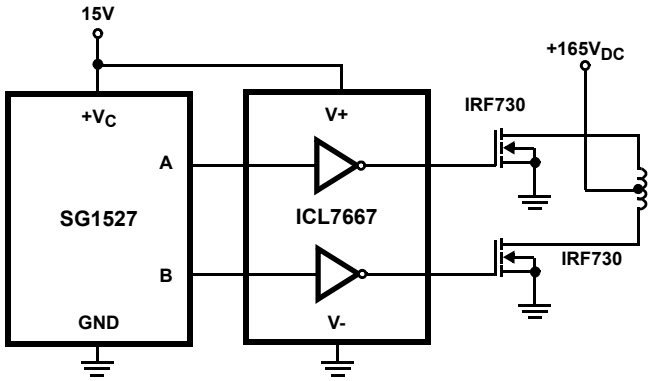


FIGURE 10A.

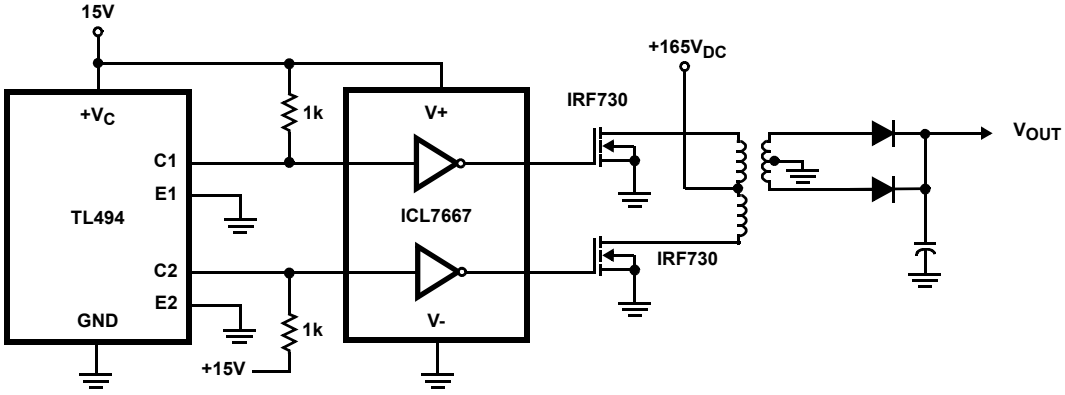


FIGURE 10B.

FIGURE 10. DIRECT DRIVE OF MOSFET GATES

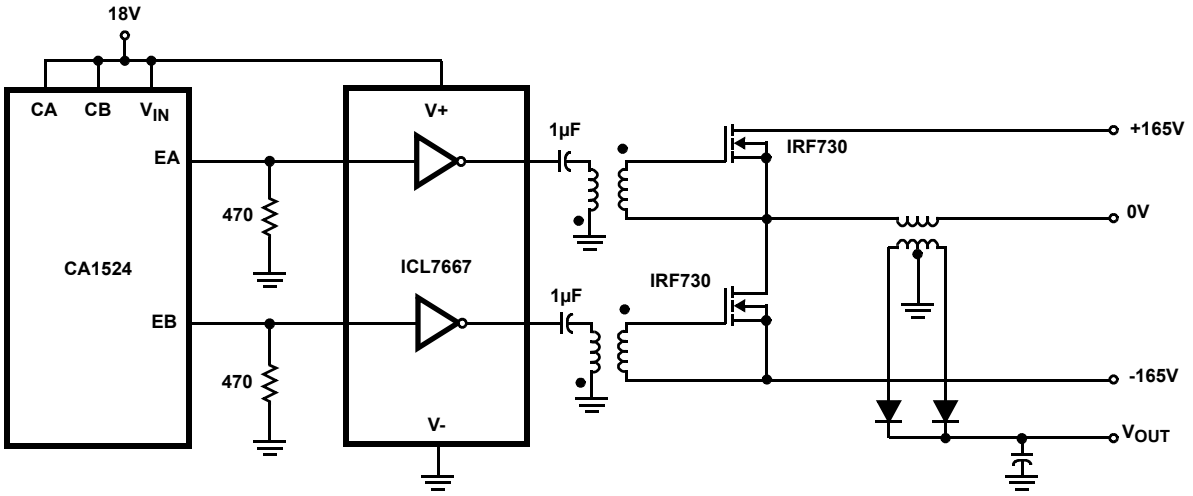


FIGURE 11. TRANSFORMER COUPLED DRIVE CIRCUIT

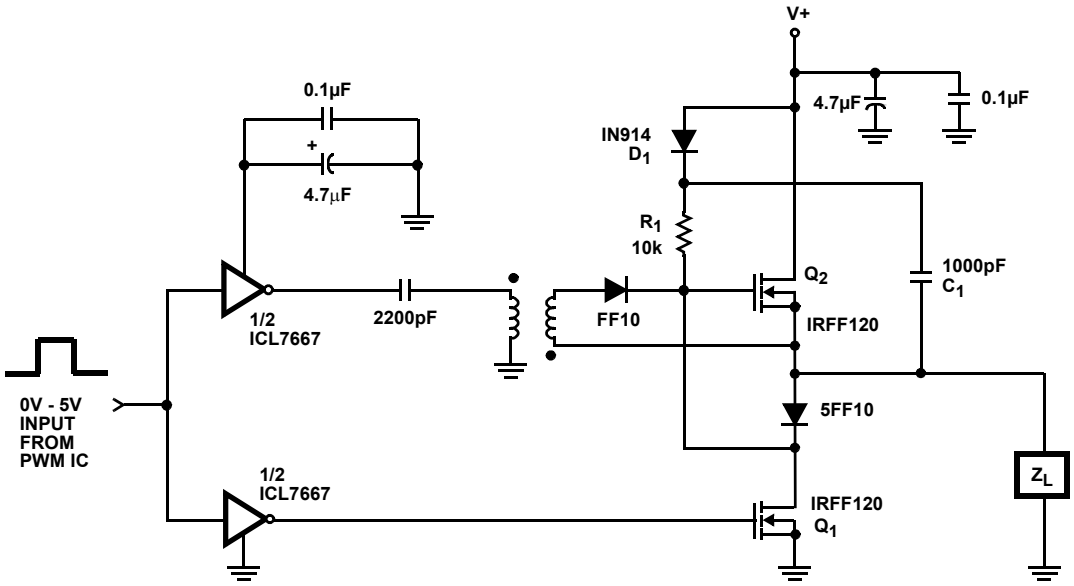


FIGURE 12. VERY HIGH SPEED DRIVER

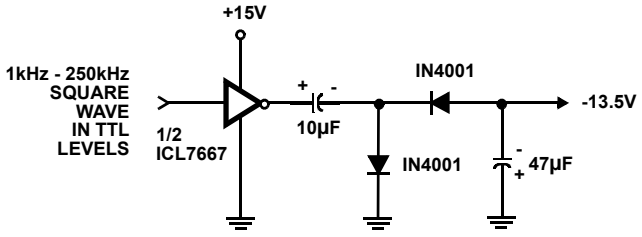


FIGURE 13A.

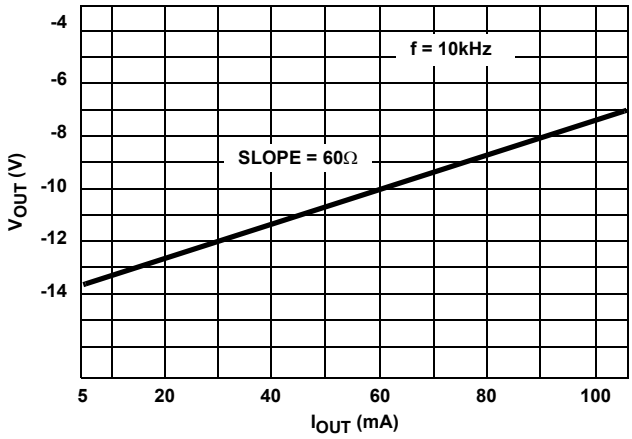


FIGURE 13B. OUTPUT CURRENT vs OUTPUT VOLTAGE

FIGURE 13. VOLTAGE INVERTER

Other Applications

Relay and Lamp Drivers

The ICL7667 is suitable for converting low power TTL or CMOS signals into high current, high voltage outputs for relays, lamps and other loads. Unlike many other level translator/driver ICs, the ICL7667 will both source and sink current. The continuous output current is limited to 200mA by the I^2R power dissipation in the output FETs.

Charge Pump or Voltage Inverters and Doublers

The low output impedance and wide V+ range of the ICL7667 make it well suited for charge pump circuits. Figure 13A shows a typical charge pump voltage inverter circuit and a typical performance curve. A common use of this circuit is to provide a low current negative supply for analog circuitry or RS232 drivers. With an input voltage of +15V, this circuit will deliver 20mA at -12.6V. By increasing the size of the capacitors, the current capability can be increased and the voltage loss decreased. The practical range of the input frequency is 500Hz to 250kHz. As the frequency goes up, the charge pump capacitors can be made smaller, but the internal losses in the ICL7667 will rise, reducing the circuit efficiency.

Figure 14, a voltage doubler, is very similar in both circuitry and performance. A potential use of Figure 13 would be to supply the higher voltage needed for EEPROM or EPROM programming.

Clock Driver

Some microprocessors (such as the CDP68HC05 families) use a clock signal to control the various LSI peripherals of the family. The ICL7667s combination of low propagation delay, high current drive capability and wide voltage swing make it attractive for this application. Although the ICL7667 is primarily intended for driving power MOSFET gates at 15V, the ICL7667 also works well as a 5V high-speed buffer. Unlike standard 4000 series CMOS, the ICL7667 uses short channel length FETs and the ICL7667 is only slightly slower at 5V than at 15V.

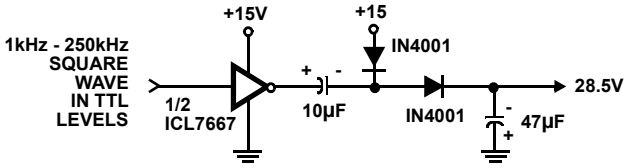


FIGURE 14. VOLTAGE DOUBLER

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
September 4, 2015	FN2853.7	Updated the Ordering Information table on page 1. Added Revision History and About Intersil sections. Updated Package Outlind Drawing M8.15 to the latest revision. -Rev 1 to Rev 2 changes - Updated to new POD format by removing table and moving dimensions onto drawing and adding land pattern -Rev 2 to Rev 3 changes - Changed in Typical Recommended Land Pattern the following: 2.41(0.095) to 2.20(0.087) 0.76 (0.030) to 0.60(0.023) 0.200 to 5.20(0.205) -Rev 3 to Rev 4 changes - Changed Note 1 "1982" to "1994"

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

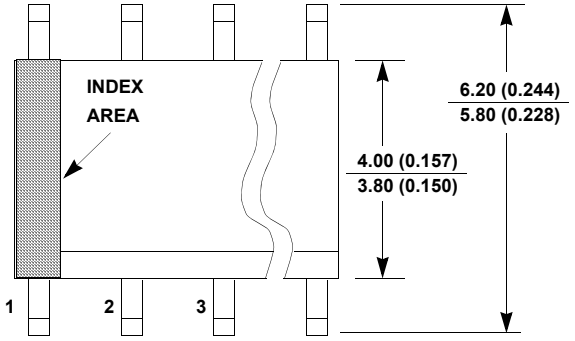
Reliability reports are also available from our website at www.intersil.com/support.

Package Outline Drawing

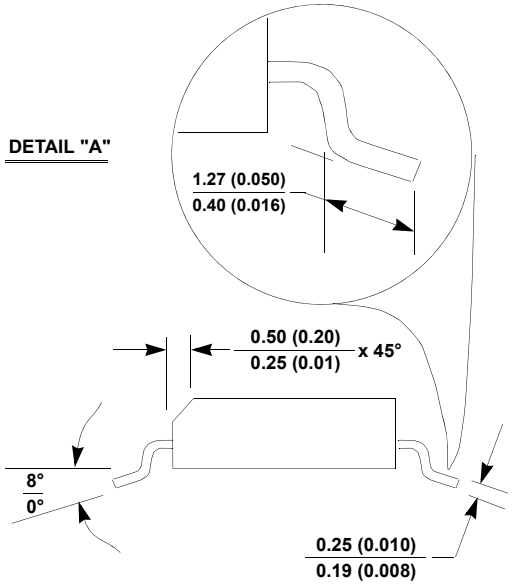
M8.15

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

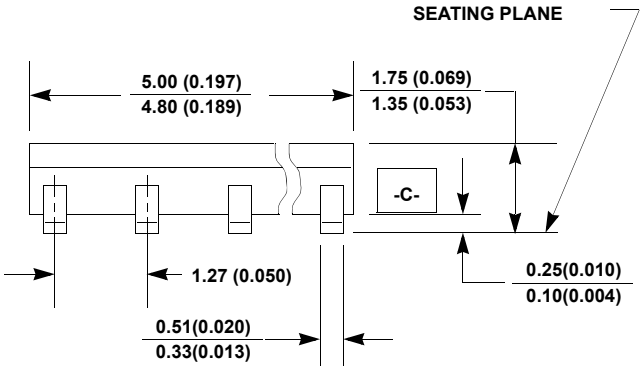
Rev 4, 1/12



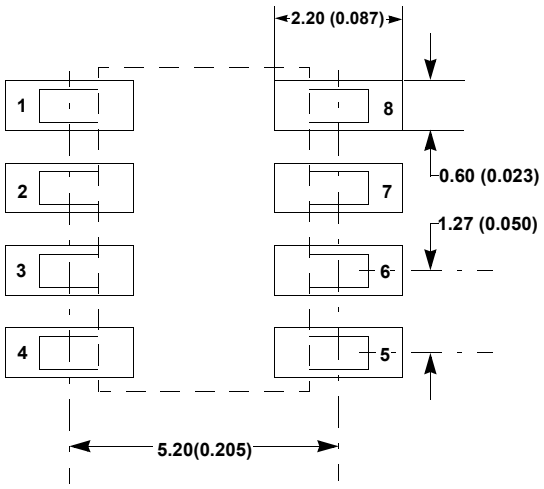
TOP VIEW



SIDE VIEW "B"



SIDE VIEW "A"

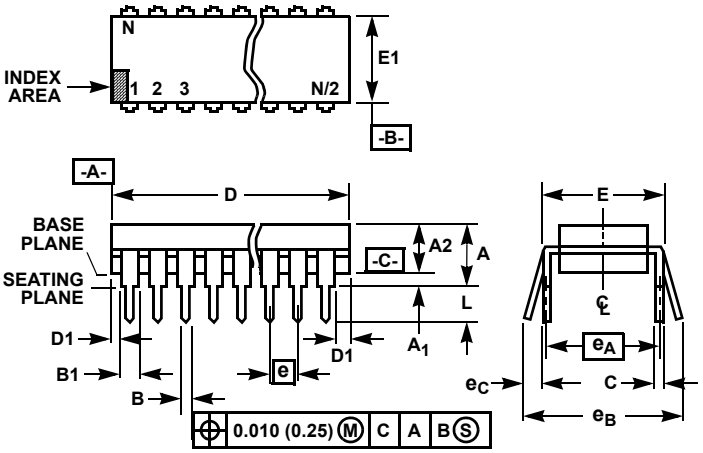


TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensioning and tolerancing per ANSI Y14.5M-1994.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.

Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E8.3 (JEDEC MS-001-BA ISSUE D)
8 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.355	0.400	9.01	10.16	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	8		8		9

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