NP180N055TUJ

MOS FIELD EFFECT TRANSISTOR

R07DS0181EJ0100
Rev.1.00
Dec 22, 2010

Description

The NP180N055TUJ is N-channel MOS Field Effect Transistor designed for high current switching applications.

Features

- Low on-state resistance
  — $R_{DS(on)}$ = 2.3 mΩ MAX. (V_{GS} = 10 V, I_D = 90 A)
- Low Ciss: Ciss = 9500 pF TYP. (V_{DS} = 25 V)
- Designed for automotive application and AEC-Q101 qualified

Ordering Information

Part No.	Lead Plating	Packing	Package
NP180N055TUJ-E1-AY *1	Pure Sn (Tin)	Tape 800 p/reel	TO-263-7pin, Taping (E1 type)
NP180N055TUJ-E2-AY *1			TO-263-7pin, Taping (E2 type)

Note: *1. Pb-free (This product does not contain Pb in the external electrode.)

Absolute Maximum Ratings (T_A = 25°C)

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	55	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±20	V
Drain Current (DC) (T_C = 25°C)	$I_{D(DC)}$	±180	A
Drain Current (pulse) *1	$I_{D(pulse)}$	±720	A
Total Power Dissipation (T_C = 25°C)	P_{T1}	348	W
Total Power Dissipation (T_A = 25°C) *2	P_{T2}	1.8	W
Channel Temperature	T_{ch}	175	°C
Storage Temperature	T_{stg}	–55 to +175	°C
Repetitive Avalanche Current *3	I_{AR}	66	A
Repetitive Avalanche Energy *3	E_{AR}	435	mJ

Thermal Resistance

Channel to Case Thermal Resistance	$R_{th(ch-C)}$	0.43	°C/W
Channel to Ambient Thermal Resistance *2	$R_{th(ch-A)}$	83.3	°C/W

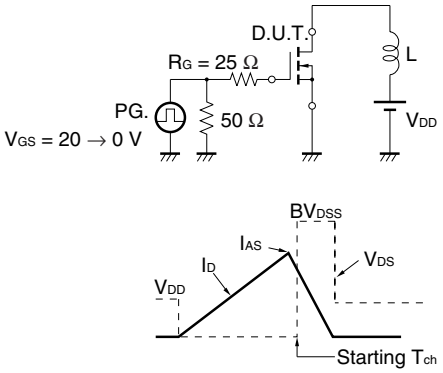
Notes: *1. T_C = 25°C, PW ≤ 10 μs, Duty Cycle ≤ 1%
*2. Mounted on glass epoxy substrate of 40 mm x 40 mm x 0.8 mmt
*3. $T_{ch(peak)}$ ≤ 150°C, R_G = 25 Ω

Electrical Characteristics (T_A = 25°C)

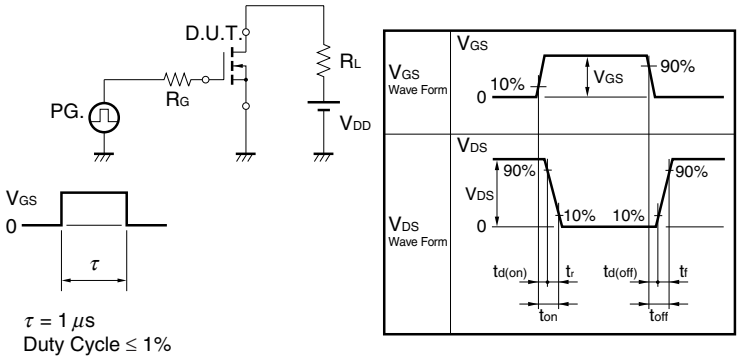
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I_{DSS}			1	μA	V_{DS} = 55 V, V_{GS} = 0 V
Gate Leakage Current	I_{GSS}			±100	nA	V_{GS} = ±20 V, V_{DS} = 0 V
Gate to Source Threshold Voltage	$V_{GS(th)}$	2.0	3.0	4.0	V	V_{DS} = V_{GS}, I_D = 250 μA
Forward Transfer Admittance *1	$\|y_{fs}\|$	65	130		S	V_{DS} = 5 V, I_D = 90 A
Drain to Source On-state Resistance *1	$R_{DS(on)}$		1.7	2.3	mΩ	V_{GS} = 10 V, I_D = 90 A
Input Capacitance	C_{iss}		9500	14250	pF	V_{DS} = 25 V,
Output Capacitance	C_{oss}		1060	1590	pF	V_{GS} = 0 V,
Reverse Transfer Capacitance	C_{rss}		320	580	pF	f = 1 MHz
Turn-on Delay Time	$t_{d(on)}$		45	100	ns	V_{DD} = 28 V, I_D = 90 A,
Rise Time	t_r		20	50	ns	V_{GS} = 10 V,
Turn-off Delay Time	$t_{d(off)}$		100	200	ns	R_G = 0 Ω
Fall Time	t_f		10	30	ns	
Total Gate Charge	Q_G		150	230	nC	V_{DD} = 44 V,
Gate to Source Charge	Q_{GS}		35		nC	V_{GS} = 10 V,
Gate to Drain Charge	Q_{GD}		45		nC	I_D = 180 A
Body Diode Forward Voltage *1	$V_{F(S-D)}$		0.9	1.5	V	I_F = 180 A, V_{GS} = 0 V
Reverse Recovery Time	t_{rr}		64		ns	I_F = 180 A, V_{GS} = 0 V,
Reverse Recovery Charge	Q_{rr}		138		nC	di/dt = 100 A/μs

Note: *1. Pulsed

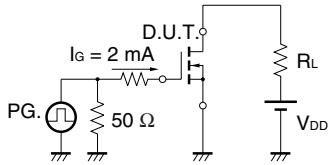
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

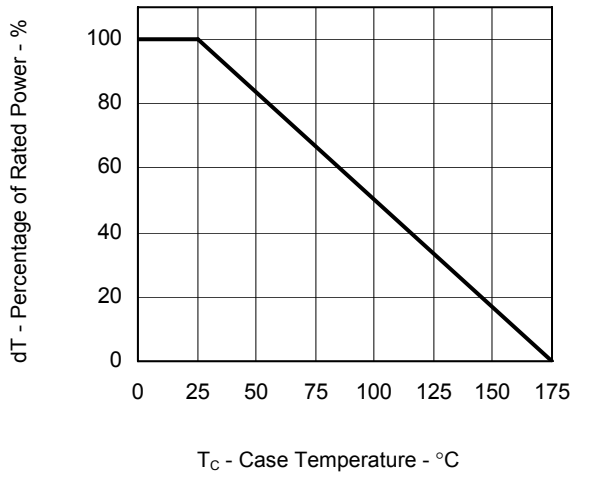


TEST CIRCUIT 3 GATE CHARGE

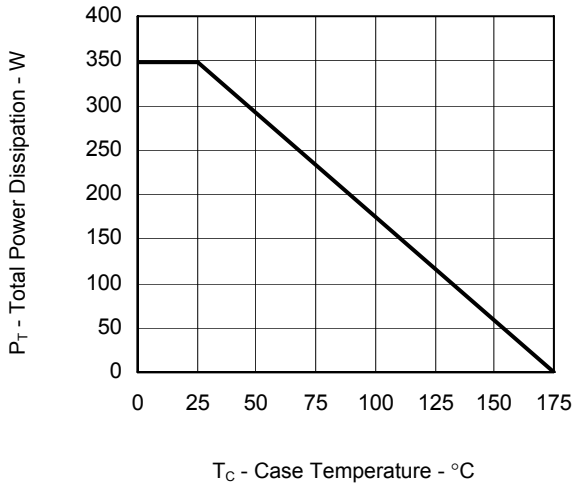


Typical Characteristics (T_A = 25°C)

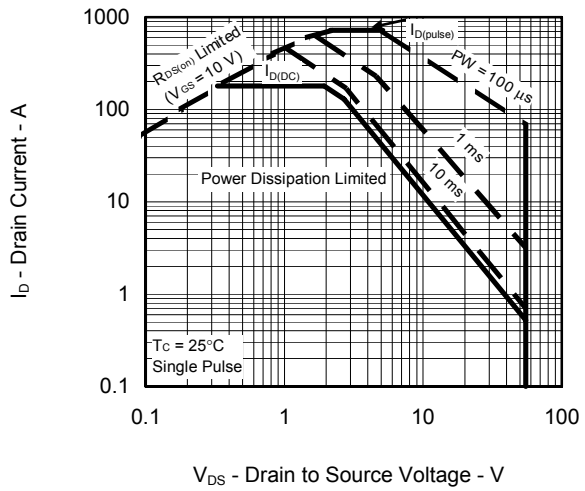
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



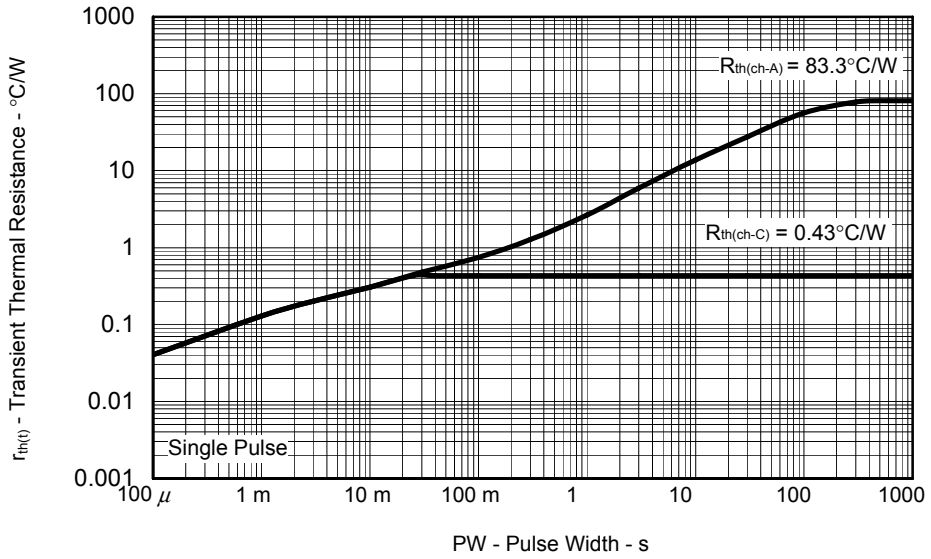
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



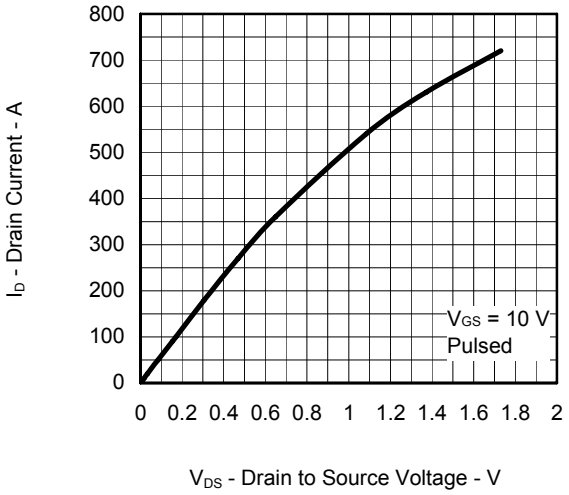
FORWARD BIAS SAFE OPERATING AREA



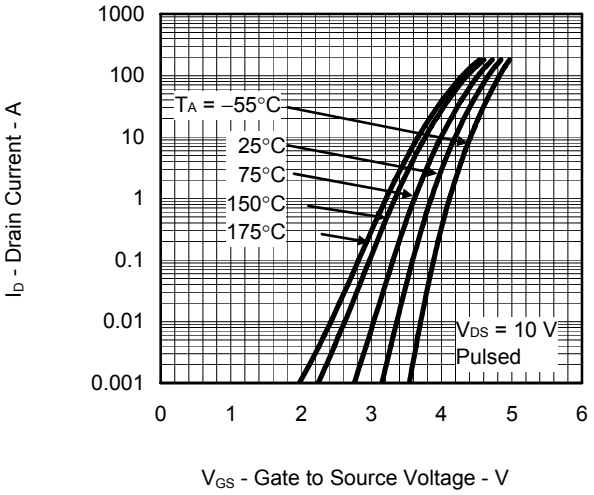
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



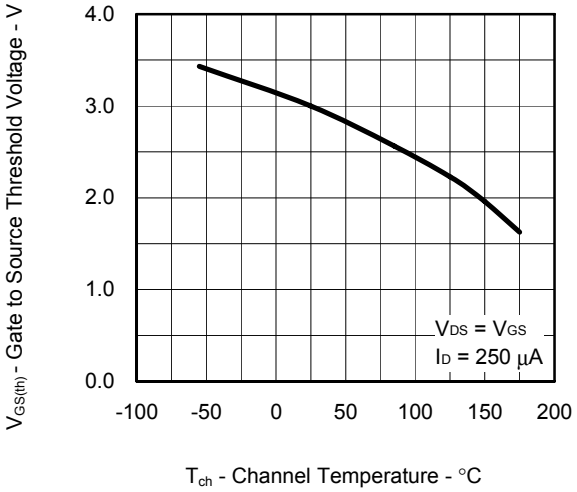
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



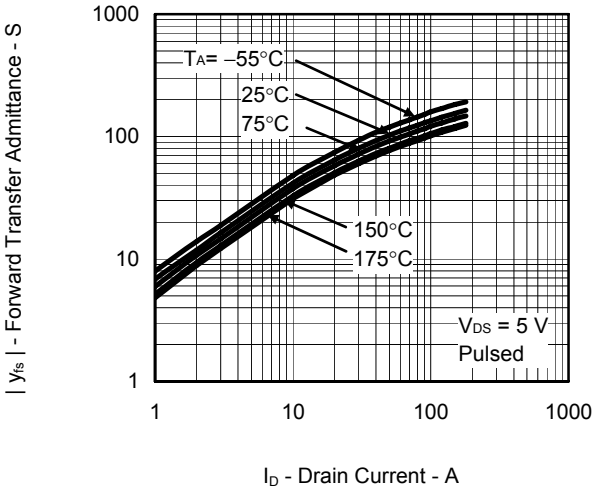
FORWARD TRANSFER CHARACTERISTICS



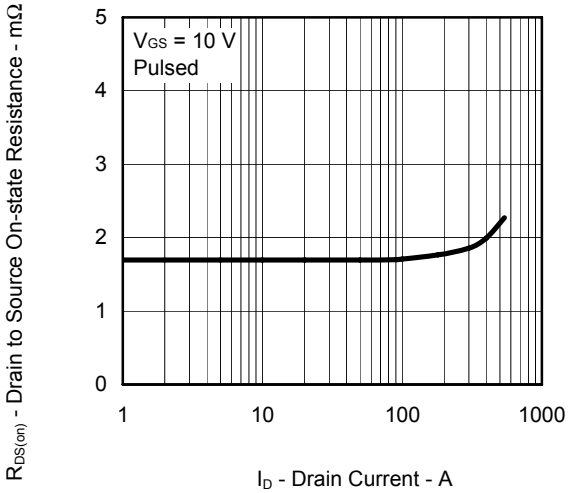
GATE TO SOURCE THRESHOLD VOLTAGE
vs. CHANNEL TEMPERATURE



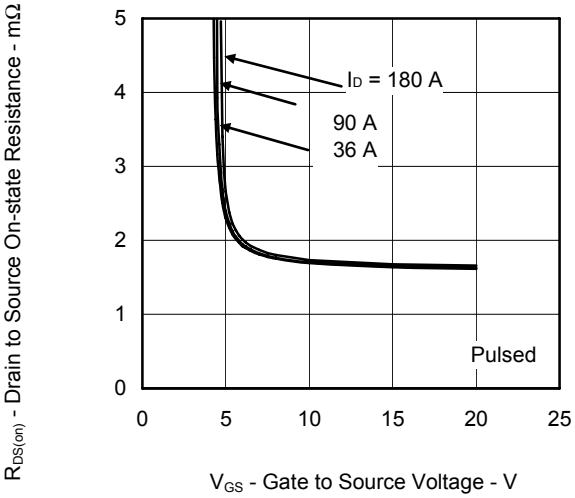
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



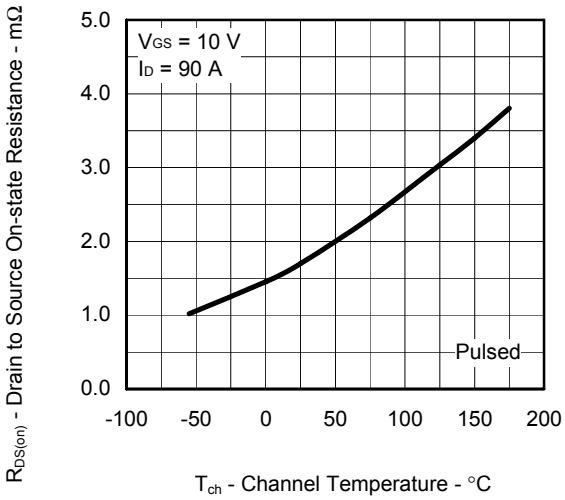
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



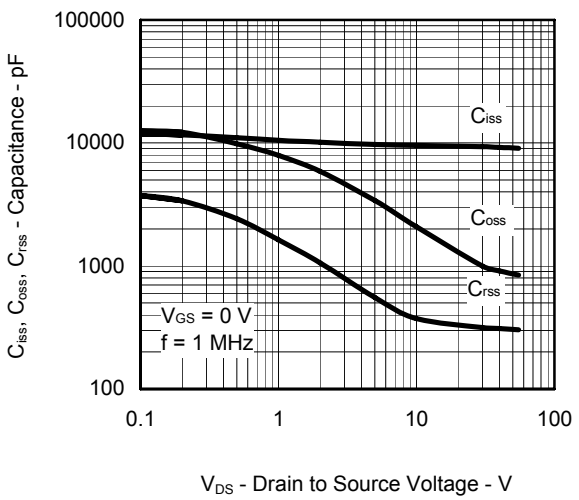
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



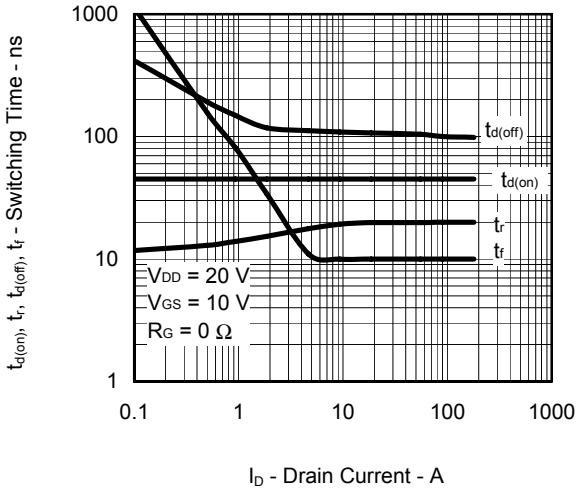
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



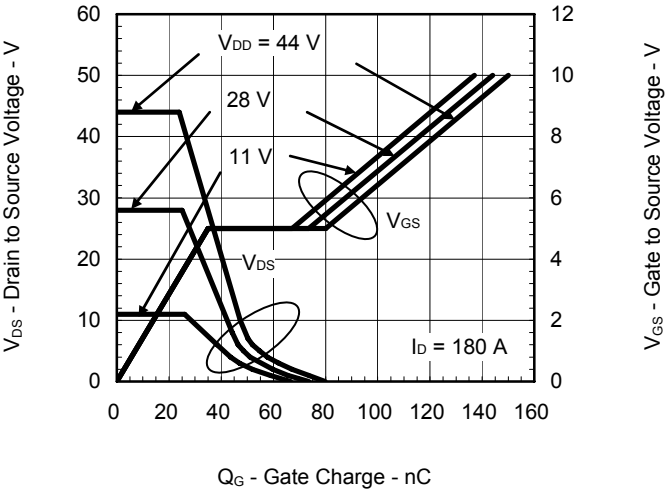
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



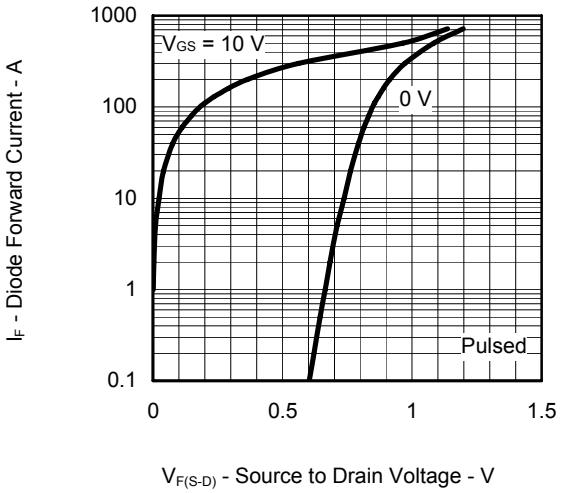
SWITCHING CHARACTERISTICS



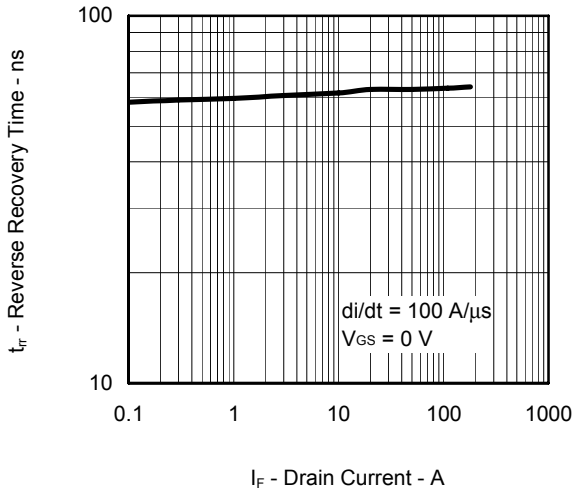
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

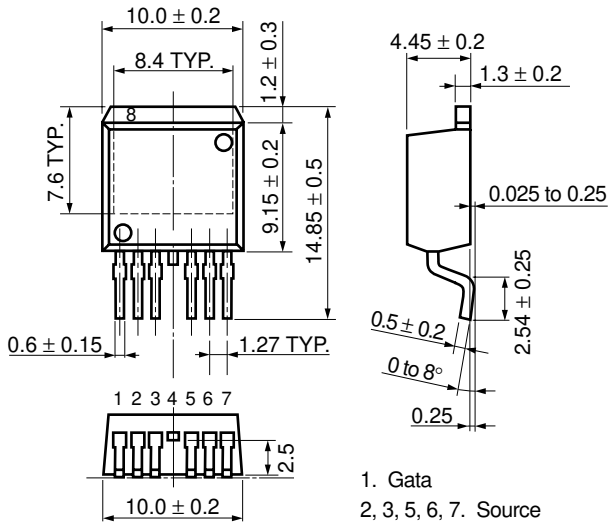


REVERSE RECOVERY TIME vs. DRAIN CURRENT



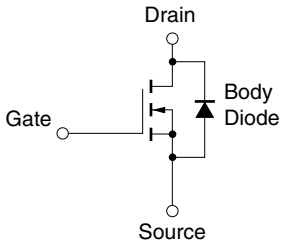
Package Drawings (Unit: mm)

TO-263-7pin (MP-25ZT) (Mass: 1.5 g TYP.)



1. Gata
2, 3, 5, 6, 7. Source
4, 8. Fin (Drain)

Equivalent Circuit



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

Revision History	NP180N055TUJ Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	Dec 22, 2010	–	First Edition Issued

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