X9319

Digitally Controlled Potentiometer (XDCP™)

FN8185
Rev 3.00
July 31, 2014

The Intersil X9319 is a digitally controlled potentiometer (XDCP). The device consists of a resistor array, wiper switches, a control section, and nonvolatile memory. The wiper position is controlled by a 3-wire interface.

The potentiometer is implemented by a resistor array composed of 99 resistive elements and a wiper switching network. Between each element and at either end are tap points accessible to the wiper terminal. The position of the wiper element is controlled by the $\overline{CS}$, U/$\overline{D}$, and $\overline{INC}$ inputs. The position of the wiper can be stored in nonvolatile memory and then be recalled upon a subsequent power-up operation.

The device can be used as a three-terminal potentiometer for voltage control or as a two-terminal variable resistor for current control in a wide variety of applications.

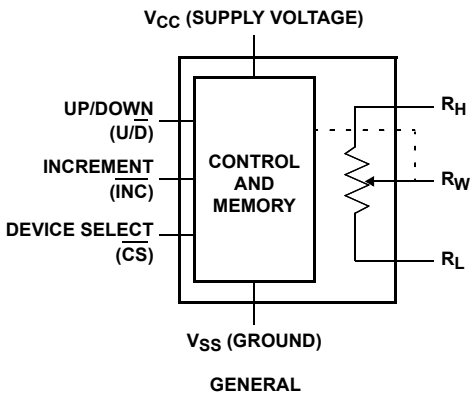
Applications

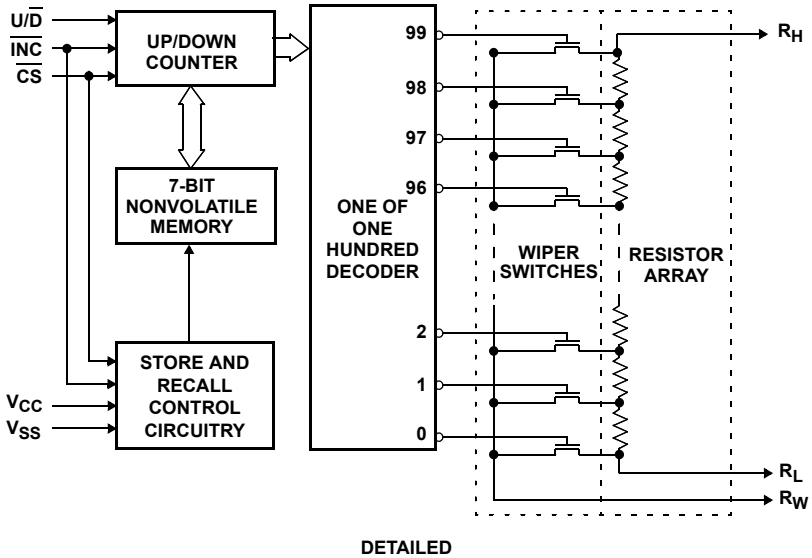
- LCD bias control
- DC bias adjustment
- Gain and offset trim
- Laser diode bias control
- Voltage regulator output control

Features

- Solid-state potentiometer
- 3-wire serial interface
- Terminal voltage, 0 to +10V
- 100 wiper tap points
  - Wiper position stored in nonvolatile memory and recalled on power-up
- 99 resistive elements
  - Temperature compensated
  - End-to-end resistance range ±20%
- Low power CMOS
  - V_{CC} = 5V
  - Active current, 3mA max.
  - Standby current, 1mA max.
- High reliability
  - Endurance, 100,000 data changes per bit
  - Register data retention, 100 years
- R_{TOTAL} value = 10kΩ
- Package
  - 8 Ld SOIC
- Pb-free (RoHS compliant)

Block Diagram





Ordering Information

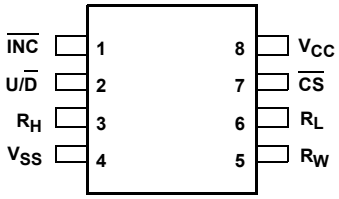
PART NUMBER (Notes 1, 2, 3)	PART MARKING	R_{TOTAL} (kΩ)	TEMP RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
X9319WS8Z	X9319W Z	10	0 to +70	8 Ld SOIC (150 mil)	M8.15E
X9319WS8IZ	X9319W ZI		-40 to +85	8 Ld SOIC (150 mil)	M8.15E

NOTES:

1. Add "T1" suffix for tape and reel.
2. Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. **For Moisture Sensitivity Level (MSL), please see product information page for X9319. For more information on MSL, please see tech brief TB363.**

Pin Configuration

X9319
(8 LD SOIC)
TOP VIEW



Pin Descriptions

SOIC	SYMBOL	BRIEF DESCRIPTION
1	$\overline{INC}$	**Increment**. Toggling $\overline{INC}$ while $\overline{CS}$ is low moves the wiper either up or down.
2	U/$\overline{D}$	**Up/Down**. The U/$\overline{D}$ input controls the direction of the wiper movement.
3	R_H	The high terminal is equivalent to one of the fixed terminals of a mechanical potentiometer.
4	V_{SS}	Ground.
5	R_W	The wiper terminal is equivalent to the movable terminal of a mechanical potentiometer.
6	R_L	The low terminal is equivalent to one of the fixed terminals of a mechanical potentiometer.
7	$\overline{CS}$	**Chip Select**. The device is selected when the $\overline{CS}$ input is LOW, and deselected when $\overline{CS}$ is high.
8	V_{CC}	Supply Voltage.

Absolute Maximum Ratings

Voltage on $\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ and V_{CC} with respect to V_{SS}. . . . -1V to +7V
R_H, R_W, R_L to ground . . . . . +12V
I_W (10s) . . . . . ±6mA

Thermal Information

Junction Temperature under bias . . . . . -65°C to +135°C
Storage Temperature . . . . . -65°C to +150°C
Pb-Free Reflow Profile. . . . . see TB493

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

Potentiometer Characteristics

V_{CC} = 5V ±10%. **Boldface limits apply across the operating temperature range, -40°C to +85°C (Industrial) and 0°C to +70°C (Commercial).**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 7)	TYP (Note 8)	MAX (Note 7)	UNIT
	End-to-end resistance tolerance	See ordering information for values	**-20**		**+20**	%
V_{RH}/R_L	R_H/R_L terminal voltage	V_{SS} = 0V	**V_{SS}**		**10**	V
	Power rating				**25**	mW
R_W	Wiper resistance	I_W = 1mA		40	**200**	W
I_W	Wiper current (Note 9)	See test circuit	**-3.0**		**+3.0**	mA
	Noise (Note 11)	Ref: 1kHz		-120		dBV
	Resolution			1		%
	Absolute linearity (Note 4)	V(RH) = 10V, V(RL) = 0V	**-1**		**+1**	MI (Note 6)
	Relative linearity (Note 5)		**-0.2**		**+0.2**	MI (Note 6)
	R_{TOTAL} temperature coefficient (Note 9)			±300		ppm/°C
	Ratiometric temperature coefficient (Notes 9, 10)		**-20**		**+20**	ppm/°C
$C_H/C_L/C_W$ (Note 9)	Potentiometer capacitances	See "Equivalent Circuit" on page 4		10/10/25		pF
V_{CC}	Supply Voltage		**4.5**		**5.5**	V

D.C. Operating Characteristics

V_{CC} = 5V ±10%. **Boldface limits apply across the operating temperature range, -40°C to +85°C (Industrial) and 0°C to +70°C (Commercial).**

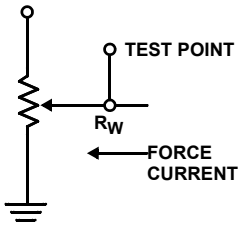
SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 7)	TYP (Note 8)	MAX (Note 7)	UNIT
I_{CC}	V_{CC} active current (Increment)	$\overline{CS}$ = V_{IL}, U/$\overline{D}$ = V_{IL} or V_{IH} and $\overline{INC}$ = 0.4V/2.4V at min. t_{CYC} R_L, R_H, R_W not connected		1	3	mA
I_{SB}	Standby supply current	$\overline{CS} \geq$ 2.4V, U/$\overline{D}$ and $\overline{INC}$ = 0.4V R_L, R_H, R_W not connected		300	1000	µA
I_{LI}	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ input leakage current	V_{IN} = V_{SS} to V_{CC}	-10		+10	µA
V_{IH}	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ input HIGH voltage		2		V_{CC} + 1	V
V_{IL}	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ input LOW voltage		-1		0.8	V
C_{IN} (Note 9)	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ input capacitance	V_{CC} = 5V, V_{IN} = V_{SS}, T_A = +25°C, f = 1MHz			10	pF

Endurance and Data Retention

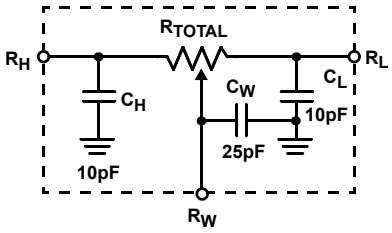
V_{CC} = 5V ±10%, T_A = Full Operating Temperature Range

PARAMETER	MIN	UNIT
Minimum endurance	100,000	Data changes per bit
Data retention	100	Years

Test Circuit



Equivalent Circuit



AC Conditions of Test

Input pulse levels	0.8V to 2V
Input rise and fall times	10ns
Input reference levels	1.4V

A.C. Operating Characteristics

V_{CC} = 5V ±10%. **Boldface limits apply across the operating temperature range, -40°C to +85°C (Industrial) and 0°C to +70°C (Commercial).**

SYMBOL	PARAMETER	MIN (Note 7)	TYP (Note 8)	MAX (Note 7)	UNIT
t_{CI}	$\overline{CS}$ to $\overline{INC}$ setup	100			ns
t_{ID} (Note 9)	$\overline{INC}$ HIGH to U/$\overline{D}$ change	100			ns
t_{DI} (Note 9)	U/$\overline{D}$ to $\overline{INC}$ setup	1			µs
t_{IL}	$\overline{INC}$ LOW period	1			µs
t_{IH}	$\overline{INC}$ HIGH period	1			µs
t_{IC}	$\overline{INC}$ inactive to $\overline{CS}$ inactive	1			µs
t_{CPHS}	$\overline{CS}$ deselect time (STORE)	20			ms
t_{CPHNS} (Note 9)	$\overline{CS}$ deselect time (NO STORE)	1			µs
t_{IW} (Note 9)	$\overline{INC}$ to R_W change		100	500	µs
t_{CYC}	$\overline{INC}$ cycle time	4			µs
t_R, t_F (Note 9)	$\overline{INC}$ input rise and fall time			500	µs
t_{PU} (Note 9)	Power-up to wiper stable			500	µs
t_R V_{CC} (Note 9)	V_{CC} power-up rate	0.2		50	V/ms

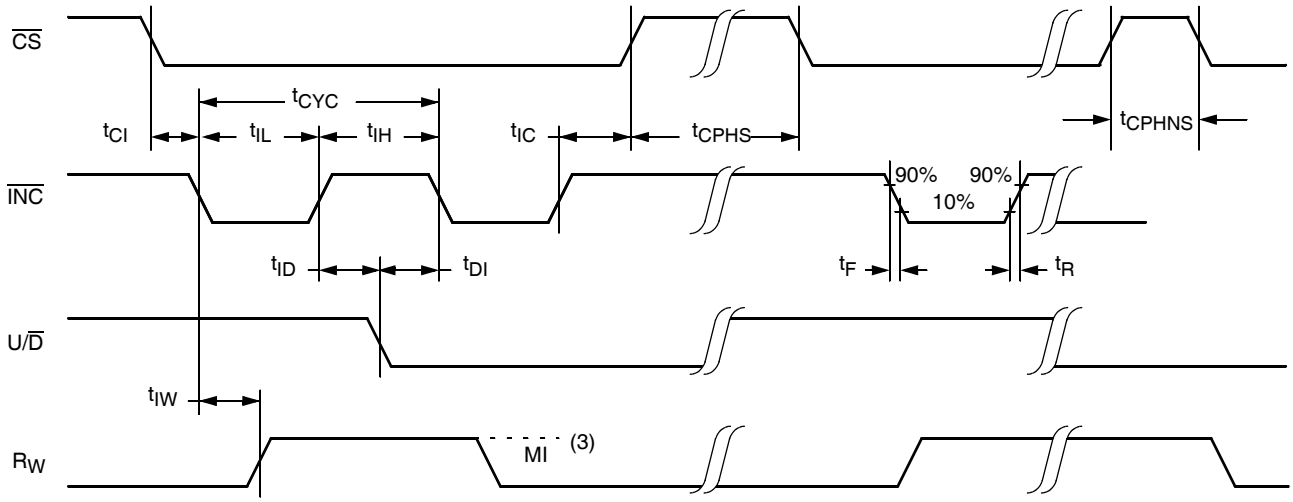
NOTES:

4. Absolute linearity is utilized to determine actual wiper voltage versus expected voltage = $[V(R_{W(n)(actual)}) - V(R_{W(n)(expected)})]/MI$ $V(R_{W(n)(expected)}) = n(V(R_H) - V(R_L))/99 + V(R_L)$, with n from 0 to 99.
5. Relative linearity is a measure of the error in step size between taps = $[V(R_{W(n+1)}) - (V(R_{W(n)}) - MI)]/MI$.
6. 1 MI = Minimum Increment = $[V(R_H) - V(R_L)]/99$.
7. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
8. Typical values are for T_A = +25°C and nominal supply voltage.
9. Guaranteed by device characterization.
10. Ratiometric temperature coefficient = $(V(R_W)_{T1(n)} - V(R_W)_{T2(n)})/[V(R_W)_{T1(n)}(T1 - T2) \times 10^6]$, with T1 and T2 being 2 temperatures, and n from 0 to 99.
11. Measured with wiper at tap position 31, R_L grounded, using test circuit.

Power-Up and Down Requirements

In order to prevent unwanted tap position changes, or an inadvertent store, bring the $\overline{CS}$ and $\overline{INC}$ high before or concurrently with the V_{CC} pin on power-up. The potentiometer voltages must be applied after this sequence is completed. During power-up, the data sheet parameters for the DCP do not fully apply until 1 millisecond after V_{CC} reaches its final value. The V_{CC} ramp spec is always in effect.

A.C. Timing



Pin Descriptions

R_H and R_L

The high (R_H) and low (R_L) terminals of the X9319 are equivalent to the fixed terminals of a mechanical potentiometer. The terminology of R_L and R_H references the relative position of the terminal in relation to wiper movement direction selected by the U/$\overline{D}$ input and not the voltage potential on the terminal.

R_W

R_W is the wiper terminal and is equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the control inputs. The wiper terminal series resistance is typically 40Ω.

Up/Down (U/$\overline{D}$)

The U/$\overline{D}$ input controls the direction of the wiper movement and whether the counter is incremented or decremented.

Increment ($\overline{INC}$)

The $\overline{INC}$ input is negative-edge triggered. Toggling $\overline{INC}$ will move the wiper and either increment or decrement the counter in the direction indicated by the logic level on the U/$\overline{D}$ input.

Chip Select ($\overline{CS}$)

The device is selected when the $\overline{CS}$ input is LOW. The current counter value is stored in nonvolatile memory when $\overline{CS}$ is returned HIGH while the $\overline{INC}$ input is also HIGH. After the store operation is complete the X9319 will be placed in the low power standby mode until the device is selected once again.

Principles of Operation

There are three sections of the X9319: the control section, the nonvolatile memory, and the resistor array. The control section operates just like an up/down counter. The output of this counter is decoded to turn on a single electronic switch connecting a point on the resistor array to the wiper output.

The contents of the counter can be stored in nonvolatile memory and retained for future use. The resistor array is comprised of 99 individual resistors connected in series. Electronic switches at either end of the array and between each resistor provide an electrical connection to the wiper pin, R_W.

The wiper acts like its mechanical equivalent and does not move beyond the first or last position. That is, the counter does not wrap around when clocked to either extreme.

The electronic switches on the device operate in a “make-before-break” mode when the wiper changes tap positions. If the wiper is moved several positions, multiple taps are connected to the wiper for t_{IW} ($\overline{INC}$ to V_W change). The R_{TOTAL} value for the device can temporarily be reduced by a significant amount if the wiper is moved several positions.

When the device is powered down, the last wiper position stored will be maintained in the nonvolatile memory. When power is restored, the contents of the memory are recalled and the wiper is set to the value last stored.

Instructions and Programming

The $\overline{INC}$, U/$\overline{D}$ and $\overline{CS}$ inputs control the movement of the wiper along the resistor array. With $\overline{CS}$ set LOW, the device is selected and enabled to respond to the U/$\overline{D}$ and $\overline{INC}$ inputs. HIGH-to-LOW transitions on $\overline{INC}$ will increment or decrement (depending on the state of the U/$\overline{D}$ input) the seven bit counter. The output of this counter is decoded to select one of one hundred wiper positions along the resistive array.

The value of the counter is stored in nonvolatile memory whenever $\overline{CS}$ transitions HIGH while the $\overline{INC}$ input is also HIGH.

The system may select the X9319, move the wiper and deselect the device without having to store the latest wiper position in nonvolatile memory. After the wiper movement is

performed as described above and once the new position is reached, the system must keep $\overline{INC}$ LOW while taking $\overline{CS}$ HIGH. The new wiper position will be maintained until changed by the system or until a power-up/down cycle recalled the previously stored data. This procedure allows the system to always power-up to a preset value stored in nonvolatile memory; then during system operation minor adjustments could be made. The adjustments might be based on user preference, system parameter changes due to temperature drift, etc.

The state of U/$\overline{D}$ may be changed while $\overline{CS}$ remains LOW. This allows the host system to enable the device and then move the wiper up and down until the proper trim is attained.

Mode Selection

$\overline{CS}$	$\overline{INC}$	U/$\overline{D}$	MODE
L	↘	H	Wiper up
L	↘	L	Wiper down

Mode Selection (Continued)

$\overline{CS}$	$\overline{INC}$	U/$\overline{D}$	MODE
↗	H	X	Store wiper position to nonvolatile memory
H	X	X	Standby
↗	L	X	No store, return to standby
↘	L	H	Wiper Up (not recommended)
↘	L	L	Wiper Down (not recommended)

Applications Information

Electronic digitally controlled (XDCP) potentiometers provide three powerful application advantages:

1. The variability and reliability of a solid-state potentiometer
2. The flexibility of computer-based digital controls
3. The retentivity of nonvolatile memory used for the storage of multiple potentiometer settings or data.

Basic Configurations of Electronic Potentiometers

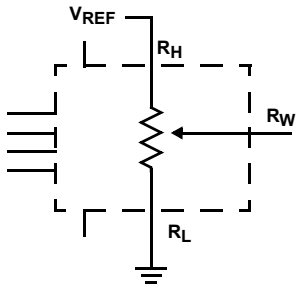


FIGURE 1. THREE TERMINAL POTENTIOMETER; VARIABLE VOLTAGE DIVIDER

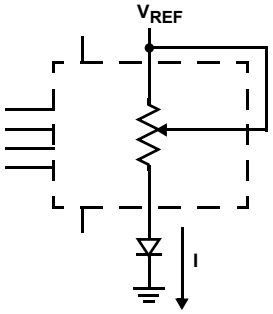


FIGURE 2. TWO TERMINAL VARIABLE RESISTOR; VARIABLE CURRENT

Basic Circuits

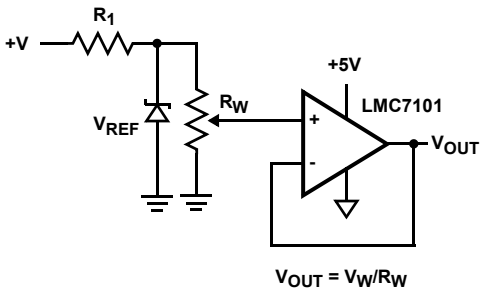


FIGURE 3. BUFFERED REFERENCE VOLTAGE

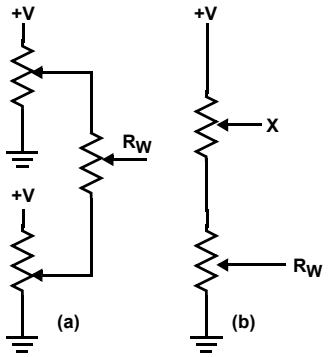


FIGURE 4. CASCADING TECHNIQUES

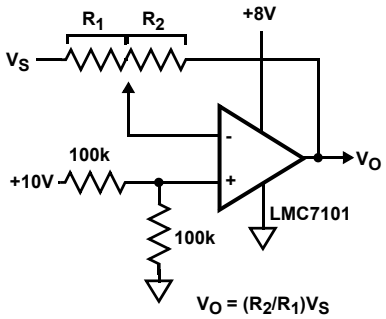
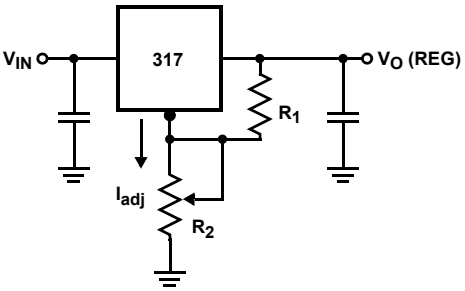


FIGURE 5. SINGLE SUPPLY INVERTING AMPLIFIER

Basic Circuits (Continued)



V_O (REG) = 1.25V (1+R_2/R_1)+I_{adj} R_2

FIGURE 6. VOLTAGE REGULATOR

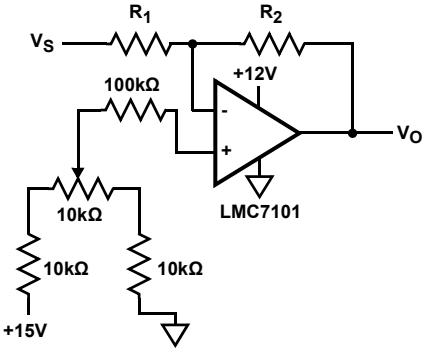
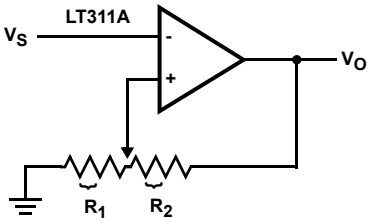


FIGURE 7. OFFSET VOLTAGE ADJUSTMENT



V_{UL} = {R_1/(R_1+R_2)} V_O(max)
V_{LL} = {R_1/(R_1+R_2)} V_O(min)

FIGURE 8. COMPARATOR WITH HYSTERESIS

© Copyright Intersil Americas LLC 2005-2014. All Rights Reserved.
All trademarks and registered trademarks are the property of their respective owners.

For additional products, see www.intersil.com/en/products.html

Intersil products are manufactured, assembled and tested utilizing ISO9001 quality systems as noted in the quality certifications found at www.intersil.com/en/support/qualandreliability.html

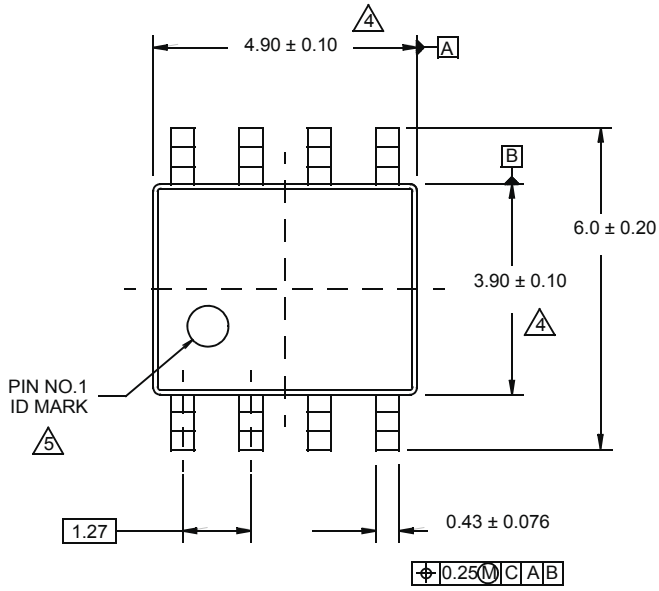
Intersil products are sold by description only. Intersil may modify the circuit design and/or specifications of products at any time without notice, provided that such modification does not, in Intersil's sole judgment, affect the form, fit or function of the product. Accordingly, the reader is cautioned to verify that datasheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com

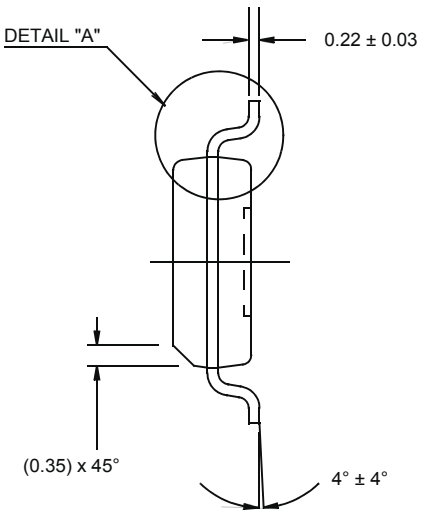
Package Outline Drawing

M8.15E

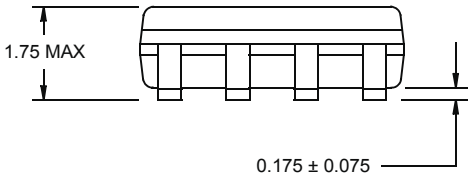
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE
Rev 0, 08/09



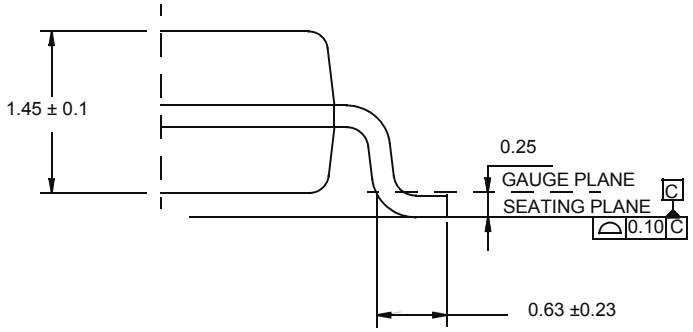
TOP VIEW



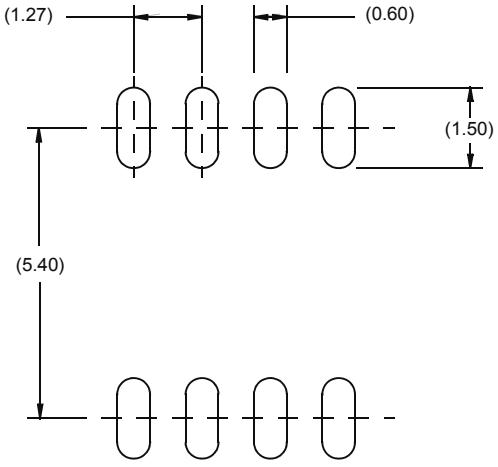
SIDE VIEW "B"



SIDE VIEW "A"



DETAIL "A"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. Reference to JEDEC MS-012.