ISL6140, ISL6150

Negative Voltage Hot Plug Controller

FN9039
Rev 5.00
December 3, 2015

The ISL6140 is an 8 Ld, negative voltage hot plug controller that allows a board to be safely inserted and removed from a live backplane. Inrush current is limited to a programmable value by controlling the gate voltage of an external N-channel pass transistor. The pass transistor is turned off if the input voltage is less than the undervoltage threshold, or greater than the overvoltage threshold. A programmable electronic circuit breaker protects the system against shorts. The active low $\overline{\text{PWRGD}}$ signal can be used to directly enable a power module (with a low enable input)

The ISL6150 is the same part, but with an active high PWRGD signal.

Features

- Low Side External NFET Switch
- Operates from -10V to -80V (-100V absolute max rating) or +10V to +80V (+100V absolute max rating)
- Programmable Inrush Current
- Programmable Electronic Circuit Breaker (overcurrent shutdown)
- Programmable Overvoltage Protection
- Programmable Undervoltage Lockout
- Power Good Control Output
  - $\overline{\text{PWRGD}}$ Active High: (H Version) ISL6150
  - $\overline{\text{PWRGD}}$ active Low: (L Version) ISL6140
- Pb-free available (RoHS compliant)

Applications

- VoIP (Voice over Internet Protocol) Servers
- Telecom systems at -48V
- Negative Power Supply Control
- +24V Wireless Base Station Power

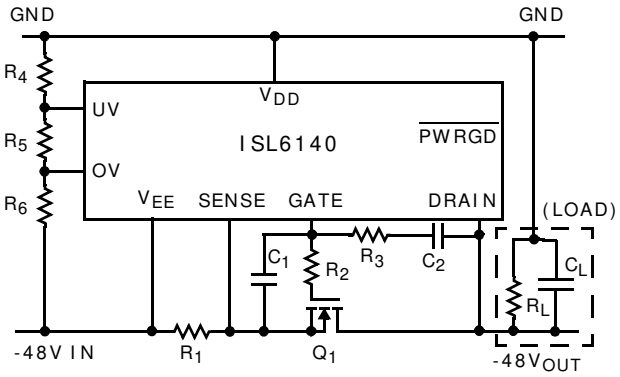
Related Literature

- ISL6140/50EVAL1 Board Set, AN9967
- ISL6116 Hot Plug Controller, FN9100

NOTE: See www.intersil.com/hotplug for more information.

Typical Application

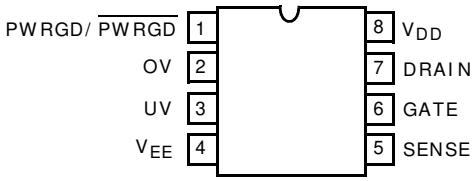
NOTE: (RL and CL are the Load)



R_5 = 9.09kΩ (1%)	R_4 = 562kΩ (1%)
R_6 = 10kΩ (1%)	C_2 = 3.3nF (100V)
C_1 = 150nF (25V)	Q_1 = IRF530 (100V, 17A, 0.11Ω)
R_2 = 10Ω (5%)	R_1 = 0.02Ω (1%)
R_3 = 18kΩ (5%)	C_L = 100µF (100V)

Pin Configuration

ISL6140, ISL6150
(8 LD SOIC)
TOP VIEW



ISL6140 has active Low (L version) $\overline{\text{PWRGD}}$ output pin

ISL6150 has active High (H version) PWRGD output pin

Ordering Information

PART NUMBER (Notes 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL6140CBZ	ISL61 40CBZ	0 to +70	8 Ld SOIC (Pb-Free)	M8.15
ISL6140CBZ-T (Note 1)	ISL61 40CBZ	0 to +70	8 Ld SOIC (Pb-Free)	M8.15
ISL6140IBZ-T (Note 1)	ISL61 40IBZ	-40 to +85	8 Ld SOIC (Pb-Free)	M8.15
ISL6140IBZ	ISL61 40IBZ	-40 to +85	8 Ld SOIC (Pb-Free)	M8.15
ISL6150CB No longer available or supported, recommended replacement: ISL6150CBZ	ISL 6150CB	0 to +70	8 Ld SOIC (Pb-Free)	M8.15
ISL6150CBZ	ISL61 50CBZ	0 to +70	8 Ld SOIC (Pb-Free)	M8.15
ISL6150CBZ-T (Note 1)	ISL61 50CBZ	0 to +70	8 Ld SOIC (Pb-Free)	M8.15
ISL6150IB-T No longer available or supported, recommended replacement: ISL6150IBZ-T	ISL 6150IB	-40 to +85	8 Ld SOIC (Pb-Free)	M8.15
ISL6150IBZ	ISL61 50IBZ	-40 to +85	8 Ld SOIC (Pb-Free)	M8.15
ISL6150IBZ-T (Note 1)	ISL61 50IBZ	-40 to +85	8 Ld SOIC (Pb-Free)	M8.15

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page forISL6140. For more information on MSL please see techbrief TB363.

Pin Description

$\overline{\text{PWRGD}}$ (ISL6140; L Version) Pin 1

This digital output is an open-drain pull-down device. The Power Good comparator looks at the DRAIN pin voltage compared to the internal VPG reference (VPG is nominal 1.7V); this essentially measures the voltage drop across the external FET and sense resistor. If the voltage drop is small (<1.7V is normal), the $\overline{\text{PWRGD}}$ pin pulls low (to VEE); this can be used as an active low enable for an external module. If the voltage drop is too large (>1.7V indicates some kind of short or overload condition), the pull-down device shuts off, and the pin becomes high impedance. Typically, an external pull-up of some kind is used to pull the pin high (many brick regulators have a pull-up function built in).

PWRGD (ISL6150; H Version) Pin 1

This digital output is a variation of an open-drain pull-down device. The power good comparator is the same as described above, but the polarity of the output is reversed, as follows:

If the voltage drop across the FET is too large (>1.7V), the open drain pull-down device will turn on, and sink current to the DRAIN pin. If the voltage drop is small (<1.7V), a 2nd pull-down device in series with a 6.2k resistor (nominal) sinks current to V_{EE}; if the external pull-up current is low enough (<1mA, for example), the voltage drop across the resistor will be big enough to look like a logic high signal (in this example, 1mA*6.2kΩ = 6.2V). This pin can thus be used as an active high enable signal for an external module.

Note that for both versions, although this is a digital pin functionally, the logic high level is determined by the external pull-up device, and the power supply to which it is connected; the IC will not clamp it below the V_{DD} voltage. Therefore, if the external device does not have its own clamp, or if it would be damaged by a high voltage, then an external clamp might be necessary.

OV (OVERVOLTAGE) Pin 2

This analog input compares the voltage on the pin to an internal voltage reference (nominal 1.223V). When the input goes above the reference (low to high transition), that signifies an OV (overvoltage) condition, and the GATE pin is immediately pulled low to shut off the external FET. Since there is 20mV of nominal hysteresis built in, the GATE will remain off until the OV pin drops below a 1.203V (nominal) high to low threshold. A typical application will use an external resistor divider from V_{DD} to V_{EE}, to set the OV level as desired; a three-resistor divider can set both OV and UV.

UV (Undervoltage) Pin 3

This analog input compares the voltage on the pin to an internal voltage reference (nominal 1.223V). When the input goes below the reference (high to low transition), that signifies an UV (Under-Voltage) condition, and the GATE pin is immediately pulled low to shut off the external FET. Since there is 20mV of nominal hysteresis built in, the GATE will remain off until the UV pin rises above a 1.243V (nominal) low to high threshold. A typical application will use an external resistor divider from V_{DD} to V_{EE}, to set the UV level as desired; a three-resistor divider can set both OV and UV.

If there is an overcurrent condition, the GATE pin is latched off, and the UV pin is then used to reset the overcurrent latch; the pin must be externally pulled below its trip point, and brought back up (toggled) in order to turn the GATE back on (assuming the fault condition has disappeared).

V_{EE} Pin 4

This is the most Negative Supply Voltage, such as in a -48V system. Most of the other signals are referenced relative to this pin, even though it may be far away from what is considered a GND reference.

SENSE Pin 5

This analog input measures the voltage drop across an external sense resistor (between SENSE and VEE), to determine if the current exceeds an overcurrent trip point, equal to nominal ($50mV/R_{SENSE}$). Noise spikes of less than 2µs are filtered out; if longer spikes need to be filtered, an additional RC time constant can be added to stretch the time (see Figure 29; note that the FET must be able to handle the high currents for the additional time). To disable the overcurrent function, connect the SENSE pin to V_{EE}.

GATE Pin 6

This analog output drives the gate of the external FET used as a pass transistor. The GATE pin is high (FET is on) when UV pin is high (above its trip point); the OV pin is low (below its trip point), and there is no overcurrent condition ($V_{SENSE} - V_{EE} < 50mV$). If any of the 3 conditions are violated, the GATE pin will be pulled low, to shut off the FET.

The Gate is driven high by a weak (-45µA nominal) pull-up current source, in order to slowly turn on the FET. It is driven low by a strong (32mA nominal) pull-down device, in order to shut off the FET very quickly in the event of an overcurrent or shorted condition.

DRAIN Pin 7

This analog input compares the voltage of the external FET DRAIN to the internal VPG reference (nominal 1.7V), for the Power Good function.

Note that the Power Good comparator does NOT turn off the GATE pin. However, whenever the GATE is turned off (by OV, UV or SENSE), the Power Good Comparator will usually then switch to the power-NOT-good state, since an off FET will have the supply voltage across it.

V_{DD} Pin 8

This is the most positive power supply pin. It can range from +10 to +80V (Relative to V_{EE}). If operation down near 10V is expected, the user should carefully choose a FET to match up with the reduced GATE voltage shown in the specification table.

Absolute Maximum Ratings

Supply Voltage (V_{DD} to V_{EE}) . . . . . -0.3V to 100V
DRAIN, PWRGD, PWRGD Voltage . . . . . -0.3V to 100V
UV, OV Input Voltage . . . . . -0.3V to 60V
SENSE, GATE Voltage . . . . . -0.3V to 20V
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7 . . .2000V

Thermal Information

Thermal Resistance (Typical, Note 4)	θ_{JA} (°C/W)
8 Lead SOIC	95

Maximum Junction Temperature (Plastic Package) . . +150°C
Maximum Storage Temperature Range . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Temperature Range (Industrial) . . . . . -40°C to +85°C
Temperature Range (Commercial) . . . . . 0°C to +70°C
Supply Voltage Range (Typical) . . . . . 36V to +72V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

V_{DD} = +48V, VEE = +0V Unless Otherwise Specified. All tests are over the full temperature range; either Commercial (0°C to +70°C) or Industrial (-40°C to +85°C). Typical specs are at +25°C. Boldface limits apply over the operating temperature range, -40°C to +85°C.

PARAMETER	SYMBOL	TEST CONDITIONS	TEST LEVEL OR NOTES	PART NUMBER OR GRADE MIN (Note 7)	TYP	MAX (Note 7)	UNITS
DC PARAMETRIC							
Supply Operating Range	V_{DD}			10	-	80	V
Supply Current	I_{DD}	UV = 3V; OV = V_{EE}; SENSE = V_{EE}; V_{DD} = 80V		0.6	0.9	1.3	mA
GATE PIN							
Gate Pin Pull-Up Current	I_{PU}	Gate Drive on, V_{GATE} = V_{EE}		-30	-45	-60	µA
Gate Pin Pull-Down Current	I_{PD}	Gate Drive off; any fault condition		24	32	70	mA
External Gate Drive	Δ-V_{GATE}	(V_{GATE} - V_{EE}), 17V ≤ V_{DD} ≤ 80V		10	14	15	V
		(V_{GATE} - V_{EE}), 10V ≤ V_{DD} ≤ 17V	5	5.4	6.2	15	V
SENSE PIN							
Circuit Breaker Trip Voltage	V_{CB}	V_{CB} = (V_{SENSE} - V_{EE})		40	50	60	mV
SENSE Pin Current	I_{SENSE}	V_{SENSE} = 50mV		-	0	-0.5	µA
UV PIN							
UV Pin High Threshold Voltage	V_{UVH}	UV Low to High Transition		1.213	1.243	1.272	V
UV Pin Low Threshold Voltage	V_{UVL}	UV High to Low Transition		1.198	1.223	1.247	V
UV Pin Hysteresis	V_{UVHY}			7	20	50	mV
UV Pin Input Current	I_{INUV}	V_{UV} = V_{EE}		-	-0.05	-0.5	µA
OV PIN							
OV Pin High Threshold Voltage	V_{OVH}	OV Low to High Transition		1.198	1.223	1.247	V
OV Pin Low Threshold Voltage	V_{OVL}	OV High to Low Transition		1.165	1.203	1.232	V
OV Pin Hysteresis	V_{OVHY}			7	20	50	mV
OV Pin Input Current	I_{INOV}	V_{OV} = V_{EE}		-	-0.05	-0.5	µA

Electrical Specifications

V_{DD} = +48V, VEE = +0V Unless Otherwise Specified. All tests are over the full temperature range; either Commercial (0°C to +70°C) or Industrial (-40°C to +85°C). Typical specs are at +25°C. Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	TEST LEVEL OR NOTES	PART NUMBER OR GRADE			UNITS
				MIN (Note 7)	TYP	MAX (Note 7)	
DRAIN PIN							
Power Good Threshold (L to H)	V_{PGLH}	V_{DRAIN} - V_{EE}, Low to High Transition		1.55	1.70	1.87	V
Power Good Threshold (H to L)	V_{PGHL}	V_{DRAIN} - V_{EE}, High to Low Transition		1.10	1.25	1.42	V
Power Good Threshold Hysteresis	V_{PGHY}			0.30	0.45	0.60	V
Drain Input Bias Current	I_{DRAIN}	V_{DRAIN} = 48V		10	35	60	µA
ISL6140 ($\overline{PWRGD}$ PIN: L VERSION)							
$\overline{PWRGD}$ Output Low Voltage	V_{OL}	(V_{DRAIN} - V_{EE}) < V_{PG} I_{OUT} = 1mA		-	0.28	0.50	V
		I_{OUT} = 3mA		-	0.88	1.20	
		I_{OUT} = 5mA		-	1.45	1.95	V
Output Leakage	I_{OH}	V_{DRAIN} = 48V, $V_{\overline{PWRGD}}$ = 80V		-	0.05	10	µA
ISL6150 (PWRGD PIN: H VERSION)							
PWRGD Output Low Voltage (PWRGD-DRAIN)	V_{OL}	V_{DRAIN} = 5V, I_{OUT} = 1mA		-	0.80	1.0	V
PWRGD Output Impedance	R_{OUT}	(V_{DRAIN} - V_{EE}) < V_{PG}		3.5	6.2	9.0	kΩ
AC TIMING							
OV High to GATE Low	t_{PHLOV}	(Figures 1, 3A)		0.6	1.6	3.0	µs
OV Low to GATE High	t_{PLHOV}	(Figures 1, 3A)		1.0	7.8	12.0	µs
UV Low to GATE Low	t_{PHLUV}	(Figures 1, 3B)		0.6	1.3	3.0	µs
UV High to GATE High	t_{PLHUV}	(Figures 1, 3B)		1.0	8.4	12.0	µs
SENSE High to GATE Low	$t_{PHLSENSE}$	(Figures 1, 2)		2	3	4	µs
ISL6140 (L VERSION)							
DRAIN Low to $\overline{PWRGD}$ Low	t_{PHLPG}	(Figures 1, 4A)		0.1	0.9	2.0	µs
DRAIN High to $\overline{PWRGD}$ High	t_{PLHPG}	(Figures 1, 4A)		0.1	0.7	2.0	µs
ISL6150 (H VERSION)							
DRAIN Low to (PWRGD-DRAIN) High	t_{PHLPG}	(Figures 1, 4B)	6	0.1	0.9	2.0	µs
DRAIN High to (PWRGD-DRAIN) Low	t_{PLHPG}	(Figures 1, 4B)	6	0.1	0.8	2.0	µs

NOTES:

5. Typical value depends on V_{DD} voltage; see Figure 13, "V_{GATE} vs V_{DD}" (<20V).
6. PWRGD is referenced to DRAIN; V_{PWRGD}-V_{DRAIN} = 0V.
7. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Test Circuit and Timing Diagrams

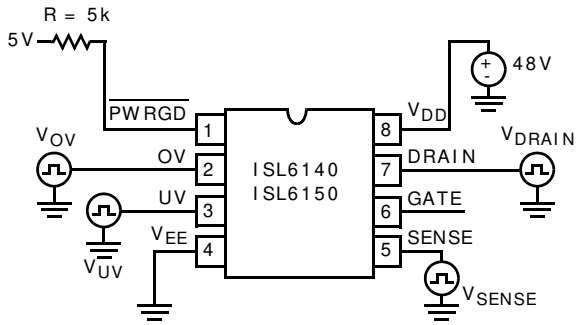


FIGURE 1. TYPICAL TEST CIRCUIT

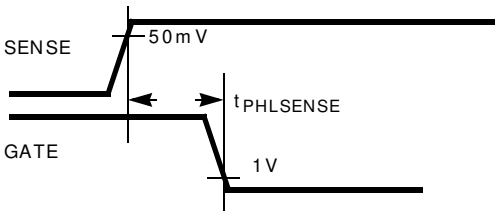


FIGURE 2. SENSE TO GATE TIMING



FIGURE 3A. OV TO GATE TIMING

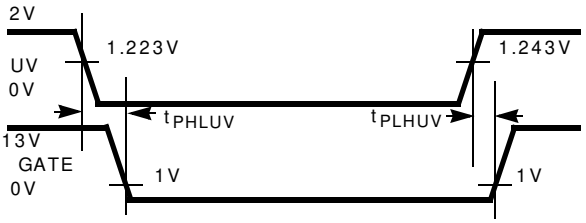


FIGURE 3B. UV TO GATE TIMING

FIGURE 3. OV AND UV TO GATE TIMING

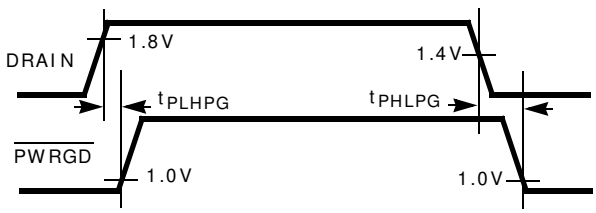


FIGURE 4A. DRAIN TO $\overline{\text{PWRGD}}$ TIMING (ISL6140)

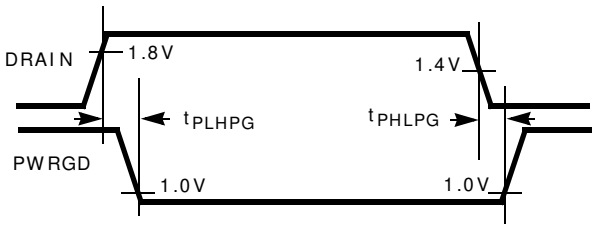
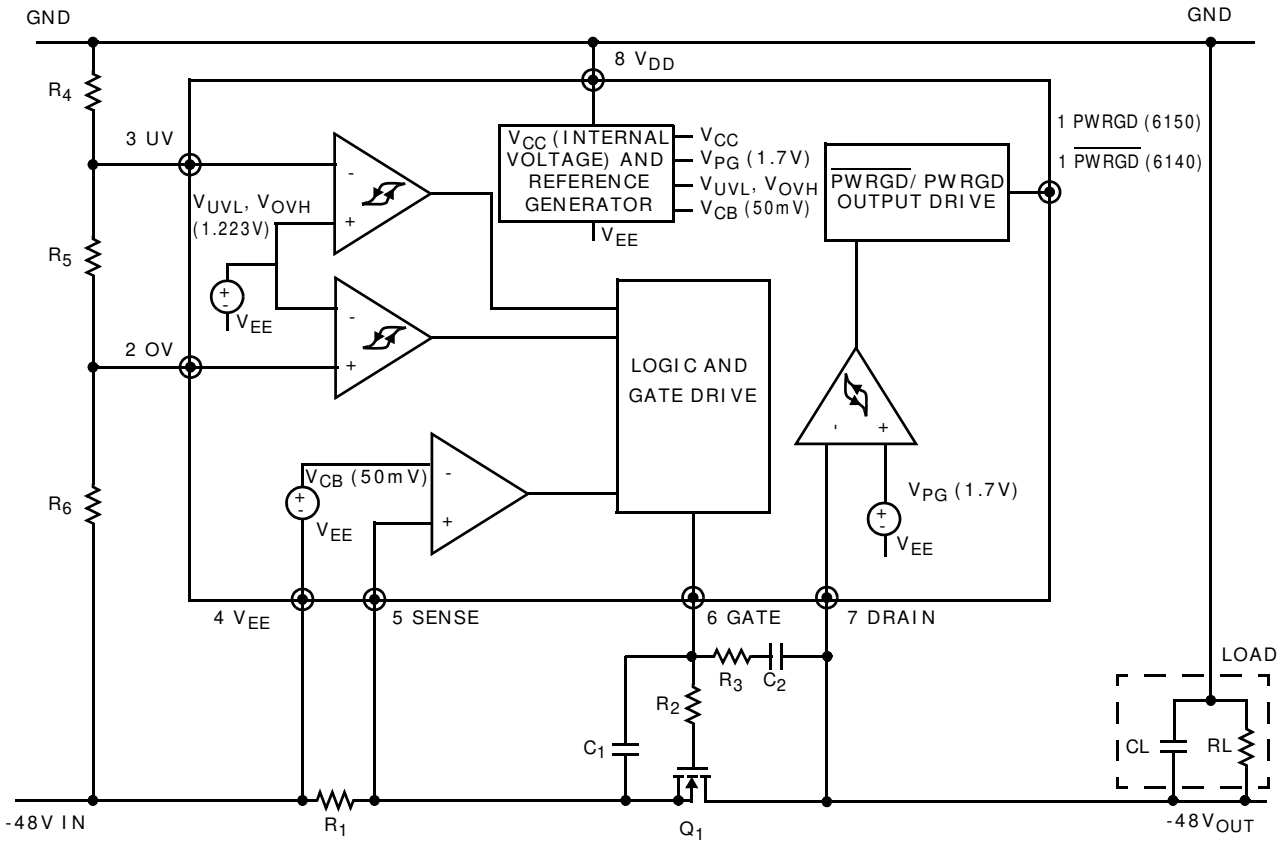


FIGURE 4B. DRAIN TO PWRGD TIMING (ISL6150)

FIGURE 4. DRAIN TO $\overline{\text{PWRGD}}$/ PWRGD TIMING

ISL6140/ISL6150 Block Diagram



Typical Values for a representative system; which assumes:

36V to 72V supply range; 48 nominal; UV = 37V; OV = 71V

1A of typical current draw; 2.5A overcurrent

100µF of load capacitance (CL); equivalent RL of 48Ω (R = V/I = 48V/1A)

R_1: 0.02Ω (1%)

R_2: 10Ω (5%)

R_3: 18kΩ (5%)

R_4: 562kΩ (1%)

R_5: 9.09kΩ (1%)

R_6: 10kΩ (1%)

C_1: 150nF (25V)

C_2: 3.3nF (100V)

Q_1: IRF530 (100V, 17A, 0.11Ω)

Applications: Quick Guide to Choosing Component Values

(See Block Diagram for reference)

This section will describe the minimum components needed for a typical application, and will show how to select component values. (Note that “typical” values may only be good for this application; the user may have to select some component values to match the system). Each block will then have more detailed explanation of how it works, and alternatives.

R_4, R_5, R_6 - together set the Under-Voltage (UV) and overvoltage (OV) trip points. When the power supply ramps up and down, these trip points (and their 20mV nominal hysteresis) will determine when the gate is allowed to turn on and off (the UV and OV do not affect the PWRGD output). The input power supply is divided down such that when each pin is equal to the trip point (nominal is 1.223V), the comparator will switch.

$$V_{UV} = 1.223 (R_4 + R_5 + R_6)/(R_5 + R_6)$$
$$V_{OV} = 1.223 (R_4 + R_5 + R_6)/(R_6)$$

The values of R_4 = 562k, R_5 = 9.09k, and R_6 = 10k will give trip points of UV = 37V and OV = 71V.

Q_1 - is the FET that connects the input supply voltage to the output load, when properly enabled. It needs to

be selected based on several criteria: maximum voltage expected on the input supply (including transients) as well as transients on the output side; maximum current expected; power dissipation and/or safe-operating-area considerations (due to the quick overcurrent latch, power dissipation is usually not a problem compared to systems where current limiting is used; however, worst case power is usually at a level just below the overcurrent shutdown). Other considerations include the gate voltage threshold which affects the $r_{DS(ON)}$ (which in turn, affects the voltage drop across the FET during normal operation), and the maximum gate voltage allowed (the IC clamp output is clamped to ~14V).

R_1 - is the overcurrent sense resistor; if the input current is high enough, such that the voltage drop across R_1 exceeds the SENSE comparator trip point (50mV nominal), the GATE pin will go low, turning off the FET, to protect the load from the excessive current. A typical value for R1 is 0.02Ω; this sets an overcurrent trip point of I = V/R = 0.05/0.02 = 2.5A. So, to choose R_1, the user must first determine at what level of current it should trip. Take into account worst case variations for the trip point (50mV ±10mV = ±20%), and the R_1 resistance (typically 1% or 5%). Note that under normal conditions, there will be a voltage drop across the resistor (V = IR), so the higher the resistor value, the bigger the voltage drop. Also note that the overcurrent should be set above the inrush current level (plus the load current); otherwise, it will latch off during that time (the alternative is to lower the in-rush current further). One rule of thumb is to set the overcurrent 2-3 times higher than the normal current (see Equation 1).

$$R_1 = V/I_{OC} = 0.05V/I_{OC}(\text{typical} = 0.02\Omega) \quad \text{(EQ. 1)}$$

CL - is the sum of all load capacitances, including the load's input capacitance itself. Its value is usually determined by the needs of the load circuitry, and not the hot plug (although there can be interaction). For example, if the load is a regulator, then the capacitance may be chosen based on the input requirements of that circuit (holding regulation under current spikes or loading, filtering noise, etc.) The value chosen will then affect how the inrush current is controlled. Note that in the case of a regulator, there may be capacitors on the output of that circuit as well; these need to be added into the capacitance calculation during inrush (unless the regulator is delayed from operation by the PWRGD signal, for example).

RL - is the equivalent resistive value of the load; it determines the normal operation current delivered through the FET. It also affects some dynamic conditions (such as the discharge time of the load capacitors during a power-down). A typical value might be 48Ω (I = V/R = 48/48 = 1A).

R2, C1, R3, C2 - are related to the gate driver, as it controls the inrush current.

R_2 prevents high frequency oscillations; 10Ω is a typical value. R_2 = 10Ω

R_3 and C_2 act as a feedback network to control the inrush current. I inrush = (Igate* C_L)/C_2, where C_L is the load capacitance (including module input capacitance), and Igate is the gate pin charging current, nominally 45µA. So choose a value of acceptable inrush for the system, and then solve for C_2. So I = 45µA*(C_L/C_2). Or C_2 = (45µA* C_L)/ I.

C_1 and R_3 prevent Q_1 from turning on momentarily when power is first applied. Without them, C_2 would pull the gate of Q1 up to a voltage roughly equal to VEE* C_2/$C_{GS}(Q_1)$ (where C_{GS} is the FET gate-source capacitance) before the ISL6140 could power up and actively pull the gate low. Place C_1 in parallel with the gate capacitance of Q1; isolate them from C_2 by R_3.

C1 = (V_{INMAX} - V_{TH})/ V_{TH}*(C_2+ C_{GD}) where V_{TH} is the FET's minimum gate threshold, Vinmax is the maximum operating input voltage, and Cgd is the FET gate-drain capacitance.

R3 = (V_{INMAX} + ΔV_{GATE})/ 5mA its value is not critical; a typical value is 18kΩ

Applications: Inrush Current

The primary function of the ISL6140 hot plug controller is to control the inrush current. When a board is plugged into a live backplane, the input capacitors of the board's power supply circuit can produce large current transients as they charge up. This can cause glitches on the system power supply (which can affect other boards!), as well as possibly cause some permanent damage to the power supply.

The key to allowing boards to be inserted into a live backplane then is to turn on the power to the board in a controlled manner, usually by limiting the current allowed to flow through a FET switch, until the input capacitors are fully charged. At that point, the FET is fully on, for the smallest voltage drop across it.

In addition to controlling the in-rush current, the ISL6140 also protects the board against overcurrent, overvoltage, undervoltage, and can signal when the output voltage is within its expected range (PWRGD).

Note that although this IC was designed for -48V systems, it can also be used as a low-side switch for positive 48V systems; the operation and components are usually similar. One possible difference is the kind of level shifting that may be needed to interface logic signals to the UV input (to reset the latch) or PWRGD output. For example, many of the IC functions are referenced to the IC substrate, connected to the VEE pin. But this pin may be considered -48V or GND, depending upon the polarity of the system. And input or output logic (running at 5V or 3.3V or even lower) might be externally referenced to either VDD or VEE of the IC, instead of GND.

Applications: Overcurrent

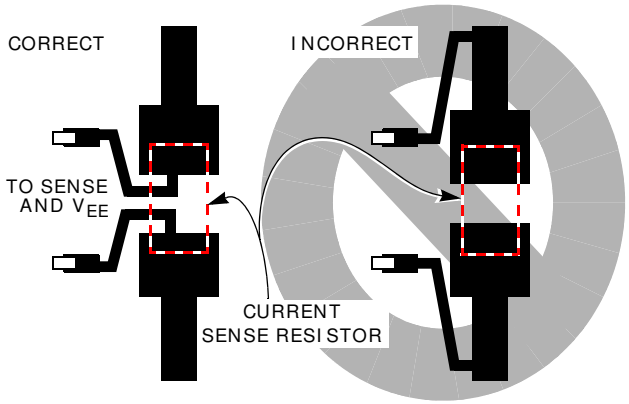


FIGURE 5. SENSE RESISTOR

Physical layout of $R_{1\ SENSE}$ resistor is critical to avoid the possibility of false overcurrent occurrences. Since it is in the main input-to-output path, the traces should be wide enough to support both the normal current, and up to the overcurrent trip point. Ideally trace routing between the R_1 resistor and the ISL6140 and ISL6150 (pin 4 (V_{EE}) and pin 5 (SENSE) is direct and as short as possible with zero current in the sense lines (see Figure 5).

There is a short filter (3µs nominal) on the comparator; current spikes shorter than this will be ignored. Any longer pulse will shut down the output, requiring the user to either power-down the system (below the UV voltage), or pull the UV pin below its trip point (usually with an external transistor).

If current pulses longer than the 3µs are expected, and need to be filtered, then an additional resistor and capacitor can be added. As shown in Figure 29, R_7 and C_3 act as a low-pass filter such that the voltage on the SENSE pin won't rise as fast, effectively delaying the shut-down. Since the ISL6140/ISL6150 has essentially zero current on the SENSE pin, there is no voltage drop or error associated with the extra resistor. R_7 is recommended to be small, 100Ω is a good value.

The delay time is approximated by the added RC time constant, modified by a factor relative to the trip point (see Equation 2).

$$t = -R*C*\ln[1 - (V(t) - V(t_0))/(V_i - V(t_0))] \quad \text{(EQ. 2)}$$

where V(t) is the trip voltage (nominally 50mV); $V(t_0)$ is the nominal voltage drop across the sense resistor before the overcurrent condition; V_i is the voltage drop across the sense resistor while the overcurrent is applied.

For example: a system has a normal 1A current load, and a 20mΩ sense resistor, for a 2.5A overcurrent. It needs to filter out a 50µs current pulse at 5A. Therefore:

V(t) = 50mV (from spec)

$V(t_0)$ = 20mV (V = IR = 1A*20mΩ)

V_i = 100mV (V = IR = 5A*20mΩ)

If R_7 = 100Ω, then C_3 is around 1µF.

Note that the FET must be rated to handle the higher current for the longer time, since the IC is not doing current limiting; the RC is just delaying the overcurrent shutdown.

Applications: OV and UV

The UV and OV input pins are high impedance, so the value of the external resistor divider is not critical with respect to input current. Therefore, the next consideration is total current; the resistors will always draw current, equal to the supply voltage divided by the total of R4 + R5 + R6; so the values should be chosen high enough to get an acceptable current. However, to the extent that the noise on the power supply can be transmitted to the pins, the resistor values might be chosen to be lower. A filter capacitor from UV to VEE or OV to UV is a possibility, if certain transients need to be filtered. (Note that even some transients which will momentarily shut off the gate might recover fast enough such that the gate or the output current does not even see the interruption).

Finally, take into account whether the resistor values are readily available, or need to be custom ordered. Tolerances of 1% are recommended for accuracy. Note that for a typical 48V system (with a 36V to 72V range), the 36V or 72V is being divided down to 1.223V, a significant scaling factor. For UV, the ratio is roughly 30x; every 3mV change on the UV pin represents roughly 0.1V change of power supply voltage. Conversely, an error of 3mV (due to the resistors, for example) results in an error of 0.1V for the supply trip point. The OV ratio is around 60. So the accuracy of the resistors comes into play.

The hysteresis of the comparators (20mV nominal) is also multiplied by the scale factor of 30 for the UV pin (30 * 20mV = 0.6V of hysteresis at the power supply) and 60 for the OV pin (60*20mV = 1.2V of hysteresis at the power supply).

With the three resistors, the UV equation is based on the simple resistor divider:

$1.223 = V_{UV}*(R_5 + R_6)/(R_4 + R_5 + R_6)$ or

$V_{UV} = 1.223\ (R_4 + R_5 + R_6)/(R_5 + R_6)$

Similarly, for OV:

$1.223 = V_{OV}*(R_6)/(R_4 + R_5 + R_6)$ or

$V_{OV} = 1.223\ (R_4 + R_5 + R_6)/(R_6)$

Note that there are two equations, but 3 unknowns. Because of the scale factor, R_4 has to be much bigger than the other two; chose its value first, to set the current (for example, 50V/500kΩ draws 100µA), and then the other two will be in the 10kΩ range. Solve the two equations for two unknowns. Note that some iteration may be necessary to select values that meet

the requirement, and are also readily available standard values.

The three resistors (R_4, R_5, R_6) is the recommended approach for most cases. But if acceptable values can't be found, then consider 2 separate resistor dividers (one for each pin; both from V_{DD} to V_{EE}). This also allows the user to adjust or trim either trip point independently.

Note that the top of the resistor dividers is shown in Figure 29 as GND (Short pin). In a system where cards are plugged into a backplane (or any other case where pins are plugged into an edge connector) the user may want to take advantage of the order in which pins make contact. Typically, pins on either end of the card make contact first (although you may not know which end is first). If you combine that with designating a pin near the center as the short pin GND, and make it shorter than the rest, then it should be the last pin to make contact.

The advantage of doing this: the V_{DD} and V_{EE} pin connections are made first. The IC is powered up, but since the top of the resistor divider is still open, both the UV and OV pins are pulled low to V_{EE}, which will keep the gate off. This allows the IC time to get initialized, and also allows the power supply to charge up any input capacitance. By the time the resistor divider makes contact, the power supply voltage on the card is presumably stabilized, and the IC ready to respond; when the UV pin reaches the proper voltage, the IC will turn on the GATE of the FET, and starts the controlled inrush current charging.

Note that this is not a requirement; if the IC gets powered at the same time as the rest of the board, it should be able to properly control the inrush current. But if finer control is needed, there are many variables involved to consider: the number of pins in the connector; the lengths of the pins; the amount of mechanical play in the pin-to-connector interface; the amount of extra time versus the shorter pin length; the amount of input capacitance versus the ability of the power supply to charge it; the manufacturing cost adder (if any) of different length pins; etc.

Applications: $\overline{\text{PWRGD}}$/ PWRGD

The $\overline{\text{PWRGD}}$/PWRGD outputs are typically used to directly enable a power module, such as a DC/DC converter. The $\overline{\text{PWRGD}}$ (ISL6140) is used for modules with active low enable (L version); PWRGD (ISL6150) for those with active high enable (H version). The modules usually have a pull-up device built-in, as well as an internal clamp. If not, an external pull-up resistor may be needed, since the output is open drain. If the pin is not used, it can be left open.

For both versions, the PG comparator compares the DRAIN pin to V_{EE} (connected to the source of the FET); if the voltage drop exceeds VPG (1.7V nominal), that implies the drop across the FET is too high, and the PWRGD pin should go in-active (power-NO-GOOD).

ISL6140 (L version; Figure 6): Under normal conditions (DRAIN < VPG), the Q2 DMOS will turn on, pulling $\overline{\text{PWRGD}}$ low, enabling the module.

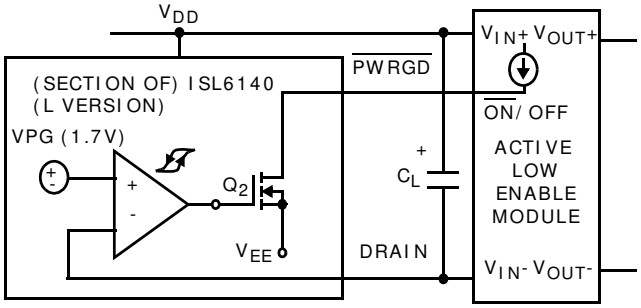


FIGURE 6. ACTIVE LOW ENABLE MODULE

When the DRAIN is too high, the Q_2 DMOS will shut off (high impedance), and the pin will be pulled high by the external module (or an optional pull-up resistor or equivalent), disabling the module. If a pull-up resistor is used, it can be connected to any supply voltage that doesn't exceed the IC pin maximum ratings on the high end, but is high enough to give acceptable logic levels to whatever signal it is driving. An external clamp may be used to limit the range.

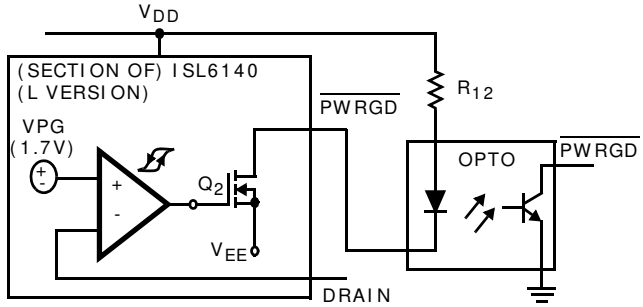


FIGURE 7. ACTIVE LOW ENABLE OPTO-ISOLATOR

The $\overline{\text{PWRGD}}$ can also drive an opto-coupler (such as a 4N25), as shown in Figure 7 or LED (Figure 8). In both cases, they are on (active) when power is good. Resistors R_{12} or R_{13} are chosen, based on the supply voltage, and the amount of current needed by the loads.

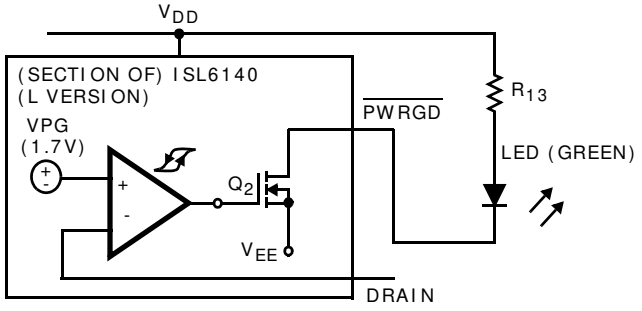


FIGURE 8. ACTIVE LOW ENABLE WITH LED

ISL6150 (H version; Figure 9): Under normal conditions (DRAIN < VPG), the Q_3 DMOS will be on, shorting the bottom of the internal resistor to V_{EE}, and turning Q_2 off. If the pull-up current from the external module is high enough, the voltage drop across the 6.2kΩ resistor will look like a logic high (relative to DRAIN). Note that the module is only referenced to DRAIN, not V_{EE} (but under normal conditions, the FET is on, and the DRAIN and V_{EE} are almost the same voltage).

When the DRAIN voltage is high compared to VPG, Q_3 DMOS turns off, and the resistor and Q_2 clamp the PWRGD pin to one diode drop (~0.7V) above the DRAIN pin. This should be able to pull low against the module pull-up current, and disable the module.

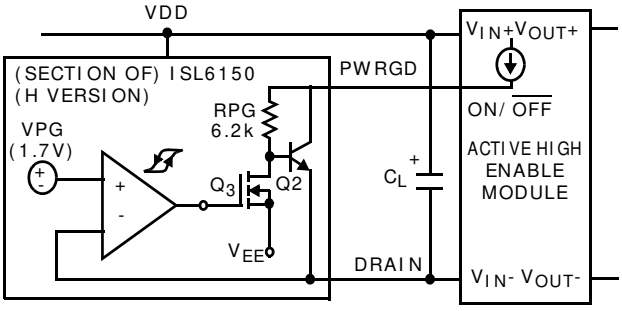


FIGURE 9. ACTIVE HIGH ENABLE MODULE

Applications: GATE Pin

To help protect the external FET, the output of the GATE pin is internally clamped; up to an 80V supply, it will not be any higher than 15V (nominal 14V). From about 18V down to 10V, the GATE voltage will be around 4V below the supply voltage; at 10V supply, the minimum GATE voltage is 5.4V (worst case is at -40°C).

Applications: Optional Components

In addition to the typical application, and the variations already mentioned, there are a few other possible components that might be used in specific cases. See Figure 29 for some possibilities.

If the input power supply exceeds the 100V absolute maximum rating, even for a short transient, that could cause permanent damage to the IC, as well as other components on the board. If this cannot be guaranteed, a voltage suppressor (such as the SMAT70A, D_1) is recommended. When placed from V_{DD} to V_{EE} on the board, it will clamp the voltage.

If transients on the input power supply occur when the supply is near either the OV or UV trip points, the GATE could turn on or off momentarily. One possible solution is to add a filter cap C_4 to the V_{DD} pin, through isolation resistor R_{10}. A large value of R_{10} is better for the filtering, but be aware of the voltage drop across it. For example, a 1kΩ resistor, with 1mA of I_{DD} would have 1V across it and dissipate 1mW. Since the UV and OV comparators are referenced with respect to the V_{EE} supply, they should not be affected. But the GATE clamp voltage could be offset by the voltage across the extra resistor.

If there are negative transients on the DRAIN pin, blocking diodes may help limit the amount of current injected into the IC substrate. General purpose diodes (such as 1N4148) may be used. Note that the ISL6140 (L version) requires one diode, while the ISL6150 (H version) requires two diodes. One consequence of the added diodes it that the V_{PG} voltage is offset by each diode drop.

The switch SW1 is shown as a simple pushbutton. It can be replaced by an active switch, such as an NPN or NFET; the principle is the same; pull the UV node below its trip point, and then release it (toggle low). To connect an NFET, for example, the drain goes to UV; the source to V_{EE}, and the gate is the input; if it goes high (relative to V_{EE}), it turns the NFET on, and UV is pulled low. Just make sure the NFET resistance is low compared to the resistor divider, so that it has no problem pulling down against it.

R_8 is a pull-up resistor for $\overline{PWRGD}$, if there is no other component acting as a pull-up device. The value of R8 is determined by how much current you want when pulled low (also affected by the V_{DD} voltage); and you want to pull it low enough for a good logic low level. An LED can also be placed in series with R_8, if desired. In that case, the criteria is the LED brightness versus current.

R_7 and C_3 are used to delay the overcurrent shutdown, as described in the OV and UV section.

Applications: “Brick” Regulators

One of the typical loads used are DC/DC regulators, some commonly known as “brick” regulators, (partly due to their shape, and because it can be considered a “building block” of a system). For a given input voltage range, there are usually whole families of different output voltages and current ranges. There are also various standardized sizes and pinouts, starting with the original “full” brick, and since getting smaller (half-bricks and quarter-bricks are now common).

Other common features may include: all components (except some filter capacitors) are self-contained in a molded plastic package; external pins for connections; and often an ENABLE input pin to turn it on or off. A hot plug IC, such as the ISL6140, is often used to gate power to a brick, as well as turn it on.

Many bricks have both logic polarities available (Enable Hi or Lo input); select the ISL6140 (L version) and ISL6150 (H version) to match. There is little difference between them, although the L version output is usually simpler to interface.

The Enable input often has a pull-up resistor or current source, or equivalent built in; care must be taken in the ISL6150 (H version) output that the given current will create a high enough input voltage (remember that current through the RPG 6.2kΩ resistor generates the high voltage level; (see Figure 9).

The input capacitance of the brick is chosen to match its system requirements, such as filtering noise, and maintaining regulation under varying loads. Note that this input capacitance appears as the load capacitance of the ISL6140/ISL6150.

The brick's output capacitance is also determined by the system, including load regulation considerations. However, it can affect the ISL6140 and ISL6150, depending upon how it is enabled. For example, if the PWRGD signal is not used to enable the brick, the following could occur. Sometime during the inrush current time, as the main power supply starts charging the brick input capacitors, the brick itself will start working, and start charging its output capacitors and load; that current has to be added to the inrush current. In some cases, the sum could exceed the overcurrent shutdown, which would shut down the whole system! Therefore, whenever practical, it is advantageous to use the PWRGD output to keep the brick off at least until the input caps are charged up, and then start-up the brick to charge its output caps.

Typical brick regulators include models such as Lucent JW050A1-E or Vicor VI-J30-CY. These are nominal -48V input, and 5V outputs, with some isolation between the input and output.

Applications: Layout Considerations

For the minimum application, there are only 6 resistors, 2 capacitors, one IC and one FET. A sample layout is shown in Figure 30. It assumes the IC is 8-SOIC; the FET is in a D2PAK (or similar SMD-220 package).

Although GND planes are common with multi-level PCBs, for a -48V system, the -48V rails (both input and output) act more like a GND than the top 0V rail (mainly because the IC signals are mostly referenced to the lower rail). So if separate planes for each voltage are not an option, consider prioritizing the bottom rails first.

Note that with the placement shown, most of the signal lines are short, and there should not be much interaction between them.

Although decoupling capacitors across the IC supply pins are often recommended in general, this application may not need one, nor even tolerate one. For one thing, a decoupling cap would add to (or be swamped out by) any other input capacitance; it also needs to be charged up when power is applied. But more importantly, there are no high speed (or any) input signals to the IC that need to be conditioned. If still desired, consider the isolation resistor R_{10}, as shown in Figure 29.

Typical Performance Curves

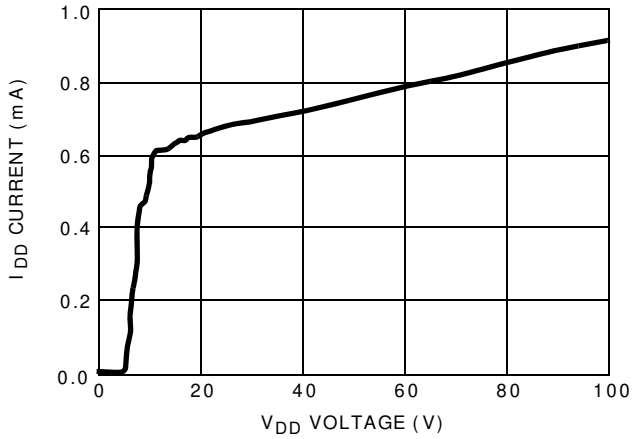


FIGURE 10. I_{DD} vs V_{DD}

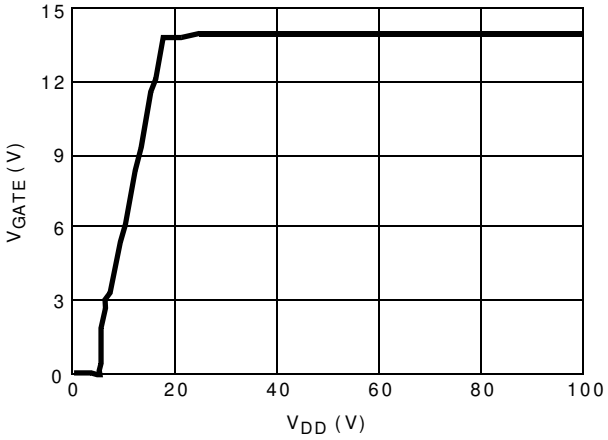


FIGURE 11. V_{GATE} vs V_{DD}

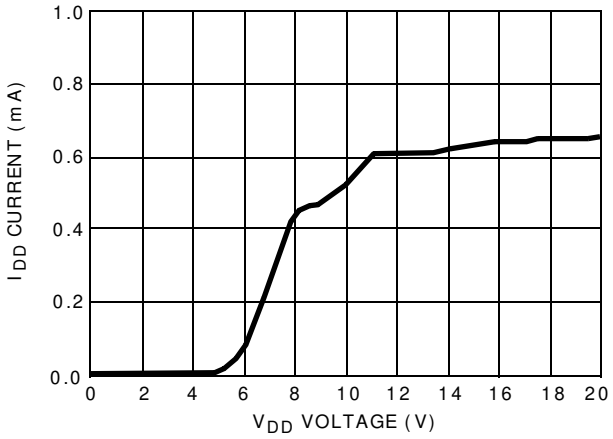


FIGURE 12. I_{DD} vs V_{DD} (<20V)

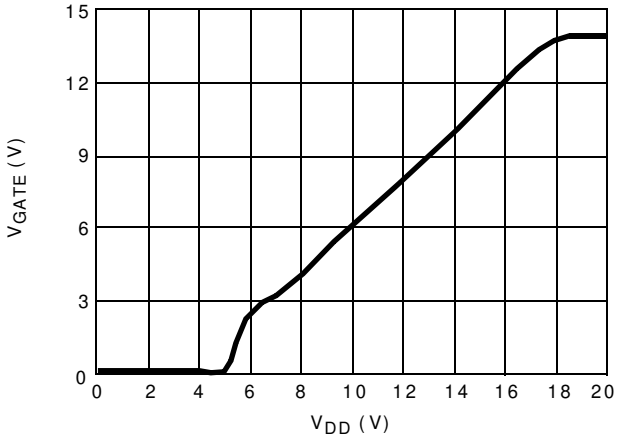


FIGURE 13. V_{GATE} vs V_{DD} (<20V)

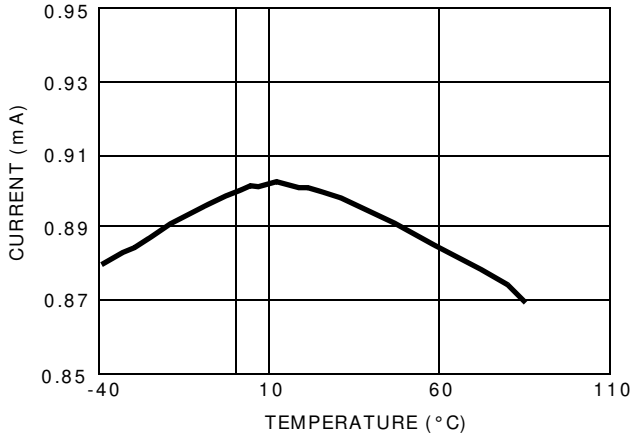


FIGURE 14. I_{DD} CURRENT (AT V_{DD} = 80V)

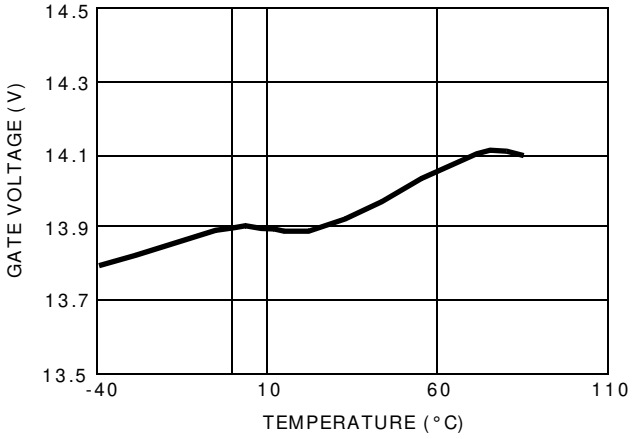


FIGURE 15. GATE VOLTAGE (AT V_{DD} = 80V)

Typical Performance Curves (Continued)

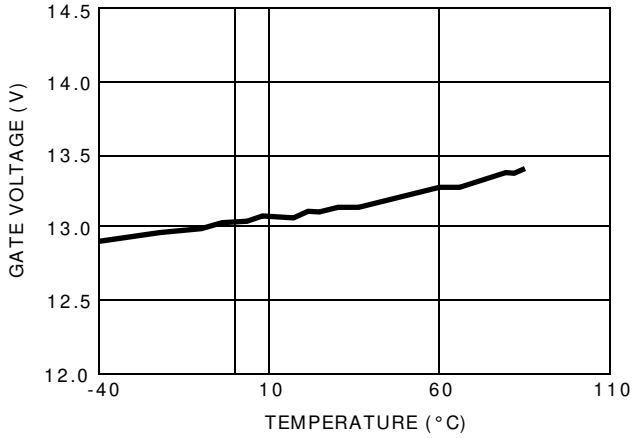


FIGURE 16. GATE VOLTAGE (AT V_{DD} = 17V)

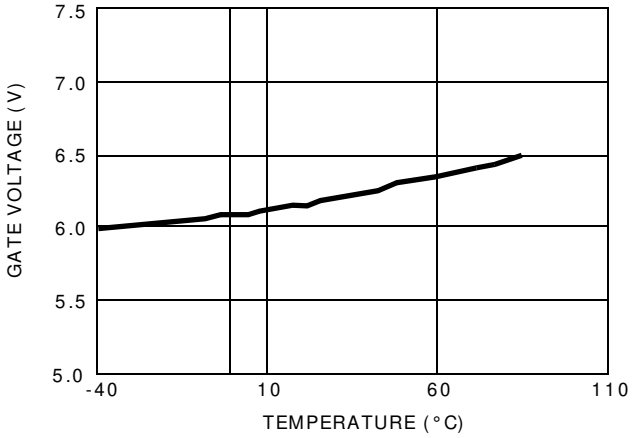


FIGURE 17. GATE VOLTAGE (AT V_{DD} = 10V)

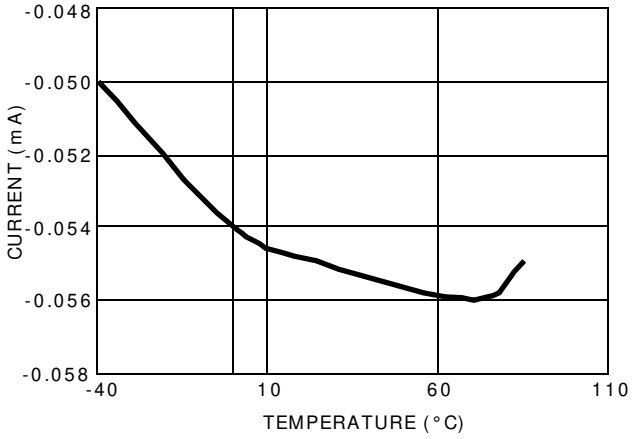


FIGURE 18. GATE PULL-UP CURRENT

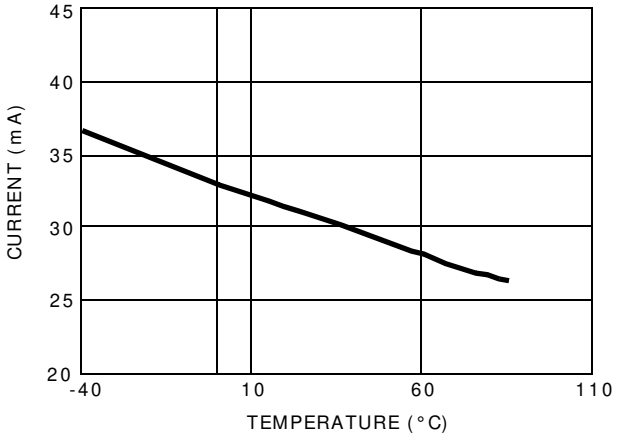


FIGURE 19. GATE PULL-DOWN CURRENT

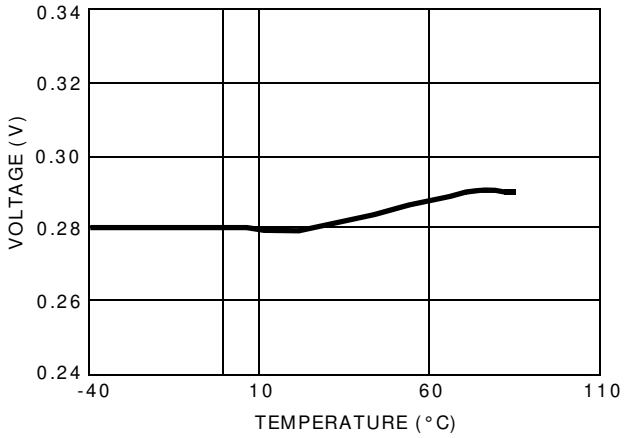


FIGURE 20. $\overline{\text{PWRGD}}$ (ISL6140) VOL (AT 1mA) VOLTAGE

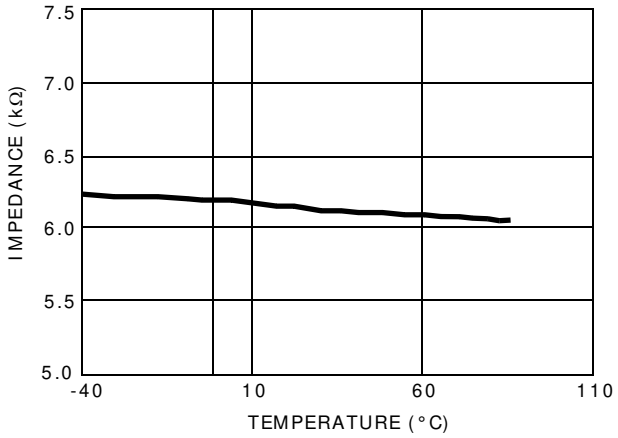


FIGURE 21. PWRGD (ISL6150) IMPEDANCE (kΩ)

Typical Performance Curves (Continued)

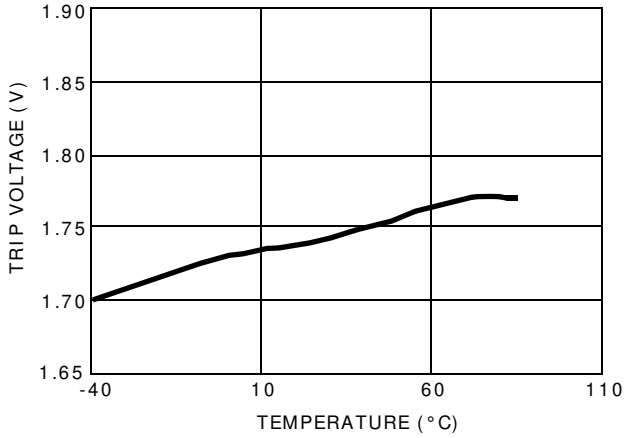


FIGURE 22. DRAIN/PG UP TRIP VOLTAGE

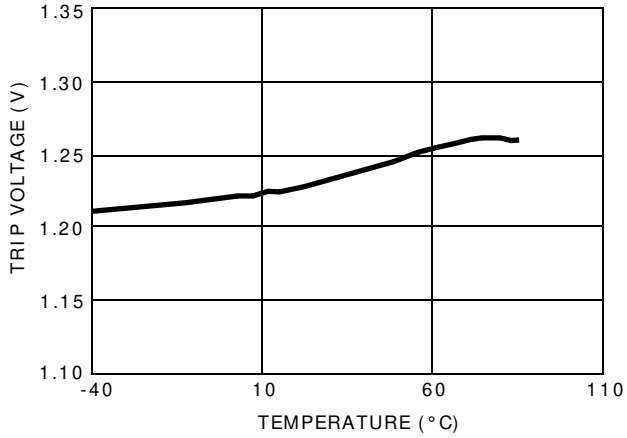


FIGURE 23. DRAIN/PG DOWN TRIP VOLTAGE

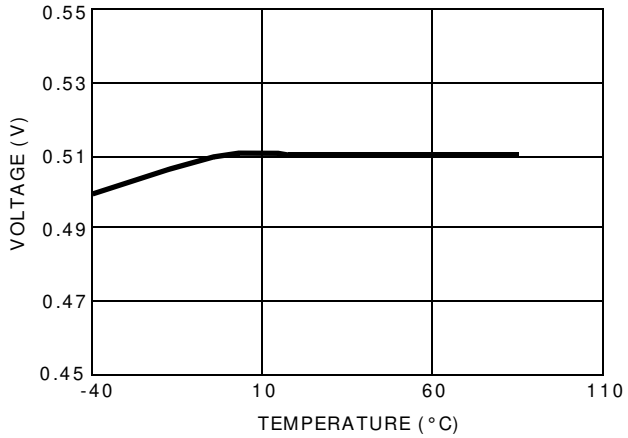


FIGURE 24. DRAIN/PG HYSTERESIS VOLTAGE

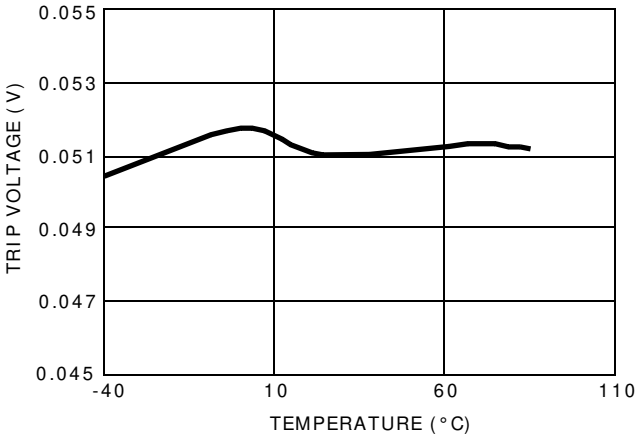


FIGURE 25. SENSE TRIP VOLTAGE

Inrush Current

In the example in Figure 26, the supply voltage is 48V and the load resistor (RL) is 620Ω, for around 80mA. The load capacitance is 100µF (100V). The Sense Resistor (R_1) is 0.02Ω (trip point at 2.5A; well above the inrush current here).

Note that the load current starts at 0 (FET off); reaches a peak of ~850mA as the GATE voltage ramps and turns on the FET slowly, and then settles out at 80mA, once the CL is fully charged to the 48V. The width of the inrush current pulse is 8ms wide. For comparison, with the same conditions, but without the gate-controlled FET, the current was over 20A, during a 130µs pulse.

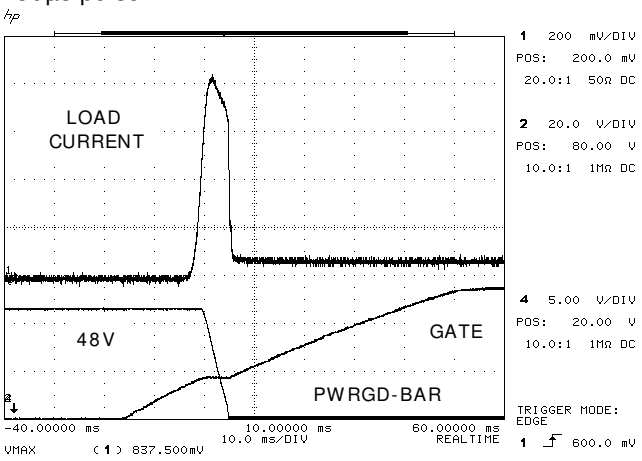


FIGURE 26. INRUSH CURRENT

Power Supply Ramp

Figure 27 shows the power supply voltage (to the V_{DD} pin, with respect to GND at the V_{EE} pin) ramping up. In this case, the values chosen were R_4 = 562k; R5 = 5.9k; R_6 = 13.3k; that sets the UV trip point around 38V, and the OV trip point to 54V. Note that the GATE starts at 0V, and stays there until the UV trip point (38V) is exceeded; then it ramps (slowly, based on the external components chosen) up to around 13V, where it is clamped; it stays there until the power supply exceeds the OV trip point at 54V (the GATE shut-off is much faster than the turn-on). The total time scale is 2 seconds; the V_{DD} ramp speed was simply based on the inherent characteristic of the particular power supply used.

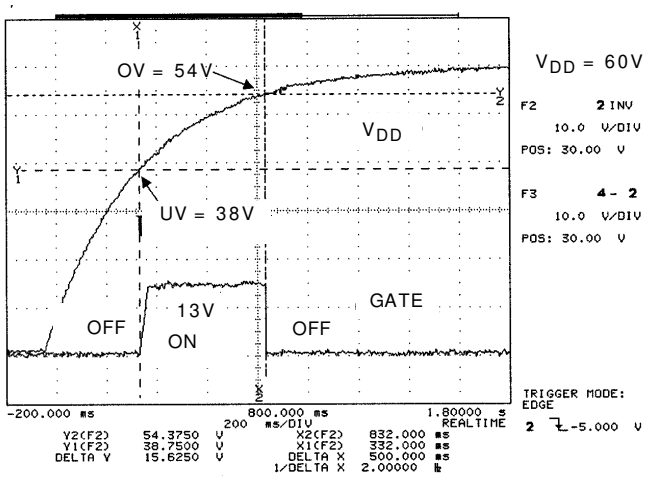


FIGURE 27. POWER SUPPLY RAMP

Overcurrent at 2.3A

In Figure 28, an Electronic Load Generator was used to ramp the load current; no load resistor or capacitor was connected. The sense Resistor R_1 is 0.02Ω; that should make the nominal overcurrent trip point 2.5A.

The GATE is high (clamped to around 13V), keeping the FET on, as the current starts to ramp up from zero; the GATE starts to go low (to shut off the FET) when the load current hits 2.3A. Note that it takes only 44µs for the GATE to shut off the FET (when the load current equals zero).

Keep in mind that the tolerance of the sense resistor (1% here) and the IC overcurrent trip voltage (V_{CB}) affect the accuracy of the trip point; that's why the trip point doesn't necessarily equal the 2.5A design target.

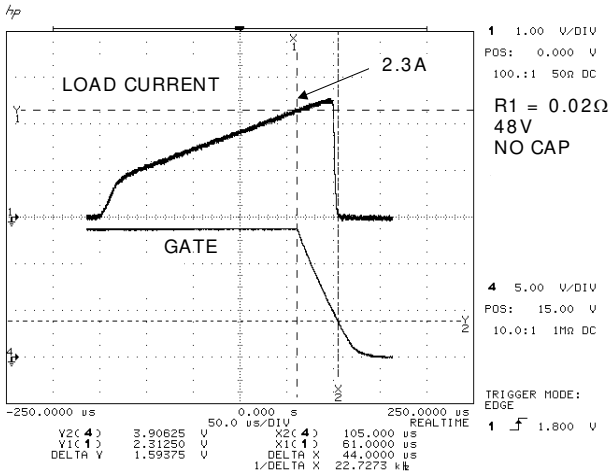


FIGURE 28. OVERCURRENT AT 2.3A

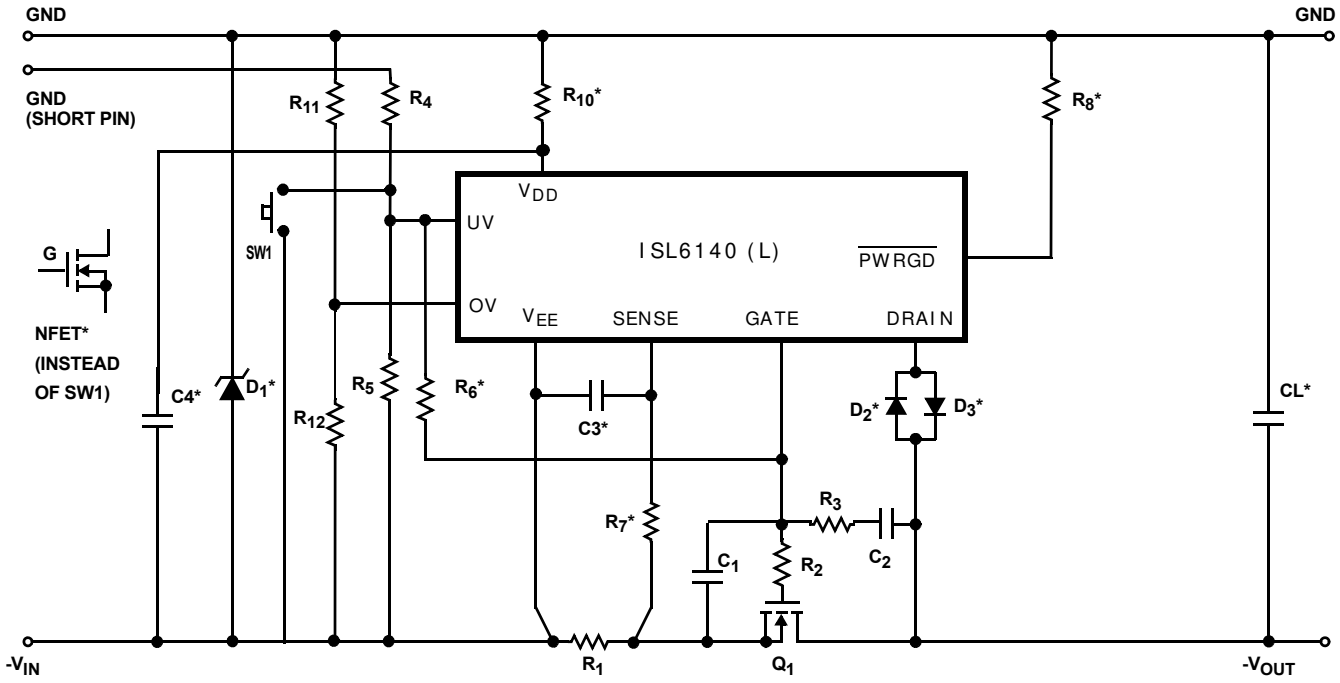


FIGURE 29. ISL6140/50 OPTIONAL COMPONENTS (SHOWN WITH *)

Optional Components

D_1 is a voltage suppressor; SMAT70A or equivalent.

D_2 and D_3 are DRAIN diodes; the ISL6150 (H version) uses both D_2 and D_3; the ISL6140 (L version) uses just D_2. If neither is used, short the path of either, to connect the DRAIN pin to C_2 and Q_1. The 1N4148 is a typical diode.

SW1 is a push-button switch, that can manually reset the fault latch after an overcurrent shutdown. It can also be replaced by a transistor switch.

R_{10} and C_4 are used to filter the V_{DD} voltage, such that small transients on the input supply do not trigger UV or OV.

R_7 and C_3 are used to delay the overcurrent shutdown. R_7 should be shorted, if not used. See the overcurrent section for more details.

R_8 is a pull-up resistor for $\overline{PWRGD}$, if there is no other component acting as a pull-up device. An LED can also be placed in series with R_8, if desired (see Figure 8).

C_L is any extra output Load capacitance, which can also be considered input capacitance for the external module.

R_6 is used to add more hysteresis to the UV threshold, which already has a built-in 20mV hysteresis. With R_6, the new thresholds with a rising and falling input are shown in Equation 3 and 4:

$$Vuv(RISING) = VUVH \bullet \left(\frac{R5 \bullet R6 + R4 \bullet R6 + R4 \bullet R5}{R5 \bullet R6}\right) \quad \text{(EQ. 3)}$$

$$Vuv(falling) = VUVL \bullet \left(\frac{R5 \bullet R6 + R4 \bullet R6 + R4 \bullet R5}{R5 \bullet R6}\right) - Vgate \bullet \left(\frac{R4}{R6}\right) \quad \text{(EQ. 4)}$$

Since R_6 is connected directly to the GATE output, it will reduce the available gate current, which will reduce the dv/dt across the MOSFET and hence the inrush current. The value of R_6 should be kept as high as possible (greater than 500k recommended) so that it does not drag down the GATE voltage below the value required to ensure the MOSFET is fully enhanced.

Figure 30 shows a sample component placement and routing for the typical application shown in Figure 31.

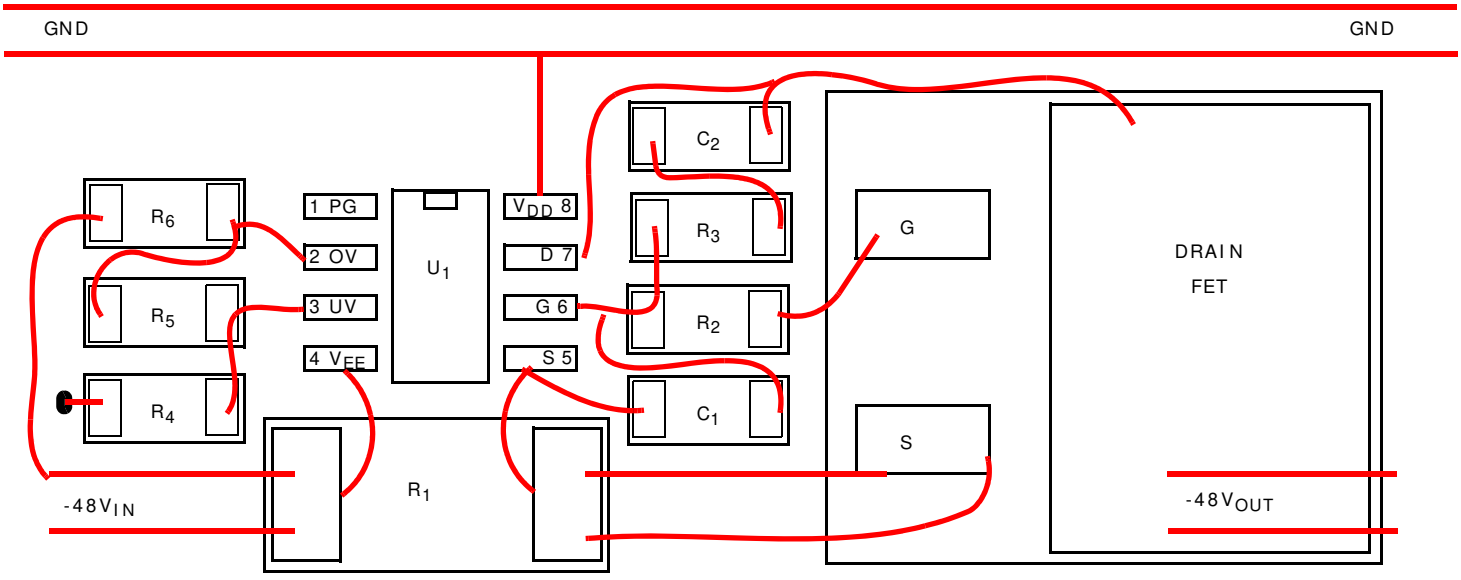


FIGURE 30. SAMPLE LAYOUT (NOT TO SCALE)

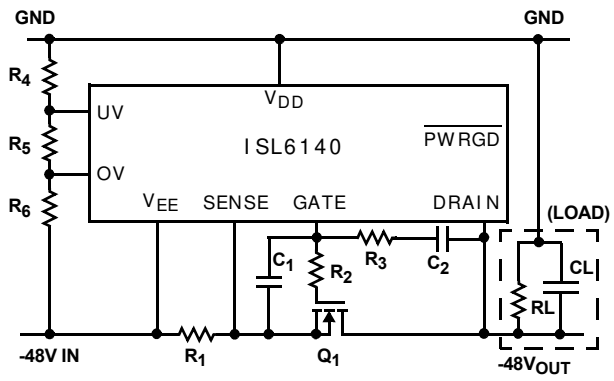


FIGURE 31. TYPICAL APPLICATION

NOTES:

1. Layout scale is approximate; routing lines are just for illustration purposes; they do not necessarily conform to normal PCB design rules. High current buses are wider, shown with parallel lines.
2. Approximate size of the above layout is 1.6 x 0.6 inches; almost half of the area is just the FET (D2PAK or similar SMD-220 package).
3. R_1 sense resistor is size 2512; all other R's and C's shown are 0805; they can all potentially use smaller footprints, if desired.
4. The RL and CL are not shown on the layout.
5. R4 uses a via to connect to GND on the bottom of the board; all other routing can be on top level. (It's even possible to eliminate the via, for an all top-level route).
6. $\overline{PWRGD}$ signal is not used here.
7. BOM (Bill Of Materials)
   R_1 = 0.02Ω (5%)
   R_2 = 10Ω (5%)
   R_3 = 18kΩ (5%)
   R_4 = 562kΩ (1%)
   R_5 = 9.09kΩ (1%)
   R_6 = 10kΩ (1%)
   C_1 = 150nF (25V)
   C_2 = 3.3nF (100V)
   Q_1 = IRF530 (100V, 17A, 0.11Ω)

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
December 3, 2015	FN9039.5	Added Rev History and About Intersil sections. Updated Ordering Information on page 2. Updated POD M8.15 to most current version with revision updates as follows: Updated to new POD format by removing table and moving dimensions onto drawing and adding land pattern. Changed in Typical Recommended Land Pattern the following: 2.41(0.095) to 2.20(0.087) 0.76 (0.030) to 0.60(0.023) 0.200 to 5.20(0.205) Changed Note 1 "1982" to "1994"

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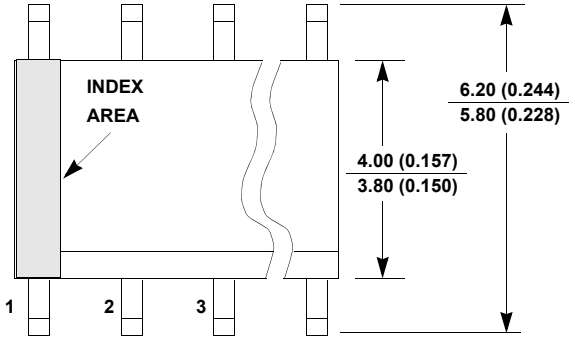
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Package Outline Drawing

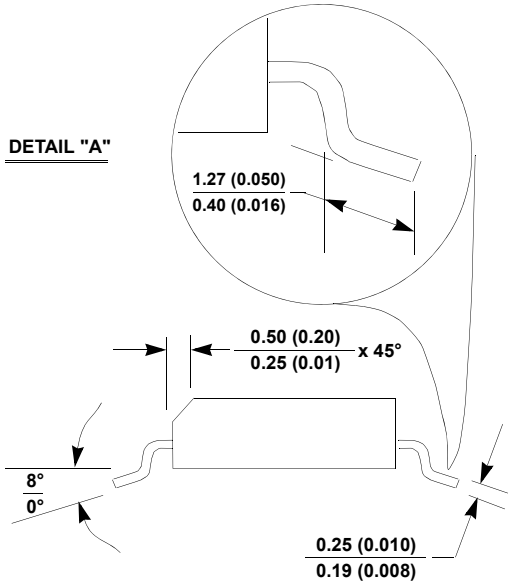
M8.15

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

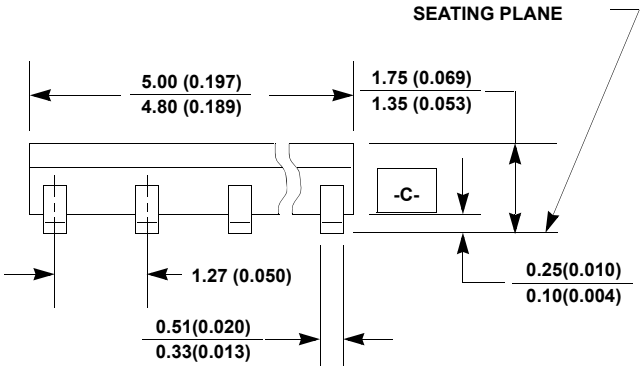
Rev 4, 1/12



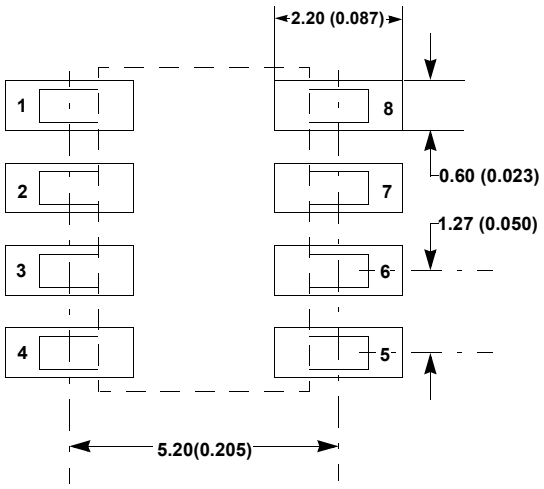
TOP VIEW



SIDE VIEW "B"



SIDE VIEW "A"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensioning and tolerancing per ANSI Y14.5M-1994.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.