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Renesas Electronics Corporation

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# 1. Overview

The M16C/62P Group (M16C/62P, M16C/62PT) of single-chip microcomputers are built using the high performance silicon gate CMOS process using a M16C/60 Series CPU core and are packaged in a 80-pin, 100-pin and 128-pin plastic molded QFP. These single-chip microcomputers operate using sophisticated instructions featuring a high level of instruction efficiency. With 1M bytes of address space, they are capable of executing instructions at high speed. In addition, this microcomputer contains a multiplier and DMAC which combined with fast instruction processing capability, makes it suitable for control of various OA, communication, and industrial equipment which requires high-speed arithmetic/logic operations.

## 1.1 Applications

Audio, cameras, television, home appliance, office/communications/portable/industrial equipment, automobile, etc.

Specifications written in this manual are believed to be accurate, but are not guaranteed to be entirely free of error. Specifications in this manual may be changed for functional or performance improvements. Please make sure your manual is the latest edition.

## 1.2 Performance Outline

Table 1.1 to 1.3 list Performance Outline of M16C/62P Group (M16C/62P, M16C/62PT)(128-pin version).

**Table 1.1 Performance Outline of M16C/62P Group (M16C/62P, M16C/62PT)(128-pin version)**

| | Item | Performance |
|---|---|---|
| | | M16C/62P |
| CPU | Number of Basic Instructions | 91 instructions |
| | Minimum Instruction Execution Time | 41.7ns(f(BCLK)=24MHz, VCC1=3.3 to 5.5V)<br>100ns(f(BCLK)=10MHz, VCC1=2.7 to 5.5V) |
| | Operating Mode | Single-chip, memory expansion and microprocessor mode |
| | Address Space | 1 Mbyte (Available to 4 Mbytes by memory space expansion function) |
| | Memory Capacity | See **Table 1.4 to 1.5 Product List** |
| Peripheral Function | Port | Input/Output : 113 pins, Input : 1 pin |
| | Multifunction Timer | Timer A : 16 bits x 5 channels,<br>Timer B : 16 bits x 6 channels,<br>Three phase motor control circuit |
| | Serial Interface | 3 channels<br>Clock synchronous, UART, I2C bus(1), IEBus(2)<br>2 channels<br>Clock synchronous |
| | A/D Converter | 10-bit A/D converter: 1 circuit, 26 channels |
| | D/A Converter | 8 bits x 2 channels |
| | DMAC | 2 channels |
| | CRC Calculation Circuit | CCITT-CRC |
| | Watchdog Timer | 15 bits x 1 channel (with prescaler) |
| | Interrupt | Internal: 29 sources, External: 8 sources, Software: 4 sources, Priority level: 7 levels |
| | Clock Generation Circuit | 4 circuits<br>Main clock generation circuit (*),<br>Subclock generation circuit (*),<br>On-chip oscillator, PLL synthesizer<br>(*)Equipped with a built-in feedback resistor. |
| | Oscillation Stop Detection Function | Stop detection of main clock oscillation, re-oscillation detection function |
| | Voltage Detection Circuit | Available (option(4)) |
| Electric Characteristics | Supply Voltage | VCC1=3.0 to 5.5 V, VCC2=2.7V to VCC1 (f(BCLK=24MHz)<br>VCC1=2.7 to 5.5 V, VCC2=2.7V to VCC1 (f(BCLK=10MHz) |
| | Power Consumption | 14 mA (VCC1=VCC2=5V, f(BCLK)=24MHz)<br>8 mA (VCC1=VCC2=3V, f(BCLK)=10MHz)<br>1.8μA (VCC1=VCC2=3V, f(XCIN)=32kHz, wait mode)<br>0.7μA (VCC1=VCC2=3V, stop mode) |
| Flash memory version | Program/Erase Supply Voltage | 3.3±0.3 V or 5.0±0.5 V |
| | Program and Erase Endurance | 100 times (all area)<br>or 1,000 times (user ROM area without block A and block 1)<br>/ 10,000 times (block A, block 1) (3) |
| Operating Ambient Temperature | | -20 to 85°C,<br>-40 to 85°C (3) |
| Package | | 128-pin plastic mold LQFP |

NOTES:
1. I2C bus is a registered trademark of Koninklijke Philips Electronics N. V.
2. IEBus is a registered trademark of NEC Electronics Corporation.
3. See **Table 1.8 Product Code** for the program and erase endurance, and operating ambient temperature. In addition 1,000 times/10,000 times are under development as of Jul., 2005. Please inquire about a release schedule.
4. All options are on request basis.

**Table 1.2 Performance Outline of M16C/62P Group (M16C/62P, M16C/62PT)(100-pin version)**

| | Item | Performance | |
|---|---|---|---|
| | | M16C/62P | M16C/62PT(4) |
| CPU | Number of Basic Instructions | 91 instructions | |
| | Minimum Instruction Execution Time | 41.7ns(f(BCLK)=24MHz, VCC1=3.3 to 5.5V)<br>100ns(f(BCLK)=10MHz, VCC1=2.7 to 5.5V) | 41.7ns(f(BCLK)=24MHz, VCC1=4.0 to 5.5V) |
| | Operating Mode | Single-chip, memory expansion and microprocessor mode | Single-chip |
| | Address Space | 1 Mbyte (Available to 4 Mbytes by memory space expansion function) | 1 Mbyte |
| | Memory Capacity | See **Table 1.4 to 1.7 Product List** | |
| Peripheral Function | Port | Input/Output : 87 pins, Input : 1 pin | |
| | Multifunction Timer | Timer A : 16 bits x 5 channels, Timer B : 16 bits x 6 channels,<br>Three phase motor control circuit | |
| | Serial Interface | 3 channels<br>Clock synchronous, UART, I2C bus(1), IEBus(2)<br>2 channels<br>Clock synchronous | |
| | A/D Converter | 10-bit A/D converter: 1 circuit, 26 channels | |
| | D/A Converter | 8 bits x 2 channels | |
| | DMAC | 2 channels | |
| | CRC Calculation Circuit | CCITT-CRC | |
| | Watchdog Timer | 15 bits x 1 channel (with prescaler) | |
| | Interrupt | Internal: 29 sources, External: 8 sources, Software: 4 sources, Priority level: 7 levels | |
| | Clock Generation Circuit | 4 circuits<br>Main clock generation circuit (*), Subclock generation circuit (*),<br>On-chip oscillator, PLL synthesizer<br>(*)Equipped with a built-in feedback resistor. | |
| | Oscillation Stop Detection Function | Stop detection of main clock oscillation, re-oscillation detection function | |
| | Voltage Detection Circuit | Available (option (5)) | Absent |
| Electric Characteristics | Supply Voltage | VCC1=3.0 to 5.5 V, VCC2=2.7V to VCC1 (f(BCLK=24MHz)<br>VCC1=2.7 to 5.5 V, VCC2=2.7V to VCC1 (f(BCLK=10MHz) | VCC1=VCC2=4.0 to 5.5V (f(BCLK=24MHz) |
| | Power Consumption | 14 mA (VCC1=VCC2=5V, f(BCLK)=24MHz)<br>8 mA (VCC1=VCC2=3V, f(BCLK)=10MHz)<br>1.8µA (VCC1=VCC2=3V, f(XCIN)=32kHz, wait mode)<br>0.7µA (VCC1=VCC2=3V, stop mode) | 14 mA (VCC1=VCC2=5V, f(BCLK)=24MHz)<br>2.0µA (VCC1=VCC2=5V, f(XCIN)=32kHz, wait mode)<br>0.8µA (VCC1=VCC2=5V, stop mode) |
| Flash memory version | Program/Erase Supply Voltage | 3.3±0.3 V or 5.0±0.5 V | 5.0±0.5 V |
| | Program and Erase Endurance | 100 times (all area)<br>or 1,000 times (user ROM area without block A and block 1)<br>/ 10,000 times (block A, block 1) (3) | |
| Operating Ambient Temperature | | -20 to 85°C,<br>-40 to 85°C (3) | T version : -40 to 85°C<br>V version : -40 to 125°C |
| Package | | 100-pin plastic mold QFP, LQFP | |

NOTES:
1. I2C bus is a registered trademark of Koninklijke Philips Electronics N. V.
2. IEBus is a registered trademark of NEC Electronics Corporation.
3. See **Table 1.8 and 1.9 Product Code** for the program and erase endurance, and operating ambient temperature.
   In addition 1,000 times/10,000 times are under development as of Jul., 2005. Please inquire about a release schedule.
4. Use the M16C/62PT on VCC1=VCC2
5. All options are on request basis.

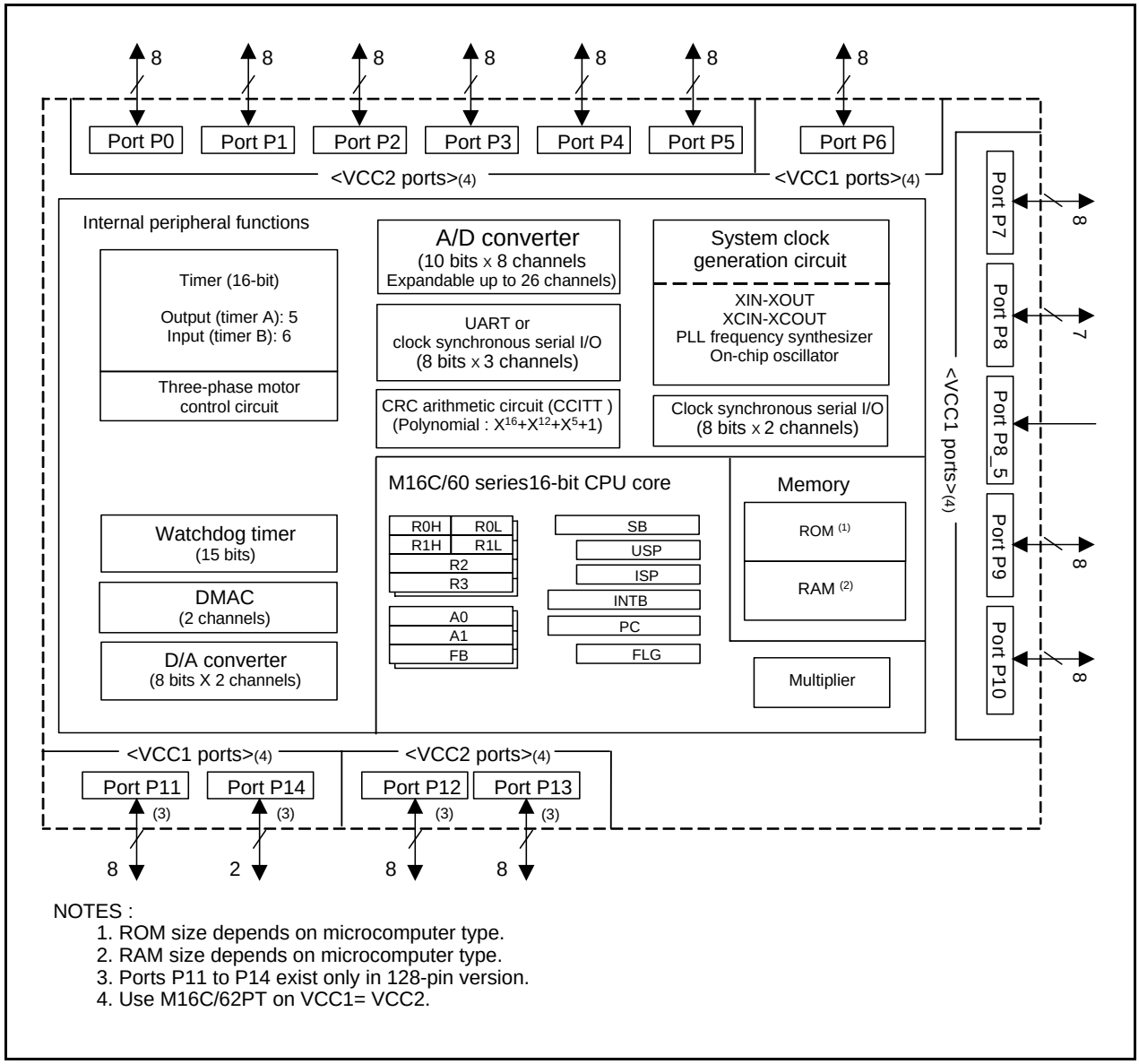
**Table 1.3 Performance Outline of M16C/62P Group (M16C/62P, M16C/62PT)(80-pin version)**

| | Item | Performance | |
|---|---|---|---|
| | | M16C/62P | M16C/62PT(4) |
| CPU | Number of Basic Instructions | 91 instructions | |
| | Minimum Instruction Execution Time | 41.7ns(f(BCLK)=24MHz, VCC1=3.3 to 5.5V)<br>100ns(f(BCLK)=10MHz, VCC1=2.7 to 5.5V) | 41.7ns(f(BCLK)=24MHz, VCC1=4.0 to 5.5V) |
| | Operating Mode | Single-chip mode | |
| | Address Space | 1 Mbyte | |
| | Memory Capacity | See **Table 1.4 to 1.7 Product List** | |
| Peripheral Function | Port | Input/Output : 70 pins, Input : 1 pin | |
| | Multifunction Timer | Timer A : 16 bits x 5 channels (Timer A1 and A2 are internal timer),<br>Timer B : 16 bits x 6 channels (Timer B1 is internal timer) | |
| | Serial Interface | 2 channels<br>Clock synchronous, UART, I2C bus(1), IEBus(2)<br>1 channel<br>Clock synchronous, I2C bus(1), IEBus(2)<br>2 channels<br>Clock synchronous (1 channel is only transmission) | |
| | A/D Converter | 10-bit A/D converter: 1 circuit, 26 channels | |
| | D/A Converter | 8 bits x 2 channels | |
| | DMAC | 2 channels | |
| | CRC Calculation Circuit | CCITT-CRC | |
| | Watchdog Timer | 15 bits x 1 channel (with prescaler) | |
| | Interrupt | Internal: 29 sources, External: 5 sources, Software: 4 sources, Priority level: 7 levels | |
| | Clock Generation Circuit | 4 circuits<br>Main clock generation circuit (*), Subclock generation circuit (*),<br>On-chip oscillator, PLL synthesizer<br>(*)Equipped with a built-in feedback resistor. | |
| | Oscillation Stop Detection Function | Stop detection of main clock oscillation, re-oscillation detection function | |
| | Voltage Detection Circuit | Available (option (4)) | Absent |
| Electric Characteristics | Supply Voltage | VCC1=3.0 to 5.5 V, (f(BCLK=24MHz)<br>VCC1=2.7 to 5.5 V, (f(BCLK=10MHz) | VCC1=4.0 to 5.5V, (f(BCLK=24MHz) |
| | Power Consumption | 14 mA (VCC1=5V, f(BCLK)=24MHz)<br>8 mA (VCC1=3V, f(BCLK)=10MHz)<br>1.8μA (VCC1=3V, f(XCIN)=32kHz, wait mode)<br>0.7μA (VCC1=3V, stop mode) | 14 mA (VCC1=5V, f(BCLK)=24MHz)<br>2.0μA (VCC1=5V, f(XCIN)=32kHz, wait mode)<br>0.8μA (VCC1=5V, stop mode) |
| Flash memory version | Program/Erase Supply Voltage | 3.3 ± 0.3V or 5.0 ± 0.5V | 5.0 ± 0.5V |
| | Program and Erase Endurance | 100 times (all area)<br>or 1,000 times (user ROM area without block A and block 1)<br>/ 10,000 times (block A, block 1) (3) | |
| Operating Ambient Temperature | | -20 to 85°C,<br>-40 to 85°C (3) | T version : -40 to 85°C<br>V version : -40 to 125°C |
| Package | | 80-pin plastic mold QFP | |

NOTES:
1. I2C bus is a registered trademark of Koninklijke Philips Electronics N. V.
2. IEBus is a registered trademark of NEC Electronics Corporation.
3. See **Table 1.8 and 1.9 Product Code** for the program and erase endurance, and operating ambient temperature.
   In addition 1,000 times/10,000 times are under development as of Jul., 2005. Please inquire about a release schedule.
4. All options are on request basis.

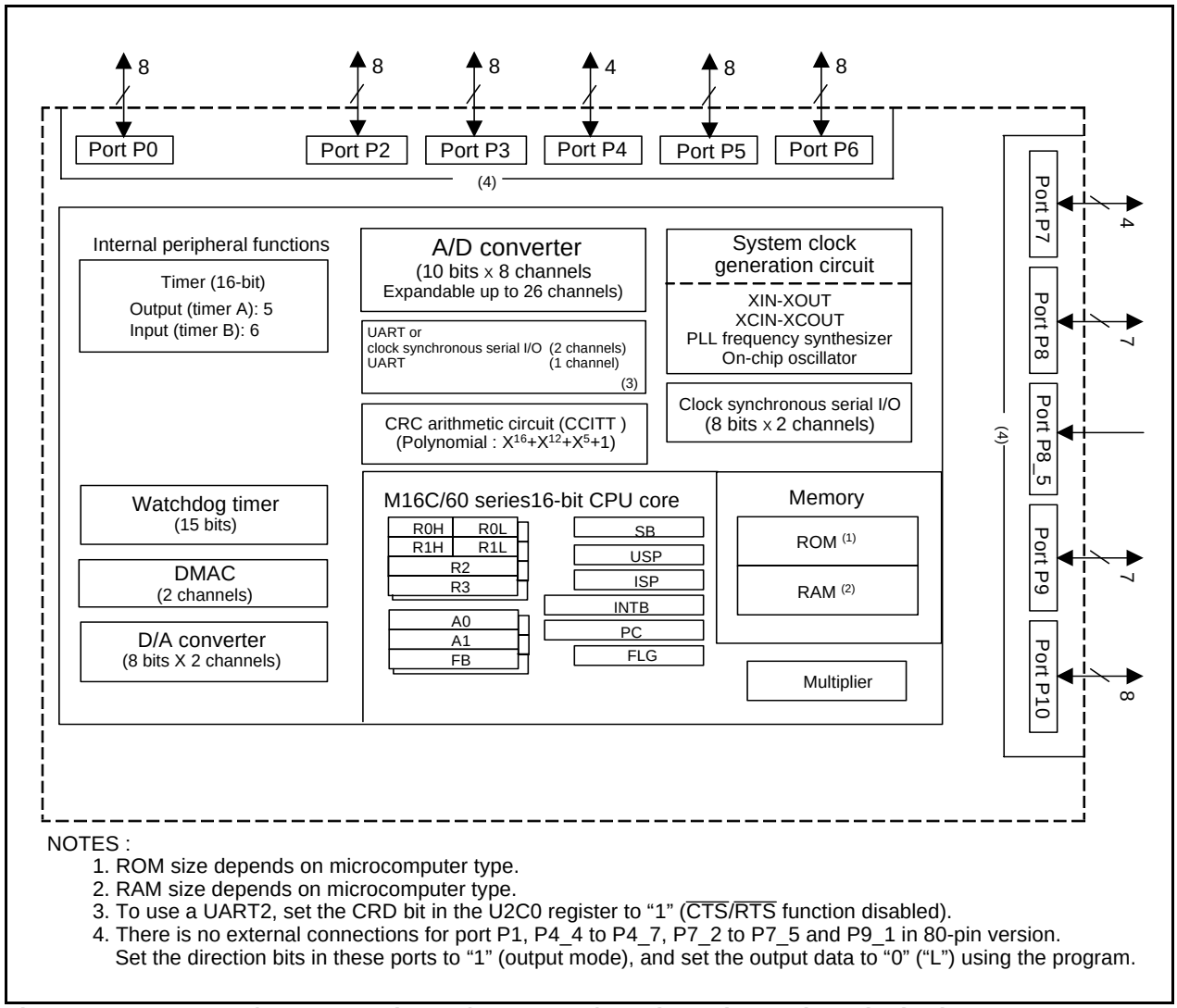
## 1.3 Block Diagram

Figure 1.1 is a M16C/62P Group (M16C/62P, M16C/62PT) 128-pin and 100-pin version Block Diagram, Figure 1.2 is a M16C/62P Group (M16C/62P, M16C/62PT) 80-pin version Block Diagram.




NOTES :
1. ROM size depends on microcomputer type.
2. RAM size depends on microcomputer type.
3. Ports P11 to P14 exist only in 128-pin version.
4. Use M16C/62PT on VCC1= VCC2.

**Figure 1.1 M16C/62P Group (M16C/62P, M16C/62PT) 128-pin and 100-pin version Block Diagram**




NOTES :
1. ROM size depends on microcomputer type.
2. RAM size depends on microcomputer type.
3. To use a UART2, set the CRD bit in the U2C0 register to “1” ($\overline{\text{CTS}}$/$\overline{\text{RTS}}$ function disabled).
4. There is no external connections for port P1, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version. Set the direction bits in these ports to “1” (output mode), and set the output data to “0” (“L”) using the program.

**Figure 1.2 M16C/62P Group (M16C/62P, M16C/62PT) 80-pin version Block Diagram**

## 1.4 Product List

Table 1.4 to 1.7 list the product list, Figure 1.3 shows the Type No., Memory Size, and Package, Table 1.8 lists the Product Code of Flash Memory version and ROMless version for M16C/62P, and Table 1.9 lists the Product Code of Flash Memory version for M16C/62PT. Figure 1.4 shows the Marking Diagram of Flash Memory version and ROM-less version for M16C/62P (Top View), and Figure 1.5 shows the Marking Diagram of Flash Memory version for M16C/62PT (Top View) at the time of ROM order.

**Table 1.4 Product List (1) (M16C/62P) As of Dec. 2005**

| Type No. | ROM Capacity | RAM Capacity | Package Type (1) | Remarks |
|---|---|---|---|---|
| M30622M6P-XXXFP | 48 Kbytes | 4 Kbytes | PRQP0100JB-A | Mask ROM version |
| M30622M6P-XXXGP | | | PLQP0100KB-A | |
| M30622M8P-XXXFP | 64 Kbytes | 4 Kbytes | PRQP0100JB-A | |
| M30622M8P-XXXGP | | | PLQP0100KB-A | |
| M30623M8P-XXXGP | | | PRQP0080JA-A | |
| M30622MAP-XXXFP | 96 Kbytes | 5 Kbytes | PRQP0100JB-A | |
| M30622MAP-XXXGP | | | PLQP0100KB-A | |
| M30623MAP-XXXGP | | | PRQP0080JA-A | |
| M30620MCP-XXXFP | 128 Kbytes | 10 Kbytes | PRQP0100JB-A | |
| M30620MCP-XXXGP | | | PLQP0100KB-A | |
| M30621MCP-XXXGP | | | PRQP0080JA-A | |
| M30622MEP-XXXFP | 192 Kbytes | 12 Kbytes | PRQP0100JB-A | |
| M30622MEP-XXXGP | | | PLQP0100KB-A | |
| M30623MEP-XXXGP | | | PLQP0128KB-A | |
| M30622MGP-XXXFP | 256 Kbytes | 12 Kbytes | PRQP0100JB-A | |
| M30622MGP-XXXGP | | | PLQP0100KB-A | |
| M30623MGP-XXXGP | | | PLQP0128KB-A | |
| M30624MGP-XXXFP | | 20 Kbytes | PRQP0100JB-A | |
| M30624MGP-XXXGP | | | PLQP0100KB-A | |
| M30625MGP-XXXGP | | | PLQP0128KB-A | |
| M30622MWP-XXXFP | 320 Kbytes | 16 Kbytes | PRQP0100JB-A | |
| M30622MWP-XXXGP | | | PLQP0100KB-A | |
| M30623MWP-XXXGP | | | PLQP0128KB-A | |
| M30624MWP-XXXFP | | 24 Kbytes | PRQP0100JB-A | |
| M30624MWP-XXXGP | | | PLQP0100KB-A | |
| M30625MWP-XXXGP | | | PLQP0128KB-A | |
| M30626MWP-XXXFP | | 31 Kbytes | PRQP0100JB-A | |
| M30626MWP-XXXGP | | | PLQP0100KB-A | |
| M30627MWP-XXXGP | | | PLQP0128KB-A | |

(D): Under development

NOTES:

1. The old package type numbers of each package type are as follows.
   PLQP0128KB-A : 128P6Q-A,
   PRQP0100JB-A : 100P6S-A,
   PLQP0100KB-A : 100P6Q-A,
   PRQP0080JA-A : 80P6S-A

**Table 1.5 Product List (2) (M16C/62P) As of Dec. 2005**

| Type No. | ROM Capacity | RAM Capacity | Package Type (1) | Remarks |
|---|---|---|---|---|
| M30622MHP-XXXFP | 384 Kbytes | 16 Kbytes | PRQP0100JB-A | Mask ROM version |
| M30622MHP-XXXGP | | | PLQP0100KB-A | |
| M30623MHP-XXXGP | | | PLQP0128KB-A | |
| M30624MHP-XXXFP | | 24 Kbytes | PRQP0100JB-A | |
| M30624MHP-XXXGP | | | PLQP0100KB-A | |
| M30625MHP-XXXGP | | | PLQP0128KB-A | |
| M30626MHP-XXXFP | | 31 Kbytes | PRQP0100JB-A | |
| M30626MHP-XXXGP | | | PLQP0100KB-A | |
| M30627MHP-XXXGP | | | PLQP0128KB-A | |
| M30626MJP-XXXFP (D) | 512 Kbytes | 31 Kbytes | PRQP0100JB-A | |
| M30626MJP-XXXGP (D) | | | PLQP0100KB-A | |
| M30627MJP-XXXGP (D) | | | PLQP0128KB-A | |
| M30622F8PFP | 64K+4 Kbytes | 4 Kbytes | PRQP0100JB-A | Flash memory version (2) |
| M30622F8PGP | | | PLQP0100KB-A | |
| M30623F8PGP | | | PRQP0080JA-A | |
| M30620FCPFP | 128K+4 Kbytes | 10 Kbytes | PRQP0100JB-A | |
| M30620FCPGP | | | PLQP0100KB-A | |
| M30621FCPGP | | | PRQP0080JA-A | |
| M3062LFGPFP(3) (D) | 256K+4 Kbytes | 20 Kbytes | PRQP0100JB-A | |
| M3062LFGPGP(3) (D) | | | PLQP0100KB-A | |
| M30625FGPGP | | | PLQP0128KB-A | |
| M30626FHPFP | 384K+4 Kbytes | 31 Kbytes | PRQP0100JB-A | |
| M30626FHPGP | | | PLQP0100KB-A | |
| M30627FHPGP | | | PLQP0128KB-A | |
| M30626FJPFP | 512K+4 Kbytes | 31 Kbytes | PRQP0100JB-A | |
| M30626FJPGP | | | PLQP0100KB-A | |
| M30627FJPGP | | | PLQP0128KB-A | |
| M30622SPFP | – | 4 Kbytes | PRQP0100JB-A | ROM-less version |
| M30622SPGP | | | PLQP0100KB-A | |
| M30620SPFP | | 10 Kbytes | PRQP0100JB-A | |
| M30620SPGP | | | PLQP0100KB-A | |
| M30624SPFP (D) | – | 20 Kbytes | PRQP0100JB-A | |
| M30624SPGP (D) | | | PLQP0100KB-A | |
| M30626SPFP (D) | | 31 Kbytes | PRQP0100JB-A | |
| M30626SPGP (D) | | | PLQP0100KB-A | |

(D): Under development

NOTES:

1. The old package type numbers of each package type are as follows.
   PLQP0128KB-A : 128P6Q-A,
   PRQP0100JB-A : 100P6S-A,
   PLQP0100KB-A : 100P6Q-A,
   PRQP0080JA-A : 80P6S-A
2. In the flash memory version, there is 4K bytes area (block A).
3. Please use M3062LFGPFP and M3062LFGPGP for your new system instead of M30624FGPFP and M30624FGPGP. The M16C/62P Group (M16C/62P, M16C/62PT) hardware manual is still good for M30624FGPFP and M30624FGPGP.

| | | | | |
|---|---|---|---|---|
| M30624FGPFP | 256K+4 Kbytes | 20 Kbytes | PRQP0100JB-A | Flash memory version |
| M30624FGPGP | | | PLQP0100KB-A | |

**Table 1.6 Product List (3) (T version (M16C/62PT)) As of Dec. 2005**

| Type No. | ROM Capacity | RAM Capacity | Package Type (1) | Remarks | |
|---|---|---|---|---|---|
| M3062CM6T-XXXFP (D) | 48 Kbytes | 4 Kbytes | PRQP0100JB-A | Mask ROM version | T Version (High reliability 85°C version) |
| M3062CM6T-XXXGP (D) | | | PLQP0100KB-A | | |
| M3062EM6T-XXXGP (P) | | | PRQP0080JA-A | | |
| M3062CM8T-XXXFP (D) | 64 Kbytes | 4 Kbytes | PRQP0100JB-A | | |
| M3062CM8T-XXXGP (D) | | | PLQP0100KB-A | | |
| M3062EM8T-XXXGP (P) | | | PRQP0080JA-A | | |
| M3062CMAT-XXXFP (D) | 96 Kbytes | 5 Kbytes | PRQP0100JB-A | | |
| M3062CMAT-XXXGP (D) | | | PLQP0100KB-A | | |
| M3062EMAT-XXXGP (P) | | | PRQP0080JA-A | | |
| M3062AMCT-XXXFP (D) | 128 Kbytes | 10 Kbytes | PRQP0100JB-A | | |
| M3062AMCT-XXXGP (D) | | | PLQP0100KB-A | | |
| M3062BMCT-XXXGP (P) | | | PRQP0080JA-A | | |
| M3062CF8TFP (D) | 64 K+4 Kbytes | 4 Kbytes | PRQP0100JB-A | Flash memory version (2) | |
| M3062CF8TGP | | | PLQP0100KB-A | | |
| M3062AFCTFP (D) | 128K+4 Kbytes | 10 Kbytes | PRQP0100JB-A | | |
| M3062AFCTGP (D) | | | PLQP0100KB-A | | |
| M3062BFCTGP (P) | | | PRQP0080JA-A | | |
| M3062JFHTFP (D) | 384K+4 Kbytes | 31 Kbytes | PRQP0100JB-A | | |
| M3062JFHTGP (D) | | | PLQP0100KB-A | | |

(D): Under development
(P): Under planning
NOTES:

1. The old package type numbers of each package type are as follows.
   PRQP0100JB-A : 100P6S-A,
   PLQP0100KB-A : 100P6Q-A,
   PRQP0080JA-A : 80P6S-A
2. In the flash memory version, there is 4K bytes area (block A).

**Table 1.7 Product List (4) (V version (M16C/62PT)) As of Dec. 2005**

| Type No. | ROM Capacity | RAM Capacity | Package Type(1) | Remarks | |
|---|---|---|---|---|---|
| M3062CM6V-XXXFP (P) | 48 Kbytes | 4 Kbytes | PRQP0100JB-A | Mask ROM version | V Version (High reliability 125°C version) |
| M3062CM6V-XXXGP (P) | | | PLQP0100KB-A | | |
| M3062EM6V-XXXGP (P) | | | PRQP0080JA-A | | |
| M3062CM8V-XXXFP (P) | 64 Kbytes | 4 Kbytes | PRQP0100JB-A | | |
| M3062CM8V-XXXGP (P) | | | PLQP0100KB-A | | |
| M3062EM8V-XXXGP (P) | | | PRQP0080JA-A | | |
| M3062CMAV-XXXFP (P) | 96 Kbytes | 5 Kbytes | PRQP0100JB-A | | |
| M3062CMAV-XXXGP (P) | | | PLQP0100KB-A | | |
| M3062EMAV-XXXGP (P) | | | PRQP0080JA-A | | |
| M3062AMCV-XXXFP (D) | 128 Kbytes | 10 Kbytes | PRQP0100JB-A | | |
| M3062AMCV-XXXGP (D) | | | PLQP0100KB-A | | |
| M3062BMCV-XXXGP (P) | | | PRQP0080JA-A | | |
| M3062AFCVFP (D) | 128K+4 Kbytes | 10 Kbytes | PRQP0100JB-A | Flash memory version (2) | |
| M3062AFCVGP (D) | | | PLQP0100KB-A | | |
| M3062BFCVGP (P) | | | PRQP0080JA-A | | |
| M3062JFHVFP (P) | 384K+4 Kbytes | 31 Kbytes | PRQP0100JB-A | | |
| M3062JFHVGP (P) | | | PLQP0100KB-A | | |

(D): Under development
(P): Under planning
NOTES:
1. The old package type numbers of each package type are as follows.
   PLQP0128KB-A : 128P6Q-A,
   PRQP0100JB-A : 100P6S-A,
   PLQP0100KB-A : 100P6Q-A,
   PRQP0080JA-A : 80P6S-A
2. In the flash memory version, there is 4K bytes area (block A).

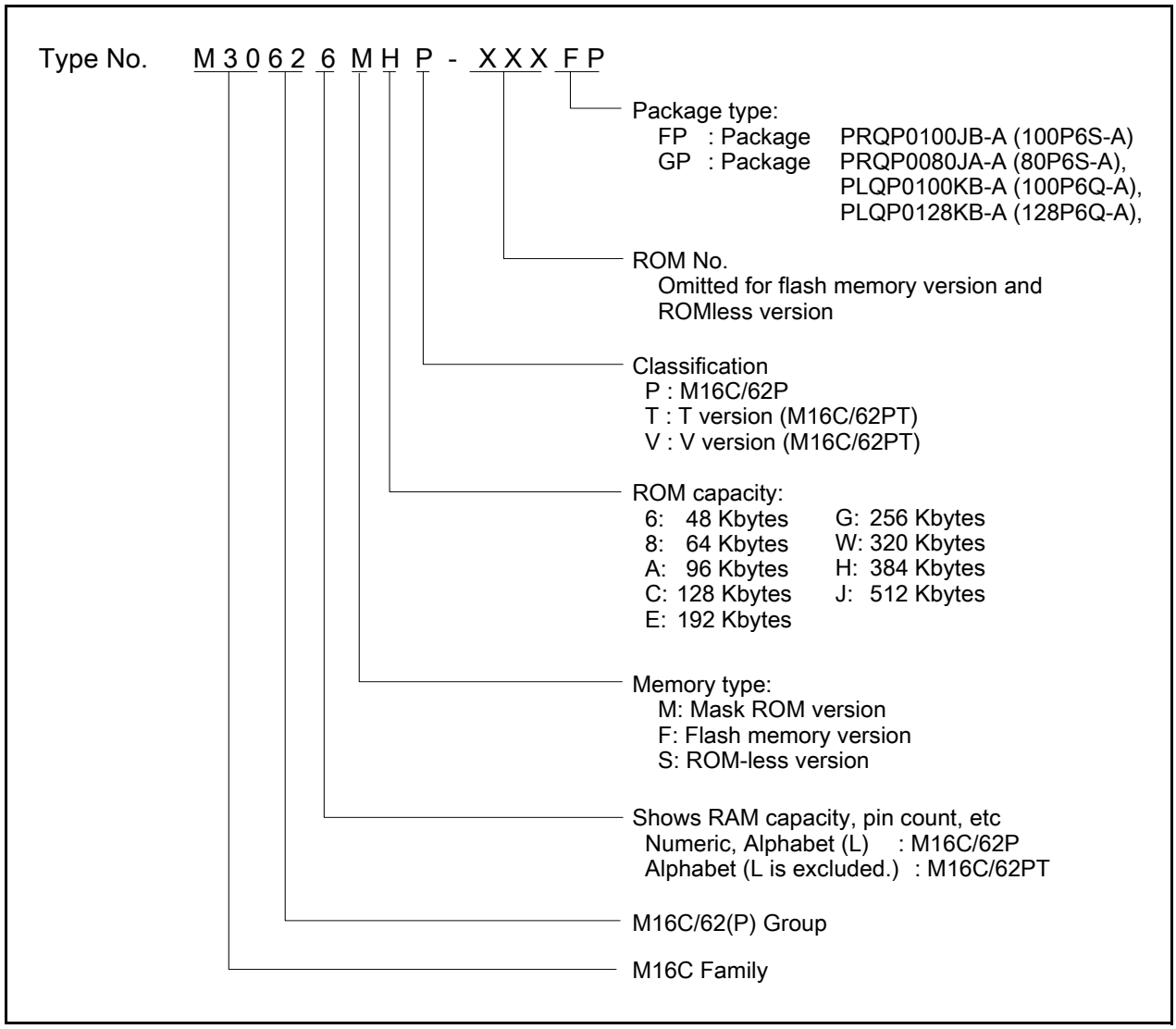



**Figure 1.3 Type No., Memory Size, and Package**

**Table 1.8 Product Code of Flash Memory version and ROMless version for M16C/62P**

| | Product Code | Package | Internal ROM (User ROM Area Without Block A, Block 1) | | Internal ROM (Block A, Block 1) | | Operating Ambient Temperature |
|---|---|---|---|---|---|---|---|
| | | | Program and Erase Endurance | Temperature Range | Program and Erase Endurance | Temperature Range | |
| Flash memory Version | D3 | Lead-included | 100 | 0°C to 60°C | 100 | 0°C to 60°C | -40°C to 85°C |
| | D5 | | | | | | -20°C to 85°C |
| | D7 | | 1,000 | | 10,000 | -40°C to 85°C | -40°C to 85°C |
| | D9 | | | | | -20°C to 85°C | -20°C to 85°C |
| | U3 | Lead-free | 100 | | 100 | 0°C to 60°C | -40°C to 85°C |
| | U5 | | | | | | -20°C to 85°C |
| | U7 | | 1,000 | | 10,000 | -40°C to 85°C | -40°C to 85°C |
| | U9 | | | | | -20°C to 85°C | -20°C to 85°C |
| ROM-less version | D3 | Lead-included | – | – | – | – | -40°C to 85°C |
| | D5 | | | | | | -20°C to 85°C |
| | U3 | Lead-free | – | – | – | – | -40°C to 85°C |
| | U5 | | | | | | -20°C to 85°C |

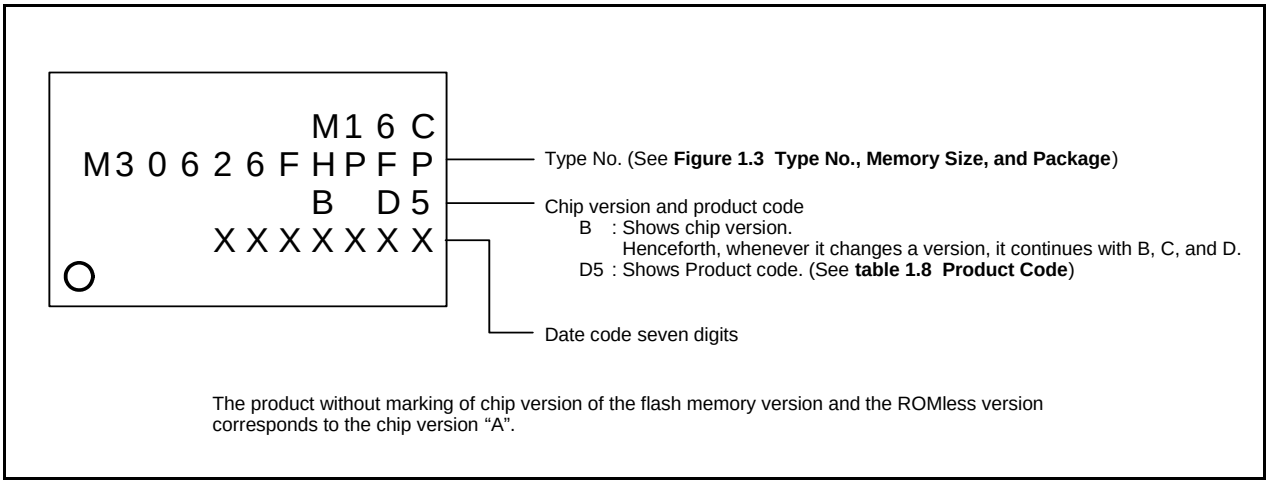



**Figure 1.4 Marking Diagram of Flash Memory version and ROM-less version for M16C/62P (Top View)**

**Table 1.9 Product Code of Flash Memory version for M16C/62PT**

| | | Product Code | Package | Internal ROM (User ROM Area Without Block A, Block 1) | | Internal ROM (Block A, Block 1) | | Operating Ambient Temperature |
|---|---|---|---|---|---|---|---|---|
| | | | | Program and Erase Endurance | Temperature Range | Program and Erase Endurance | Temperature Range | |
| Flash memory Version | T Version | B | Lead-included | 100 | 0°C to 60°C | 100 | 0°C to 60°C | -40°C to 85°C |
| | V Version | | | | | | | -40°C to 125°C |
| | T Version | B7 | | 1,000 | | 10,000 | -40°C to 85°C | -40°C to 85°C |
| | V Version | | | | | | -40°C to 125°C | -40°C to 125°C |
| | T Version | U | Lead-free | 100 | | 100 | 0°C to 60°C | -40°C to 85°C |
| | V Version | | | | | | | -40°C to 125°C |
| | T Version | U7 | | 1,000 | | 10,000 | -40°C to 85°C | -40°C to 85°C |
| | V Version | | | | | | -40°C to 125°C | -40°C to 125°C |

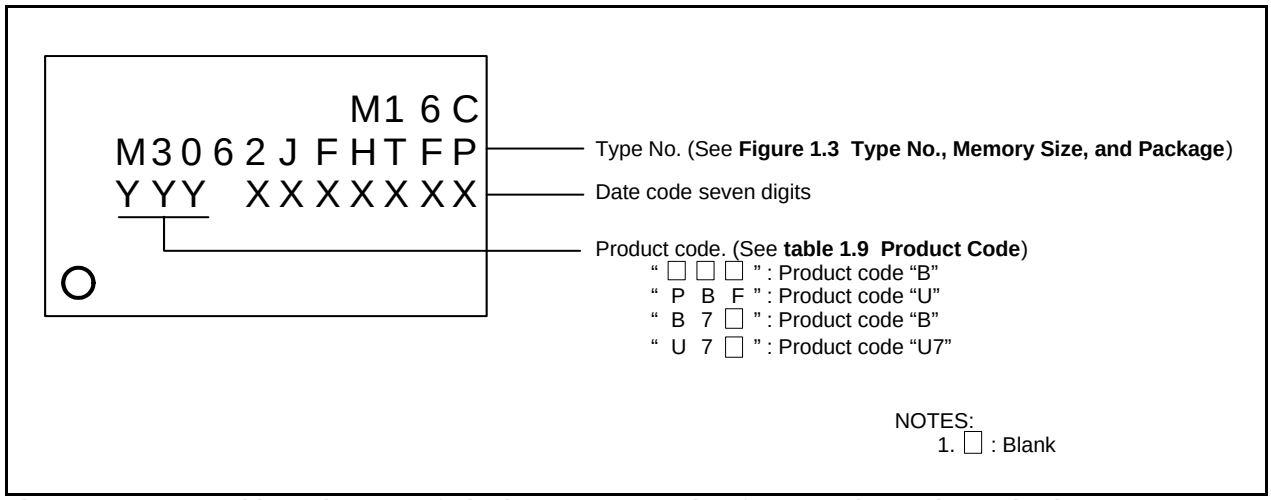



**Figure 1.5 Marking Diagram of Flash Memory version for M16C/62PT (Top View)**

## 1.5 Pin Configuration

Figures 1.6 to 1.9 show the Pin Configuration (Top View).

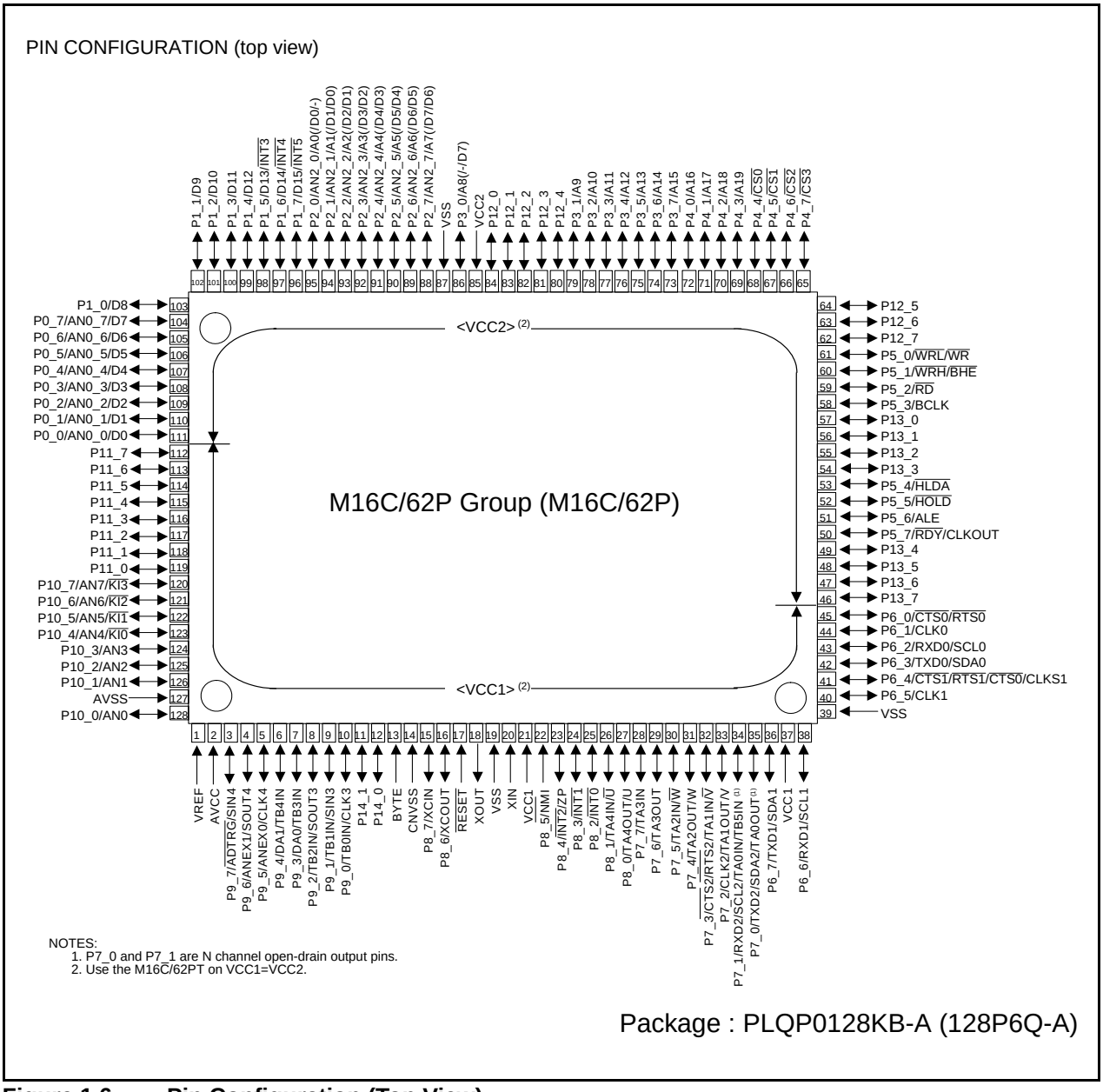



**Figure 1.6 Pin Configuration (Top View)**

**Table 1.10 Pin Characteristics for 128-Pin Package (1)**

| Pin No. | Control Pin | Port | Interrupt Pin | Timer Pin | UART Pin | Analog Pin | Bus Control Pin |
|---|---|---|---|---|---|---|---|
| 1 | VREF | | | | | | |
| 2 | AVCC | | | | | | |
| 3 | | P9_7 | | | SIN4 | $\overline{\text{ADTRG}}$ | |
| 4 | | P9_6 | | | SOUT4 | ANEX1 | |
| 5 | | P9_5 | | | CLK4 | ANEX0 | |
| 6 | | P9_4 | | TB4IN | | DA1 | |
| 7 | | P9_3 | | TB3IN | | DA0 | |
| 8 | | P9_2 | | TB2IN | SOUT3 | | |
| 9 | | P9_1 | | TB1IN | SIN3 | | |
| 10 | | P9_0 | | TB0IN | CLK3 | | |
| 11 | | P14_1 | | | | | |
| 12 | | P14_0 | | | | | |
| 13 | BYTE | | | | | | |
| 14 | CNVSS | | | | | | |
| 15 | XCIN | P8_7 | | | | | |
| 16 | XCOUT | P8_6 | | | | | |
| 17 | $\overline{\text{RESET}}$ | | | | | | |
| 18 | XOUT | | | | | | |
| 19 | VSS | | | | | | |
| 20 | XIN | | | | | | |
| 21 | VCC1 | | | | | | |
| 22 | | P8_5 | $\overline{\text{NMI}}$ | | | | |
| 23 | | P8_4 | $\overline{\text{INT2}}$ | ZP | | | |
| 24 | | P8_3 | $\overline{\text{INT1}}$ | | | | |
| 25 | | P8_2 | $\overline{\text{INT0}}$ | | | | |
| 26 | | P8_1 | | TA4IN/$\overline{\text{U}}$ | | | |
| 27 | | P8_0 | | TA4OUT/U | | | |
| 28 | | P7_7 | | TA3IN | | | |
| 29 | | P7_6 | | TA3OUT | | | |
| 30 | | P7_5 | | TA2IN/$\overline{\text{W}}$ | | | |
| 31 | | P7_4 | | TA2OUT/W | | | |
| 32 | | P7_3 | | TA1IN/$\overline{\text{V}}$ | $\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$ | | |
| 33 | | P7_2 | | TA1OUT/V | CLK2 | | |
| 34 | | P7_1 | | TA0IN/TB5IN | RXD2/SCL2 | | |
| 35 | | P7_0 | | TA0OUT | TXD2/SDA2 | | |
| 36 | | P6_7 | | | TXD1/SDA1 | | |
| 37 | VCC1 | | | | | | |
| 38 | | P6_6 | | | RXD1/SCL1 | | |
| 39 | VSS | | | | | | |
| 40 | | P6_5 | | | CLK1 | | |
| 41 | | P6_4 | | | $\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$/$\overline{\text{CTS0}}$/CLKS1 | | |
| 42 | | P6_3 | | | TXD0/SDA0 | | |
| 43 | | P6_2 | | | RXD0/SCL0 | | |
| 44 | | P6_1 | | | CLK0 | | |
| 45 | | P6_0 | | | $\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$ | | |
| 46 | | P13_7 | | | | | |
| 47 | | P13_6 | | | | | |
| 48 | | P13_5 | | | | | |
| 49 | | P13_4 | | | | | |
| 50 | | P5_7 | | | | | $\overline{\text{RDY}}$/CLKOUT |

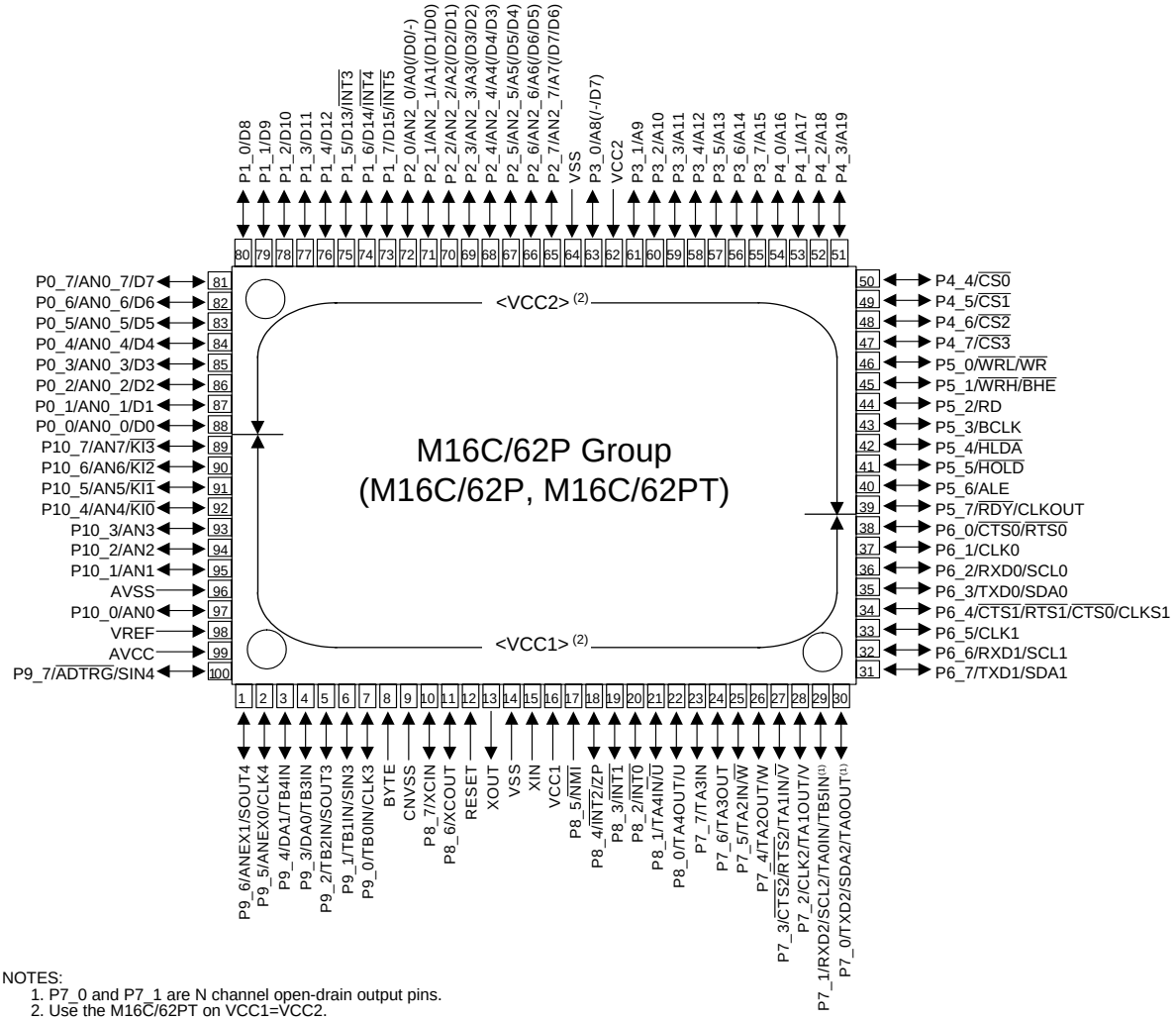
**Table 1.11 Pin Characteristics for 128-Pin Package (2)**

| Pin No. | Control Pin | Port | Interrupt Pin | Timer Pin | UART Pin | Analog Pin | Bus Control Pin |
|---|---|---|---|---|---|---|---|
| 51 | | P5_6 | | | | | ALE |
| 52 | | P5_5 | | | | | $\overline{\text{HOLD}}$ |
| 53 | | P5_4 | | | | | $\overline{\text{HLDA}}$ |
| 54 | | P13_3 | | | | | |
| 55 | | P13_2 | | | | | |
| 56 | | P13_1 | | | | | |
| 57 | | P13_0 | | | | | |
| 58 | | P5_3 | | | | | BCLK |
| 59 | | P5_2 | | | | | $\overline{\text{RD}}$ |
| 60 | | P5_1 | | | | | $\overline{\text{WRH}}$/$\overline{\text{BHE}}$ |
| 61 | | P5_0 | | | | | $\overline{\text{WRL}}$/$\overline{\text{WR}}$ |
| 62 | | P12_7 | | | | | |
| 63 | | P12_6 | | | | | |
| 64 | | P12_5 | | | | | |
| 65 | | P4_7 | | | | | $\overline{\text{CS3}}$ |
| 66 | | P4_6 | | | | | $\overline{\text{CS2}}$ |
| 67 | | P4_5 | | | | | $\overline{\text{CS1}}$ |
| 68 | | P4_4 | | | | | $\overline{\text{CS0}}$ |
| 69 | | P4_3 | | | | | A19 |
| 70 | | P4_2 | | | | | A18 |
| 71 | | P4_1 | | | | | A17 |
| 72 | | P4_0 | | | | | A16 |
| 73 | | P3_7 | | | | | A15 |
| 74 | | P3_6 | | | | | A14 |
| 75 | | P3_5 | | | | | A13 |
| 76 | | P3_4 | | | | | A12 |
| 77 | | P3_3 | | | | | A11 |
| 78 | | P3_2 | | | | | A10 |
| 79 | | P3_1 | | | | | A9 |
| 80 | | P12_4 | | | | | |
| 81 | | P12_3 | | | | | |
| 82 | | P12_2 | | | | | |
| 83 | | P12_1 | | | | | |
| 84 | | P12_0 | | | | | |
| 85 | VCC2 | | | | | | |
| 86 | | P3_0 | | | | | A8(/-/D7) |
| 87 | VSS | | | | | | |
| 88 | | P2_7 | | | | AN2_7 | A7(/D7/D6) |
| 89 | | P2_6 | | | | AN2_6 | A6(/D6/D5) |
| 90 | | P2_5 | | | | AN2_5 | A5(/D5/D4) |
| 91 | | P2_4 | | | | AN2_4 | A4(/D4/D3) |
| 92 | | P2_3 | | | | AN2_3 | A3(/D3/D2) |
| 93 | | P2_2 | | | | AN2_2 | A2(/D2/D1) |
| 94 | | P2_1 | | | | AN2_1 | A1(/D1/D0) |
| 95 | | P2_0 | | | | AN2_0 | A0(/D0/-) |
| 96 | | P1_7 | $\overline{\text{INT5}}$ | | | | D15 |
| 97 | | P1_6 | $\overline{\text{INT4}}$ | | | | D14 |
| 98 | | P1_5 | $\overline{\text{INT3}}$ | | | | D13 |
| 99 | | P1_4 | | | | | D12 |
| 100 | | P1_3 | | | | | D11 |

**Table 1.12 Pin Characteristics for 128-Pin Package (3)**

| Pin No. | Control Pin | Port | Interrupt Pin | Timer Pin | UART Pin | Analog Pin | Bus Control Pin |
|---|---|---|---|---|---|---|---|
| 101 | | P1_2 | | | | | D10 |
| 102 | | P1_1 | | | | | D9 |
| 103 | | P1_0 | | | | | D8 |
| 104 | | P0_7 | | | | AN0_7 | D7 |
| 105 | | P0_6 | | | | AN0_6 | D6 |
| 106 | | P0_5 | | | | AN0_5 | D5 |
| 107 | | P0_4 | | | | AN0_4 | D4 |
| 108 | | P0_3 | | | | AN0_3 | D3 |
| 109 | | P0_2 | | | | AN0_2 | D2 |
| 110 | | P0_1 | | | | AN0_1 | D1 |
| 111 | | P0_0 | | | | AN0_0 | D0 |
| 112 | | P11_7 | | | | | |
| 113 | | P11_6 | | | | | |
| 114 | | P11_5 | | | | | |
| 115 | | P11_4 | | | | | |
| 116 | | P11_3 | | | | | |
| 117 | | P11_2 | | | | | |
| 118 | | P11_1 | | | | | |
| 119 | | P11_0 | | | | | |
| 120 | | P10_7 | $\overline{KI3}$ | | | AN7 | |
| 121 | | P10_6 | $\overline{KI2}$ | | | AN6 | |
| 122 | | P10_5 | $\overline{KI1}$ | | | AN5 | |
| 123 | | P10_4 | $\overline{KI0}$ | | | AN4 | |
| 124 | | P10_3 | | | | AN3 | |
| 125 | | P10_2 | | | | AN2 | |
| 126 | | P10_1 | | | | AN1 | |
| 127 | AVSS | | | | | | |
| 128 | | P10_0 | | | | AN0 | |

PIN CONFIGURATION (top view)

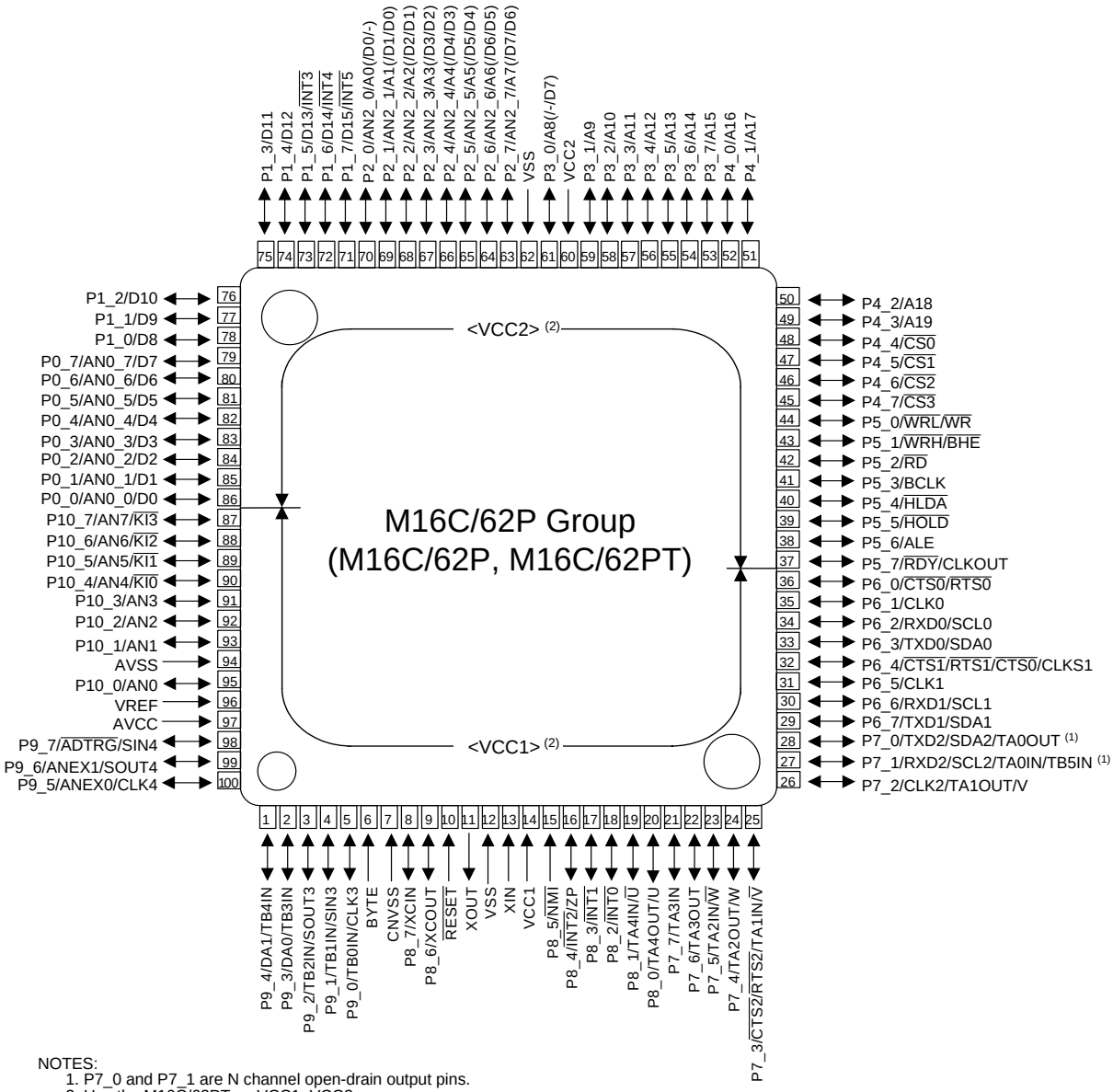



NOTES:
1. P7_0 and P7_1 are N channel open-drain output pins.
2. Use the M16C/62PT on VCC1=VCC2.

Package : PRQP0100JB-A (100P6S-A)

**Figure 1.7 Pin Configuration (Top View)**

PIN CONFIGURATION (top view)




NOTES:
1. P7_0 and P7_1 are N channel open-drain output pins.
2. Use the M16C/62PT on VCC1=VCC2.

Package : PLQP0100KB-A (100P6Q-A)

**Figure 1.8 Pin Configuration (Top View)**

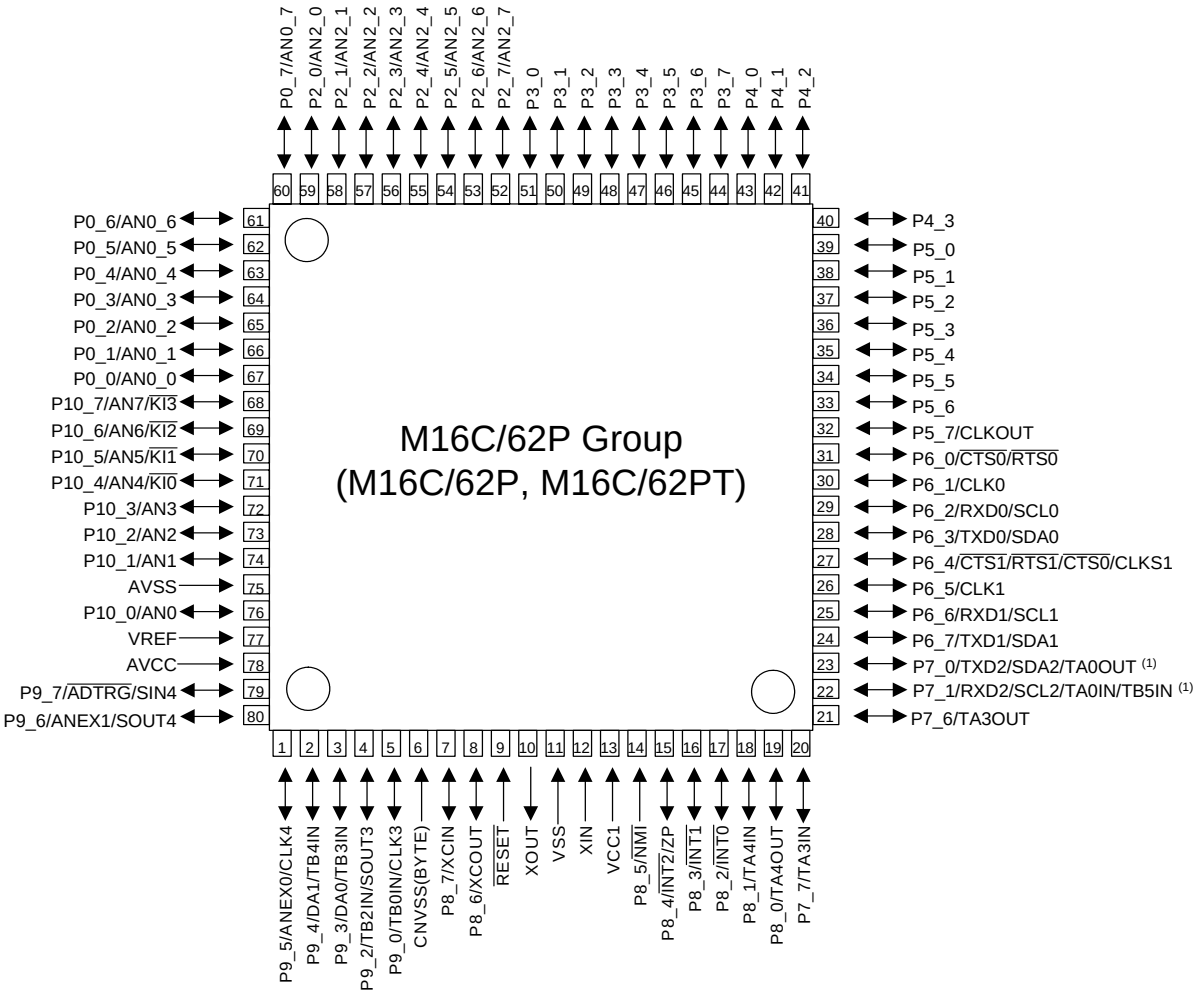
**Table 1.13 Pin Characteristics for 100-Pin Package (1)**

| Pin No. | | Control Pin | Port | Interrupt Pin | Timer Pin | UART Pin | Analog Pin | Bus Control Pin |
|---|---|---|---|---|---|---|---|---|
| FP | GP | | | | | | | |
| 1 | 99 | | P9_6 | | | SOUT4 | ANEX1 | |
| 2 | 100 | | P9_5 | | | CLK4 | ANEX0 | |
| 3 | 1 | | P9_4 | | TB4IN | | DA1 | |
| 4 | 2 | | P9_3 | | TB3IN | | DA0 | |
| 5 | 3 | | P9_2 | | TB2IN | SOUT3 | | |
| 6 | 4 | | P9_1 | | TB1IN | SIN3 | | |
| 7 | 5 | | P9_0 | | TB0IN | CLK3 | | |
| 8 | 6 | BYTE | | | | | | |
| 9 | 7 | CNVSS | | | | | | |
| 10 | 8 | XCIN | P8_7 | | | | | |
| 11 | 9 | XCOUT | P8_6 | | | | | |
| 12 | 10 | $\overline{\text{RESET}}$ | | | | | | |
| 13 | 11 | XOUT | | | | | | |
| 14 | 12 | VSS | | | | | | |
| 15 | 13 | XIN | | | | | | |
| 16 | 14 | VCC1 | | | | | | |
| 17 | 15 | | P8_5 | $\overline{\text{NMI}}$ | | | | |
| 18 | 16 | | P8_4 | $\overline{\text{INT2}}$ | ZP | | | |
| 19 | 17 | | P8_3 | $\overline{\text{INT1}}$ | | | | |
| 20 | 18 | | P8_2 | $\overline{\text{INT0}}$ | | | | |
| 21 | 19 | | P8_1 | | TA4IN/$\overline{\text{U}}$ | | | |
| 22 | 20 | | P8_0 | | TA4OUT/U | | | |
| 23 | 21 | | P7_7 | | TA3IN | | | |
| 24 | 22 | | P7_6 | | TA3OUT | | | |
| 25 | 23 | | P7_5 | | TA2IN/$\overline{\text{W}}$ | | | |
| 26 | 24 | | P7_4 | | TA2OUT/W | | | |
| 27 | 25 | | P7_3 | | TA1IN/$\overline{\text{V}}$ | $\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$ | | |
| 28 | 26 | | P7_2 | | TA1OUT/V | CLK2 | | |
| 29 | 27 | | P7_1 | | TA0IN/TB5IN | RXD2/SCL2 | | |
| 30 | 28 | | P7_0 | | TA0OUT | TXD2/SDA2 | | |
| 31 | 29 | | P6_7 | | | TXD1/SDA1 | | |
| 32 | 30 | | P6_6 | | | RXD1/SCL1 | | |
| 33 | 31 | | P6_5 | | | CLK1 | | |
| 34 | 32 | | P6_4 | | | $\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$/$\overline{\text{CTS0}}$/CLKS1 | | |
| 35 | 33 | | P6_3 | | | TXD0/SDA0 | | |
| 36 | 34 | | P6_2 | | | RXD0/SCL0 | | |
| 37 | 35 | | P6_1 | | | CLK0 | | |
| 38 | 36 | | P6_0 | | | $\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$ | | |
| 39 | 37 | | P5_7 | | | | | $\overline{\text{RDY}}$/CLKOUT |
| 40 | 38 | | P5_6 | | | | | ALE |
| 41 | 39 | | P5_5 | | | | | $\overline{\text{HOLD}}$ |
| 42 | 40 | | P5_4 | | | | | $\overline{\text{HLAD}}$ |
| 43 | 41 | | P5_3 | | | | | BCLK |
| 44 | 42 | | P5_2 | | | | | $\overline{\text{RD}}$ |
| 45 | 43 | | P5_1 | | | | | $\overline{\text{WRH}}$/$\overline{\text{BHE}}$ |
| 46 | 44 | | P5_0 | | | | | $\overline{\text{WRL}}$/$\overline{\text{WR}}$ |
| 47 | 45 | | P4_7 | | | | | $\overline{\text{CS3}}$ |
| 48 | 46 | | P4_6 | | | | | $\overline{\text{CS2}}$ |
| 49 | 47 | | P4_5 | | | | | $\overline{\text{CS1}}$ |
| 50 | 48 | | P4_4 | | | | | $\overline{\text{CS0}}$ |

**Table 1.14 Pin Characteristics for 100-Pin Package (2)**

| Pin No. | | Control Pin | Port | Interrupt Pin | Timer Pin | UART Pin | Analog Pin | Bus Control Pin |
|---|---|---|---|---|---|---|---|---|
| FP | GP | | | | | | | |
| 51 | 49 | | P4_3 | | | | | A19 |
| 52 | 50 | | P4_2 | | | | | A18 |
| 53 | 51 | | P4_1 | | | | | A17 |
| 54 | 52 | | P4_0 | | | | | A16 |
| 55 | 53 | | P3_7 | | | | | A15 |
| 56 | 54 | | P3_6 | | | | | A14 |
| 57 | 55 | | P3_5 | | | | | A13 |
| 58 | 56 | | P3_4 | | | | | A12 |
| 59 | 57 | | P3_3 | | | | | A11 |
| 60 | 58 | | P3_2 | | | | | A10 |
| 61 | 59 | | P3_1 | | | | | A9 |
| 62 | 60 | VCC2 | | | | | | |
| 63 | 61 | | P3_0 | | | | | A8(/-/D7) |
| 64 | 62 | VSS | | | | | | |
| 65 | 63 | | P2_7 | | | | AN2_7 | A7(/D7/D6) |
| 66 | 64 | | P2_6 | | | | AN2_6 | A6(/D6/D5) |
| 67 | 65 | | P2_5 | | | | AN2_5 | A5(/D5/D4) |
| 68 | 66 | | P2_4 | | | | AN2_4 | A4(/D4/D3) |
| 69 | 67 | | P2_3 | | | | AN2_3 | A3(/D3/D2) |
| 70 | 68 | | P2_2 | | | | AN2_2 | A2(/D2/D1) |
| 71 | 69 | | P2_1 | | | | AN2_1 | A1(/D1/D0) |
| 72 | 70 | | P2_0 | | | | AN2_0 | A0(/D0/-) |
| 73 | 71 | | P1_7 | $\overline{\text{INT5}}$ | | | | D15 |
| 74 | 72 | | P1_6 | $\overline{\text{INT4}}$ | | | | D14 |
| 75 | 73 | | P1_5 | $\overline{\text{INT3}}$ | | | | D13 |
| 76 | 74 | | P1_4 | | | | | D12 |
| 77 | 75 | | P1_3 | | | | | D11 |
| 78 | 76 | | P1_2 | | | | | D10 |
| 79 | 77 | | P1_1 | | | | | D9 |
| 80 | 78 | | P1_0 | | | | | D8 |
| 81 | 79 | | P0_7 | | | | AN0_7 | D7 |
| 82 | 80 | | P0_6 | | | | AN0_6 | D6 |
| 83 | 81 | | P0_5 | | | | AN0_5 | D5 |
| 84 | 82 | | P0_4 | | | | AN0_4 | D4 |
| 85 | 83 | | P0_3 | | | | AN0_3 | D3 |
| 86 | 84 | | P0_2 | | | | AN0_2 | D2 |
| 87 | 85 | | P0_1 | | | | AN0_1 | D1 |
| 88 | 86 | | P0_0 | | | | AN0_0 | D0 |
| 89 | 87 | | P10_7 | $\overline{\text{KI3}}$ | | | AN7 | |
| 90 | 88 | | P10_6 | $\overline{\text{KI2}}$ | | | AN6 | |
| 91 | 89 | | P10_5 | $\overline{\text{KI1}}$ | | | AN5 | |
| 92 | 90 | | P10_4 | $\overline{\text{KI0}}$ | | | AN4 | |
| 93 | 91 | | P10_3 | | | | AN3 | |
| 94 | 92 | | P10_2 | | | | AN2 | |
| 95 | 93 | | P10_1 | | | | AN1 | |
| 96 | 94 | AVSS | | | | | | |
| 97 | 95 | | P10_0 | | | | AN0 | |
| 98 | 96 | VREF | | | | | | |
| 99 | 97 | AVCC | | | | | | |
| 100 | 98 | | P9_7 | | | SIN4 | $\overline{\text{ADTRG}}$ | |

PIN CONFIGURATION (top view)




NOTES:
1. P7_0 and P7_1 are N channel open-drain output pins.

Package : PRQP0080JA-A (80P6S-A)

**Figure 1.9 Pin Configuration (Top View)**

**Table 1.15 Pin Characteristics for 80-Pin Package (1)**

| Pin No. | Control Pin | Port | Interrupt Pin | Timer Pin | UART Pin | Analog Pin | Bus Control Pin |
|---|---|---|---|---|---|---|---|
| 1 | | P9_5 | | | CLK4 | ANEX0 | |
| 2 | | P9_4 | | TB4IN | | DA1 | |
| 3 | | P9_3 | | TB3IN | | DA0 | |
| 4 | | P9_2 | | TB2IN | SOUT3 | | |
| 5 | | P9_0 | | TB0IN | CLK3 | | |
| 6 | CNVSS (BYTE) | | | | | | |
| 7 | XCIN | P8_7 | | | | | |
| 8 | XCOUT | P8_6 | | | | | |
| 9 | $\overline{\text{RESET}}$ | | | | | | |
| 10 | XOUT | | | | | | |
| 11 | VSS | | | | | | |
| 12 | XIN | | | | | | |
| 13 | VCC1 | | | | | | |
| 14 | | P8_5 | $\overline{\text{NMI}}$ | | | | |
| 15 | | P8_4 | $\overline{\text{INT2}}$ | ZP | | | |
| 16 | | P8_3 | $\overline{\text{INT1}}$ | | | | |
| 17 | | P8_2 | $\overline{\text{INT0}}$ | | | | |
| 18 | | P8_1 | | TA4IN | | | |
| 19 | | P8_0 | | TA4OUT | | | |
| 20 | | P7_7 | | TA3IN | | | |
| 21 | | P7_6 | | TA3OUT | | | |
| 22 | | P7_1 | | TA0IN/TB5IN | RXD2/SCL2 | | |
| 23 | | P7_0 | | TA0OUT | TXD2/SDA2 | | |
| 24 | | P6_7 | | | TXD1/SDA1 | | |
| 25 | | P6_6 | | | RXD1/SCL1 | | |
| 26 | | P6_5 | | | CLK1 | | |
| 27 | | P6_4 | | | $\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$/$\overline{\text{CTS0}}$/CLKS1 | | |
| 28 | | P6_3 | | | TXD0/SDA0 | | |
| 29 | | P6_2 | | | RXD0/SCL0 | | |
| 30 | | P6_1 | | | CLK0 | | |
| 31 | | P6_0 | | | $\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$ | | |
| 32 | | P5_7 | | | | | CLKOUT |
| 33 | | P5_6 | | | | | |
| 34 | | P5_5 | | | | | |
| 35 | | P5_4 | | | | | |
| 36 | | P5_3 | | | | | |
| 37 | | P5_2 | | | | | |
| 38 | | P5_1 | | | | | |
| 39 | | P5_0 | | | | | |
| 40 | | P4_3 | | | | | |
| 41 | | P4_2 | | | | | |
| 42 | | P4_1 | | | | | |
| 43 | | P4_0 | | | | | |
| 44 | | P3_7 | | | | | |
| 45 | | P3_6 | | | | | |
| 46 | | P3_5 | | | | | |
| 47 | | P3_4 | | | | | |
| 48 | | P3_3 | | | | | |
| 49 | | P3_2 | | | | | |
| 50 | | P3_1 | | | | | |

**Table 1.16 Pin Characteristics for 80-Pin Package (2)**

| Pin No. | Control Pin | Port | Interrupt Pin | Timer Pin | UART Pin | Analog Pin | Bus Control Pin |
|---|---|---|---|---|---|---|---|
| 51 | | P3_0 | | | | | |
| 52 | | P2_7 | | | | AN2_7 | |
| 53 | | P2_6 | | | | AN2_6 | |
| 54 | | P2_5 | | | | AN2_5 | |
| 55 | | P2_4 | | | | AN2_4 | |
| 56 | | P2_3 | | | | AN2_3 | |
| 57 | | P2_2 | | | | AN2_2 | |
| 58 | | P2_1 | | | | AN2_1 | |
| 59 | | P2_0 | | | | AN2_0 | |
| 60 | | P0_7 | | | | AN0_7 | |
| 61 | | P0_6 | | | | AN0_6 | |
| 62 | | P0_5 | | | | AN0_5 | |
| 63 | | P0_4 | | | | AN0_4 | |
| 64 | | P0_3 | | | | AN0_3 | |
| 65 | | P0_2 | | | | AN0_2 | |
| 66 | | P0_1 | | | | AN0_1 | |
| 67 | | P0_0 | | | | AN0_0 | |
| 68 | | P10_7 | $\overline{KI3}$ | | | AN7 | |
| 69 | | P10_6 | $\overline{KI2}$ | | | AN6 | |
| 70 | | P10_5 | $\overline{KI1}$ | | | AN5 | |
| 71 | | P10_4 | $\overline{KI0}$ | | | AN4 | |
| 72 | | P10_3 | | | | AN3 | |
| 73 | | P10_2 | | | | AN2 | |
| 74 | | P10_1 | | | | AN1 | |
| 75 | AVSS | | | | | | |
| 76 | | P10_0 | | | | AN0 | |
| 77 | VREF | | | | | | |
| 78 | AVCC | | | | | | |
| 79 | | P9_7 | | | SIN4 | $\overline{ADTRG}$ | |
| 80 | | P9_6 | | | SOUT4 | ANEX1 | |

## 1.6 Pin Description

**Table 1.17 Pin Description (100-pin and 128-pin Version) (1)**

| Signal Name | Pin Name | I/O Type | Power Supply(3) | Description |
|---|---|---|---|---|
| Power supply input | VCC1,VCC2<br>VSS | I | – | Apply 2.7 to 5.5 V to the VCC1 and VCC2 pins and 0 V to the VSS pin. The VCC apply condition is that VCC1 ≥ VCC2. (1, 2) |
| Analog power supply input | AVCC<br>AVSS | I | VCC1 | Applies the power supply for the A/D converter. Connect the AVCC pin to VCC1. Connect the AVSS pin to VSS. |
| Reset input | $\overline{\text{RESET}}$ | I | VCC1 | The microcomputer is in a reset state when applying “L” to the this pin. |
| CNVSS | CNVSS | I | VCC1 | Switches processor mode. Connect this pin to VSS to when after a reset to start up in single-chip mode. Connect this pin to VCC1 to start up in microprocessor mode. |
| External data bus width select input | BYTE | I | VCC1 | Switches the data bus in external memory space. The data bus is 16 bits long when the this pin is held "L" and 8 bits long when the this pin is held "H". Set it to either one. Connect this pin to VSS when an single-chip mode. |
| Bus control pins (4) | D0 to D7 | I/O | VCC2 | Inputs and outputs data (D0 to D7) when these pins are set as the separate bus. |
| | D8 to D15 | I/O | VCC2 | Inputs and outputs data (D8 to D15) when external 16-bit data bus is set as the separate bus. |
| | A0 to A19 | O | VCC2 | Output address bits (A0 to A19). |
| | A0/D0 to A7/D7 | I/O | VCC2 | Input and output data (D0 to D7) and output address bits (A0 to A7) by timesharing when external 8-bit data bus are set as the multiplexed bus. |
| | A1/D0 to A8/D7 | I/O | VCC2 | Input and output data (D0 to D7) and output address bits (A1 to A8) by timesharing when external 16-bit data bus are set as the multiplexed bus. |
| | $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$ | O | VCC2 | Output $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$ signals. $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$ are chip-select signals to specify an external space. |
| | $\overline{\text{WRL}}$/$\overline{\text{WR}}$<br>$\overline{\text{WRH}}$/$\overline{\text{BHE}}$<br>$\overline{\text{RD}}$ | O | VCC2 | Output $\overline{\text{WRL}}$, $\overline{\text{WRH}}$, ($\overline{\text{WR}}$, $\overline{\text{BHE}}$), $\overline{\text{RD}}$ signals. $\overline{\text{WRL}}$ and $\overline{\text{WRH}}$ or $\overline{\text{BHE}}$ and $\overline{\text{WR}}$ can be switched by program.<br>• $\overline{\text{WRL}}$, $\overline{\text{WRH}}$ and $\overline{\text{RD}}$ are selected<br>The $\overline{\text{WRL}}$ signal becomes "L" by writing data to an even address in an external memory space.<br>The $\overline{\text{WRH}}$ signal becomes "L" by writing data to an odd address in an external memory space.<br>The $\overline{\text{RD}}$ pin signal becomes "L" by reading data in an external memory space.<br>• $\overline{\text{WR}}$, $\overline{\text{BHE}}$ and $\overline{\text{RD}}$ are selected<br>The $\overline{\text{WR}}$ signal becomes "L" by writing data in an external memory space.<br>The $\overline{\text{RD}}$ signal becomes "L" by reading data in an external memory space.<br>The $\overline{\text{BHE}}$ signal becomes "L" by accessing an odd address.<br>Select $\overline{\text{WR}}$, $\overline{\text{BHE}}$ and $\overline{\text{RD}}$ for an external 8-bit data bus. |
| | ALE | O | VCC2 | ALE is a signal to latch the address. |
| | $\overline{\text{HOLD}}$ | I | VCC2 | While the $\overline{\text{HOLD}}$ pin is held "L", the microcomputer is placed in a hold state. |
| | $\overline{\text{HLDA}}$ | O | VCC2 | In a hold state, $\overline{\text{HLDA}}$ outputs a "L" signal. |
| | $\overline{\text{RDY}}$ | I | VCC2 | While applying a "L" signal to the $\overline{\text{RDY}}$ pin, the microcomputer is placed in a wait state. |

I : Input O : Output I/O : Input and output

Power Supply : Power supplies which relate to the external bus pins are separated as VCC2, thus they can be interfaced using the different voltage as VCC1.

NOTES:

1. In this manual, hereafter, VCC refers to VCC1 unless otherwise noted.
2. In M16C/62PT, apply 4.0 to 5.5 V to the VCC1 and VCC2 pins. Also the apply condition is that VCC1 = VCC2.
3. When use VCC1 > VCC2, contacts due to some points or restrictions to be checked.
4. Bus control pins in M16C/62PT cannot be used.

**Table 1.18 Pin Description (100-pin and 128-pin Version) (2)**

| Signal Name | Pin Name | I/O Type | Power Supply(1) | Description |
|---|---|---|---|---|
| Main clock input | XIN | I | VCC1 | I/O pins for the main clock generation circuit. Connect a ceramic resonator or crystal oscillator between XIN and XOUT (3). To use the external clock, input the clock from XIN and leave XOUT open. |
| Main clock output | XOUT | O | VCC1 | |
| Sub clock input | XCIN | I | VCC1 | I/O pins for a sub clock oscillation circuit. Connect a crystal oscillator between XCIN and XCOUT (3). To use the external clock, input the clock from XCIN and leave XCOUT open. |
| Sub clock output | XCOUT | O | VCC1 | |
| BCLK output (2) | BCLK | O | VCC2 | Outputs the BCLK signal. |
| Clock output | CLKOUT | O | VCC2 | The clock of the same cycle as fC, f8, or f32 is outputted. |
| $\overline{\text{INT}}$ interrupt input | $\overline{\text{INT0}}$ to $\overline{\text{INT2}}$ | I | VCC1 | Input pins for the $\overline{\text{INT}}$ interrupt. |
| | $\overline{\text{NT3}}$ to $\overline{\text{INT5}}$ | I | VCC2 | |
| $\overline{\text{NMI}}$ interrupt input | $\overline{\text{NMI}}$ | I | VCC1 | Input pin for the $\overline{\text{NMI}}$ interrupt. Pin states can be read by the P8_5 bit in the P8 register. |
| Key input interrupt input | $\overline{\text{KI0}}$ to $\overline{\text{KI3}}$ | I | VCC1 | Input pins for the key input interrupt. |
| Timer A | TA0OUT to TA4OUT | I/O | VCC1 | These are timer A0 to timer A4 I/O pins. (however, output of TA0OUT for the N-channel open drain output.) |
| | TA0IN to TA4IN | I | VCC1 | These are timer A0 to timer A4 input pins. |
| | ZP | I | VCC1 | Input pin for the Z-phase. |
| Timer B | TB0IN to TB5IN | I | VCC1 | These are timer B0 to timer B5 input pins. |
| Three-phase motor control output | U, $\overline{\text{U}}$, V, $\overline{\text{V}}$, W, $\overline{\text{W}}$ | O | VCC1 | These are Three-phase motor control output pins. |
| Serial interface | $\overline{\text{CTS0}}$ to $\overline{\text{CTS2}}$ | I | VCC1 | These are send control input pins. |
| | $\overline{\text{RTS0}}$ to $\overline{\text{RTS2}}$ | O | VCC1 | These are receive control output pins. |
| | CLK0 to CLK4 | I/O | VCC1 | These are transfer clock I/O pins. |
| | RXD0 to RXD2 | I | VCC1 | These are serial data input pins. |
| | SIN3, SIN4 | I | VCC1 | These are serial data input pins. |
| | TXD0 to TXD2 | O | VCC1 | These are serial data output pins. (however, output of TXD2 for the N-channel open drain output.) |
| | SOUT3, SOUT4 | O | VCC1 | These are serial data output pins. |
| | CLKS1 | O | VCC1 | This is output pin for transfer clock output from multiple pins function. |
| $I^2C$ mode | SDA0 to SDA2 | I/O | VCC1 | These are serial data I/O pins. (however, output of SDA2 for the N-channel open drain output.) |
| | SCL0 to SCL2 | I/O | VCC1 | These are transfer clock I/O pins. (however, output of SCL2 for the N-channel open drain output.) |

I : Input O : Output I/O : Input and output

NOTES:
1. When use VCC1 > VCC2, contacts due to some points or restrictions to be checked.
2. This pin function in M16C/62PT cannot be used.
3. Ask the oscillator maker the oscillation characteristic.

**Table 1.19 Pin Description (100-pin and 128-pin Version) (3)**

| Signal Name | Pin Name | I/O Type | Power Supply(1) | Description |
|---|---|---|---|---|
| Reference voltage input | VREF | I | VCC1 | Applies the reference voltage for the A/D converter and D/A converter. |
| A/D converter | AN0 to AN7, AN0_0 to AN0_7, AN2_0 to AN2_7 | I | VCC1 | Analog input pins for the A/D converter. |
| | $\overline{\text{ADTRG}}$ | I | VCC1 | This is an A/D trigger input pin. |
| | ANEX0 | I/O | VCC1 | This is the extended analog input pin for the A/D converter, and is the output in external op-amp connection mode. |
| | ANEX1 | I | VCC1 | This is the extended analog input pin for the A/D converter. |
| D/A converter | DA0, DA1 | O | VCC1 | This is the output pin for the D/A converter. |
| I/O port | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7 (2), P13_0 to P13_7 (2) | I/O | VCC2 | 8-bit I/O ports in CMOS, having a direction register to select an input or output.<br>Each pin is set as an input port or output port. An input port can be set for a pull-up or for no pull-up in 4-bit unit by program. |
| | P6_0 to P6_7, P7_0 to P7_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7 (2) | I/O | VCC1 | 8-bit I/O ports having equivalent functions to P0.<br>(however, output of P7_0 and P7_1 for the N-channel open drain output.) |
| | P8_0 to P8_4, P8_6, P8_7, P14_0, P14_1(2) | I/O | VCC1 | I/O ports having equivalent functions to P0. |
| Input port | P8_5 | I | VCC1 | Input pin for the $\overline{\text{NMI}}$ interrupt.<br>Pin states can be read by the P8_5 bit in the P8 register. |

I : Input O : Output I/O : Input and output

NOTES:
1. When use VCC1 > VCC2, contacts due to some points or restrictions to be checked.
2. Ports P11 to P14 in M16C/62P (100-pin version) and M16C/62PT (100-pin version) cannot be used.

**Table 1.20 Pin Description (80-pin Version) (1)** (1)

| Signal Name | Pin Name | I/O Type | Power Supply | Description |
|---|---|---|---|---|
| Power supply input | VCC1, VSS | I | – | Apply 2.7 to 5.5 V to the VCC1 pin and 0 V to the VSS pin. (1, 2) |
| Analog power supply input | AVCC<br>AVSS | I | VCC1 | Applies the power supply for the A/D converter. Connect the AVCC pin to VCC1. Connect the AVSS pin to VSS. |
| Reset input | $\overline{\text{RESET}}$ | I | VCC1 | The microcomputer is in a reset state when applying "L" to the this pin. |
| CNVSS | CNVSS<br>(BYTE) | I | VCC1 | Switches processor mode. Connect this pin to VSS to when after a reset to start up in single-chip mode. Connect this pin to VCC1 to start up in microprocessor mode. As for the BYTE pin of the 80-pin versions, pull-up processing is performed within the microcomputer. |
| Main clock input | XIN | I | VCC1 | I/O pins for the main clock generation circuit. Connect a ceramic resonator or crystal oscillator between XIN and XOUT (3). To use the external clock, input the clock from XIN and leave XOUT open. |
| Main clock output | XOUT | O | VCC1 | |
| Sub clock input | XCIN | I | VCC1 | I/O pins for a sub clock oscillation circuit. Connect a crystal oscillator between XCIN and XCOUT (3). To use the external clock, input the clock from XCIN and leave XCOUT open. |
| Sub clock output | XCOUT | O | VCC1 | |
| Clock output | CLKOUT | O | VCC2 | The clock of the same cycle as fC, f8, or f32 is outputted. |
| $\overline{\text{INT}}$ interrupt input | $\overline{\text{INT0}}$ to $\overline{\text{INT2}}$ | I | VCC1 | Input pins for the $\overline{\text{INT}}$ interrupt. |
| $\overline{\text{NMI}}$ interrupt input | $\overline{\text{NMI}}$ | I | VCC1 | Input pin for the $\overline{\text{NMI}}$ interrupt. |
| Key input interrupt input | $\overline{\text{KI0}}$ to $\overline{\text{KI3}}$ | I | VCC1 | Input pins for the key input interrupt. |
| Timer A | TA0OUT,<br>TA3OUT,<br>TA4OUT | I/O | VCC1 | These are Timer A0,Timer A3 and Timer A4 I/O pins. (however, output of TA0OUT for the N-channel open drain output.) |
| | TA0IN, TA3IN,<br>TA4IN | I | VCC1 | These are Timer A0, Timer A3 and Timer A4 input pins. |
| | ZP | I | VCC1 | Input pin for the Z-phase. |
| Timer B | TB0IN, TB2IN<br>to TB5IN | I | VCC1 | These are Timer B0, Timer B2 to Timer B5 input pins. |
| Serial interface | $\overline{\text{CTS0}}$ to $\overline{\text{CTS1}}$ | I | VCC1 | These are send control input pins. |
| | $\overline{\text{RTS0}}$ to $\overline{\text{RTS1}}$ | O | VCC1 | These are receive control output pins. |
| | CLK0, CLK1,<br>CLK3, CLK4 | I/O | VCC1 | These are transfer clock I/O pins. |
| | RXD0 to RXD2 | I | VCC1 | These are serial data input pins. |
| | SIN4 | I | VCC1 | This is serial data input pin. |
| | TXD0 to TXD2 | O | VCC1 | These are serial data output pins. (however, output of TXD2 for the N-channel open drain output.) |
| | SOUT3,<br>SOUT4 | O | VCC1 | These are serial data output pins. |
| | CLKS1 | O | VCC1 | This is output pin for transfer clock output from multiple pins function. |
| $I^2C$ mode | SDA0 to SDA2 | I/O | VCC1 | These are serial data I/O pins. (however, output of SDA2 for the N-channel open drain output.) |
| | SCL0 to SCL2 | I/O | VCC1 | These are transfer clock I/O pins. (however, output of SCL2 for the N-channel open drain output.) |

I : Input O : Output I/O : Input and output

NOTES:
1. In this manual, hereafter, VCC refers to VCC1 unless otherwise noted.
2. In M16C/62PT, apply 4.0 to 5.5 V to the VCC1 pin.
3. Ask the oscillator maker the oscillation characteristic.

**Table 1.21 Pin Description (80-pin Version) (2)**

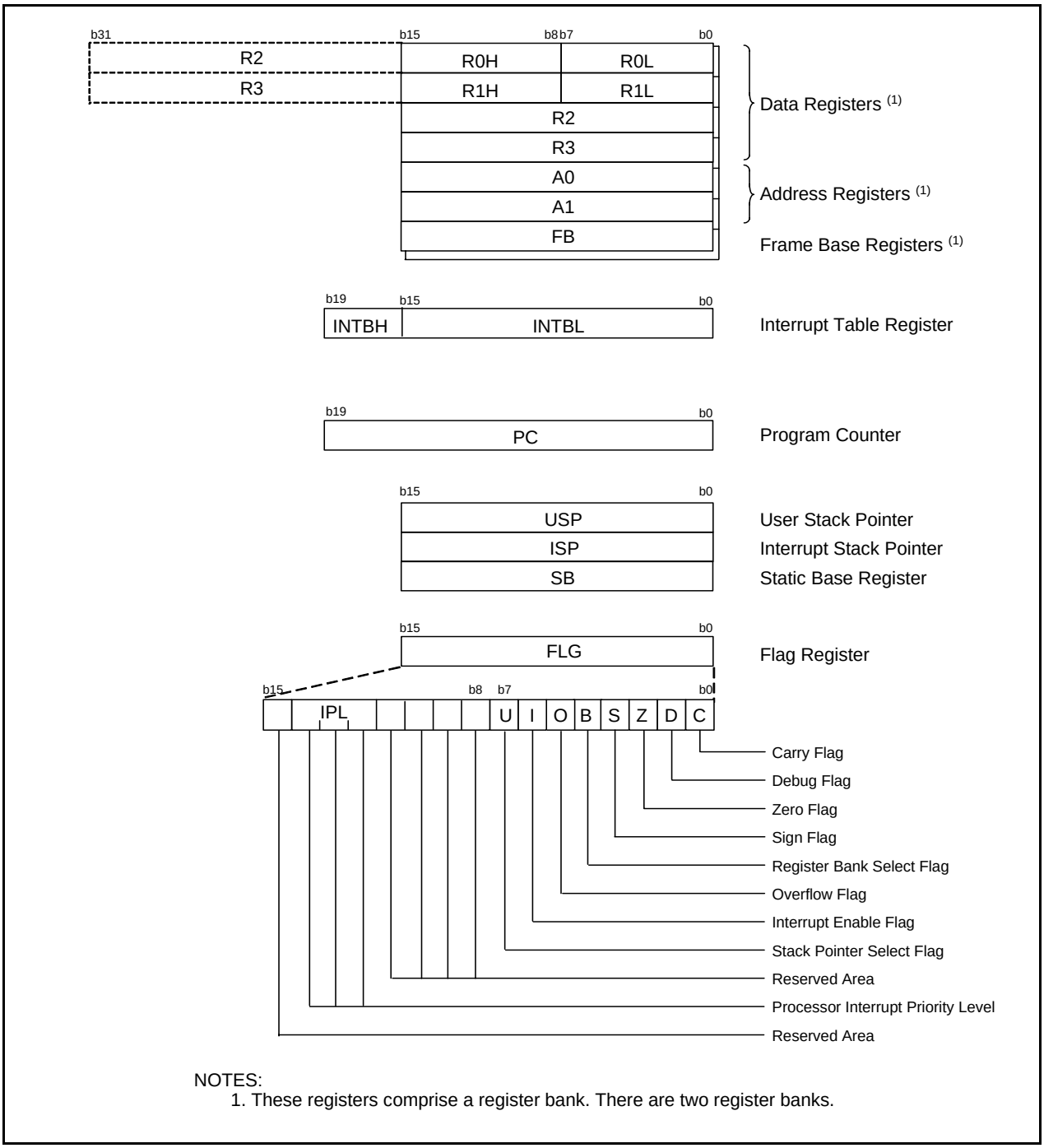
| Signal Name | Pin Name | I/O Type | Power Supply(1) | Description |
|---|---|---|---|---|
| Reference voltage input | VREF | I | VCC1 | Applies the reference voltage for the A/D converter and D/A converter. |
| A/D converter | AN0 to AN7, AN0_0 to AN0_7, AN2_0 to AN2_7 | I | VCC1 | Analog input pins for the A/D converter. |
| | $\overline{\text{ADTRG}}$ | I | VCC1 | This is an A/D trigger input pin. |
| | ANEX0 | I/O | VCC1 | This is the extended analog input pin for the A/D converter, and is the output in external op-amp connection mode. |
| | ANEX1 | I | VCC1 | This is the extended analog input pin for the A/D converter. |
| D/A converter | DA0, DA1 | O | VCC1 | This is the output pin for the D/A converter. |
| I/O port (1) | P0_0 to P0_7, P2_0 to P2_7, P3_0 to P3_7, P5_0 to P5_7, P6_0 to P6_7, P10_0 to P10_7 | I/O | VCC1 | 8-bit I/O ports in CMOS, having a direction register to select an input or output.<br>Each pin is set as an input port or output port. An input port can be set for a pull-up or for no pull-up in 4-bit unit by program. |
| | P8_0 to P8_4, P8_6, P8_7, P9_0, P9_2 to P9_7 | I/O | VCC1 | I/O ports having equivalent functions to P0. |
| | P4_0 to P4_3, P7_0, P7_1, P7_6, P7_7 | I/O | VCC1 | I/O ports having equivalent functions to P0.<br>(however, output of P7_0 and P7_1 for the N-channel open drain output.) |
| Input port | P8_5 | I | VCC1 | Input pin for the $\overline{\text{NMI}}$ interrupt.<br>Pin states can be read by the P8_5 bit in the P8 register. |

I : Input O : Output I/O : Input and output

NOTES:
1. There is no external connections for port P1, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version. Set the direction bits in these ports to “1” (output mode), and set the output data to “0” (“L”) using the program.

# 2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. The CPU has 13 registers. Of these, R0, R1, R2, R3, A0, A1 and FB comprise a register bank. There are two register banks.




NOTES:
1. These registers comprise a register bank. There are two register banks.

**Figure 2.1 Central Processing Unit Register**

## 2.1 Data Registers (R0, R1, R2 and R3)

The R0 register consists of 16 bits, and is used mainly for transfers and arithmetic/logic operations. R1 to R3 are the same as R0.

The R0 register can be separated between high (R0H) and low (R0L) for use as two 8-bit data registers.

R1H and R1L are the same as R0H and R0L. Conversely, R2 and R0 can be combined for use as a 32-bit data register (R2R0). R3R1 is the same as R2R0.

## 2.2 Address Registers (A0 and A1)

The register A0 consists of 16 bits, and is used for address register indirect addressing and address register relative addressing. They also are used for transfers and logic/logic operations. A1 is the same as A0.
In some instructions, registers A1 and A0 can be combined for use as a 32-bit address register (A1A0).

## 2.3 Frame Base Register (FB)

FB is configured with 16 bits, and is used for FB relative addressing.

## 2.4 Interrupt Table Register (INTB)

INTB is configured with 20 bits, indicating the start address of an interrupt vector table.

## 2.5 Program Counter (PC)

PC is configured with 20 bits, indicating the address of an instruction to be executed.

## 2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

Stack pointer (SP) comes in two types: USP and ISP, each configured with 16 bits.
Your desired type of stack pointer (USP or ISP) can be selected by the U flag of FLG.

## 2.7 Static Base Register (SB)

SB is configured with 16 bits, and is used for SB relative addressing.

## 2.8 Flag Register (FLG)

FLG consists of 11 bits, indicating the CPU status.

### 2.8.1 Carry Flag (C Flag)

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

### 2.8.2 Debug Flag (D Flag)

The D flag is used exclusively for debugging purpose. During normal use, it must be set to “0”.

### 2.8.3 Zero Flag (Z Flag)

This flag is set to “1” when an arithmetic operation resulted in 0; otherwise, it is “0”.

### 2.8.4 Sign Flag (S Flag)

This flag is set to “1” when an arithmetic operation resulted in a negative value; otherwise, it is “0”.

### 2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when this flag is “0” ; register bank 1 is selected when this flag is “1”.

### 2.8.6 Overflow Flag (O Flag)

This flag is set to “1” when the operation resulted in an overflow; otherwise, it is “0”.

### 2.8.7 Interrupt Enable Flag (I Flag)

This flag enables a maskable interrupt.
Maskable interrupts are disabled when the I flag is “0”, and are enabled when the I flag is “1”. The I flag is cleared to “0” when the interrupt request is accepted.

### 2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is “0”; USP is selected when the U flag is “1”.
The U flag is cleared to “0” when a hardware interrupt request is accepted or an INT instruction for software interrupt Nos. 0 to 31 is executed.

### 2.8.9 Processor Interrupt Priority Level (IPL)

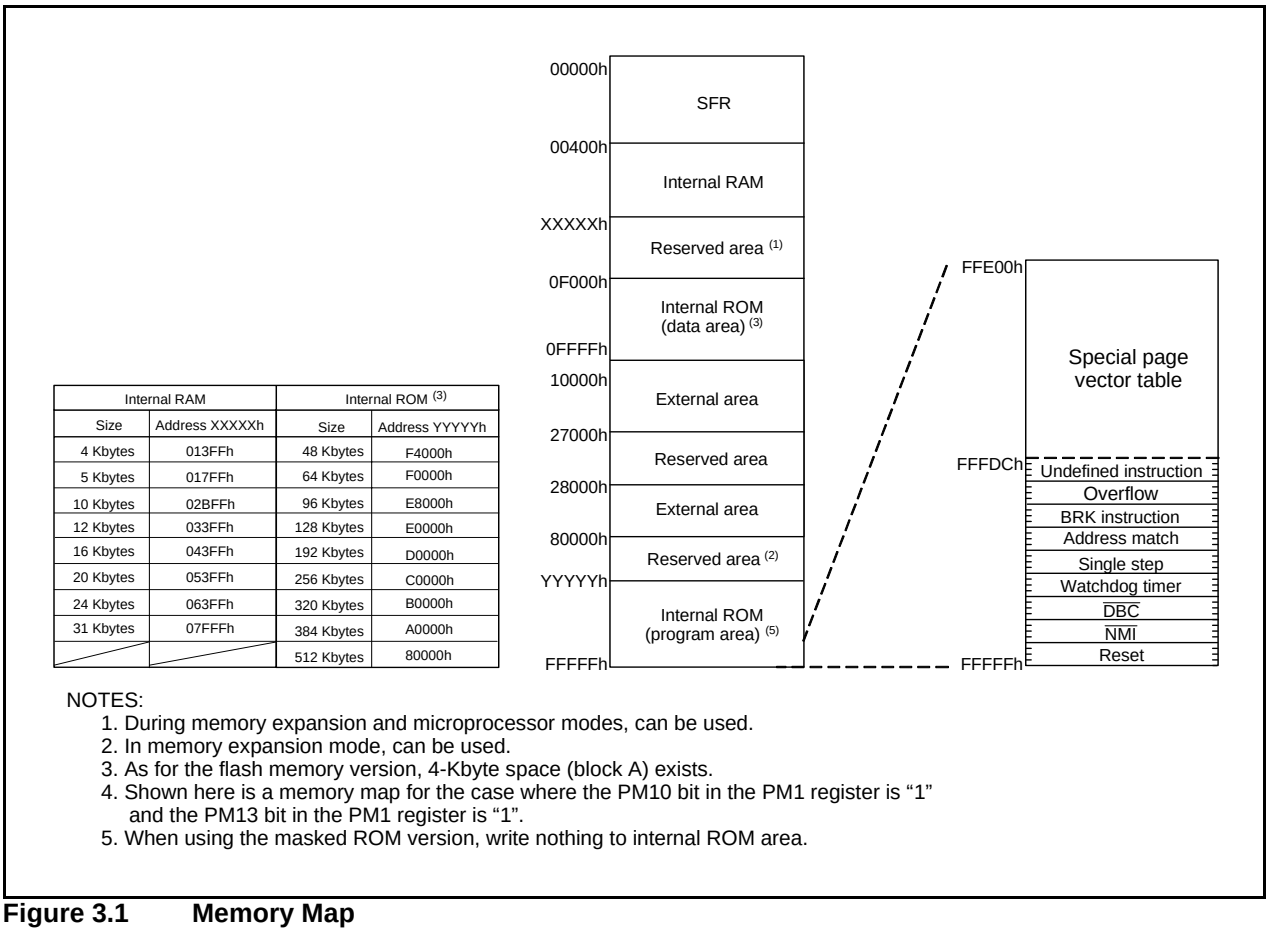
IPL is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has priority greater than IPL, the interrupt is enabled.

### 2.8.10 Reserved Area

When write to this bit, write “0”. When read, its content is indeterminate.

# 3. Memory

Figure 3.1 is a Memory Map of the M16C/62P group. The address space extends the 1M bytes from address 00000h to FFFFFh.
The internal ROM is allocated in a lower address direction beginning with address FFFFFh. For example, a 64-Kbyte internal ROM is allocated to the addresses from F0000h to FFFFFh.
As for the flash memory version, 4-Kbyte space (block A) exists in 0F000h to 0FFFFh. 4-Kbyte space is mainly for storing data. In addition to storing data, 4-Kbyte space also can store programs.
The fixed interrupt vector table is allocated to the addresses from FFFDCh to FFFFFh. Therefore, store the start address of each interrupt routine here.
The internal RAM is allocated in an upper address direction beginning with address 00400h. For example, a 10-Kbyte internal RAM is allocated to the addresses from 00400h to 02BFFh. In addition to storing data, the internal RAM also stores the stack used when calling subroutines and when interrupts are generated.
The SRF is allocated to the addresses from 00000h to 003FFh. Peripheral function control registers are located here. Of the SFR, any area which has no functions allocated is reserved for future use and cannot be used by users.
The special page vector table is allocated to the addresses from FFE00h to FFFDBh. This vector is used by the JMPS or JSRS instruction. For details, refer to the **M16C/60 and M16C/20 Series Software Manual**.
In memory expansion and microprocessor modes, some areas are reserved for future use and cannot be used by users. Use M16C/62P (80-pin version) and M16C/62PT in single-chip mode. The memory expansion and microprocessor modes cannot be used
.




| Internal RAM | | Internal ROM (3) | |
|---|---|---|---|
| Size | Address XXXXXh | Size | Address YYYYYh |
| 4 Kbytes | 013FFh | 48 Kbytes | F4000h |
| 5 Kbytes | 017FFh | 64 Kbytes | F0000h |
| 10 Kbytes | 02BFFh | 96 Kbytes | E8000h |
| 12 Kbytes | 033FFh | 128 Kbytes | E0000h |
| 16 Kbytes | 043FFh | 192 Kbytes | D0000h |
| 20 Kbytes | 053FFh | 256 Kbytes | C0000h |
| 24 Kbytes | 063FFh | 320 Kbytes | B0000h |
| 31 Kbytes | 07FFFh | 384 Kbytes | A0000h |
| | | 512 Kbytes | 80000h |

NOTES:
1. During memory expansion and microprocessor modes, can be used.
2. In memory expansion mode, can be used.
3. As for the flash memory version, 4-Kbyte space (block A) exists.
4. Shown here is a memory map for the case where the PM10 bit in the PM1 register is “1” and the PM13 bit in the PM1 register is “1”.
5. When using the masked ROM version, write nothing to internal ROM area.

**Figure 3.1 Memory Map**

# 4. Special Function Register (SFR)

SFR(Special Function Register) is the control register of peripheral functions. Tables 4.1 to 4.6 list the SFR information.

**Table 4.1 SFR Information (1)** (1)

| Address | Register | Symbol | After Reset |
|---|---|---|---|
| 0000h | | | |
| 0001h | | | |
| 0002h | | | |
| 0003h | | | |
| 0004h | Processor Mode Register 0 (2) | PM0 | 00000000b(CNVSS pin is "L")<br>00000011b(CNVSS pin is "H") |
| 0005h | Processor Mode Register 1 | PM1 | 00001000b |
| 0006h | System Clock Control Register 0 | CM0 | 01001000b |
| 0007h | System Clock Control Register 1 | CM1 | 00100000b |
| 0008h | Chip Select Control Register (6) | CSR | 00000001b |
| 0009h | Address Match Interrupt Enable Register | AIER | XXXXXX00b |
| 000Ah | Protect Register | PRCR | XX000000b |
| 000Bh | Data Bank Register (6) | DBR | 00h |
| 000Ch | Oscillation Stop Detection Register (3) | CM2 | 0X000000b |
| 000Dh | | | |
| 000Eh | Watchdog Timer Start Register | WDTS | XXh |
| 000Fh | Watchdog Timer Control Register | WDC | 00XXXXXXb (4) |
| 0010h<br>0011h<br>0012h | Address Match Interrupt Register 0 | RMAD0 | 00h<br>00h<br>X0h |
| 0013h | | | |
| 0014h<br>0015h<br>0016h | Address Match Interrupt Register 1 | RMAD1 | 00h<br>00h<br>X0h |
| 0017h | | | |
| 0018h | | | |
| 0019h | Voltage Detection Register 1 (5, 6) | VCR1 | 00001000b |
| 001Ah | Voltage Detection Register 2 (5, 6) | VCR2 | 00h |
| 001Bh | Chip Select Expansion Control Register (6) | CSE | 00h |
| 001Ch | PLL Control Register 0 | PLC0 | 0001X010b |
| 001Dh | | | |
| 001Eh | Processor Mode Register 2 | PM2 | XXX00000b |
| 001Fh | Low Voltage Detection Interrupt Register (6) | D4INT | 00h |
| 0020h<br>0021h<br>0022h | DMA0 Source Pointer | SAR0 | XXh<br>XXh<br>XXh |
| 0023h | | | |
| 0024h<br>0025h<br>0026h | DMA0 Destination Pointer | DAR0 | XXh<br>XXh<br>XXh |
| 0027h | | | |
| 0028h<br>0029h | DMA0 Transfer Counter | TCR0 | XXh<br>XXh |
| 002Ah | | | |
| 002Bh | | | |
| 002Ch | DMA0 Control Register | DM0CON | 00000X00b |
| 002Dh | | | |
| 002Eh | | | |
| 002Fh | | | |
| 0030h<br>0031h<br>0032h | DMA1 Source Pointer | SAR1 | XXh<br>XXh<br>XXh |
| 0033h | | | |
| 0034h<br>0035h<br>0036h | DMA1 Destination Pointer | DAR1 | XXh<br>XXh<br>XXh |
| 0037h | | | |
| 0038h<br>0039h | DMA1 Transfer Counter | TCR1 | XXh<br>XXh |
| 003Ah | | | |
| 003Bh | | | |
| 003Ch | DMA1 Control Register | DM1CON | 00000X00b |
| 003Dh | | | |
| 003Eh | | | |
| 003Fh | | | |

NOTES:
1. The blank areas are reserved and cannot be accessed by users.
2. The PM00 and PM01 bits do not change at software reset, watchdog timer reset and oscillation stop detection reset.
3. The CM20, CM21, and CM27 bits do not change at oscillation stop detection reset.
4. The WDC5 bit is "0" (cold start) immediately after power-on. I t can only be set to "1" in a program.
5. This register does not change at software reset, watchdog timer reset and oscillation stop detection reset.
6. This register in M16C/62PT cannot be used.

X : Nothing is mapped to this bit

**Table 4.2 SFR Information (2)** (1)

| Address | Register | Symbol | After Reset |
|---|---|---|---|
| 0040h | | | |
| 0041h | | | |
| 0042h | | | |
| 0043h | | | |
| 0044h | INT3 Interrupt Control Register | INT3IC | XX00X000b |
| 0045h | Timer B5 Interrupt Control Register | TB5IC | XXXXX000b |
| 0046h | Timer B4 Interrupt Control Register, UART1 BUS Collision Detection Interrupt Control Register | TB4IC, U1BCNIC | XXXXX000b |
| 0047h | Timer B3 Interrupt Control Register, UART0 BUS Collision Detection Interrupt Control Register | TB3IC, U0BCNIC | XXXXX000b |
| 0048h | SI/O4 Interrupt Control Register, INT5 Interrupt Control Register | S4IC, INT5IC | XX00X000b |
| 0049h | SI/O3 Interrupt Control Register, INT4 Interrupt Control Register | S3IC, INT4IC | XX00X000b |
| 004Ah | UART2 Bus Collision Detection Interrupt Control Register | BCNIC | XXXXX000b |
| 004Bh | DMA0 Interrupt Control Register | DM0IC | XXXXX000b |
| 004Ch | DMA1 Interrupt Control Register | DM1IC | XXXXX000b |
| 004Dh | Key Input Interrupt Control Register | KUPIC | XXXXX000b |
| 004Eh | A/D Conversion Interrupt Control Register | ADIC | XXXXX000b |
| 004Fh | UART2 Transmit Interrupt Control Register | S2TIC | XXXXX000b |
| 0050h | UART2 Receive Interrupt Control Register | S2RIC | XXXXX000b |
| 0051h | UART0 Transmit Interrupt Control Register | S0TIC | XXXXX000b |
| 0052h | UART0 Receive Interrupt Control Register | S0RIC | XXXXX000b |
| 0053h | UART1 Transmit Interrupt Control Register | S1TIC | XXXXX000b |
| 0054h | UART1 Receive Interrupt Control Register | S1RIC | XXXXX000b |
| 0055h | Timer A0 Interrupt Control Register | TA0IC | XXXXX000b |
| 0056h | Timer A1 Interrupt Control Register | TA1IC | XXXXX000b |
| 0057h | Timer A2 Interrupt Control Register | TA2IC | XXXXX000b |
| 0058h | Timer A3 Interrupt Control Register | TA3IC | XXXXX000b |
| 0059h | Timer A4 Interrupt Control Register | TA4IC | XXXXX000b |
| 005Ah | Timer B0 Interrupt Control Register | TB0IC | XXXXX000b |
| 005Bh | Timer B1 Interrupt Control Register | TB1IC | XXXXX000b |
| 005Ch | Timer B2 Interrupt Control Register | TB2IC | XXXXX000b |
| 005Dh | INT0 Interrupt Control Register | INT0IC | XX00X000b |
| 005Eh | INT1 Interrupt Control Register | INT1IC | XX00X000b |
| 005Fh | INT2 Interrupt Control Register | INT2IC | XX00X000b |
| 0060h | | | |
| 0061h | | | |
| 0062h | | | |
| 0063h | | | |
| 0064h | | | |
| 0065h | | | |
| 0066h | | | |
| 0067h | | | |
| 0068h | | | |
| 0069h | | | |
| 006Ah | | | |
| 006Bh | | | |
| 006Ch | | | |
| 006Dh | | | |
| 006Eh | | | |
| 006Fh | | | |
| 0070h | | | |
| 0071h | | | |
| 0072h | | | |
| 0073h | | | |
| 0074h | | | |
| 0075h | | | |
| 0076h | | | |
| 0077h | | | |
| 0078h | | | |
| 0079h | | | |
| 007Ah | | | |
| 007Bh | | | |
| 007Ch | | | |
| 007Dh | | | |
| 007Eh | | | |
| 007Fh | | | |

NOTES:
1. The blank areas are reserved and cannot be accessed by users.

X : Nothing is mapped to this bit

**Table 4.3 SFR Information (3) (1)**

| Address | Register | Symbol | After Reset |
|---|---|---|---|
| 0080h | | | |
| 0081h | | | |
| 0082h | | | |
| 0083h | | | |
| 0084h | | | |
| 0085h | | | |
| 0086h | | | |
| 0087h to 01AFh | | | |
| 01B0h | | | |
| 01B1h | | | |
| 01B2h | | | |
| 01B3h | | | |
| 01B4h | Flash Identification Register (2) | FIDR | XXXXXX00b |
| 01B5h | Flash Memory Control Register 1 (2) | FMR1 | 0X00XX0Xb |
| 01B6h | | | |
| 01B7h | Flash Memory Control Register 0 (2) | FMR0 | 00000001b |
| 01B8h | Address Match Interrupt Register 2 | RMAD2 | 00h |
| 01B9h | | | 00h |
| 01BAh | | | XXh |
| 01BBh | Address Match Interrupt Enable Register 2 | AIER2 | XXXXXX00b |
| 01BCh | Address Match Interrupt Register 3 | RMAD3 | 00h |
| 01BDh | | | 00h |
| 01BEh | | | XXh |
| 01C0h to 024Fh | | | |
| 0250h | | | |
| 0251h | | | |
| 0252h | | | |
| 0253h | | | |
| 0254h | | | |
| 0255h | | | |
| 0256h | | | |
| 0257h | | | |
| 0258h | | | |
| 0259h | | | |
| 025Ah | | | |
| 025Bh | | | |
| 025Ch | | | |
| 025Dh | | | |
| 025Eh | Peripheral Clock Select Register | PCLKR | 00000011b |
| 025Fh | | | |
| 0260h to 032Fh | | | |
| 0330h | | | |
| 0331h | | | |
| 0332h | | | |
| 0333h | | | |
| 0334h | | | |
| 0335h | | | |
| 0336h | | | |
| 0337h | | | |
| 0338h | | | |
| 0339h | | | |
| 033Ah | | | |
| 033Bh | | | |
| 033Ch | | | |
| 033Dh | | | |
| 033Eh | | | |
| 033Fh | | | |

NOTES:
1. The blank areas are reserved and cannot be accessed by users.
2. This register is included in the flash memory version.

X : Nothing is mapped to this bit

**Table 4.4 SFR Information (4)** (1)

| Address | Register | Symbol | After Reset |
|---|---|---|---|
| 0340h | Timer B3, 4, 5 Count Start Flag | TBSR | 000XXXXXb |
| 0341h | | | |
| 0342h | Timer A1-1 Register | TA11 | XXh |
| 0343h | | | XXh |
| 0344h | Timer A2-1 Register | TA21 | XXh |
| 0345h | | | XXh |
| 0346h | Timer A4-1 Register | TA41 | XXh |
| 0347h | | | XXh |
| 0348h | Three-Phase PWM Control Register 0 | INVC0 | 00h |
| 0349h | Three-Phase PWM Control Register 1 | INVC1 | 00h |
| 034Ah | Three-Phase Output Buffer Register 0 | IDB0 | 00h |
| 034Bh | Three-Phase Output Buffer Register 1 | IDB1 | 00h |
| 034Ch | Dead Time Timer | DTT | XXh |
| 034Dh | Timer B2 Interrupt Occurrence Frequency Set Counter | ICTB2 | XXh |
| 034Eh | | | |
| 034Fh | | | |
| 0350h | Timer B3 Register | TB3 | XXh |
| 0351h | | | XXh |
| 0352h | Timer B4 Register | TB4 | XXh |
| 0353h | | | XXh |
| 0354h | Timer B5 Register | TB5 | XXh |
| 0355h | | | XXh |
| 0356h | | | |
| 0357h | | | |
| 0358h | | | |
| 0359h | | | |
| 035Ah | | | |
| 035Bh | Timer B3 Mode Register | TB3MR | 00XX0000b |
| 035Ch | Timer B4 Mode Register | TB4MR | 00XX0000b |
| 035Dh | Timer B5 Mode Register | TB5MR | 00XX0000b |
| 035Eh | Interrupt Factor Select Register 2 | IFSR2A | 00XXXXXXb |
| 035Fh | Interrupt Factor Select Register | IFSR | 00h |
| 0360h | SI/O3 Transmit/Receive Register | S3TRR | XXh |
| 0361h | | | |
| 0362h | SI/O3 Control Register | S3C | 01000000b |
| 0363h | SI/O3 Bit Rate Generator | S3BRG | XXh |
| 0364h | SI/O4 Transmit/Receive Register | S4TRR | XXh |
| 0365h | | | |
| 0366h | SI/O4 Control Register | S4C | 01000000b |
| 0367h | SI/O4 Bit Rate Generator | S4BRG | XXh |
| 0368h | | | |
| 0369h | | | |
| 036Ah | | | |
| 036Bh | | | |
| 036Ch | UART0 Special Mode Register 4 | U0SMR4 | 00h |
| 036Dh | UART0 Special Mode Register 3 | U0SMR3 | 000X0X0Xb |
| 036Eh | UART0 Special Mode Register 2 | U0SMR2 | X0000000b |
| 036Fh | UART0 Special Mode Register | U0SMR | X0000000b |
| 0370h | UART1 Special Mode Register 4 | U1SMR4 | 00h |
| 0371h | UART1 Special Mode Register 3 | U1SMR3 | 000X0X0Xb |
| 0372h | UART1 Special Mode Register 2 | U1SMR2 | X0000000b |
| 0373h | UART1 Special Mode Register | U1SMR | X0000000b |
| 0374h | UART2 Special Mode Register 4 | U2SMR4 | 00h |
| 0375h | UART2 Special Mode Register 3 | U2SMR3 | 000X0X0Xb |
| 0376h | UART2 Special Mode Register 2 | U2SMR2 | X0000000b |
| 0377h | UART2 Special Mode Register | U2SMR | X0000000b |
| 0378h | UART2 Transmit/Receive Mode Register | U2MR | 00h |
| 0379h | UART2 Bit Rate Generator | U2BRG | XXh |
| 037Ah | UART2 Transmit Buffer Register | U2TB | XXh |
| 037Bh | | | XXh |
| 037Ch | UART2 Transmit/Receive Control Register 0 | U2C0 | 00001000b |
| 037Dh | UART2 Transmit/Receive Control Register 1 | U2C1 | 00000010b |
| 037Eh | UART2 Receive Buffer Register | U2RB | XXh |
| 037Fh | | | XXh |

NOTES:
1. The blank areas are reserved and cannot be accessed by users.

X : Nothing is mapped to this bit

**Table 4.5 SFR Information (5)** (1)

| Address | Register | Symbol | After Reset |
|---|---|---|---|
| 0380h | Count Start Flag | TABSR | 00h |
| 0381h | Clock Prescaler Reset Fag | CPSRF | 0XXXXXXXb |
| 0382h | One-Shot Start Flag | ONSF | 00h |
| 0383h | Trigger Select Register | TRGSR | 00h |
| 0384h | Up-Down Flag | UDF | 00h (2) |
| 0385h | | | |
| 0386h | Timer A0 Register | TA0 | XXh |
| 0387h | | | XXh |
| 0388h | Timer A1 Register | TA1 | XXh |
| 0389h | | | XXh |
| 038Ah | Timer A2 Register | TA2 | XXh |
| 038Bh | | | XXh |
| 038Ch | Timer A3 Register | TA3 | XXh |
| 038Dh | | | XXh |
| 038Eh | Timer A4 Register | TA4 | XXh |
| 038Fh | | | XXh |
| 0390h | Timer B0 Register | TB0 | XXh |
| 0391h | | | XXh |
| 0392h | Timer B1 Register | TB1 | XXh |
| 0393h | | | XXh |
| 0394h | Timer B2 Register | TB2 | XXh |
| 0395h | | | XXh |
| 0396h | Timer A0 Mode Register | TA0MR | 00h |
| 0397h | Timer A1 Mode Register | TA1MR | 00h |
| 0398h | Timer A2 Mode Register | TA2MR | 00h |
| 0399h | Timer A3 Mode Register | TA3MR | 00h |
| 039Ah | Timer A4 Mode Register | TA4MR | 00h |
| 039Bh | Timer B0 Mode Register | TB0MR | 00XX0000b |
| 039Ch | Timer B1 Mode Register | TB1MR | 00XX0000b |
| 039Dh | Timer B2 Mode Register | TB2MR | 00XX0000b |
| 039Eh | Timer B2 Special Mode Register | TB2SC | XXXXXX00b |
| 039Fh | | | |
| 03A0h | UART0 Transmit/Receive Mode Register | U0MR | 00h |
| 03A1h | UART0 Bit Rate Generator | U0BRG | XXh |
| 03A2h | UART0 Transmit Buffer Register | U0TB | XXh |
| 03A3h | | | XXh |
| 03A4h | UART0 Transmit/Receive Control Register 0 | U0C0 | 00001000b |
| 03A5h | UART0 Transmit/Receive Control Register 1 | U0C1 | 00XX0010b |
| 03A6h | UART0 Receive Buffer Register | U0RB | XXh |
| 03A7h | | | XXh |
| 03A8h | UART1 Transmit/Receive Mode Register | U1MR | 00h |
| 03A9h | UART1 Bit Rate Generator | U1BRG | XXh |
| 03AAh | UART1 Transmit Buffer Register | U1TB | XXh |
| 03ABh | | | XXh |
| 03ACh | UART1 Transmit/Receive Control Register 0 | U1C0 | 00001000b |
| 03ADh | UART1 Transmit/Receive Control Register 1 | U1C1 | 00XX0010b |
| 03AEh | UART1 Receive Buffer Register | U1RB | XXh |
| 03AFh | | | XXh |
| 03B0h | UART Transmit/Receive Control Register 2 | UCON | X0000000b |
| 03B1h | | | |
| 03B2h | | | |
| 03B3h | | | |
| 03B4h | | | |
| 03B5h | | | |
| 03B6h | | | |
| 03B7h | | | |
| 03B8h | DMA0 Request Factor Select Register | DM0SL | 00h |
| 03B9h | | | |
| 03BAh | DMA1 Request Factor Select Register | DM1SL | 00h |
| 03BBh | | | |
| 03BCh | CRC Data Register | CRCD | XXh |
| 03BDh | | | XXh |
| 03BEh | CRC Input Register | CRCIN | XXh |
| 03BFh | | | |

NOTES:
1. The blank areas are reserved and cannot be accessed by users.
2. Bit 5 in the Up-down flag is “0” by reset. However, The values in these bits when read are indeterminate.

X : Nothing is mapped to this bit

**Table 4.6 SFR Information (6) (1)**

| Address | Register | Symbol | After Reset |
|---|---|---|---|
| 03C0h<br>03C1h | A/D Register 0 | AD0 | XXh<br>XXh |
| 03C2h<br>03C3h | A/D Register 1 | AD1 | XXh<br>XXh |
| 03C4h<br>03C5h | A/D Register 2 | AD2 | XXh<br>XXh |
| 03C6h<br>03C7h | A/D Register 3 | AD3 | XXh<br>XXh |
| 03C8h<br>03C9h | A/D Register 4 | AD4 | XXh<br>XXh |
| 03CAh<br>03CBh | A/D Register 5 | AD5 | XXh<br>XXh |
| 03CCh<br>03CDh | A/D Register 6 | AD6 | XXh<br>XXh |
| 03CEh<br>03CFh | A/D Register 7 | AD7 | XXh<br>XXh |
| 03D0h | | | |
| 03D1h | | | |
| 03D2h | | | |
| 03D3h | | | |
| 03D4h | A/D Control Register 2 | ADCON2 | 00h |
| 03D5h | | | |
| 03D6h | A/D Control Register 0 | ADCON0 | 00000XXXb |
| 03D7h | A/D Control Register 1 | ADCON1 | 00h |
| 03D8h | D/A Register 0 | DA0 | 00h |
| 03D9h | | | |
| 03DAh | D/A Register 1 | DA1 | 00h |
| 03DBh | | | |
| 03DCh | D/A Control Register | DACON | 00h |
| 03DDh | | | |
| 03DEh | Port P14 Control Register (3) | PC14 | XX00XXXXb |
| 03DFh | Pull-Up Control Register 3 (3) | PUR3 | 00h |
| 03E0h | Port P0 Register | P0 | XXh |
| 03E1h | Port P1 Register | P1 | XXh |
| 03E2h | Port P0 Direction Register | PD0 | 00h |
| 03E3h | Port P1 Direction Register | PD1 | 00h |
| 03E4h | Port P2 Register | P2 | XXh |
| 03E5h | Port P3 Register | P3 | XXh |
| 03E6h | Port P2 Direction Register | PD2 | 00h |
| 03E7h | Port P3 Direction Register | PD3 | 00h |
| 03E8h | Port P4 Register | P4 | XXh |
| 03E9h | Port P5 Register | P5 | XXh |
| 03EAh | Port P4 Direction Register | PD4 | 00h |
| 03EBh | Port P5 Direction Register | PD5 | 00h |
| 03ECh | Port P6 Register | P6 | XXh |
| 03EDh | Port P7 Register | P7 | XXh |
| 03EEh | Port P6 Direction Register | PD6 | 00h |
| 03EFh | Port P7 Direction Register | PD7 | 00h |
| 03F0h | Port P8 Register | P8 | XXh |
| 03F1h | Port P9 Register | P9 | XXh |
| 03F2h | Port P8 Direction Register | PD8 | 00X00000b |
| 03F3h | Port P9 Direction Register | PD9 | 00h |
| 03F4h | Port P10 Register | P10 | XXh |
| 03F5h | Port P11 Register (3) | P11 | XXh |
| 03F6h | Port P10 Direction Register | PD10 | 00h |
| 03F7h | Port P11 Direction Register (3) | PD11 | 00h |
| 03F8h | Port P12 Register (3) | P12 | XXh |
| 03F9h | Port P13 Register (3) | P13 | XXh |
| 03FAh | Port P12 Direction Register (3) | PD12 | 00h |
| 03FBh | Port P13 Direction Register (3) | PD13 | 00h |
| 03FCh | Pull-Up Control Register 0 | PUR0 | 00h |
| 03FDh | Pull-Up Control Register 1 | PUR1 | 00000000b (2)<br>00000010b (2) |
| 03FEh | Pull-Up Control Register 2 | PUR2 | 00h |
| 03FFh | Port Control Register | PCR | 00h |

NOTES:
1. The blank areas are reserved and cannot be accessed by users.
2. At hardware reset 1 or hardware reset 2, the register is as follows:
   - "00000000b" where "L" is inputted to the CNVSS pin
   - "00000010b" where "H" is inputted to the CNVSS pin

   At software reset, watchdog timer reset and oscillation stop detection reset, the register is as follows:
   - "00000000b" where the PM01 to PM00 bits in the PM0 register are "00b" (single-chip mode).
   - "00000010b" where the PM01 to PM00 bits in the PM0 register are "01b" (memory expansion mode) or "11b" (microprocessor mode).
3. These registers do not exist in M16C/62P (80-pin version), and M16C/62PT (80-pin version).

X : Nothing is mapped to this bit

# 5. Electrical Characteristics

## 5.1 Electrical Characteristics (M16C/62P)

**Table 5.1 Absolute Maximum Ratings**

| Symbol | Parameter | | Condition | Rated Value | Unit |
|---|---|---|---|---|---|
| $V_{CC1}$, $V_{CC2}$ | Supply Voltage | | $V_{CC1}$=AVcc | –0.3 to 6.5 | V |
| $V_{CC2}$ | Supply Voltage | | $V_{CC2}$ | –0.3 to $V_{CC1}$+0.1 | V |
| AVcc | Analog Supply Voltage | | $V_{CC1}$=AVcc | –0.3 to 6.5 | V |
| $V_I$ | Input Voltage | $\overline{\text{RESET}}$, CNVSS, BYTE, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, VREF, XIN | | –0.3 to $V_{CC1}$+0.3 (1) | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7 | | –0.3 to $V_{CC2}$+0.3 (1) | V |
| | | P7_0, P7_1 | | –0.3 to 6.5 | V |
| $V_O$ | Output Voltage | P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, XOUT | | –0.3 to $V_{CC1}$+0.3 (1) | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7 | | –0.3 to $V_{CC2}$+0.3 (1) | V |
| | | P7_0, P7_1 | | –0.3 to 6.5 | V |
| $P_d$ | Power Dissipation | | –40°C<$T_{opr}$≤85°C | 300 | mW |
| $T_{opr}$ | Operating Ambient Temperature | When the Microcomputer is Operating | | –20 to 85 / –40 to 85 | °C |
| | | Flash Program Erase | | 0 to 60 | |
| $T_{stg}$ | Storage Temperature | | | –65 to 150 | °C |

NOTES:
1. There is no external connections for port P1_0 to P1_7, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version.

**Table 5.2 Recommended Operating Conditions (1)** (1)

| Symbol | Parameter | | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{CC1}$, $V_{CC2}$ | Supply Voltage ($V_{CC1} \geq V_{CC2}$) | | 2.7 | 5.0 | 5.5 | V |
| AVcc | Analog Supply Voltage | | | $V_{CC1}$ | | V |
| Vss | Supply Voltage | | | 0 | | V |
| AVss | Analog Supply Voltage | | | 0 | | V |
| $V_{IH}$ | HIGH Input Voltage | P3_1 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7 | 0.8$V_{CC2}$ | | $V_{CC2}$ | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (during single-chip mode) | 0.8$V_{CC2}$ | | $V_{CC2}$ | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (data input during memory expansion and microprocessor mode) | 0.5$V_{CC2}$ | | $V_{CC2}$ | V |
| | | P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, XIN, $\overline{RESET}$, CNVSS, BYTE | 0.8$V_{CC1}$ | | $V_{CC1}$ | V |
| | | P7_0, P7_1 | 0.8$V_{CC1}$ | | 6.5 | V |
| $V_{IL}$ | LOW Input Voltage | P3_1 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7 | 0 | | 0.2$V_{CC2}$ | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (during single-chip mode) | 0 | | 0.2$V_{CC2}$ | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (data input during memory expansion and microprocessor mode) | 0 | | 0.16$V_{CC2}$ | V |
| | | P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, XIN, $\overline{RESET}$, CNVSS, BYTE | 0 | | 0.2$V_{CC}$ | V |
| $I_{OH(peak)}$ | HIGH Peak Output Current | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1 | | | –10.0 | mA |
| $I_{OH(avg)}$ | HIGH Average Output Current | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1 | | | –5.0 | mA |
| $I_{OL(peak)}$ | LOW Peak Output Current | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1 | | | 10.0 | mA |
| $I_{OL(avg)}$ | LOW Average Output Current | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1 | | | 5.0 | mA |

NOTES:

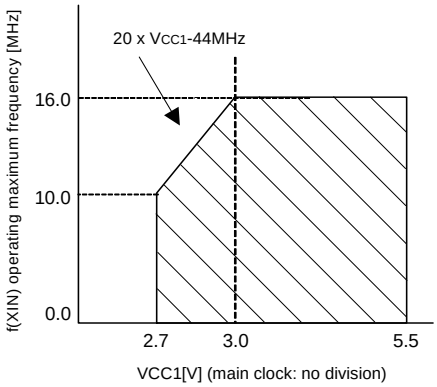
1. Referenced to $V_{CC1}$ = $V_{CC2}$ = 2.7 to 5.5V at $T_{opr}$ = –20 to 85°C / –40 to 85°C unless otherwise specified.
2. The Average Output Current is the mean value within 100ms.
3. The total $I_{OL(peak)}$ for ports P0, P1, P2, P8_6, P8_7, P9, P10, P11, P14_0, and P14_1 must be 80mA max. The total $I_{OL(peak)}$ for ports P3, P4, P5, P6, P7, P8_0 to P8_4, P12, and P13 must be 80mA max. The total $I_{OH(peak)}$ for ports P0, P1, and P2 must be –40mA max. The total $I_{OH(peak)}$ for ports P3, P4, P5, P12, and P13 must be –40mA max. The total $I_{OH(peak)}$ for ports P6, P7, and P8_0 to P8_4 must be –40mA max. The total $I_{OH(peak)}$ for ports P8_6, P8_7, P9, P10, P14_0, and P14_1 must be –40mA max. Set Average Output Current to 1/2 of peak. The total $I_{OH(peak)}$ for ports P8_6, P8_7, P9 , P10, P11, P14_0, and P14_1 must be –40mA max.
   As for 80-pin version, the total $I_{OL(peak)}$ for all ports and $I_{OH(peak)}$ must be 80mA. max. due to one $V_{CC}$ and one $V_{SS}$.
4. There is no external connections for port P1_0 to P1_7, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version.

**Table 5.3 Recommended Operating Conditions (2)** (1)

| Symbol | Parameter | | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| f(XIN) | Main Clock Input Oscillation Frequency (2) | $V_{CC1}$=3.0V to 5.5V | 0 | | 16 | MHz |
| | | $V_{CC1}$=2.7V to 3.0V | 0 | | $20\times V_{CC1}-44$ | MHz |
| f(XCIN) | Sub-Clock Oscillation Frequency | | | 32.768 | 50 | kHz |
| f(Ring) | On-chip Oscillation Frequency | | 0.5 | 1 | 2 | MHz |
| f(PLL) | PLL Clock Oscillation Frequency (2) | $V_{CC1}$=3.0V to 5.5V | 10 | | 24 | MHz |
| | | $V_{CC1}$=2.7V to 3.0V | 10 | | $46.67\times V_{CC1}-116$ | MHz |
| f(BCLK) | CPU Operation Clock | | 0 | | 24 | MHz |
| $t_{SU}$(PLL) | PLL Frequency Synthesizer Stabilization Wait Time | $V_{CC1}$=5.5V | | | 20 | ms |
| | | $V_{CC1}$=3.0V | | | 50 | ms |

NOTES:
1. Referenced to $V_{CC1}$ = $V_{CC2}$ = 2.7 to 5.5V at $T_{opr}$ = –20 to 85°C / –40 to 85°C unless otherwise specified.
2. Relationship between main clock oscillation frequency, and supply voltage.

Main clock input oscillation frequency




PLL clock oscillation frequency

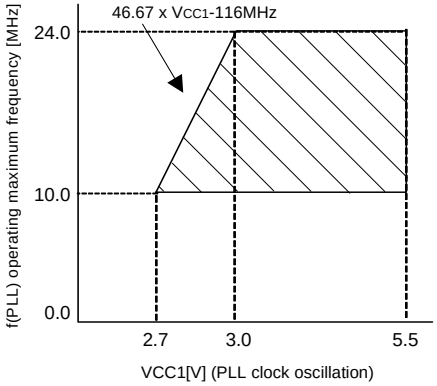


**Table 5.4 A/D Conversion Characteristics** (1)

| Symbol | Parameter | | Measuring Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Typ. | Max. | |
| – | Resolution | | $V_{REF}=V_{CC1}$ | | | | 10 | Bits |
| INL | Integral Non-Linearity Error | 10bit | $V_{REF}=V_{CC1}=5V$ | AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input | | | ±3 | LSB |
| | | | | External operation amp connection mode | | | ±7 | LSB |
| | | | $V_{REF}=V_{CC1}=3.3V$ | AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input | | | ±5 | LSB |
| | | | | External operation amp connection mode | | | ±7 | LSB |
| | | 8bit | $V_{REF}=V_{CC1}$=5V, 3.3V | | | | ±2 | LSB |
| – | Absolute Accuracy | 10bit | $V_{REF}=V_{CC1}=5V$ | AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input | | | ±3 | LSB |
| | | | | External operation amp connection mode | | | ±7 | LSB |
| | | | $V_{REF}=V_{CC1}=3.3V$ | AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input | | | ±5 | LSB |
| | | | | External operation amp connection mode | | | ±7 | LSB |
| | | 8bit | $V_{REF}=V_{CC1}$=5V, 3.3V | | | | ±2 | LSB |
| – | Tolerance Level Impedance | | | | | 3 | | kΩ |
| DNL | Differential Non-Linearity Error | | | | | | ±1 | LSB |
| – | Offset Error | | | | | | ±3 | LSB |
| – | Gain Error | | | | | | ±3 | LSB |
| $R_{LADDER}$ | Ladder Resistance | | $V_{REF}=V_{CC1}$ | | 10 | | 40 | kΩ |
| $t_{CONV}$ | 10-bit Conversion Time, Sample & Hold Available | | $V_{REF}=V_{CC1}$=5V, ϕAD=12MHz | | 2.75 | | | µs |
| $t_{CONV}$ | 8-bit Conversion Time, Sample & Hold Available | | $V_{REF}=V_{CC1}$=5V, ϕAD=12MHz | | 2.33 | | | µs |
| $t_{SAMP}$ | Sampling Time | | | | 0.25 | | | µs |
| $V_{REF}$ | Reference Voltage | | | | 2.0 | | $V_{CC1}$ | V |
| $V_{IA}$ | Analog Input Voltage | | | | 0 | | $V_{REF}$ | V |

NOTES:
1. Referenced to $V_{CC1}=AV_{CC}=V_{REF}$=3.3 to 5.5V, $V_{SS}=AV_{SS}$=0V at $T_{opr}$ = −20 to 85°C / −40 to 85°C unless otherwise specified.
2. If $V_{CC1} > V_{CC2}$, do not use AN0_0 to AN0_7 and AN2_0 to AN2_7 as analog input pins.
3. ϕAD frequency must be 12 MHz or less. And divide the fAD if $V_{CC1}$ is less than 4.0V, and ϕAD frequency into 10 MHz or less.
4. When sample & hold is disabled, ϕAD frequency must be 250 kHz or more, in addition to the limitation in Note 3.
   When sample & hold is enabled, ϕAD frequency must be 1MHz or more, in addition to the limitation in Note 3.

**Table 5.5 D/A Conversion Characteristics** (1)

| Symbol | Parameter | Measuring Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| – | Resolution | | | | 8 | Bits |
| – | Absolute Accuracy | | | | 1.0 | % |
| $t_{SU}$ | Setup Time | | | | 3 | µs |
| $R_O$ | Output Resistance | | 4 | 10 | 20 | kΩ |
| $I_{VREF}$ | Reference Power Supply Input Current | (NOTE 2) | | | 1.5 | mA |

NOTES:

1. Referenced to $V_{CC1}$=$V_{REF}$=3.3 to 5.5V, $V_{SS}$=$AV_{SS}$=0V at $T_{opr}$ = –20 to 85°C / –40 to 85°C unless otherwise specified.
2. This applies when using one D/A converter, with the D/A register for the unused D/A converter set to “00h”. The resistor ladder of the A/D converter is not included. Also, when D/A register contents are not “00h”, the $I_{VREF}$ will flow even if Vref id disconnected by the A/D control register.

**Table 5.6 Flash Memory Version Electrical Characteristics (1) for 100 cycle products (D3, D5, U3, U5)**

| Symbol | Parameter | | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| – | Program and Erase Endurance (3) | | 100 | | | cycle |
| – | Word Program Time ($V_{CC1}$=5.0V) | | | 25 | 200 | µs |
| – | Lock Bit Program Time | | | 25 | 200 | µs |
| – | Block Erase Time ($V_{CC1}$=5.0V) | 4-Kbyte block | | 0.3 | 4 | s |
| – | | 8-Kbyte block | | 0.3 | 4 | s |
| – | | 32-Kbyte block | | 0.5 | 4 | s |
| – | | 64-Kbyte block | | 0.8 | 4 | s |
| – | Erase All Unlocked Blocks Time (2) | | | | 4×n | s |
| $t_{PS}$ | Flash Memory Circuit Stabilization Wait Time | | | | 15 | µs |
| – | Data Hold Time (5) | | 10 | | | year |

**Table 5.7 Flash Memory Version Electrical Characteristics (6) for 10,000 cycle products (D7, D9, U7, U9) (Block A and Block 1 (7))**

| Symbol | Parameter | | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| – | Program and Erase Endurance (3, 8, 9) | | 10,000 (4) | | | cycle |
| – | Word Program Time ($V_{CC1}$=5.0V) | | | 25 | | µs |
| – | Lock Bit Program Time | | | 25 | | µs |
| – | Block Erase Time ($V_{CC1}$=5.0V) | 4-Kbyte block | | 0.3 | | s |
| $t_{PS}$ | Flash Memory Circuit Stabilization Wait Time | | | | 15 | µs |
| – | Data Hold Time (5) | | 10 | | | year |

NOTES:
1. Referenced to $V_{CC1}$=4.5 to 5.5V, 3.0 to 3.6V at Topr = 0 to 60 °C (D3, D5, U3, U5) unless otherwise specified.
2. n denotes the number of block erases.
3. Program and Erase Endurance refers to the number of times a block erase can be performed.
   If the program and erase endurance is n (n=100, 1,000, or 10,000), each block can be erased n times.
   For example, if a 4 Kbytes block A is erased after writing 1 word data 2,048 times, each to a different address, this counts as one program and erase endurance. Data cannot be written to the same address more than once without erasing the block. (Rewrite prohibited)
4. Maximum number of E/W cycles for which operation is guaranteed.
5. Topr = -40 to 85 °C (D3, D7, U3, U7) / -20 to 85 °C (D5, D9, U5, U9).
6. Referenced to $V_{CC1}$ = 4.5 to 5.5V, 3.0 to 3.6V at $T_{opr}$ = -40 to 85 °C (D7, U7) / -20 to 85 °C (D9, U9) unless otherwise specified.
7. Table 5.7 applies for block A or block 1 program and erase endurance > 1,000. Otherwise, use Table 5.6.
8. To reduce the number of program and erase endurance when working with systems requiring numerous rewrites, write to unused word addresses within the block instead of rewrite. Erase block only after all possible addresses are used. For example, an 8-word program can be written 256 times maximum before erase becomes necessary.
   Maintaining an equal number of erasure between block A and block 1 will also improve efficiency. It is important to track the total number of times erasure is used.
9. Should erase error occur during block erase, attempt to execute clear status register command, then block erase command at least three times until erase error disappears.
10. Set the PM17 bit in the PM1 register to “1” (wait state) when executing more than 100 times rewrites (D7, D9, U7 and U9).
11. Customers desiring E/W failure rate information should contact their Renesas technical support representative.

**Table 5.8 Flash Memory Version Program / Erase Voltage and Read Operation Voltage Characteristics (at $T_{opr}$ = 0 to 60 °C(D3, D5, U3, U5), $T_{opr}$ = -40 to 85 °C(D7, U7) / $T_{opr}$ = -20 to 85 °C(D9, U9))**

| Flash Program, Erase Voltage | Flash Read Operation Voltage |
|---|---|
| $V_{CC1}$ = 3.3 V ± 0.3 V or 5.0 V ± 0.5 V | $V_{CC1}$=2.7 to 5.5 V |

**Table 5.9 Low Voltage Detection Circuit Electrical Characteristics**

| Symbol | Parameter | Measuring Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{det4}$ | Low Voltage Detection Voltage (1) | $V_{CC1}$=0.8V to 5.5V | 3.3 | 3.8 | 4.4 | V |
| $V_{det3}$ | Reset Level Detection Voltage (1, 2) | | 2.2 | 2.8 | 3.6 | V |
| $V_{det4}$-$V_{det3}$ | Electric potential difference of Low Voltage Detection and Reset Level Detection | | 0.3 | | | V |
| $V_{det3s}$ | Low Voltage Reset Retention Voltage | | | | 0.8 | V |
| $V_{det3r}$ | Low Voltage Reset Release Voltage (3) | | 2.2 | 2.9 | 4.0 | V |

NOTES:
1. $V_{det4} > V_{det3}$.
2. Where reset level detection voltage is less than 2.7 V, if the supply power voltage is greater than the reset level detection voltage, the microcomputer operates with f(BCLK) ≤ 10MHz.
3. $V_{det3r} > V_{det3}$ is not guaranteed.
4. The voltage detection circuit is designed to use when VCC1 is set to 5V.

**Table 5.10 Power Supply Circuit Timing Characteristics**

| Symbol | Parameter | Measuring Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $t_{d(P-R)}$ | Time for Internal Power Supply Stabilization During Powering-On | $V_{CC1}$=2.7V to 5.5V | | | 2 | ms |
| $t_{d(R-S)}$ | STOP Release Time | | | | 150 | µs |
| $t_{d(W-S)}$ | Low Power Dissipation Mode Wait Mode Release Time | | | | 150 | µs |
| $t_{d(S-R)}$ | Brown-out Detection Reset (Hardware Reset 2) Release Wait Time | $V_{CC1}$=$V_{det3r}$ to 5.5V | | 6 (1) | 20 | ms |
| $t_{d(E-A)}$ | Low Voltage Detection Circuit Operation Start Time | $V_{CC1}$=2.7V to 5.5V | | | 20 | µs |

NOTES:
1. When $V_{CC1}$ = 5V.

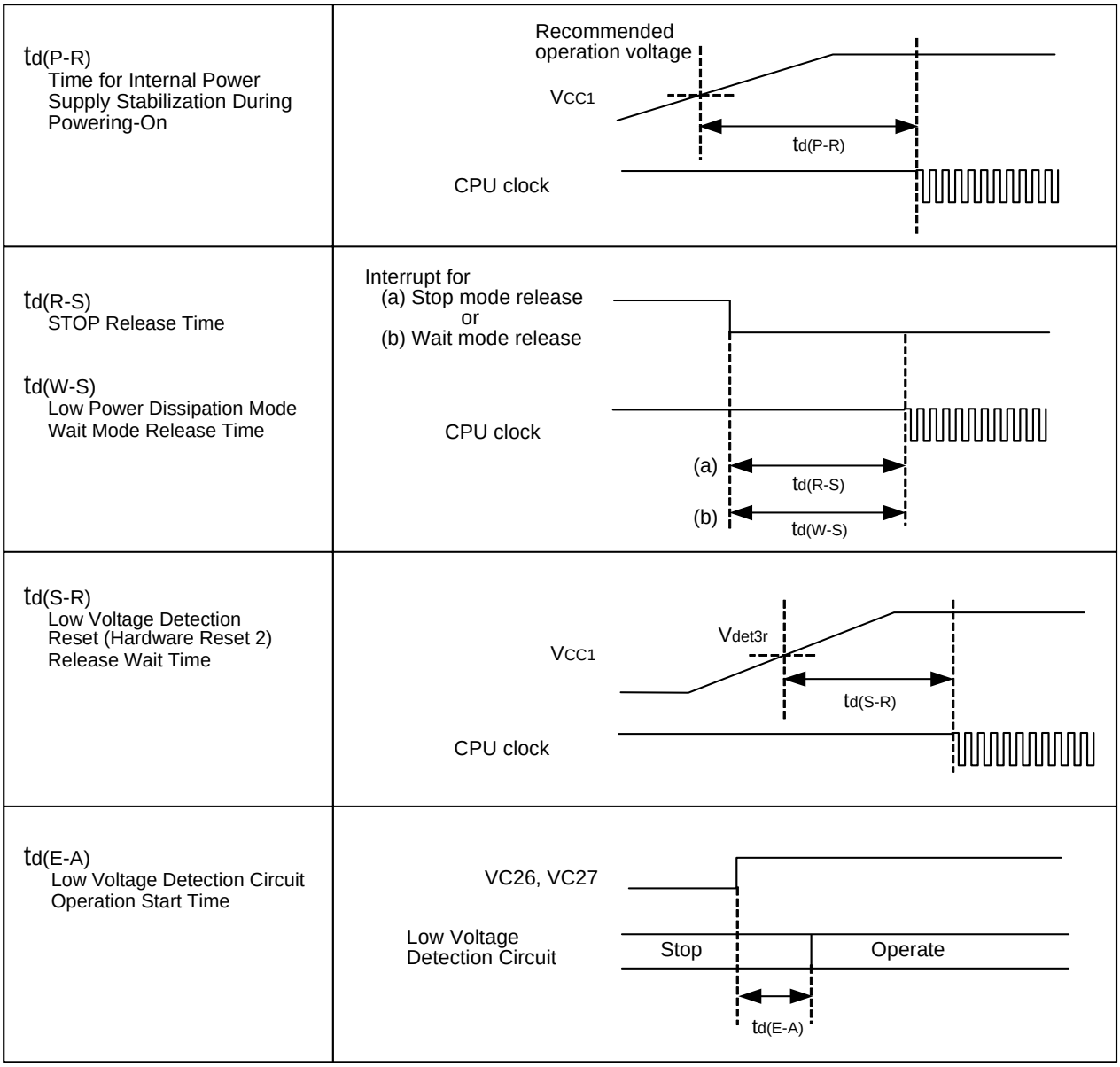



**Figure 5.1 Power Supply Circuit Timing Diagram**

# $V_{CC1}=V_{CC2}=5V$

**Table 5.11 Electrical Characteristics (1)** (1)

| Symbol | Parameter | | | Measuring Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Typ. | Max. | |
| $V_{OH}$ | HIGH Output Voltage (3) | P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1 | | $I_{OH}$=−5mA | $V_{CC1}$−2.0 | | $V_{CC1}$ | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7 | | $I_{OH}$=−5mA (2) | $V_{CC2}$−2.0 | | $V_{CC2}$ | |
| $V_{OH}$ | HIGH Output Voltage (3) | P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1 | | $I_{OH}$=−200μA | $V_{CC1}$−0.3 | | $V_{CC1}$ | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7 | | $I_{OH}$=−200μA (2) | $V_{CC2}$−0.3 | | $V_{CC2}$ | |
| $V_{OH}$ | HIGH Output Voltage XOUT | | HIGHPOWER | $I_{OH}$=−1mA | $V_{CC1}$−2.0 | | $V_{CC1}$ | V |
| | | | LOWPOWER | $I_{OH}$=−0.5mA | $V_{CC1}$−2.0 | | $V_{CC1}$ | |
| | HIGH Output Voltage XCOUT | | HIGHPOWER | With no load applied | | 2.5 | | V |
| | | | LOWPOWER | With no load applied | | 1.6 | | |
| $V_{OL}$ | LOW Output Voltage (3) | P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1 | | $I_{OL}$=5mA | | | 2.0 | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7 | | $I_{OL}$=5mA (2) | | | 2.0 | |
| $V_{OL}$ | LOW Output Voltage (3) | P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1 | | $I_{OL}$=200μA | | | 0.45 | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7 | | $I_{OL}$=200μA (2) | | | 0.45 | |
| $V_{OL}$ | LOW Output Voltage XOUT | | HIGHPOWER | $I_{OL}$=1mA | | | 2.0 | V |
| | | | LOWPOWER | $I_{OL}$=0.5mA | | | 2.0 | |
| | LOW Output Voltage XCOUT | | HIGHPOWER | With no load applied | | 0 | | V |
| | | | LOWPOWER | With no load applied | | 0 | | |
| $V_{T+}$-$V_{T-}$ | Hysteresis | $\overline{HOLD}$, $\overline{RDY}$, TA0IN to TA4IN, TB0IN to TB5IN, $\overline{INT0}$ to $\overline{INT5}$, $\overline{NMI}$, $\overline{ADTRG}$, $\overline{CTS0}$ to $\overline{CTS2}$, CLK0 to CLK4, TA0OUT to TA4OUT, $\overline{KI0}$ to $\overline{KI3}$, RXD0 to RXD2, SCL0 to SCL2, SDA0 to SDA2, SIN3, SIN4 | | | 0.2 | | 1.0 | V |
| $V_{T+}$-$V_{T-}$ | Hysteresis | $\overline{RESET}$ | | | 0.2 | | 2.5 | V |
| $I_{IH}$ | HIGH Input Current (3) | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1, XIN, $\overline{RESET}$, CNVSS, BYTE | | $V_I$=5V | | | 5.0 | μA |
| $I_{IL}$ | LOW Input Current (3) | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7,P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1, XIN, $\overline{RESET}$, CNVSS, BYTE | | $V_I$=0V | | | −5.0 | μA |
| $R_{PULLUP}$ | Pull-Up Resistance (3) | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7,P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1 | | $V_I$=0V | 30 | 50 | 170 | kΩ |
| $R_{fXIN}$ | Feedback Resistance XIN | | | | | 1.5 | | MΩ |
| $R_{fXCIN}$ | Feedback Resistance XCIN | | | | | 15 | | MΩ |
| $V_{RAM}$ | RAM Retention Voltage | | | At stop mode | 2.0 | | | V |

NOTES:
1. Referenced to $V_{CC1}$=$V_{CC2}$=4.2 to 5.5V, $V_{SS}$ = 0V at $T_{opr}$ = −20 to 85°C / −40 to 85°C, f(BCLK)=24MHz unless otherwise specified.
2. Where the product is used at $V_{CC1}$ = 5 V and $V_{CC2}$ = 3 V, refer to the 3 V version value for the pin specified value on $V_{CC2}$ port side.
3. There is no external connections for port P1_0 to P1_7, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version.

**Table 5.12 Electrical Characteristics (2)** (1)

| Symbol | Parameter | | Measuring Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Typ. | Max. | |
| $I_{CC}$ | Power Supply Current ($V_{CC1}$=$V_{CC2}$=4.0V to 5.5V) | In single-chip mode, the output pins are open and other pins are $V_{SS}$ | Mask ROM | f(BCLK)=24MHz<br>No division, PLL operation | | 14 | 20 | mA |
| | | | | No division,<br>On-chip oscillation | | 1 | | mA |
| | | | Flash Memory | f(BCLK)=24MHz,<br>No division, PLL operation | | 18 | 27 | mA |
| | | | | No division,<br>On-chip oscillation | | 1.8 | | mA |
| | | | Flash Memory Program | f(BCLK)=10MHz,<br>VCC1=5.0V | | 15 | | mA |
| | | | Flash Memory Erase | f(BCLK)=10MHz,<br>VCC1=5.0V | | 25 | | mA |
| | | | Mask ROM | f(XCIN)=32kHz<br>Low power dissipation mode, ROM (3) | | 25 | | µA |
| | | | Flash Memory | f(BCLK)=32kHz<br>Low power dissipation mode, RAM (3) | | 25 | | µA |
| | | | | f(BCLK)=32kHz<br>Low power dissipation mode, Flash Memory (3) | | 420 | | µA |
| | | | | On-chip oscillation,<br>Wait mode | | 50 | | µA |
| | | | Mask ROM Flash Memory | f(BCLK)=32kHz<br>Wait mode (2),<br>Oscillation capability High | | 7.5 | | µA |
| | | | | f(BCLK)=32kHz<br>Wait mode (2),<br>Oscillation capability Low | | 2.0 | | µA |
| | | | | Stop mode<br>Topr =25°C | | 0.8 | 3.0 | µA |
| $I_{det4}$ | Low Voltage Detection Dissipation Current (4) | | | | | 0.7 | 4 | µA |
| $I_{det3}$ | Reset Area Detection Dissipation Current (4) | | | | | 1.2 | 8 | µA |

NOTES:
1. Referenced to $V_{CC1}$=$V_{CC2}$=4.2 to 5.5V, $V_{SS}$ = 0V at $T_{opr}$ = –20 to 85°C / –40 to 85°C, f(BCLK)=24MHz unless otherwise specified.
2. With one timer operated using fC32.
3. This indicates the memory in which the program to be executed exists.
4. $I_{det}$ is dissipation current when the following bit is set to “1” (detection circuit enabled).

   $I_{det4}$: VC27 bit in the VCR2 register

   $I_{det3}$: VC26 bit in the VCR2 register

# $V_{CC1}=V_{CC2}=5V$

**Timing Requirements**
**($V_{CC1}$ = $V_{CC2}$ = 5V, $V_{SS}$ = 0V, at $T_{opr}$ = –20 to 85°C / –40 to 85°C unless otherwise specified)**

**Table 5.13 External Clock Input (XIN input) (1)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_c$ | External Clock Input Cycle Time | 62.5 | | ns |
| $t_{w(H)}$ | External Clock Input HIGH Pulse Width | 25 | | ns |
| $t_{w(L)}$ | External Clock Input LOW Pulse Width | 25 | | ns |
| $t_r$ | External Clock Rise Time | | 15 | ns |
| $t_f$ | External Clock Fall Time | | 15 | ns |

NOTES:
1. The condition is $V_{CC1}$=$V_{CC2}$=3.0 to 5.0V.

**Table 5.14 Memory Expansion Mode and Microprocessor Mode**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{ac1(RD-DB)}$ | Data Input Access Time (for setting with no wait) | | (NOTE 1) | ns |
| $t_{ac2(RD-DB)}$ | Data Input Access Time (for setting with wait) | | (NOTE 2) | ns |
| $t_{ac3(RD-DB)}$ | Data Input Access Time (when accessing multiplex bus area) | | (NOTE 3) | ns |
| $t_{su(DB-RD)}$ | Data Input Setup Time | 40 | | ns |
| $t_{su(RDY-BCLK)}$ | $\overline{RDY}$ Input Setup Time | 30 | | ns |
| $t_{su(HOLD-BCLK)}$ | $\overline{HOLD}$ Input Setup Time | 40 | | ns |
| $t_{h(RD-DB)}$ | Data Input Hold Time | 0 | | ns |
| $t_{h(BCLK-RDY)}$ | $\overline{RDY}$ Input Hold Time | 0 | | ns |
| $t_{h(BCLK-HOLD)}$ | $\overline{HOLD}$ Input Hold Time | 0 | | ns |

NOTES:
1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 45[ns]$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(BCLK)} - 45[ns]$$ n is ”2” for 1-wait setting, “3” for 2-wait setting and “4” for 3-wait setting.

3. Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(BCLK)} - 45[ns]$$ n is “2” for 2-wait setting, “3” for 3-wait setting.

# $V_{CC1}=V_{CC2}=5V$

**Timing Requirements**
**($V_{CC1}$ = $V_{CC2}$ = 5V, $V_{SS}$ = 0V, at $T_{opr}$ = –20 to 85°C / –40 to 85°C unless otherwise specified)**

**Table 5.15 Timer A Input (Counter Input in Event Counter Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TA)}$ | TAiIN Input Cycle Time | 100 | | ns |
| $t_{w(TAH)}$ | TAiIN Input HIGH Pulse Width | 40 | | ns |
| $t_{w(TAL)}$ | TAiIN Input LOW Pulse Width | 40 | | ns |

**Table 5.16 Timer A Input (Gating Input in Timer Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TA)}$ | TAiIN Input Cycle Time | 400 | | ns |
| $t_{w(TAH)}$ | TAiIN Input HIGH Pulse Width | 200 | | ns |
| $t_{w(TAL)}$ | TAiIN Input LOW Pulse Width | 200 | | ns |

**Table 5.17 Timer A Input (External Trigger Input in One-shot Timer Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TA)}$ | TAiIN Input Cycle Time | 200 | | ns |
| $t_{w(TAH)}$ | TAiIN Input HIGH Pulse Width | 100 | | ns |
| $t_{w(TAL)}$ | TAiIN Input LOW Pulse Width | 100 | | ns |

**Table 5.18 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{w(TAH)}$ | TAiIN Input HIGH Pulse Width | 100 | | ns |
| $t_{w(TAL)}$ | TAiIN Input LOW Pulse Width | 100 | | ns |

**Table 5.19 Timer A Input (Counter Increment/Decrement Input in Event Counter Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(UP)}$ | TAiOUT Input Cycle Time | 2000 | | ns |
| $t_{w(UPH)}$ | TAiOUT Input HIGH Pulse Width | 1000 | | ns |
| $t_{w(UPL)}$ | TAiOUT Input LOW Pulse Width | 1000 | | ns |
| $t_{su(UP-TIN)}$ | TAiOUT Input Setup Time | 400 | | ns |
| $t_{h(TIN-UP)}$ | TAiOUT Input Hold Time | 400 | | ns |

**Table 5.20 Timer A Input (Two-phase Pulse Input in Event Counter Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TA)}$ | TAiIN Input Cycle Time | 800 | | ns |
| $t_{su(TAIN-TAOUT)}$ | TAiOUT Input Setup Time | 200 | | ns |
| $t_{su(TAOUT-TAIN)}$ | TAiIN Input Setup Time | 200 | | ns |

# $V_{CC1}=V_{CC2}=5V$

**Timing Requirements**
**($V_{CC1}$ = $V_{CC2}$ = 5V, $V_{SS}$ = 0V, at $T_{opr}$ = –20 to 85°C / –40 to 85°C unless otherwise specified)**

**Table 5.21 Timer B Input (Counter Input in Event Counter Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TB)}$ | TBiIN Input Cycle Time (counted on one edge) | 100 | | ns |
| $t_{w(TBH)}$ | TBiIN Input HIGH Pulse Width (counted on one edge) | 40 | | ns |
| $t_{w(TBL)}$ | TBiIN Input LOW Pulse Width (counted on one edge) | 40 | | ns |
| $t_{c(TB)}$ | TBiIN Input Cycle Time (counted on both edges) | 200 | | ns |
| $t_{w(TBH)}$ | TBiIN Input HIGH Pulse Width (counted on both edges) | 80 | | ns |
| $t_{w(TBL)}$ | TBiIN Input LOW Pulse Width (counted on both edges) | 80 | | ns |

**Table 5.22 Timer B Input (Pulse Period Measurement Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TB)}$ | TBiIN Input Cycle Time | 400 | | ns |
| $t_{w(TBH)}$ | TBiIN Input HIGH Pulse Width | 200 | | ns |
| $t_{w(TBL)}$ | TBiIN Input LOW Pulse Width | 200 | | ns |

**Table 5.23 Timer B Input (Pulse Width Measurement Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TB)}$ | TBiIN Input Cycle Time | 400 | | ns |
| $t_{w(TBH)}$ | TBiIN Input HIGH Pulse Width | 200 | | ns |
| $t_{w(TBL)}$ | TBiIN Input LOW Pulse Width | 200 | | ns |

**Table 5.24 A/D Trigger Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(AD)}$ | $\overline{\text{ADTRG}}$ Input Cycle Time | 1000 | | ns |
| $t_{w(ADL)}$ | $\overline{\text{ADTRG}}$ input LOW Pulse Width | 125 | | ns |

**Table 5.25 Serial Interface**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(CK)}$ | CLKi Input Cycle Time | 200 | | ns |
| $t_{w(CKH)}$ | CLKi Input HIGH Pulse Width | 100 | | ns |
| $t_{w(CKL)}$ | CLKi Input LOW Pulse Width | 100 | | ns |
| $t_{d(C-Q)}$ | TXDi Output Delay Time | | 80 | ns |
| $t_{h(C-Q)}$ | TXDi Hold Time | 0 | | ns |
| $t_{su(D-C)}$ | RXDi Input Setup Time | 70 | | ns |
| $t_{h(C-D)}$ | RXDi Input Hold Time | 90 | | ns |

**Table 5.26 External Interrupt $\overline{\text{INTi}}$ Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{w(INH)}$ | $\overline{\text{INTi}}$ Input HIGH Pulse Width | 250 | | ns |
| $t_{w(INL)}$ | $\overline{\text{INTi}}$ Input LOW Pulse Width | 250 | | ns |

# $V_{CC1}=V_{CC2}=5V$

## Switching Characteristics

**($V_{CC1}$ = $V_{CC2}$ = 5V, $V_{SS}$ = 0V, at $T_{opr}$ = –20 to 85°C / –40 to 85°C unless otherwise specified)**

**Table 5.27 Memory Expansion and Microprocessor Modes (for setting with no wait)**

| Symbol | Parameter | | Standard | | Unit |
|---|---|---|---|---|---|
| | | | Min. | Max. | |
| td(BCLK-AD) | Address Output Delay Time | See **Figure 5.2** | | 25 | ns |
| th(BCLK-AD) | Address Output Hold Time (in relation to BCLK) | | 4 | | ns |
| th(RD-AD) | Address Output Hold Time (in relation to RD) | | 0 | | ns |
| th(WR-AD) | Address Output Hold Time (in relation to WR) | | (NOTE 2) | | ns |
| td(BCLK-CS) | Chip Select Output Delay Time | | | 25 | ns |
| th(BCLK-CS) | Chip Select Output Hold Time (in relation to BCLK) | | 4 | | ns |
| td(BCLK-ALE) | ALE Signal Output Delay Time | | | 15 | ns |
| th(BCLK-ALE) | ALE Signal Output Hold Time | | –4 | | ns |
| td(BCLK-RD) | RD Signal Output Delay Time | | | 25 | ns |
| th(BCLK-RD) | RD Signal Output Hold Time | | 0 | | ns |
| td(BCLK-WR) | WR Signal Output Delay Time | | | 25 | ns |
| th(BCLK-WR) | WR Signal Output Hold Time | | 0 | | ns |
| td(BCLK-DB) | Data Output Delay Time (in relation to BCLK) | | | 40 | ns |
| th(BCLK-DB) | Data Output Hold Time (in relation to BCLK) (3) | | 4 | | ns |
| td(DB-WR) | Data Output Delay Time (in relation to WR) | | (NOTE 1) | | ns |
| th(WR-DB) | Data Output Hold Time (in relation to WR) (3) | | (NOTE 2) | | ns |
| td(BCLK-HLDA) | HLDA Output Delay Time | | | 40 | ns |

NOTES:

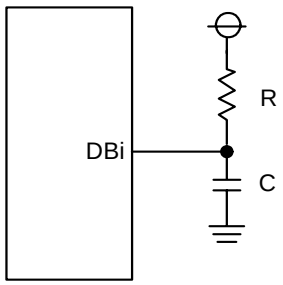
1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5\times10^{9}}{f(BCLK)} - 40[ns]$$ f(BCLK) is 12.5MHz or less.

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5\times10^{9}}{f(BCLK)} - 10[ns]$$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
   Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
   Hold time of data bus is expressed in
   $t = -CR \times \ln(1 - V_{OL} / V_{CC2})$
   by a circuit of the right figure.
   For example, when $V_{OL} = 0.2V_{CC2}$, C = 30pF, R = 1kΩ, hold time of output "L" level is
   $t = -30pF \times 1k\Omega \times \ln(1 - 0.2V_{CC2} / V_{CC2})$
   = 6.7ns.



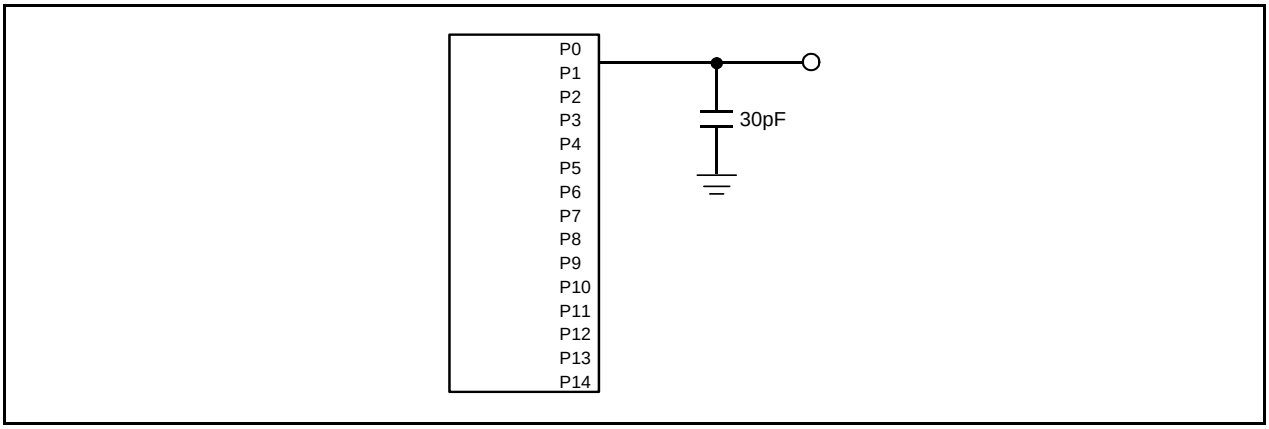




**Figure 5.2 Ports P0 to P14 Measurement Circuit**

# $V_{CC1}=V_{CC2}=5V$

## Switching Characteristics

**($V_{CC1}$ = $V_{CC2}$ = 5V, $V_{SS}$ = 0V, at $T_{opr}$ = –20 to 85°C / –40 to 85°C unless otherwise specified)**

**Table 5.28 Memory Expansion and Microprocessor Modes (for 1- to 3-wait setting and external area access)**

| Symbol | Parameter | | Standard | | Unit |
|---|---|---|---|---|---|
| | | | Min. | Max. | |
| $t_{d(BCLK-AD)}$ | Address Output Delay Time | See **Figure 5.2** | | 25 | ns |
| $t_{h(BCLK-AD)}$ | Address Output Hold Time (in relation to BCLK) | | 4 | | ns |
| $t_{h(RD-AD)}$ | Address Output Hold Time (in relation to RD) | | 0 | | ns |
| $t_{h(WR-AD)}$ | Address Output Hold Time (in relation to WR) | | (NOTE 2) | | ns |
| $t_{d(BCLK-CS)}$ | Chip Select Output Delay Time | | | 25 | ns |
| $t_{h(BCLK-CS)}$ | Chip Select Output Hold Time (in relation to BCLK) | | 4 | | ns |
| $t_{d(BCLK-ALE)}$ | ALE Signal Output Delay Time | | | 15 | ns |
| $t_{h(BCLK-ALE)}$ | ALE Signal Output Hold Time | | -4 | | ns |
| $t_{d(BCLK-RD)}$ | RD Signal Output Delay Time | | | 25 | ns |
| $t_{h(BCLK-RD)}$ | RD Signal Output Hold Time | | 0 | | ns |
| $t_{d(BCLK-WR)}$ | WR Signal Output Delay Time | | | 25 | ns |
| $t_{h(BCLK-WR)}$ | WR Signal Output Hold Time | | 0 | | ns |
| $t_{d(BCLK-DB)}$ | Data Output Delay Time (in relation to BCLK) | | | 40 | ns |
| $t_{h(BCLK-DB)}$ | Data Output Hold Time (in relation to BCLK) (3) | | 4 | | ns |
| $t_{d(DB-WR)}$ | Data Output Delay Time (in relation to WR) | | (NOTE 1) | | ns |
| th(WR-DB) | Data Output Hold Time (in relation to WR)(3) | | (NOTE 2) | | ns |
| $t_{d(BCLK-HLDA)}$ | HLDA Output Delay Time | | | 40 | ns |

NOTES:

1. Calculated according to the BCLK frequency as follows:

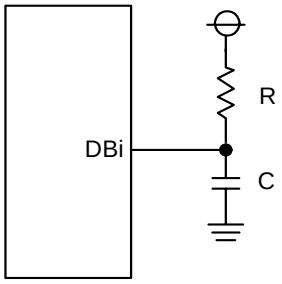
$$\frac{(n-0.5)\times 10^9}{f(BCLK)} - 40[ns]$$

n is “1” for 1-wait setting, “2” for 2-wait setting and “3” for 3-wait setting.
(BCLK) is 12.5MHz or less.

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5\times 10^9}{f(BCLK)} - 10[ns]$$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
Hold time of data bus is expressed in
$t = -CR \times \ln(1 - V_{OL} / V_{CC2})$
by a circuit of the right figure.
For example, when $V_{OL}$ = 0.2$V_{CC2}$, C = 30pF, R = 1kΩ, hold time of output ”L” level is
$t = -30pF \times 1k\Omega \times \ln(1 - 0.2V_{CC2} / V_{CC2})$
= 6.7ns.



## $V_{CC1}=V_{CC2}=5V$

### Switching Characteristics

**($V_{CC1}$ = $V_{CC2}$ = 5V, $V_{SS}$ = 0V, at $T_{opr}$ = –20 to 85°C / –40 to 85°C unless otherwise specified)**

**Table 5.29 Memory Expansion and Microprocessor Modes (for 2- to 3-wait setting, external area access and multiplex bus selection)**

| Symbol | Parameter | | Standard | | Unit |
|---|---|---|---|---|---|
| | | | Min. | Max. | |
| td(BCLK-AD) | Address Output Delay Time | See **Figure 5.2** | | 25 | ns |
| th(BCLK-AD) | Address Output Hold Time (in relation to BCLK) | | 4 | | ns |
| th(RD-AD) | Address Output Hold Time (in relation to RD) | | (NOTE 1) | | ns |
| th(WR-AD) | Address Output Hold Time (in relation to WR) | | (NOTE 1) | | ns |
| td(BCLK-CS) | Chip Select Output Delay Time | | | 25 | ns |
| th(BCLK-CS) | Chip Select Output Hold Time (in relation to BCLK) | | 4 | | ns |
| th(RD-CS) | Chip Select Output Hold Time (in relation to RD) | | (NOTE 1) | | ns |
| th(WR-CS) | Chip Select Output Hold Time (in relation to WR) | | (NOTE 1) | | ns |
| td(BCLK-RD) | RD Signal Output Delay Time | | | 25 | ns |
| th(BCLK-RD) | RD Signal Output Hold Time | | 0 | | ns |
| td(BCLK-WR) | WR Signal Output Delay Time | | | 25 | ns |
| th(BCLK-WR) | WR Signal Output Hold Time | | 0 | | ns |
| td(BCLK-DB) | Data Output Delay Time (in relation to BCLK) | | | 40 | ns |
| th(BCLK-DB) | Data Output Hold Time (in relation to BCLK) | | 4 | | ns |
| td(DB-WR) | Data Output Delay Time (in relation to WR) | | (NOTE 2) | | ns |
| th(WR-DB) | Data Output Hold Time (in relation to WR) | | (NOTE 1) | | ns |
| td(BCLK-HLDA) | HLDA Output Delay Time | | | 40 | ns |
| td(BCLK-ALE) | ALE Signal Output Delay Time (in relation to BCLK) | | | 15 | ns |
| th(BCLK-ALE) | ALE Signal Output Hold Time (in relation to BCLK) | | –4 | | ns |
| td(AD-ALE) | ALE Signal Output Delay Time (in relation to Address) | | (NOTE 3) | | ns |
| th(AD-ALE) | ALE Signal Output Hold Time (in relation to Address) | | (NOTE 4) | | ns |
| td(AD-RD) | RD Signal Output Delay From the End of Address | | 0 | | ns |
| td(AD-WR) | WR Signal Output Delay From the End of Address | | 0 | | ns |
| tdz(RD-AD) | Address Output Floating Start Time | | | 8 | ns |

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 10[ns]$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(BCLK)} - 40[ns]$$

n is “2” for 2-wait setting, “3” for 3-wait setting.

3. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 25[ns]$$

4. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 15[ns]$$

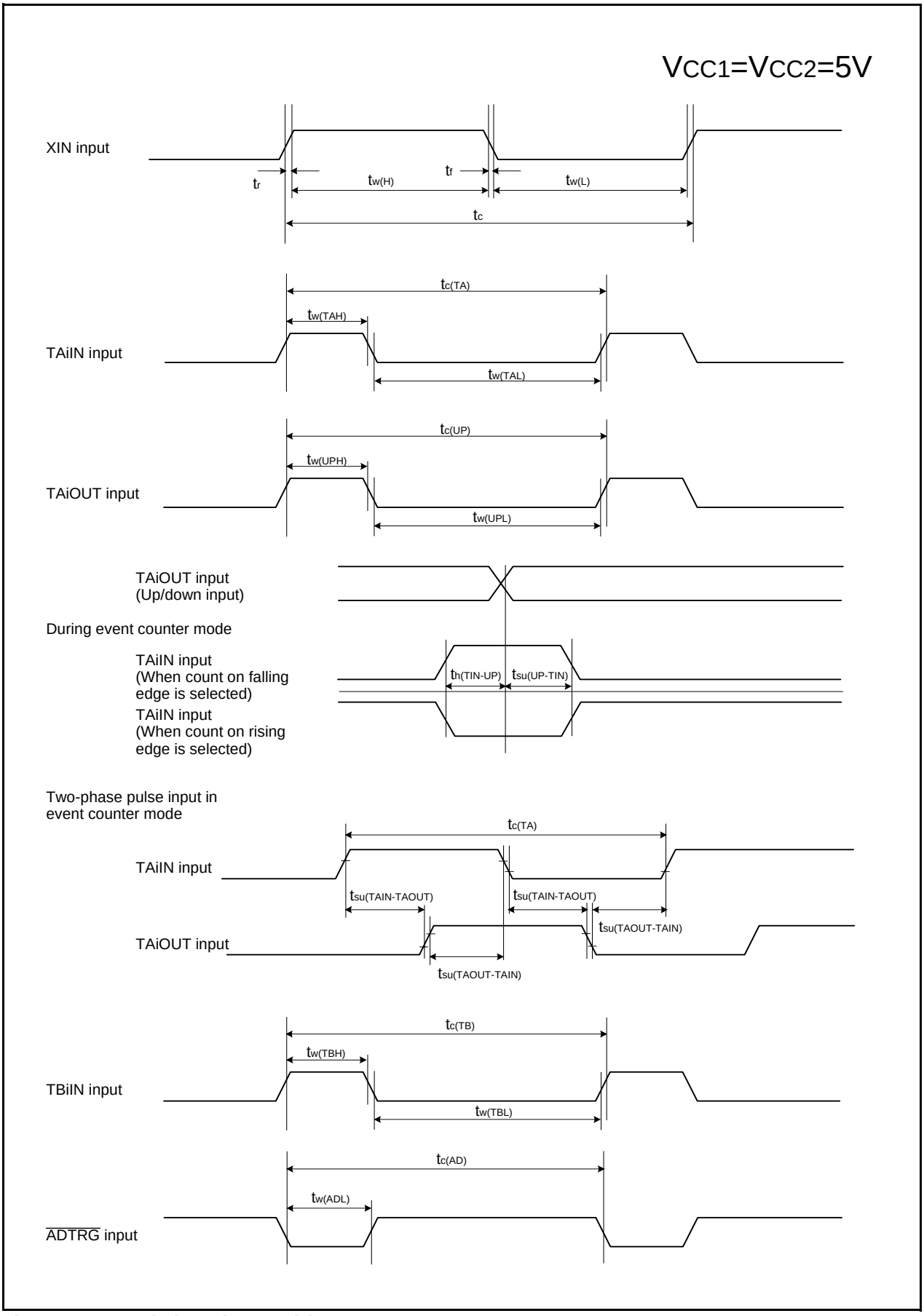



**Figure 5.3 Timing Diagram (1)**

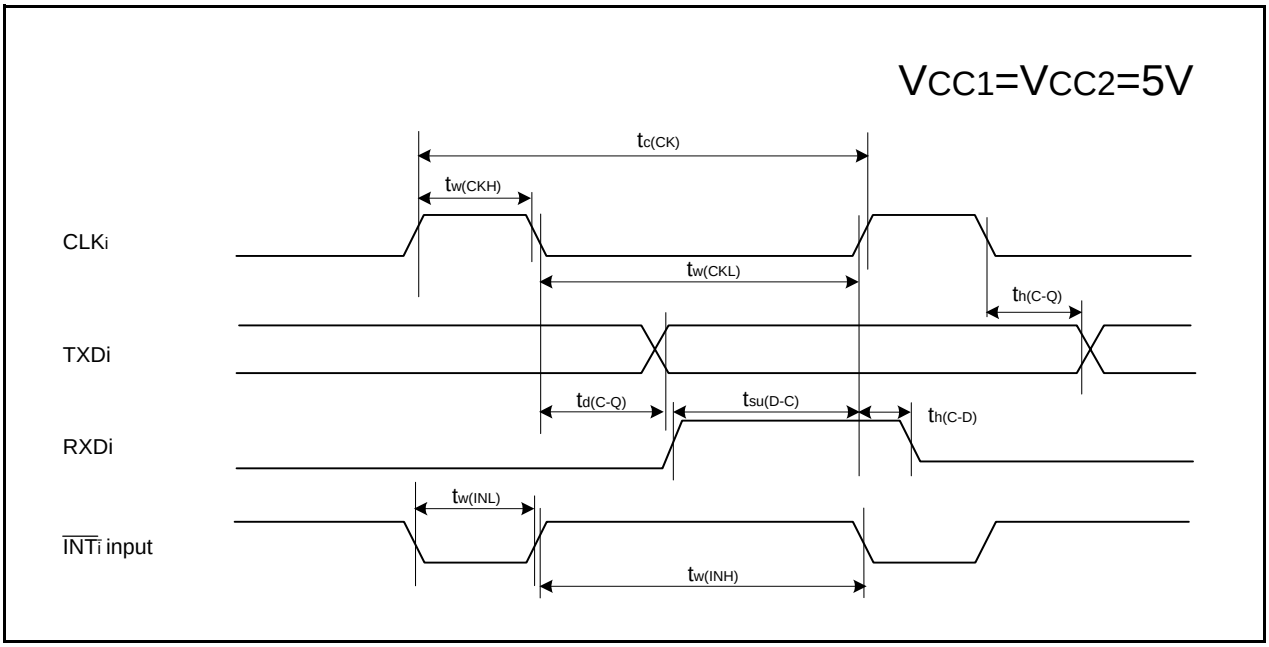
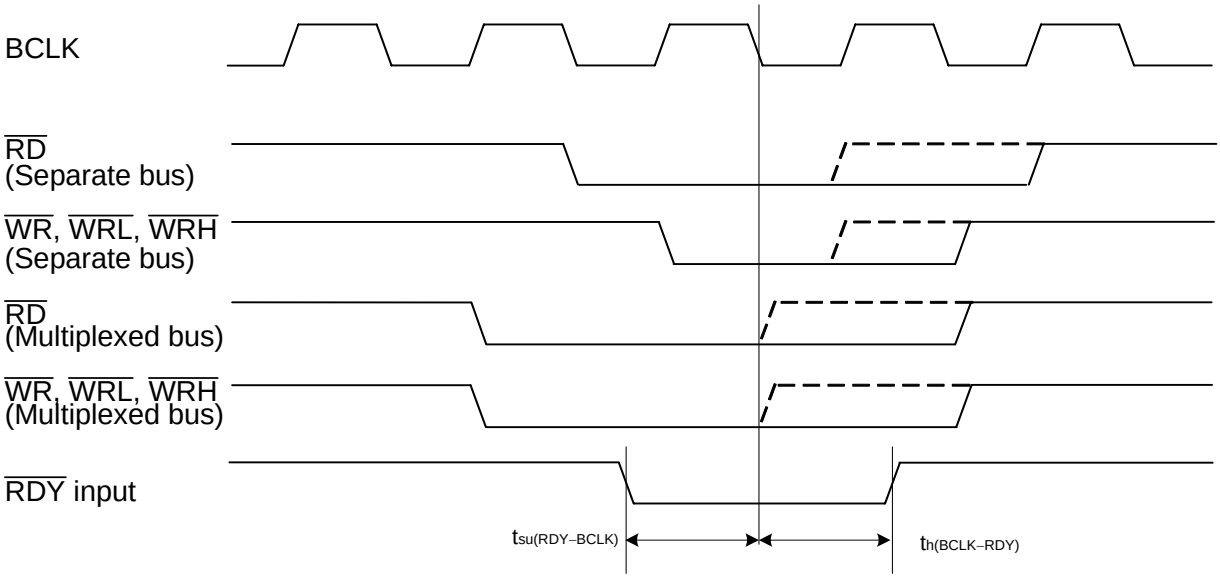



**Figure 5.4 Timing Diagram (2)**

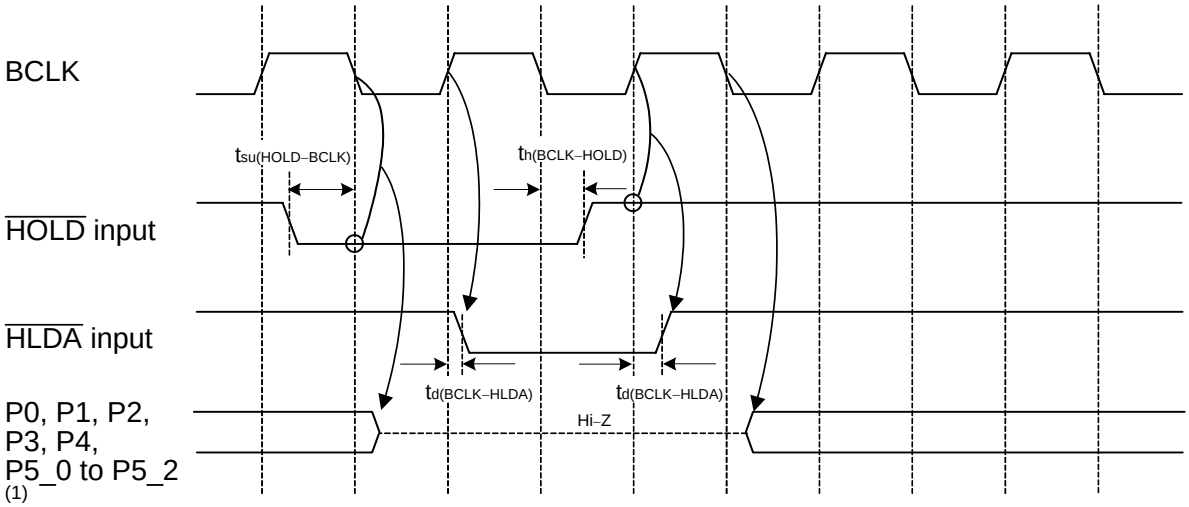
$V_{CC1}=V_{CC2}=5V$

**Memory Expansion Mode, Microprocessor Mode**

**(**Effective for setting with wait**)**




**(**Common to setting with wait and setting without wait**)**




NOTES:

1. These pins are set to high-impedance regardless of the input level of the BYTE pin, PM06 bit in PM0 register and PM11 bit in PM1 register.

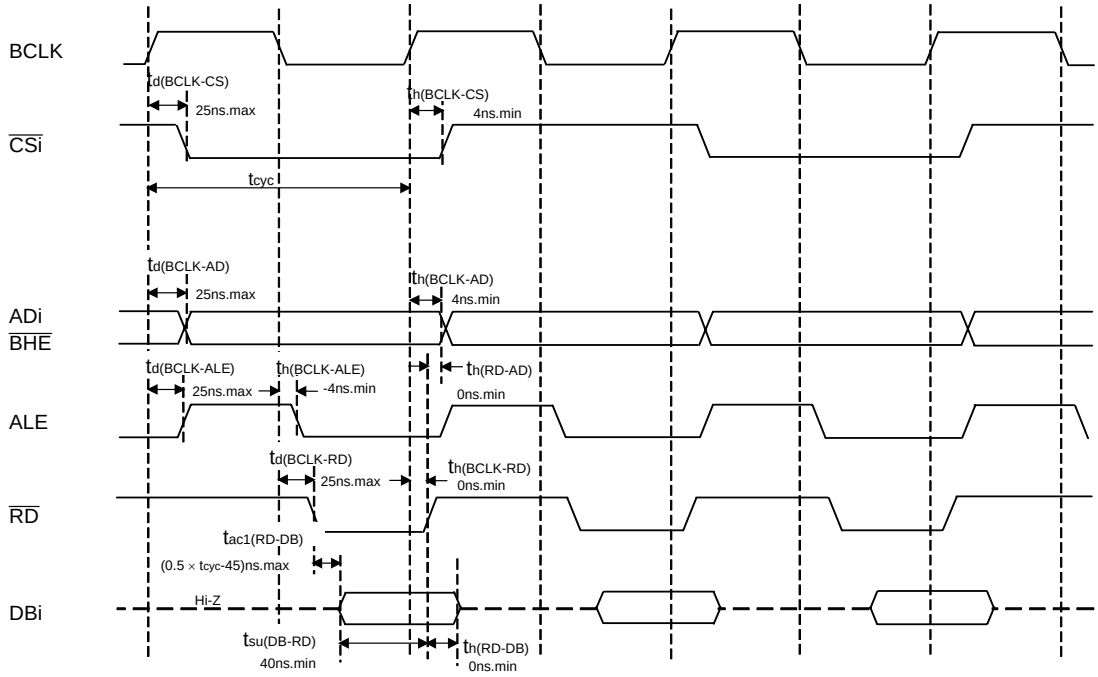
· Measuring conditions :
· $V_{CC1}=V_{CC2}=5V$
· Input timing voltage : Determined with $V_{IL}=1.0V$, $V_{IH}=4.0V$
· Output timing voltage : Determined with $V_{OL}=2.5V$, $V_{OH}=2.5V$

**Figure 5.5 Timing Diagram (3)**

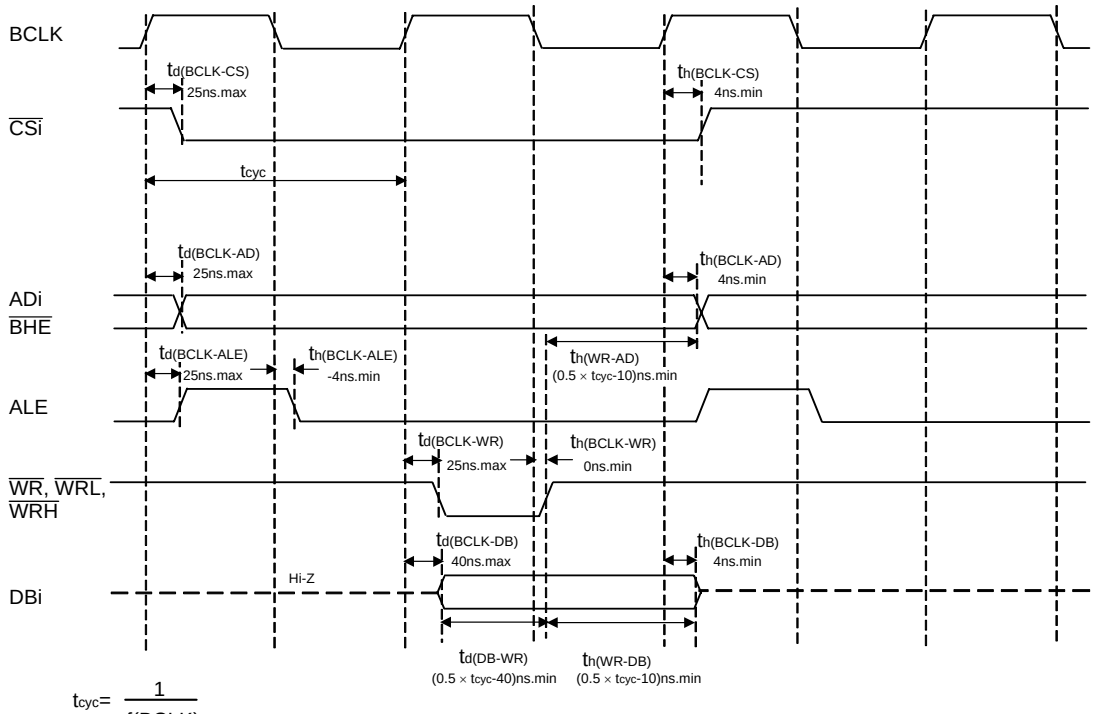
**Memory Expansion Mode, Microprocessor Mode**
**(**For setting with no wait**)**

$V_{CC1}=V_{CC2}=5V$

**Read timing**




**Write timing**




$$t_{cyc}=\frac{1}{f(BCLK)}$$

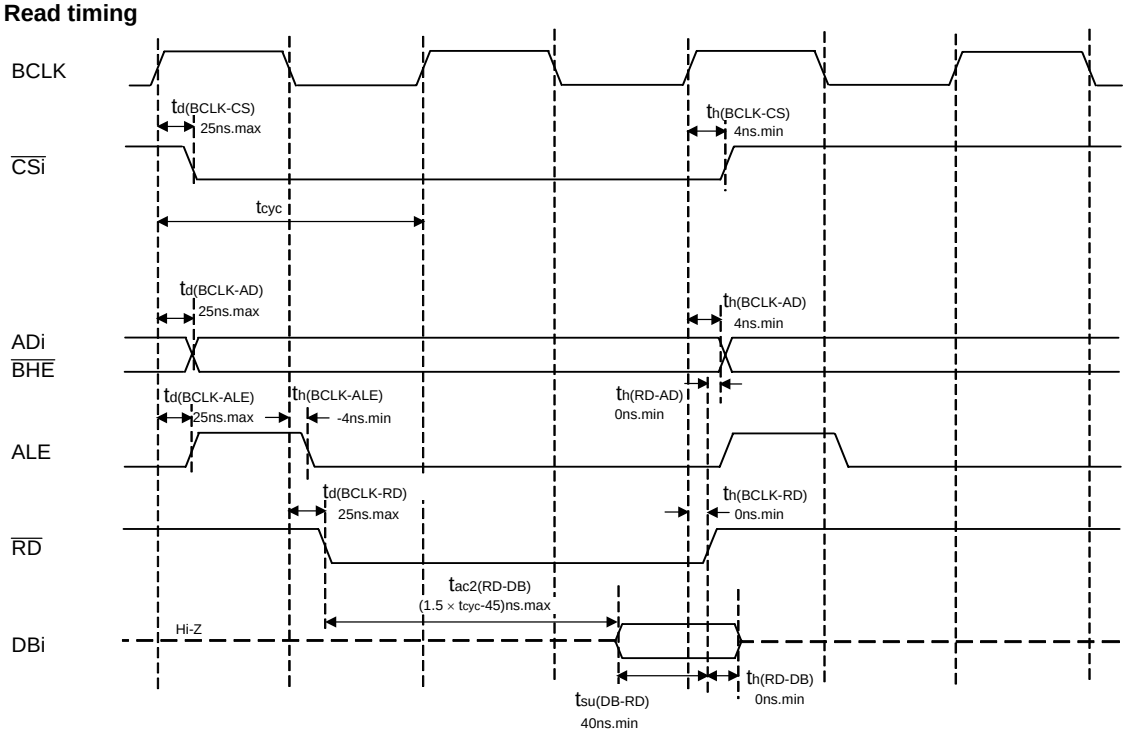
Measuring conditions
· $V_{CC1}=V_{CC2}=5V$
· Input timing voltage : $V_{IL}=0.8V$, $V_{IH}=2.0V$
· Output timing voltage : $V_{OL}=0.4V$, $V_{OH}=2.4V$

**Figure 5.6 Timing Diagram (4)**

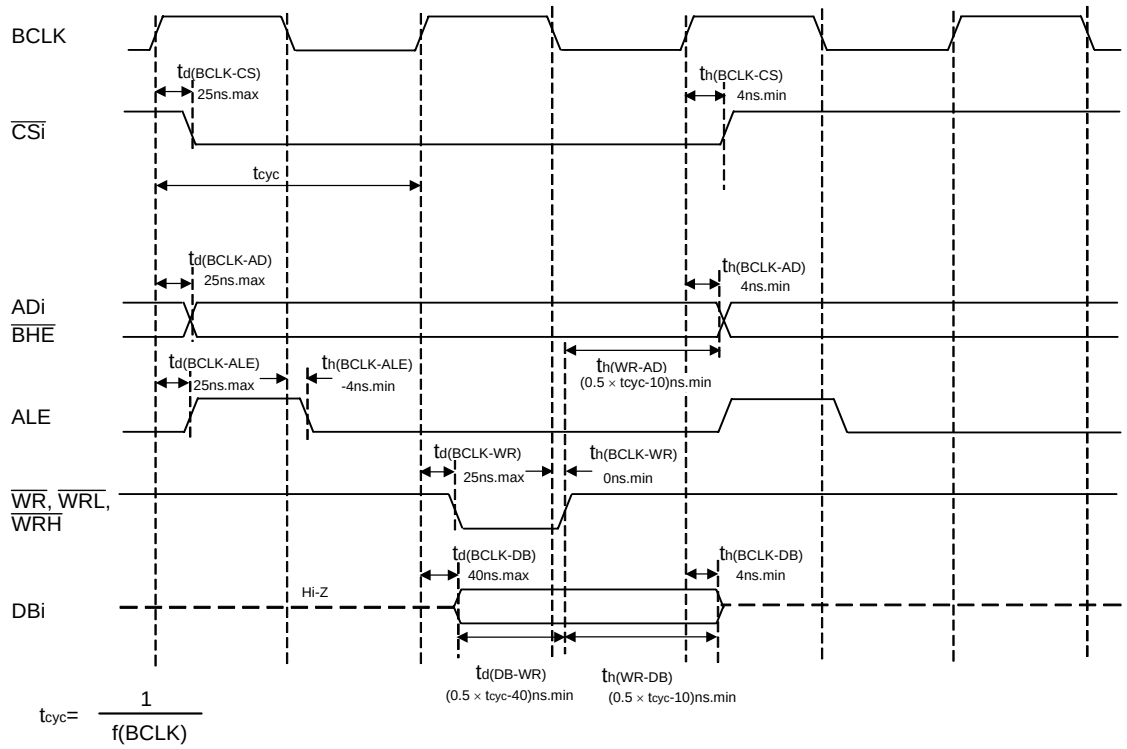
$V_{CC1}=V_{CC2}=5V$

**Memory Expansion Mode, Microprocessor Mode**
**(**for 1-wait setting and external area access**)**

**Read timing**




**Write timing**




$$t_{cyc}=\frac{1}{f(BCLK)}$$

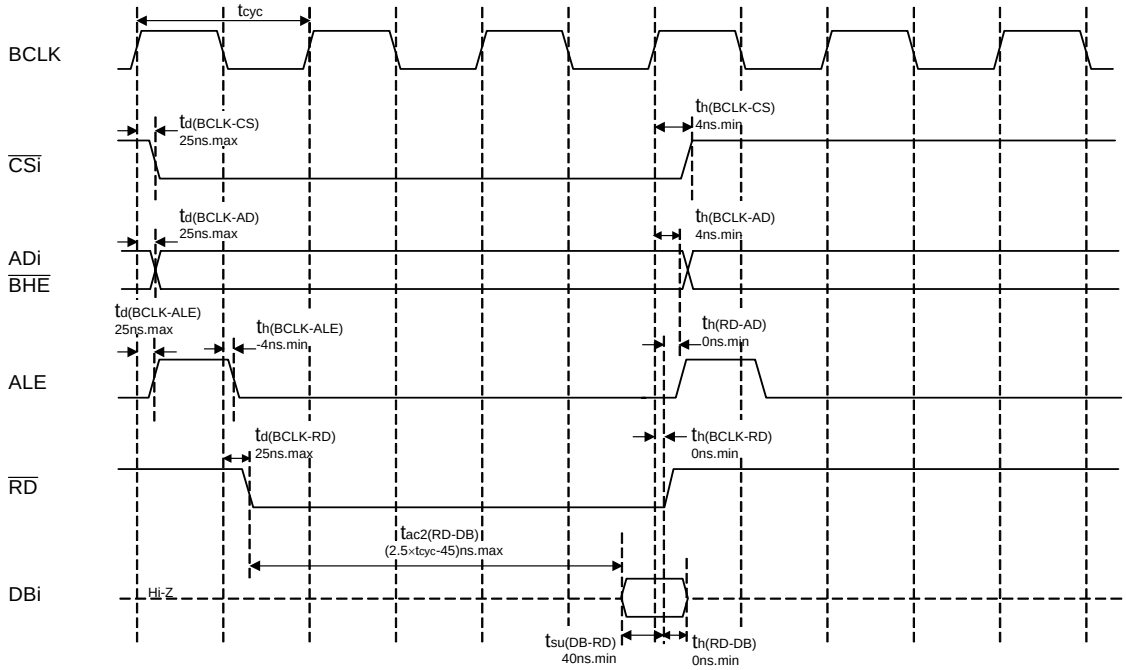
Measuring conditions
· $V_{CC1}=V_{CC2}=5V$
· Input timing voltage : $V_{IL}=0.8V$, $V_{IH}=2.0V$
· Output timing voltage : $V_{OL}=0.4V$, $V_{OH}=2.4V$

**Figure 5.7 Timing Diagram (5)**

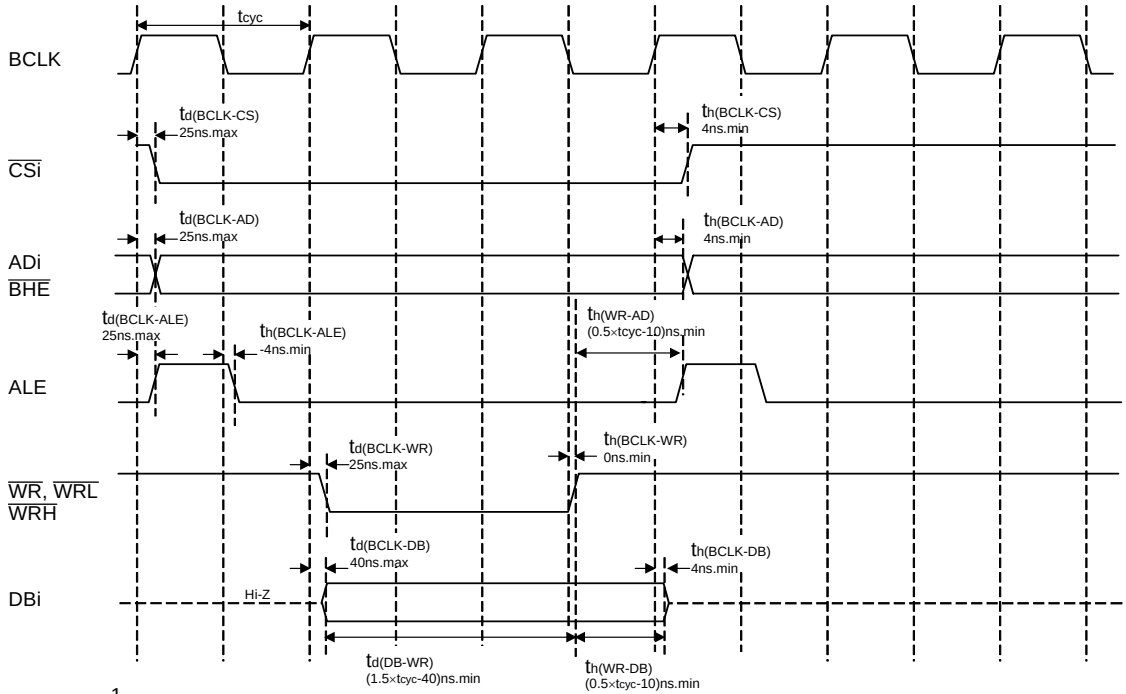
$V_{CC1}=V_{CC2}=5V$

**Memory Expansion Mode, Microprocessor Mode**
**(**for 2-wait setting and external area access**)**

**Read timing**




**Write timing**




$$T_{cyc}=\frac{1}{f(BCLK)}$$

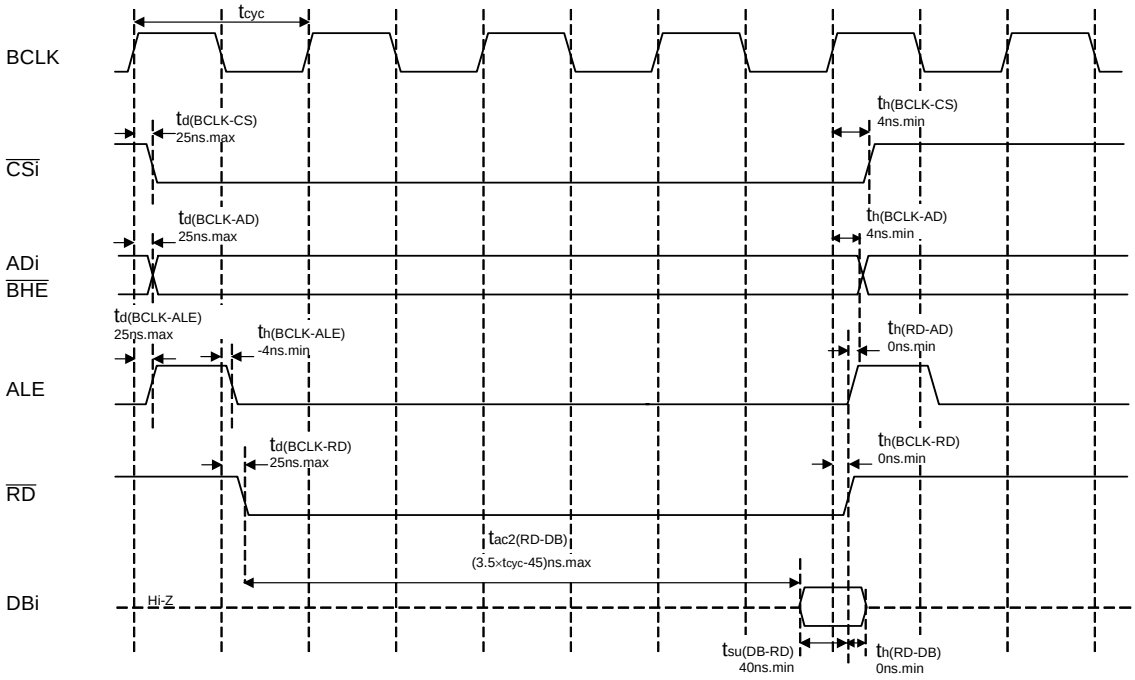
Measuring conditions
· $V_{CC1}=V_{CC2}=5V$
· Input timing voltage : $V_{IL}=0.8V$, $V_{IH}=2.0V$
· Output timing voltage : $V_{OL}=0.4V$, $V_{OH}=2.4V$

**Figure 5.8 Timing Diagram (6)**

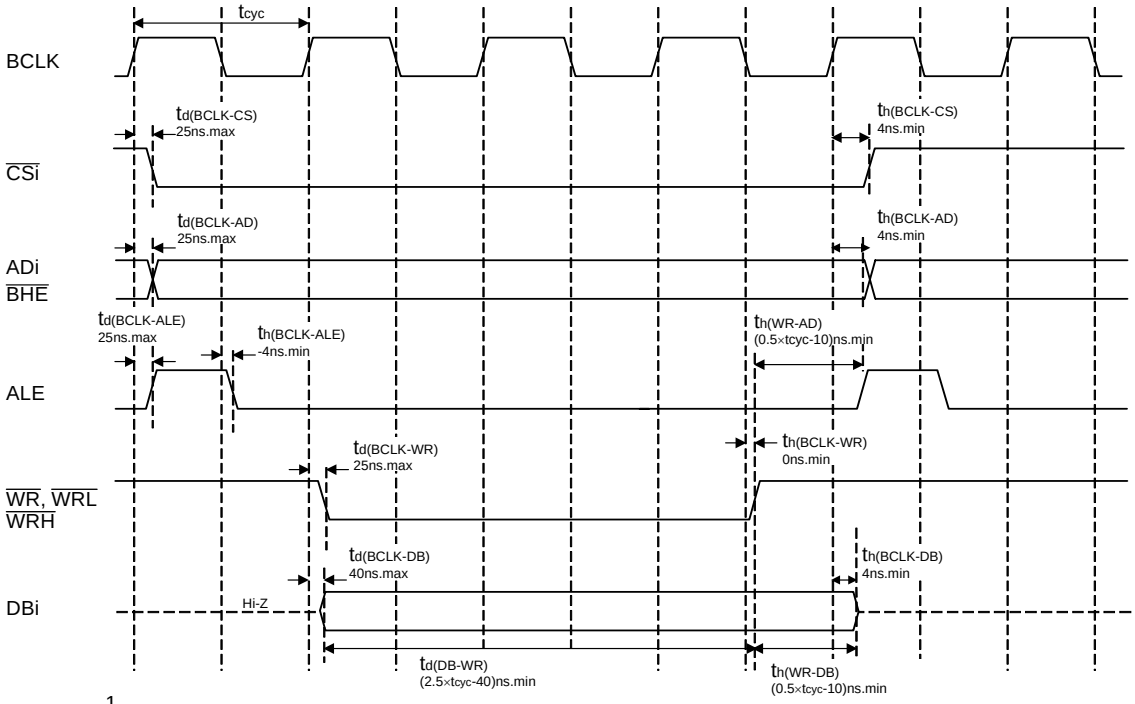
**Memory Expansion Mode, Microprocessor Mode**
**(**for 3-wait setting and external area access**)**

$V_{CC1}=V_{CC2}=5V$

**Read timing**




**Write timing**




$$t_{cyc}=\frac{1}{f(BCLK)}$$

Measuring conditions
· $V_{CC1}=V_{CC2}=5V$
· Input timing voltage : $V_{IL}=0.8V$, $V_{IH}=2.0V$
· Output timing voltage : $V_{OL}=0.4V$, $V_{OH}=2.4V$

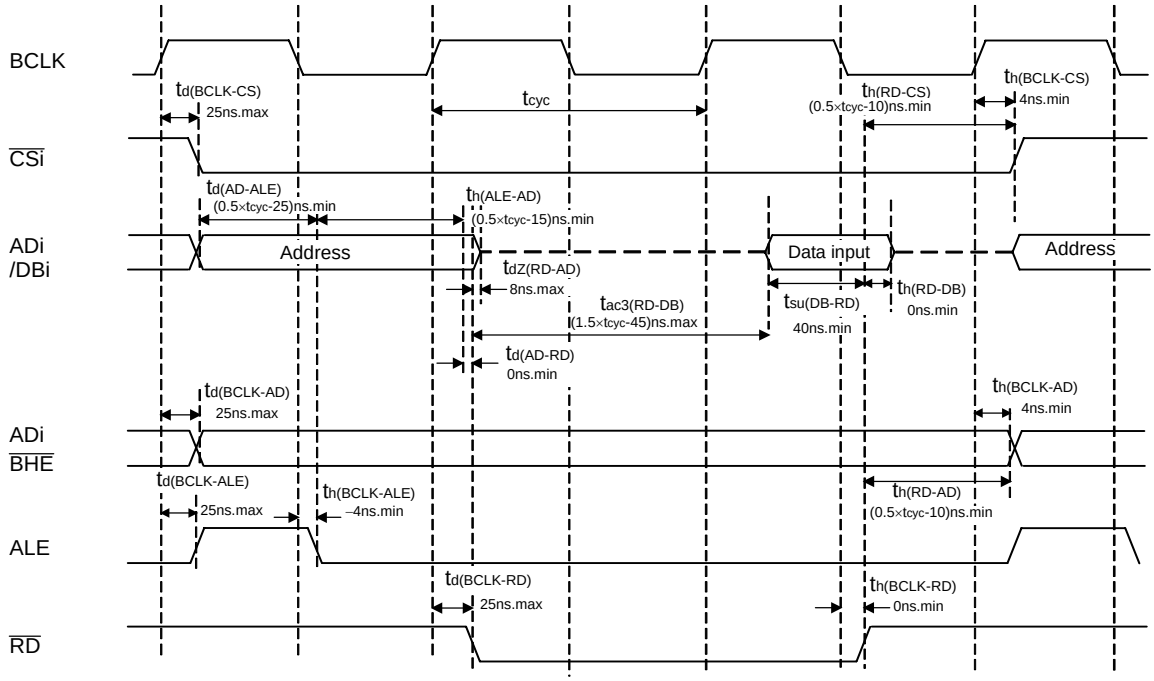
**Figure 5.9 Timing Diagram (7)**

$V_{CC1}=V_{CC2}=5V$

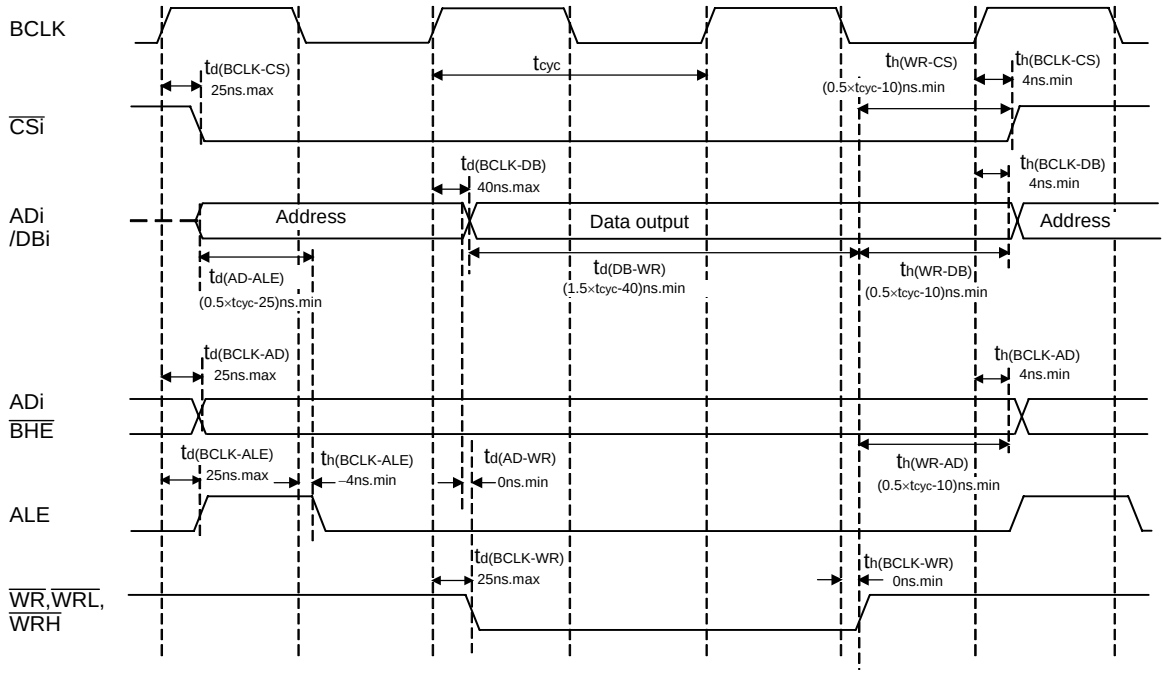
## Memory Expansion Mode, Microprocessor Mode

**(**For 1- or 2-wait setting, external area access and multiplex bus selection**)**

### Read timing




### Write timing



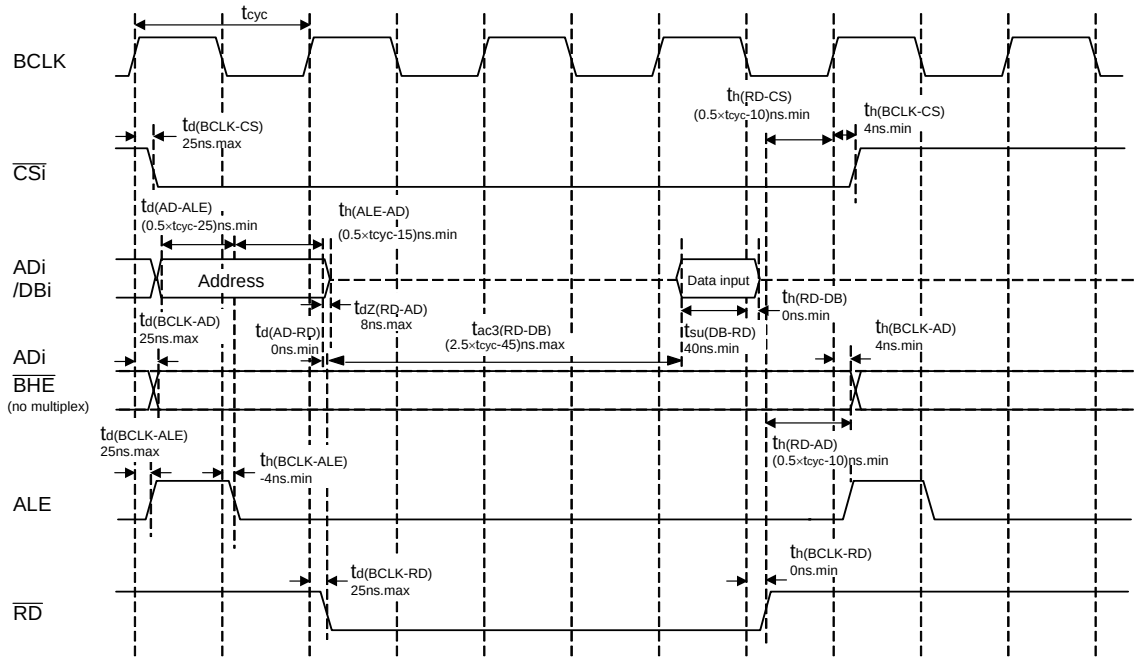

Measuring conditions
· $V_{CC1}=V_{CC2}=5V$
· Input timing voltage : $V_{IL}=0.8V$, $V_{IH}=2.0V$
· Output timing voltage : $V_{OL}=0.4V$, $V_{OH}=2.4V$

**Figure 5.10 Timing Diagram (8)**

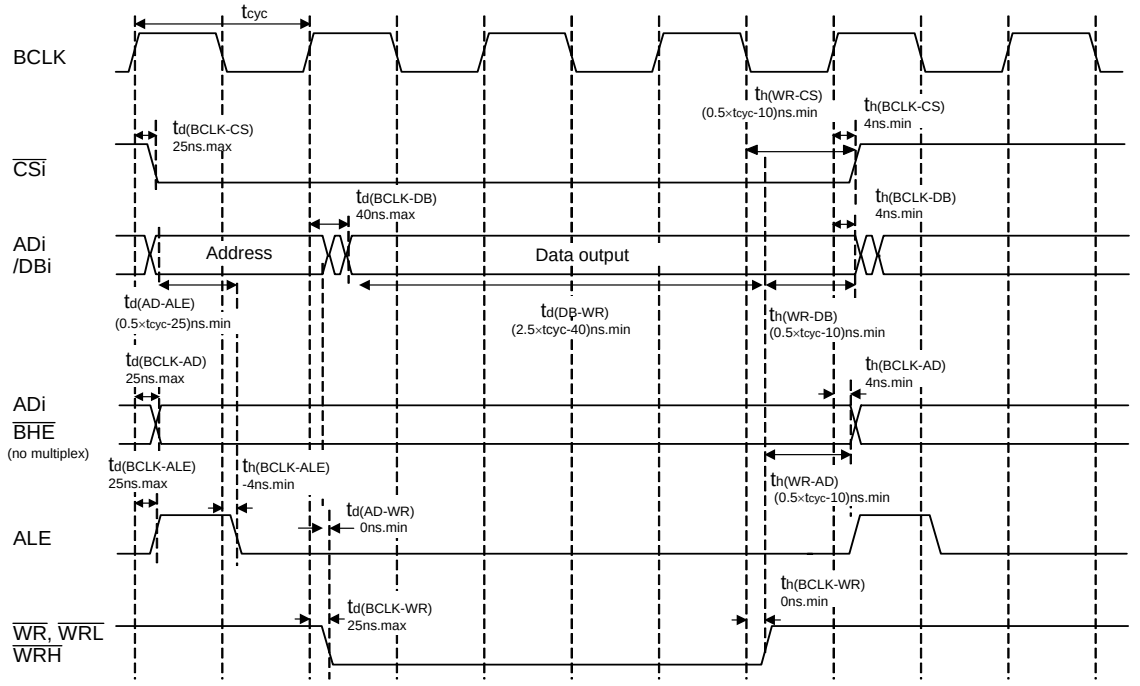
$V_{CC1}=V_{CC2}=5V$

**Memory Expansion Mode, Microprocessor Mode**
**(**For 3-wait setting, external area access and multiplex bus selection**)**

**Read timing**




**Write timing**




$$t_{cyc}=\frac{1}{f(BCLK)}$$

Measuring conditions
· $V_{CC1}=V_{CC2}=5V$
· Input timing voltage : $V_{IL}=0.8V$, $V_{IH}=2.0V$
· Output timing voltage : $V_{OL}=0.4V$, $V_{OH}=2.4V$

**Figure 5.11 Timing Diagram (9)**

## $V_{CC1}=V_{CC2}=3V$

**Table 5.30 Electrical Characteristics (1)** (1)

| Symbol | Parameter | | Measuring Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $V_{OH}$ | HIGH Output Voltage (3) | P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1 | $I_{OH}$=–1mA | $V_{CC1}$–0.5 | | $V_{CC1}$ | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7 | $I_{OH}$=–1mA (2) | $V_{CC2}$–0.5 | | $V_{CC2}$ | |
| $V_{OH}$ | HIGH Output Voltage XOUT | HIGHPOWER | $I_{OH}$=–0.1mA | $V_{CC1}$–0.5 | | $V_{CC1}$ | V |
| | | LOWPOWER | $I_{OH}$=–50µA | $V_{CC1}$–0.5 | | $V_{CC1}$ | |
| | HIGH Output Voltage XCOUT | HIGHPOWER | With no load applied | | 2.5 | | V |
| | | LOWPOWER | With no load applied | | 1.6 | | |
| $V_{OL}$ | LOW Output Voltage (3) | P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1 | $I_{OL}$=1mA | | | 0.5 | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7 | $I_{OL}$=1mA (2) | | | 0.5 | |
| $V_{OL}$ | LOW Output Voltage XOUT | HIGHPOWER | $I_{OL}$=0.1mA | | | 0.5 | V |
| | | LOWPOWER | $I_{OL}$=50µA | | | 0.5 | |
| | LOW Output Voltage XCOUT | HIGHPOWER | With no load applied | | 0 | | V |
| | | LOWPOWER | With no load applied | | 0 | | |
| $V_{T+}$-$V_{T-}$ | Hysteresis | $\overline{HOLD}$, $\overline{RDY}$, TA0IN to TA4IN, $\overline{TB0IN}$ to $\overline{TB5IN}$, $\overline{INT0}$ to $\overline{INT5}$, $\overline{NMI}$, $\overline{ADTRG}$, $\overline{CTS0}$ to $\overline{CTS2}$, CLK0 to CLK4, TA0OUT to TA4OUT, $\overline{KI0}$ to $\overline{KI3}$, RXD0 to RXD2, SCL0 to SCL2, SDA0 to SDA2, SIN3, SIN4 | | 0.2 | | 0.8 | V |
| $V_{T+}$-$V_{T-}$ | Hysteresis | $\overline{RESET}$ | | 0.2 | (0.7) | 1.8 | V |
| $I_{IH}$ | HIGH Input Current (3) | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1, XIN, $\overline{RESET}$, CNVSS, BYTE | $V_I$=3V | | | 4.0 | µA |
| $I_{IL}$ | LOW Input Current (3) | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1, XIN, $\overline{RESET}$, CNVSS, BYTE | $V_I$=0V | | | –4.0 | µA |
| $R_{PULLUP}$ | Pull-Up Resistance (3) | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7,P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1 | $V_I$=0V | 50 | 100 | 500 | kΩ |
| $R_{fXIN}$ | Feedback Resistance XIN | | | | 3.0 | | MΩ |
| $R_{fXCIN}$ | Feedback Resistance XCIN | | | | 25 | | MΩ |
| $V_{RAM}$ | RAM Retention Voltage | | At stop mode | 2.0 | | | V |

NOTES:
1. Referenced to $V_{CC1}$ = $V_{CC2}$ = 2.7 to 3.3V, $V_{SS}$ = 0V at Topr = –20 to 85°C / –40 to 85°C, f(XIN)=10MHz no wait unless otherwise specified.
2. $V_{CC1}$ for the port P6 to P11 and P14, and $V_{CC2}$ for the port P0 to P5 and P12 to P13
3. There is no external connections for port P1_0 to P1_7, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version.

**Table 5.31 Electrical Characteristics (2)** (1)

| Symbol | Parameter | | Measuring Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Typ. | Max. | |
| $I_{CC}$ | Power Supply Current ($V_{CC1}$=$V_{CC2}$=2.7V to 3.6V) | In single-chip mode, the output pins are open and other pins are $V_{SS}$ | Mask ROM | f(BCLK)=10MHz<br>No division | | 8 | 11 | mA |
| | | | | No division,<br>On-chip oscillation | | 1 | | mA |
| | | | Flash Memory | f(BCLK)=10MHz,<br>No division | | 8 | 13 | mA |
| | | | | No division,<br>On-chip oscillation | | 1.8 | | mA |
| | | | Flash Memory Program | f(BCLK)=10MHz,<br>VCC1=3.0V | | 12 | | mA |
| | | | Flash Memory Erase | f(BCLK)=10MHz,<br>VCC1=3.0V | | 22 | | mA |
| | | | Mask ROM | f(XCIN)=32kHz<br>Low power dissipation mode, ROM (3) | | 25 | | µA |
| | | | Flash Memory | f(BCLK)=32kHz<br>Low power dissipation mode, RAM (3) | | 25 | | µA |
| | | | | f(BCLK)=32kHz<br>Low power dissipation mode, Flash Memory (3) | | 420 | | µA |
| | | | | On-chip oscillation,<br>Wait mode | | 45 | | µA |
| | | | Mask ROM<br>Flash Memory | f(BCLK)=32kHz<br>Wait mode (2),<br>Oscillation capability High | | 6.0 | | µA |
| | | | | f(BCLK)=32kHz<br>Wait mode (2),<br>Oscillation capability Low | | 1.8 | | µA |
| | | | | Stop mode<br>Topr =25°C | | 0.7 | 3.0 | µA |
| $I_{det4}$ | Low Voltage Detection Dissipation Current (4) | | | | | 0.6 | 4 | µA |
| $I_{det3}$ | Reset Area Detection Dissipation Current (4) | | | | | 0.4 | 2 | µA |

NOTES:
1. Referenced to $V_{CC1}$=$V_{CC2}$=2.7 to 3.3V, $V_{SS}$ = 0V at $T_{opr}$ = –20 to 85°C / –40 to 85°C, f(BCLK)=10MHz unless otherwise specified.
2. With one timer operated using fC32.
3. This indicates the memory in which the program to be executed exists.
4. $I_{det}$ is dissipation current when the following bit is set to “1” (detection circuit enabled).

   $I_{det4}$: VC27 bit in the VCR2 register

   $I_{det3}$: VC26 bit in the VCR2 register

# $V_{CC1}=V_{CC2}=3V$

**Timing Requirements**
**($V_{CC1}$ = $V_{CC2}$ = 3V, $V_{SS}$ = 0V, at $T_{opr}$ = –20 to 85°C / –40 to 85°C unless otherwise specified)**

**Table 5.32 External Clock Input (XIN input)(1)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_c$ | External Clock Input Cycle Time | (NOTE 2) | | ns |
| $t_{w(H)}$ | External Clock Input HIGH Pulse Width | (NOTE 3) | | ns |
| $t_{w(L)}$ | External Clock Input LOW Pulse Width | (NOTE 3) | | ns |
| $t_r$ | External Clock Rise Time | | (NOTE 4) | ns |
| $t_f$ | External Clock Fall Time | | (NOTE 4) | ns |

NOTES:
1. The condition is $V_{CC1}$=$V_{CC2}$=2.7 to 3.0V.
2. Calculated according to the $V_{CC1}$ voltage as follows:

$$\frac{10^{-6}}{20 \times V_{CC2} - 44} \text{ [ns]}$$

3. Calculated according to the $V_{CC1}$ voltage as follows:

$$\frac{10^{-6}}{20 \times V_{CC1} - 44} \times 0.4 \text{ [ns]}$$

4. Calculated according to the $V_{CC1}$ voltage as follows:

$$-10 \times V_{CC1} + 45 \text{ [ns]}$$

**Table 5.33 Memory Expansion Mode and Microprocessor Mode**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{ac1(RD-DB)}$ | Data Input Access Time (for setting with no wait) | | (NOTE 1) | ns |
| $t_{ac2(RD-DB)}$ | Data Input Access Time (for setting with wait) | | (NOTE 2) | ns |
| $t_{ac3(RD-DB)}$ | Data Input Access Time (when accessing multiplex bus area) | | (NOTE 3) | ns |
| $t_{su(DB-RD)}$ | Data Input Setup Time | 50 | | ns |
| $t_{su(RDY-BCLK)}$ | $\overline{RDY}$ Input Setup Time | 40 | | ns |
| $t_{su(HOLD-BCLK)}$ | $\overline{HOLD}$ Input Setup Time | 50 | | ns |
| $t_{h(RD-DB)}$ | Data Input Hold Time | 0 | | ns |
| $t_{h(BCLK-RDY)}$ | $\overline{RDY}$ Input Hold Time | 0 | | ns |
| $t_{h(BCLK-HOLD)}$ | $\overline{HOLD}$ Input Hold Time | 0 | | ns |

NOTES:
1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 60 \text{[ns]}$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(BCLK)} - 60 \text{[ns]}$$ n is ”2” for 1-wait setting, “3” for 2-wait setting and “4” for 3-wait setting.

3. Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(BCLK)} - 60 \text{[ns]}$$ n is “2” for 2-wait setting, “3” for 3-wait setting.

# $V_{CC1}=V_{CC2}=3V$

**Timing Requirements**
**($V_{CC1}$ = $V_{CC2}$ = 3V, $V_{SS}$ = 0V, at $T_{opr}$ = –20 to 85°C / –40 to 85°C unless otherwise specified)**

**Table 5.34 Timer A Input (Counter Input in Event Counter Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TA)}$ | TAiIN Input Cycle Time | 150 | | ns |
| $t_{w(TAH)}$ | TAiIN Input HIGH Pulse Width | 60 | | ns |
| $t_{w(TAL)}$ | TAiIN Input LOW Pulse Width | 60 | | ns |

**Table 5.35 Timer A Input (Gating Input in Timer Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TA)}$ | TAiIN Input Cycle Time | 600 | | ns |
| $t_{w(TAH)}$ | TAiIN Input HIGH Pulse Width | 300 | | ns |
| $t_{w(TAL)}$ | TAiIN Input LOW Pulse Width | 300 | | ns |

**Table 5.36 Timer A Input (External Trigger Input in One-shot Timer Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TA)}$ | TAiIN Input Cycle Time | 300 | | ns |
| $t_{w(TAH)}$ | TAiIN Input HIGH Pulse Width | 150 | | ns |
| $t_{w(TAL)}$ | TAiIN Input LOW Pulse Width | 150 | | ns |

**Table 5.37 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{w(TAH)}$ | TAiIN Input HIGH Pulse Width | 150 | | ns |
| $t_{w(TAL)}$ | TAiIN Input LOW Pulse Width | 150 | | ns |

**Table 5.38 Timer A Input (Counter Increment/Decrement Input in Event Counter Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(UP)}$ | TAiOUT Input Cycle Time | 3000 | | ns |
| $t_{w(UPH)}$ | TAiOUT Input HIGH Pulse Width | 1500 | | ns |
| $t_{w(UPL)}$ | TAiOUT Input LOW Pulse Width | 1500 | | ns |
| $t_{su(UP-TIN)}$ | TAiOUT Input Setup Time | 600 | | ns |
| $t_{h(TIN-UP)}$ | TAiOUT Input Hold Time | 600 | | ns |

**Table 5.39 Timer A Input (Two-phase Pulse Input in Event Counter Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TA)}$ | TAiIN Input Cycle Time | 2 | | µs |
| $t_{su(TAIN-TAOUT)}$ | TAiOUT Input Setup Time | 500 | | ns |
| $t_{su(TAOUT-TAIN)}$ | TAiIN Input Setup Time | 500 | | ns |

# $V_{CC1}=V_{CC2}=3V$

**Timing Requirements**
**($V_{CC1}$ = $V_{CC2}$ = 3V, $V_{SS}$ = 0V, at $T_{opr}$ = –20 to 85°C / –40 to 85°C unless otherwise specified)**

**Table 5.40 Timer B Input (Counter Input in Event Counter Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TB)}$ | TBiIN Input Cycle Time (counted on one edge) | 150 | | ns |
| $t_{w(TBH)}$ | TBiIN Input HIGH Pulse Width (counted on one edge) | 60 | | ns |
| $t_{w(TBL)}$ | TBiIN Input LOW Pulse Width (counted on one edge) | 60 | | ns |
| $t_{c(TB)}$ | TBiIN Input Cycle Time (counted on both edges) | 300 | | ns |
| $t_{w(TBH)}$ | TBiIN Input HIGH Pulse Width (counted on both edges) | 120 | | ns |
| $t_{w(TBL)}$ | TBiIN Input LOW Pulse Width (counted on both edges) | 120 | | ns |

**Table 5.41 Timer B Input (Pulse Period Measurement Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TB)}$ | TBiIN Input Cycle Time | 600 | | ns |
| $t_{w(TBH)}$ | TBiIN Input HIGH Pulse Width | 300 | | ns |
| $t_{w(TBL)}$ | TBiIN Input LOW Pulse Width | 300 | | ns |

**Table 5.42 Timer B Input (Pulse Width Measurement Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TB)}$ | TBiIN Input Cycle Time | 600 | | ns |
| $t_{w(TBH)}$ | TBiIN Input HIGH Pulse Width | 300 | | ns |
| $t_{w(TBL)}$ | TBiIN Input LOW Pulse Width | 300 | | ns |

**Table 5.43 A/D Trigger Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(AD)}$ | $\overline{\text{ADTRG}}$ Input Cycle Time | 1500 | | ns |
| $t_{w(ADL)}$ | $\overline{\text{ADTRG}}$ Input LOW Pulse Width | 200 | | ns |

**Table 5.44 Serial Interface**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(CK)}$ | CLKi Input Cycle Time | 300 | | ns |
| $t_{w(CKH)}$ | CLKi Input HIGH Pulse Width | 150 | | ns |
| $t_{w(CKL)}$ | CLKi Input LOW Pulse Width | 150 | | ns |
| $t_{d(C-Q)}$ | TXDi Output Delay Time | | 160 | ns |
| $t_{h(C-Q)}$ | TXDi Hold Time | 0 | | ns |
| $t_{su(D-C)}$ | RXDi Input Setup Time | 100 | | ns |
| $t_{h(C-D)}$ | RXDi Input Hold Time | 90 | | ns |

**Table 5.45 External Interrupt $\overline{\text{INTi}}$ Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{w(INH)}$ | $\overline{\text{INTi}}$ Input HIGH Pulse Width | 380 | | ns |
| $t_{w(INL)}$ | $\overline{\text{INTi}}$ Input LOW Pulse Width | 380 | | ns |

# $V_{CC1}=V_{CC2}=3V$

## Switching Characteristics

**($V_{CC1}$ = $V_{CC2}$ = 3V, $V_{SS}$ = 0V, at $T_{opr}$ = –20 to 85°C / –40 to 85°C unless otherwise specified)**

**Table 5.46 Memory Expansion and Microprocessor Modes (for setting with no wait)**

| Symbol | Parameter | | Standard | | Unit |
|---|---|---|---|---|---|
| | | | Min. | Max. | |
| td(BCLK-AD) | Address Output Delay Time | See **Figure 5.12** | | 30 | ns |
| th(BCLK-AD) | Address Output Hold Time (in relation to BCLK) | | 4 | | ns |
| th(RD-AD) | Address Output Hold Time (in relation to RD) | | 0 | | ns |
| th(WR-AD) | Address Output Hold Time (in relation to WR) | | (NOTE 2) | | ns |
| td(BCLK-CS) | Chip Select Output Delay Time | | | 30 | ns |
| th(BCLK-CS) | Chip Select Output Hold Time (in relation to BCLK) | | 4 | | ns |
| td(BCLK-ALE) | ALE Signal Output Delay Time | | | 25 | ns |
| th(BCLK-ALE) | ALE Signal Output Hold Time | | –4 | | ns |
| td(BCLK-RD) | RD Signal Output Delay Time | | | 30 | ns |
| th(BCLK-RD) | RD Signal Output Hold Time | | 0 | | ns |
| td(BCLK-WR) | WR Signal Output Delay Time | | | 30 | ns |
| th(BCLK-WR) | WR Signal Output Hold Time | | 0 | | ns |
| td(BCLK-DB) | Data Output Delay Time (in relation to BCLK) | | | 40 | ns |
| th(BCLK-DB) | Data Output Hold Time (in relation to BCLK) (3) | | 4 | | ns |
| td(DB-WR) | Data Output Delay Time (in relation to WR) | | (NOTE 1) | | ns |
| th(WR-DB) | Data Output Hold Time (in relation to WR) (3) | | (NOTE 2) | | ns |
| td(BCLK-HLDA) | HLDA Output Delay Time | | | 40 | ns |

NOTES:

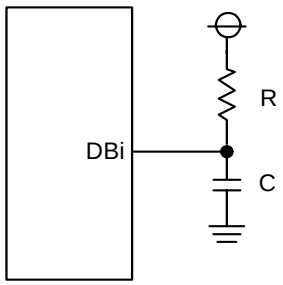
1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5\times10^{9}}{f(BCLK)} - 40[ns]$$ f(BCLK) is 12.5MHz or less.

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5\times10^{9}}{f(BCLK)} - 10[ns]$$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
   Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
   Hold time of data bus is expressed in
   $t = -CR \times \ln(1 - V_{OL} / V_{CC2})$
   by a circuit of the right figure.
   For example, when $V_{OL} = 0.2V_{CC2}$, C = 30pF, R = 1kΩ, hold time of output "L" level is
   $t = -30pF \times 1k\Omega \times \ln(1 - 0.2V_{CC2} / V_{CC2})$
   = 6.7ns.



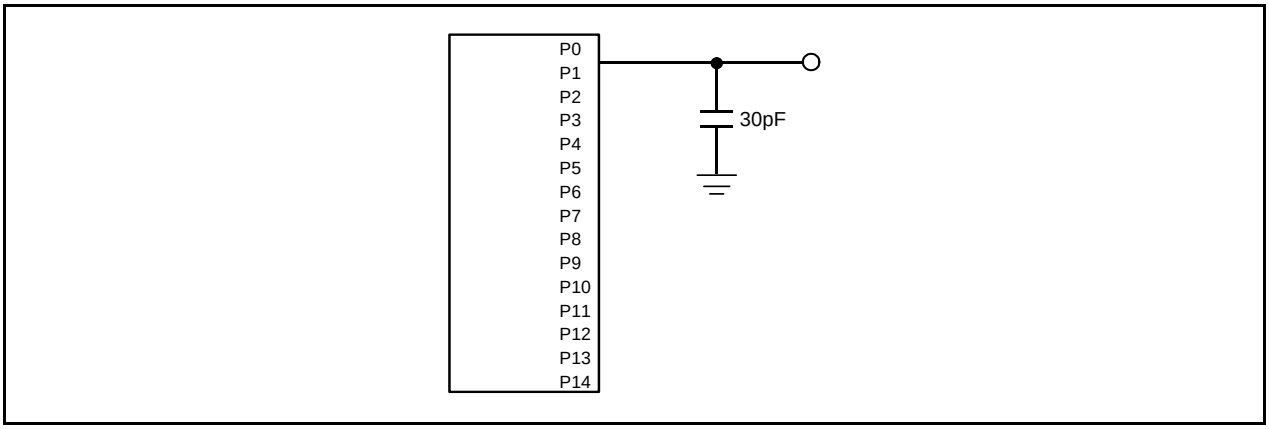




**Figure 5.12 Ports P0 to P14 Measurement Circuit**

# $V_{CC1}=V_{CC2}=3V$

## Switching Characteristics

**($V_{CC1}$ = $V_{CC2}$ = 5V, $V_{SS}$ = 0V, at $T_{opr}$ = –20 to 85°C / –40 to 85°C unless otherwise specified)**

**Table 5.47 Memory Expansion and Microprocessor Modes (for 1- to 3-wait setting and external area access)**

| Symbol | Parameter | | Standard | | Unit |
|---|---|---|---|---|---|
| | | | Min. | Max. | |
| $t_{d(BCLK-AD)}$ | Address Output Delay Time | See **Figure 5.12** | | 30 | ns |
| $t_{h(BCLK-AD)}$ | Address Output Hold Time (in relation to BCLK) | | 4 | | ns |
| $t_{h(RD-AD)}$ | Address Output Hold Time (in relation to RD) | | 0 | | ns |
| $t_{h(WR-AD)}$ | Address Output Hold Time (in relation to WR) | | (NOTE 2) | | ns |
| $t_{d(BCLK-CS)}$ | Chip Select Output Delay Time | | | 30 | ns |
| $t_{h(BCLK-CS)}$ | Chip Select Output Hold Time (in relation to BCLK) | | 4 | | ns |
| $t_{d(BCLK-ALE)}$ | ALE Signal Output Delay Time | | | 25 | ns |
| $t_{h(BCLK-ALE)}$ | ALE Signal Output Hold Time | | -4 | | ns |
| $t_{d(BCLK-RD)}$ | RD Signal Output Delay Time | | | 30 | ns |
| $t_{h(BCLK-RD)}$ | RD Signal Output Hold Time | | 0 | | ns |
| $t_{d(BCLK-WR)}$ | WR Signal Output Delay Time | | | 30 | ns |
| $t_{h(BCLK-WR)}$ | WR Signal Output Hold Time | | 0 | | ns |
| $t_{d(BCLK-DB)}$ | Data Output Delay Time (in relation to BCLK) | | | 40 | ns |
| $t_{h(BCLK-DB)}$ | Data Output Hold Time (in relation to BCLK) (3) | | 4 | | ns |
| $t_{d(DB-WR)}$ | Data Output Delay Time (in relation to WR) | | (NOTE 1) | | ns |
| th(WR-DB) | Data Output Hold Time (in relation to WR)(3) | | (NOTE 2) | | ns |
| $t_{d(BCLK-HLDA)}$ | HLDA Output Delay Time | | | 40 | ns |

NOTES:

1. Calculated according to the BCLK frequency as follows:

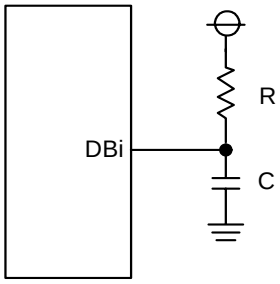
$$\frac{(n-0.5)\times 10^9}{f(BCLK)} - 40[ns]$$

n is “1” for 1-wait setting, “2” for 2-wait setting and “3” for 3-wait setting.
(BCLK) is 12.5MHz or less.

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5\times 10^9}{f(BCLK)} - 10[ns]$$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
Hold time of data bus is expressed in
$t = -CR \times \ln(1 - V_{OL} / V_{CC2})$
by a circuit of the right figure.
For example, when $V_{OL}$ = 0.2$V_{CC2}$, C = 30pF, R = 1kΩ, hold time of output ”L” level is
$t = -30pF \times 1k\Omega \times \ln(1 - 0.2V_{CC2} / V_{CC2})$
= 6.7ns.



# $V_{CC1}=V_{CC2}=3V$

**Switching Characteristics**
**($V_{CC1}$ = $V_{CC2}$ = 5V, $V_{SS}$ = 0V, at $T_{opr}$ = –20 to 85°C / –40 to 85°C unless otherwise specified)**

**Table 5.48 Memory Expansion and Microprocessor Modes (for 2- to 3-wait setting, external area access and multiplex bus selection)**

| Symbol | Parameter | | Standard | | Unit |
|---|---|---|---|---|---|
| | | | Min. | Max. | |
| $t_{d(BCLK-AD)}$ | Address Output Delay Time | See **Figure 5.12** | | 50 | ns |
| $t_{h(BCLK-AD)}$ | Address Output Hold Time (in relation to BCLK) | | 4 | | ns |
| $t_{h(RD-AD)}$ | Address Output Hold Time (in relation to RD) | | (NOTE 1) | | ns |
| $t_{h(WR-AD)}$ | Address Output Hold Time (in relation to WR) | | (NOTE 1) | | ns |
| $t_{d(BCLK-CS)}$ | Chip Select Output Delay Time | | | 50 | ns |
| $t_{h(BCLK-CS)}$ | Chip Select Output Hold Time (in relation to BCLK) | | 4 | | ns |
| $t_{h(RD-CS)}$ | Chip Select Output Hold Time (in relation to RD) | | (NOTE 1) | | ns |
| $t_{h(WR-CS)}$ | Chip Select Output Hold Time (in relation to WR) | | (NOTE 1) | | ns |
| $t_{d(BCLK-RD)}$ | RD Signal Output Delay Time | | | 40 | ns |
| $t_{h(BCLK-RD)}$ | RD Signal Output Hold Time | | 0 | | ns |
| $t_{d(BCLK-WR)}$ | WR Signal Output Delay Time | | | 40 | ns |
| $t_{h(BCLK-WR)}$ | WR Signal Output Hold Time | | 0 | | ns |
| $t_{d(BCLK-DB)}$ | Data Output Delay Time (in relation to BCLK) | | | 50 | ns |
| $t_{h(BCLK-DB)}$ | Data Output Hold Time (in relation to BCLK) | | 4 | | ns |
| $t_{d(DB-WR)}$ | Data Output Delay Time (in relation to WR) | | (NOTE 2) | | ns |
| $t_{h(WR-DB)}$ | Data Output Hold Time (in relation to WR) | | (NOTE 1) | | ns |
| $t_{d(BCLK-HLDA)}$ | HLDA Output Delay Time | | | 40 | ns |
| $t_{d(BCLK-ALE)}$ | ALE Signal Output Delay Time (in relation to BCLK) | | | 25 | ns |
| $t_{h(BCLK-ALE)}$ | ALE Signal Output Hold Time (in relation to BCLK) | | –4 | | ns |
| $t_{d(AD-ALE)}$ | ALE Signal Output Delay Time (in relation to Address) | | (NOTE 3) | | ns |
| $t_{h(AD-ALE)}$ | ALE Signal Output Hold Time (in relation to Address) | | (NOTE 4) | | ns |
| $t_{d(AD-RD)}$ | RD Signal Output Delay From the End of Address | | 0 | | ns |
| $t_{d(AD-WR)}$ | WR Signal Output Delay From the End of Address | | 0 | | ns |
| $t_{dz(RD-AD)}$ | Address Output Floating Start Time | | | 8 | ns |

NOTES:
1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 10[ns]$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 50[ns]$$ n is “2” for 2-wait setting, “3” for 3-wait setting.

3. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 40[ns]$$

4. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 15[ns]$$

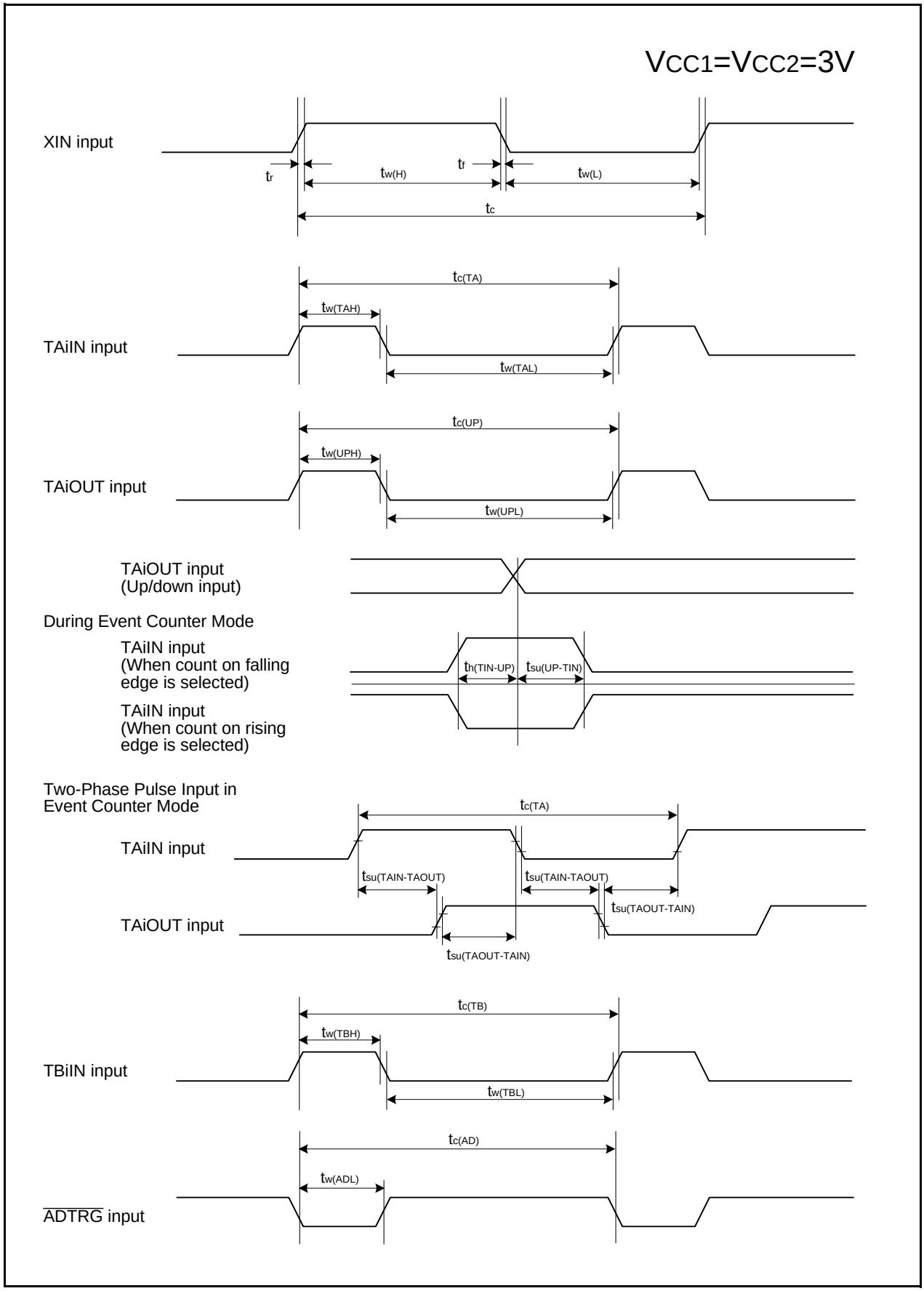



**Figure 5.13 Timing Diagram (1)**

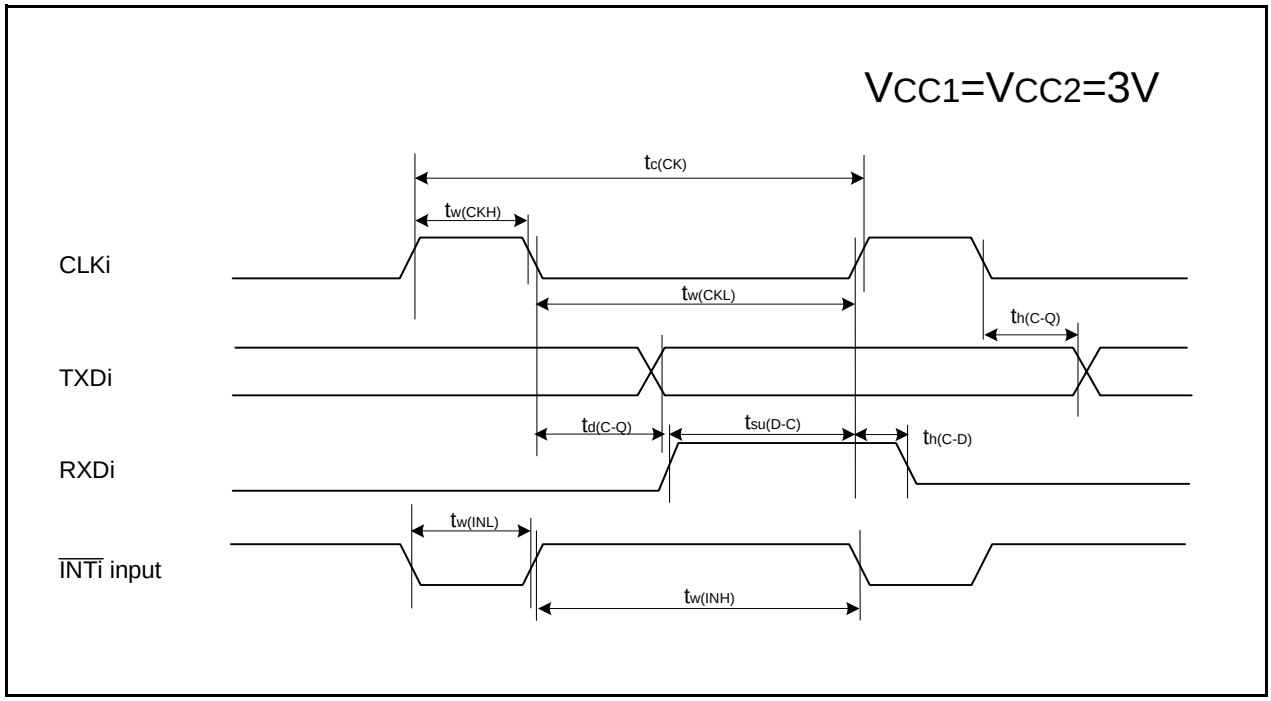
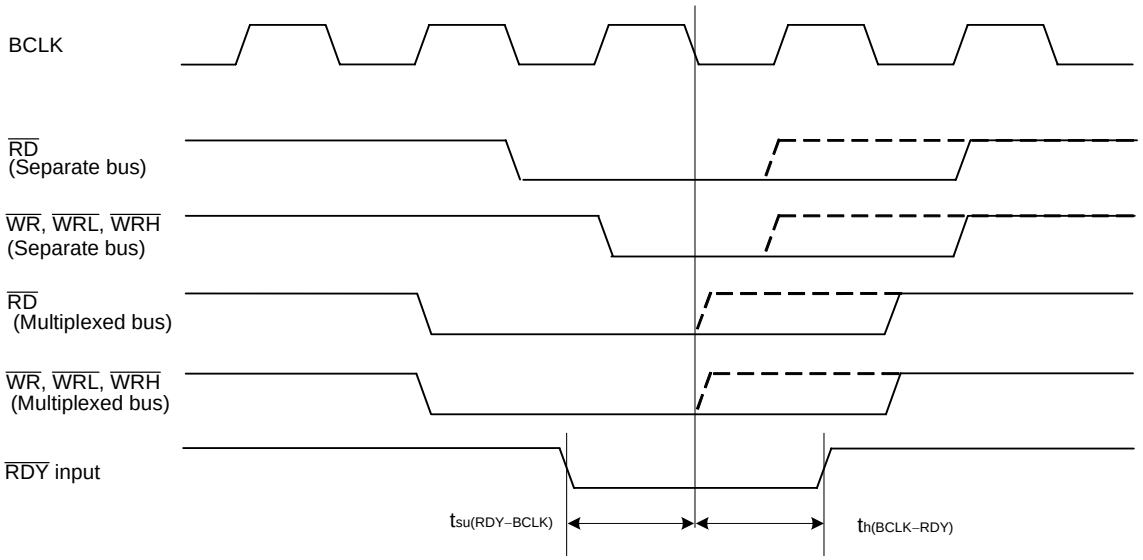



**Figure 5.14 Timing Diagram (2)**

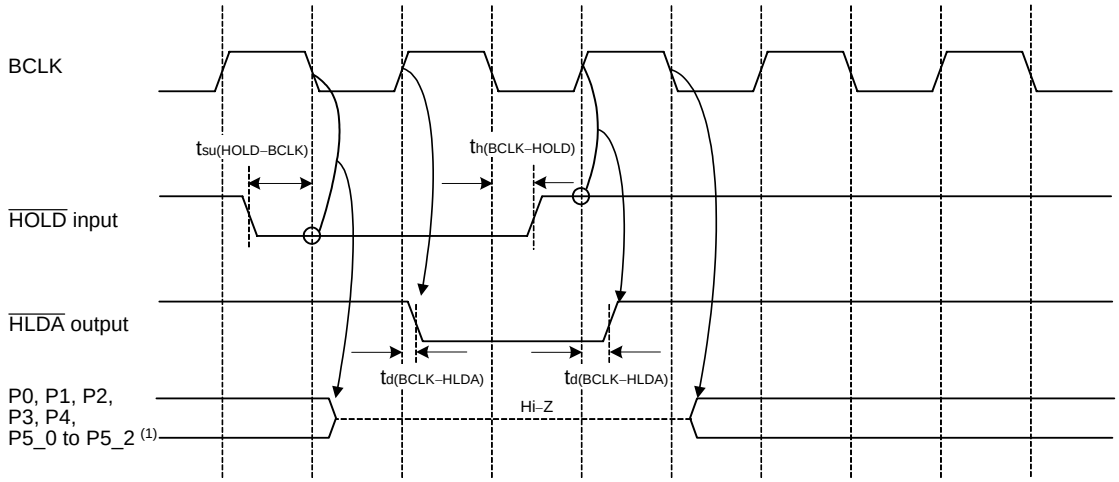
**Memory Expansion Mode, Microprocessor Mode**

$V_{CC1}=V_{CC2}=3V$

(Effective for setting with wait)




(Common to setting with wait and setting without wait)




NOTES:
1. These pins are set to high-impedance regardless of the input level of the BYTE pin, PM06 bit in PM0 register and PM11 bit in PM1 register.

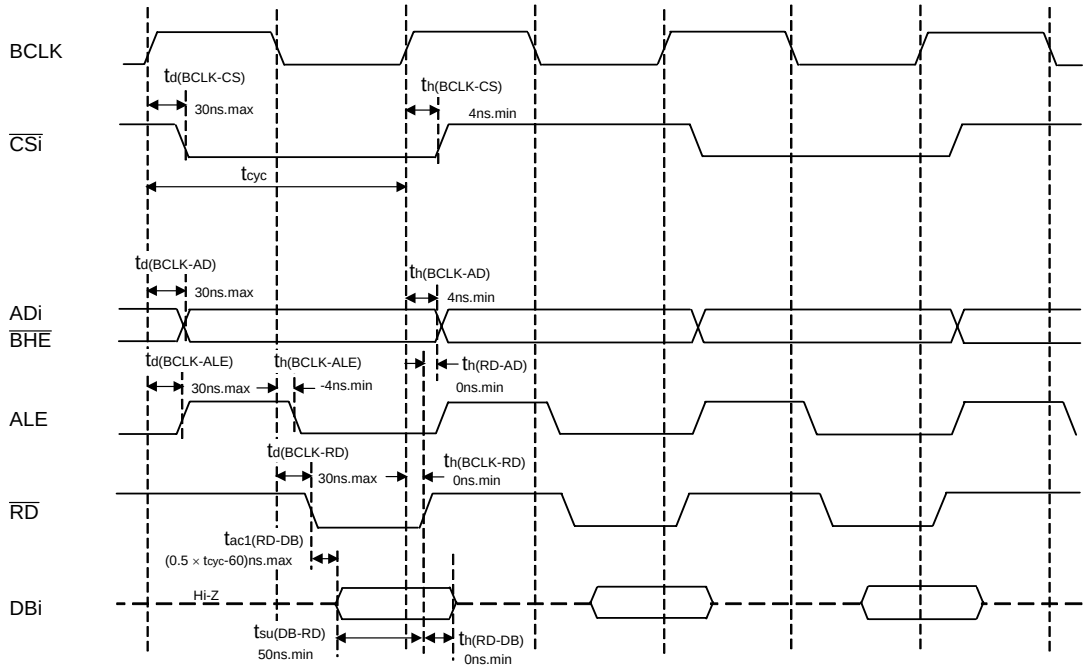
Measuring conditions :
· $V_{CC1}=V_{CC2}=3V$
· Input timing voltage : Determined with $V_{IL}=0.6V$, $V_{IH}=2.4V$
· Output timing voltage : Determined with $V_{OL}=1.5V$, $V_{OH}=1.5V$

**Figure 5.15 Timing Diagram (3)**

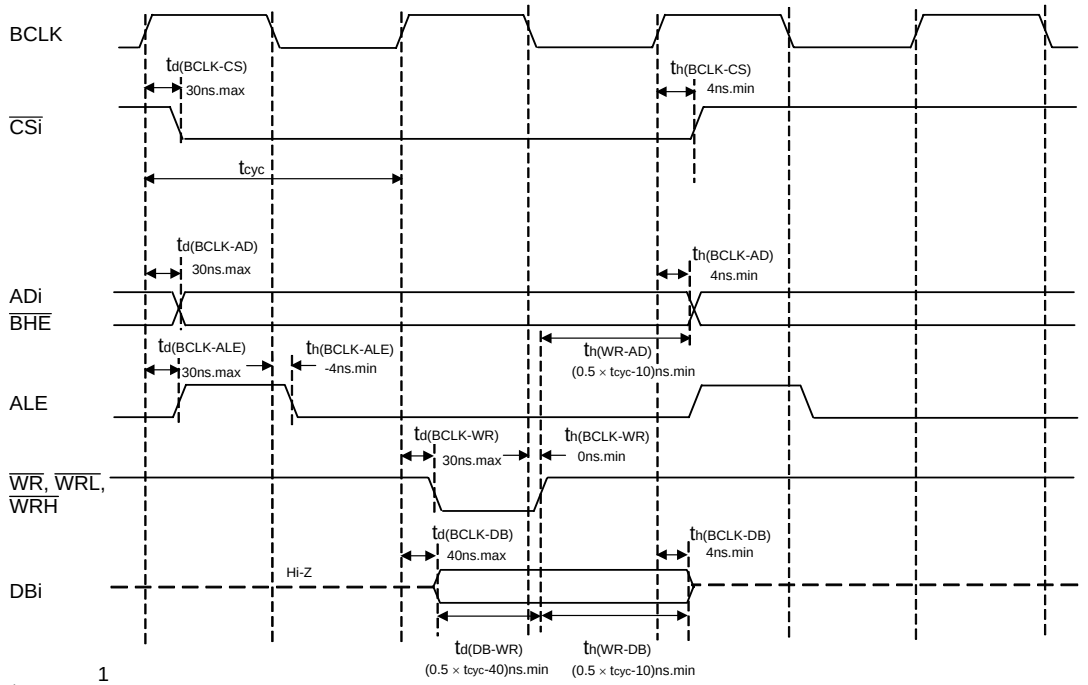
**Memory Expansion Mode, Microprocessor Mode**
**(**for setting with no wait**)**

$V_{CC1}=V_{CC2}=3V$

**Read timing**




**Write timing**




$$t_{cyc}=\frac{1}{f(BCLK)}$$

Measuring conditions
· $V_{CC1}=V_{CC2}=3V$
· Input timing voltage : $V_{IL}=0.6V$, $V_{IH}=2.4V$
· Output timing voltage : $V_{OL}=1.5V$, $V_{OH}=1.5V$

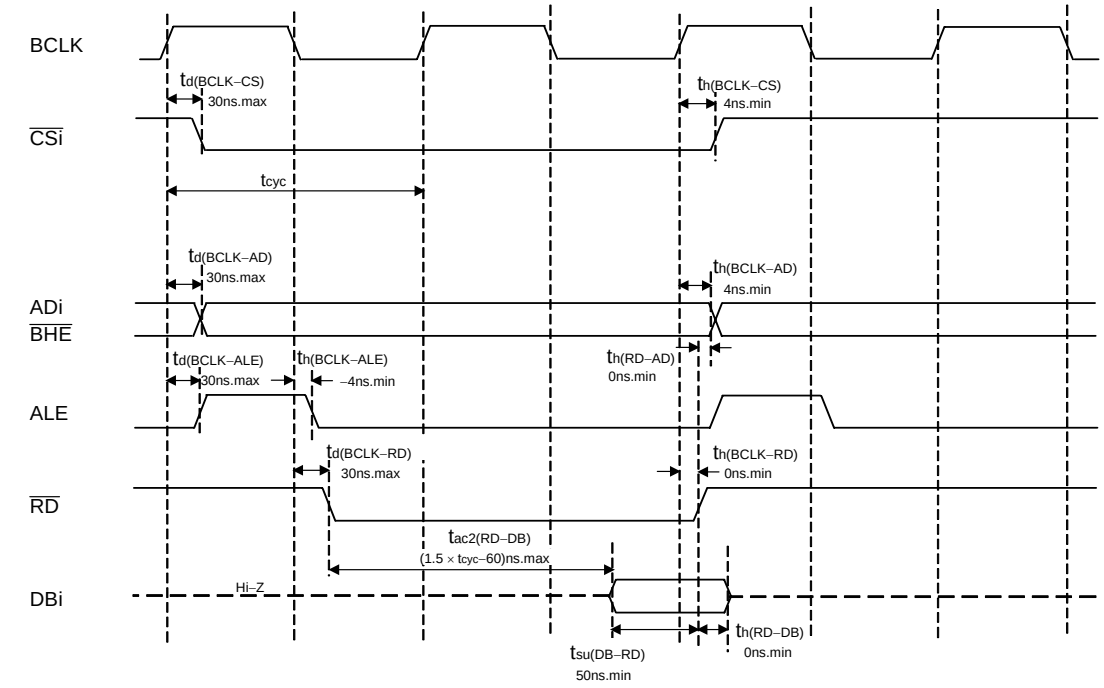
**Figure 5.16 Timing Diagram (4)**

## Memory Expansion Mode, Microprocessor Mode

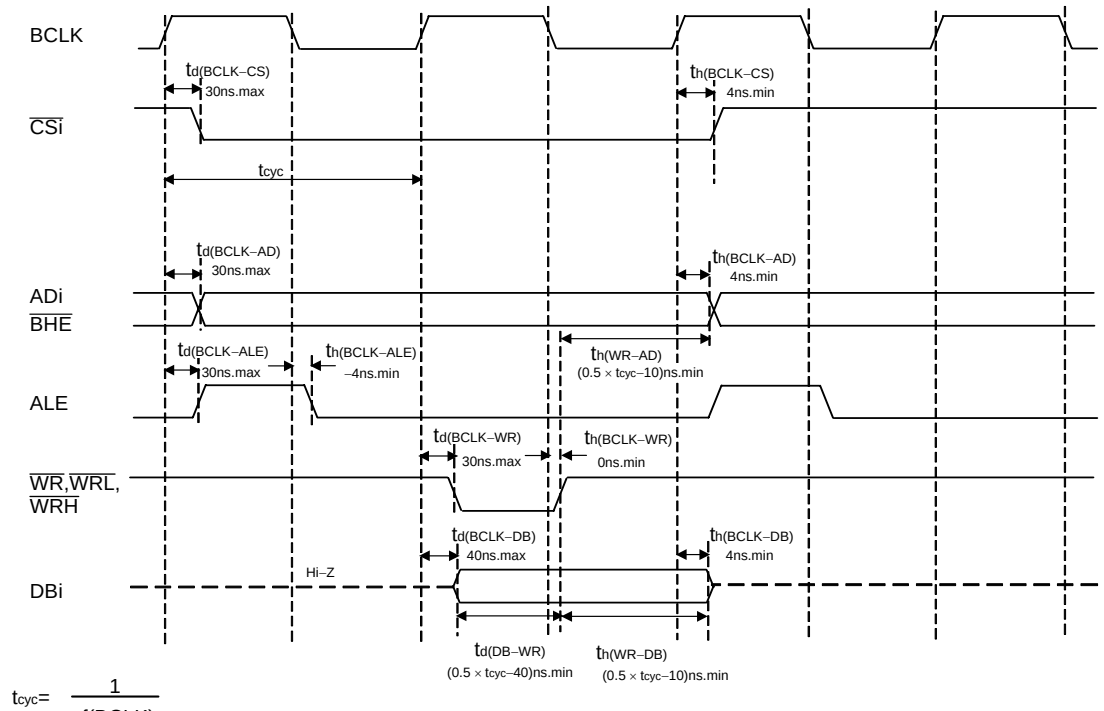
**(**for 1-wait setting and external area access**)**

$V_{CC1}=V_{CC2}=3V$

**Read timing**




**Write timing**




$$t_{cyc}=\frac{1}{f(BCLK)}$$

Measuring conditions

· $V_{CC1}=V_{CC2}=3V$

· Input timing voltage : $V_{IL}=0.6V$, $V_{IH}=2.4V$

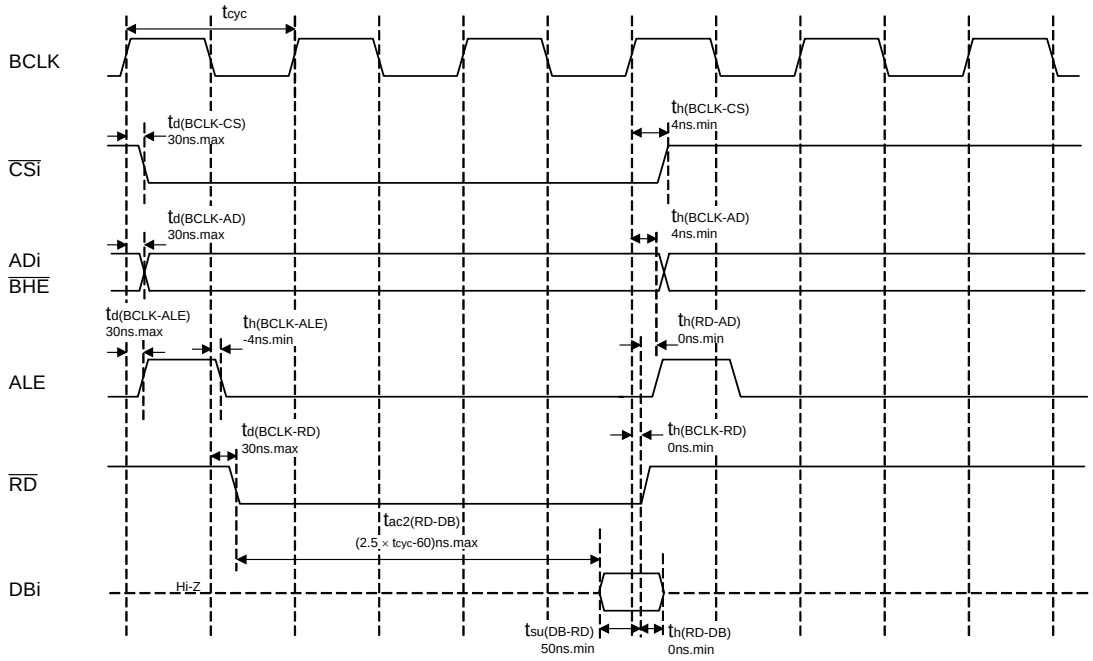
· Output timing voltage : $V_{OL}=1.5V$, $V_{OH}=1.5V$

**Figure 5.17 Timing Diagram (5)**

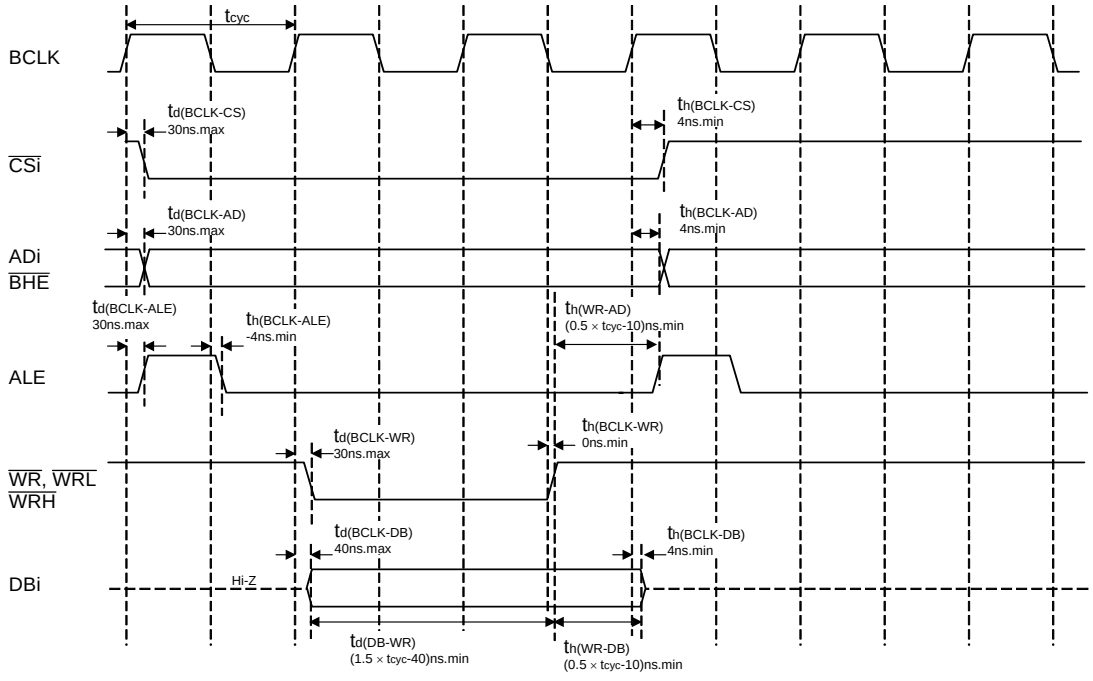
$V_{CC1}=V_{CC2}=3V$

**Memory Expansion Mode, Microprocessor Mode**
**(**for 2-wait setting and external area access**)**

**Read timing**




**Write timing**




$$t_{cyc}=\frac{1}{f(BCLK)}$$

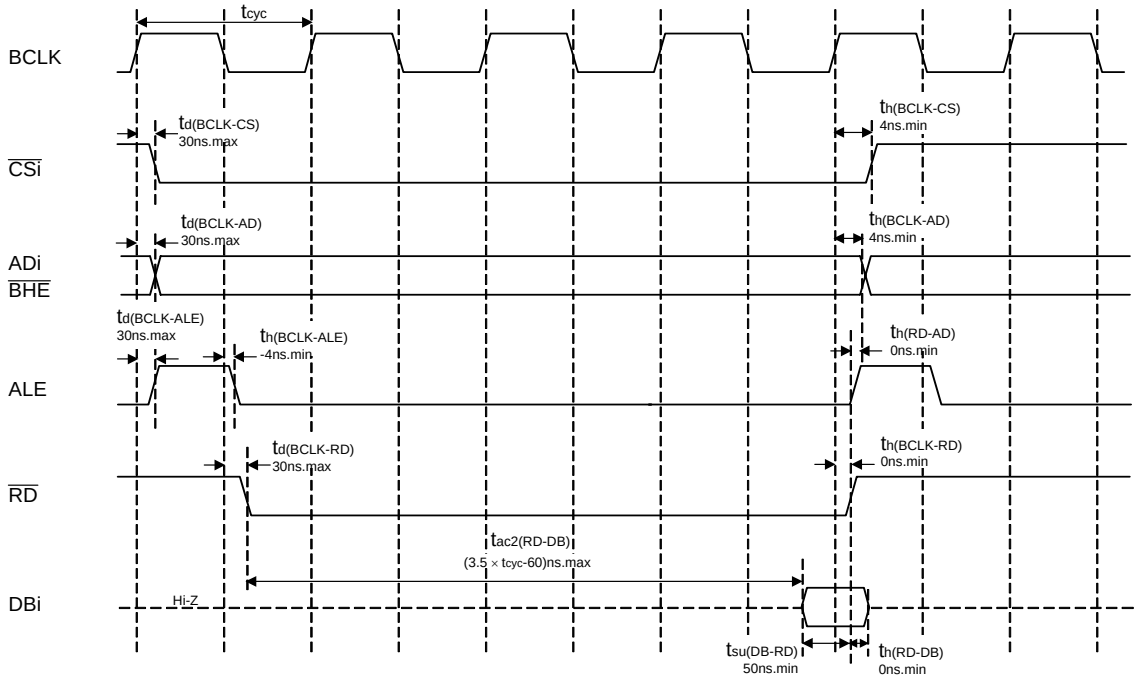
Measuring conditions
· $V_{CC1}=V_{CC2}=3V$
· Input timing voltage : $V_{IL}=0.6V$, $V_{IH}=2.4V$
· Output timing voltage : $V_{OL}=1.5V$, $V_{OH}=1.5V$

**Figure 5.18 Timing Diagram (6)**

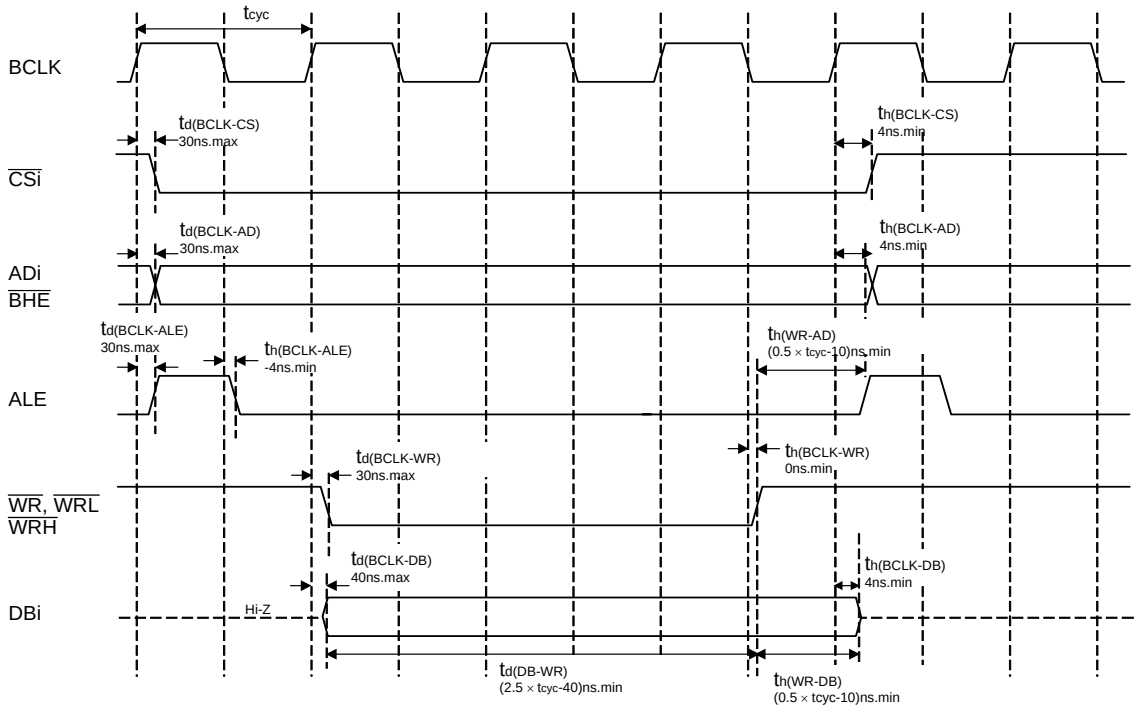
$V_{CC1} = V_{CC2} = 3V$

**Memory Expansion Mode, Microprocessor Mode**
**(**for 3-wait setting and external area access**)**

**Read timing**




**Write timing**




$$t_{cyc} = \frac{1}{f(BCLK)}$$

Measuring conditions
· $V_{CC1}$=$V_{CC2}$=3V
· Input timing voltage : $V_{IL}$=0.6V, $V_{IH}$=2.4V
· Output timing voltage : $V_{OL}$=1.5V, $V_{OH}$=1.5V

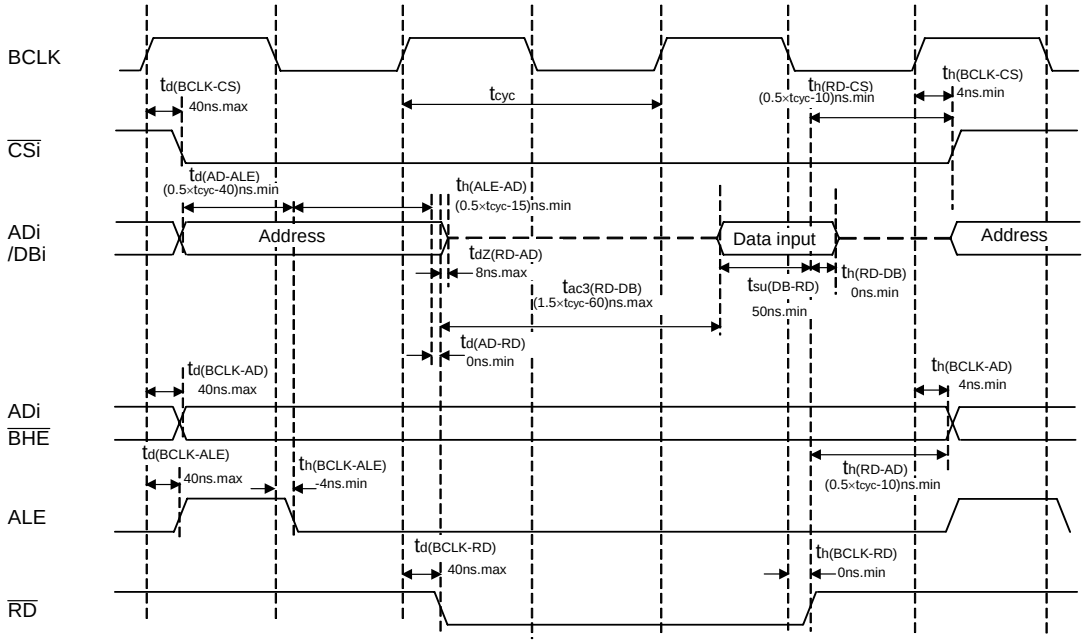
**Figure 5.19 Timing Diagram (7)**

## Memory Expansion Mode, Microprocessor Mode

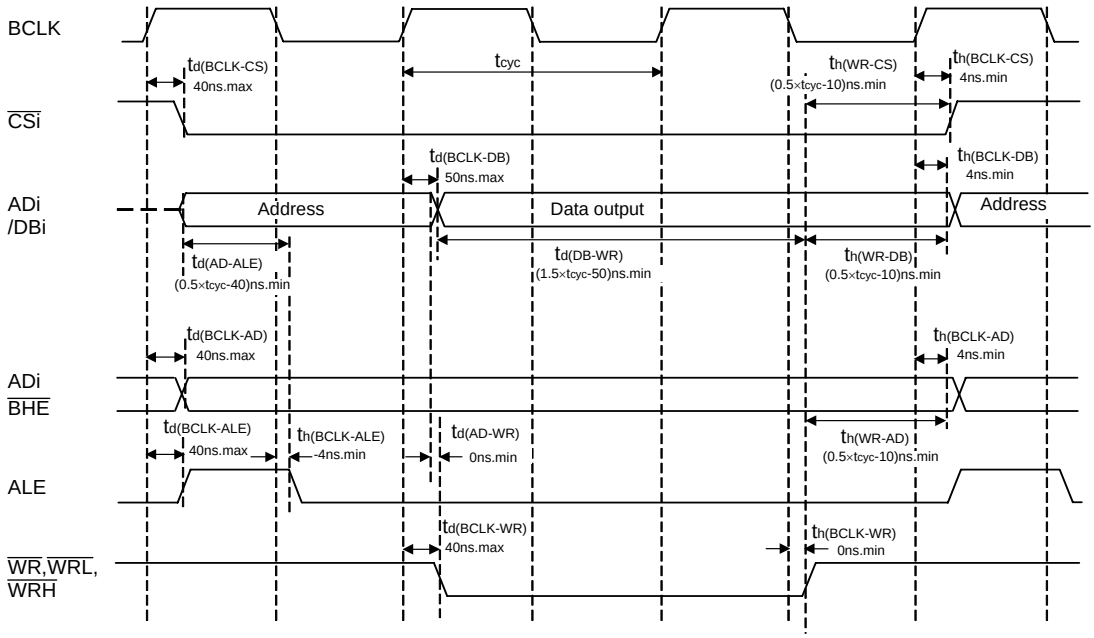
$V_{CC1}=V_{CC2}=3V$

**(**For 2-wait setting, external area access and multiplex bus selection**)**

**Read timing**




**Write timing**




$$t_{cyc}=\frac{1}{f(BCLK)}$$

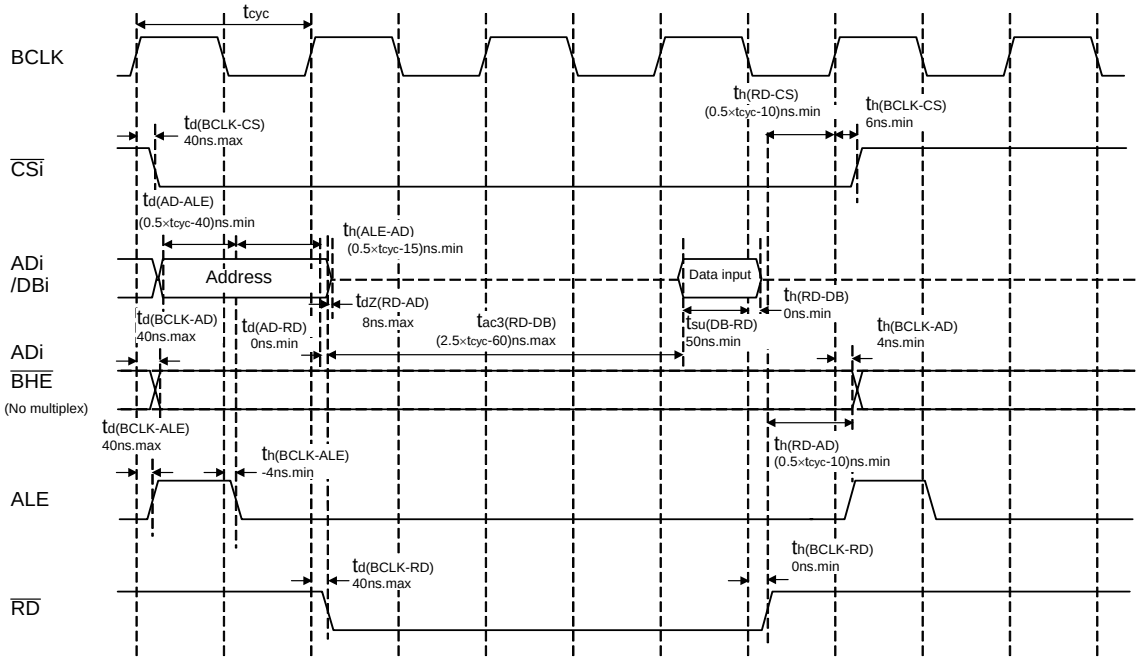
Measuring conditions
- $V_{CC1}=V_{CC2}=3V$
- Input timing voltage : $V_{IL}=0.6V$, $V_{IH}=2.4V$
- Output timing voltage : $V_{OL}=1.5V$, $V_{OH}=1.5V$

**Figure 5.20 Timing Diagram (8)**

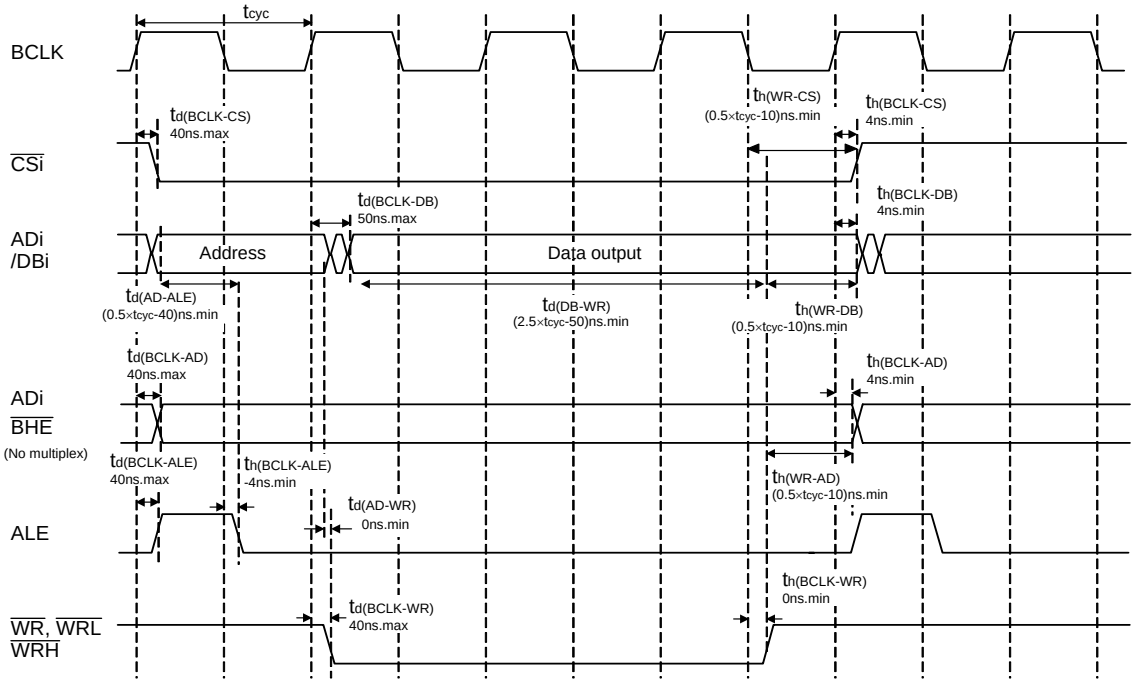
$V_{CC1}=V_{CC2}=3V$

**Memory Expansion Mode, Microprocessor Mode**
(For 3-wait setting, external area access and multiplex bus selection)

**Read timing**




**Write timing**




$$t_{cyc}=\frac{1}{f(BCLK)}$$

Measuring conditions
- $V_{CC1}=V_{CC2}=3V$
- Input timing voltage : $V_{IL}=0.6V$, $V_{IH}=2.4V$
- Output timing voltage : $V_{OL}=1.5V$, $V_{OH}=1.5V$

**Figure 5.21 Timing Diagram (9)**

## 5.2 Electrical Characteristics (M16C/62PT)

**Table 5.49 Absolute Maximum Ratings**

| Symbol | Parameter | | Condition | Rated Value | Unit |
|---|---|---|---|---|---|
| $V_{CC1}$, $V_{CC2}$ | Supply Voltage | | $V_{CC1}$=$V_{CC2}$=AVcc | –0.3 to 6.5 | V |
| AVcc | Analog Supply Voltage | | $V_{CC1}$=$V_{CC2}$=AVcc | –0.3 to 6.5 | V |
| $V_I$ | Input Voltage | $\overline{\text{RESET}}$, CNVSS, BYTE, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, VREF, XIN | | –0.3 to $V_{CC1}$+0.3 (1) | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7 | | –0.3 to $V_{CC2}$+0.3 (1) | V |
| | | P7_0, P7_1 | | –0.3 to 6.5 | V |
| $V_O$ | Output Voltage | P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, XOUT | | –0.3 to $V_{CC1}$+0.3 (1) | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7 | | –0.3 to $V_{CC2}$+0.3 (1) | V |
| | | P7_0, P7_1 | | –0.3 to 6.5 | V |
| $P_d$ | Power Dissipation | | –40°C<$T_{opr}$≤85°C | 300 | mW |
| | | | 85°C<$T_{opr}$≤125°C | 200 | |
| $T_{opr}$ | Operating Ambient Temperature | When the Microcomputer is Operating | | –40 to 85 / –40 to 125 (2) | °C |
| | | Flash Program Erase | | 0 to 60 | |
| $T_{stg}$ | Storage Temperature | | | –65 to 150 | °C |

NOTES:
1. There is no external connections for port P1_0 to P1_7, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version.
2. T version = –40 to 85 °C, V version= –40 to 125 °C.

**Table 5.50 Recommended Operating Conditions (1)** (1)

| Symbol | Parameter | | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{CC1}$, $V_{CC2}$ | Supply Voltage ($V_{CC1}$ = $V_{CC2}$) | | 4.0 | 5.0 | 5.5 | V |
| AVcc | Analog Supply Voltage | | | $V_{CC1}$ | | V |
| Vss | Supply Voltage | | | 0 | | V |
| AVss | Analog Supply Voltage | | | 0 | | V |
| $V_{IH}$ | HIGH Input Voltage (4) | P3_1 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7 | 0.8$V_{CC2}$ | | $V_{CC2}$ | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (during single-chip mode) | 0.8$V_{CC2}$ | | $V_{CC2}$ | V |
| | | P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, XIN, RESET, CNVSS, BYTE | 0.8$V_{CC1}$ | | $V_{CC1}$ | V |
| | | P7_0, P7_1 | 0.8$V_{CC1}$ | | 6.5 | V |
| $V_{IL}$ | LOW Input Voltage (4) | P3_1 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7 | 0 | | 0.2$V_{CC2}$ | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (during single-chip mode) | 0 | | 0.2$V_{CC2}$ | V |
| | | P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, XIN, RESET, CNVSS, BYTE | 0 | | 0.2Vcc | V |
| $I_{OH(peak)}$ | HIGH Peak Output Current (4) | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1 | | | –10.0 | mA |
| $I_{OH(avg)}$ | HIGH Average Output Current (4) | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1 | | | –5.0 | mA |
| $I_{OL(peak)}$ | LOW Peak Output Current (4) | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1 | | | 10.0 | mA |
| $I_{OL(avg)}$ | LOW Average Output Current (4) | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1 | | | 5.0 | mA |
| f(XIN) | Main Clock Input Oscillation Frequency | $V_{CC1}$=4.0V to 5.5V | 0 | | 16 | MHz |
| f(XCIN) | Sub-Clock Oscillation Frequency | | | 32.768 | 50 | kHz |
| f(Ring) | On-chip Oscillation Frequency | | 0.5 | 1 | 2 | MHz |
| f(PLL) | PLL Clock Oscillation Frequency | $V_{CC1}$=4.0V to 5.5V | 10 | | 24 | MHz |
| f(BCLK) | CPU Operation Clock | | 0 | | 24 | MHz |
| $t_{SU}$(PLL) | PLL Frequency Synthesizer Stabilization Wait Time | $V_{CC1}$=5.5V | | | 20 | ms |

NOTES:

1. Referenced to $V_{CC1}$ = $V_{CC2}$ = 4.7 to 5.5V at $T_{opr}$ = –40 to 85°C / –40 to 125°C unless otherwise specified.
   T version = –40 to 85 °C, V version= –40 to 125 °C.
2. The Average Output Current is the mean value within 100ms.
3. The total $I_{OL(peak)}$ for ports P0, P1, P2, P8_6, P8_7, P9, P10 P1, P14_0 and P14_1 must be 80mA max. The total $I_{OL(peak)}$ for ports P3, P4, P5, P6, P7, P8_0 to P8_4, P12, and P13 must be 80mA max. The total $I_{OH(peak)}$ for ports P0, P1, and P2 must be –40mA max. The total $I_{OH(peak)}$ for ports P3, P4, P5, P12, and P13 must be –40mA max. The total $I_{OH(peak)}$ for ports P6, P7, and P8_0 to P8_4 must be –40mA max. The total $I_{OH(peak)}$ for ports P8_6, P8_7, P9 , P10, P11, P14_0, and P14_1 must be –40mA max.
   As for 80-pin version, the total $I_{OL(peak)}$ for all ports and $I_{OH(peak)}$ must be 80mA. max. due to one $V_{CC}$ and one $V_{SS}$.
4. There is no external connections for port P1_0 to P1_7, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version.

**Table 5.51 A/D Conversion Characteristics** (1)

| Symbol | Parameter | | Measuring Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Typ. | Max. | |
| – | Resolution | | $V_{REF}=V_{CC1}$ | | | | 10 | Bits |
| INL | Integral Non-Linearity Error | 10bit | $V_{REF}=V_{CC1}=5V$ | AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input | | | ±3 | LSB |
| | | | | External operation amp connection mode | | | ±7 | LSB |
| | | 8bit | $V_{REF}=V_{CC1}=5V$ | | | | ±2 | LSB |
| – | Absolute Accuracy | 10bit | $V_{REF}=V_{CC1}=5V$ | AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input | | | ±3 | LSB |
| | | | | External operation amp connection mode | | | ±7 | LSB |
| | | 8bit | $V_{REF}=V_{CC1}=5V$ | | | | ±2 | LSB |
| – | Tolerance Level Impedance | | | | | 3 | | kΩ |
| DNL | Differential Non-Linearity Error | | | | | | ±1 | LSB |
| – | Offset Error | | | | | | ±3 | LSB |
| – | Gain Error | | | | | | ±3 | LSB |
| $R_{LADDER}$ | Ladder Resistance | | $V_{REF}=V_{CC1}$ | | 10 | | 40 | kΩ |
| $t_{CONV}$ | 10-bit Conversion Time, Sample & Hold Function Available | | $V_{REF}=V_{CC1}=5V$, ϕAD=12MHz | | 2.75 | | | µs |
| $t_{CONV}$ | 8-bit Conversion Time, Sample & Hold Function Available | | $V_{REF}=V_{CC1}=5V$, ϕAD=12MHz | | 2.33 | | | µs |
| $t_{SAMP}$ | Sampling Time | | | | 0.25 | | | µs |
| $V_{REF}$ | Reference Voltage | | | | 2.0 | | $V_{CC1}$ | V |
| $V_{IA}$ | Analog Input Voltage | | | | 0 | | $V_{REF}$ | V |

NOTES:
1. Referenced to $V_{CC1}=AV_{CC}=V_{REF}=4.0$ to 5.5V, $V_{SS}=AV_{SS}=0V$ at $T_{opr}$ = –40 to 85°C / –40 to 125°C unless otherwise specified. T version = –40 to 85°C, V version =–40 to 125°C
2. ϕAD frequency must be 12 MHz or less.
3. When sample & hold is disabled, ϕAD frequency must be 250 kHz or more, in addition to the limitation in Note 2. When sample & hold is enabled, ϕAD frequency must be 1MHz or more, in addition to the limitation in Note 2.

**Table 5.52 D/A Conversion Characteristics** (1)

| Symbol | Parameter | Measuring Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| – | Resolution | | | | 8 | Bits |
| – | Absolute Accuracy | | | | 1.0 | % |
| $t_{SU}$ | Setup Time | | | | 3 | µs |
| $R_O$ | Output Resistance | | 4 | 10 | 20 | kΩ |
| $I_{VREF}$ | Reference Power Supply Input Current | (NOTE 2) | | | 1.5 | mA |

NOTES:
1. Referenced to $V_{CC1}=V_{REF}=4.0$ to 5.5V, $V_{SS}=AV_{SS}=0V$ at $T_{opr}$ = –40 to 85°C / –40 to 125°C unless otherwise specified. T version = –40 to 85°C, V version =–40 to 125°C
2. This applies when using one D/A converter, with the D/A register for the unused D/A converter set to “00h”. The resistor ladder of the A/D converter is not included. Also, when D/A register contents are not “00h”, the $I_{VREF}$ will flow even if Vref id disconnected by the A/D control register.

**Table 5.53 Flash Memory Version Electrical Characteristics (1) for 100 cycle products (B, U)**

| Symbol | Parameter | | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| – | Program and Erase Endurance (3) | | 100 | | | cycle |
| – | Word Program Time ($V_{CC1}$=5.0V) | | | 25 | 200 | µs |
| – | Lock Bit Program Time | | | 25 | 200 | µs |
| – | Block Erase Time ($V_{CC1}$=5.0V) | 4-Kbyte block | 4 | 0.3 | 4 | s |
| – | | 8-Kbyte block | | 0.3 | 4 | s |
| – | | 32-Kbyte block | | 0.5 | 4 | s |
| – | | 64-Kbyte block | | 0.8 | 4 | s |
| – | Erase All Unlocked Blocks Time (2) | | | | 4×n | s |
| $t_{PS}$ | Flash Memory Circuit Stabilization Wait Time | | | | 15 | µs |
| – | Data Hold Time (5) | | 20 | | | year |

**Table 5.54 Flash Memory Version Electrical Characteristics (6) for 10,000 cycle products (B7, U7) (Block A and Block 1 (7))**

| Symbol | Parameter | | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| – | Program and Erase Endurance (3, 8, 9) | | 10,000 (4) | | | cycle |
| – | Word Program Time ($V_{CC}$1=5.0V) | | | 25 | | µs |
| – | Lock Bit Program Time | | | 25 | | µs |
| – | Block Erase Time ($V_{CC1}$=5.0V) | 4-Kbyte block | 4 | 0.3 | | s |
| $t_{PS}$ | Flash Memory Circuit Stabilization Wait Time | | | | 15 | µs |
| – | Data Hold Time (5) | | 20 | | | year |

NOTES:
1. Referenced to $V_{CC1}$=4.5 to 5.5V at $T_{opr}$ = 0 to 60 °C unless otherwise specified.
2. n denotes the number of block erases.
3. Program and Erase Endurance refers to the number of times a block erase can be performed.
   If the program and erase endurance is n (n=100, 1,000, or 10,000), each block can be erased n times.
   For example, if a 4 Kbytes block A is erased after writing 1 word data 2,048 times, each to a different address, this counts as one program and erase endurance. Data cannot be written to the same address more than once without erasing the block. (Rewrite prohibited)
4. Maximum number of E/W cycles for which operation is guaranteed.
5. Ta (ambient temperature)=55 °C. As to the data hold time except Ta=55 °C, please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor.
6. Referenced to $V_{CC1}$ = 4.5 to 5.5V at $T_{opr}$ = –40 to 85 °C (B7, U7 (T version)) / –40 to 125 °C (B7, U7 (V version)) unless otherwise specified.
7. Table 5.54 applies for block A or block 1 program and erase endurance > 1,000. Otherwise, use Table 5.53.
8. To reduce the number of program and erase endurance when working with systems requiring numerous rewrites, write to unused word addresses within the block instead of rewrite. Erase block only after all possible addresses are used. For example, an 8-word program can be written 256 times maximum before erase becomes necessary.
   Maintaining an equal number of erasure between block A and block 1 will also improve efficiency. It is important to track the total number of times erasure is used.
9. Should erase error occur during block erase, attempt to execute clear status register command, then block erase command at least three times until erase error disappears.
10. Set the PM17 bit in the PM1 register to “1” (wait state) when executing more than 100 times rewrites (B7 and U7).
11. Customers desiring E/W failure rate information should contact their Renesas technical support representative.

**Table 5.55 Flash Memory Version Program/Erase Voltage and Read Operation Voltage Characteristics (at $T_{opr}$ = 0 to 60 °C(B, U), $T_{opr}$ = –40 to 85 °C (B7, U7 (T version)) / –40 to 125 °C (B7, U7 (V version))**

| Flash Program, Erase Voltage | Flash Read Operation Voltage |
|---|---|
| $V_{CC1}$ = 5.0 V ± 0.5 V | $V_{CC1}$=4.0 to 5.5 V |

**Table 5.56 Power Supply Circuit Timing Characteristics**

| Symbol | Parameter | Measuring Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $t_{d(P-R)}$ | Time for Internal Power Supply Stabilization During Powering-On | $V_{CC1}$=4.0V to 5.5V | | | 2 | ms |
| $t_{d(R-S)}$ | STOP Release Time | | | | 150 | µs |
| $t_{d(W-S)}$ | Low Power Dissipation Mode Wait Mode Release Time | | | | 150 | µs |

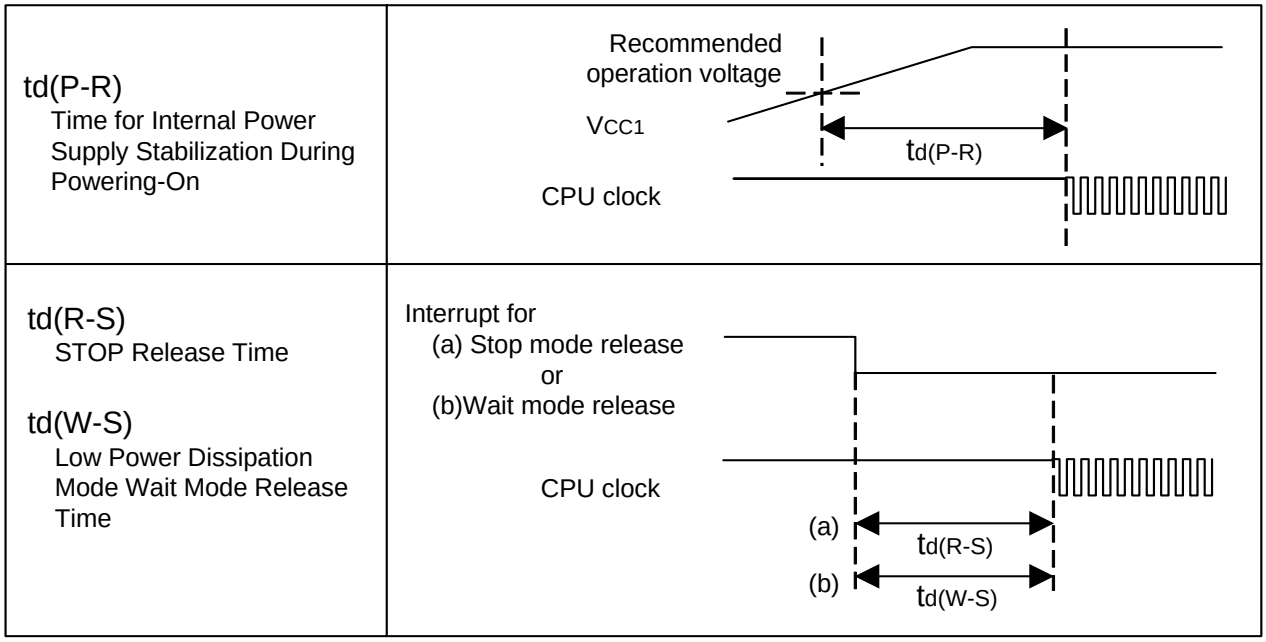



**Figure 5.22 Power Supply Circuit Timing Diagram**

# $V_{CC1}=V_{CC2}=5V$

**Table 5.57 Electrical Characteristics (1)** (1)

| Symbol | Parameter | | Measuring Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $V_{OH}$ | HIGH Output Voltage (2) | P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1 | $I_{OH}$=–5mA | $V_{CC1}$–2.0 | | $V_{CC1}$ | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7 | $I_{OH}$=–5mA | $V_{CC2}$–2.0 | | $V_{CC2}$ | |
| $V_{OH}$ | HIGH Output Voltage (2) | P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1 | $I_{OH}$=–200μA | $V_{CC1}$–0.3 | | $V_{CC1}$ | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7 | $I_{OH}$=–200μA | $V_{CC2}$–0.3 | | $V_{CC2}$ | |
| $V_{OH}$ | HIGH Output Voltage XOUT | HIGHPOWER | $I_{OH}$=–1mA | $V_{CC1}$–2.0 | | $V_{CC1}$ | V |
| | | LOWPOWER | $I_{OH}$=–0.5mA | $V_{CC1}$–2.0 | | $V_{CC1}$ | |
| | HIGH Output Voltage XCOUT | HIGHPOWER | With no load applied | | 2.5 | | V |
| | | LOWPOWER | With no load applied | | 1.6 | | |
| $V_{OL}$ | LOW Output Voltage (2) | P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1 | $I_{OL}$=5mA | | | 2.0 | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7 | $I_{OL}$=5mA | | | 2.0 | |
| $V_{OL}$ | LOW Output Voltage (2) | P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1 | $I_{OL}$=200μA | | | 0.45 | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7 | $I_{OL}$=200μA | | | 0.45 | |
| $V_{OL}$ | LOW Output Voltage XOUT | HIGHPOWER | $I_{OL}$=1mA | | | 2.0 | V |
| | | LOWPOWER | $I_{OL}$=0.5mA | | | 2.0 | |
| | LOW Output Voltage XCOUT | HIGHPOWER | With no load applied | | 0 | | V |
| | | LOWPOWER | With no load applied | | 0 | | |
| $V_{T+}$-$V_{T-}$ | Hysteresis | HOLD, RDY, TA0IN to TA4IN, TB0IN to TB5IN, INT0 to INT5, NMI, ADTRG, CTS0 to CTS2, CLK0 to CLK4, TA0OUT to TA4OUT, KI0 to KI3, RXD0 to RXD2, SCL0 to SCL2, SDA0 to SDA2, SIN3, SIN4 | | 0.2 | | 1.0 | V |
| $V_{T+}$-$V_{T-}$ | Hysteresis | RESET | | 0.2 | | 2.5 | V |
| $I_{IH}$ | HIGH Input Current (2) | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1, XIN, RESET, CNVSS, BYTE | $V_I$=5V | | | 5.0 | μA |
| $I_{IL}$ | LOW Input Current (2) | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7,P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1, XIN, RESET, CNVSS, BYTE | $V_I$=0V | | | –5.0 | μA |
| $R_{PULLUP}$ | Pull-Up Resistance (2) | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7,P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1 | $V_I$=0V | 30 | 50 | 170 | kΩ |
| $R_{fXIN}$ | Feedback Resistance XIN | | | | 1.5 | | MΩ |
| $R_{fXCIN}$ | Feedback Resistance XCIN | | | | 15 | | MΩ |
| $V_{RAM}$ | RAM Retention Voltage | | At stop mode | 2.0 | | | V |

NOTES:
1. Referenced to $V_{CC1}=V_{CC2}$=4.0 to 5.5V, $V_{SS}$ = 0V at $T_{opr}$ = –40 to 85°C / –40 to 125°C, f(BCLK)=24MHz unless otherwise specified. T version = –40 to 85°C, V version =–40 to 125°C.
2. There is no external connections for port P1_0 to P1_7, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version.

**Table 5.58 Electrical Characteristics (2)** (1)

| Symbol | Parameter | | Measuring Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Typ. | Max. | |
| $I_{CC}$ | Power Supply Current ($V_{CC1}$=$V_{CC2}$=4.0V to 5.5V) | In single-chip mode, the output pins are open and other pins are $V_{SS}$ | Mask ROM | f(BCLK)=24MHz<br>No division, PLL operation | | 14 | 20 | mA |
| | | | | No division,<br>On-chip oscillation | | 1 | | mA |
| | | | Flash Memory | f(BCLK)=24MHz,<br>No division, PLL operation | | 18 | 27 | mA |
| | | | | No division,<br>On-chip oscillation | | 1.8 | | mA |
| | | | Flash Memory Program | f(BCLK)=10MHz,<br>$V_{CC1}$=5.0V | | 15 | | mA |
| | | | Flash Memory Erase | f(BCLK)=10MHz,<br>$V_{CC1}$=5.0V | | 25 | | mA |
| | | | Mask ROM | f(XCIN)=32kHz<br>Low power dissipation mode, ROM (3) | | 25 | | µA |
| | | | Flash Memory | f(BCLK)=32kHz<br>Low power dissipation mode, RAM (3) | | 25 | | µA |
| | | | | f(BCLK)=32kHz<br>Low power dissipation mode, Flash Memory (3) | | 420 | | µA |
| | | | | On-chip oscillation,<br>Wait mode | | 50 | | µA |
| | | | Mask ROM Flash Memory | f(BCLK)=32kHz<br>Wait mode (2),<br>Oscillation capability High | | 7.5 | | µA |
| | | | | f(BCLK)=32kHz<br>Wait mode (2),<br>Oscillation capability Low | | 2.0 | | µA |
| | | | | Stop mode<br>Topr =25°C | | 2.0 | 6.0 | µA |
| | | | | Stop mode<br>Topr =85°C | | | 20 | µA |
| | | | | Stop mode<br>Topr =125°C | | | TBD | µA |

NOTES:
1. Referenced to $V_{CC1}$=$V_{CC2}$=4.0 to 5.5V, $V_{SS}$ = 0V at $T_{opr}$ = –40 to 85°C / –40 to 125°C, f(BCLK)=24MHz unless otherwise specified. T version = –40 to 85°C, V version =–40 to 125°C.
2. With one timer operated using fC32.
3. This indicates the memory in which the program to be executed exists.

# $V_{CC1}=V_{CC2}=5V$

**Timing Requirements**
**($V_{CC1}$ = $V_{CC2}$ = 5V, $V_{SS}$ = 0V, at $T_{opr}$ = –40 to 85°C (T version) / –40 to 125°C (V version) unless otherwise specified)**

**Table 5.59 External Clock Input (XIN input)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_c$ | External Clock Input Cycle Time | 62.5 | | ns |
| $t_{w(H)}$ | External Clock Input HIGH Pulse Width | 25 | | ns |
| $t_{w(L)}$ | External Clock Input LOW Pulse Width | 25 | | ns |
| $t_r$ | External Clock Rise Time | | 15 | ns |
| $t_f$ | External Clock Fall Time | | 15 | ns |

# $V_{CC1}$=$V_{CC2}$=5V

**Timing Requirements**
**($V_{CC1}$ = $V_{CC2}$ = 5V, $V_{SS}$ = 0V, at $T_{opr}$ = –40 to 85°C (T version) / –40 to 125°C (V version) unless otherwise specified)**

**Table 5.60 Timer A Input (Counter Input in Event Counter Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TA)}$ | TAiIN Input Cycle Time | 100 | | ns |
| $t_{w(TAH)}$ | TAiIN Input HIGH Pulse Width | 40 | | ns |
| $t_{w(TAL)}$ | TAiIN Input LOW Pulse Width | 40 | | ns |

**Table 5.61 Timer A Input (Gating Input in Timer Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TA)}$ | TAiIN Input Cycle Time | 400 | | ns |
| $t_{w(TAH)}$ | TAiIN Input HIGH Pulse Width | 200 | | ns |
| $t_{w(TAL)}$ | TAiIN Input LOW Pulse Width | 200 | | ns |

**Table 5.62 Timer A Input (External Trigger Input in One-shot Timer Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TA)}$ | TAiIN Input Cycle Time | 200 | | ns |
| $t_{w(TAH)}$ | TAiIN Input HIGH Pulse Width | 100 | | ns |
| $t_{w(TAL)}$ | TAiIN Input LOW Pulse Width | 100 | | ns |

**Table 5.63 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{w(TAH)}$ | TAiIN Input HIGH Pulse Width | 100 | | ns |
| $t_{w(TAL)}$ | TAiIN Input LOW Pulse Width | 100 | | ns |

**Table 5.64 Timer A Input (Counter Increment/Decrement Input in Event Counter Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(UP)}$ | TAiOUT Input Cycle Time | 2000 | | ns |
| $t_{w(UPH)}$ | TAiOUT Input HIGH Pulse Width | 1000 | | ns |
| $t_{w(UPL)}$ | TAiOUT Input LOW Pulse Width | 1000 | | ns |
| $t_{su(UP-TIN)}$ | TAiOUT Input Setup Time | 400 | | ns |
| $t_{h(TIN-UP)}$ | TAiOUT Input Hold Time | 400 | | ns |

**Table 5.65 Timer A Input (Two-phase Pulse Input in Event Counter Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TA)}$ | TAiIN Input Cycle Time | 800 | | ns |
| $t_{su(TAIN-TAOUT)}$ | TAiOUT Input Setup Time | 200 | | ns |
| $t_{su(TAOUT-TAIN)}$ | TAiIN Input Setup Time | 200 | | ns |

# $V_{CC1}$=$V_{CC2}$=5V

**Timing Requirements**
**($V_{CC1}$ = $V_{CC2}$ = 5V, $V_{SS}$ = 0V, at $T_{opr}$ = –40 to 85°C (T version) / –40 to 125°C (V version) unless otherwise specified)**

**Table 5.66 Timer B Input (Counter Input in Event Counter Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TB)}$ | TBiIN Input Cycle Time (counted on one edge) | 100 | | ns |
| $t_{w(TBH)}$ | TBiIN Input HIGH Pulse Width (counted on one edge) | 40 | | ns |
| $t_{w(TBL)}$ | TBiIN Input LOW Pulse Width (counted on one edge) | 40 | | ns |
| $t_{c(TB)}$ | TBiIN Input Cycle Time (counted on both edges) | 200 | | ns |
| $t_{w(TBH)}$ | TBiIN Input HIGH Pulse Width (counted on both edges) | 80 | | ns |
| $t_{w(TBL)}$ | TBiIN Input LOW Pulse Width (counted on both edges) | 80 | | ns |

**Table 5.67 Timer B Input (Pulse Period Measurement Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TB)}$ | TBiIN Input Cycle Time | 400 | | ns |
| $t_{w(TBH)}$ | TBiIN Input HIGH Pulse Width | 200 | | ns |
| $t_{w(TBL)}$ | TBiIN Input LOW Pulse Width | 200 | | ns |

**Table 5.68 Timer B Input (Pulse Width Measurement Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TB)}$ | TBiIN Input Cycle Time | 400 | | ns |
| $t_{w(TBH)}$ | TBiIN Input HIGH Pulse Width | 200 | | ns |
| $t_{w(TBL)}$ | TBiIN Input LOW Pulse Width | 200 | | ns |

**Table 5.69 A/D Trigger Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(AD)}$ | $\overline{\text{ADTRG}}$ Input Cycle Time | 1000 | | ns |
| $t_{w(ADL)}$ | $\overline{\text{ADTRG}}$ input LOW Pulse Width | 125 | | ns |

**Table 5.70 Serial Interface**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(CK)}$ | CLKi Input Cycle Time | 200 | | ns |
| $t_{w(CKH)}$ | CLKi Input HIGH Pulse Width | 100 | | ns |
| $t_{w(CKL)}$ | CLKi Input LOW Pulse Width | 100 | | ns |
| $t_{d(C-Q)}$ | TXDi Output Delay Time | | 80 | ns |
| $t_{h(C-Q)}$ | TXDi Hold Time | 0 | | ns |
| $t_{su(D-C)}$ | RXDi Input Setup Time | 70 | | ns |
| $t_{h(C-D)}$ | RXDi Input Hold Time | 90 | | ns |

**Table 5.71 External Interrupt $\overline{\text{INTi}}$ Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{w(INH)}$ | $\overline{\text{INTi}}$ Input HIGH Pulse Width | 250 | | ns |
| $t_{w(INL)}$ | $\overline{\text{INTi}}$ Input LOW Pulse Width | 250 | | ns |

$V_{CC1}=V_{CC2}=5V$

**Switching Characteristics**
**($V_{CC1}$ = $V_{CC2}$ = 5V, $V_{SS}$ = 0V, at $T_{opr}$ = –40 to 85°C (T version) / –40 to 125°C (V version) unless otherwise specified)**

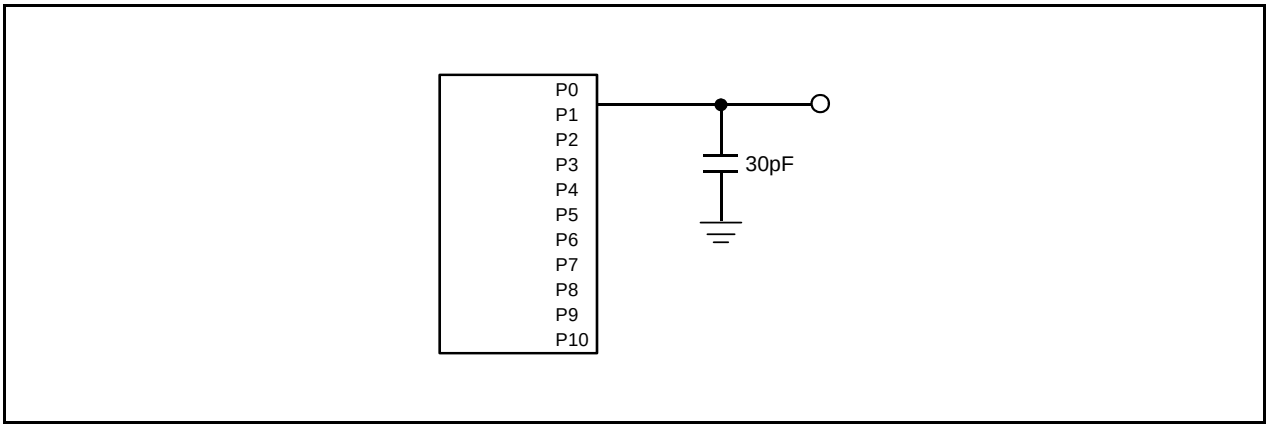



**Figure 5.23 Ports P0 to P10 Measurement Circuit**

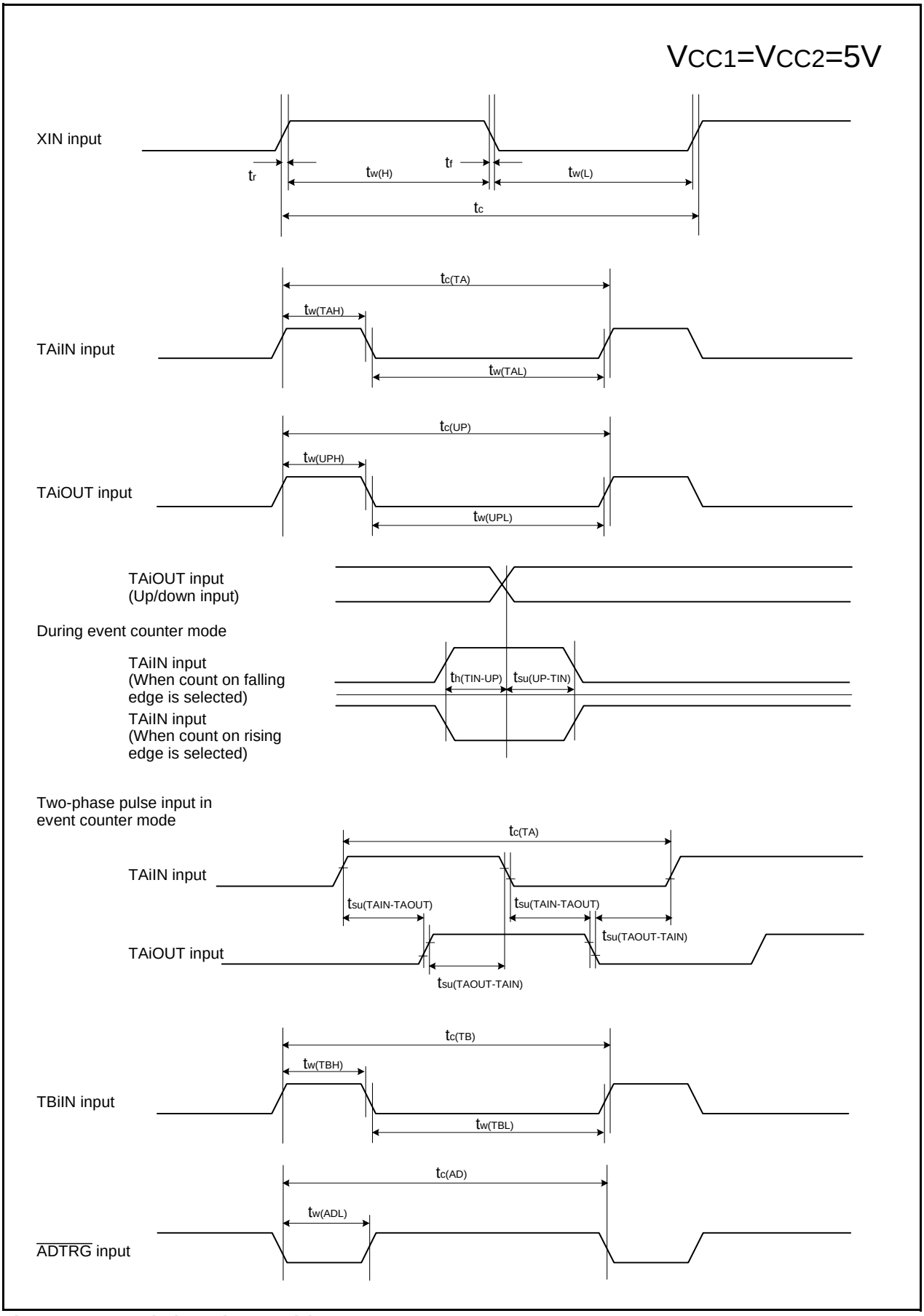



**Figure 5.24 Timing Diagram (1)**

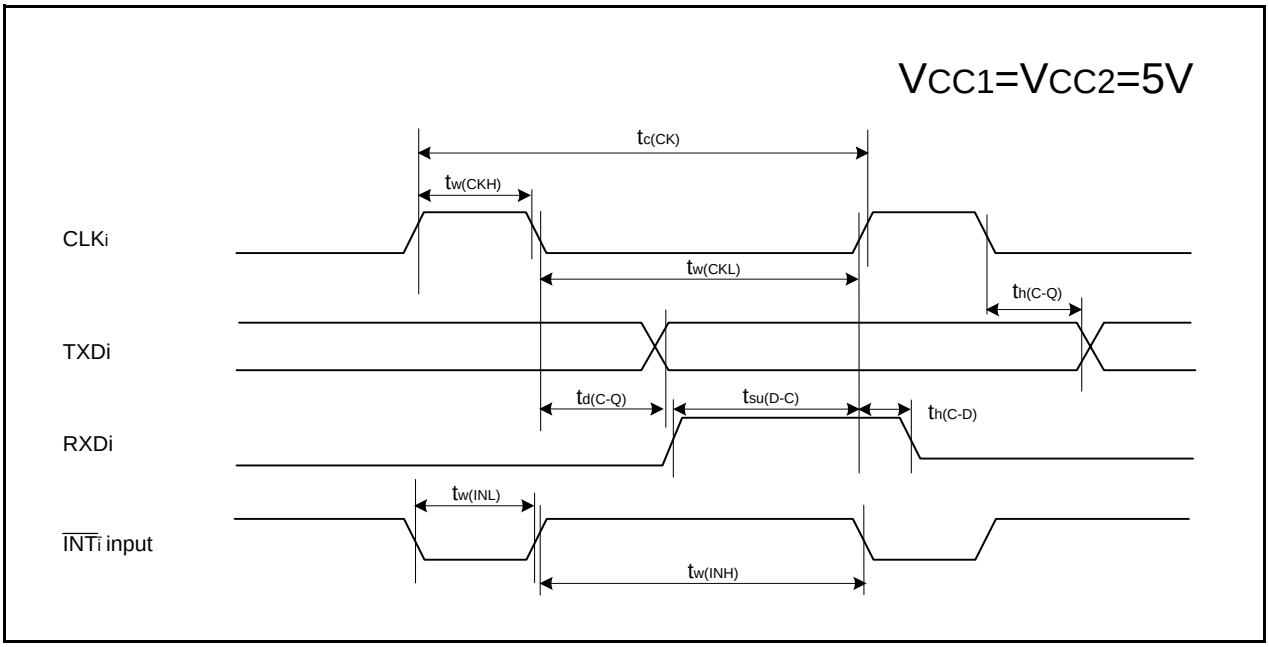
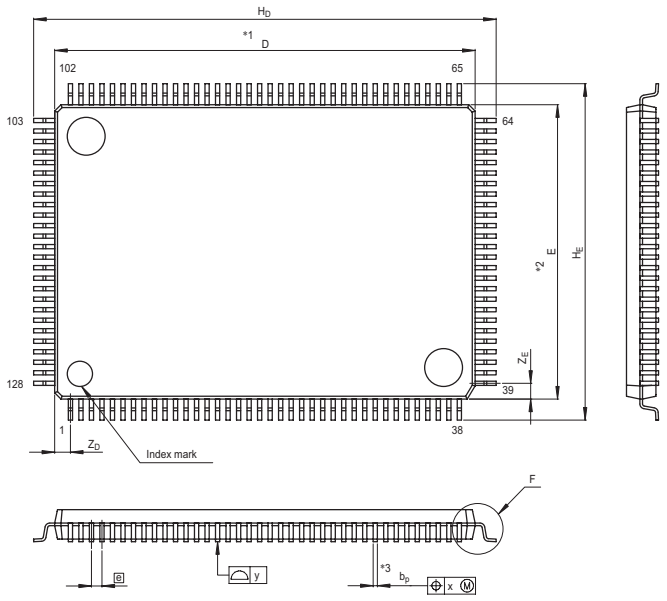
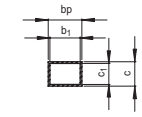



**Figure 5.25 Timing Diagram (2)**

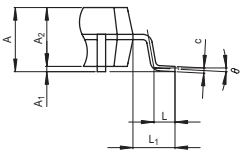
# Appendix 1.Package Dimensions

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-LQFP128-14x20-0.50 | PLQP0128KB-A | 128P6Q-A | 0.9g |




Terminal cross section

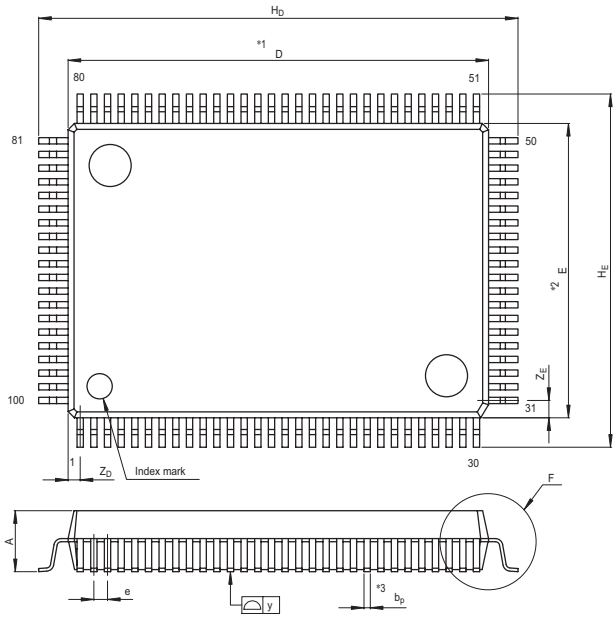


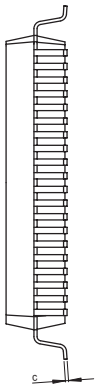

DetailF

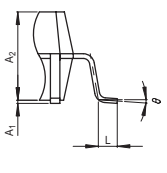
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 19.9 | 20.0 | 20.1 |
| E | 13.9 | 14.0 | 14.1 |
| $A_2$ | — | 1.4 | — |
| $H_D$ | 21.8 | 22.0 | 22.2 |
| $H_E$ | 15.8 | 16.0 | 16.2 |
| A | — | — | 1.7 |
| $A_1$ | 0.05 | 0.125 | 0.2 |
| $b_p$ | 0.17 | 0.22 | 0.27 |
| $b_1$ | — | 0.20 | — |
| c | 0.09 | 0.145 | 0.20 |
| $c_1$ | — | 0.125 | — |
| θ | 0° | — | 8° |
| e | — | 0.5 | — |
| x | — | — | 0.10 |
| y | — | — | 0.10 |
| $Z_D$ | — | 0.75 | — |
| $Z_E$ | — | 0.75 | — |
| L | 0.35 | 0.5 | 0.65 |
| $L_1$ | — | 1.0 | — |

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-QFP100-14x20-0.65 | PRQP0100JB-A | 100P6S-A | 1.6g |



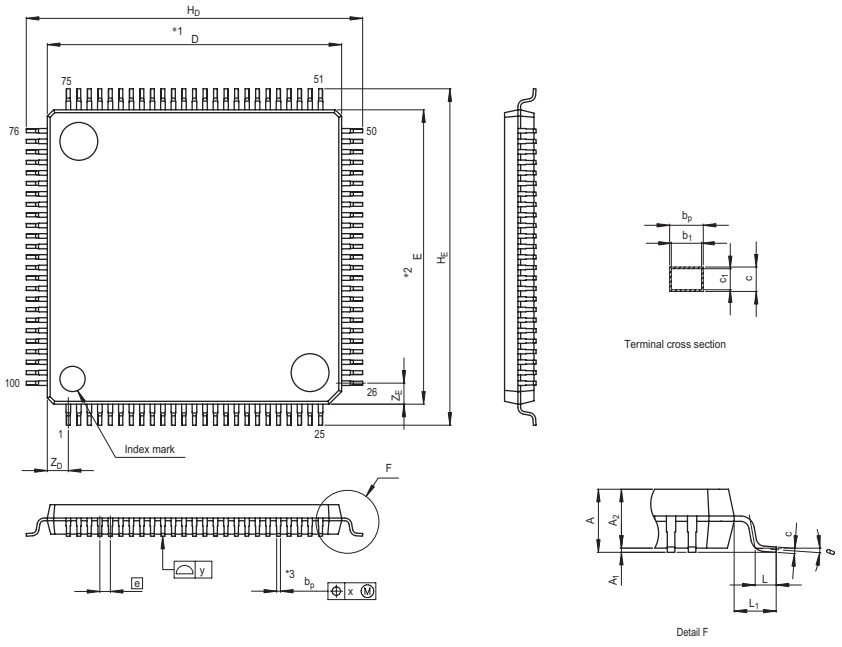




Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 19.8 | 20.0 | 20.2 |
| E | 13.8 | 14.0 | 14.2 |
| $A_2$ | — | 2.8 | — |
| $H_D$ | 22.5 | 22.8 | 23.1 |
| $H_E$ | 16.5 | 16.8 | 17.1 |
| A | — | — | 3.05 |
| $A_1$ | 0 | 0.1 | 0.2 |
| $b_p$ | 0.25 | 0.3 | 0.4 |
| c | 0.13 | 0.15 | 0.2 |
| θ | 0° | — | 10° |
| e | 0.5 | 0.65 | 0.8 |
| y | — | — | 0.10 |
| $Z_D$ | — | 0.575 | — |
| $Z_E$ | — | 0.825 | — |
| L | 0.4 | 0.6 | 0.8 |

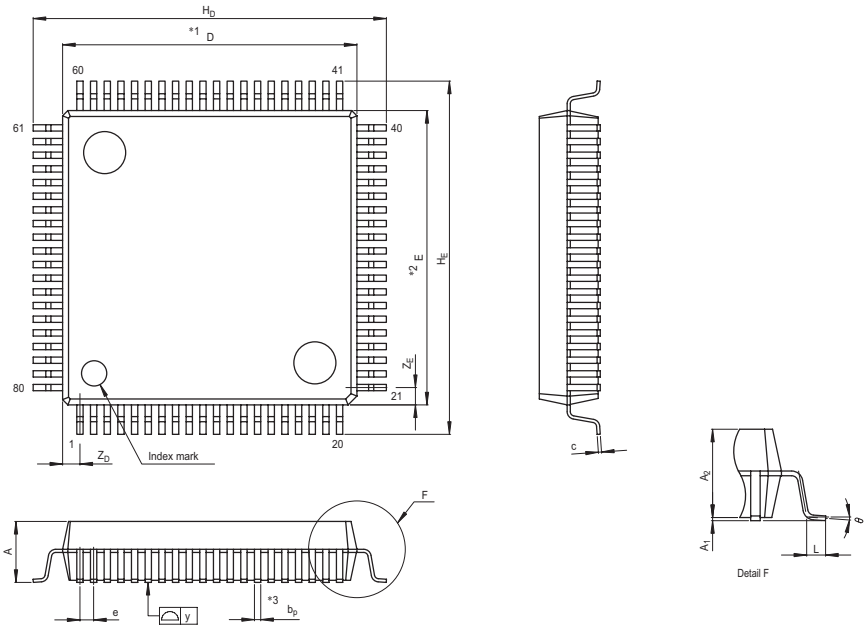
| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-LQFP100-14x14-0.50 | PLQP0100KB-A | 100P6Q-A / FP-100U / FP-100UV | 0.6g |




NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 13.9 | 14.0 | 14.1 |
| E | 13.9 | 14.0 | 14.1 |
| $A_2$ | — | 1.4 | — |
| $H_D$ | 15.8 | 16.0 | 16.2 |
| $H_E$ | 15.8 | 16.0 | 16.2 |
| A | — | — | 1.7 |
| $A_1$ | 0.05 | 0.1 | 0.15 |
| $b_p$ | 0.15 | 0.20 | 0.25 |
| $b_1$ | — | 0.18 | — |
| c | 0.09 | 0.145 | 0.20 |
| $c_1$ | — | 0.125 | — |
| θ | 0° | — | 8° |
| e | — | 0.5 | — |
| x | — | — | 0.08 |
| y | — | — | 0.08 |
| $Z_D$ | — | 1.0 | — |
| $Z_E$ | — | 1.0 | — |
| L | 0.35 | 0.5 | 0.65 |
| $L_1$ | — | 1.0 | — |

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-QFP80-14x14-0.65 | PRQP0080JA-A | 80P6S-A | 1.1g |




NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 13.8 | 14.0 | 14.2 |
| E | 13.8 | 14.0 | 14.2 |
| $A_2$ | — | 2.8 | — |
| $H_D$ | 16.5 | 16.8 | 17.1 |
| $H_E$ | 16.5 | 16.8 | 17.1 |
| A | — | — | 3.05 |
| $A_1$ | 0 | 0.1 | 0.2 |
| $b_p$ | 0.25 | 0.3 | 0.4 |
| c | 0.13 | 0.15 | 0.2 |
| θ | 0° | — | 10° |
| e | 0.5 | 0.65 | 0.8 |
| y | — | — | 0.10 |
| $Z_D$ | — | 0.825 | — |
| $Z_E$ | — | 0.825 | — |
| L | 0.4 | 0.6 | 0.8 |

| REVISION HISTORY | M16C/62P Group (M16C/62P, M16C/62PT) Hardware Manual |
|---|---|

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 1.10 | May 28, 2003 | 1 | Applications are partly revised. |
| | | 2 | Table 1.1.1 is partly revised. |
| | | 4-5 | Table 1.1.2 and 1.1.3 is partly revised.<br>"Note 1" is partly revised. |
| | | 22 | Table 1.5.3 is partly revised. |
| | | 23 | Table 1.5.5 is partly revised.<br>Table 1.5.6 is added. |
| | | 24 | Table 1.5.9 is partly revised. |
| | | 30 | Notes 1 and 2 in Table 1.5.26 is partly revised. |
| | | 31 | Notes 1 in Table 1.5.27 is partly revised. |
| | | 30-31 | Note 3 is added to "Data output hold time (refers to BCLK)" in Table 1.5.26 and 1.5.27. |
| | | 32 | Note 4 is added to "th(ALE-AD)" in Table 1.5.28. |
| | | 30-32 | Switching Characteristics is partly revised. |
| | | 36-39 | th(WR-AD) and th(WR-DB) in Figure 1.5.5 to 1.5.8 is partly revised. |
| | | 40-41 | th(ALE-AD), th(WR-CS), th(WR-DB) and th(WR-AD) in Figure 1.5.9 to 1.5.10 is partly revised. |
| | | 42 | Note 2 is added to Table 1.5.29. |
| | | 47 | Notes 1 and 2 in Table 1.5.45 is partly revised. |
| | | 48 | Notes 1 in Table 1.5.46 is partly revised. |
| | | 47-48 | Note 3 is added to "Data output hold time (refers to BCLK)" in Table 1.5.45 and 1.5.46. |
| | | 49 | Note 4 is added to "th(ALE-AD)" in Table 1.5.47. |
| | | 47-48 | Switching Characteristics is partly revised. |
| | | 53-56 | th(WR-AD) and th(WR-DB) in Figure 1.5.15 to 1.5.18 is partly revised. |
| | | 57-58 | th(ALE-AD), th(WR-CS), th(WR-DB) and th(WR-AD) in Figure 1.5.19 to 1.5.20 is partly revised. |
| 2.00 | Oct 29, 2003 | - | Since high reliability version is added, a group name is revised.<br>M16C/62 Group (M16C/62P) → M16C/62 Group (M16C/62P, M16C/62PT) |
| | | 2-4 | Table 1.1 to 1.3 are revised.<br>Note 3 is partly revised. |
| | | 2-4 | Table 1.1 to 1.3 are revised.<br>Note 3 is partly revised. |
| | | 6 | Figure 1.2 Note5 is deleted. |
| | | 7-9 | Table 1.4 to 1.7 Product List is partly revised. |
| | | 11 | Table 1.8 and Figure 1.4 are added. |
| | | 12-15 | Figure 1.5 to 1.9 ZP is added. |
| | | 17,19 | Table 1.10 and 1.12 ZP is added to timer A. |
| | | 18,20 | Table 1.11 and 1.13 VCC1 is added to VREF. |
| | | 30 | Table 5.1 is revised. |
| | | 31-32 | Table 5.2 and 5.3 are revised. |

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| | | 33 | Table 5.4 A-D Conversion Characteristics is revised. |
| | | | Table 5.5 D-A Conversion Characteristics revised. |
| | | 34,74 | Table 5.6 to 5.7 and table 5.54 to 5.55 are revised. |
| | | 36 | Table 5.11 is revised. |
| | | 38,55 | Table 5.14 and 5.33 HLDA output deley time is deleted. |
| | | 41 | Figure 5.1 is partly revised. |
| | | 41-43, 58-60 | Table 5.27 to 5.29 and table 5.46 to 48 HLDA output deley time is added. |
| | | 44 | Figure 5.2 Timing Diagram (1) XIN input is added. |
| | | 47-48 | Figure 5.5 to 5.6 Read timing DB → DBi |
| | | 49-50 | Figure 5.7 to 5.8 Write timing DB → DBi |
| | | 52 | Figure 5.10 DB → DBi |
| | | 53 | Table 5.30 is revised. |
| | | 58 | Figure 5.11 is partly revised. |
| | | 61 | Figure 5.12 Timing Diagram (1) XIN input is added. |
| | | 64-65 | Figure 5.15 to 5.16 Read timing DB → DBi |
| | | 66-67 | Figure 5.17 to 5.18 Write timing DB → DBi |
| | | 69 | Figure 5.20 DB → DBi |
| | | 70-85 | Electrical Characteristics (M16C/62PT) is added. |
| 2.10 | Nov 07, 2003 | 8-9 | Table 1.5 to 1.7 Product List is partly revised. Note 1 is deleted. |
| | | 23 | Table 3.1 is revised. |
| | | 71 | Table 5.50 is revised. |
| | | 72 | Table 5.51 is deleted. |
| 2.11 | Jan 06, 2004 | 16 | Table 1.9 NOTE 3 VCC1 VCC2 → VCC1 > VCC2 |
| | | 17-18 | Table 1.10 to 1.11 NOTE 1 VCC1 VCC2 → VCC1 > VCC2 |
| | | 31 | Table 5.2 Power Supply Ripple Allowable Frequency Unit MHz → kHz |
| 2.30 | Sep 01, 2004 | 12 | Table 1.9 and Figure 1.5 are added. |
| | | 18, 20 | Table 1.11 to 1.13 are revised. |
| | | 19,21 | Table 1.12 to 1.14 are revised. |
| | | 24 | Figure 3.1 is partly revised. |
| | | | Note 3 is added. |
| | | 25 | Note 6 is added. |
| | | 33 | Table 5.3 is revised. |
| | | | Note 2 in Table 5.4 is added. |
| | | 34 | Table 5.5 to 5.6 is partly revised. |
| | | 35 | Table 5.8 is revised. |
| | | | Table 5.9 is revised. |
| | | 37 | Table 5.11 is revised. |

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| | | 40 | Table 5.24 is partly revised. |
| | | 57 | Table 5.43 is partly revised. |
| | | 70 | Table 5.48 is partly revised. |
| | | 72 | Table 5.50 is partly revised. |
| | | 73 | Table 5.53 is partly revised. |
| | | 74 | Table 5.55 is revised. |
| | | 76 | Table 5.57 is partly revised. |
| | | 79 | Table 5.69 is partly revised. |
| 2.41 | Jan 01, 2006 | - | voltage down detection reset -> brown-out detection Reset |
| | | 2-4 | Tables 1.1 to 1.3 Performance outline of M16C/62P group are partly revised. |
| | | 7 | Table 1.4 Product List (1) is partly revised.<br>Note 1 is added. |
| | | 8 | Table 1.5 Product List (2) is partly revised.<br>Note 1, 2 and 3 are added. |
| | | 9 | Table 1.6 Product List (3) is partly revised.<br>Note 1 and 2 are added. |
| | | 10 | Table 1.7 Product List (4) is partly revised.<br>Note 1 and 2 are added. |
| | | 11 | Figure 1.3 Type No., Memory Size, Shows RAM capacity, and Package is partly revised |
| | | 12 | Table 1.8 Product Code of Flash Memory version and ROMless version for M16C/62P is partly revised. |
| | | 13 | Table 1.9 Product Code of Flash Memory version for M16C/62P is partly revised. |
| | | 14 | Figure 1.6 Pin Configuration (Top View) is partly revised. |
| | | 15-17 | Tables 1.10 to 1.12 Pin Characteristics for 128-Pin Package are added. |
| | | 18-19 | Figure 1.7 and 1.8 Pin Configuration (Top View) are partly revised. |
| | | 20-21 | Tables 1.13 to 1.14 Pin Characteristics for 100-Pin Package are added. |
| | | 22 | Figure 1.9 Pin Configuration (Top View) is partly revised. |
| | | 23-24 | Tables 1.15 to 1.16 Pin Characteristics for 80-Pin Package are added. |
| | | 25-29 | Tables 1.17 to 1.21 are partly revised. |
| | | 34 | Note 4 of Table 4.1 SFR Information is partly revised. |
| | | 43 | Table 5.4 A/D Conversion Characteristics is partly revised. |
| | | 45 | Table 5.6 Flash Memory Version Electrical Characteristics for 100 cycle products is partly revised. |
| | | | Table 5.7 Flash Memory Version Electrical Characteristics for 10,000 cycle products is partly revised. |
| | | | Table 5.8 Flash Memory Version Program / Erase Voltage and Read Operation Voltage Characteristics is partly revised. |
| | | 46 | Table 5.9 Low Voltage Detection Circuit Electrical Characteristics is partly revised. |

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| | | 47 | Figure 5.1 Power Supply Circuit Timing Diagram is partly revised. |
| | | 48 | Table 5.11 Electrical Characteristics (1) is partly deleted. |
| | | 49 | Table 5.12 Electrical Characteristics (2) is partly revised. |
| | | 50 | Note 1 of Table 5.13 External Clock Input (XIN input) is added. |
| | | 67 | Notes 1 to 4 of Table 5.32 External Clock Input (XIN input) are added. |
| | | 85 | Table 5.53 Flash Memory Version Electrical Characteristics for 100 cycle products is partly revised. Standard (Min.) is partly revised.<br>Table 5.54 Flash Memory Version Electrical Characteristics for 10,000 cycle products is partly revised. Standard (Min.) is partly revised.<br>Note 5 is revised.<br>Table 23.55 Flash Memory Version Program / Erase Voltage and Read Operation Voltage Characteristics is partly revised. |
| | | 87 | Table 5.57 Electrical Characteristics (1) is partly deleted. |
| | | 88 | Table 5.58 Electrical Characteristics is partly revised. |

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