APS12000 and APS12060

Vertical and Planar Hall-Effect Latches

FEATURES AND BENEFITS

- ASIL Compliant: ASIL A safety element out-of-context (SEooC) developed in accordance with ISO 26262, when used as specified in the safety manual
- Planar and vertical Hall-effect sensor ICs
- 3.3 to 24 V operation
- Automotive-grade ruggedness and fault tolerance
  - □ Extended AEC-Q100 qualification
  - □ Internal protection circuits enable 40 V load dump compliance
  - □ Reverse-battery protection
  - □ Output short-circuit and overvoltage protection
  - □ Operation from –40°C to 175°C junction temperature
  - □ High EMC immunity
- Symmetrical latch switch points
- Choice of output polarity
- Open-drain output
- Solid-state reliability

ISO 26262 ASIL Compliant

BY ALLEGRO VHT

PACKAGES

Not to scale



3-pin SOT23W
(suffix LH)



3-pin SIP (suffix UA)

DESCRIPTION

The APS12000 and APS12060 families of Hall-effect latches are AEC-Q100 qualified for 24 V automotive applications and compliant with ISO 26262 ASIL A. These sensors are temperature-stable and suited for operation over extended junction temperature ranges up to 175°C. The APS12000 and APS12060 families are available in several different magnetic sensitivities to offer flexible options for system design. They are available in active high and active low variants for ease of integration into electronic subsystems.

The APS12000 features a Hall-effect element that is sensitive to magnetic flux perpendicular to the face of the IC package. The APS12060 features a vertical Hall-effect sensing element sensitive to magnetic flux parallel to the face of the IC package.

The devices include on-board reverse-battery and overvoltage protection for operating directly from an automobile battery, as well as protection from shorts to ground by limiting the output current until the short is removed. The device is especially suited for operation from unregulated supplies.

Continued on next page...

TYPICAL APPLICATIONS

- Automotive and industrial safety systems
- Industrial motors/encoders
- Trunk/door/liftgate/wiper motors
- Electronic power steering (EPS)
- Transmission actuators

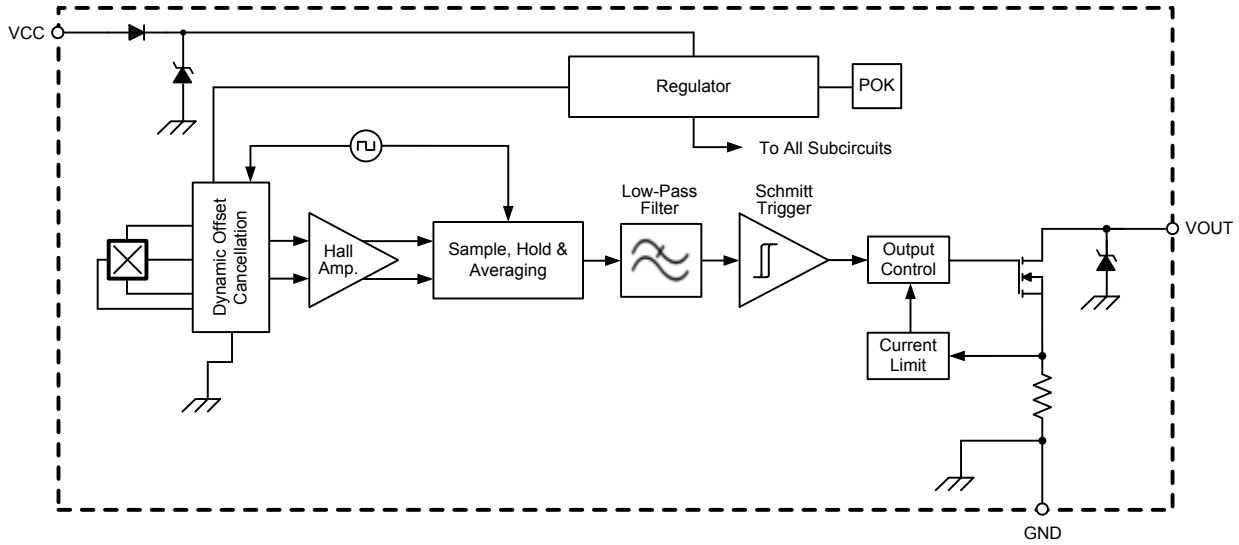
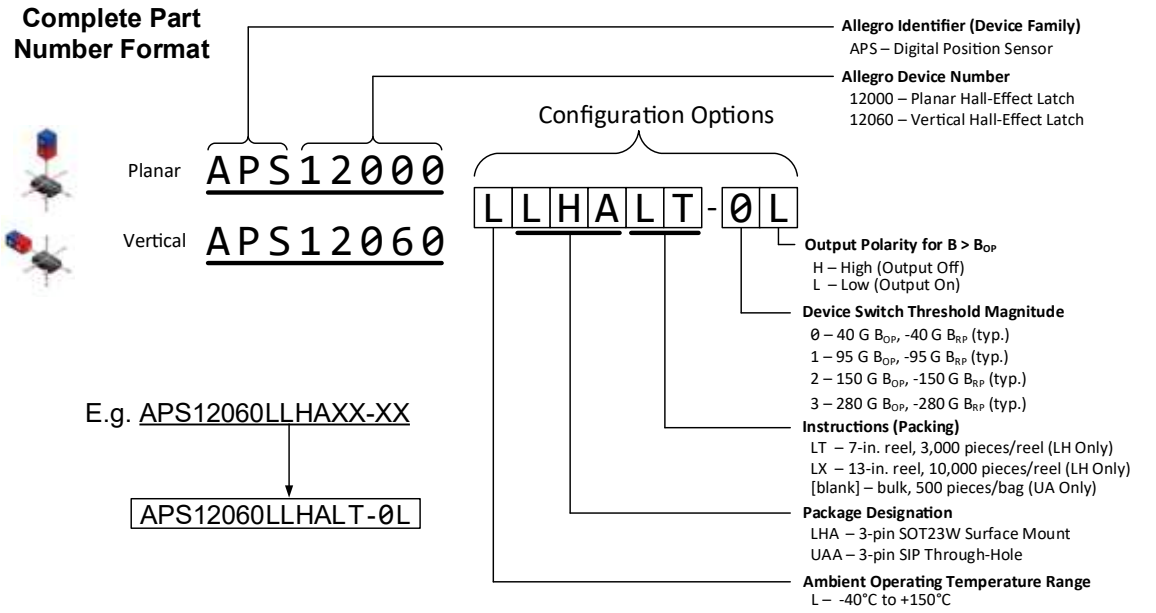


Figure 1: Functional Block Diagram

DESCRIPTION (continued)

The APS12000 and APS12060 were developed in accordance with ISO 26262 as a hardware safety element out-of-context with ASIL A capability for use in automotive safety-related systems when integrated and used in the manner prescribed in the applicable safety manual and datasheet.

Two package styles provide a choice of through-hole or surface mounting. Package type LH is a modified 3-pin SOT23W surface mount package, while package type UA is a 3-pin ultra-mini SIP for through-hole mounting. Both packages are lead (Pb) free, with 100% matte-tin-plated leadframes.



SELECTION GUIDE

Part Number [1]	Packing [2]	Mounting	Sensing Orientation	Output Polarity for B > B_{OP}	Typical B_{OP}/B_{RP} Threshold (G)
APS12000LLHALT-0H	7-in. reel, 3000 pieces/reel	3-pin SOT23W surface mount	Z-Axis	High	±40
APS12000LLHALX-0H	13-in. reel, 10000 pieces/reel	3-pin SOT23W surface mount			
APS12000LUAA-0H	Bulk, 500 pieces/bag	3-pin SIP through-hole			
APS12060LLHALT-0L	7-in. reel, 3000 pieces/reel	3-pin SOT23W surface mount	X-Axis	Low	±40
APS12060LLHALX-0L	13-in. reel, 10000 pieces/reel	3-pin SOT23W surface mount			
APS12060LUAA-0L	Bulk, 500 pieces/bag	3-pin SIP through-hole	Y-Axis		
APS12060LLHALT-0H	7-in. reel, 3000 pieces/reel	3-pin SOT23W surface mount	X-Axis	High	±40
APS12060LLHALX-0H	13-in. reel, 10000 pieces/reel	3-pin SOT23W surface mount			
APS12060LUAA-0H	Bulk, 500 pieces/bag	3-pin SIP through-hole	Y-Axis		
APS12060LLHALT-1L	7-in. reel, 3000 pieces/reel	3-pin SOT23W surface mount	X-Axis	Low	±95
APS12060LLHALX-1L	13-in. reel, 10000 pieces/reel	3-pin SOT23W surface mount			
APS12060LUAA-1L	Bulk, 500 pieces/bag	3-pin SIP through-hole	Y-Axis		

[1] Contact Allegro MicroSystems for options not listed in the selection guide.
[2] Contact Allegro MicroSystems for additional packing options.

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ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Units
Supply Voltage [1]	V_{CC}		40	V
Reverse Supply Voltage [1]	V_{RCC}		–18	V
Output Voltage [1]	V_{OUT}		–0.3 to 32	V
Output Current [2]	I_{OUT}		40	mA
Reverse Output Current	I_{ROUT}		–50	mA
Magnetic Flux Density [3]	B		Unlimited	G
Operating Ambient Temperature	T_A	Range L	–40 to 150	°C
Maximum Junction Temperature	$T_{J(max)}$		165	°C
		For 1000 hours	175	°C
Storage Temperature	T_{stg}		–65 to 170	°C

[1] This rating does not apply to extremely short voltage transients. Transient events such as Load Dump and/or ESD have individual, specific ratings.
[2] Through short-circuit current limiting device.
[3] Guaranteed by design.

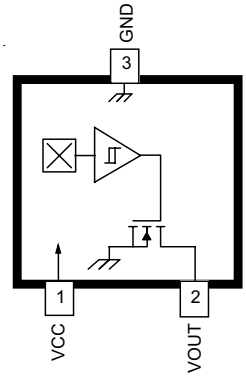
ESD PERFORMANCE [4]

Characteristic	Symbol	Notes	Rating	Units
ESD Voltage	$V_{ESD(HBM)}$	Human Body Model according to AEC-Q100-002	±11	kV

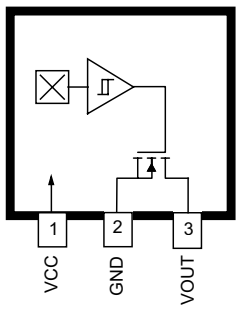
[4] ESD ratings provided are based on qualification per AEC-Q100 as an expected level of ESD robustness.

PINOUT DIAGRAMS AND TERMINAL LIST

(View from branded face)



3-pin SOT23W
(suffix LH)



3-pin SIP
(suffix UA)

Terminal List

Name	Description	Number	
		LH	UA
VCC	Connects power supply to chip	1	1
VOUT	Output from circuit	2	3
GND	Terminal for ground connection	3	2

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ELECTRICAL CHARACTERISTICS: Valid over full operating voltage and ambient temperature ranges for $T_J < T_{J(max)}$ and C_{BYP} = 0.1 µF, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit
SUPPLY AND STARTUP						
Supply Voltage	V_{CC}		3.3	–	24	V
Supply Current	I_{CC}	APS12000	1	2.2	4	mA
		APS12060	1	2.5	5	mA
Power-On Time [2]	t_{PO}	$V_{CC} \geq V_{CC}$(min)	–	180	350	µs
Power-On State [5]	POS	$V_{CC} \geq V_{CC}$(min), $t < t_{PO}$		High		–
Undervoltage Lockout [3]	V_{UVLO}	Voltage threshold at which the device is fully disabled during power down	–	2.25	–	V
UVLO Reset Time [3]	t_{POR}		–	100	–	µs
CHOPPER STABILIZATION AND OUTPUT MOSFET CHARACTERISTICS						
Chopping Frequency	f_C		–	800	–	kHz
Output Leakage Current [4]	I_{OUTOFF}	$V_{OUT(OFF)}$ = 12 V, T_A = –40°C to 85°C, output off, $V_{CC} \geq V_{CC(min)}$, $t > t_{PO}$	–	–	0.1	µA
Output Leakage Current	I_{OUTOFF}	$V_{OUT(OFF)}$ = 24 V, output off, $V_{CC} \geq V_{CC(min)}$, $t > t_{PO}$	–	–	1	µA
Output Leakage Current, Power-On [4][5]	$I_{OUTOFF(PO)}$	$V_{CC} \geq V_{CC(min)}$, $t < t_{PO}$	–	–	95	µA
Output Saturation Voltage	$V_{OUT(SAT)}$	Output on, I_{OUT} = 5 mA	–	100	500	mV
Output Off Voltage	$V_{OUT(OFF)}$		–	–	24	V
Output Rise Time [6][7]	t_r	C_L = 20 pF, $R_{PULL-UP}$ = 4.8 kΩ	–	0.2	2	µs
Output Fall Time [6][7]	t_f	C_L = 20 pF, $R_{PULL-UP}$ = 4.8 kΩ	–	0.1	2	µs
ON-BOARD PROTECTION						
Output Short-Circuit Current Limit	I_{OM}	Output on, $V_{PULL-UP} \leq$ 24 V	15	25	40	mA
Output Zener Clamp Voltage	$V_{Z(OUT)}$	I_{OUT} = 1.5 mA, T_A = 25°C	32	–	–	V
Supply Zener Clamp Voltage	V_Z	$I_{CC} = I_{CC}$(max) + 3 mA, T_A = 25°C	40	–	–	V
Reverse Battery Zener Clamp Voltage	V_{RZ}	I_{CC} = –5 mA, T_A = 25°C	–	–	–18	V
Reverse Battery Current	I_{RCC}	V_{CC} = –18 V, T_A = 25°C	–5	–	–	mA

[1] Typical data is at T_A = 25°C and V_{CC} = 12 V unless otherwise noted.
[2] Measured from $V_{CC} \geq$ 3.3 V to valid output.
[3] See Undervoltage Lockout section for operational characteristics.
[4] Guaranteed by device design and characterization.
[5] See Power-On Behavior section and Figure 4.
[6] C_L = oscilloscope probe capacitance.
[7] See Figure 2 - Definition of Output Rise and Fall Time.

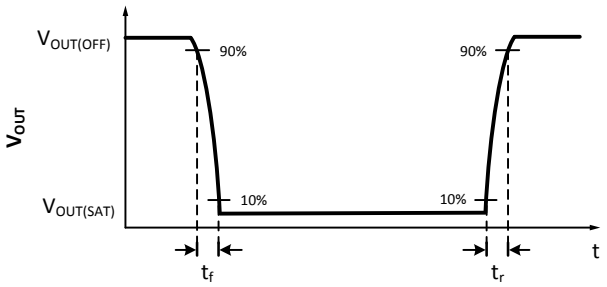


Figure 2: Definition of Output Rise and Fall Time

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MAGNETIC CHARACTERISTICS: Valid over full operating voltage and ambient temperature ranges for $T_J < T_{J(max)}$ and C_{BYP} = 0.1 µF, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit [2]
-0x OPTION						
Operate Point	B_{OPS}	-0x	10	35	70	G
Release Point	B_{RPS}	-0x	–70	–35	–10	G
Hysteresis	B_{HYS}	-0x	20	70	140	G
-1x OPTION						
Operate Point	B_{OPS}	-1x Option	50	95	135	G
Release Point	B_{RPS}	-1x Option	–135	–95	–50	G
Hysteresis	B_{HYS}	-1x Option	100	190	270	G
-2x OPTION						
Operate Point	B_{OPN}	-2x Option	120	150	200	G
Release Point	B_{RPN}	-2x Option	–200	–150	–120	G
Hysteresis	B_{HYS}	-2x Option	140	300	400	G
-3x OPTION						
Operate Point	B_{OPN}	-3x Option	205	280	355	G
Release Point	B_{RPN}	-3x Option	–355	–280	–205	G
Hysteresis	B_{HYS}	-3x Option	410	560	710	G

[1] Typical data are at T_A = 25°C and V_{CC} = 12 V unless otherwise noted.
[2] Magnetic flux density, B, is indicated as a negative value for north-polarity magnetic fields, and a positive value for south-polarity magnetic fields.

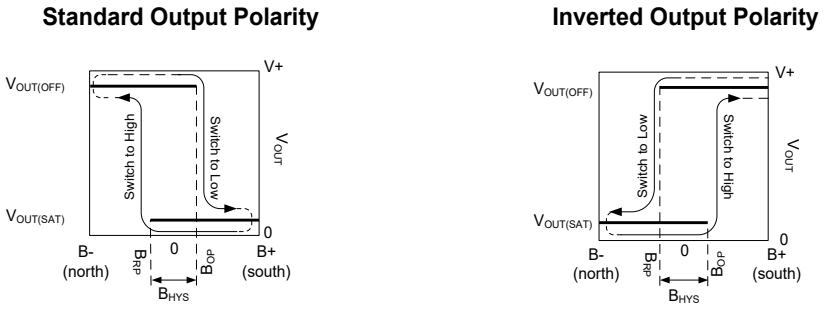


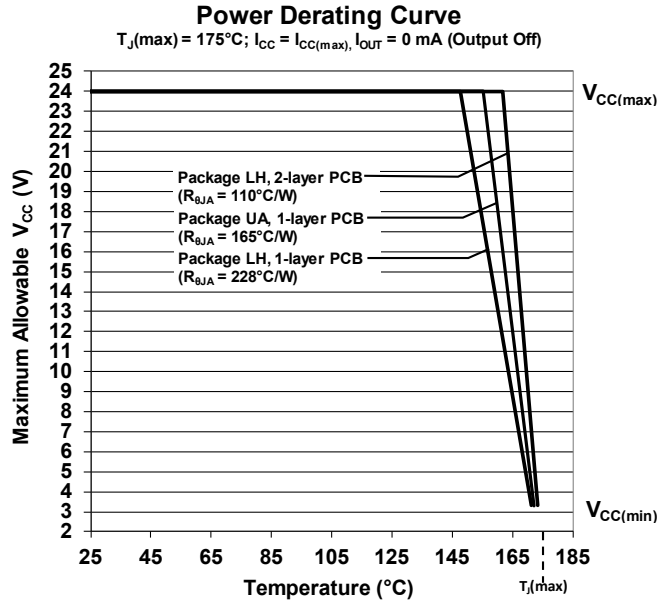
Figure 3: Hall Switch Output State vs. Magnetic Field

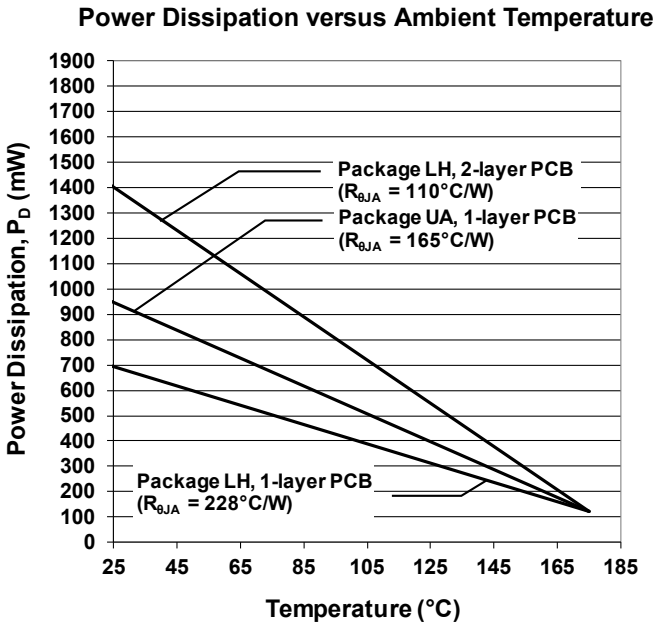
B- indicates increasing north polarity magnetic field strength, and B+ indicates increasing south polarity magnetic field strength.

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PACKAGE THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information.

Characteristic	Symbol	Test Conditions	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	Package LH, 1-layer PCB with copper limited to solder pads	228	°C/W
		Package LH, 2-layer PCB with 0.463 in^2 of copper area each side connected by thermal vias	110	°C/W
		Package UA, 1-layer PCB with copper limited to solder pads	165	°C/W

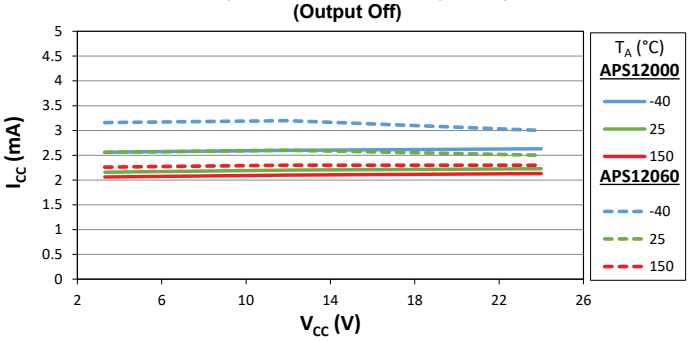




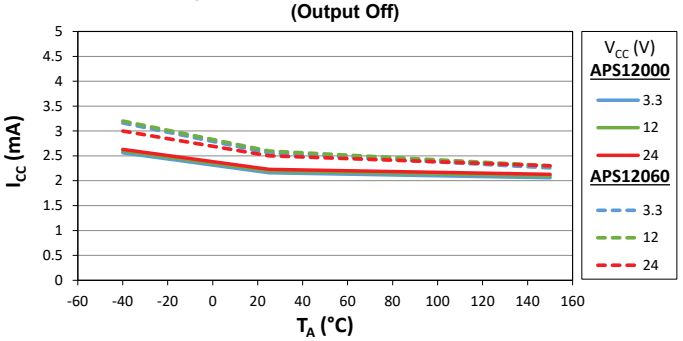
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CHARACTERISTIC PERFORMANCE DATA
Electrical Characteristics

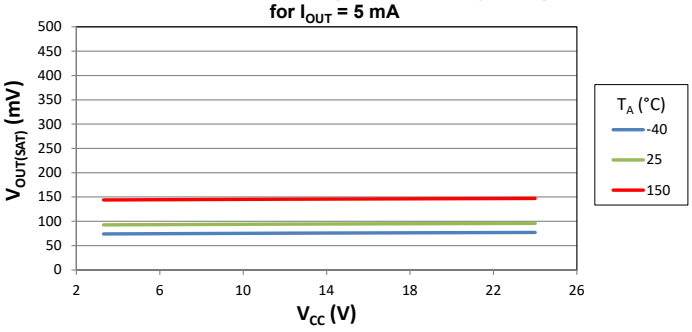
Supply Current versus Supply Voltage (Output Off)



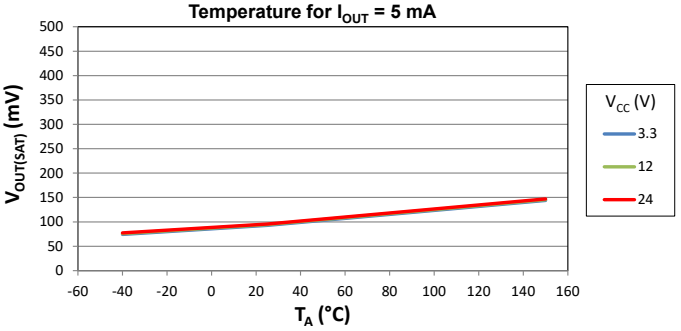
Supply Current versus Ambient Temperature (Output Off)



Output Saturation Voltage versus Supply Voltage for I_{OUT} = 5 mA

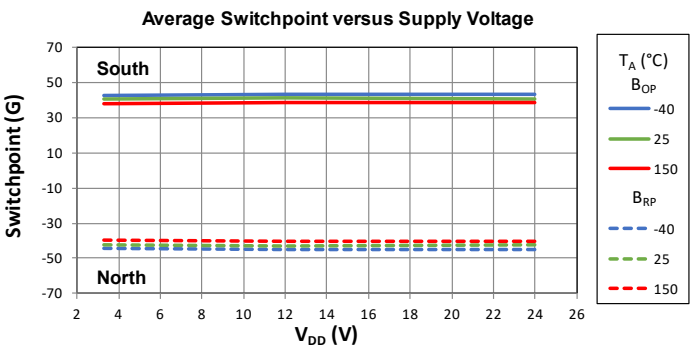


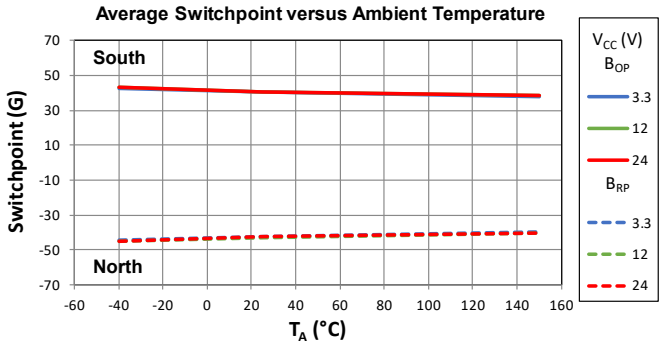
Output Saturation Voltage versus Ambient Temperature for I_{OUT} = 5 mA

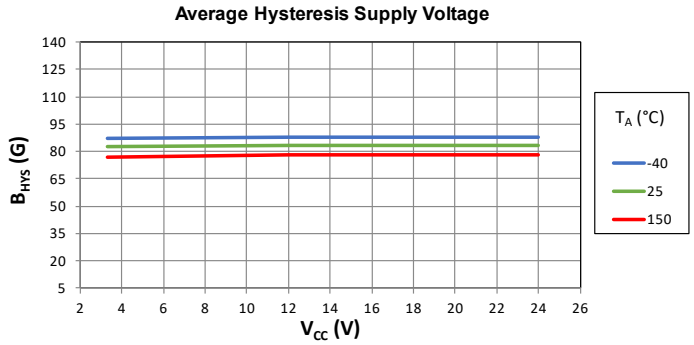


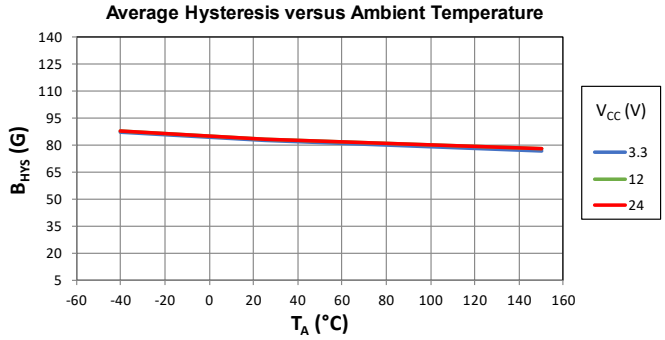
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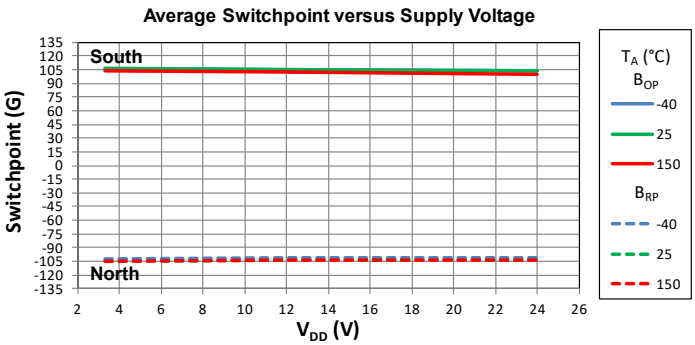


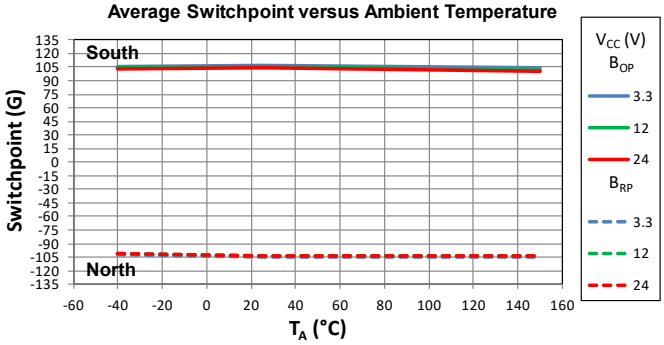


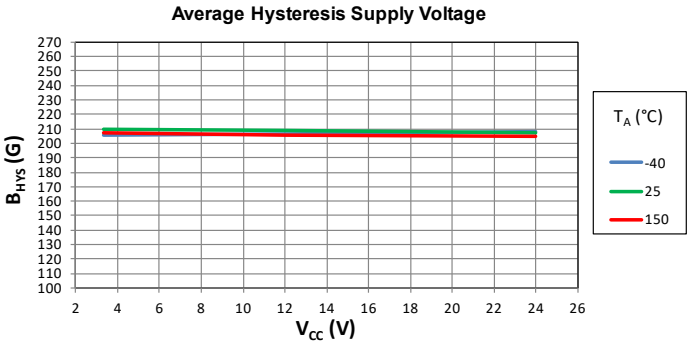


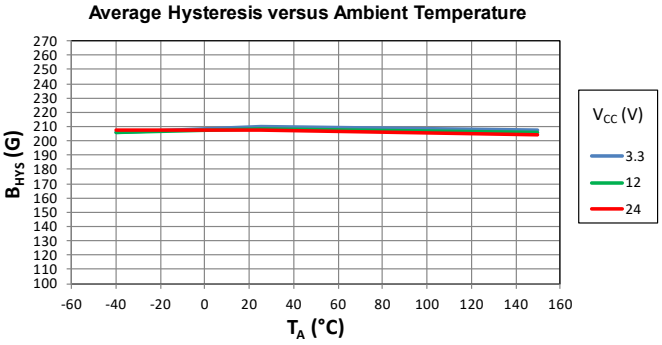
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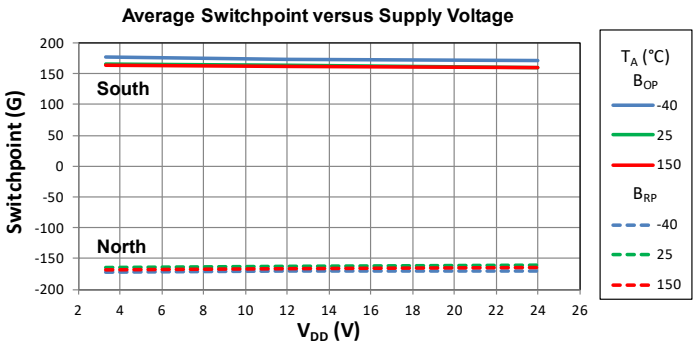


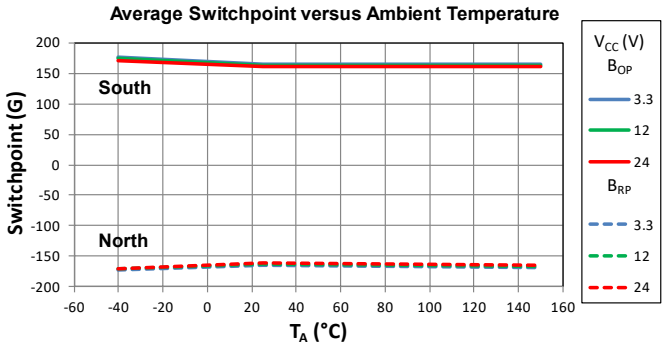


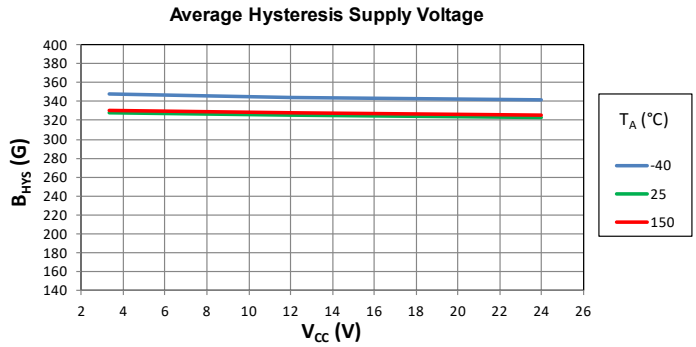


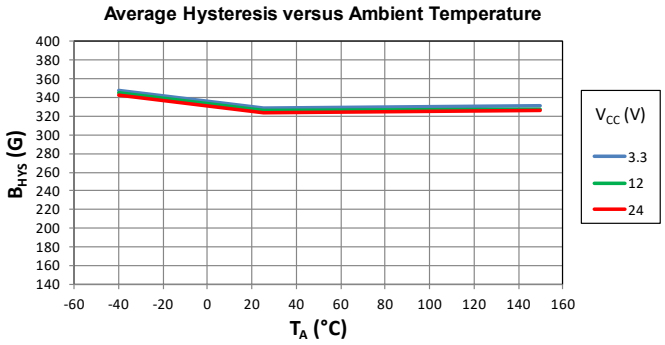
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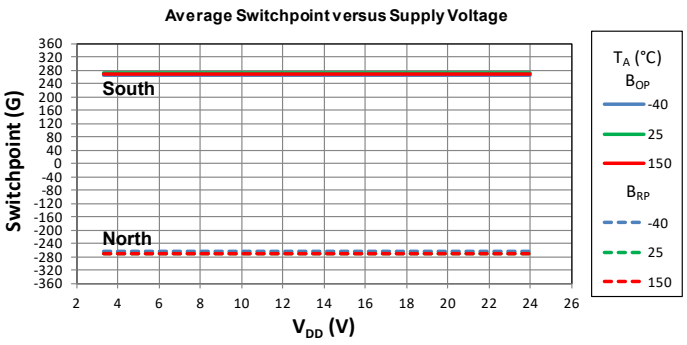


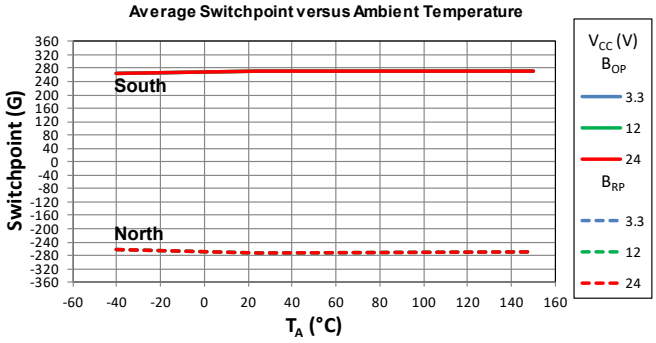


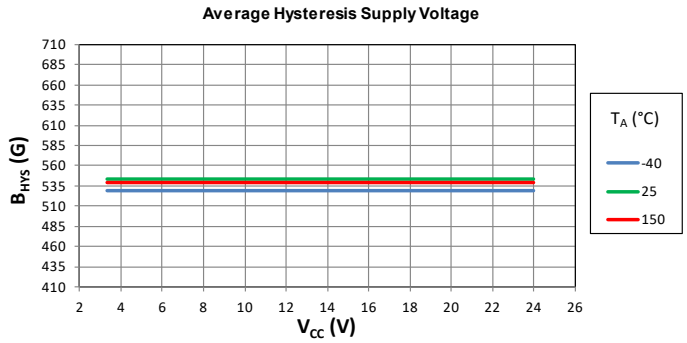


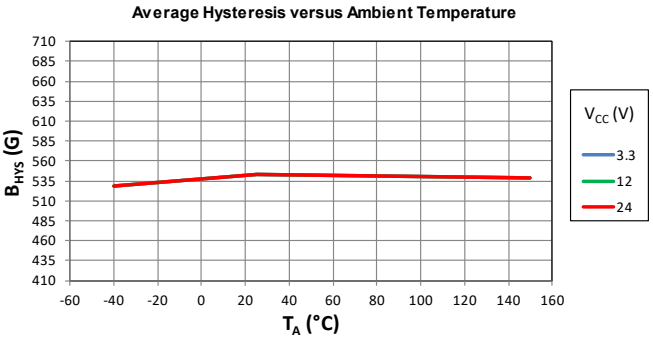
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CHARACTERISTIC PERFORMANCE DATA
Magnetic Characteristics
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FUNCTIONAL DESCRIPTION

Power-On Behavior

Device power-on begins when the supply voltage reaches V_{CC}(min). During the power-on time, t_{PO}, the device output is off with the exception of the leakage current, $I_{OUTOFF(PO)}$. Use of a large pull-up resistor, $R_{PULL-UP}$ (see Figure 6), can influence the Power-On State (POS) voltage level on the output pin during t_{ON}. The output voltage level during the POS is a function of the pull-up resistor and pull-up voltage. The level can be determined by subtracting the voltage drop created by $R_{PULL-UP}$ and $I_{OUTOFF(PO)}$ from the pull-up voltage. To retain a power-on output voltage level above $V_{PULL-UP}/2$, a pull-up resistor less than or equal to 20 kΩ is recommended. After power-on is complete and the power-on time has elapsed, the device output will correspond with the applied magnetic field for $B > B_{OP}$ and $B < B_{RP}$. Powering-on the device in the hysteresis range (less than B_{OP} and higher than B_{RP}) will cause the device output to remain off. A valid output state is attained after the first excursion beyond B_{OP} or B_{RP}.

Undervoltage Lockout Operation

The APS12000 and APS12060 have an internal diagnostic to check the voltage supply (an undervoltage lockout regulator). When the supply voltage falls below the undervoltage lockout voltage threshold, V_{UVLO}, the device enters reset, where the output state becomes undefined until V_{CC} is increased to V_{CC} (min). Once the V_{CC} (min) threshold is reached, the power-on sequence begins and the output will correspond with the applied magnetic field for $B > B_{OP}$ and $B < B_{RP}$ after t_{POR} has elapsed. In the case the supply voltage does not return to these operational levels, or if the applied magnetic field is within the hysteresis range, the output will remain in the power-on state. See Figure 4 for an example of the undervoltage lockout behavior.

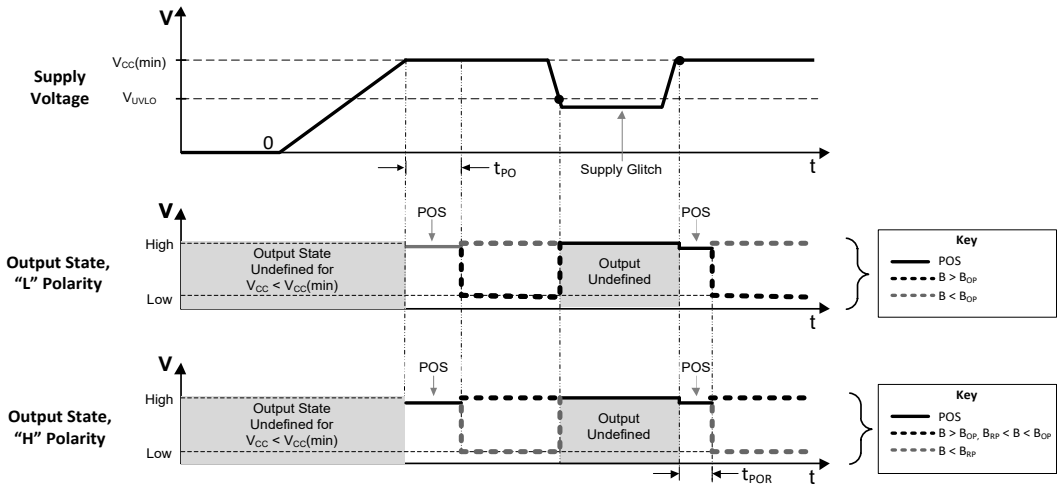


Figure 4: Power-On and Undervoltage Lockout Behavior

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Functional Safety

The APS12000 and APS12060 were designed and developed in accordance with the international standard for automotive functional safety, ISO 26262. These products achieve an ASIL (automotive safety integrity level) rating of ASIL A according to the standard. The APS12000 and APS12060 are both classified as a SEooC (safety element out of context) and can be easily integrated into safety-critical systems requiring higher ASIL ratings that incorporate external diagnostics or use measures such as redundancy. Safety documentation will be provided to support and guide the integration process. For further information, contact your local FAE for A^2-SIL™ documentation: www.allegromicro.com/ASIL.

Operation

The APS12000 and APS12060 are integrated Hall-effect sensor ICs with an open-drain output. The output polarity of the -xL configuration device is Low for a south-polarity magnetic field, $B > B_{OP}$, and High for a north polarity magnetic field, $B < B_{RP}$. The -xH variant is complementary, in that for this device the output goes High for a south polarity magnetic field, $B > B_{OP}$, and Low for a north polarity magnetic field, $B < B_{RP}$. The open-drain output is an NMOS transistor that actuates in response to a magnetic field. The direction of the applied magnetic field is perpendicular to the branded face for the APS12000, and parallel with the branded face for the APS12060; see Figure 5 for an illustration. The devices are offered in two packages: the UA package, a 3-pin through-hole mounting configuration, or in the LH package, a 3-pin surface-mount configuration. See the Selection Guide for a complete list of available options.

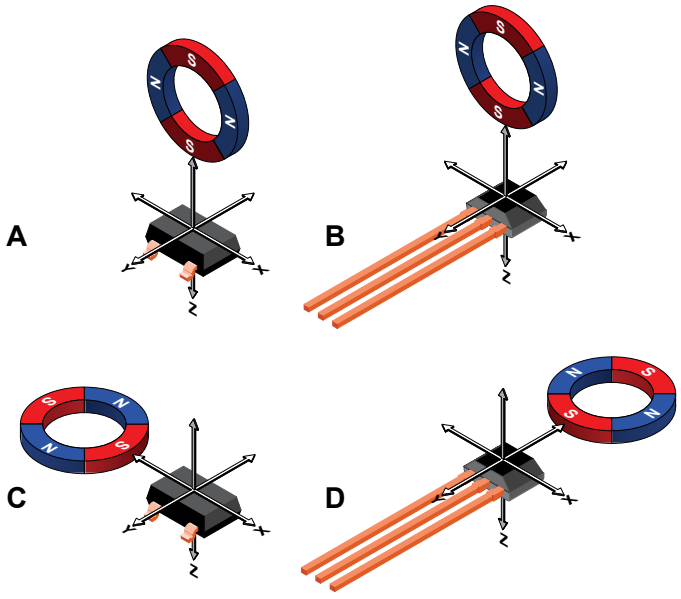


Figure 5: Magnetic Sensing Orientations
APS12000 LH (Panel A), APS12000 UA (Panel B), APS12060 LH (Panel C), and APS12060 UA (Panel D)

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Applications

It is strongly recommended that an external bypass capacitor be connected (in close proximity to the Hall element) between the supply and ground of the device to guarantee correct performance under harsh environmental conditions and to reduce noise from internal circuitry. As is shown in Figure 6: Typical and Enhanced Protection Application Circuits, a 0.1 µF capacitor is required.

In applications where the APS12000 or APS12060 receives its power from an unregulated source such as a car battery, or where greater immunity is required, additional measures may be employed. Specifications for such transients will vary, so protection circuit design should be optimized for each application. For example, the circuit shown in Figure 6 includes an optional series resistor and output capacitor which improves performance during powered ESD testing (ISO 10605) and bulk current injection testing (ISO 11452-4).

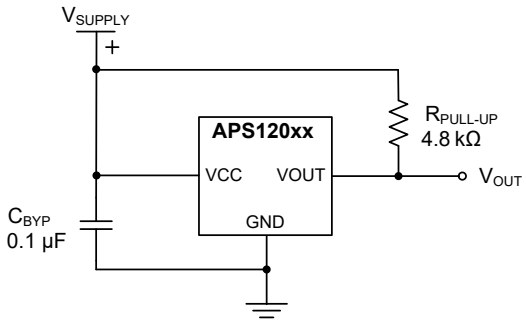
Extensive applications information for Hall-effect devices is available in:

- *Hall-Effect IC Applications Guide, AN27701,*
- *Hall-Effect Devices: Guidelines for Designing Subassemblies Using Hall-Effect Devices AN27703.1*
- *Soldering Methods for Allegro's Products – SMD and Through-Hole, AN26009*
- Functional Safety Challenges to the Automotive Supply Chain (https://www.allegromicro.com/en/insights-and-innovations/technical-documents/general-semiconductor-information/functional-safety-challenges-automotive-supply-chain)

All are provided on the Allegro website:

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Typical Applications Circuit



Enhanced Protection Circuit

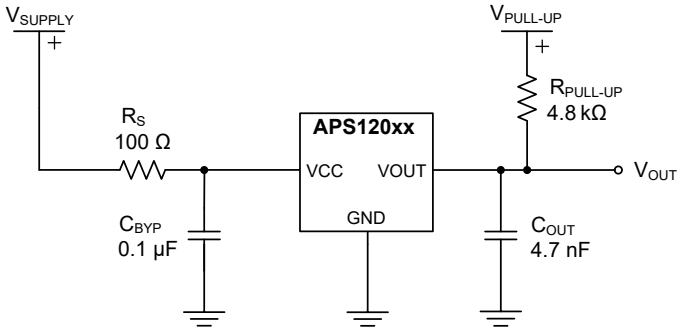


Figure 6: Typical and Enhanced Protection Application Circuits

Recommended $R_{PULL-UP} \leq 20$ kΩ.
See Power-On Behavior section.

Vertical Hall-Effect Sensor Linear Tools

System design and magnetic sensor evaluation often require an in-depth look at the overall strength and profile generated by a magnetic field input. To aid in this evaluation, Allegro MicroSystems provides a high-accuracy linear output tool capable of reporting the nonperpendicular magnetic field by means of a vertical Hall-effect sensor IC equipped with a calibrated analog output. For further information, contact your local Allegro field applications engineer or sales representative.

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CHOPPER STABILIZATION

A limiting factor for switch point accuracy when using Hall-effect technology is the small signal voltage developed across the Hall plate. This voltage is proportionally small relative to the offset that can be produced at the output of the Hall sensor. This makes it difficult to process the signal and maintain an accurate, reliable output over the specified temperature and voltage range. Chopper stabilization is a proven approach used to minimize Hall offset.

The technique, dynamic quadrature offset cancellation, removes key sources of the output drift induced by temperature and package stress. This offset reduction technique is based on a signal modulation-demodulation process. Figure 7: Model of Chopper Stabilization Circuit (Dynamic Offset Cancellation) illustrates how it is implemented.

The undesired offset signal is separated from the magnetically induced signal in the frequency domain through modulation. The subsequent demodulation acts as a modulation process for the offset causing the magnetically induced signal to recover its original spectrum at baseband while the DC offset becomes a high-frequency signal. Then, using a low-pass filter, the signal passes while the modulated DC offset is suppressed. Allegro's innovative chopper-stabilization technique uses a high-frequency clock.

The high-frequency operation allows a greater sampling rate that produces higher accuracy, reduced jitter, and faster signal processing. Additionally, filtering is more effective and results in a lower noise analog signal at the sensor output. Devices such as the APS12000 and APS12060 that use this approach have an extremely stable quiescent Hall output voltage, are immune to thermal stress, and have precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process which allows the use of low offset and low noise amplifiers in combination with high-density logic and sample-and-hold circuits.

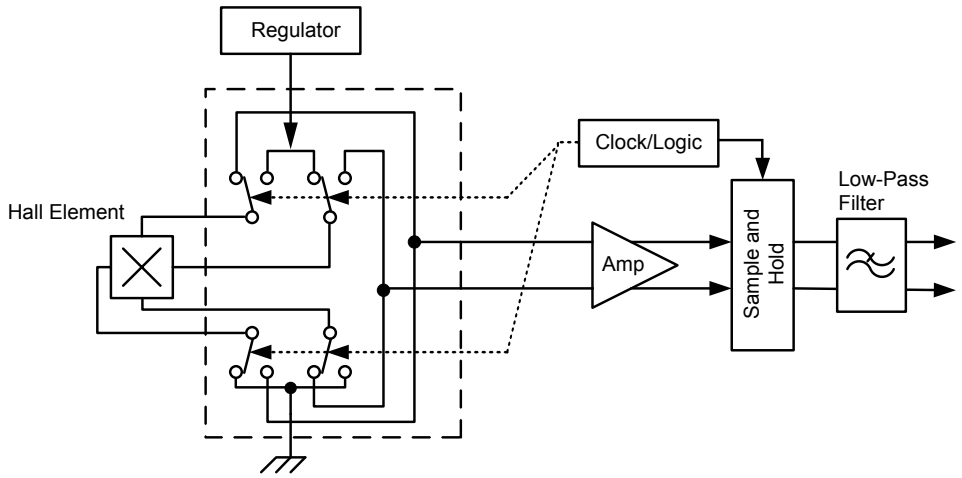


Figure 7: Model of Chopper Stabilization Circuit (Dynamic Offset Cancellation)

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POWER DERATING

The device must be operated below the maximum junction temperature, $T_{J(max)}$. Reliable operation may require derating supplied power and/or improving the heat dissipation properties of the application.

Thermal Resistance, $R_{\theta JA}$ (junction to ambient), is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to ambient air. $R_{\theta JA}$ is dominated by the Effective Thermal Conductivity, K, of the printed circuit board which includes adjacent devices and board layout. Thermal resistance from the die junction to case, $R_{\theta JC}$, is a relatively small component of $R_{\theta JA}$. Ambient air temperature, T_A, and air motion are significant external factors in determining a reliable thermal operating point.

The following three equations can be used to determine operation points for given power and thermal conditions:

$$P_D = V_{IN} \times I_{IN} \text{ (1)}$$

$$\Delta T = P_D \times R_{\theta JA} \text{ (2)}$$

$$T_J = T_A + \Delta T \text{ (3)}$$

Determining Junction Temperature

For example, given common conditions: T_A = 25°C, V_{CC} = 12 V, I_{CC} = 2.5 mA, $V_{OUT(SAT)}$ = 100 mV, I_{OUT} = 5 mA, and $R_{\theta JA}$ = 165°C/W, then:

$$P_D = (V_{CC} \times I_{CC}) + (V_{OUT} \times I_{OUT}) =$$

$$(12\ V \times 2.5\ mA) + (100\ mV \times 5\ mA) =$$

$$30\ mW + 0.5\ mW = 30.5\ mW$$

$$\Delta T = P_D \times R_{\theta JA} = 30.5\ mW \times 165°C/W = 5°C$$

$$T_J = T_A + \Delta T = 25°C + 5°C = 30°C$$

Determining Maximum V_{CC}

For a given ambient temperature (T_A), the maximum allowable power dissipation as a function of V_{CC} can be calculated. $P_{D(max)}$, represents the maximum allowable power level without exceeding $T_{J(max)}$, at a selected $R_{\theta JA}$ and T_A.

Example: V_{CC} estimation using the conditions $R_{\theta JA}$ = 228°C/W, $T_{A(max)}$ = 150°C, $T_{J(max)}$ = 175°C, $V_{CC(max)}$ = 24 V, $I_{CC(max)}$ = 5 mA, V_{OUT} = 500 mV, and I_{OUT} = 20 mA (output on), calculate the maximum allowable power level, P_D(max), first using equation 3:

$$\Delta T_{(max)} = T_{J(max)} - T_A = 175°C - 150°C = 25°C$$

This provides the allowable increase to T_J resulting from internal power dissipation. Then, using equation 2 first for the output as shown below:

$$P_{D(VOUT)} = V_{OUT} \times I_{OUT} = 500\ mV \times 20\ mA = 10\ mW$$

Then, for the V_{CC} supply:

$$P_{D(VCC)} = V_{CC} \times I_{CC} = 24\ V \times 5\ mA = 120\ mW$$

Combine the power dissipated by the device pins:

$$P_{D(total)} = (P_{D(VOUT)} + P_{D(VCC)})$$

$$P_{D(total)} = (10\ mW + 120\ mW) = 130\ mW$$

Next, solve for the maximum allowable V_{CC} for the given conditions using equation 1:

$$V_{CC(est)} = P_{D(total)} \div (I_{CC} + I_{OUT})$$

$$130\ mW \div (5\ mA + 20\ mA)$$

$$V_{CC(est)} = 130\ mW \div 25\ mA = 5.2\ V$$

The result indicates that, at T_A, the application and device can dissipate adequate amounts of heat at voltages ≤ $V_{CC(est)}$.

If the application requires $V_{CC} > V_{CC(est)}$ then $R_{\theta JA}$ must by improved. This can be accomplished by adjusting the layout, PCB materials, or by controlling the ambient temperature.

Determining Maximum T_A

In cases where the $V_{CC(max)}$ level is known, and the system designer would like to determine the maximum allowable ambient temperature, $T_{A(max)}$, the calculations can be reversed.

For example, in a worst-case scenario with conditions $V_{CC(max)}$ = 24 V, $I_{CC(max)}$ = 5 mA, V_{OUT} = 500 mV, $I_{OUT(max)}$ = 15 mA, and $R_{\theta JA}$ = 228°C/W, for the LH package using equation 1, the largest possible amount of dissipated power is:

$$P_D = V_{IN} \times I_{IN}$$

$$P_D = P_{D(VOUT)} + P_{D(VCC)} = 500\ mV \times 15\ mA + 24\ V \times 5\ mA$$

$$P_D = 7.5\ mW + 120\ mW = 127.5\ mW$$

Then, by rearranging equation 3:

$$T_{A(max)} = T_{J(max)} - \Delta T$$

$$T_{A(max)} = 175°C - (127.5\ mW \times 228°C/W)$$

$$T_{A(max)} = 175°C - 29.1°C = 145.9°C$$

Finally, note that the $T_{A(max)}$ rating of the device is 150°C and performance is not guaranteed above this temperature for any power level.

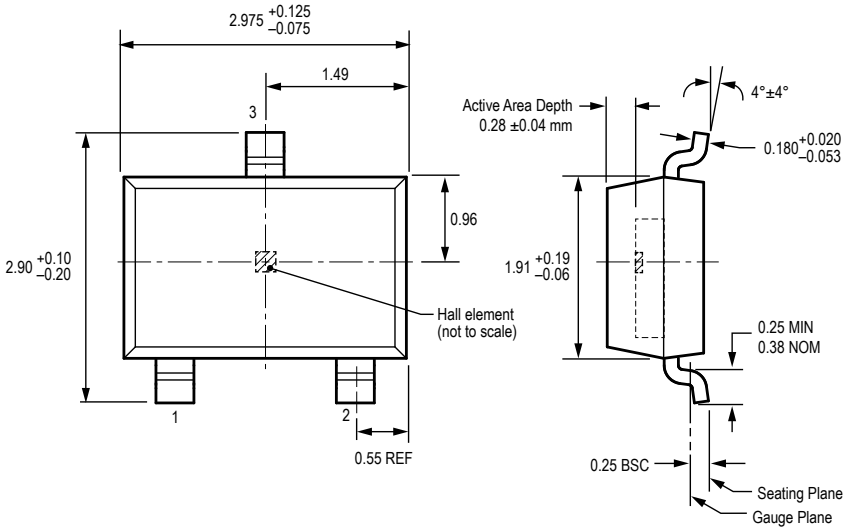
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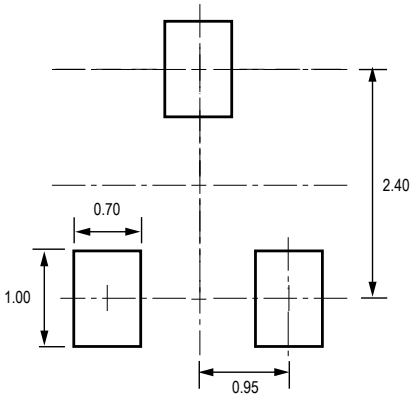
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Package LH, 3-Pin SMD (SOT23W)
APS12000

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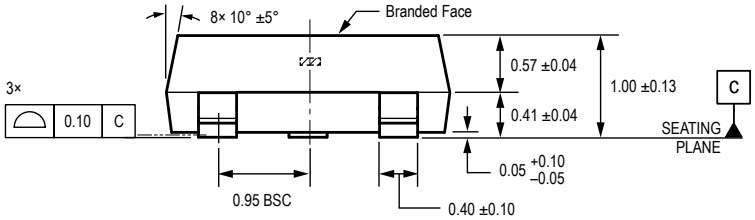
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Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

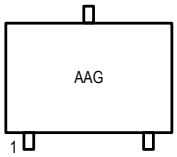




PCB Layout Reference View

All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances





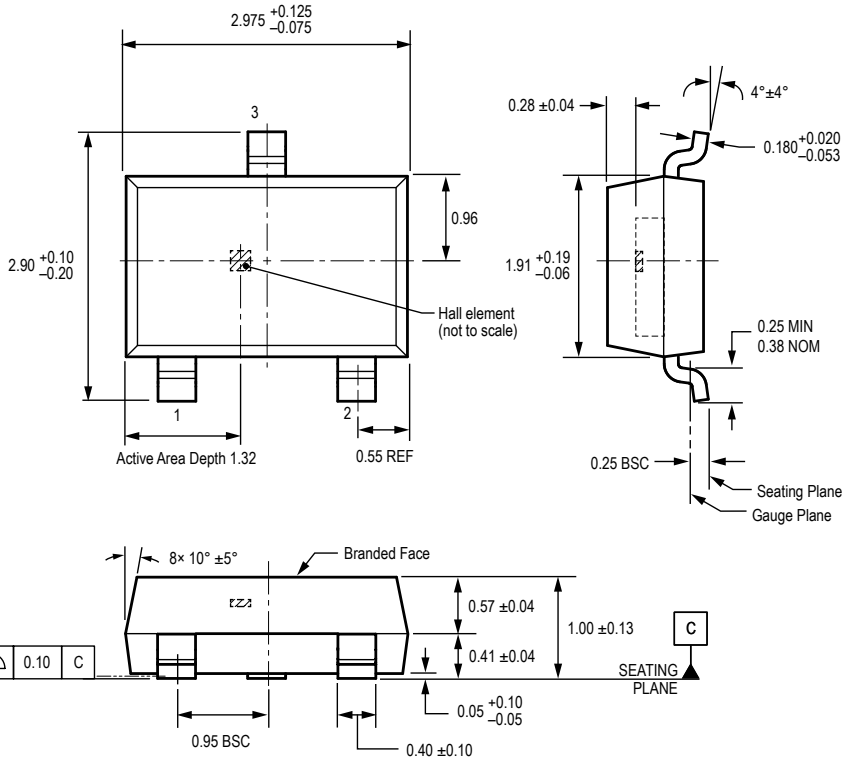
Standard Branding Reference View

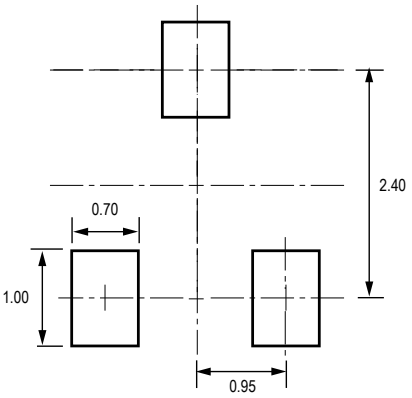
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Package LH, 3-Pin SMD (SOT23W)
APS12060

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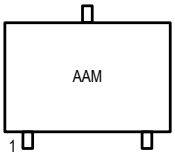
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Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown





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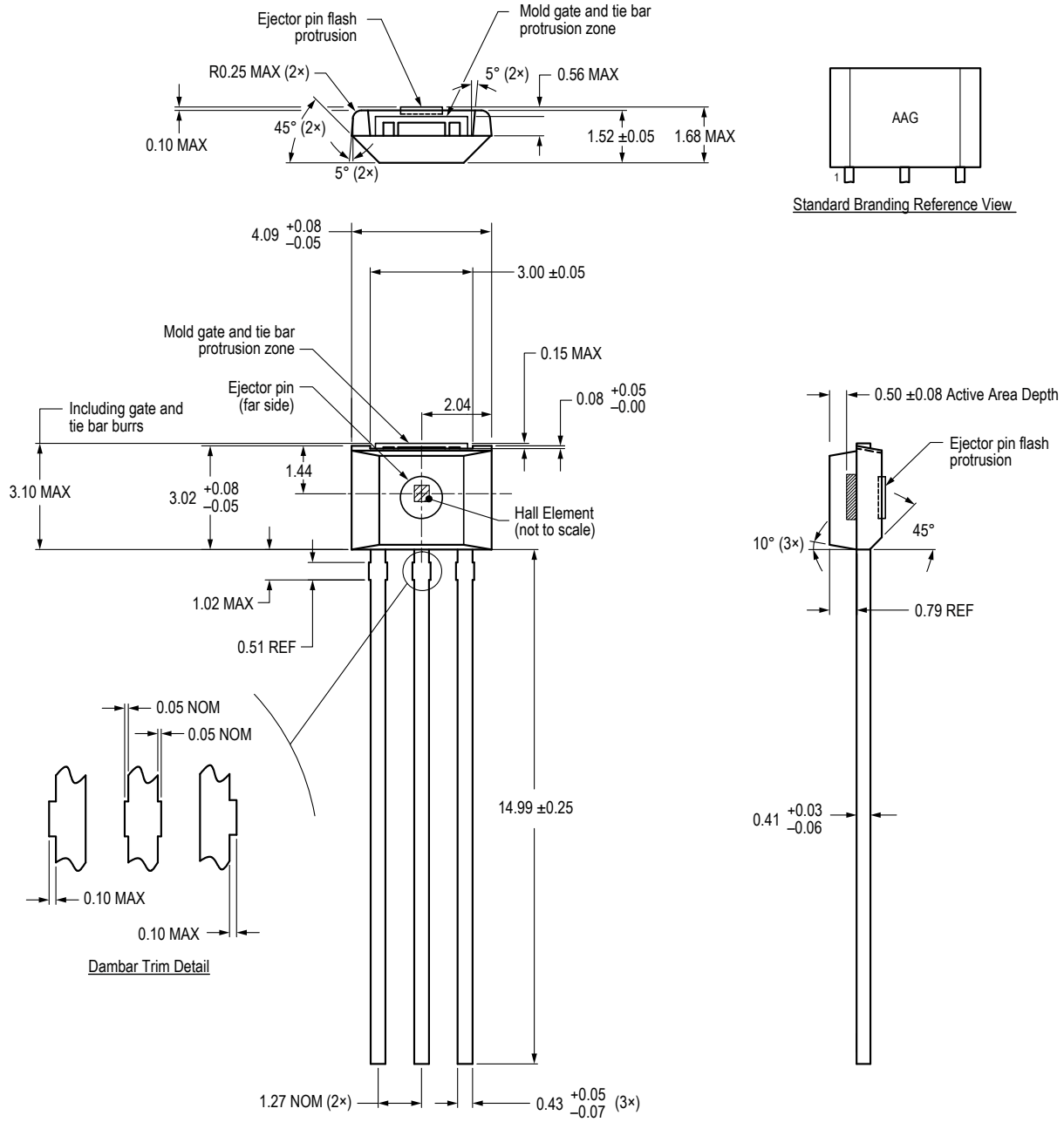
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Package UA, 3-Pin SIP
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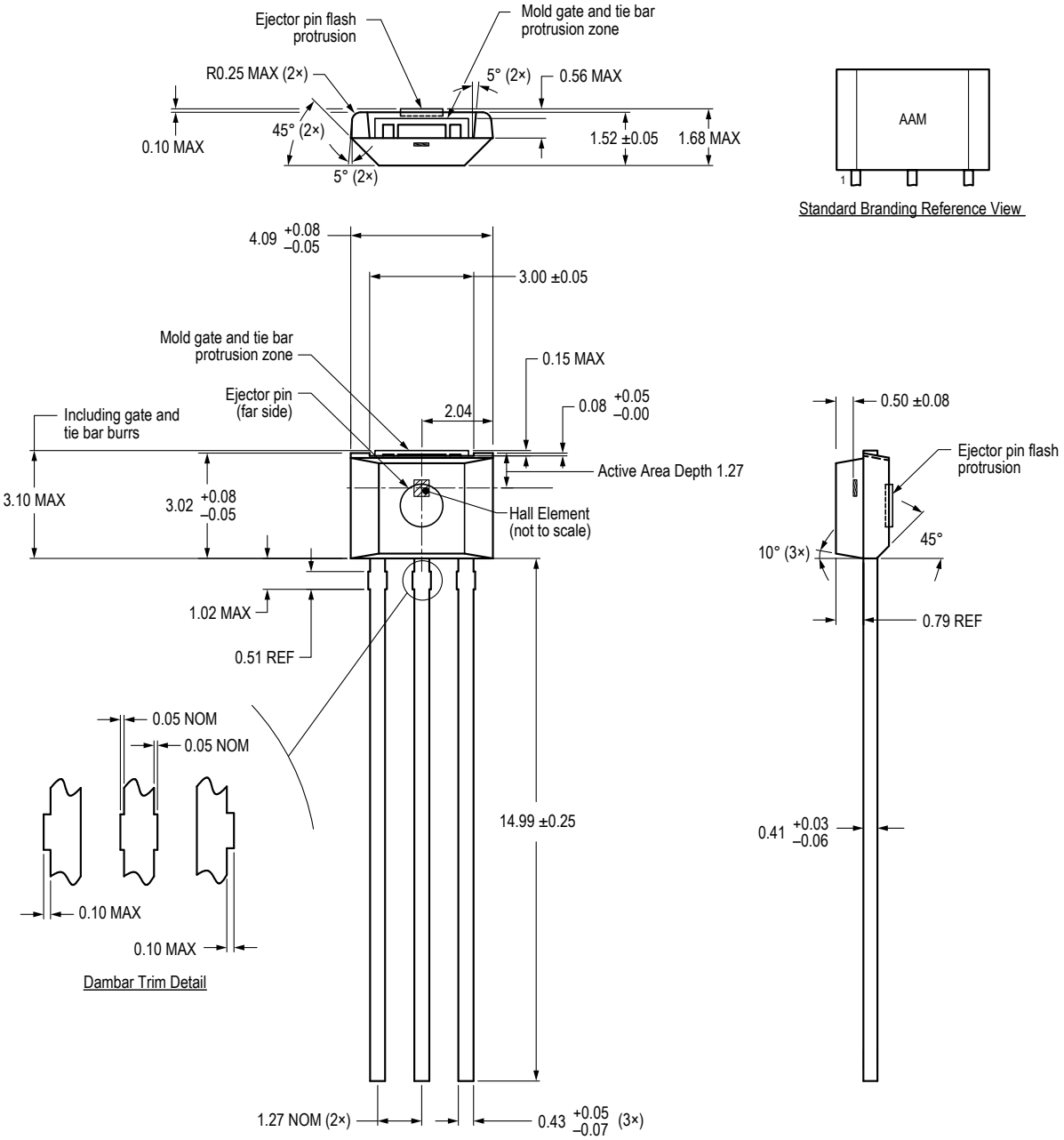


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Package UA, 3-Pin SIP
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Revision History

Number	Date	Description
–	September 13, 2018	Initial preliminary release
1	February 5, 2019	Updated maximum junction temperature (page 1 and 3), Selection Guide table (page 2), Undervoltage Lockout (page 4), Operate Point (page 5, -0x option minimum value), Power Derating Curve and Power Dissipation versus Ambient Temperature plots (page 6), Undervoltage Lockout description (page 11), Figure 4 (page 11), Applications section (page 13), and package branding (pages 16 and 17). Added Magnetic Characteristics plots (page 9-10) and APS12000 part variant (all pages).
2	April 4, 2019	Updated Selection Guide (page 2), Character Performance Data plot labels (pages 8-10) , and Power Derating section (page 15).
3	March 10, 2020	Updated Selection Guide (page 2), Added -3x option magnetic plots (page 11).
4	May 12, 2020	Added “(pending confirmation)” to ASIL references.
5	June 7, 2022	Updated package drawings (pages 17-20).
6	May 30, 2024	Fixed broken link (page 14).
7	December 3, 2024	Removed “(pending confirmation)” to ASIL references (pages 1 and 13).
8	February 24, 2026	Updated ASIL branding and text (pages 1, 2, and 13).

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