Brief Description

The ZSC31150 is a CMOS integrated circuit for highly accurate amplification and sensor-specific correction of bridge sensor signals. Digital compensation of sensor offset, sensitivity, temperature drift, and non-linearity is accomplished via an internal 16-bit RISC microcontroller running a correction algorithm, with calibration coefficients stored in an EEPROM.

The ZSC31150 is adjustable to nearly all bridge sensor types. Measured values are provided at the analog voltage output or at the digital ZACwire™ and I²C interface. The digital interface can be used for a simple PC-controlled calibration procedure in order to program a set of calibration coefficients into an on-chip EEPROM. A specific sensor and a ZSC31150 can be mated digitally: fast, precise, and without the cost overhead associated with trimming by external devices or a laser.

Features

- Digital compensation of sensor offset, sensitivity, temperature drift, and non-linearity
- Adjustable to nearly all bridge sensor types
- Analog gain of up to 420
- Output options: ratiometric analog voltage output (5% to 95% maximum, 12.4-bit resolution) or ZACwire™ (digital one-wire-interface)
- Temperature compensation: internal or external diode, bridge resistance, thermistor
- Sensor biasing by voltage or constant current
- Sample rate: up to 7.8kHz
- High voltage protection up to 33V
- Supply current: max. 5.5mA
- Reverse polarity and short-circuit protection
- Wide operation temperature depending on part number: up to -40°C to +150°C
- Traceability by user-defined EEPROM entries
- Safety and diagnostic functions

Benefits

- No external trimming components required
- Only a few external protection devices needed
- PC-controlled configuration and single pass calibration via I²C or ZACwire™ interface: simple, cost efficient, quick, and precise
- End-of-line calibration via I²C or ZACwire™ interface
- High accuracy (0.25% FSO at -25 to 85°C; 0.5% FSO at -40°C to 125°C)
- Excellent EMC/ESD robustness and AEC-Q100 qualification

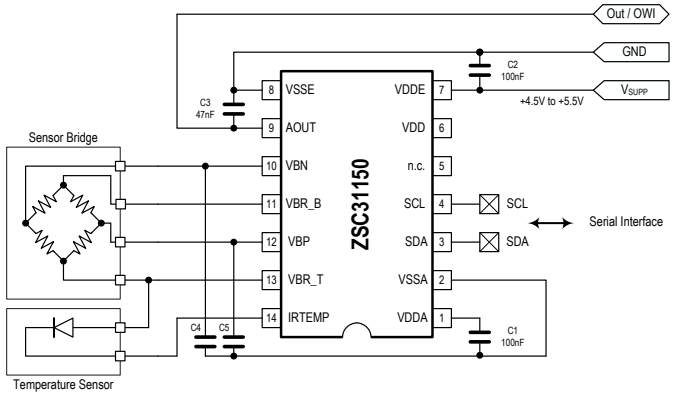
Available Support

- Evaluation Kits
- Application Notes
- Mass Calibration System

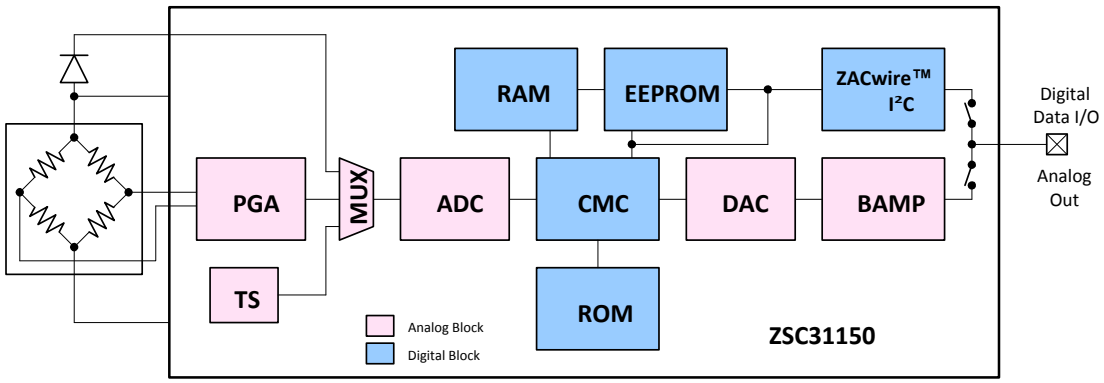
Physical Characteristics

- Supply voltage: 4.5V to 5.5V
- Operation temperature: -40°C to 125°C (-40°C to +150°C extended temperature range)
- Available as 14-DFN (5 × 4 mm; wettable flanks), SSOP14, and die

ZSC31150 Application Circuit



ZSC31150 Block Diagram



Ordering Information

Sales Code	Description	Package
ZSC31150GE	ZSC31150 Die – Temperature range: -40°C to +150°C	Unsawn on Wafer: add "B" to sales code Sawn on Wafer Frame: add "C" Waffle Pack: add "D"
ZSC31150GEG2-R	ZSC31150 14-DFN (5 × 4 mm; wettable flanks) – Temperature range: -40°C to 150°C	Tape and Reel
ZSC31150GAG2-R	ZSC31150 14-DFN (5 × 4 mm; wettable flanks) – Temperature range: -40°C to 125°C	Tape and Reel
ZSC31150GAB	ZSC31150 Die – Temperature range: -40°C to +125°C	Unsawn on Wafer
ZSC31150GAC	ZSC31150 Die – Temperature range: -40°C to +125°C	Sawn on Wafer Frame
ZSC31150GEG1	ZSC31150 14-SSOP – Temperature range: -40°C to +150°C	Tube: add "-T" to sales code Tape & Reel: add "-R"
ZSC31150GLG1	ZSC31150 14-SSOP – Temperature range: -40°C to +150°C (Long life: 5000h @150°C)	
ZSC31150GAG1	ZSC31150 14-SSOP – Temperature range: -40°C to +125°C	
ZSC31150KITV1P2	ZSC31150 SSC Evaluation Kit V1.2: Three interconnecting boards, five ZSC31150 SSOP14 samples, USB cable (software can be downloaded from product page at www.IDT.com/ZSC31150)	
ZSC31150MCSV1P1	Modular Mass Calibration System (MSC) V1.1 for ZSC31150: MCS boards, cable, connectors (software can be downloaded from product page)	

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1. Electrical Characteristics

1.1 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. The ZSC31150 might not function or be operable above the recommended operating conditions. Stresses exceeding the absolute maximum ratings might also damage the device. In addition, extended exposure to stresses above the recommended operating conditions might affect device reliability. IDT does not recommend designing to the "Absolute Maximum Ratings."

Parameters apply in operation temperature range and without time limitations.

Table 1.1 Absolute Maximum Ratings

No.	Parameter	Symbol	Conditions	Min	Max	Unit
1.1.1	Supply voltage [a]	VDDE	To VSSE.	-33	33	VDC
1.1.2	Potential at the AOUT pin [a]	V_{OUT}	Relative to VSSE.	-33	33	VDC
1.1.3	Analog supply voltage [a]	VDDA	Relative to VSSA. VDDE - VDDA < 0.35V	-0.3	6.5	VDC
1.1.4	Voltage at all analog and digital IO pins	V_{A_IO} V_{D_IO}	Relative to VSSA.	-0.3	VDDA + 0.3	VDC
1.1.5	Storage temperature	T_{STG}		-55	150	°C

[a] Refer to the *ZSC31150 Technical Note – High Voltage Protection* for specification and detailed conditions for high voltage protection.

1.2 Operating Conditions

All voltages are related to VSSA. See important table notes at the end of the table.

Table 1.2 Operating Conditions

No.	Parameter	Symbol	Conditions	Min	Typ	Max	Unit
1.2.1	TQE ambient temperature range for part numbers ZSC31150x***E***xx [a]	T_{AMB_TQE}	TQE	-40		150	°C
	TQA ambient temperature range for part numbers ZSC31150x***A***xx [b]	T_{AMB_TQA}	TQA	-40		125	°C
	TQI ambient temperature range for advanced performance [b]	T_{AMB_TQI}	TQI	-25		85	°C
1.2.2	Supply voltage	VDDE		4.5	5.0	5.5	VDC
1.2.3	Bridge resistance—Bridge Voltage Mode [b], [c]	R_{BR_V}		2		25	kΩ
1.2.4	Bridge resistance—Bridge Current Excitation Mode [b], [c]	R_{BR_C}	See specification 1.2.6 for I_{BR_MAX}			10	kΩ
1.2.5	Current reference resistor [b],[d]	R_{IBR}	I_{BR} = VDDA / (16 * R_{IBR})	0.07 * R_{BR}			kΩ
1.2.6	Maximum bridge current	I_{BR_MAX}				2	mA

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No.	Parameter	Symbol	Conditions	Min	Typ	Max	Unit
1.2.7	Maximum bridge top voltage	V_{BR_TOP}				($^{15}/_{16}$ * VDDA) - 0.3	V
1.2.8	TC current reference resistor [b]	TC R_{IBR}	Behavior influences current generated		50		ppm/K

[a] Refer to the temperature profile description in the *ZSC31150 Technical Note – Die and Package Specifications* for operation in temperature range > 125°C.

[b] No measurement in mass production; parameter is guaranteed by design and/or quality observation.

[c] Symmetric behavior and identical electrical properties (especially with regard to the low pass characteristic) of both sensor inputs of the ZSC31150 are required. Unsymmetrical conditions of the sensor and/or external components connected to the sensor input pins of ZSC31150 can generate a failure in signal operation.

[d] See application circuit components in Table 3.1.

1.3 Electrical Parameters

All parameter values are valid for operating conditions specified in section 1.2 except as noted. All voltages related to VSSA. See important table notes at the end of the table.

Table 1.3 Electrical Parameters

No.	Parameter	Symbol	Conditions	Min	Typ	Max	Unit
1.3.1	**Supply Current and System Operation Conditions**						
1.3.1.1	Supply current	I_S	Without bridge and load current; T_{AMB_TQA}; $f_{CLK} \leq 3MHz$			5.5	mA
1.3.1.2	Clock frequency [a]	f_{OSC}	Guaranteed adjustment range (see the *ZSC31150 Functional Description* for details); T_{AMB_TQA}	2	3	4	MHz
1.3.2	**Analog Front-End (AFE) Characteristics**						
1.3.2.1	Input span	V_{IN_SP}	Analog gain: 420 to 2.8	1		275	mV/V
1.3.2.2	Analog offset compensation range		Depends on gain adjust; refer to section 2.3.1	-300		300	% V_{IN_SP}
1.3.2.3	Parasitic differential input offset current [a]	I_{IN_OFF}	Within T_{AMB_TQE}	-10		10	nA
			Within T_{AMB_TQI}	-2		2	nA
1.3.2.4	Common mode input range	V_{IN_CM}	Depends on gain adjustment; no XZC; see section 2.3.1	0.29 * VDDA		0.65 * VDDA	V
1.3.3	**Temperature Measurement [b]**						
1.3.3.1	External temperature diode channel gain	a_{TSED}		300		1300	ppm FS / (mV/V)
1.3.3.2	External temperature diode bias current	I_{TSE}		6	10	20	µA

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No.	Parameter	Symbol	Conditions	Min	Typ	Max	Unit
1.3.3.3	External temperature diode input range [a]			0		1.5	V
1.3.3.4	External temperature resistor channel gain	a_{TSER}		1200		3500	ppm FS / (mV/V)
1.3.3.5	External temperature resistor/ input voltage range [a]	V_{TSER}		0		600	mV/V
1.3.3.6	Internal temperature diode sensitivity	ST_{TSI}	Raw values – without conditioning	700		2700	ppm FS / K
1.3.4	**Analog-to-Digital Conversion (ADC)**						
1.3.4.1	ADC resolution [a]	r_{ADC}		13		16	Bit
1.3.4.2	ADC differential nonlinearity (DNL) [a]	DNL_{ADC}	r_{ADC} =13-bit; f_{CLK}=3MHz; best fit, 2nd order; complete AFE; with ADC input range specified in 1.3.4.5			0.95	LSB
1.3.4.3	ADC integral nonlinearity (INL) within TQA [a]	INL_{ADC}				4	LSB
1.3.4.4	ADC INL within TQE	INL_{ADC}				5	LSB
1.3.4.5	ADC input range	Range		10		90	%VDDA
1.3.5	**Sensor Connection Check**						
1.3.5.1	Sensor connection loss detection threshold	R_{SCC_min}		100			kΩ
1.3.5.2	Sensor input short check	R_{SSC_short}	Short detection guaranteed	0		50	Ω
1.3.5.3	Sensor input no-short threshold	R_{SSC_pass}	A short is not indicated above this threshold	1000			Ω
1.3.6	**Digital-to-Analog Conversion (DAC) and Analog Output (AOUT Pin)**						
1.3.6.1	DAC resolution	r_{DAC}	Analog output, 10-90%		12		Bit
1.3.6.2	Output current sink and source for VDDE=5V	$I_{SRC/SINK_OUT}$	V_{OUT}: 5-95%, $R_{LOAD} \geq 2k\Omega$			2.5	mA
			V_{OUT}: 10-90%, $R_{LOAD} \geq 1k\Omega$			5	mA
1.3.6.3	Short circuit current	I_{OUT_max}	To VSSE or VDDE [c]	-25		25	mA
1.3.6.4	Addressable output signal range	V_{SR_OUT95}	@ $R_{LOAD} \geq 2k\Omega$	0.05		0.95	VDDE
		V_{SR_OUT90}	@ $R_{LOAD} \geq 1k\Omega$	0.1		0.9	VDDE
1.3.6.5	Output slew rate [a]	SR_{OUT}	C_{LOAD} < 50nF	0.1			V/µs
1.3.6.6	Output resistance in diagnostic mode	R_{OUT_DIA}	Diagnostic Range: <4|96>%, $R_{LOAD} \geq 2k\Omega$ <8|92>%, $R_{LOAD} \geq 1k\Omega$			82	Ω
1.3.6.7	Load capacitance [a]	C_{LOAD}	C3 (see section 3)			150	nF
1.3.6.8	DNL (DAC)	DNL_{OUT}		-1.5		1.5	LSB
1.3.6.9	INL TQA (DAC) [a]	INL_{OUT}	Best fit, r_{DAC} =12-bit	-5		5	LSB

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No.	Parameter	Symbol	Conditions	Min	Typ	Max	Unit
1.3.6.10	INL TQE (DAC)	INL_{OUT}	Best fit, r_{DAC} =12-bit	-8		8	LSB
1.3.6.11	Output leak current @150°C	I_{LEAK_OUT}	power or ground loss	-25		25	µA
1.3.7 System Response							
1.3.7.1	Startup time [d]	t_{STA}	To 1st output; f_{CLK}=3MHz; no ROM check; ADC 14-bit and 2nd order			5	ms
1.3.7.2	Response time (100% jump) [a]	t_{RESP}	f_{CLK}=4MHz; 13-bit, 2nd order; refer to Table 2.3	256		512	µs
1.3.7.3	Bandwidth [a]		Comparable to analog SSCs		5		kHz
1.3.7.4	Analog output noise peak-to-peak [a]	$V_{NOISE,PP}$	Shorted inputs; bandwidth ≤ 10kHz			10	mV
1.3.7.5	Analog output noise RMS [a]	$V_{NOISE,RMS}$	Shorted inputs; bandwidth ≤ 10kHz			3	mV
1.3.7.6	Ratiometricity error	RE_{OUT_5}	Maximum error of VDDE=5V to 4.5/5.5V			1000	ppm
1.3.7.7	Overall failure (deviation from ideal line including the INL, gain, offset and temperature errors) [e]	F_{ALL} TQI	13-bit, 2nd order ADC; f_{CLK} ≤ 3MHz; XZC=0		0.25 (0.1)		% FS
		F_{ALL} TQA	No sensor caused effects; value in parentheses is the digital readout.		0.5 (0.25)		% FS
		F_{ALL} TQE			1.0 (0.5)		% FS

[a] No measurement in mass production; parameter is guaranteed by design and/or quality observation.

[b] Refer to section 2.4.

[c] Minimum output voltage to VDDE or maximum output voltage to VSSE.

[d] Depends on resolution and configuration - start routine begins approximately 0.8ms after power on.

[e] XZC is active: additional overall failure of 25ppm/K for XZC=31 at maximum; failure decreases linearly for XZC adjustments lower than 31.

1.4 Interface Characteristics and EEPROM

Table 1.4 Interface and EEPROM Characteristics

No.	Parameter	Symbol	Conditions	Min	Typ	Max	Unit
1.4.1 I²C Interface [a]							
1.4.1.1	Input-high level [b]	$V_{I2C_IN_H}$		0.8			VDDA
1.4.1.2	Input-low level [b],	$V_{I2C_IN_L}$				0.2	VDDA
1.4.1.3	Output-low level [b]	$V_{I2C_OUT_L}$	Open Drain, I_{OL}<2mA			0.15	VDDA
1.4.1.4	SDA load capacitance [b]	C_{SDA}				400	pF

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No.	Parameter	Symbol	Conditions	Min	Typ	Max	Unit
1.4.1.5	SCL clock frequency [b]	f_{SCL}				400	kHz
1.4.1.6	Internal pull-up resistor [b]	R_{I2C}		25		100	kΩ
1.4.2 ZACwire™ One Wire Interface (OWI)							
1.4.2.1	Input-low level [b]	$V_{OWI_IN_L}$				0.2	VDDA
1.4.2.2	Input-high level [b]	$V_{OWI_IN_H}$		0.75			VDDA
1.4.2.3	Pull-up resistance master	R_{OWI_PUP}		0.3	3.3		kΩ
1.4.2.4	OWI load capacitance	C_{OWI_LOAD}	Summarized OWI line load			50	nF
1.4.2.5	Start window [b]		Typ: @ f_{CLK}=3MHz	96	175	455	ms
1.4.3 EEPROM							
1.4.3.1	Ambient temperature EEPROM programming [b]	T_{AMB_EEP}		-40		150	°C
1.4.3.2	Write cycles [b]	n_{WRI_EEP}	Write temperature: <=85°C			100k	
			Write temperature: up to 150°C			100	
1.4.3.3	Read cycles [b], [c]	n_{READ_EEP}	Read temperature: <=175°C			$8 * 10^8$	
1.4.3.4	Data retention [b], [d]	t_{RET_EEP}	1300h at 175°C =100000h at 55°C; 27000h at 125°C; 3000h at 150°C)			15	years
1.4.3.5	Programming time [b]	t_{WRI_EEP}	Per written word, f_{CLK}=3MHz		12		ms

[a] Refer to the ZSC31150 Functional Description for timing details.

[b] No measurement in mass production; parameter is guaranteed by design and/or quality observation.

[c] Note that the package and temperature versions cause additional restrictions.

[d] Over lifetime; use calculation sheet *SSC Temperature Profile Calculation Spreadsheet* for temperature stress calculation; note additional restrictions are caused by different package and temperature versions.

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2. Circuit Description

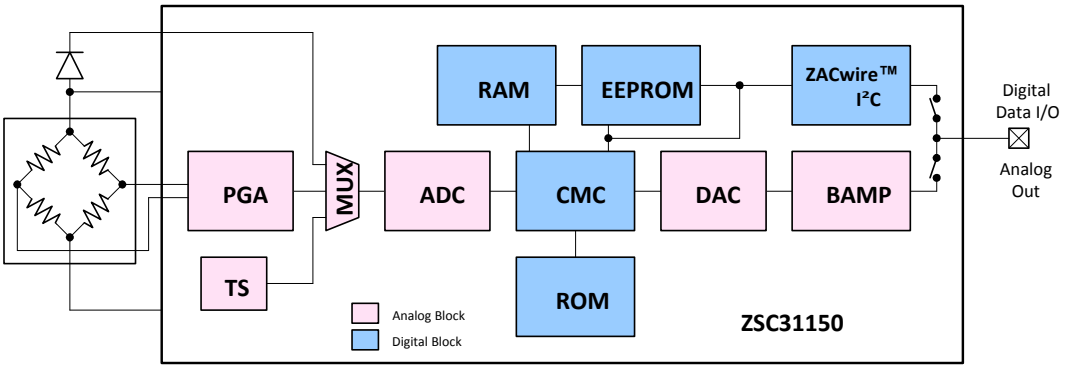
Note: This data sheet provides specifications and a general overview of ZSC31150 operation. For details of operation, including configuration settings and related EEPROM registers, refer to the *ZSC31150 Functional Description*.

2.1 Signal Flow

The ZSC31150's signal path includes both analog (shown in blue in Figure 2.1) and digital (pink) sections. The analog path is differential; i.e., the differential bridge sensor signal is handled internally via two signal lines that are symmetrical around a common mode potential (analog ground = VDDA/2), which improves noise rejection.

Consequently, it is possible to amplify positive and negative input signals, which are located within the common mode range of the signal input.

Figure 2.1 Block Diagram of the ZSC31150



The differential signal from the bridge sensor is pre-amplified by the programmable gain amplifier (PGA). The multiplexer (MUX) transmits the signals from either the bridge sensor, the external diode, or the separate temperature sensor to the analog-to-digital converter (ADC) in a specific sequence (the internal pn-junction (TS) can be used instead of the external temperature diode). Next, the ADC converts these signals into digital values.

The digital signal correction takes place in the calibration microcontroller (CMC). It is based on a correction formula located in the ROM and sensor-specific coefficients stored in the EEPROM during calibration. Depending on the programmed output configuration, the corrected sensor signal is output as an analog value or in a digital format (I^2C or ZACwire™). The configuration data and the correction parameters can be programmed into the EEPROM via the digital interfaces.

2.2 Application Modes

For each application, a configuration set must be established (generally prior to calibration) by programming the on-chip EEPROM regarding to the following modes:

Sensor Channel

- Sensor mode: ratiometric bridge excitation in voltage or current supply mode.
- Input range: the gain adjustment of the AFE with respect to the maximum sensor signal span and the zero point of the ADC have to be chosen.
- An additional analog offset compensation, the Extended Zero-Point Compensation (XZC), must be enabled if required; e.g., if the sensor offset voltage is close to or larger than the sensor span.
- Resolution/response time: The ADC must be configured for resolution and conversion settings (1^{st} or 2^{nd} order). These settings influence the sampling rate, signal integration time, and, as a result, the noise immunity.

Temperature

- Temperature measurement: the source for the temperature correction must be chosen.

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2.3 Analog Front End (AFE)

The analog front end (AFE) consists of the programmable gain amplifier (PGA), the multiplexer (MUX), and the analog-to-digital converter (ADC).

2.3.1 Programmable Gain Amplifier (PGA)

Table 2.1 shows the adjustable gains, the sensor signal spans, and the allowed common mode range.

Table 2.1 Adjustable Gains, Resulting Sensor Signal Spans, and Common Mode Ranges

No.	Overall Gain a_{IN}	Max. Span V_{IN_SP} [mV/V] [a]	Gain Amp1	Gain Amp2	Gain Amp3	Input Common Mode Range V_{IN_CM} as % of VDDA [b]	
						XZC = Off	XZC = On
1	420	1.8	30	7	2	29 to 65	45 to 55
2	280	2.7	30	4.66	2	29 to 65	45 to 55
3	210	3.6	15	7	2	29 to 65	45 to 55
4	140	5.4	15	4.66	2	29 to 65	45 to 55
5	105	7.1	7.5	7	2	29 to 65	45 to 55
6	70	10.7	7.5	4.66	2	29 to 65	45 to 55
7	52.5	14.3	3.75	7	2	29 to 65	45 to 55
8	35	21.4	3.75	4.66	2	29 to 65	45 to 55
9	26.3	28.5	3.75	3.5	2	29 to 65	45 to 55
10	14	53.75	1	7	2	29 to 65	45 to 55
11	9.3	80	1	4.66	2	29 to 65	45 to 55
12	7	107	1	3.5	2	29 to 65	45 to 55
13	2.8	267	1	1.4	2	32 to 57	not applicable

[a] Recommended internal signal range maximum is 80% of the VDDA voltage. Span is calculated by the following formula: Span = 80% / gain.

[b] Bridge in Voltage Mode with maximum input signal (with XZC = +300% Offset), 14-bit accuracy. Refer to the *ZSC31150 Functional Description* for usable input signal/common mode range at bridge in current mode. See section 2.3.2 for an explanation of the extended analog zero compensation (XZC).

2.3.2 Offset Compensation

The ZSC31150 supports two methods of sensor offset compensation (zero shift):

- Digital offset correction
- XZC: analog compensation for large offset values (up to a maximum of approximately 300% of the span, depending on the gain adjustment)

The digital sensor offset correction will be processed during the digital signal correction/conditioning by the calibration microcontroller (CMC).

Analog sensor offset pre-compensation is needed for compensation of large offset values, which would overdrive the analog signal path by uncompensated gaining. For analog sensor offset pre-compensation, a compensation voltage is added in the analog pre-gaining signal path (coarse offset removal). The analog offset compensation in the AFE can be adjusted by 6 EEPROM bits (refer to the *ZSC31150 Functional Description* for details).

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Table 2.2 Analog Zero Point Shift Ranges (XZC)

PGA gain a_{IN}	Max. Span V_{IN_SP} [mV/V]	Offset shift per step as % of full span	Approximate maximum offset shift [mV/V]	Approximate maximum shift [% V_{IN_SP}] (at ± 31)
420	1.8	12.5%	7.8	388%
280	2.7	7.6%	7.1	237%
210	3.6	12.5%	15.5	388%
140	5.4	7.6%	14.2	237%
105	7.1	12.5%	31	388%
70	10.7	7.6%	28	237%
52.5	14.3	12.5%	32	388%
35	21.4	7.6%	57	237%
26.3	28.5	5.2%	52	161%
14	53.75	12.5%	194	388%
9.3	80	7.6%	189	237%
7	107	5.2%	161	161%
2.8	267	0.83%	72	26%

2.3.3 Measurement Cycle

The complete measurement cycle is controlled by the CMC. Depending on EEPROM settings, the multiplexer (MUX) selects the following input signals in a defined sequence:

- Temperature measured by external diode or thermistor, internal pn-junction, or bridge
- Internal offset of the input channel (V_{OFF})
- Pre-amplified bridge sensor signal

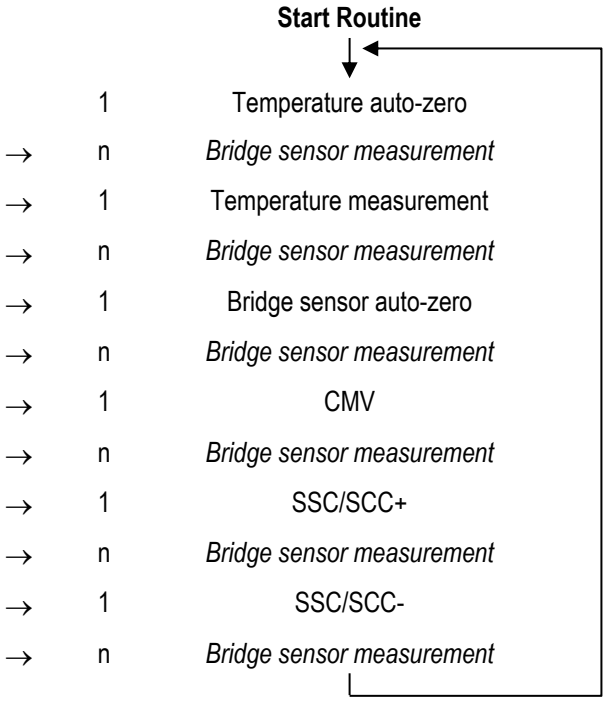
The cycle diagram in Figure 2.2 shows the basic structure of the measurement cycle. The bridge sensor measurement count can be configured in EEPROM for a value within n=<1,31>.

After power-on, the startup routine is processed, which performs all measurements needed to acquire an initial valid conditioned sensor output. After the startup routine, the normal measurement cycle runs.

Note: The “CMV,” “SSC/SCC+” and “SSC/SCC-” measurements are always performed in every cycle independent of the EEPROM configuration.

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Figure 2.2 Measurement Cycle



2.3.4 Analog-to-Digital Converter

The ADC is an integrating analog-to-digital converter in full differential switched capacitor technique.

Programmable ADC resolutions are r_{ADC}=<13, 14> or with segmentation, r_{ADC}=<15, 16> bit.

The ADC can be used as a first or second order converter. In the **first order** mode, it is inherently monotone and insensitive to short and long-term instability of the clock frequency. The conversion cycle time depends on the desired resolution and can be roughly calculated by the following equation where r_{ADC} is the ADC resolution and t_{ADC_1} is the conversion cycle time in seconds in first-order mode:

$$t_{ADC_1} = \frac{2^{r_{ADC}}}{\left(\frac{f_{OSC}}{2}\right)}$$

In the **second order** mode, two conversions are stacked with the advantage of a much shorter conversion cycle time but the drawback of a lower noise immunity caused by the shorter signal integration period. The approximate conversion cycle time t_{ADC_2} in second-order mode is calculated by the following equation:

$$t_{ADC_2} = \frac{2^{(r_{ADC}+3)/2}}{\left(\frac{f_{OSC}}{2}\right)}$$

The calculation formulas for t_{ADC} give an overview of conversion time for one AD conversion. Refer to the *ZSC31150 Bandwidth Calculation Spreadsheet* for detailed calculations for sampling time and bandwidth.

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The result of the AD conversion is a relative counter result corresponding to the following equation (see the *ZSC31150 Functional Description* for more detailed equations):

$$Z_{ADC} = 2^{r_{ADC}} \left(\frac{V_{ADC_DIFF}}{V_{ADC_REF}} + RS_{ADC} \right)$$

Z_{ADC} Number of counts (result of the conversion)

r_{ADC} Selected ADC resolution in bits

V_{ADC_DIFF} Differential input voltage of the ADC

V_{ADC_REF} Reference voltage of the ADC

RS_{ADC} Digital ADC range shift (RS_{ADC} = $^1/_{16}$, $^1/_8$, $^1/_4$, $^1/_2$, controlled by the EEPROM setting)

The sensor input signal can be shifted to the optimal input range of the ADC with the RS_{ADC} value.

Table 2.3 Analog Output Resolution versus Sample Rate

ADC Adjustment		Approximated Output Resolution [a]		Sample Rate f_{CON} [b]		Averaged Bandwidth at f_{CLK}	
ADC Order	r_{ADC}	Digital	Analog	f_{CLK}=3MHz	f_{CLK}=4MHz	f_{CLK}=3MHz	f_{CLK}=4MHz
	[Bit]	[Bit]	[Bit]	[Hz]	[Hz]	[Hz]	[Hz]
1	13	13	12	345	460	130	172
	14	14	12	178	237	67	89
	15	14	12	90	120	34	45
	16	14	12	45	61	17	23
2	13	13	12	5859	7813	2203	2937
	14	14	12	3906	5208	1469	1958
	15	14	12	2930	3906	1101	1468
	16	14	12	1953	2604	734	979

[a] The ADC resolution should be one bit higher than the required output resolution if the AFE gain is adjusted so that more than 50% of the input range is used. Otherwise the ADC resolution should be more than one bit higher than the required output resolution.

[b] The sampling rate (A/D conversion time) is only a part of the whole cycle; refer to the *ZSC31150 Bandwidth Calculation Spreadsheet* for detailed information.

Note: The ADC's reference voltage ADC_{VREF} is defined by the potential between <VBR_T> and <VBR_B> (or <VDDA> to <VSSA>, if selected in EEPROM by the bit CFGAPP:BREF=1). Theoretically, the input range ADC_{RANGE_INP} of the ADC is equivalent to the ADC's reference voltage.

In practice, the maximum ADC input range used should be from 10% to 90% of ADC_{RANGE_INP}, which is a necessary condition for ensuring the specified accuracy, stability, and nonlinearity parameters of the AFE. This condition is also valid for whole temperature range and all applicable sensor tolerances. The ZSC31150 does not have an internal failsafe function that verifies that the input meets this condition.

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2.4 Temperature Measurement

The ZSC31150 supports four different methods for acquiring the temperature data needed for calibration of the sensor signal in the specified temperature range.

Temperature data can be acquired using one of these temperature sensors:

- an internal pn-junction temperature sensor
- an external pn-junction temperature sensor connected to sensor top potential (V_{BRTOP})
- an external resistive half bridge temperature sensor
- the temperature coefficient of the sensor bridge at bridge current excitation

Refer to the *ZSC31150 Functional Description* for a detailed explanation of temperature sensor adaptation and adjustment.

2.5 System Control and Conditioning Calculation

The system control supports the following tasks/features:

- Controlling the measurement cycle according to the EEPROM-stored configuration data
- Performing the16-bit correction calculation for each measurement signal using the EEPROM-stored calibration coefficients and ROM-based algorithms; i.e., the signal conditioning
- Managing the start-up sequence and starting signal conditioning
- Handling communication requests received by the digital interface
- Managing failsafe tasks for the functions of the ZSC31150 and indicating detected errors with diagnostic states

Refer to the *ZSC31150 Functional Description* for a detailed description.

2.5.1 Operation Modes

The internal state machine has three main states:

- The continuously running signal conditioning mode, which is called Normal Operation Mode (NOM)
- The calibration mode with access to all internal registers and states, which is called Command Mode (CM)
- The failure messaging mode, which is called Diagnostic Mode (DM)

2.5.2 Start Up Phase

The start-up phase* consists of following segments:

1. Internal supply voltage settling phase (i.e., the VDDA - VSSA potential), which is ended when the reset signal is disabled through the power-on clear block (POR). Refer to the *ZSC31150 Technical Note – High Voltage Protection* document, section 4 for power on/off thresholds.
   Time (from beginning with VDDA-VSSA=0V): 500µs to 2000µs; AOUT is in tri-state
2. System start, EEPROM read out, and signature check (and ROM check if selected by setting EEPROM bit CFGAPP:CHKROM=1).
   Time: ~200µs (~9000µs with ROM-check; i.e., 28180 clocks); AOUT is LOW (DM)
3. Processing the start routine for signal conditioning (all measurements and conditioning calculations).
   Time: 5 x A/D conversion time; AOUT behavior depends on selected OWI mode (refer to section 2.6):
   - **OWIANA & OWIDIS** => AOUT is LOW (DM)
   - **OWIWIN & OWIENA** => AOUT is in tri-state

* All timings described are roughly estimated values and are affected by the internal clock frequency. Timings are estimated for f_{CLK}=3MHz.

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The analog output AOUT will be activated at the end of the start-up phase depending on the adjusted output and communication mode (refer to section 2.6). If errors are detected, the Diagnostic Mode (DM) is activated and the diagnostic output signal is driven at the output.

After the start-up phase, the continuously running measurement and calibration cycle is started. Refer to *ZSC31150 Bandwidth Calculation Spreadsheet* for detailed information about output update rate.

2.5.3 Conditioning Calculation

The digitalized value for the bridge sensor measurement (acquired raw data) is processed with the correction formula to remove offset and temperature dependency and to compensate nonlinearity up to 3rd order. The result of the correction calculation is a non-negative 15-bit value for the bridge sensor in the range [0; 1). This value P is clipped with programmed limitation coefficients and continuously written to the output register of the digital serial interface and the output DAC.

Note: The conditioning includes up to third-order nonlinearity sensor input correction. The available adjustment ranges depend on the specific calibration parameters; for a detailed description, refer to *ZSC31150 Functional Description.* Basically, offset compensation and linear correction are only limited by the loss of resolution they will cause. The second-order correction is possible up to approximately 30% of the full scale difference from a straight line; third order is possible up to approximately 20% (ADC resolution = 13-bit). The calibration principle used is able to reduce existing nonlinearity errors of the sensor up to 90%. The temperature calibration includes first and second order correction and should be fairly sufficient in all relevant cases. ADC resolution also influences calibration possibilities; e.g., 1 additional bit of resolution reduces the calibration range by approximately 50%. The maximum calculation input data width is 14-bit. The 15 or 16 bit ADC resolution mode uses only a 14-bit segment of the ADC range.

2.6 Analog Output AOUT

The analog output is used for outputting the analog signal conditioning result and for “end of line” communication via the ZACwire™ interface one-wire communication interface (OWI). The ZSC31150 supports four different modes of the analog output in combination with the OWI behavior:

- OWIENA: Analog output is deactivated; OWI communication is enabled.
- OWIDIS: Analog output is active (~2ms after power-on); OWI communication is disabled.
- OWIWIN: Analog output will be activated after the time window;
  OWI communication is enabled in a time window of ~500ms (maximum);
  transmission of the “START_CM” command must be finished during the time window.
- OWIANA: Analog output will be activated after a ~2ms power on time;
  OWI communication is enabled in a time window of ~500ms (maximum);
  transmission of the START_CM” command must be finished during time window;
  to communicate, the internal driven potential at AOUT must be overwritten
  by the external communication master (AOUT drive capability is current limited).

The analog output potential is driven by a unity gain output buffer for which the input signal is generated by a 12.4-bit resistor-string DAC. The output buffer (BAMP), which is a rail-to-rail op amp, is offset compensated and current limited. Therefore, a short-circuit of the analog output to ground or the power supply does not damage the ZSC31150.

2.7 Serial Digital Interface

The ZSC31150 includes a serial digital interface (SIF), which is used for communication with the circuit to calibrate the sensor module. The serial interface is able to communicate with two communication protocols: I²C and the ZACwire™ one-wire communication interface (OWI). The OWI can be used to for an “end of line” calibration via the analog output AOUT of the complete assembled sensor module.

Refer to the *ZSC31150 Functional Description* for a detailed description of the serial interfaces and communication protocols.

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2.8 Failsafe Features, Watchdog and Error Detection

The ZSC31150 detects various possible errors. A detected error is indicated by a change in the internal status in Diagnostic Mode (DM). In this case, the analog output is set to LOW (minimum possible output value; i.e., the lower diagnostic range LDR) and the output registers of the digital serial interface are set to a significant error code.

A watchdog oversees the continuous operation of the CMC and the running measurement loop. The operation of the internal clock oscillator is verified continuously by the oscillator failure detection.

A check of the sensor bridge for broken wires is done continuously by two comparators watching the input voltage of each input (sensor connection and short check). Additionally, the common mode voltages of the sensor and sensor input short are watched continuously (sensor aging).

Different functions and blocks in the digital section, e.g. the RAM, ROM, EEPROM, and register content, are watched continuously. Refer to the *ZSC31150 Functional Description* for a detailed description of safety features and methods of error indication.

2.9 High Voltage, Reverse Polarity, and Short Circuit Protection

The ZSC31150 is designed for 5V power supply operation.

The ZSC31150 and the connected sensor are protected from overvoltage and reverse polarity damage by an internal supply voltage limiter. The analog output AOUT can be connected with all potentials (short circuit, over-voltage, and reverse voltage) in the protection range under all potential conditions at the VDDE and VSSE pins.

All external components (see section 3) are required to guarantee this operation. The protection is not time limited. Refer the *ZSC31150 Technical Note – High Voltage Protection* for a detailed description of protection cases and conditions.

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3. Application Circuit Examples

The application circuits contain external components that are needed for over-voltage, reverse polarity, and short circuit protection.

Recommendation: Check the ZSC31150 product page www.IDT.com/ZSC31150 for other application examples given in application notes. Note: Some application notes require a customer login—see section 9 for details.

Table 3.1 Application Circuit Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Notes
C1	C	100		470	nF	
C2	C	100			nF	
C3 [a]	C	4	47	160	nF	The value of C3 is the sum of the load capacitor and the cable capacitance.
C4, C5 [a]	C	0		10	nF	Recommended to increase EMC immunity.
R1			10		kΩ	
R_{IBR}	R	Refer to section 1.2.			Ω	

[a] Higher values for C3, C4, and C5 increase EMC immunity.

Figure 3.1 Bridge in Voltage Mode, External Diode Temperature Sensor

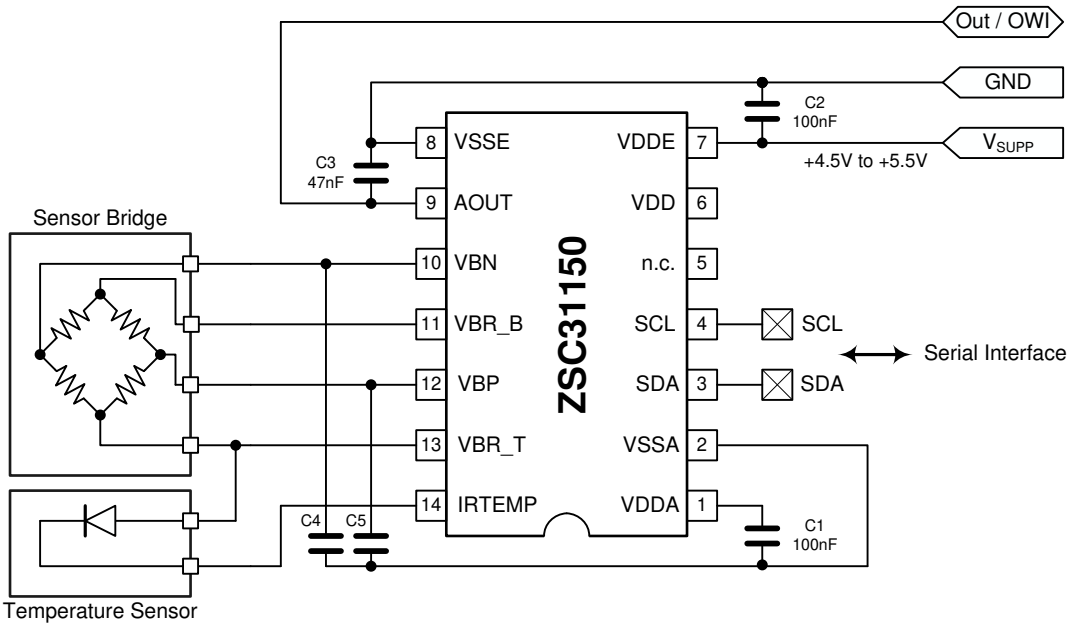


Figure 3.2 Bridge in Voltage Mode, External Thermistor

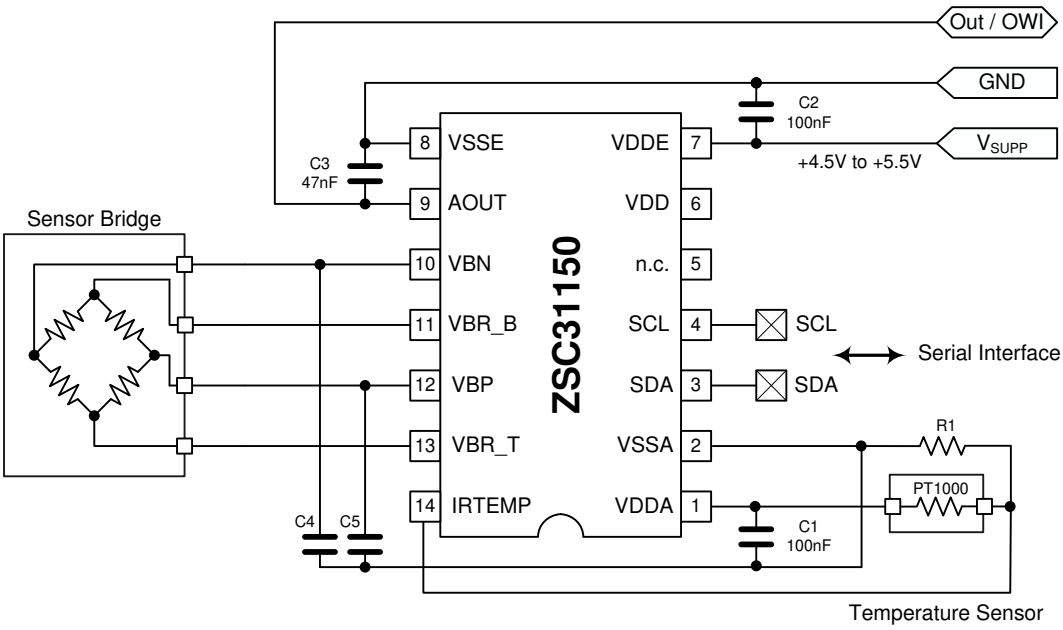
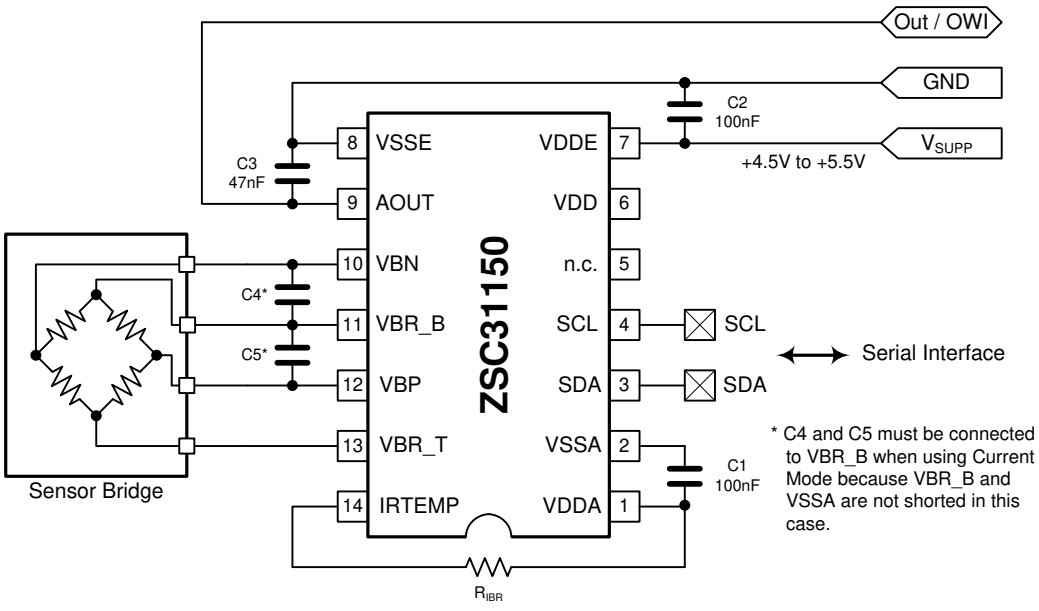


Figure 3.3 Bridge in Current Mode, Temperature Measurement via Bridge TC



4. Pin Configuration, Latch-Up and ESD Protection

4.1 Pin Configuration and Latch-up Conditions

Table 4.1 Pin Configuration and Latch-Up Conditions

Pin	Name	Description	Notes	Usage/ Connection [a]	Latch-up Related Application Circuit Restrictions and/or Notes
1	VDDA	Positive analog supply voltage	Analog IO	Required/-	
2	VSSA	Negative analog supply voltage	Analog IO	Required/-	
3	SDA	I²C data IO	Digital IO, pull-up	-/VDDA	Trigger Current/Voltage to VDDA/VSSA: +/-100mA or 8/-4V
4	SCL	I²C clock	Digital IN, pull-up	-/VDDA	
5	N.C.	No connection			
6	VDD	Positive digital supply voltage	Analog IO	Required or open/-	Only capacitor to VSSA is allowed, otherwise no application access
7	VDDE	Positive external supply voltage	Supply	Required/-	Trigger Current/Voltage: -100mA/33V
8	VSSE	Negative external supply voltage	Ground	Required/-	
9	AOUT	Analog output and one wire IF IO	IO	Required/-	Trigger Current/Voltage: -100mA/33V
10	VBN	Negative input sensor bridge	Analog IN	Required/-	
11	VBR_B	Bridge bottom potential	Analog IO	Required/VSSA	Depending on application circuit, short to VDDA/VSSA possible
12	VBP	Positive input sensor bridge	Analog IN	Required/-	
13	VBR_T	Bridge top potential	Analog IO	Required / VDDA	
14	IRTEMP	Temp sensor and current source resistor	Analog IO	- / VDDA, VSSA	Depending on application circuit

[a] **Usage**: If "Required" is specified, an electrical connection is necessary; refer to the application circuits in section 3.
Connection: To be connected to this potential if not used or if no application/configuration-related constraints are given.

4.2 ESD Protection

All pins have an ESD protection of > 2000V. Additionally, the pins VDDE, VSSE and AOUT have an ESD protection of >4000V.

ESD protection referenced to the Human Body Model is tested with devices during product qualification. The ESD test follows the Human Body Model with 1.5kΩ/100pF based on MIL 883, Method 3015.7.

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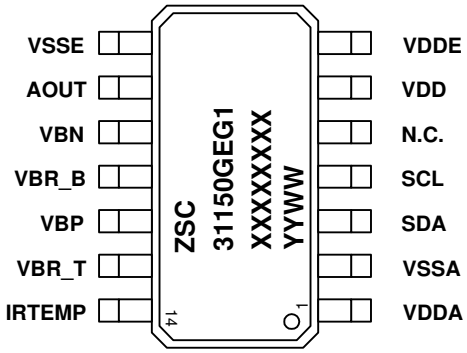
5. Package

5.1 SSOP14 Package

The standard packages of the ZSC31150 are the SSOP14 green package (5.3mm body width) with a lead pitch of 0.65mm and the DFN14 (4mmx5mm) package with a lead pitch of 0.5mm.

For the SSOP14 package markings shown in Figure 5.1, YYWW refers to the last two digits of the year (YY) and two digits for the work-week designation (WW). XXXXXXXX refers to the lot number.

Figure 5.1 SSOP14 Pin Diagram



5.2 14-DFNPackage

For the 14-DFN package, the pin assignment is the same as in SSOP14. Refer to the *ZSC31150 Technical Note – Die and Package Specifications* for a description of package markings.

Figure 5.2 provides the dimensions for the 14-DFN package option, which are based on JEDEC MO-229. The 14-DFN package has wettable flanks.

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Figure 5.2 Outline Drawing for 14-DFN Package with Wettable Flanks

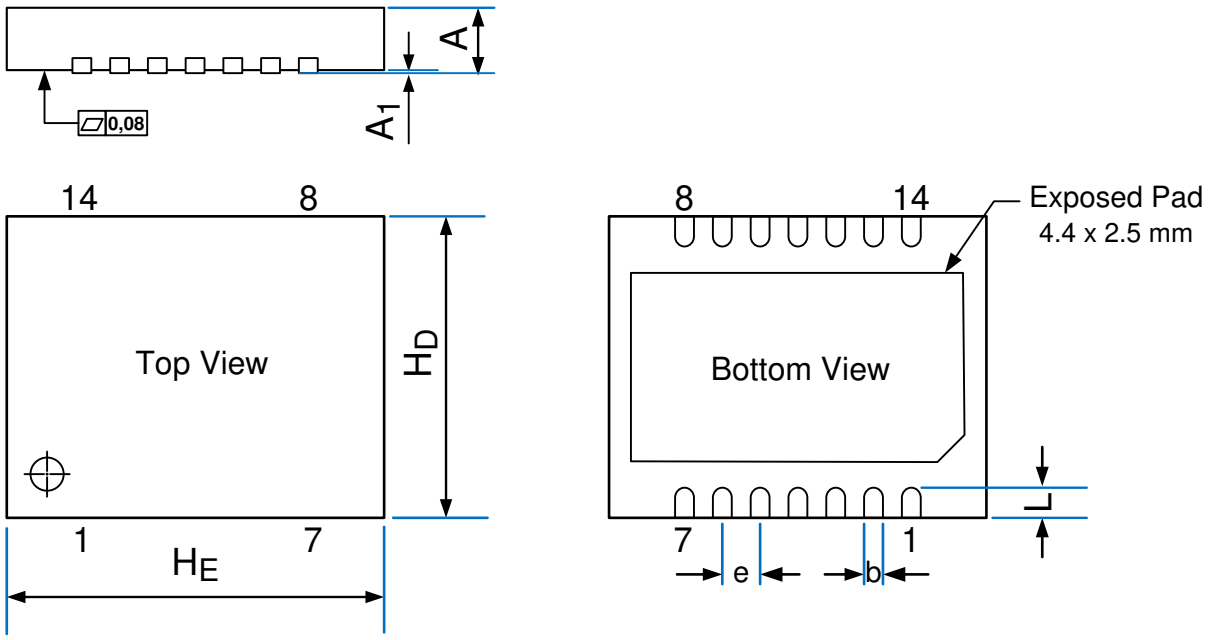


Table 5.1 14-DFN Package Dimensions

Dimension	Minimum	Maximum
A	0.8	0.9
A_1	0	0.05
b	0.2	0.3
e	0.5 nominal	
H_D	3.9	4.1
H_E	4.9	5.1
L	0.3	0.5

6. Quality and Reliability

The ZSC31150 is qualified according to the AEC-Q100 standard, operating temperature grade 0. A fit rate < 5fit (temperature =55°C, S=60%) is guaranteed. A typical fit rate of the C7D technology, which is used for ZSC31150, is 2.5fit.

7. Customization

For high-volume applications, which require an upgraded or downgraded functionality compared to the standard ZSC31150, IDT can customize the circuit design by adding or removing certain functional blocks.

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For this purpose, IDT has a considerable library of sensor-dedicated circuitry blocks. As a result, IDT can provide a custom solution quickly. Please contact IDT for further information.

8. Ordering Information

Product Sales Code	Description	Package
ZSC31150GEB	ZSC31150 Die — Temperature range: -40°C to +150°C	Unsawn on Wafer
ZSC31150GEC	ZSC31150 Die — Temperature range: -40°C to +150°C	Sawn on Wafer Frame
ZSC31150GED	ZSC31150 Die — Temperature range: -40°C to +150°C	Waffle Pack
ZSC31150GEG2-R	ZSC31150 14-DFN (5 × 4 mm with wettable flank—Temperature range: -40°C to 150°C	Tape & Reel
ZSC31150GAG2-R	ZSC31150 14-DFN (5 × 4 mm with wettable flank —Temperature range: -40°C to 125°C	Tape & Reel
ZSC31150GAB	ZSC31150 Die — Temperature range: -40°C to +125°C	Unsawn on Wafer
ZSC31150GAC	ZSC31150 Die — Temperature range: -40°C to +125°C	Sawn on Wafer Frame
ZSC31150GEG1	ZSC31150 SSOP14—Temperature range: -40°C to +150°C	Tube: add “-T” to sales code Tape & Reel: add “-R”
ZSC31150GLG1	ZSC31150 SSOP14—Temperature range: -40°C to +150°C (Long life: 5000h @150°C)	Tube: add “-T” to sales code Tape & Reel: add “-R”
ZSC31150GAG1	ZSC31150 SSOP14—Temperature range: -40°C to +125°C	Tube: add “-T” to sales code Tape & Reel: add “-R”
ZSC31150KITV1P2	ZSC31150 SSC Evaluation Kit V1.2: three interconnecting boards, five ZSC31150 SSOP14 samples, USB cable (software can be downloaded from product page at www.IDT.com/ZSC31150)	
ZSC31150MCSV1P1	Modular Mass Calibration System (MSC) V1.1 for ZSC31150: MCS boards, cable, connectors (software can be downloaded from product page at www.IDT.com/ZSC31150)	

9. Related Documents and Tools

Visit the ZSC31150 product page www.IDT.com/ZSC31150 on the IDT website at www.IDT.com or contact your nearest sales office for the latest version of this document and related documents.

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10. Glossary

Term	Description
ADC	Analog-to-Digital Converter
AEC	Automotive Electronics Council
AFE	Analog Front End
AOUT	Analog Output
BAMP	Buffer Amplifier
CM	Command Mode
CMC	Calibration Microcontroller
CMV	Common Mode Voltage
CMOS	Complementary Metal Oxide Semiconductor
DAC	Digital-to-Analog Converter
DM	Diagnostic Mode
EEPROM	Electrically Erasable Programmable Read Only Memory
ESD	Electrostatic Device
LDR	Lower Diagnostic Range
MUX	Multiplexer
NOM	Normal Operation Mode
OWI	One Wire Interface
P	Bridge Sensor Measurement; e.g., Pressure Sensor
PGA	Programmable Gain Amplifier
POC	Power on Clear
RAM	Random-Access Memory
RISC	Reduced Instruction Set Computer
RMS	Root-Mean-Square
ROM	Read Only Memory
SCC	Sensor Connection Check
SIF	Serial Interface
SSC+	Positive-biased Sensor Short Check
SSC-	Negative-biased Sensor Short Check
TS	Temperature Sensor
XZC	eXtended Zero Compensation

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11. Document Revision History

Date	Description
September 20, 2008 (Revision 1.01)	Section 6: fit rate added. Section 1.5.2: ROM check time revised/corrected. Section 5.3.4.3: SC – no detection limit added.
September 20, 2009 (Revision 1.02)	Update to new ZMDI template.
October 2, 2009 (Revision 1.03)	Update to ZMDI denotation.
October 22, 2009 (Revision 1.04)	Formatting and linking issues solved.
February 26, 2010 (Revision 1.05)	Update for ZMDI template, including *ZSC31150 Functional Description* at page 2 and 3. Added ordering codes for ZSC31150 and evaluation kits. Extended glossary. Update for contact information.
July 29, 2010 (Revision 1.06)	Correct “Offset shift per step” and “Approx. maximum offset shift” in Table 2.2 for PGA gain = 105 and 52.5. Moved 1.4.1.6 “Internal pull-up resistor” into section 1.4.1 in Table 1.2. Redrew of Sensor Bridge in Figure 3.1, Figure 3.2, and Figure 3.3. Added comment for C4 and C5 in Figure 3.3. Renamed ZMD31150 as ZSC31150.
August 31, 2010 (Revision 1.07)	Connection of R_{IBR} in Figure 3.3 corrected.
August 15, 2011 (Revision 1.08)	Update ordering information with “Long Life Automotive” in “Ordering Information” on page 3 and section 8.
December 15, 2012 (Revision 2.00)	Update for part numbers and IDT contact information. Minor edits.
March 31, 2014 (Revision 2.10)	Revision of specifications in section 1.4.2. Recommended internal signal range revised to 80%. OWI interface parameters list extended. ADC formula corrected. DFN14 package added. Minor edits for clarity. Updated contact information. Updated imagery for cover and headings.
April 30, 2014 (Revision 2.20)	Added notation that DFN14 package has wettable flanks. Update for contact information and addition of CAD model files to section 9.
August 27, 2014 (Revision 2.30)	Minor edits on page 2. Minor edits for die description in part code tables.
December 3, 2014 (Revision 2.40)	Corrected connection of temperature PTC sensor in Figure 3.2. Update for contact information.
July 27, 2015 (Revision 2.41)	Update for order code for ZSC31150 SSC Evaluation Kit order code. Update for contact information.
January 29, 2016	Changed to IDT branding. The document release date is now the revision reference.
December 6, 2016	Added ZSC31150GAB and ZSC31150GAC order codes. Correction for order codes for kit and MCS. Updates for formatting and minor edits.

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