Multi-touch LCD Module

User Manual



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CONTENTS

CHAPTER 1 *INTRODUCTION* 3

1.1 About the Package 3

1.2 Power Adapter for MTL 4

1.3 Setup License for Terasic Multi-touch IP 5

1.4 Assembly 6

1.5 Connectivity 7

1.6 Getting Help 7

CHAPTER 2 *ARCHITECTURE OF MTL* 8

2.1 Features 8

2.2 MTL Kit 8

2.3 Multi-touch LCD Module (MTL) 8

2.4 IDE Cable 11

2.5 ITG Adapter 11

CHAPTER 3 *USING THE MTL* 13

3.1 Pin Definition of 2x20 GPIO Connector 13

3.2 Using LCD 15

3.3 Using Terasic Multi-touch IP 15

CHAPTER 4 *EPHOTO DEMONSTRATION* 18

4.1 Operation Description 18

4.2 Block Diagram of the ePhoto Design 19

4.3 Loading Photos into FLASH 20

4.4 Demonstration for Terasic DE2-115 FPGA Board 21

4.5 Custom Display Photo 23

CHAPTER 5 *PAINTER DEMONSTRATION* 24

5.1 Operation Description 24

5.2 System Description 25

5.3 Demonstration for Terasic DE2-115 FPGA Board 26

5.4 Demonstration Source Code 27

CHAPTER 6 *APPENDIX* 28

6.1 Revision History 28

6.2 Copyright Statement 28

Chapter 1

Introduction

The Terasic Multi-touch LCD Module (MTL) is an all-purpose capacitive touch-screen for FPGA applications and provides multi-touch gesture and single-touch support. An IDE cable with an IDE to GPIO (ITG) adapter is used to interface with various Terasic FPGA development boards through a 2x20 GPIO interface on the MTL. The kit contains complete reference designs and source code for an ePhoto demonstration and Painter application. This chapter provides the key information about the kit.

1.1 About the Package

The MTL kit comes with the following contents:

- Multi-touch LCD Module
- IDE Cable with ITG Adapter
- MTL System CD-ROM
- 5V Power Supply
- Four Silicon Footstands

The system CD contains technical documents of the MTL kit, which includes component datasheets, demonstrations, schematic, cable and user manual.

Figure 1-1 shows the contents of MTL kit.



Figure 1-1 Contents of MTL Kit

1.2 Power Adapter for MTL

Figure 1-2 shows the power adapter for the MTL. Due to the fact that the LCD panel in the MTL consumes more power than some boards can provide a dedicated power adapter for MTL is required. Note: the power adapter is not necessary for the DE2-115 FPGA board.



Figure 1-2 MTL Power Adapter

1.3 Setup License for Terasic Multi-touch IP

To utilize the multi-touch panel in a Quartus II project, a Terasic Multi-Touch IP is required. After a license file for Quartus II is installed, there is one more license file needed to implement Terasic's Multi-touch IP. Error messages will be displayed if the license file is not added before compiling projects using Terasic Multi-touch IP. The license file is located at:

MTL System CD\License\license_multi_touch.dat

There are two ways to install the License. The first one is to add the license file (license_multi_touch.dat) to the licensed file listed in Quartus II, as shown in **Figure 1-3**.

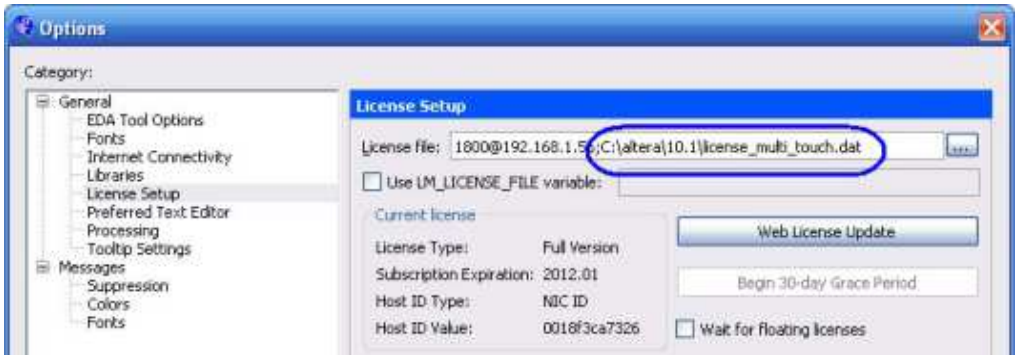


Figure 1-3 License Setup

The second way is to add license content to the existing license file. The procedures are listed below:

Use Notepad or other text editing software to open the file license_multi_touch.dat.

1. The license contains the FEATURE lines required to license the IP Cores as shown in **Figure 1-4**.

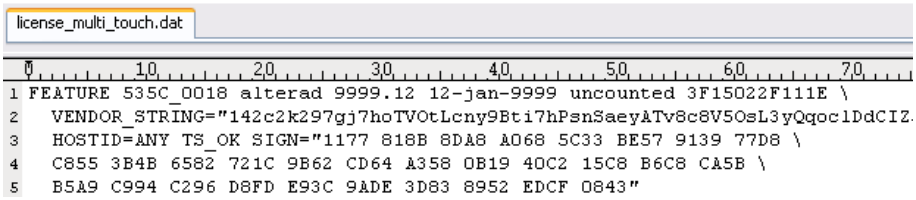


Figure 1-4 Content of license_multi_touch.dat

2. Open your Quartus II license.dat file in a text editor.
3. Copy everything under license_multi_touch.dat and paste it at the end of your Quartus II license file. (Note: Do not delete any FEATURE lines from the Quartus II license file. Doing so will result in an unusable license file.) .
4. Save the Quartus II license file.

Note: The Terasic IP Multi-touch IP can also be found under the \IP folder in the system CD as well as the \IP folder in the reference designs.

1.4 Assembly

Here are the procedures to assemble the MTL kit:

1. Connect the IDE cable to the IDE connector on the back of the MTL as shown in the **Figure 1-5**.

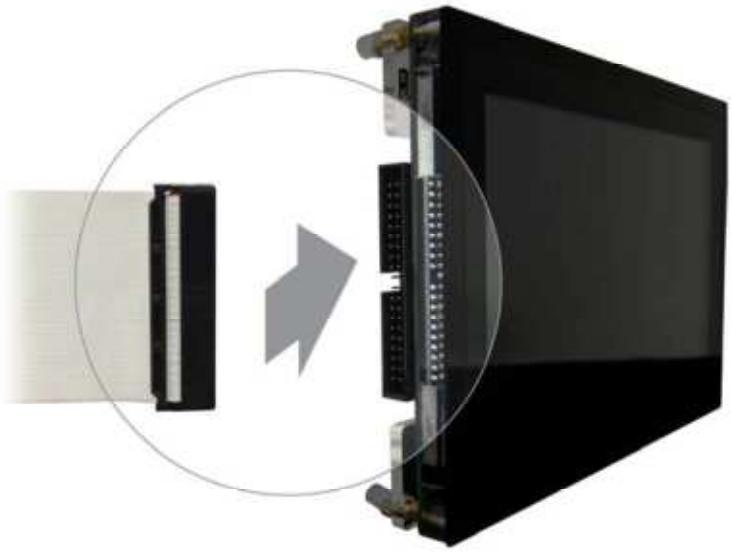


Figure 1-5 MTL connection for the IDE cable

2. Place four silicon footstands to foot pegs of the MTL as shown in **Figure 1-6**.



Figure 1-6 MTL Footstand Setup

1.5 Connectivity

The following figures show the connectivity for MTL to DE2-115 and DE2 FPGA Development Boards. Note: The 5V power supply is required to connect to the DE2.



Figure 1-7 MTL with DE2-115



Figure 1-8 MTL with DE2

1.6 Getting Help

Here is information of how to get help if you encounter any problem:

- Office Hours: 9:00 a.m. to 6:00 p.m. (GMT +8)
- Telephone: +886-3-550-8800
- Email: support@terasic.com

Chapter 2

Architecture of MTL

This chapter provides information regarding features and architecture of the Multi-touch LCD Module (MTL).

2.1 Features

The key features of this module are listed below:

- 800x480 pixel resolution LCD with 24-bit color depth
- Two-point multi-gesture support
- Single touch support
- IDE interface
- 2x20 GPIO interface with ITG adapter

2.2 MTL Kit

The MTL kit is assembled via three components:

- Multi-touch LCD Module
- IDE Cable
- IDE to GPIO (ITG) adapter

The IDE cable is used to provide a high-speed signal transmission for 33 MHz video signals. The ITG adapter is designed to map the standard IDE pin assignment to the 2x20 GPIO interface on the FPGA boards.

2.3 Multi-touch LCD Module (MTL)

Component and Layout

The top view of MTL is shown in **Figure 2-1**.



Figure 2-1 Multi-touch LCD Module (Top View)

The bottom view of Multi-touch LCD Module is shown in Figure 2-2. It depicts the layout and indicates the locations of connectors and key components.



Figure 2-2 Multi-touch LCD Module (Bottom View)

Block Diagram

Figure 2-3 shows the block diagram of MTL. The IDE connector houses all the wires from peripheral interfaces, connecting to the FPGA of a development kit through the IDE cable and ITG adapter.

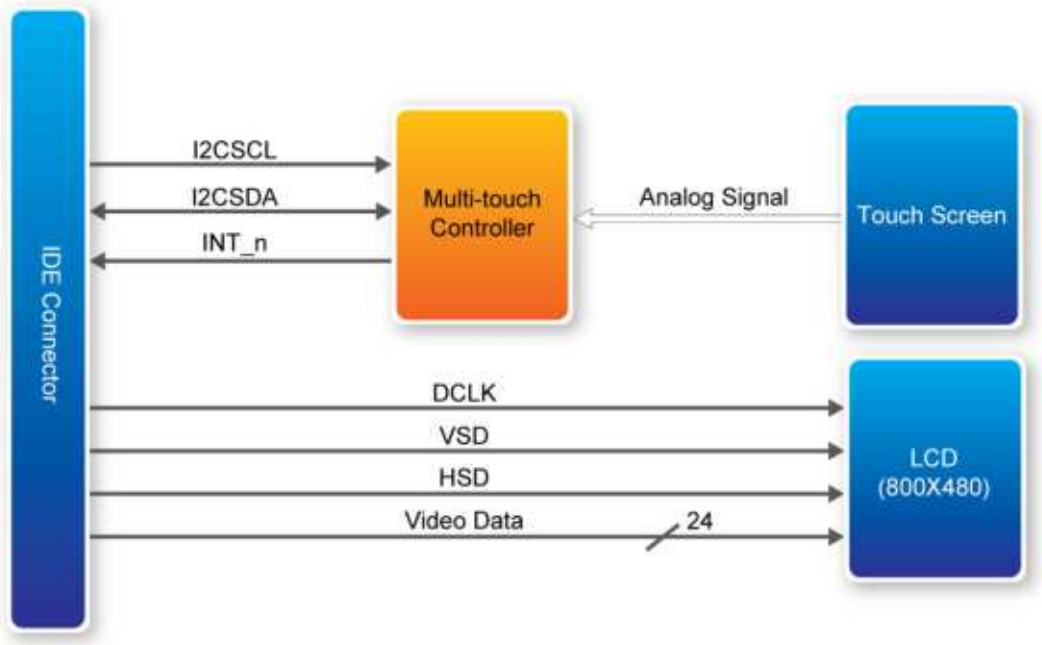


Figure 2-3 Block Diagram of MTL

Figure 2-4 illustrates the connection for MTL to the Terasic FPGA boards.

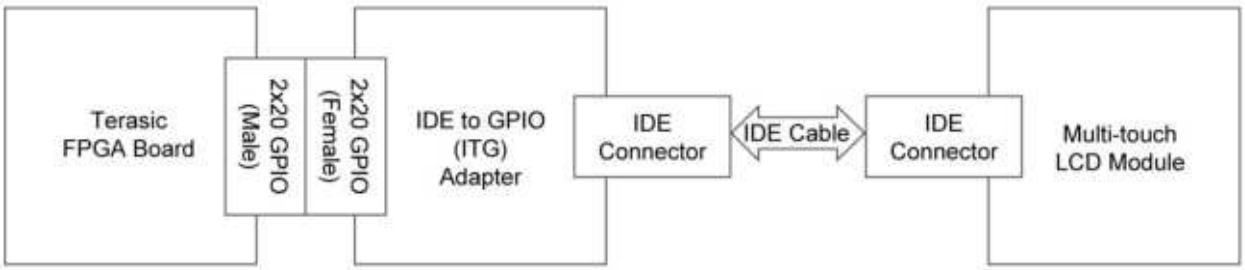


Figure 2-4 Connection Diagram of MTL Kit with Terasic FPGA boards

2.4 IDE Cable

The connection cable included is a standard IDE cable. However, to achieve the best performance, we strongly recommend users use the bundled IDE cable only. Third-party IDE cables may cause the MTL to malfunction, or even damage the module. The IDE cable is shown in Figure 2-5.



Figure 2-5 IDE cable

2.5 ITG Adapter

The IDE to GPIO (ITG) adapter is designed to remap IDE pins to GPIO pins.

Component and Layout

Figure 2-6 and Figure 2-7 show the top view and bottom view of ITG adapter, respectively.

The J1 connector is used to connect the FPGA board. The J2 connector is used to interface with the IDE cable.

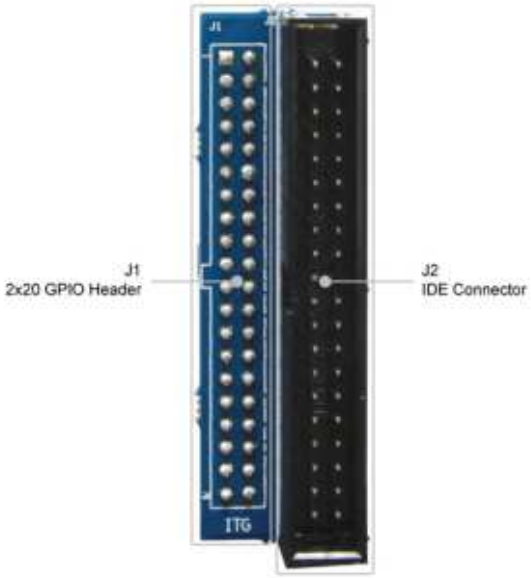


Figure 2-6 ITG Adapter (Top View)

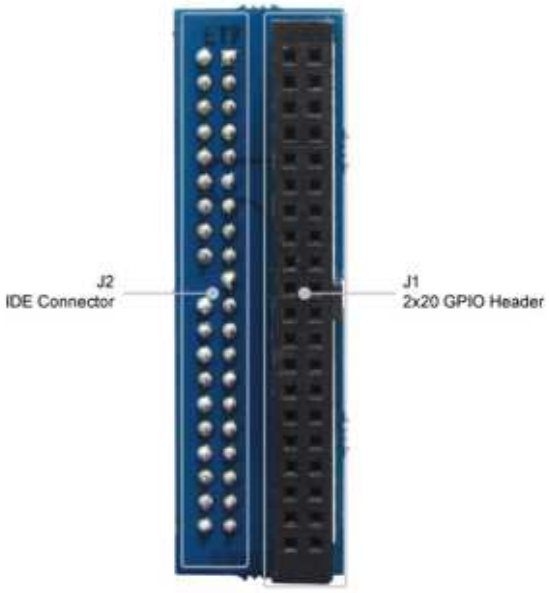


Figure 2-7 ITG Adapter (Bottom View)

Chapter 3

Using the MTL

This chapter provides information on how to control the Multi-touch LCD Module (MTL) hardware, including definition of 2x20 GPIO interface, LCD control, and multi-touch control signals.

3.1 Pin Definition of 2x20 GPIO Connector

The 2x20 GPIO female connector is designed to directly connect to the 2x20 GPIO male connector on the Terasic FPGA development boards. Figure 3-1 shows the signal names of the 2x20 GPIO from the ITG adapter.

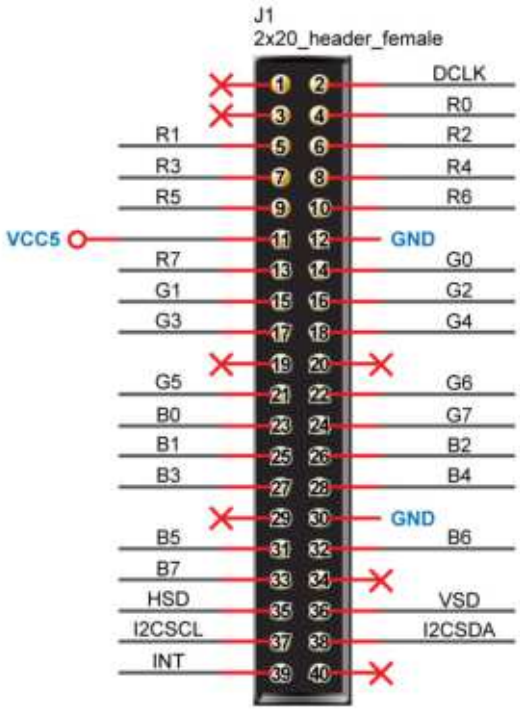


Figure 3-1 2x20 GPIO

Table 3-1 shows the recommended pin assignments for the 2x20 GPIO pins in Quartus II.

Table 3-1 Recommended Pin Assignments of 2x20 GPIO in Quartus II

Pin Numbers	*Pin Name*	*Direction*	*IO Standard*
1	-	-	-
2	MTL_DCLK	Output	3.3-V LVTTL
3	-	-	-
4	MTL_R[0]	Output	3.3-V LVTTL
5	MTL_R[1]	Output	3.3-V LVTTL
6	MTL_R[2]	Output	3.3-V LVTTL
7	MTL_R[3]	Output	3.3-V LVTTL
8	MTL_R[4]	Output	3.3-V LVTTL
9	MTL_R[5]	Output	3.3-V LVTTL
10	MTL_R[6]	Output	3.3-V LVTTL
11	-	-	-
12	-	-	-
13	MTL_R[7]	Output	3.3-V LVTTL
14	MTL_G[0]	Output	3.3-V LVTTL
15	MTL_G[1]	Output	3.3-V LVTTL
16	MTL_G[2]	Output	3.3-V LVTTL
17	MTL_G[3]	Output	3.3-V LVTTL
18	MTL_G[4]	Output	3.3-V LVTTL
19	-	-	-
20	-	-	-
21	MTL_G[5]	Output	3.3-V LVTTL
22	MTL_G[6]	Output	3.3-V LVTTL
23	MTL_B[0]	Output	3.3-V LVTTL
24	MTL_G[7]	Output	3.3-V LVTTL
25	MTL_B[1]	Output	3.3-V LVTTL
26	MTL_B[2]	Output	3.3-V LVTTL
27	MTL_B[3]	Output	3.3-V LVTTL
28	MTL_B[4]	Output	3.3-V LVTTL
29	-	-	-
30	-	-	-
31	MTL_B[5]	Output	3.3-V LVTTL
32	MTL_B[6]	Output	3.3-V LVTTL
33	MTL_B[7]	Output	3.3-V LVTTL
34	-	-	-
35	MTL_HSD	Output	3.3-V LVTTL
36	MTL_VSD	Output	3.3-V LVTTL
37	MTL_TOUCH_I2C_SCL	Output	3.3-V LVTTL
38	MTL_TOUCH_I2C_SDA	Inout	3.3-V LVTTL
39	MTL_TOUCH_INT_n	Input	3.3-V LVTTL
40	-	-	-

3.2 Using LCD

The LCD features 800x480 pixel resolution, and runs a 33 MHz pixel rate. No configuration is required to drive the LCD. The timing specification is defined as in the Table 3-2.

Table 3-2 LCD Timing

Item	*Typical Value*	*Unit*
Pixel Rate	33	MHz
Horizontal Period	1056	Pixel
Horizontal Pulse Width	30	Pixel
Horizontal Back Porch	16	Pixel
Horizontal Front Porch	210	Pixel
Horizontal Valid	800	Pixel
Vertical Period	525	Line
Vertical Pulse Width	13	Line
Vertical Back Porch	10	Line
Vertical Front Porch	22	Line
Vertical Valid	480	Line

3.3 Using Terasic Multi-touch IP

Terasic Multi-touch IP is provided for developers to retrieve user inputs, including multi-touch gestures and single-touch. The file name of this IP is **i2c_touch_config** and it is encrypted. To compile projects with the IP, users need to install the IP license first. For license installation, please refer to Chapter 1 in this document. The license file is located at:

MTL System CD\License\license_multi_touch.dat

The IP decodes I2C information and outputs coordinate and gesture information. The IP interface is shown below:

```
module i2c_touch_config  (
            // Host Side
            iCLK,
            iRSTN,
            iTRIG,
            oREADY,
            oREG_X1,
            oREG_Y1,
            oREG_X2,
            oREG_Y2,
            oREG_TOUCH_COUNT,
            oREG_GESTURE,
            // I2C Side
            I2C_SCLK,
            I2C_SDAT
);
```

The signal purpose of the IP is described in **Table 3-3.** The IP requires a 50 MHz signal as a reference clock to the **iCLK** pin and system reset signal to **iRSTN**. **iTRIG**, **I2C_SCLK**, and **IC2_SDAT** pins should be connected of the MTL_TOUCH_INT_n, MTL_TOUCH_I2C_SCL, and MTL_TOUCH_I2C_DAT signals in the 2x20 GPIO header respectively. When **oREADY** rises, it means there is touch activity, and associated information is given in the oREG_X1, oREG_Y1, oREG_X2, oREG_Y2, oREG_TOUCH_COUNT, and oREG_GESTURE pins.

For the control application, when touch activity occurs, it should check whether the value of oREG_GESTURE matched a pre-defined gesture ID defined in **Table 3-3**. If it is not a gesture, it means a single-touch has occurred and the relative X/Y coordinates can be derived from oREG_X1 and oREG_Y1.

Table 3-3 Interface Definitions of Terasic Multi-touch IP

Pin Name	*Direction*	*Description*
iCLK	Input	Connect to 50MHz Clock
iRSTN	Input	Connect to system reset signal
iTRIG	Input	Connect to Interrupt Pin of Touch IC
oREADY	Output	Rising Trigger when following six output data is valid
oREG_X1	Output	10-bits X coordinate of first touch point
oREG_Y1	Output	9-bits Y coordinate of first touch point
oREG_X2	Output	10-bits X coordinate of second touch point
oREG_Y2	Output	9-bits Y coordinate of second touch point
oREG_TOUCH_COUNT	Output	2-bits touch count. Valid value is 0, 1, or 2.
oREG_GESTURE	Output	8-bits gesture ID (See Table 3-4)
I2C_SCLK	Output	Connect to I2C Clock Pin of Touch IC
I2C_SDAT	Inout	Connect to I2C Data Pin of Touch IC

The supported gestures and IDs are shown in **Table 3-4**.

Table 3-4 Gestures

Gesture	*ID (hex)*
One Point Gesture	
North	0x10
North-East	0x12
East	0x14
South-East	0x16
South	0x18
South-West	0x1A
West	0x1C
North-West	0x1E
Rotate Clockwise	0x28
Rotate Anti-clockwise	0x29
Click	0x20
Double Click	0x22

Two Point Gesture	
North	0x30
North-East	0x32
East	0x34
South-East	0x36
South	0x38
South-West	0x3A
West	0x3C
North-West	0x3E
Click	0x40
Zoom In	0x48
Zoom Out	0x49

Note: The Terasic IP Multi-touch IP can also be found under the \IP folder in the system CD as well as the \IP folder in the reference designs.

Chapter 4

ePhoto Demonstration

This chapter describes how to use MTL to design a simple photo viewer. The demonstration can support the following Terasic FPGA boards:

- DE2-115
- DE2

4.1 Operation Description

This demonstration implements a simple photo viewer. Before running this demonstration, three 800x480 photos should be vertically merged into one 800x1440 photo and be stored in FLASH of the FPGA board in advance. In this demonstration, users can browse each photo by using single touch west or east gesture to select the previous or next photo, as shown in **Figure 4-1.**



Figure 4-1 Select Next Photo by East Gesture

Also, users can use two-point zoom-in and zoom-out gestures to zoom the photo displayed, as shown in **Figure 4-2.**



Figure 4-2 Zoom-in using Zoom-in Gesture

4.2 Block Diagram of the ePhoto Design

This section describes the block diagram of the ePhoto demonstration to give users a better understanding of the code provided.

Figure 4-3 shows the block diagram of the ePhoto demonstration. When the demonstration starts up, the system will control the ***Flash Controller*** to read the RGB data of three photos stored in the FLASH, and write the data into SDRAM by using the writing port of the ***SDRAM***. The ***SDRAM Controller*** provides two reading ports and two writing ports. In this demonstration, only one reading port and one write porting are used. To display the selected photo on the 800x480 LCD, the ***VGA Controller*** will retrieve the photo data via reading the port of the ***SDRAM***, and drive the LCD display with the retrieved photo data. The ***VGA Controller*** retrieves the photo data at a rate of 60 photos per second. ***Zoom*** handles the photo zooming process. The displayed photo is zoomed before being sent to the LCD display.

When users touch the MTL screen, ***I2C Touch Config*** will receive an interrupt signal from the touch screen. When an interrupt is detected, ***I2C Touch Config*** will read touch information from the touch panel and assert the oREADY signal. When ***Touch Controller*** detects a rising signal of oREADY, it will read touch information and determine the input, which may be a gesture or a single-point touch. If a west or east gesture is detected, it will change the reading port address of the desired active photo in the ***SDRAM Controller***. If a zoom-in or zoom-out gesture is detected, it will change the zooming factor in ***Zoom***.

For multi-touch gesture processing, a Terasic Memory-Mapped IP ***I2C_Touch_Config*** is used to retrieve the touch information. For IP-usage details, please refer to the Chapter 3 in this document. Note: the IP is encrypted, so the license should be installed before compiling the Quartus II project.

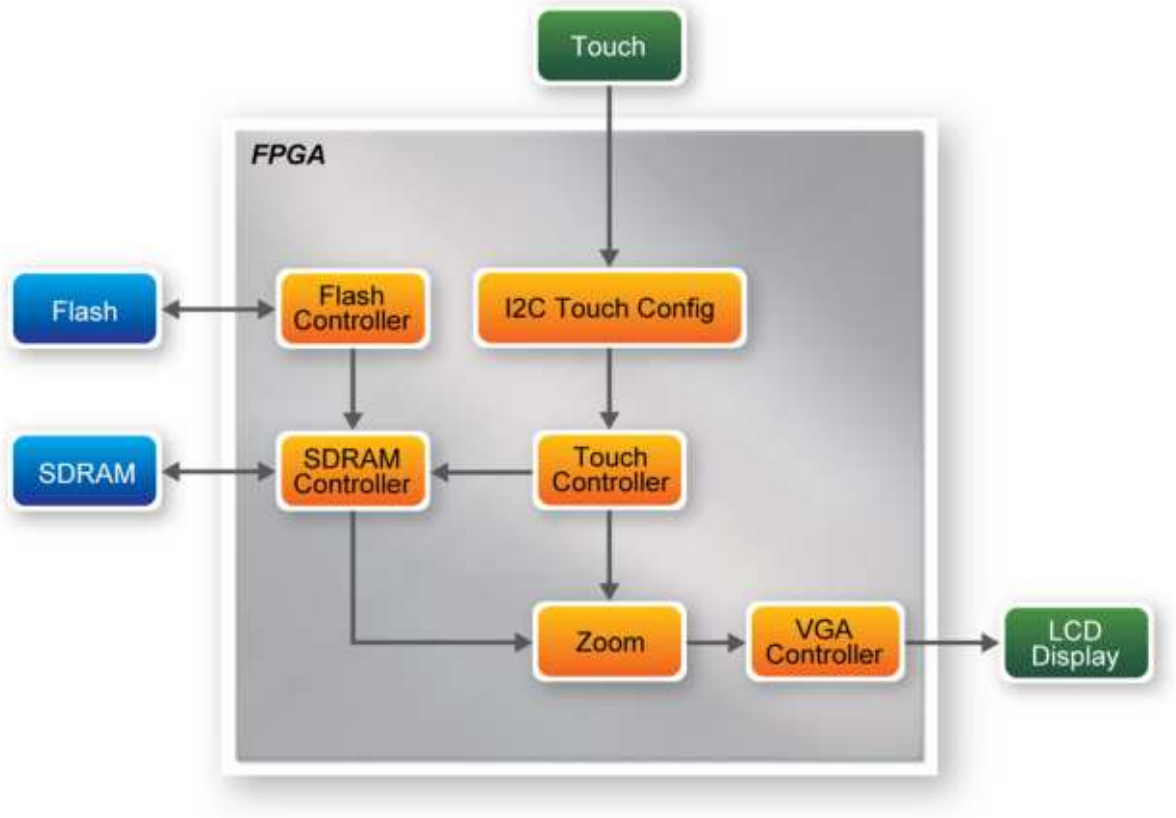


Figure 4-3 The Block Diagram of the ePhoto Demonstration

4.3 Loading Photos into FLASH

Before executing the demonstration, users have to utilize the Control Panel software to load photos into the FLASH of the FPGA board first. The Control Panel software is available in the CD of the FPGA development kit. Table 4-1 shows the respective Control Panel names and bitstreams for various FPGA development boards.

Table 4-1 Control Panel Names and Bitstreams for Various FPGA Boards

FPGA Board	*Control Panel Name*	*FPGA Bitstream*
DE2-115	DE2_115_Control_Panel	DE2_115_ControlPanel.sof
DE2	DE2_Control_Panel_V1.04	DE2_USB_API.sof

Procedure for loading photos to FLASH:

1. Make sure the USB-Blaster download cable is connected to the host PC.
2. Power on the FPGA Development Board.
3. Execute the Control Panel application software. Please refer to the user manual of the FPGA development kit for more information for the Control Panel software.
4. Switch to the FLASH page and click on the “Chip Erase (xx Sec)” button to erase FLASH data.
5. Click on the “File Length” checkbox to indicate that you want to load the entire file.
6. Click on the “Write a File to FLASH” button. When the Control Panel responds with the standard Windows dialog box and asks for the source file, select the “DEMO.raw” file in the “Demonstrations\RTL\Photo” directory
7. When loading is completed, a prompt will appear indicating success.

4.4 Demonstration for Terasic DE2-115 FPGA Board

This section shows how to setup the painter demo on the Terasic DE2-115 FPGA Board. For other Terasic FPGA boards, the setup procedures are similar.

Hardware Setup

The demonstration configuration is as shown in **Figure 4-4.** Make sure the ITG adapter is connected firmly to the IDE cable. Plug the ITG adapter into the GPIO-0 header of the FPGA development kit from MTL before turning on. Important: Plug the MTL power adaptor into the power connector of MTL unless the DE2-115 FPGA board is used.

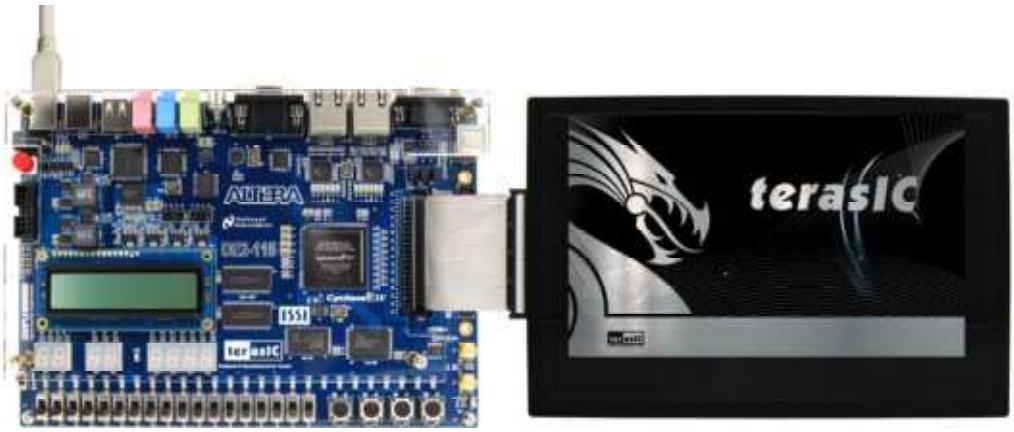


Figure 4-4 ePhoto Configuration Setup

Execute Demonstration

Procedure to execute demonstration:

1. Make sure the DE2-115 is powered off.
2. Mount the ITG adapter onto the 2x20 GPIO 0 expansion header of the DE2-115.
3. Connect the DE2-115 USB-Blaster USB port to the PC USB Port with a USB Cable.
4. Power on the DE2-115* FPGA Development Board.
5. Make sure Quartus II 10.1 and NIOS II 10.1 are installed in your system.
6. If you haven't already, store pictures into the flash memory. For more detailed instructions please refer to section *4.3 Loading Photos into FLASH*.
7. Copy the folder Demonstrations\RTL\DE2_115_EPHOTO\demo_batch in the MTL System CD onto your system and execute "test.bat".
8. A photo should be displayed in the LCD, as shown in **Figure 4-5**.
9. Slide left or right with one finger on the touch panel to display the previous and next photos respectively.
10. Slide with two fingers in the opposite direction to zoom-in on the picture and pinch two fingers together to zoom the picture out.

*Note: Please attach the 5V USB power adapter when using the DE2 FPGA Development Board.

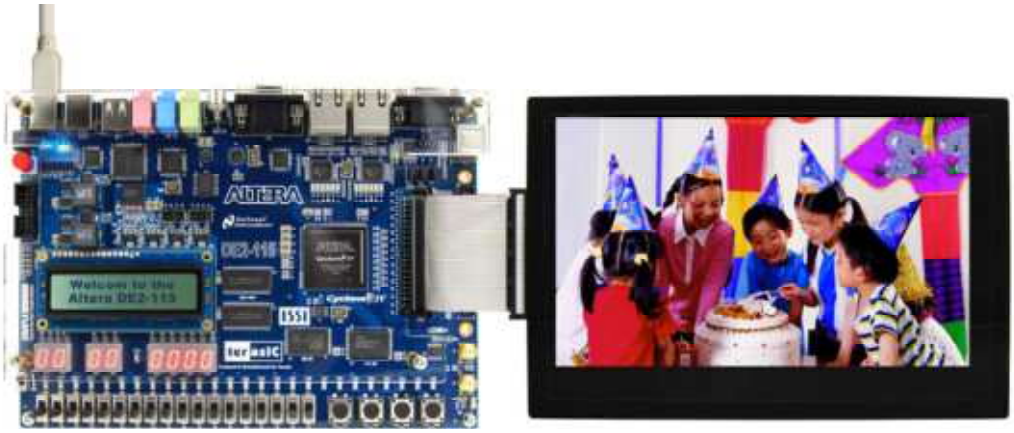


Figure 4-5 Photo Display

Table 4-2 lists the demonstration bitstream files for various Terasic FPGA boards.

Table 4-2 Bitstream Files for Various FPGA Boards

FPGA Board	*Quartus II Project Directory*	*FPGA Bitstream Used*
DE2-115	Demonstrations\RTL\DE2_115_MTL_EPHOTO	MTL_DEMO.sof
DE2	Demonstrations\RTL\DE2_MTL_ EPHOTO	DE2_MTL.sof

4.5 Custom Display Photo

Procedure for creating custom photos for ePhoto:

1. Prepare three 24-bit *bitmap* format photos with image resolutions of 800 (width) x 480 (height) pixels for each, as shown in **Figure 4-6.**



Figure 4-6 Original Photo Resolution

2. Use image processing software to vertically merge the three photos into a new photo image with 24-bits color *bitmap* format. The merged photo resolution should be 800 (width) x 1440 (height) pixels, as shown in **Figure 4-7.**
3. Use the tool "bmp_to_raw.exe" in the "Demonstrations\RTL\Photo" directory to convert the picture to raw file.



Figure 4-7 Photo Format for the ePhoto Demonstration

Chapter 5

Painter Demonstration

This chapter shows how to implement a painter demo on the Multi-Touch LCD Module based on SOPC Builder and the Altera's Video and Image Processing Suite (VIP). The design demonstrates how to use multi-touch gestures and single-touch. The demonstration requires the following hardware:

- Terasic FPGA Board
- Multi-touch LCD Module

5.1 Operation Description

Figure 5-1 shows the Graphical User Interface (GUI) of the Painter Demo. The GUI is classified into four separate areas: Painting Area, Gesture Indicator, Clear Button, and Color Palette. Users can select a pen color from the color palette and start painting in the paint area. If a gesture is detected, the associated gesture symbol is shown in the gesture area. To clear the painting area, click the "Clear" button.

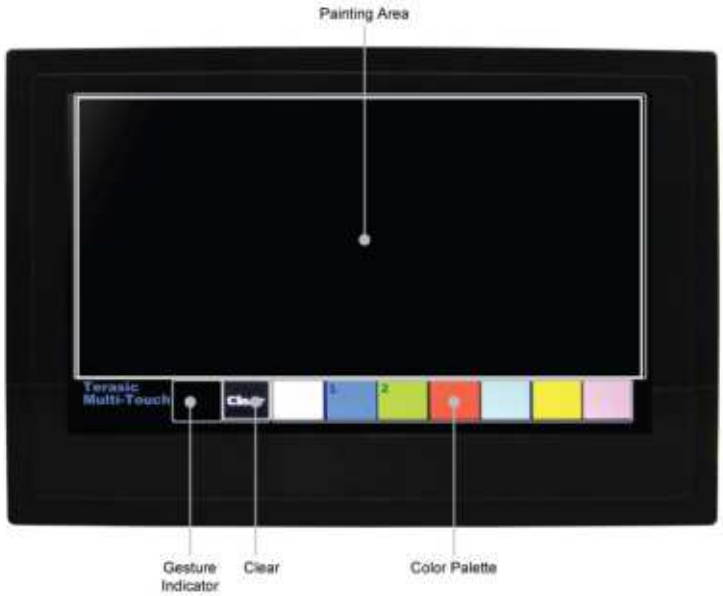


Figure 5-1 GUI of Painter Demo

Figure 5-2 displays the single-finger painting of the canvas area.



Figure 5-2 Single-finger Painting

Figure 5-3 displays the counter-clockwise rotation gesture.



Figure 5-3 Counter-clockwise Rotation Gesture

Figure 5-4 shows the zoom-in gesture.



Figure 5-4 Zoom-in Gesture

5.2 System Description

For LCD display processing, the reference design is developed based on Altera's Video and Image Processing Suite (VIP). The Frame Reader VIP is used for reading display content from the associated video memory, and VIP Video Out is used to display the display content. The display content is drawn by the NIOS II processor according to user input.

For multi-touch processing, a Terasic Memory-Mapped IP is used to retrieve the user input, including multi-touch gestures and single-touch coordinates. For IP--usage details please refer to the Chapter Three in this document. Note: the IP is encrypted, so the license should be installed before compiling the Quartus II project.

Figure 5-5 shows the system generic block diagram of demonstration reference design.

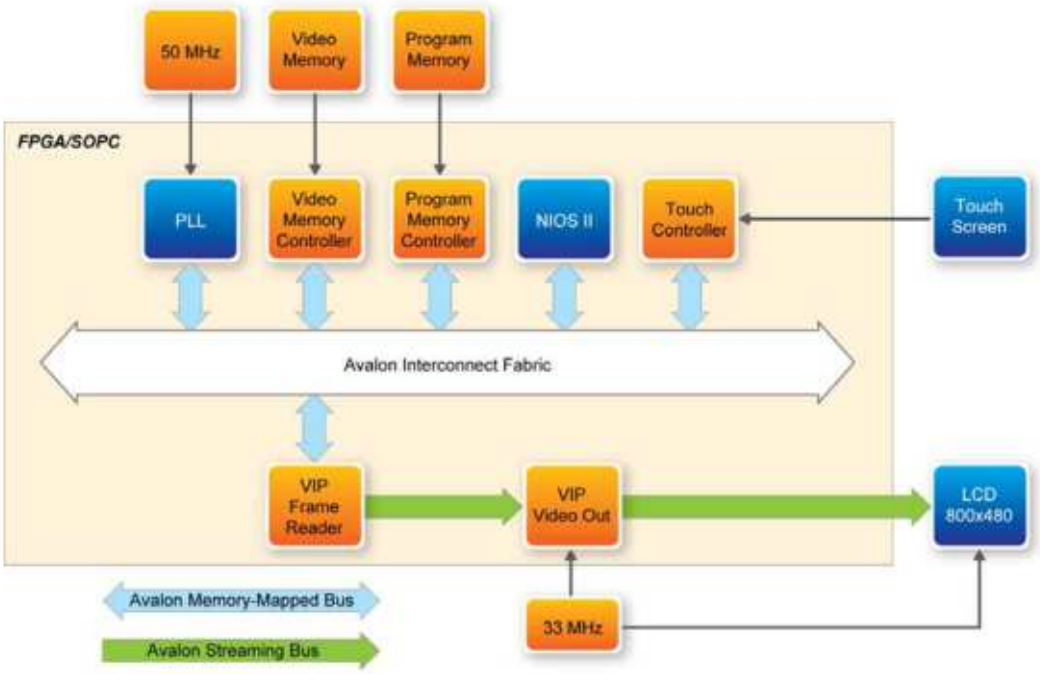


Figure 5-5 System Block Diagram

5.3 Demonstration for Terasic DE2-115 FPGA Board

This section shows how to setup the painter demo on the Terasic DE2-115 FPGA Board. For other Terasic FPGA boards, the setup procedures are similar.

Hardware Setup



Figure 5-6 Hardware Setup with DE2-115

Execute Demonstration

Please follow the procedures below to setup the demonstration:

1. Make sure the DE2-115 is powered off.
2. Mount the ITG adapter onto the 2x20 GPIO 0 expansion header of the DE2-115.
3. Connect the DE2-115 USB-Blaster USB-B port to the PC USB Port with a USB Cable.
4. Power on the DE2-115* FPGA Development Board.
5. Make sure Quartus II 10.1 and NIOS II 10.1 are installed on your system.
6. Copy the folder Demonstrations/SOPC/DE2_115_SOPC_MTL_PAINTER/demo_batch in the MTL System CD onto your system and execute “test.bat”.
7. Now, you should see the painter GUI on the LCD.

*Note: Please attach the 5V USB power adapter when using the DE2 FPGA Development Board.

5.4 Demonstration Source Code

The source code locations of this demonstration for the various Terasic FPGA boards are shown in **Table 5-1.** Note: The project is built under Quartus II 10.1, and both Altera VIP license and Terasic Multi-Touch IP license are required for rebuilding the project.

Table 5-1 Source Code Locations of Painter Demonstration

FPGA Board	*Location*
DE2	Demonstrations\SOPC\DE2_MTL_PAINTER
DE2-115	Demonstrations\SOPC\DE2_115_MTL_PAINTER

Chapter 6

Appendix

6.1 Revision History

Version	Change Log
V1.0	Initial Version (Preliminary)

6.2 Copyright Statement

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We will continue to provide interesting examples and labs on our MTL webpage. Please visit mtl.terasic.com for more information.