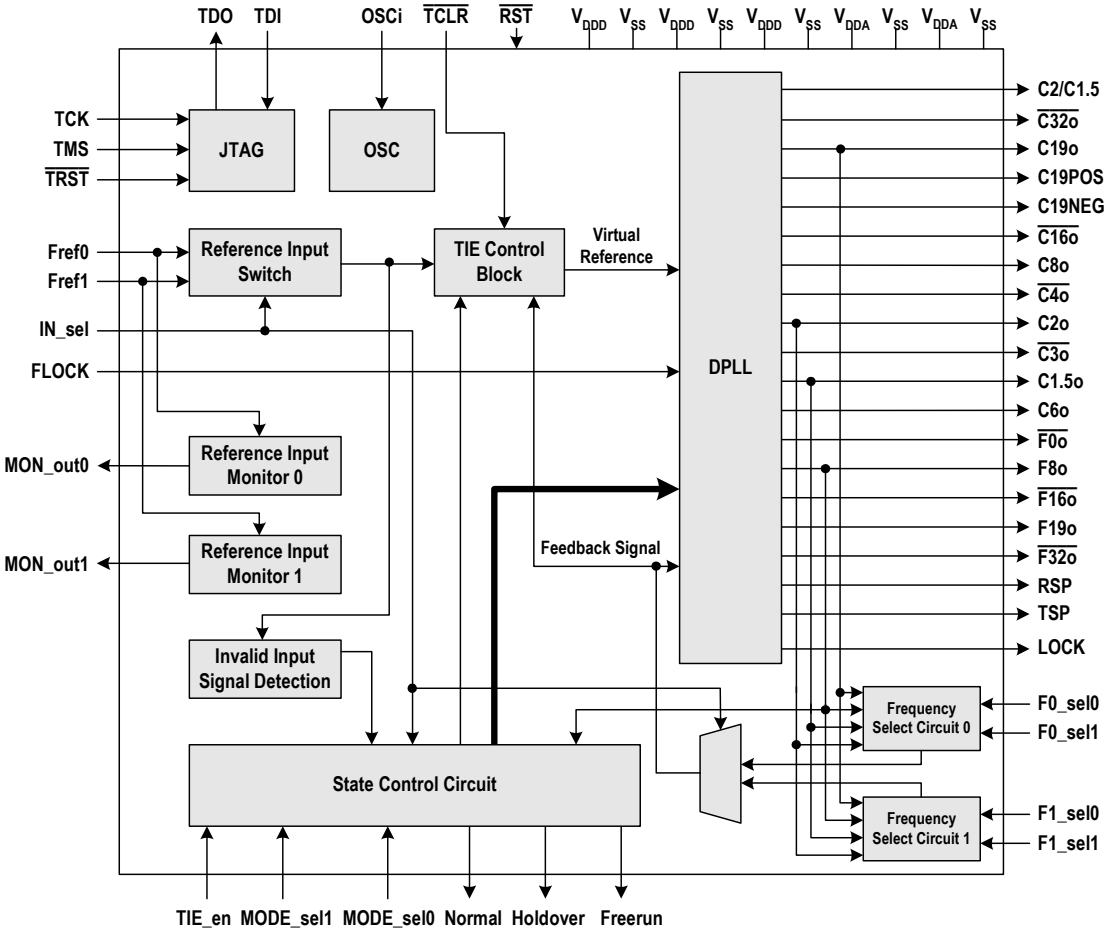
T1/E1/OC3 WAN PLL WITH DUAL REFERENCE INPUTS

IDT82V3012

FEATURES

- Supports AT&T TR62411 and Telcordia GR-1244-CORE Stratum 3, Stratum 4 Enhanced and Stratum 4 timing for DS1 interfaces
- Supports ITU-T G.813 Option 1 clocks
- Supports ITU-T G.812 Type IV clocks
- Supports ETSI ETS 300 011, TBR 4, TBR 12 and TBR 13 timing for E1 interface
- Selectable reference inputs: 8 kHz, 1.544 MHz, 2.048 MHz or 19.44 MHz
- Accepts two independent reference inputs which may have same or different nominal frequencies applied to them
- Provides C1.5o, $\overline{C3o}$, C2o, $\overline{C4o}$, C6o, C8o, $\overline{C16o}$, C19o and $\overline{C32o}$ output clock signals
- Provides 7 types of 8 kHz framing pulses: $\overline{F0o}$, F8o, $\overline{F16o}$, F19o, $\overline{F32o}$, RSP and TSP
- Provides a C2/C1.5 output clock signal with the frequency controlled by the selected reference input Fref0 or Fref1
- Holdover frequency accuracy of 0.025 ppm
- Phase slope of 5 ns per 125 µs
- Attenuates wander from 2.1 Hz
- Fast lock mode
- Provides Time Interval Error (TIE) correction
- MTIE of 600 ns
- JTAG boundary scan
- Holdover status indication
- Freerun status indication
- Normal status indication
- Lock status indication
- Input reference quality indication
- 3.3 V operation with 5 V tolerant I/O
- Package available: 56-pin SSOP (Green option available)

FUNCTIONAL BLOCK DIAGRAM



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DESCRIPTION

The IDT82V3012 is a T1/E1/OC3 WAN PLL with dual reference inputs. It contains a Digital Phase-Locked Loop (DPLL), which generates low jitter ST-BUS and 19.44 MHz clock and framing signals that are phase locked to an 8 kHz, 1.544 MHz, 2.048 MHz or 19.44 MHz input reference.

The IDT82V3012 provides 9 types of clock signals (C1.5o, $\overline{C3o}$, C6o, C2o, $\overline{C4o}$, C8o, $\overline{C16o}$, C19o, $\overline{C32o}$) and 7 types of framing signals ($\overline{F0o}$, F8o, $\overline{F16o}$, F19o, $\overline{F32o}$, RSP, TSP) for multitrunk T1/E1 and STS3/OC3 links.

The IDT82V3012 is compliant with AT&T TR62411, Telcordia GR-1244-CORE Stratum 3, Stratum 4 Enhanced and Stratum 4, ETSI ETS 300 011, ITU-T G.813 Option 1, and ITU-T G.812 Type IV clocks. It meets the jitter/wander tolerance, jitter/wander transfer, intrinsic jitter/wander, frequency accuracy, capture range, phase change slope, holdover frequency accuracy and MTIE (Maximum Time Interval Error) requirements for these specifications.

The IDT82V3012 can be used in synchronization and timing control for T1, E1 and OC3 systems, or used as ST-BUS clock and frame pulse source. It also can be used in access switch, access routers, ATM edge switches, wireless base station controllers, or IADs (Integrated Access Devices), PBXs, line cards and SONET/SDH equipments.

PIN CONFIGURATION

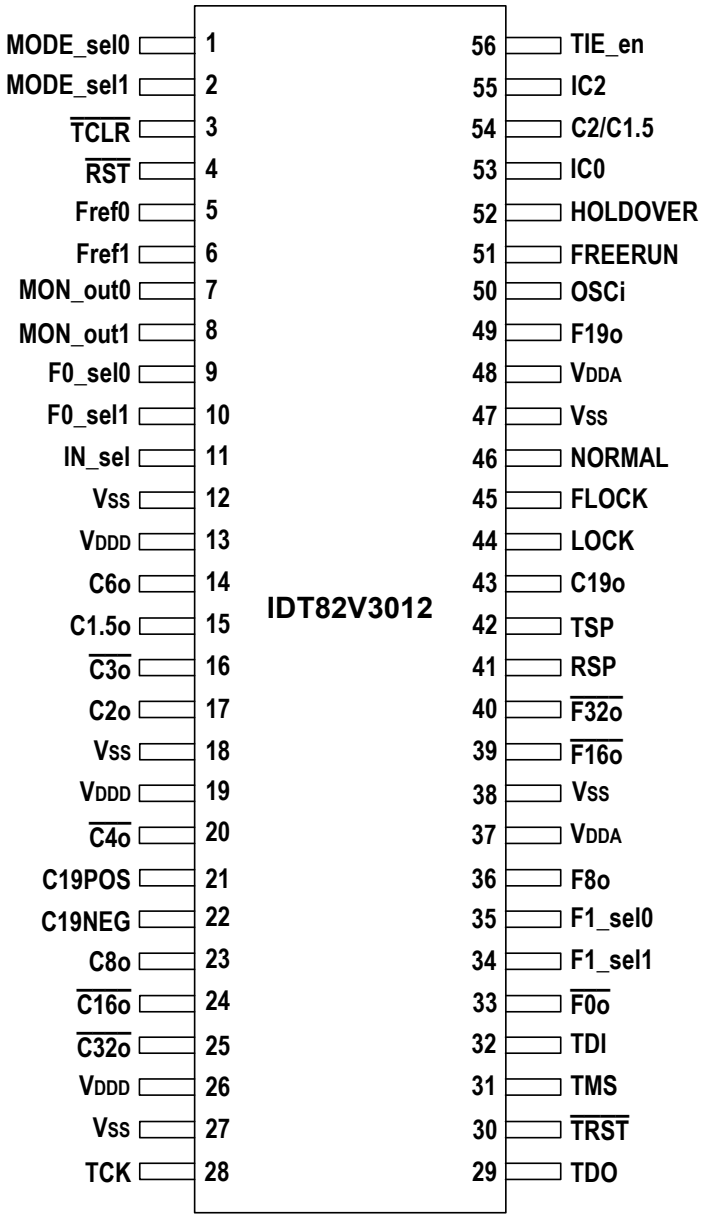


Figure - 1 IDT82V3012 SSOP56 Package Pin Assignment

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TABLE OF CONTENTS

1 Pin Description 7

2 Functional Description 10
2.1 State Control Circuit 10
2.1.1 Normal Mode 11
2.1.2 Fast Lock Mode 11
2.1.3 Holdover Mode 11
2.1.4 Freerun Mode 11
2.2 Frequency Select Circuit 11
2.3 Reference Input Switch 11
2.4 Reference Input Monitor 12
2.5 Invalid Input Signal Detection 12
2.6 TIE Control Block 12
2.7 DPLL Block 13
2.7.1 Phase Detector (PHD) 13
2.7.2 Limiter 13
2.7.3 Loop Filter 14
2.7.4 Fraction Block 14
2.7.5 Digital Control Oscillator (DCO) 14
2.7.6 Lock Indicator 14
2.7.7 Output Interface 14
2.8 OSC 15
2.8.1 Clock Oscillator 15
2.9 JTAG 15
2.10 Reset, Lock and TIE Application 15
2.11 Power Supply Filtering Techniques 16

3 Measures of Performance 17
3.1 Intrinsic Jitter 17
3.2 Jitter Tolerance 17
3.3 Jitter Transfer 17
3.4 Frequency Accuracy 17
3.5 Holdover Accuracy 17
3.6 Capture Range 17
3.7 Lock Range 17
3.8 Phase Slope 17
3.9 Time Interval Error (TIE) 17
3.10 Maximum Time Interval Error (MTIE) 17
3.11 Phase Continuity 18
3.12 Phase Lock Time 18

4 Absolute Maximum Ratings 19

5 Recommended DC Operating Conditions 19

6 DC Electrical Characteristics 19
6.1 Single End Input/Output Port 19
6.2 Differential Output Port (LVDS) 20

7 AC Electrical Characteristics 21
7.1 Performance 21
7.2 Intrinsic Jitter Unfiltered 22
7.3 C1.5o (1.544 MHz) Intrinsic Jitter Filtered 22
7.4 C2o (2.048 MHz) Intrinsic Jitter Filtered 22
7.5 C19o (19.44 MHz) Intrinsic Jitter Filtered 22
7.6 8 kHz Input to 8 kHz Output Jitter Transfer 23
7.7 1.544 MHz Input to 1.544 MHz Output Jitter Transfer 23
7.8 2.048 MHz Input to 2.048 MHz Output Jitter Transfer 23

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7.9 19.44 MHz Input to 19.44 MHz Output Jitter Transfer 24
7.10 8 kHz Input Jitter Tolerance 24
7.11 1.544 MHz Input Jitter Tolerance 24
7.12 2.048 MHz Input Jitter Tolerance 25
7.13 19.44 MHz Input Jitter Tolerance 25

8 Timing Characteristics 27
8.1 Timing Parameter Measurement Voltage Levels 27
8.2 Input/Output Timing 27

9 Ordering Information 32

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LIST OF FIGURES

Figure - 1 IDT82V3012 SSOP56 Package Pin Assignment 2
Figure - 2 State Control Circuit 10
Figure - 3 State Control Diagram 10
Figure - 4 TIE Control Block Diagram 12
Figure - 5 Reference Switch with TIE Control Block Enabled 13
Figure - 6 Reference Switch with TIE Control Block Disabled 13
Figure - 7 DPLL Block Diagram 14
Figure - 8 Clock Oscillator Circuit 15
Figure - 9 Power-Up Reset Circuit 16
Figure - 10 IDT82V3012 Power Decoupling Scheme 16
Figure - 11 Timing Parameter Measurement Voltage Levels 27
Figure - 12 Input to Output Timing (Normal Mode) 29
Figure - 13 Output Timing 1 30
Figure - 14 Output Timing 2 31
Figure - 15 Input Control Setup and Hold Timing 31

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LIST OF TABLES

Table - 1 Operating Modes Selection 10
Table - 2 Fref0 Frequency Selection 11
Table - 3 Fref1 Frequency Selection 11
Table - 4 Input Reference Selection 12
Table - 5 C2/C1.5 Output Frequency Control 15

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1 PIN DESCRIPTION

Name	Type	Pin Number	Description
V_{SS}	Power	12, 18, 27 38, 47	**Ground.** 0 V. All V_{SS} pins should be connected to the ground.
V_{DDA}	Power	37, 48	**3.3 V Analog Power Supply.** Refer to Chapter 2.11 Power Supply Filtering Techniques.
V_{DDD}	Power	13, 19, 26	**3.3 V Digital Power Supply.** Refer to Chapter 2.11 Power Supply Filtering Techniques.
OSCi	(CMOS) I	50	**Oscillator Master Clock Input.** This pin is connected to a clock source.
Fref0 **Fref1**	I	5 6	**Reference Input 0 and Reference Input 1.** These are two input reference sources (falling edge of 8 kHz, 1.544 MHz and 2.048 MHz or rising edge of 19.44 MHz) used for synchronization. The IN_sel pin determines which one of the two reference inputs to be used. See Table - 4 for details. The frequency of the reference inputs can be 8 kHz, 1.544 MHz, 2.048 MHz or 19.44 MHz. These two pins are internally pulled up to V_{DDD}.
IN_sel	I	11	**Input Reference Selection.** A logic low at this pin selects Reference Input 0 (Fref0) and a logic high at this pin selects Reference Input 1 (Fref1). The logic level on this input is gated in by the rising edges of F8o. This Pin is internally pulled down to V_{SS}.
F0_sel0 **F0_sel1**	I	9 10	**Frequency Selection Inputs for Fref0.** These two inputs select one of the four possible frequencies (8 kHz, 1.544 MHz, 2.048 MHz or 19.44 MHz) for the Reference Input 0 (Fref0). See Table - 2 for details.
F1_sel0 **F1_sel1**	I	35 34	**Frequency Selection Inputs for Fref1.** These two inputs select one of the four possible frequencies (8 kHz, 1.544 MHz, 2.048 MHz or 19.44 MHz) for the Reference Input 1 (Fref1). These two pins are internally pulled down to V_{ss}. See Table - 3 for details.
MODE_sel0 **MODE_sel1**	I	1 2	**Mode Selection Inputs.** These two inputs determine the operating mode of the IDT82V3012 (Normal, Holdover or Freerun). See Table - 1 for details. The logic levels on these two pins are gated in by the rising edges of F8o. These two pins are internally pulled down to V_{SS}.
$\overline{RST}$	I	4	**Reset Input.** Pulling this pin to logic low for at least 300 ns will reset the IDT82V3012. While the $\overline{RST}$ pin is low, all framing and clock outputs are at logic high. To ensure proper operation, the device must be reset after it is powered up.
$\overline{TCLR}$	I	3	**TIE Control Block Reset.** Pulling this pin to logic low for at least 300 ns will reset the TIE (Maximum Time Interval Error) control block and result in a realignment of the output phase with the input phase. This pin is internally pulled up to V_{DDD}.
TIE_en	I	56	**TIE Control Block Enable.** A logic high at this pin enables the TIE control block while a logic low disables it. The logic level on this input is gated in by the rising edges of F8o. This pin is internally pulled down to V_{ss}.
FLOCK	I	45	**Fast Lock Mode Enable.** When this pin is set to logic high, the DPLL will quickly lock to the input reference within 500 ms.
LOCK	(CMOS) O	44	**Lock Indicator.** This output pin will go high when the DPLL is frequency locked to the input reference.
HOLDOVER	(CMOS) O	52	**Holdover Indicator.** This output pin will go high whenever the DPLL enters Holdover mode.
NORMAL	(CMOS) O	46	**Normal Indicator.** This output pin will go high whenever the DPLL enters Normal mode.
FREERUN	(CMOS) O	51	**Freerun Indicator.** This output pin will go high whenever the DPLL enters Freerun mode.
MON_out0	O	**7**	**Frequency Out-of-range Indicator for Fref0.** A logic high at this pin indicates that Fref0 is off the nominal frequency by more than ±12 ppm.
MON_out1	O	**8**	**Frequency Out-of-range Indicator for Fref1.** A logic high at this pin indicates that Fref1 is off the nominal frequency by more than ±12 ppm.

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Name	Type	Pin Number	Description
C19POS C19NEG	(LVDS) O	21 22	**19.44 MHz Clock Output (LVDS Level).** This pair of outputs is used for OC3/STS3 applications.
C19o	(CMOS) O	43	**19.44 MHz Clock Output (CMOS Level).** This output is used for OC3/STS3 applications.
$\overline{\text{C32o}}$	(CMOS) O	25	**32.768 MHz Clock Output.** This output is a 32.768 MHz clock used for ST-BUS operation.
$\overline{\text{C16o}}$	(CMOS) O	24	**16.384 MHz Clock Output.** This output is a 16.384 MHz clock used for ST-BUS operation.
C8o	(CMOS) O	23	**8.192 MHz Clock Output.** This output is an 8.192 MHz clock used for ST-BUS operation.
$\overline{\text{C4o}}$	(CMOS) O	20	**4.096 MHz Clock Output.** This output is a 4.096 MHz clock used for ST-BUS operation.
C2o	(CMOS) O	17	**2.048 MHz Clock Output.** This output is a 2.048 MHz clock used for ST-BUS operation.
$\overline{\text{C3o}}$	(CMOS) O	16	**3.088 MHz Clock Output.** This output is used for T1 applications.
C1.5o	(CMOS) O	15	**1.544 MHz Clock Output.** This output is used for T1 applications.
C6o	(CMOS) O	14	**6.312 MHz Clock Output.** This output is used for DS2 applications.
C2/C1.5	(CMOS) O	54	**2.048 MHz or 1.544 MHz Clock Output.** This output is a 2.048 MHz or 1.544 MHz clock signal. If the selected reference input (Fref0 or Fref1) is 8 kHz, 2.048 MHz, or 19.44 MHz, the C2/C1.5 pin will output a 2.048 MHz clock signal. If the frequency of the selected reference input (Fref0 or Fref1) is 1.544 MHz, the C2/C1.5 pin will output a 1.544 MHz clock signal. Refer to Table - 5 for details.
F19o	(CMOS) O	49	**8 kHz Frame Signal with 19.44 MHz Pulse Width.** This output is used for OC3/STS3 applications.
$\overline{\text{F32o}}$	(CMOS) O	40	**Frame Pulse ST-BUS 8.192 Mb/s.** This is an 8 kHz 30 ns active low framing pulse, which marks the beginning of an ST-BUS frame. This framing signal is typically used for ST-BUS operation at 8.192 Mb/s.
$\overline{\text{F16o}}$	(CMOS) O	39	**Frame Pulse ST-BUS 8.192 Mb/s.** This is an 8 kHz 61 ns active low framing pulse, which marks the beginning of an ST-BUS frame. This framing signal is typically used for ST-BUS operation at 8.192 Mb/s.
F8o	(CMOS) O	36	**Frame Pulse.** This is an 8 kHz 122 ns active high framing pulse, which marks the beginning of a frame.
$\overline{\text{F0o}}$	(CMOS) O	33	**Frame Pulse ST-BUS 2.048 Mb/s.** This is an 8 kHz 244 ns active low framing pulse, which marks the beginning of an ST-BUS frame. This framing signal is typically used for ST-BUS operation at 2.048 Mb/s and 4.096 Mb/s.
RSP	(CMOS) O	41	**Receive Sync Pulse.** This is an 8 kHz 488 ns active high framing pulse, which marks the beginning of a ST-BUS frame. This framing signal is typically used to connect to the Siemens MUNICH-32 device.
TSP	(CMOS) O	42	**Transmit Sync Pulse.** This is an 8 kHz 488 ns active high framing pulse, which marks the beginning of an ST-BUS frame. This framing is typically used to connect to the Siemens MUNICH-32 device.
TDO	(CMOS) O	29	**Test Serial Data Out.** JTAG serial data is output on this pin on the falling edge of TCK. This pin is held in high impedance state when JTAG scan is not enabled.
TDI	I	32	**Test Serial Data In.** JTAG serial test instructions and data are shifted in on this pin. This pin is internally pulled up to V_{DDD}.
$\overline{\text{TRST}}$	I	30	**Test Reset.** Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-Reset state. This pin is internally pulled up to V_{DDD}. It is connected to the ground for normal applications.
TCK	I	28	**Test Clock.** Provides the clock for the JTAG test logic.
TMS	I	31	**Test Mode Select.** JTAG signal that controls the state transitions of the TAP controller. This pin is internally pulled up to V_{DDD}.

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Name	Type	Pin Number	Description
IC0, IC2	-	53, 55	These pins should be connected to V_{SS}.

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2 FUNCTIONAL DESCRIPTION

The IDT82V3012 is a T1/E1/OC3 WAN PLL with dual reference inputs, providing timing (clock) and synchronization (framing) signals to interface circuits for multitrunk T1/E1 and STS3/OC3 links. The details are described in the following sections.

2.1 STATE CONTROL CIRCUIT

The State Control Circuit is an important part in the IDT82V3012. It is used to control the TIE block and the DPLL block as shown in Figure - 2. The control is based on the result of Invalid Input Signal Detection and the logic levels on the MODE_sel0, MODE_sel1, IN_sel and TIE_en pins.

The IDT82V3012 can be operated in three different modes: Normal, Holdover and Freerun. The operating mode is selected by the MODE_sel1 and MODE_sel0 pins, as shown in Table - 1.

Figure - 3 shows the state control diagram. All state changes occur synchronously on the rising edge of F8o. Three operating modes, Normal (S1), Holdover (S3) and Freerun (S0) can be switched from one to another by changing the logic levels on the MODE_sel0 and MODE_sel1 pins.

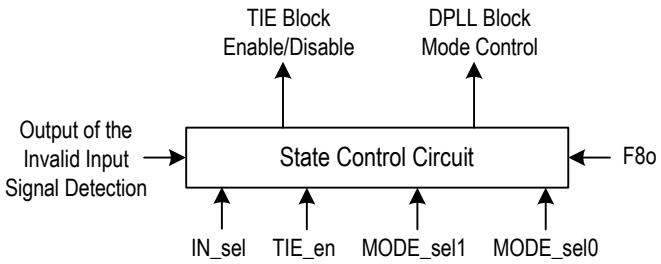
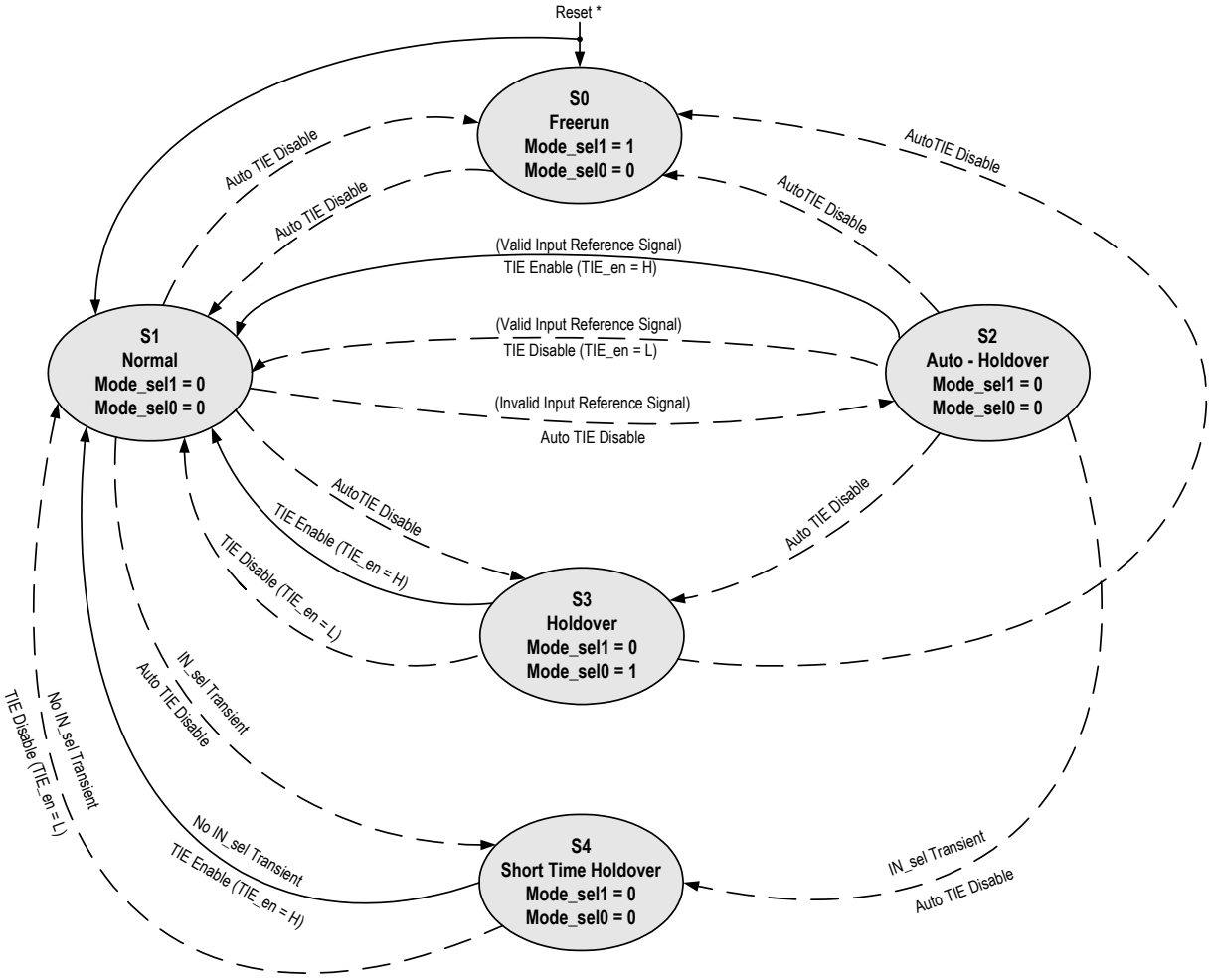


Figure - 2 State Control Circuit

Table - 1 Operating Modes Selection

Mode Selection Pins		Operating Mode
MODE_sel1	MODE_sel0	
0	0	Normal
0	1	Holdover
1	0	Freerun
1	1	Reserved



* Note: After reset, the Mode_sel1 and Mode_sel0 should be initially set to '10' or '00'.

Figure - 3 State Control Diagram

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The mode changes between Normal (S1) and Auto-Holdover (S2) are triggered by the Invalid Input Reference Detection Circuit and are irrelative to the logic levels on the MODE_sel0 and MODE_sel1 pins. At the stage of S1, if the input reference is invalid (out of the capture range), the operating mode will be changed to Auto-Holdover (S2) automatically. At the stage of S2, if no IN_sel transient occurs and the input reference becomes valid, the operating mode will be changed back to Normal (S1) automatically. If an IN_sel transient is detected at the stage of S2, the operating mode will be changed to Short Time Holdover (S4) with the TIE Control Block automatically disabled. Refer to "2.5 Invalid Input Signal Detection" for more information.

The mode changes between Normal (S1) and Short Time Holdover (S4) are triggered by the IN_sel transient. At the stage of S1, if a voltage transient occurs on the IN_sel pin, the operating mode will be changed to Short Time Holdover (S4) automatically. At the stage of S4, if no voltage transient occurs on the IN_sel pin, the operating mode will be changed back to S1 automatically. See "2.3 Reference Input Switch" for details.

When the operating mode is changed from one to another, the TIE control block is automatically disabled as shown in Figure - 3, except the changes from Short Time Holdover (S4), Holdover (S3) or Auto-Holdover (S2) to Normal (S1). In the case of changing from S4, S3 or S2 to S1, the TIE control block is enabled or disabled by the TIE_en pin.

2.1.1 NORMAL MODE

The Normal mode is typically used when a slave clock source synchronized to the network is required.

In this mode, the IDT82V3012 provides timing (C1.5o, $\overline{C3o}$, C2o, $\overline{C4o}$, C8o, $\overline{C16o}$, C19o, $\overline{C32o}$) and synchronization ($\overline{F0o}$, F8o, $\overline{F16o}$, F19o, $\overline{F32o}$, TSP, RSP) signals. All these signals are synchronous to one of the two input references. The nominal frequency of the input reference can be 8 kHz, 1.544 MHz, 2.048 MHz or 19.44 MHz.

After reset, the IDT82V3012 will take 30 seconds at most to make the output signals synchronous (phase locked) to the input reference.

Whenever the IDT82V3012 works in the Normal mode, the NORMAL pin will be set to logic high.

2.1.2 FAST LOCK MODE

The Fast Lock mode is a submode of the Normal mode. It allows the DPLL to lock to a reference more quickly than the Normal mode allows. Typically, the locking time in the Fast Lock mode is less than 500 ms.

When the FLOCK pin is set to high, the Fast Lock mode will be enabled.

2.1.3 HOLDOVER MODE

The Holdover mode is typically used for short duration (e.g., 2 seconds) while network synchronization is temporarily disrupted.

In the Holdover mode, the IDT82V3012 provides timing and synchronization signals that are not locked to an external reference signal, but are based on storage techniques. In the Normal mode, when the output frequency is locked to the input reference signal, a numerical value corresponding to the output frequency is stored alternately in two memory locations every 30 ms. When the device is changed to the Holdover mode, the stored value from between 30 ms and 60 ms is used to set the output frequency of the device.

The frequency accuracy in the Holdover mode is ±0.025 ppm, which corresponds to a worst case of 18 frame (125 µs per frame) slips in 24 hours. This meets the AT&T TR62411 and Telcordia GR-1244-CORE Stratum 3 requirement of ±0.37 ppm (255 frame slips per 24 hours).

Whenever the IDT82V3012 works in the Holdover mode, the HOLDOVER pin will be set to logic high.

2.1.4 FREERUN MODE

The Freerun mode is typically used when a master clock source is required, or used when a system is just powered up and the network synchronization has not been achieved.

In this mode, the IDT82V3012 provides timing and synchronization signals which are based on the master clock frequency (OSCi) only, and are not synchronized to the input reference signal.

The accuracy of the output clock is equal to the accuracy of the master clock (OSCi). So if a ±32 ppm output clock is required, the master clock must also be ±32 ppm. Refer to "2.8 OSC" for more information.

Whenever the IDT82V3012 works in the Freerun mode, the FREERUN pin will be set to logic high.

2.2 FREQUENCY SELECT CIRCUIT

The input reference can be 8 kHz, 1.544 MHz, 2.048 MHz or 19.44 MHz. The F0_sel1 and F0_sel0 pins select one of the four frequencies for the reference input 0 (Fref0). The F1_sel1 and F1_sel0 pins select one of the four frequencies for the reference input 1 (Fref1). See Table - 2 and Table - 3 for details.

The reference inputs Fref0 and Fref1 may have different frequencies applied to them. Every time the frequency is changed, the device must be reset to make the change effective.

Table - 2 Fref0 Frequency Selection

Frequency Selection Pins		Fref0 Input Frequency
F0_sel1	F0_sel0	
0	0	19.44 MHz
0	1	8 kHz
1	0	1.544 MHz
1	1	2.048 MHz

Table - 3 Fref1 Frequency Selection

Frequency Selection Pins		Fref1 Input Frequency
F1_sel1	F1_sel0	
0	0	19.44 MHz
0	1	8 kHz
1	0	1.544 MHz
1	1	2.048 MHz

2.3 REFERENCE INPUT SWITCH

The IDT82V3012 accepts two simultaneous reference signals Fref0 and Fref1, and operates on the falling edge (8 kHZ, 1.544 MHz and 2.048 MHz) or rising edge (19.44 MHz). One of the two reference signals will be input to the device, as determined by the IN_sel pin. See

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Table - 4. The selected reference signal is sent to the TIE control block, Reference Input Monitor and Invalid Input Signal Detection block for further processing.

Table - 4 Input Reference Selection

IN_sel	Input Reference
0	Fref0
1	Fref1

When a transient voltage occurs on the IN_sel pin, the operating mode will be changed to Short Time Holdover (S4) with the TIE Control Block automatically disabled. At the stage of S4, if no IN_sel transient occurs, the reference signal will be switched from one to the other, and the operating mode will be changed back to Normal (S1) automatically. During the change from S4 to S1, the TIE Control Block can be enabled or disabled, depending on the logic level on the TIE_en pin. See Figure - 3 for details.

2.4 REFERENCE INPUT MONITOR

The Telcordia GR-1244-CORE standard recommends that the DPLL should be able to reject the references that are off the nominal frequency by more than ±12 ppm. The IDT82V3012 monitors the Fref0 and Fref1 frequencies and outputs two signals at MON_out0 pin and MON_out1 pin to indicate the monitoring results respectively. Whenever the Fref0 frequency is off the nominal frequency by more than ±12 ppm, the MON_out0 pin will go high. The MON_out1 pin indicates the monitoring result of Fref1 in the same way. The MON_out0 and MON_out1 signals are updated every 2 seconds.

2.5 INVALID INPUT SIGNAL DETECTION

This circuit is used to detect if the selected input reference (Fref0 or Fref1) is out of the capture range. Refer to "3.6 Capture Range" for details. This includes a complete loss of the input reference and a large frequency shift in the input reference.

If the input reference is invalid (out of the capture range), the IDT82V3012 will be automatically changed to the Holdover mode (Auto-Holdover). When the input reference becomes valid, the device will be changed back to the Normal mode and the output signals will be locked to the input reference.

In the Holdover mode, the output signals are based on the output reference signal 30 ms to 60 ms prior to entering the Holdover mode. The amount of phase drift while in holdover can be negligible because the Holdover mode is very accurate (e.g., 0.025 ppm). Consequently, the phase delay between the input and output after switching back to the Normal mode is preserved.

2.6 TIE CONTROL BLOCK

If the current reference is badly damaged or lost, it is necessary to use the other reference or the one generated by storage techniques instead. But when switching the reference, a step change in phase on the input reference will occur. A step change in phase in the input to DPLL may lead to an unacceptable phase change on the output signals. The TIE control block, when enabled, prevents a step change in phase on the input reference signals from causing a step change in phase on the output of the DPLL block. Figure - 4 shows the TIE Control Block diagram.

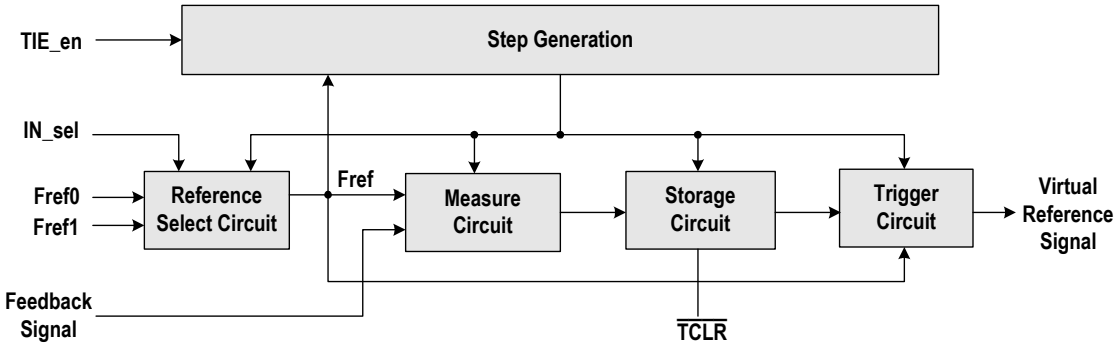


Figure - 4 TIE Control Block Diagram

When the TIE Control Block is enabled manually or automatically (by the TIE_en pin or TIE auto-enable logic generated by the State Control Circuit), it works under the control of the Step Generation circuit.

At the Measure Circuit stage, the selected reference signal (Fref0 or Fref1) is compared with the feedback signal (current output feed back from the Frequency Select Circuit). The phase difference between the input reference and the feedback signal is stored in the Storage Circuit for TIE correction. According to the value stored in the storage circuit, the Trigger Circuit generates a virtual reference with the same phase as the previous reference. In this way, the reference can be switched without generating a step change in phase.

Figure - 5 shows the phase transient that will result if a reference switch is performed with the TIE Control Block enabled.

The value of the phase difference in the Storage Circuit can be cleared by applying a logic low reset signal to the $\overline{\text{TCLR}}$ pin. The minimum width of the reset pulse should be 300 ns.

When the IDT82V3012 primarily enters the Holdover mode for a short time period and then returns back to the Normal mode, the TIE Control Circuit should not be enabled. This will prevent undesired accumulated phase change between the input and output.

If the TIE Control Block is disabled manually or automatically, a reference switch will result in a phase alignment between the input signal and the output signal as shown in Figure - 6. The slope of the phase adjustment is limited to 5 ns per 125 µs.

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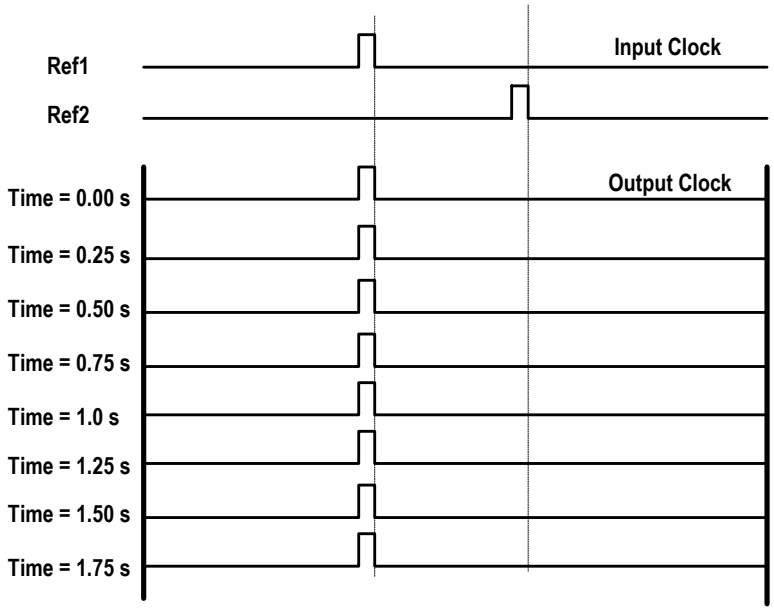


Figure - 5 Reference Switch with TIE Control Block Enabled

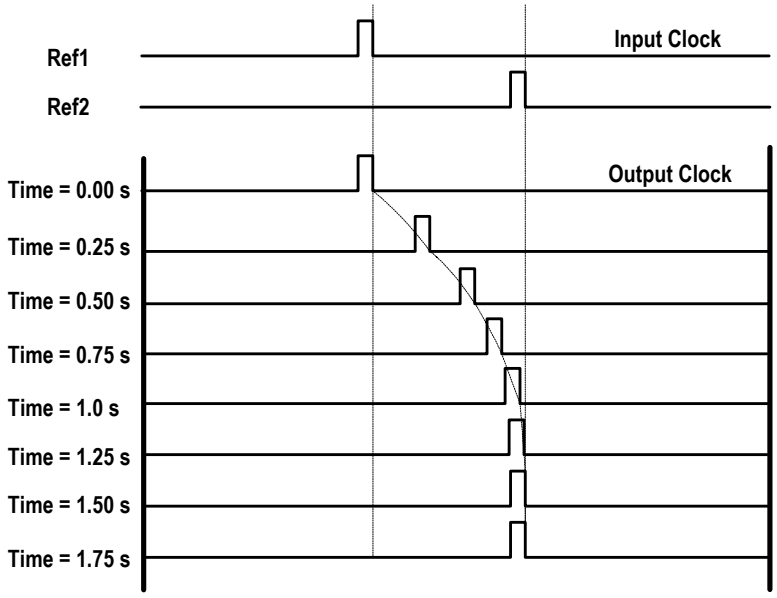


Figure - 6 Reference Switch with TIE Control Block Disabled

2.7 DPLL BLOCK

As shown in Figure - 7, the DPLL Block consists of a Phase Detector, a Limiter, a Loop Filter, a Digital Control Oscillator and Divider.

2.7.1 PHASE DETECTOR (PHD)

In the Normal mode, the Phase Detector compares the virtual reference signal from the TIE Control Circuit with the feedback signal from the Frequency Select Circuit, and outputs an error signal corresponding to the phase difference. This error signal is sent to the Limiter circuit for phase slope control.

In the Freerun or Holdover mode, the Frequency Select Circuit, the Phase Detector and the Limiter are inactive, and the input reference signal is not used.

2.7.2 LIMITER

The Limiter is used to limit the phase slope. It ensures that the maximum output phase slope is limited to 5 ns per 125 µs for all input transient conditions. This well meets the AT&T TR62411 and Telcordia GR-1244-CORE specifications, which specify the maximum phase slope of 7.6 ns per 125 µs and 81 ns per 1.326 ms respectively.

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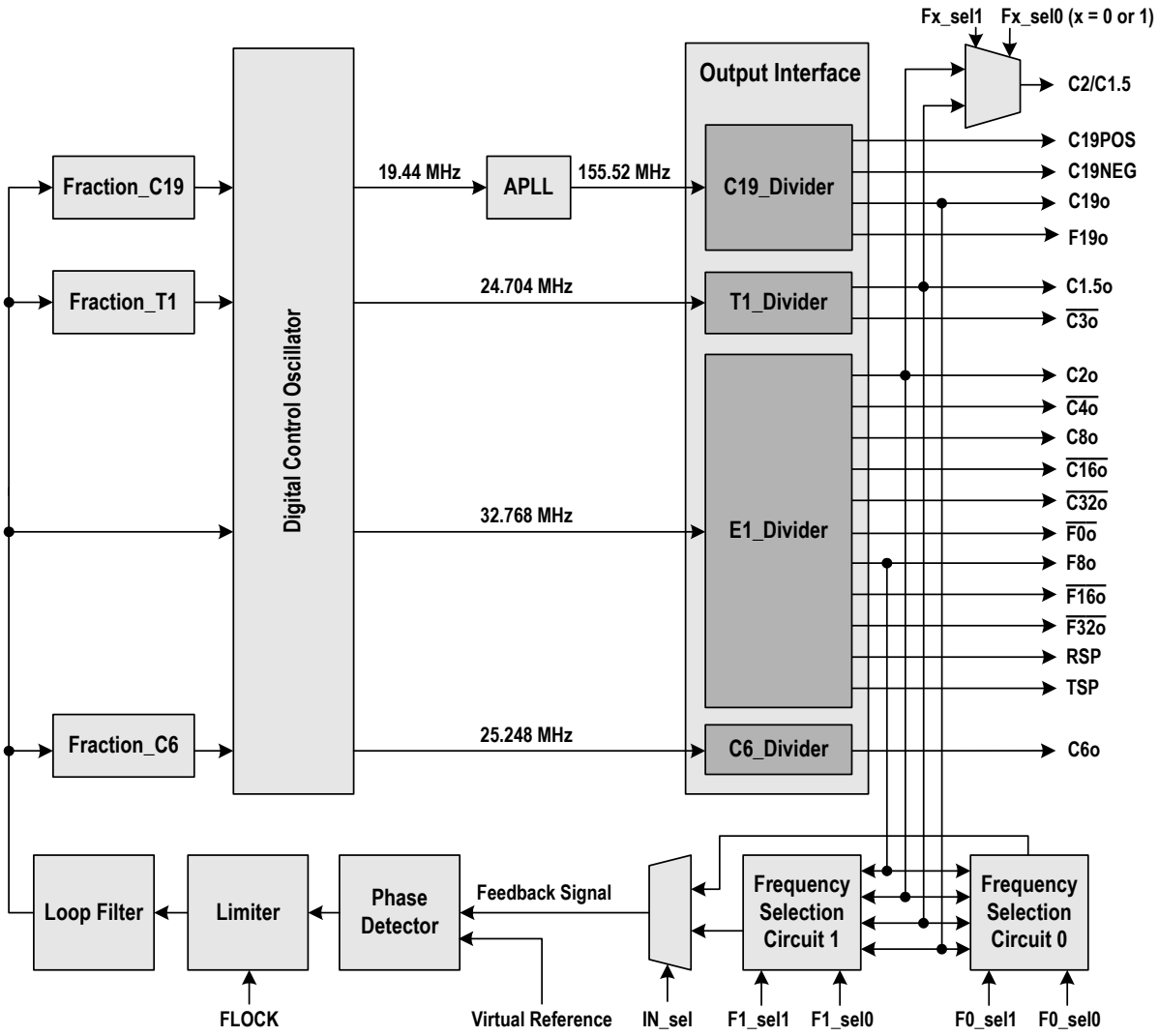


Figure - 7 DPLL Block Diagram

In the Normal mode, the Limiter receives the error signal from the Phase Detector, limits the phase slope within 5 ns per 125 µs and sends the limited signal to the Loop Filter.

In the Fast Lock mode, the Limiter is disabled, and the DPLL locks to the input reference within 500 ms, which is much shorter than that in the Normal mode.

2.7.3 LOOP FILTER

The Loop Filter ensures that the jitter transfer meets the ETS 300 011 and AT&T TR62411 requirements. It works similarly to a first order low pass filter with 2.1 Hz cutoff frequency for the four valid input frequencies (8 kHz, 1.544 MHz, 2.048 MHz or 19.44 MHz).

The output of the Loop Filter goes to the Digital Control Oscillator directly or through the Fraction blocks, in which E1, T1, C6 and C19 signals are generated.

2.7.4 FRACTION BLOCK

By applying some algorithms to the incoming E1 signal, the Fraction_C19, Fraction_C6 and Fraction_T1 blocks generate C19, C6 and T1 signals respectively.

2.7.5 DIGITAL CONTROL OSCILLATOR (DCO)

In the Normal mode, the DCO receives four limited and filtered signals from Loop Filter or Fraction blocks. Based on the values of the received signals, the DCO generates four digital outputs: 19.44 MHz, 25.248 MHz, 32.768 MHz and 24.704 MHz for C19, C6, E1 and T1 dividers respectively.

In the Holdover mode, the DCO is running at the same frequency as that generated by storage techniques.

In the Freerun mode, the DCO is running at the same frequency as that of the master clock.

2.7.6 LOCK INDICATOR

If the output frequency of the DPLL is identical to the input frequency, and the input phase offset is small enough so that no slope limiting is exhibited, the LOCK pin will be set high.

2.7.7 OUTPUT INTERFACE

The Output Interface uses three output signals from the DCO to generate totally 9 types of clock signals and 7 types of framing signals All these output signals are synchronous to F8o.

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The 32.768 MHz signal is used by the E1_divider to generate five types of clock signals (C2o, C4o, C8o, C16o and C32o) with nominal 50% duty cycle and six types of framing signals (F0o, F8o, F16o, F32o, RSP and TSP).

The 24.704 MHz signal is used by the T1_divider to generate two types of T1 signals (C1.5o and C3o) with nominal 50% duty cycle.

The 25.248 MHz signal is used by the C6_divider to generate a C6o signal with nominal 50% duty cycle.

The 19.44 MHz signal is sent to an APLL, which outputs a 155.52 MHz signal. The 155.52 MHz signal is used by the C19_divider to generate 19.44 MHz clock signals (C19o, C19POS and C19NEG) with nominal 50% duty cycle and a framing signal F19o.

Additionally, the IDT82V3012 provides an output clock (C2/C1.5) with the frequency controlled by the frequency selection pins Fx_sel0 and Fx_sel1 (see Table - 5 for details). If the selected reference input (Fref0 or Fref1) is 8 kHz, 2.048 MHz or 19.44 MHz, the C2/C1.5 pin will output a 2.048 MHz clock signal. If the selected reference input (Fref0 or Fref1) is 1.544 MHz, the C2/C1.5 pin will output a 1.544 MHz clock signal. The electrical and timing characteristics of this output (2.048 MHz or 1.544 MHz) is the same as that of C2o or C1.5o.

Table - 5 C2/C1.5 Output Frequency Control

Frequency Selection Pins		Frefx Input Frequency	C2/C1.5 Output Frequency
Fx_sel1	Fx_sel0		
0	0	19.44 MHz	2.048 MHz
0	1	8 kHz	2.048 MHz
1	0	1.544 MHz	1.544 MHz
1	1	2.048 MHz	2.048 MHz

Note: 'x' can be 0 or 1, as selected by IN_sel pin.
IN_sel = 0: x = 0, Fref0 is the selected reference input. The frequency of Fref0 is determined by F0_sel0 and F0_sel1 pins.
IN_sel = 1: x = 1, Fref1 is the selected reference input. The frequency of Fref1 is determined by F1_sel0 and F1_sel1 pins.

2.8 OSC

The IDT82V3012 can use a clock as the master timing source. In the Freerun mode, the frequency tolerance of the clock outputs is identical to that of the source at the OSCi pin. For applications not requiring an accurate Freerun mode, the tolerance of the master timing source may be ±100 ppm. For applications requiring an accurate Freerun mode, such as AT&T TR62411, the tolerance of the master timing source must be no greater than ±32 ppm.

The desired capture range should be taken into consideration when determining the accuracy of the master timing source. The sum of the accuracy of the master timing source and the capture range of the IDT82V3012 will always equal 230 ppm. For example, if the master timing source is 100 ppm, the capture range will be 130 ppm.

2.8.1 CLOCK OSCILLATOR

When selecting a Clock Oscillator, numerous parameters must be considered. This includes absolute frequency, frequency change over temperature, output rise and fall times, output levels and duty cycle.

For applications requiring ±32 ppm clock accuracy, the following clock oscillator module may be used.

FOX F7C-2E3-20.0 MHz
Frequency: 20.0 MHz
Tolerance: 25 ppm 0°C to 70°C
Rise & Fall Time: 10 ns (0.33 V, 2.97 V, 15 pF)
Duty Cycle: 40% to 60%

For Stratum 3 application, the clock oscillator should meet the following requirements:

Frequency: 20.0 MHz
Tolerance: ±4.6 ppm over 20 years life time
Drift: ±0.04 ppm per day @ constant temperature
±0.3 ppm over temperature range of 0 to 70°C

The output clock should be connected directly (not AC coupled) to the OSCi input of the IDT82V3012, as shown in Figure - 8.

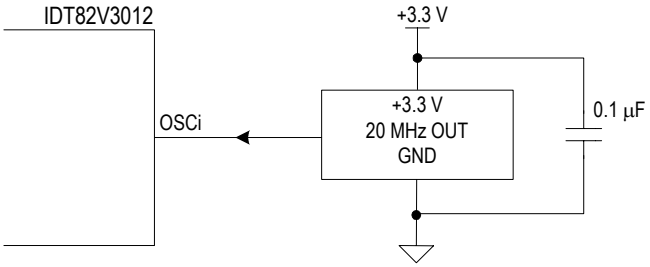


Figure - 8 Clock Oscillator Circuit

2.9 JTAG

The IDT82V3012 supports IEEE 1149.1 JTAG Scan.

2.10 RESET, LOCK AND TIE APPLICATION

A simple power-up reset circuit is shown as Figure - 9. The logic low reset pulse is about 50 µs.

The resistor Rp is used for protection only and limits current into the RST pin during power down. The logic low reset pulse width is not critical but should be greater than 300 ns.

When the DPLL operates in Normal mode after power-up or reset, the lock pin may indicate frequency lock before the output phase is synchronized with the input. The phase lock requires 30 seconds (at most) after frequency lock.

If users want to switch the input reference, it is highly recommended to do the switch after phase lock, with TIE control block enabled.

After TIE control block is cleared, the DPLL requires some time for the phase relationship to stabilize. In general, the phase lock requires 30 seconds (at most) after frequency lock.

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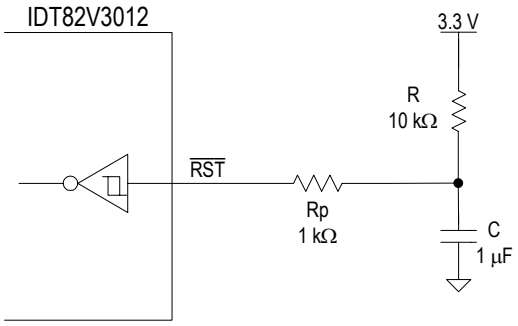


Figure - 9 Power-Up Reset Circuit

2.11 POWER SUPPLY FILTERING TECHNIQUES

To achieve optimum jitter performance, power supply filtering is required to minimize supply noise modulation of the output clocks. The common sources of power supply noise are switching power supplies and the high switching noise from the outputs to the internal PLL. The 82V3012 provides separate power pins: V_{DDA} and V_{DDD}. V_{DDA} pins are for the internal analog PLL, and V_{DDD} pins are for the core logic as well as I/O driver circuits.

To minimize switching power supply noise generated by the switching regulator, the power supply output should be filtered with sufficient bulk capacity to minimize ripple and 0.1 uF (0402 case size, ceramic) capacitors to filter out the switching transients.

For the 82V3012, the decoupling for V_{DDA} and V_{DDD} are handled individually. V_{DDD} and V_{DDA} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. Figure - 10 illustrates how bypass capacitor and ferrite bead should be connected to each power pin.

The analog power supply V_{DDA} should have low impedance. This can be achieved by using one 10 uF (1210 case size, ceramic) and at least two 0.1 uF (0402 case size, ceramic) capacitors in parallel. The 0.1 uF (0402 case size, ceramic) capacitors must be placed next to the V_{DDA} pins and as close as possible. Note that the 10 uF capacitor must be of 1210 case size, and it must be ceramic for lowest possible ESR (Effective Series Resistance). The 0.1 uF should be of case size 0402, which offers the lowest ESL (Effective Series Inductance) to achieve low impedance towards the high speed range.

For V_{DDD}, at least three 0.1 uF (0402 case size, ceramic) and one 10 uF (1210 case size, ceramic) capacitors are recommended. The 0.1 uF capacitors should be placed as close to the V_{DDD} pins as possible.

Please refer to evaluation board schematic for details.

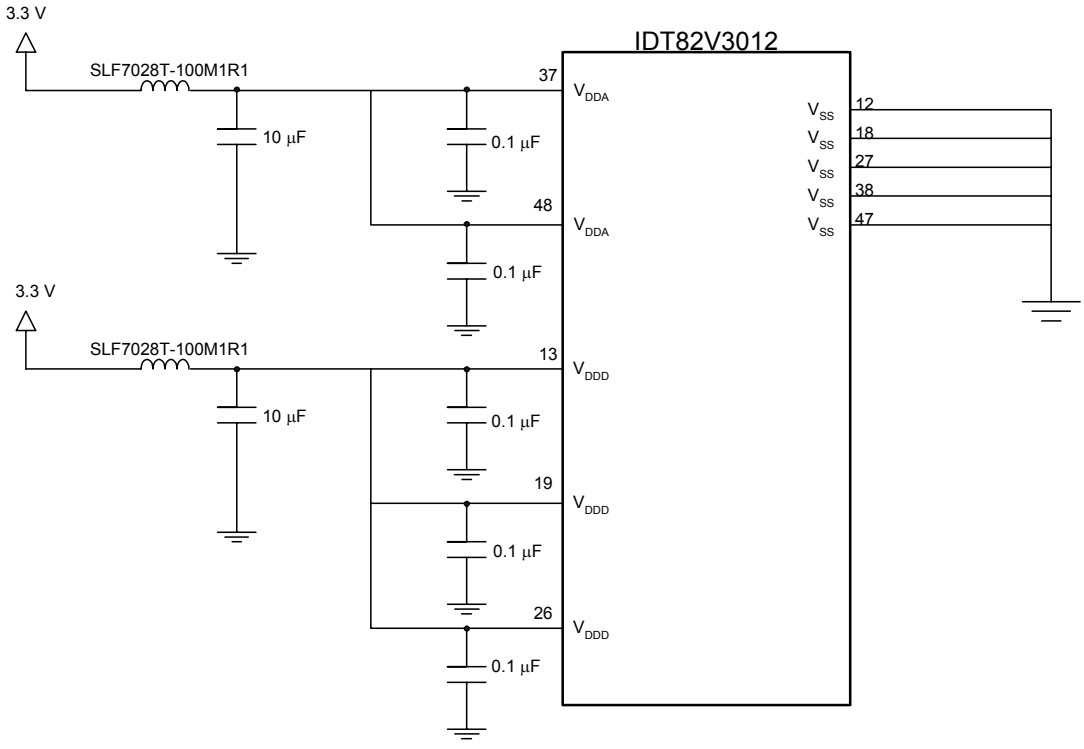


Figure - 10 IDT82V3012 Power Decoupling Scheme

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3 MEASURES OF PERFORMANCE

The following are some synchronizer performance indicators and their corresponding definitions.

3.1 INTRINSIC JITTER

Intrinsic jitter is the jitter produced by the synchronizing circuit and is measured at its output. It is measured by applying a reference signal with no jitter to the input of the device, and measuring its output jitter. Intrinsic jitter may also be measured when the device is in a non-synchronizing mode, such as free running or holdover, by measuring the output jitter of the device. Intrinsic jitter is usually measured with various band limiting filters depending on the applicable standards. For the IDT82V3012, the intrinsic Jitter is limited to less than 0.02 UI on the 2.048 MHz and 1.544 MHz clocks.

3.2 JITTER TOLERANCE

Jitter tolerance is a measure of the ability of a DPLL to operate properly (i.e., remain in lock and or regain lock in the presence of large jitter magnitudes at various jitter frequencies) when jitter is applied to its reference. The applied jitter magnitude and jitter frequency depends on the applicable standards.

3.3 JITTER TRANSFER

Jitter transfer or jitter attenuation refers to the magnitude of jitter at the output of a device for a given amount of jitter at the input of the device. Input jitter is applied at various amplitudes and frequencies, and output jitter is measured with various filters depending on the applicable standards.

For the IDT82V3012, two internal elements determine the jitter attenuation. This includes the internal 2.1 Hz low pass loop filter and the phase slope limiter. The phase slope limiter limits the output phase slope to 5 ns per 125 µs. Therefore, if the input signal exceeds this rate, such as for very large amplitude, low frequency input jitter, the maximum output phase slope will be limited (i.e., attenuated) to 5 ns per 125 µs.

The IDT82V3012 has 16 outputs with 4 possible input frequencies for a total of 64 possible jitter transfer functions. Since all outputs are derived from the same signal, the jitter transfer values for the four cases, 8 kHz to 8 kHz, 1.544 MHz to 1.544 MHz, 2.048 MHz to 2.048 MHz and 19.44 MHz to 19.44 MHz can be applied to all outputs.

It should be noted that 1 UI at 1.544 MHz is 644 ns, which is not equal to 1 UI at 2.048 MHz, which is 488 ns. Consequently, a transfer value using different input and output frequencies must be calculated in common units (e.g., seconds).

Using the above method, the jitter attenuation can be calculated for all combinations of inputs and outputs based on the four jitter transfer functions provided. Note that the resulting jitter transfer functions for all combinations of inputs (8 kHz, 1.544 MHz, 2.048 MHz, 19.44 MHz) and outputs (8 kHz, 1.544 MHz, 3.088 MHz, 6.312 MHz, 2.048 MHz, 4.096 MHz, 8.192 MHz, 16.384 MHz, 19.44 MHz, 32.768 MHz) for a given input signal (jitter frequency and jitter amplitude) are the same.

Since intrinsic jitter is always present, jitter attenuation will appear to be lower for small input jitter signals than for large ones. Consequently, accurate jitter transfer function measurements are usually made with large input jitter signals (e.g., 75% of the specified maximum jitter tolerance).

3.4 FREQUENCY ACCURACY

Frequency accuracy is defined as the absolute tolerance of an output clock signal when it is not locked to an external reference, but is operating in a free running mode. For the IDT82V3012, the Freerun accuracy is equal to the Master Clock (OSCi) accuracy.

3.5 HOLDOVER ACCURACY

Holdover accuracy is defined as the absolute tolerance of an output clock signal, when it is not locked to an external reference signal, but is operating using storage techniques. For the IDT82V3012, the storage value is determined while the device is in Normal mode and locked to an external reference signal.

The absolute Master Clock (OSCi) accuracy of the IDT82V3012 does not affect Holdover accuracy, but the change in OSCi accuracy while in Holdover mode does.

3.6 CAPTURE RANGE

Also referred to as pull-in range. This is the input frequency range over which the synchronizer must be able to pull into synchronization. The IDT82V3012 capture range is equal to ±230 ppm minus the accuracy of the master clock (OSCi). For example, a 32 ppm master clock results in a capture range of 198 ppm.

The Telcordia GR-1244-CORE standard, recommends that the DPLL should be able to reject references that are off the nominal frequency by more than ±12 ppm. The IDT82V3012 provides two pins, MON_out0 and MON_out1, to respectively indicate whether the reference inputs Fref0 and Fref1 are within ±12 ppm of the nominal frequency.

3.7 LOCK RANGE

This is the input frequency range over which the synchronizer must be able to maintain synchronization. The lock range is equal to the capture range for the IDT82V3012.

3.8 PHASE SLOPE

Phase slope is measured in seconds per second and is the rate at which a given signal changes phase with respect to an ideal signal. The given signal is typically the output signal. The ideal signal is of constant frequency and is nominally equal to the value of the final output signal or final input signal.

3.9 TIME INTERVAL ERROR (TIE)

TIE is the time delay between a given timing signal and an ideal timing signal.

3.10 MAXIMUM TIME INTERVAL ERROR (MTIE)

MTIE is the maximum peak to peak delay between a given timing signal and an ideal timing signal within a particular observation period.

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3.11 PHASE CONTINUITY

Phase continuity is the phase difference between a given timing signal and an ideal timing signal at the end of a particular observation period. Usually, the given timing signal and the ideal timing signal are of the same frequency. Phase continuity applies to the output of the synchronizer after a signal disturbance due to a mode change. The observation period is usually the time from the disturbance, to just after the synchronizer has settled to a steady state.

In the case of the IDT82V3012, the output signal phase continuity is maintained to within ±5 ns at the instance (over one frame) of all mode changes. The total phase shift, depending on the type of mode change, may accumulate up to 200 ns over many frames. The rate of change of the 200 ns phase shift is limited to a maximum phase slope of approximately 5 ns per 125 µs. This meets the AT&T TR62411 maximum phase slope requirement of 7.6 ns per 125 µs and Telcordia GR-1244-CORE (81 ns per 1.326 ms).

3.12 PHASE LOCK TIME

This is the time it takes the synchronizer to phase lock to the input signal. Phase lock occurs when the input signal and output signal are not changing in phase with respect to each other (not including jitter).

Lock time is very difficult to determine because it is affected by many factors including:

1. Initial input to output phase difference
2. Initial input to output frequency difference
3. Synchronizer loop filter
4. Synchronizer limiter

Although a short lock time is desirable, it is not always possible to achieve due to other synchronizer requirements. For instance, better jitter transfer performance is achieved with a lower frequency loop filter which increases lock time. And better (smaller) phase slope performance (limiter) results in longer lock times. The IDT82V3012 loop filter and limiter are optimized to meet the AT&T TR62411 jitter transfer and phase slope requirements. Consequently, phase lock time, which is not a standard requirement, may be longer than in other applications. See “7.1 Performance”for details.

The IDT82V3012 provides a FLOCK pin to enable the Fast Lock mode. When this pin is set to high, the DPLL will lock to an input reference within approximately 500 ms.

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4 ABSOLUTE MAXIMUM RATINGS

Ratings	Min.	Max.	Unit
Power supply voltage	-0.5	5.0	V
Voltage on any pin with respect to ground	-0.5	5.5	V
Package power dissipation		200	mW
Storage temperature	-55	125	°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

5 RECOMMENDED DC OPERATING CONDITIONS

Parameter	Min.	Max.	Unit
Operating temperature	-40	+85	°C
Power supply voltage	3.0	3.6	V

6 DC ELECTRICAL CHARACTERISTICS

6.1 SINGLE END INPUT/OUTPUT PORT

Parameter	Description	Min.	Typ.	Max.	Units	Test Conditions *
I_{DDS}	Supply current with OSCi = 0 V			10	mA	Outputs unloaded
I_{DD}	Supply current with OSCi = Clock			60	mA	Outputs unloaded
V_{CIH}	CMOS high-level input voltage	$0.7V_{DDD}$			V	OSCi, Fref0 and Fref1
V_{CIL}	CMOS low-level input voltage			$0.3V_{DDD}$	V	OSCi, Fref0 and Fref1
V_{TIH}	TTL high-level input voltage	2.0			V	All input pins except for OSCi, Fref0 and Fref1
V_{TIL}	TTL low-level input voltage			0.8	V	All input pins except for OSCi, Fref0 and Fref1
I_{IL}	Input leakage current: Normal (low level) Normal (high level) Pull up (low level) Pull up (high level) Pull down (low level) Pull down (high level)	 -15 -15 -100 -15 -15 0		 15 15 0 15 15 100	µA	$V_I = V_{DDD}$ or 0 V
V_{OH}	High-level output voltage	2.4			V	I_{OH} = 8 mA
V_{OL}	Low-level output voltage			0.4	V	I_{OL} = 8 mA

*** Note:**

1. Voltages are with respect to ground (V_{SS}) unless otherwise stated.
2. Supply voltage and operating temperature are as per Recommended Operating Conditions.

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6.2 DIFFERENTIAL OUTPUT PORT (LVDS)

Parameter	Description	Min.	Typ.	Max.	Units	Test Conditions
VOD	Differential Output Voltage	250	350	450	mV	RL = 100 Ω
∆VOD	Change in Magnitude of VOD for Complementary Output States		4	35	mV	RL = 100 Ω
VOS	Offset Voltage	1.125	1.25	1.375	V	RL = 100 Ω
∆VOS	Change in Magnitude of VOS for Complementary Output States		5	25	mV	RL = 100 Ω
VOH	Output Voltage High		1.38	1.6	V	RL = 100 Ω
VOL	Output Voltage Low	0.9	1.03		V	RL = 100 Ω
t_{TLH}	Output Rise time		0.38	1.5	ns	RL = 100 Ω
t_{THL}	Output Fall time		0.40	1.5	ns	RL = 100 Ω
IOS	Output Short Circuit Current		6.0		mA	
IOSD	Differential Output Short Circuit Current		6.0	10	mA	

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7 AC ELECTRICAL CHARACTERISTICS

7.1 PERFORMANCE

Description	Min.	Typ.	Max.	Units	Test Conditions / Notes (see "Notes" on page 26)
Freerun Mode accuracy with OSCi at: 0 ppm	-0		+0	ppm	5-9
Freerun Mode accuracy with OSCi at: ±32 ppm	-32		+32	ppm	5-9
Freerun Mode accuracy with OSCi at: ±100 ppm	-100		+100	ppm	5-9
Holdover Mode accuracy with OSCi at: 0 ppm	-0.025		+0.025	ppm	1, 2, 4, 6-9, 43, 44
Holdover Mode accuracy with OSCi at: ±32 ppm	-0.025		+0.025	ppm	1, 2, 4, 6-9, 43, 44
Holdover Mode accuracy with OSCi at: ±100 ppm	-0.025		+0.025	ppm	1, 2, 4, 6-9, 43, 44
Capture range with OSCi at: 0 ppm	-230		+230	ppm	1-3, 6-9
Capture range with OSCi at: ±32 ppm	-198		+198	ppm	1-3, 6-9
Capture range with OSCi at: ±100 ppm	-130		+130	ppm	1-3, 6-9
Phase lock time		50		s	1-3, 6-15, 45
Output phase continuity with reference switch			200	ns	1-3, 6-15
Output phase continuity with mode switch to Normal			200	ns	1-2, 4-15
Output phase continuity with mode switch to Freerun			200	ns	1-4, 6-15
Output phase continuity with mode switch to Holdover			50	ns	1-3, 6-15
Fref0 Frequency accuracy when MON_out0 is logic low	-12		+12	ppm	
Fref1 Frequency accuracy when MON_out1 is logic low	-12		+12	ppm	
MTIE (maximum time interval error)			600	ns	1-15, 28
Output phase slope			40	µs/s	1-15, 28
Reference input for Auto-Holdover with 8 kHz	-18 k		+18 k	ppm	1-3, 6, 10-12
Reference input for Auto-Holdover with 1.544 MHz	-36 k		+36 k	ppm	1-3, 7, 10-12
Reference input for Auto-Holdover with 2.048 MHz	-36 k		+36 k	ppm	1-3, 8, 10-12
Reference input for Auto-Holdover with 19.44 MHz	-36 k		+36 k	ppm	1-3, 9, 10-12

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7.2 INTRINSIC JITTER UNFILTERED

Description	Min.	Typ.	Max.	Units	Test Conditions / Notes (see "Notes" on page 26)
Intrinsic jitter at F8o (8 kHz)			0.0001	UIpp	1-15, 22-25, 29
Intrinsic jitter at $\overline{\text{F0o}}$ (8 kHz)			0.0001	UIpp	1-15, 22-25, 29
Intrinsic jitter at $\overline{\text{F16o}}$ (8 kHz)			0.0001	UIpp	1-15, 22-25, 29
Intrinsic jitter at C1.5o (1.544 MHz)			0.015	UIpp	1-15, 22-25, 30
Intrinsic jitter at $\overline{\text{C3o}}$ (3.088 MHz)			0.03	UIpp	1-15, 22-25, 32
Intrinsic jitter at C2o (2.048 MHz)			0.01	UIpp	1-15, 22-25, 31
Intrinsic jitter at C6o (6.312 MHz)			0.06	UIpp	1-15, 22-25, 34
Intrinsic jitter at $\overline{\text{C4o}}$ (4.096 MHz)			0.02	UIpp	1-15, 22-25, 33
Intrinsic jitter at C8o (8.192 MHz)			0.04	UIpp	1-15, 22-25, 35
Intrinsic jitter at $\overline{\text{C16o}}$ (16.834 MHz)			0.04	UIpp	1-15, 22-25, 36
Intrinsic jitter at TSP (8 kHz)			0.0001	UIpp	1-15, 22-25, 29
Intrinsic jitter at RSP (8 kHz)			0.0001	UIpp	1-15, 22-25, 29
Intrinsic jitter at $\overline{\text{C32o}}$ (32.768 MHz)			0.08	UIpp	1-15, 22-25, 38

7.3 C1.5o (1.544 MHZ) INTRINSIC JITTER FILTERED

Description	Min.	Typ.	Max.	Units	Test Conditions / Notes (see "Notes" on page 26)
Intrinsic jitter (4 Hz to 100 kHz filter)			0.008	UIpp	1-15, 22-25, 30
Intrinsic jitter (10 Hz to 40 kHz filter)			0.006	UIpp	1-15, 22-25, 30
Intrinsic jitter (8 kHz to 40 kHz filter)			0.006	UIpp	1-15, 22-25, 30
Intrinsic jitter (10 Hz to 8 kHz filter)			0.003	UIpp	1-15, 22-25, 30

7.4 C2o (2.048 MHZ) INTRINSIC JITTER FILTERED

Description	Min.	Typ.	Max.	Units	Test Conditions / Notes (see "Notes" on page 26)
Intrinsic jitter (4 Hz to 100 kHz filter)			0.005	UIpp	1-15, 22-25, 31
Intrinsic jitter (10 Hz to 40 kHz filter)			0.004	UIpp	1-15, 22-25, 31
Intrinsic jitter (8 kHz to 40 kHz filter)			0.003	UIpp	1-15, 22-25, 31
Intrinsic jitter (10 Hz to 8 kHz filter)			0.002	UIpp	1-15, 22-25, 31

7.5 C19o (19.44 MHZ) INTRINSIC JITTER FILTERED

Description	Min.	Typ.	Max.	Units	Test Conditions / Notes (see "Notes" on page 26)
Intrinsic jitter (500 Hz to 1.3 MHz filter)		0.4	0.5	nspp	1-15, 22-25, 37
Intrinsic jitter (65 kHz to 1.3 MHz filter)		0.2	0.3	nspp	1-15, 22-25, 37

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7.6 8 KHZ INPUT TO 8 KHZ OUTPUT JITTER TRANSFER

Description	Min.	Typ.	Max.	Units	Test Conditions / Notes (see "Notes" on page 26)
Jitter attenuation for 1 Hz@0.01 UIpp input	0		6	dB	1-3, 6, 10-15, 22-23, 25, 29, 39
Jitter attenuation for 1 Hz@0.54 UIpp input	6		16	dB	1-3, 6, 10-15, 22-23, 25, 29, 39
Jitter attenuation for 10 Hz@0.10 UIpp input	15		22	dB	1-3, 6, 10-15, 22-23, 25, 29, 39
Jitter attenuation for 60 Hz@0.10 UIpp input	32		38	dB	1-3, 6, 10-15, 22-23, 25, 29, 39
Jitter attenuation for 300 Hz@0.10 UIpp input	42			dB	1-3, 6, 10-15, 22-23, 25, 29, 39
Jitter attenuation for 3600 Hz@0.005 UIpp input	50			dB	1-3, 6, 10-15, 22-23, 25, 29, 39

7.7 1.544 MHZ INPUT TO 1.544 MHZ OUTPUT JITTER TRANSFER

Description	Min.	Typ.	Max.	Units	Test Conditions / Notes (see "Notes" on page 26)
Jitter attenuation for 1 Hz@20 UIpp input	0		6	dB	1-3, 7, 10-15, 22-23, 25, 30, 39
Jitter attenuation for 1 Hz@104 UIpp input	6		16	dB	1-3, 7, 10-15, 22-23, 25, 30, 39
Jitter attenuation for 10 Hz@20 UIpp input	17		22	dB	1-3, 7, 10-15, 22-23, 25, 30, 39
Jitter attenuation for 60 Hz@20 UIpp input	33		38	dB	1-3, 7, 10-15, 22-23, 25, 30, 39
Jitter attenuation for 300 Hz@20 UIpp input	45			dB	1-3, 7, 10-15, 22-23, 25, 30, 39
Jitter attenuation for 10 kHz@0.3 UIpp input	48			dB	1-3, 7, 10-15, 22-23, 25, 30, 39
Jitter attenuation for 40 kHz@0.3 UIpp input	50			dB	1-3, 7, 10-15, 22-23, 25, 30, 39

7.8 2.048 MHZ INPUT TO 2.048 MHZ OUTPUT JITTER TRANSFER

Description	Min.	Typ.	Max.	Units	Test Conditions / Notes (see "Notes" on page 26)
Jitter at output for 1 Hz@3.00 UIpp input			2.5	UIpp	1-3, 8, 10-15, 22-23, 25, 31, 39
Jitter at output for 1 Hz@3.00 UIpp input with 40 Hz to 100 kHz filter			0.07	UIpp	1-3, 8, 10-15, 22-23, 25, 31, 40
Jitter at output for 3 Hz@2.33 UIpp input			1.4	UIpp	1-3, 8, 10-15, 22-23, 25, 31, 39
Jitter at output for 3 Hz@2.33 UIpp input with 40 Hz to 100 kHz filter			0.10	UIpp	1-3, 8, 10-15, 22-23, 25, 31, 40
Jitter at output for 5 Hz@2.07 UIpp input			0.90	UIpp	1-3, 8, 10-15, 22-23, 25, 31, 39
Jitter at output for 5 Hz@2.07 UIpp input with 40 Hz to 100 kHz filter			0.10	UIpp	1-3, 8, 10-15, 22-23, 25, 31, 40
Jitter at output for 10 Hz@1.76 UIpp input			0.40	UIpp	1-3, 8, 10-15, 22-23, 25, 31, 39
Jitter at output for 10 Hz@1.76 UIpp input with 40 Hz to 100 kHz filter			0.10	UIpp	1-3, 8, 10-15, 22-23, 25, 31, 40
Jitter at output for 100 Hz@1.50 UIpp input			0.06	UIpp	1-3, 8, 10-15, 22-23, 25, 31, 39
Jitter at output for 100 Hz@1.50 UIpp input with 40 Hz to 100 kHz filter			0.05	UIpp	1-3, 8, 10-15, 22-23, 25, 31, 40
Jitter at output for 2400 Hz@1.50 UIpp input			0.04	UIpp	1-3, 8, 10-15, 22-23, 25, 31, 39
Jitter at output for 2400 Hz@1.50 UIpp input with 40 Hz to 100 kHz filter			0.03	UIpp	1-3, 8, 10-15, 22-23, 25, 31, 40
Jitter at output for 100 kHz@0.20 UIpp input			0.04	UIpp	1-3, 8, 10-15, 22-23, 25, 31, 39
Jitter at output for 100 kHz@0.20 UIpp input with 40 Hz to 100 kHz filter			0.02	UIpp	1-3, 8, 10-15, 22-23, 25, 31, 40

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7.9 19.44 MHZ INPUT TO 19.44 MHZ OUTPUT JITTER TRANSFER

Description	Min.	Typ.	Max.	Units	Test Conditions / Notes (see "Notes" on page 26)
Jitter attenuation for 1 Hz@20 Ulpp input	0		6	dB	1-3, 9-15, 22-23, 25, 37, 39
Jitter attenuation for 1 Hz@104 Ulpp input	6		16	dB	1-3, 9-15, 22-23, 25, 37, 39
Jitter attenuation for 10 Hz@20 Ulpp input	17		22	dB	1-3, 9-15, 22-23, 25, 37, 39
Jitter attenuation for 60 Hz@20 Ulpp input	33		38	dB	1-3, 9-15, 22-23, 25, 37, 39
Jitter attenuation for 300 Hz@20 Ulpp input	45			dB	1-3, 9-15, 22-23, 25, 37, 39
Jitter attenuation for 10 kHz@0.3 Ulpp input	48			dB	1-3, 9-15, 22-23, 25, 37, 39
Jitter attenuation for 40 kHz@0.3 Ulpp input	50			dB	1-3, 9-15, 22-23, 25, 37, 39

7.10 8 KHZ INPUT JITTER TOLERANCE

Description	Min.	Typ.	Max.	Units	Test Conditions / Notes (see "Notes" on page 26)
Jitter tolerance for 1 Hz input	0.80			Ulpp	1-3, 6, 10-15, 22-23, 25-27, 29
Jitter tolerance for 5 Hz input	0.70			Ulpp	1-3, 6, 10-15, 22-23, 25-27, 29
Jitter tolerance for 20 Hz input	0.60			Ulpp	1-3, 6, 10-15, 22-23, 25-27, 29
Jitter tolerance for 300 Hz input	0.16			Ulpp	1-3, 6, 10-15, 22-23, 25-27, 29
Jitter tolerance for 400 Hz input	0.14			Ulpp	1-3, 6, 10-15, 22-23, 25-27, 29
Jitter tolerance for 700 Hz input	0.07			Ulpp	1-3, 6, 10-15, 22-23, 25-27, 29
Jitter tolerance for 2400 Hz input	0.02			Ulpp	1-3, 6, 10-15, 22-23, 25-27, 29
Jitter tolerance for 3600 Hz input	0.01			Ulpp	1-3, 6, 10-15, 22-23, 25-27, 29

7.11 1.544 MHZ INPUT JITTER TOLERANCE

Description	Min.	Typ.	Max.	Units	Test Conditions / Notes (see "Notes" on page 26)
Jitter tolerance for 1 Hz input	150			Ulpp	1-3, 7, 10-15, 22-23, 25-27, 30
Jitter tolerance for 5 Hz input	140			Ulpp	1-3, 7, 10-15, 22-23, 25-27, 30
Jitter tolerance for 20 Hz input	130			Ulpp	1-3, 7, 10-15, 22-23, 25-27, 30
Jitter tolerance for 300 Hz input	38			Ulpp	1-3, 7, 10-15, 22-23, 25-27, 30
Jitter tolerance for 400 Hz input	25			Ulpp	1-3, 7, 10-15, 22-23, 25-27, 30
Jitter tolerance for 700 Hz input	15			Ulpp	1-3, 7, 10-15, 22-23, 25-27, 30
Jitter tolerance for 2400 Hz input	5			Ulpp	1-3, 7, 10-15, 22-23, 25-27, 30
Jitter tolerance for 10 kHz input	1.2			Ulpp	1-3, 7, 10-15, 22-23, 25-27, 30
Jitter tolerance for 40 kHz input	0.5			Ulpp	1-3, 7, 10-15, 22-23, 25-27, 30

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7.12 2.048 MHZ INPUT JITTER TOLERANCE

Description	Min.	Typ.	Max.	Units	Test Conditions / Notes (see "Notes" on page 26)
Jitter tolerance for 1 Hz input	150			UIpp	1-3, 8, 10-15, 22-23, 25-27, 31
Jitter tolerance for 5 Hz input	140			UIpp	1-3, 8, 10-15, 22-23, 25-27, 31
Jitter tolerance for 20 Hz input	130			UIpp	1-3, 8, 10-15, 22-23, 25-27, 31
Jitter tolerance for 300 Hz input	40			UIpp	1-3, 8, 10-15, 22-23, 25-27, 31
Jitter tolerance for 400 Hz input	33			UIpp	1-3, 8, 10-15, 22-23, 25-27, 31
Jitter tolerance for 700 Hz input	18			UIpp	1-3, 8, 10-15, 22-23, 25-27, 31
Jitter tolerance for 2400 Hz input	5.5			UIpp	1-3, 8, 10-15, 22-23, 25-27, 31
Jitter tolerance for 10 kHz input	1.3			UIpp	1-3, 8, 10-15, 22-23, 25-27, 31
Jitter tolerance for 100 kHz input	0.4			UIpp	1-3, 8, 10-15, 22-23, 25-27, 31

7.13 19.44 MHZ INPUT JITTER TOLERANCE

Description	Min.	Typ.	Max.	Units	Test Conditions / Notes (see "Notes" on page 26)
Jitter tolerance for 12 µHz input	2800			UIpp	1-3, 9-15, 22-23, 25-27, 37
Jitter tolerance for 178 µHz input	2800			UIpp	1-3, 9-15, 22-23, 25-27, 37
Jitter tolerance for 0.0016 Hz input	311			UIpp	1-3, 9-15, 22-23, 25-27, 37
Jitter tolerance for 0.0156 Hz input	311			UIpp	1-3, 9-15, 22-23, 25-27, 37
Jitter tolerance for 0.125 Hz input	39			UIpp	1-3, 9-15, 22-23, 25-27, 37
Jitter tolerance for 19.3 Hz input	39			UIpp	1-3, 9-15, 22-23, 25-27, 37
Jitter tolerance for 500 Hz input	1.5			UIpp	1-3, 9-15, 22-23, 25-27, 37
Jitter tolerance for 6.5 kHz input	1.5			UIpp	1-3, 9-15, 22-23, 25-27, 37
Jitter tolerance for 65 kHz input	0.15			UIpp	1-3, 9-15, 22-23, 25-27, 37
Jitter tolerance for 1.3 MHz input	0.15			UIpp	1-3, 9-15, 22-23, 25-27, 37

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Notes:

Voltages are with respect to ground (V_{SS}) unless otherwise stated. Supply voltage and operating temperature are as per Recommended Operating Conditions. Timing parameters are as per Timing Parameter Measurement Voltage Levels.

1. Fref0 reference input selected.
2. Fref1 reference input selected.
3. Normal mode selected.
4. Holdover mode selected.
5. Freerun mode selected.
6. 8 kHz frequency mode selected.
7. 1.544 MHz frequency mode selected.
8. 2.048 MHz frequency mode selected.
9. 19.44 MHz frequency mode selected.
10. Master clock input OSCi at 20 MHz ±0 ppm.
11. Master clock input OSCi at 20 MHz ±32 ppm.
12. Master clock input OSCi at 20 MHz ±100 ppm.
13. Selected reference input at ±0 ppm.
14. Selected reference input at ±32 ppm.
15. Selected reference input at ±100 ppm.
16. For Freerun mode of ±0 ppm.
17. For Freerun mode of ±32 ppm.
18. For Freerun mode of ±100 ppm.
19. For capture range of ±230 ppm.
20. For capture range of ±198 ppm.
21. For capture range of ±130 ppm.
22. 25 pF capacitive load.
23. OSCi Master Clock jitter is less than 2 nspp, or 0.04 UIpp where 1 UIpp = 1/20 MHz.
24. Jitter on reference input is less than 7 nspp.
25. Applied jitter is sinusoidal.
26. Minimum applied input jitter magnitude to regain synchronization.
27. Loss of synchronization is obtained at slightly higher input jitter amplitudes.
28. Within 10 ms of the state, reference or input change.
29. 1 UIpp = 125 µs for 8 kHz signals.
30. 1 UIpp = 648 ns for 1.544 MHz signals.
31. 1 UIpp = 488 ns for 2.048 MHz signals.
32. 1 UIpp = 323 ns for 3.088 MHz signals.
33. 1 UIpp = 244 ns for 4.096 MHz signals.
34. 1 UIpp = 158 ns for 6.312 MHz signals.
35. 1 UIpp = 122 ns for 8.192 MHz signals.
36. 1 UIpp = 61 ns for 16.484 MHz signals.
37. 1 UIpp = 51 ns for 19.44 MHz signals.
38. 1 UIpp = 30 ns for 32.968 MHz signals.
39. No filter.
40. 40 Hz to 100 kHz bandpass filter.
41. With respect to reference input signal frequency.
42. After a $\overline{RST}$ or $\overline{TCLR}$.
43. Master clock duty 40% to 60%.
44. Prior to Holdover mode, device as in Normal mode and phase locked.
45. With input frequency offset of 100 ppm.

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8 TIMING CHARACTERISTICS

8.1 TIMING PARAMETER MEASUREMENT VOLTAGE LEVELS

Parameter	Description	CMOS	Units
V_T	Threshold Voltage	$0.5V_{DDD}$	V
V_{HM}	Rise and Fall Threshold Voltage High	$0.7V_{DDD}$	V
V_{LM}	Rise and Fall Threshold Voltage Low	$0.3V_{DDD}$	V

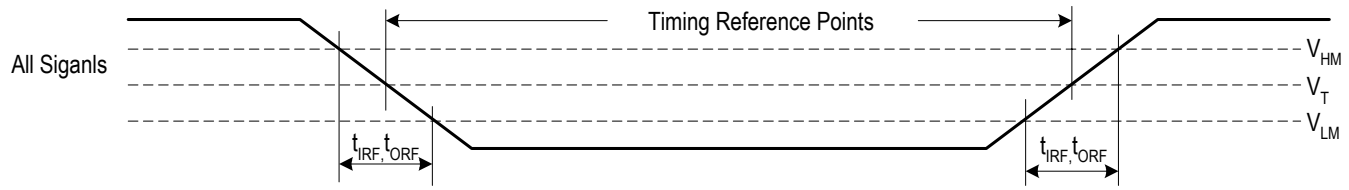


Figure - 11 Timing Parameter Measurement Voltage Levels

Notes:

1. Voltages are with respect to ground (V_{SS}) unless otherwise stated.
2. Supply voltage and operating temperature are as per Recommended Operating Conditions.
3. Timing for input and output signals is based on the worst case result of the CMOS thresholds.

8.2 INPUT/OUTPUT TIMING

Parameter	Description	Min.	Typ.	Max.	Units	Test Conditions
t_{RW}	Reference input pulse width high or low	51			ns	8 kHz, 1.544 MHz or 2.048 MHz reference input
		5			ns	19.44 MHz reference input
t_{IRF}	Reference input rise or fall time			10	ns	
t_{R8D}	8 kHz reference input to F8o delay		8		ns	
t_{R15D}	1.544 MHz reference input to F8o delay		332		ns	
t_{R2D}	2.048 MHz reference input to F8o delay		253		ns	
t_{R19D}	19.44 MHz reference input to F8o delay		8		ns	
t_{F0D}	F8o to $\overline{F0o}$ delay	118	121	124	ns	
t_{F16S}	$\overline{F16o}$ setup to $\overline{C16o}$ falling	25		40	ns	
t_{F16H}	$\overline{F16o}$ hold to $\overline{C16o}$ falling	25		40	ns	
t_{F19S}	F19o setup to C19o falling	20		35	ns	
t_{F19H}	F19o hold to C19o falling	20		35	ns	
t_{C15D}	F8o to C1.5o delay	-3	0	+3	ns	
t_{C3D}	F8o to $\overline{C3o}$ delay	-3	1.6	+3	ns	
t_{C6D}	F8o to C6o delay	-3	1.6	+3	ns	
t_{C2D}	F8o to C2o	-2	0	+2	ns	
t_{C4D}	F8o to $\overline{C4o}$	-2	0	+2	ns	
t_{C8D}	F8o to C8o delay	-2	0	+2	ns	
t_{C16D}	F8o to $\overline{C16o}$ delay	-2	0	+2	ns	

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Parameter	Description	Min.	Typ.	Max.	Units	Test Conditions
t_{C19D}	F8o to C19o delay	-8	0	+8	ns	
t_{C32D}	F8o to $\overline{C32o}$ delay	-2	2	+2	ns	
t_{TSPD}	F8o to TSP delay	-3	0	+3	ns	
t_{RSPD}	F8o to RSP delay	-3	0	+3	ns	
t_{C15W}	C1.5o pulse width high or low		323		ns	
t_{C3W}	$\overline{C3o}$ pulse width high or low		161		ns	
t_{C6W}	C6o pulse width high or low		82		ns	
t_{C2W}	C2o pulse width high or low		244		ns	
t_{C4W}	$\overline{C4o}$ pulse width high or low		122		ns	
t_{C8W}	C8o pulse width high or low		61		ns	
t_{C16W}	$\overline{C16o}$ pulse width high or low		30.5		ns	
t_{C19W}	C19o pulse width high or low		25		ns	
t_{C32WH}	$\overline{C32o}$ pulse width high		14.4		ns	
t_{TSPW}	TSP pulse width high		486		ns	
t_{RSPW}	RSP pulse width high		490		ns	
t_{F0WL}	$\overline{F0o}$ pulse width low		243		ns	
t_{F8WH}	F8o pulse width high		123.6		ns	
t_{F16WL}	$\overline{F16o}$ pulse width low		60.9		ns	
t_{F19WH}	F19o pulse width high		25		ns	
t_{0RF}	Output clock and frame pulse rise or fall time		3		ns	
t_S	Input controls setup Time	100			ns	
t_H	Input controls hold Time	100			ns	
t_{F16D}	F8o to $\overline{F16o}$ delay	27.1	30.1	33.1	ns	
t_{F19D}	F8o to F19o delay	17	25	33	ns	
t_{F32D}	F8o to $\overline{F32o}$ delay	12	15.8	19	ns	
t_{F32S}	$\overline{F32o}$ setup to $\overline{C32o}$ falling	11			ns	
t_{F32H}	$\overline{F32o}$ hold to $\overline{C32o}$ falling	11			ns	
t_{F32WL}	$\overline{F32o}$ pulse width low		30.6		ns	

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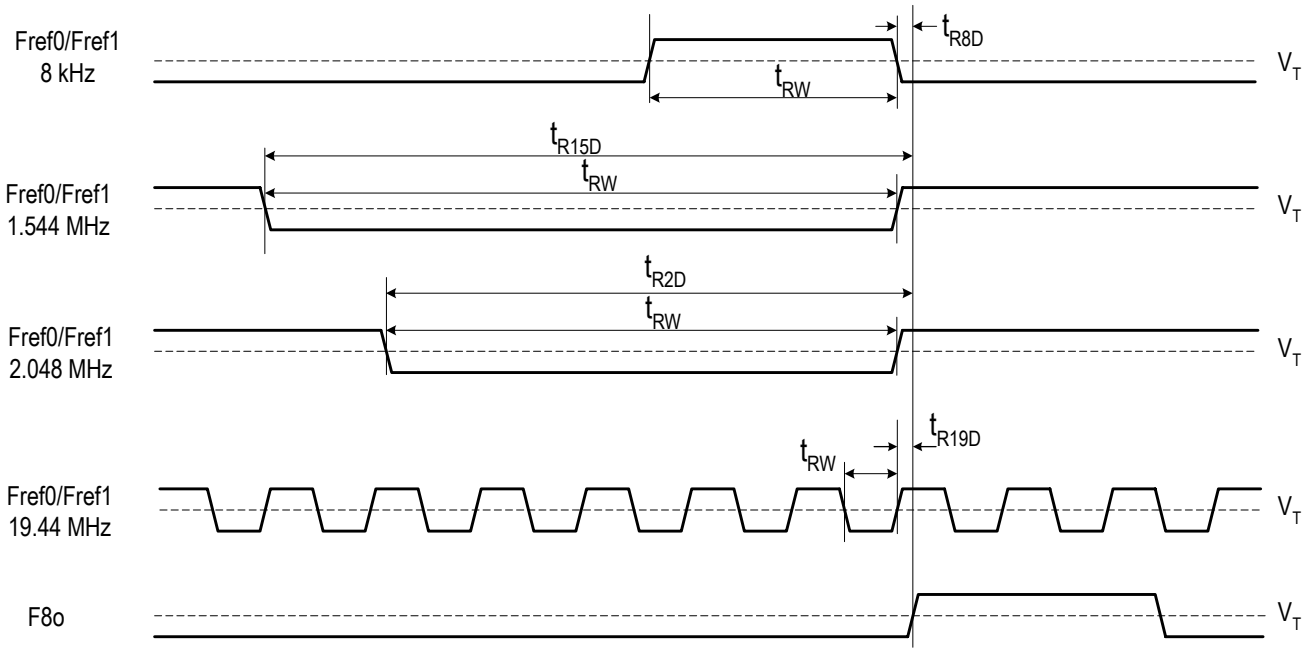


Figure - 12 Input to Output Timing (Normal Mode)

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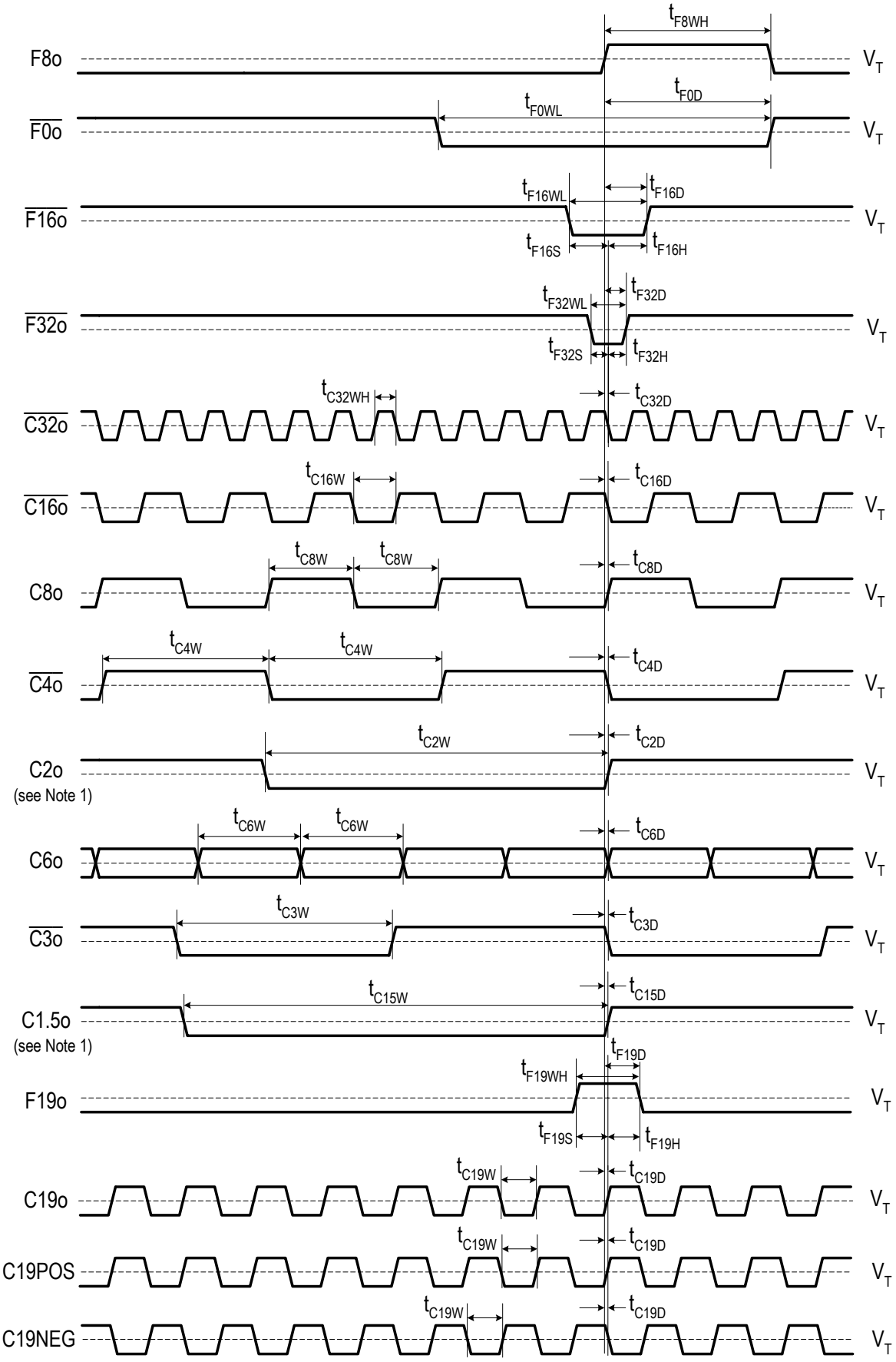


Figure - 13 Output Timing 1

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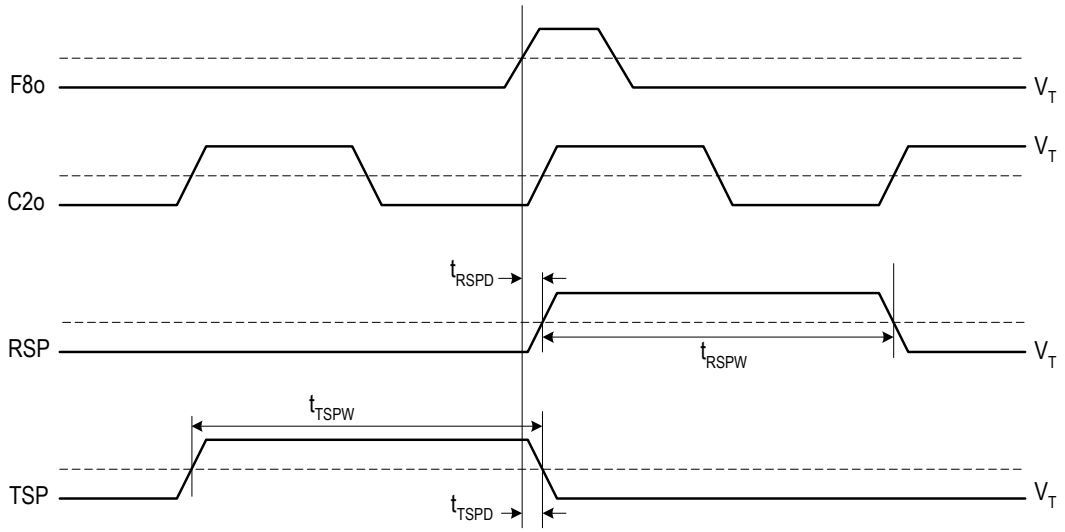


Figure - 14 Output Timing 2

Note 1: The timing characteristic of C2/C1.5 (2.048 MHz or 1.544 MHz) is the same as that of C2o or C1.5o.

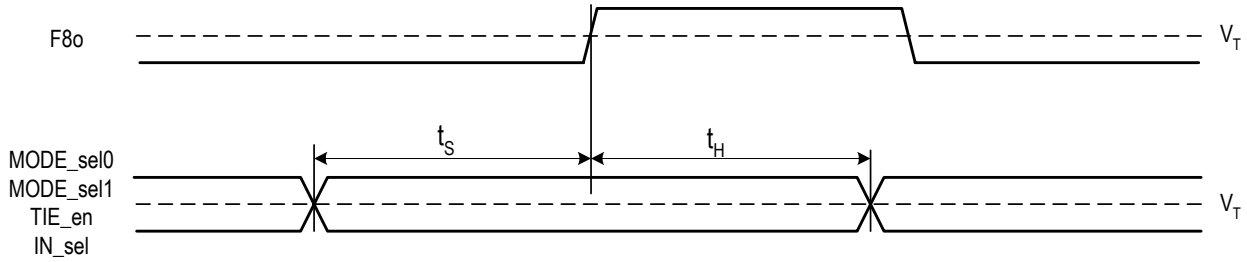
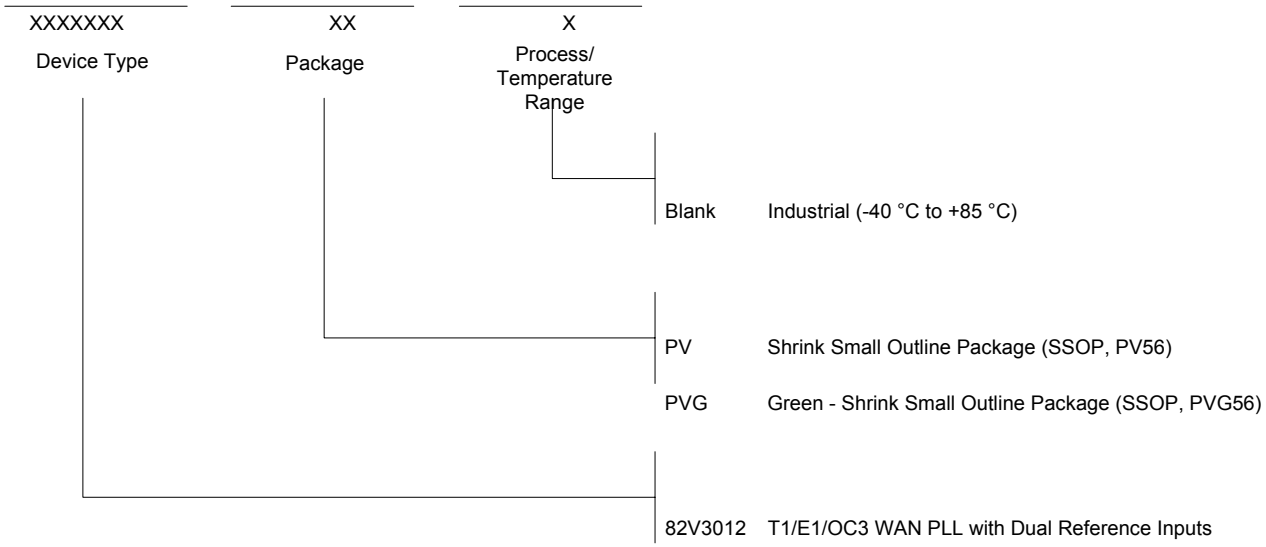


Figure - 15 Input Control Setup and Hold Timing

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9 ORDERING INFORMATION



DATASHEET DOCUMENT HISTORY

07/21/2003 pgs. 7, 8, 17
10/22/2003 pgs. 1, 10, 11, 19, 20, 25, 26
02/02/2004 pgs. 14, 15
11/18/2004 pgs. 1, 10, 31
05/24/2006 pgs. 2, 7, 16
02/06/2009 removed IDT from orderable part number.

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