Low Noise, High Precision, Factory-Programmed Linear Hall-Effect Sensor IC

with Advanced Temperature Compensation and High Bandwidth (120 kHz) Analog Output

FEATURES AND BENEFITS

- Factory-programmed sensitivity and quiescent output voltage with high resolution
- Proprietary segmented linear interpolated temperature compensation (TC) technology provides a typical accuracy of 1% across the full operating temperature range
- Extremely low noise and high resolution achieved via proprietary Hall element and low noise amplifier circuits
- 120 kHz nominal bandwidth achieved via proprietary packaging and chopper stabilization techniques
- Patented circuits suppress IC output spiking during fast current step inputs
- Open circuit detection on ground pin (broken wire)
- Undervoltage lockout for V_{CC} below specification
- Ratiometric sensitivity and quiescent voltage output
- Precise recoverability after temperature cycling

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PACKAGE: 4-pin SIP (suffix KT)

TN Leadform



Not to scale

TH Leadform



Contact Allegro about legacy leadform options

DESCRIPTION

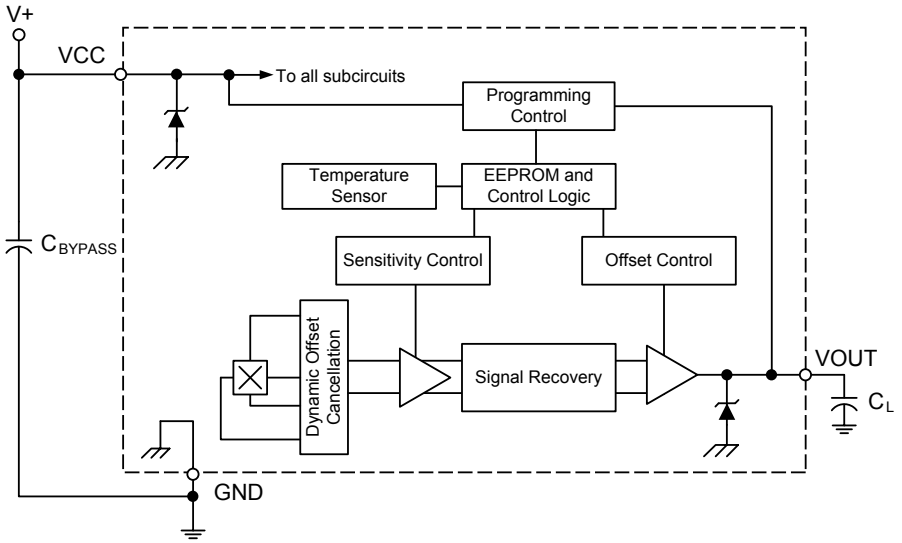
The Allegro™ A1366 factory-programmable linear Hall-effect current sensor IC has been designed to achieve high accuracy and resolution. The goal is achieved through new proprietary linearly interpolated temperature compensation technology that is programmed at the Allegro factory, which provides sensitivity and offset that are virtually flat across the full operating temperature range. The flat performance over temperature makes this IC ideally suited for current sensing applications. Temperature compensation is done in the digital domain with integrated EEPROM technology without sacrificing the analog signal path bandwidth, making this device ideal for HEV inverter, DC-to-DC converter, and electric power steering (EPS) applications.

This ratiometric Hall-effect sensor IC provides a voltage output that is proportional to the applied magnetic field. Sensitivity and quiescent (zero field) output voltage are factory programmed with high resolution, which provides for an accuracy of less than ±1% typical over temperature.

The sensor IC incorporates a highly sensitive Hall element with a BiCMOS interface integrated circuit that employs a low noise, small-signal high-gain amplifier, as well as a low-impedance output stage, and a proprietary, high bandwidth dynamic offset cancellation technique. These advances in Hall-effect technology work together to provide an industry-leading sensing resolution at the full 120 kHz bandwidth. The device has built-in broken ground wire detection for high reliability in automotive applications.

Continued on the next page…

Functional Block Diagram



FEATURES AND BENEFITS (CONTINUED)

- Wide ambient temperature range: –40°C to 150°C
- Immune to mechanical stress
- Extremely thin package: 1 mm case thickness
- AEC-Q100 automotive qualified

DESCRIPTION (CONTINUED)

Device parameters are specified across an extended ambient temperature range: –40°C to 150°C. The A1366 sensor IC is provided in an extremely thin case (1 mm thick), 4-pin SIP (single in-line package, suffix KT) that is lead (Pb) free, with 100% matte tin leadframe plating.

SELECTION GUIDE

Part Number [1]	Leadform	Package	Packing [2]	Sensitivity (Typ.) (mV/G)
A1366LKTTN-1-T	TN (Straight)	4-pin SIP	4000 pieces per 13-inch reel	1
A1366LKTTN-2-T	TN (Straight)	4-pin SIP	4000 pieces per 13-inch reel	2.5
A1366LKTTN-5-T [3]	TN (Straight)	4-pin SIP	4000 pieces per 13-inch reel	5
A1366LKTTN-10-T [3]	TN (Straight)	4-pin SIP	4000 pieces per 13-inch reel	10

[1] TH package leadform options available.
[2] Contact Allegro for additional packing options.
[3] Part variants A1366LKTTN-5-T and A1366LKTTN-10-T are in production but have been determined to be LAST TIME BUY. This classification indicates that the product is obsolete and notice has been given. Sale of this device is currently restricted to existing customer applications. The device should not be purchased for new design applications because of obsolescence in the near future. Samples are no longer available. Status change date: April 1, 2024. Last-time buy date: July 31, 2024

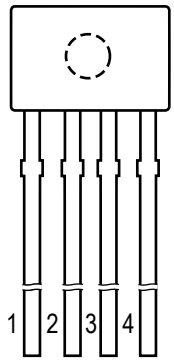
ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{CC}		6	V
Reverse Supply Voltage	V_{RCC}		–0.1	V
Forward Output Voltage	V_{OUT}		25	V
Reverse Output Voltage	V_{ROUT}		–0.1	V
Output Source Current	$I_{OUT(source)}$	VOUT to GND	10	mA
Output Sink Current	$I_{OUT(sink)}$	VCC to VOUT	10	mA
Operating Ambient Temperature	T_A	L temperature range	–40 to 150	°C
Storage Temperature	T_{stg}		–65 to 165	°C
Maximum Junction Temperature	T_J(max)		165	°C

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PINOUT DIAGRAM AND TERMINAL LIST TABLE

Pinout Diagram



(Ejector pin mark on opposite side)

Terminal List Table

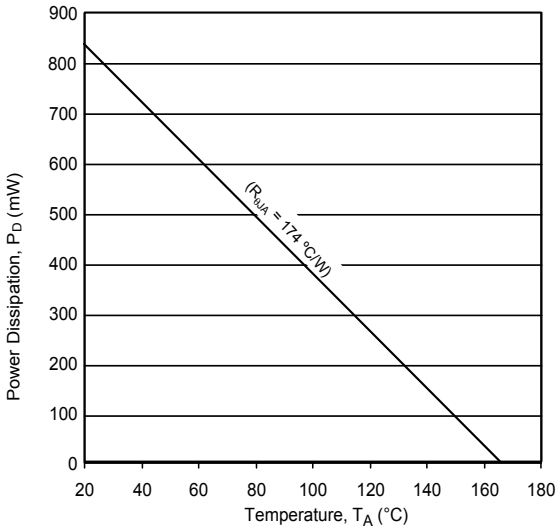
Number	Name	Function
1	VCC	Input power supply, use bypass capacitor to connect to ground
2	VOUT	Output signal
3	NC	No connection; connect to GND for optimal ESD performance
4	GND	Ground

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	On 1-layer PCB with exposed copper limited to solder pads	174	°C/W

*Additional thermal information available on the Allegro website

Power Dissipation versus Ambient Temperature



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COMMON OPERATING CHARACTERISTICS: Valid through the full operating temperature range, T_A, C_{BYPASS} = 0.1 µF, V_{CC} = 5 V, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit [1]
ELECTRICAL CHARACTERISTICS						
Supply Voltage	V_{CC}		4.5	5.0	5.5	V
Supply Current	I_{CC}	No load on VOUT	–	10	15	mA
Power-On Time [2]	t_{PO}	T_A = 25°C, C_{BYPASS} = Open, C_L = 1 nF, Sens = 2.5 mV/G, constant magnetic field of 320 G	–	78	–	µs
Temperature Compensation Power-On Time [2]	t_{TC}	T_A = 150°C, C_{BYPASS} = Open, C_L = 1 nF, Sens = 2.5 mV/G, constant magnetic field of 320 G	–	30	–	µs
Undervoltage Lockout (UVLO) Threshold [2]	V_{UVLOH}	T_A = 25°C, V_{CC} rising and device function enabled	–	4	–	V
	V_{UVLOL}	T_A = 25°C, V_{CC} falling and device function disabled	–	3.5	–	V
UVLO Enable/Disable Delay Time [2]	t_{UVLOE}	T_A = 25°C, C_{BYPASS} = Open, C_L = 1 nF, Sens = 2.5 mV/G, V_{CC} Fall Time (5 V to 3 V) = 1.5 µs	–	64	–	µs
	t_{UVLOD}	T_A = 25°C, C_{BYPASS} = Open, C_L = 1 nF, Sens = 2.5 mV/G, V_{CC} Recover Time (3 V to 5 V) = 1.5 µs	–	14	–	µs
Power-On Reset Voltage [2]	V_{PORH}	T_A = 25°C, V_{CC} rising	–	2.6	–	V
	V_{PORL}	T_A = 25°C, V_{CC} falling	–	2.3	–	V
Power-On Reset Release Time [2]	t_{PORR}	T_A = 25°C, V_{CC} rising	–	64	–	µs
Supply Zener Clamp Voltage	V_z	T_A = 25°C, I_{CC} = 30 mA	6.5	7.5	–	V
Internal Bandwidth	BW_i	Small signal –3 dB, C_L = 1 nF, T_A = 25°C	–	120	–	kHz
Chopping Frequency [3]	f_C	T_A = 25°C	–	500	–	kHz
OUTPUT CHARACTERISTICS						
Propagation Delay Time [2]	t_{PD}	T_A = 25°C, magnetic field step of 320 G, C_L = 1 nF, Sens = 2.5 mV/G	–	2.2	–	µs
Rise Time [2]	t_R	T_A = 25°C, magnetic field step of 320 G, C_L = 1 nF, Sens = 2.5 mV/G	–	3.6	–	µs
Response Time [2]	$t_{RESPONSE}$	T_A = 25°C, magnetic field step of 320 G, C_L = 1 nF, Sens = 2.5 mV/G	–	3.7	–	µs
Output Saturation Voltage [2]	$V_{SAT(HIGH)}$	T_A = 25°C, $R_{L(PULLDWN)}$ = 10 kΩ to GND	4.7	–	–	V
	$V_{SAT(LOW)}$	T_A = 25°C, $R_{L(PULLUP)}$ = 10 kΩ to VCC	–	–	400	mV
Broken Wire Voltage [2]	$V_{BRK(HIGH)}$	T_A = 25°C, $R_{L(PULLUP)}$ = 10 kΩ to VCC	–	V_{CC}	–	V
	$V_{BRK(LOW)}$	T_A = 25°C, $R_{L(PULLDWN)}$ = 10 kΩ to GND	–	100	–	mV

Continued on the next page…

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COMMON OPERATING CHARACTERISTICS (continued): Valid through the full operating temperature range, T_A, C_{BYPASS} = 0.1 µF, V_{CC} = 5 V, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit [1]
OUTPUT CHARACTERISTICS (continued)						
Noise	B_N	T_A = 25°C, C_L = 1 nF, Bandwidth = BW_i	–	1.1	–	$mG_{RMS}/\sqrt{(Hz)}$
DC Output Resistance	R_{OUT}		–	9	–	Ω
Output Load Resistance	$R_{L(PULLUP)}$	VOUT to VCC	4.7	–	–	kΩ
	$R_{L(PULLDWN)}$	VOUT to GND	4.7	–	–	kΩ
Output Load Capacitance [4]	C_L	VOUT to GND	–	1	10	nF
Output Slew Rate [5]	SR	Sens = 2.5 mV/G, C_L = 1 nF	–	230	–	V/ms
ERROR COMPONENTS						
Linearity Sensitivity Error [2][6]	Lin_{ERR}		–1	< ±0.25	1	%
Symmetry Sensitivity Error [2]	Sym_{ERR}		–1	< ±0.25	1	%
Ratiometry Quiescent Voltage Output Error [2][7]	$Rat_{ERRVOUT(Q)}$	Through supply voltage range (relative to V_{CC} = 5 V)	–1	0	1	%
Ratiometry Sensitivity Error [2][7]	$Rat_{ERRSens}$	Through supply voltage range (relative to V_{CC} = 5 V)	–	±1	–	%

[1] 1 G (gauss) = 0.1 mT (millitesla).
[2] See Characteristic Definitions section.
[3] f_C varies up to approximately ± 20% over the full operating ambient temperature range, T_A, and process.
[4] Output stability is maintained for capacitive loads as large as 10 nF.
[5] High-to-low transition of output voltage is a function of external load components and device sensitivity.
[6] Linearity applies to output voltage ranges of ±2 V from the quiescent output for bidirectional devices.
[7] Percent change from actual value at V_{CC} = 5 V, for a given temperature, through the supply voltage operating range.

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A1366LKT-1-T PERFORMANCE CHARACTERISTICS [1]**:** T_A = –40°C to 150°C, C_{BYPASS} = 0.1 µF, V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit [2]
Sensitivity [3]	$Sens_{TA}$	Measured using 600 G, T_A = 25°C	0.975	1	1.025	mV/G
Sensitivity Drift through Temperature Range	$\Delta Sens_{TC}$	T_A = 25°C to 150°C	–2.5	0	2.5	%
		T_A = –40°C to 25°C	–2.5	0	2.5	%
Sensitivity Drift Due to Package Hysteresis	$\Delta Sens_{PKG}$	T_A = 25°C, after temperature cycling, 25°C to 150°C and back to 25°C	–	±1.25	–	%
Sensitivity Drift Over Lifetime [4]	$\Delta Sens_{LIFE}$	T_A = –40°C to 150°C, shift after AEC-Q100 grade 0 qualification testing	–	±1	–	%
Noise	V_N	T_A = 25°C, C_L = 1 nF	–	3.15	–	mV_{P-P}
		T_A = 25°C, C_L = 1 nF	–	0.5	–	mV_{RMS}
Quiescent Output Voltage [5]	$V_{OUT(Q)TA}$	T_A = 25°C	2.490	2.500	2.510	V
	$V_{OUT(Q)HT}$	T_A = 25°C to 150°C	2.490	2.500	2.510	V
	$V_{OUT(Q)LT}$	T_A = –40°C to 25°C	2.490	2.500	2.510	V
Quiescent Output Voltage Drift Over Lifetime [4]	$\Delta V_{OUT(Q)LIFE}$	T_A = –40°C to 150°C, shift after AEC-Q100 grade 0 qualification testing	–	±2	–	mV

[1] See Characteristic Performance Data section for parameter distributions across temperature range.
[2] 1 G (gauss) = 0.1 mT (millitesla).
[3] This parameter may drift a maximum of $\Delta Sens_{LIFE}$ over lifetime.
[4] Based on characterization data obtained during standardized stress test for Qualification of Integrated Circuits, cannot be guaranteed. Drift is a function of customer application conditions. Contact Allegro MicroSystems for further information.
[5] This parameter may drift a maximum of $\Delta V_{OUT(Q)LIFE}$ over lifetime.

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A1366LKT-2-T PERFORMANCE CHARACTERISTICS [1]**:** T_A = –40°C to 150°C, C_{BYPASS} = 0.1 µF, V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit [2]
Sensitivity [3]	$Sens_{TA}$	Measured using 400 G, T_A = 25°C	2.437	2.5	2.563	mV/G
Sensitivity Drift through Temperature Range	$\Delta Sens_{TC}$	T_A = 25°C to 150°C	–2.5	0	2.5	%
		T_A = –40°C to 25°C	–2.5	0	2.5	%
Sensitivity Drift Due to Package Hysteresis	$\Delta Sens_{PKG}$	T_A = 25°C, after temperature cycling, 25°C to 150°C and back to 25°C	–	±1.25	–	%
Sensitivity Drift Over Lifetime [4]	$\Delta Sens_{LIFE}$	T_A = –40°C to 150°C, shift after AEC-Q100 grade 0 qualification testing	–	±1	–	%
Noise	V_N	T_A = 25°C, C_L = 1 nF	–	7.875	–	mV_{P-P}
		T_A = 25°C, C_L = 1 nF	–	1.25	–	mV_{RMS}
Quiescent Output Voltage [5]	$V_{OUT(Q)TA}$	T_A = 25°C	2.490	2.500	2.510	V
	$V_{OUT(Q)HT}$	T_A = 25°C to 150°C	2.490	2.500	2.510	V
	$V_{OUT(Q)LT}$	T_A = –40°C to 25°C	2.490	2.500	2.510	V
Quiescent Output Voltage Drift Over Lifetime [4]	$\Delta V_{OUT(Q)LIFE}$	T_A = –40°C to 150°C, shift after AEC-Q100 grade 0 qualification testing	–	±2	–	mV

[1] See Characteristic Performance Data section for parameter distributions across temperature range.
[2] 1 G (gauss) = 0.1 mT (millitesla).
[3] This parameter may drift a maximum of $\Delta Sens_{LIFE}$ over lifetime.
[4] Based on characterization data obtained during standardized stress test for Qualification of Integrated Circuits, cannot be guaranteed. Drift is a function of customer application conditions. Contact Allegro MicroSystems for further information.
[5] This parameter may drift a maximum of $\Delta V_{OUT(Q)LIFE}$ over lifetime.

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A1366LKT-5-T PERFORMANCE CHARACTERISTICS [1]: T_A = –40°C to 150°C, C_{BYPASS} = 0.1 µF, V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit [2]
Sensitivity [3]	$Sens_{TA}$	Measured using 200 G, T_A = 25°C	4.875	5	5.125	mV/G
Sensitivity Drift through Temperature Range	$\Delta Sens_{TC}$	T_A = 25°C to 150°C	–2.5	0	2.5	%
		T_A = –40°C to 25°C	–2.5	0	2.5	%
Sensitivity Drift Due to Package Hysteresis	$\Delta Sens_{PKG}$	T_A = 25°C, after temperature cycling, 25°C to 150°C and back to 25°C	–	±1.25	–	%
Sensitivity Drift Over Lifetime [4]	$\Delta Sens_{LIFE}$	T_A = –40°C to 150°C, shift after AEC-Q100 grade 0 qualification testing	–	±1	–	%
Noise	V_N	T_A = 25°C, C_L = 1 nF	–	15.75	–	mV_{P-P}
		T_A = 25°C, C_L = 1 nF	–	2.5	–	mV_{RMS}
Quiescent Output Voltage [5]	$V_{OUT(Q)TA}$	T_A = 25°C	2.490	2.500	2.510	V
	$V_{OUT(Q)HT}$	T_A = 25°C to 150°C	2.490	2.500	2.510	V
	$V_{OUT(Q)LT}$	T_A = –40°C to 25°C	2.490	2.500	2.510	V
Quiescent Output Voltage Drift Over Lifetime [4]	$\Delta V_{OUT(Q)LIFE}$	T_A = –40°C to 150°C, shift after AEC-Q100 grade 0 qualification testing	–	±2	–	mV

[1] See Characteristic Performance Data section for parameter distributions across temperature range.
[2] 1 G (gauss) = 0.1 mT (millitesla).
[3] This parameter may drift a maximum of $\Delta Sens_{LIFE}$ over lifetime.
[4] Based on characterization data obtained during standardized stress test for Qualification of Integrated Circuits, cannot be guaranteed. Drift is a function of customer application conditions. Contact Allegro MicroSystems for further information.
[5] This parameter may drift a maximum of $\Delta V_{OUT(Q)LIFE}$ over lifetime.

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A1366LKT-10-T PERFORMANCE CHARACTERISTICS [1]: T_A = –40°C to 150°C, C_{BYPASS} = 0.1 µF, V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit [2]
Sensitivity [3]	$Sens_{TA}$	Measured using 100 G, T_A = 25°C	9.75	10	10.25	mV/G
Sensitivity Drift through Temperature Range	$\Delta Sens_{TC}$	T_A = 25°C to 150°C	–2.5	0	2.5	%
		T_A = –40°C to 25°C	–2.5	0	2.5	%
Sensitivity Drift Due to Package Hysteresis	$\Delta Sens_{PKG}$	T_A = 25°C, after temperature cycling, 25°C to 150°C and back to 25°C	–	±1.25	–	%
Sensitivity Drift Over Lifetime [4]	$\Delta Sens_{LIFE}$	T_A = –40°C to 150°C, shift after AEC-Q100 grade 0 qualification testing	–	±1	–	%
Noise	V_N	T_A = 25°C, C_L = 1 nF	–	31.5	–	mV_{P-P}
		T_A = 25°C, C_L = 1 nF	–	5	–	mV_{RMS}
Quiescent Output Voltage [5]	$V_{OUT(Q)TA}$	T_A = 25°C	2.485	2.500	2.515	V
	$V_{OUT(Q)HT}$	T_A = 25°C to 150°C	2.485	2.500	2.515	V
	$V_{OUT(Q)LT}$	T_A = –40°C to 25°C	2.485	2.500	2.515	V
Quiescent Output Voltage Drift Over Lifetime [4]	$\Delta V_{OUT(Q)LIFE}$	T_A = –40°C to 150°C, shift after AEC-Q100 grade 0 qualification testing	–	±2	–	mV

[1] See Characteristic Performance Data section for parameter distributions across temperature range.
[2] 1 G (gauss) = 0.1 mT (millitesla).
[3] This parameter may drift a maximum of $\Delta Sens_{LIFE}$ over lifetime.
[4] Based on characterization data obtained during standardized stress test for Qualification of Integrated Circuits, cannot be guaranteed. Drift is a function of customer application conditions. Contact Allegro MicroSystems for further information.
[5] This parameter may drift a maximum of $\Delta V_{OUT(Q)LIFE}$ over lifetime.

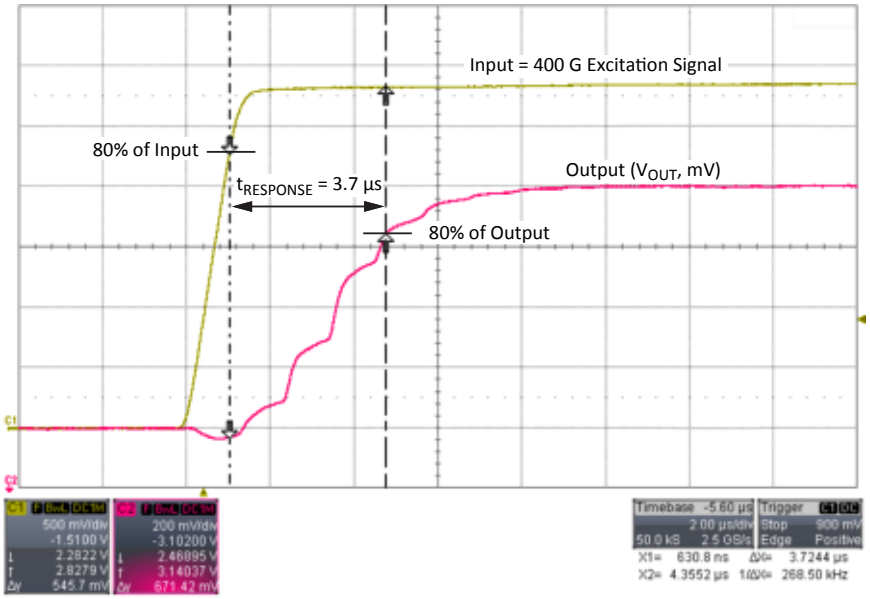
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CHARACTERISTIC PERFORMANCE DATA

Response Time ($t_{RESPONSE}$)

400 G excitation signal with 10%-90% rise time = 1 µs

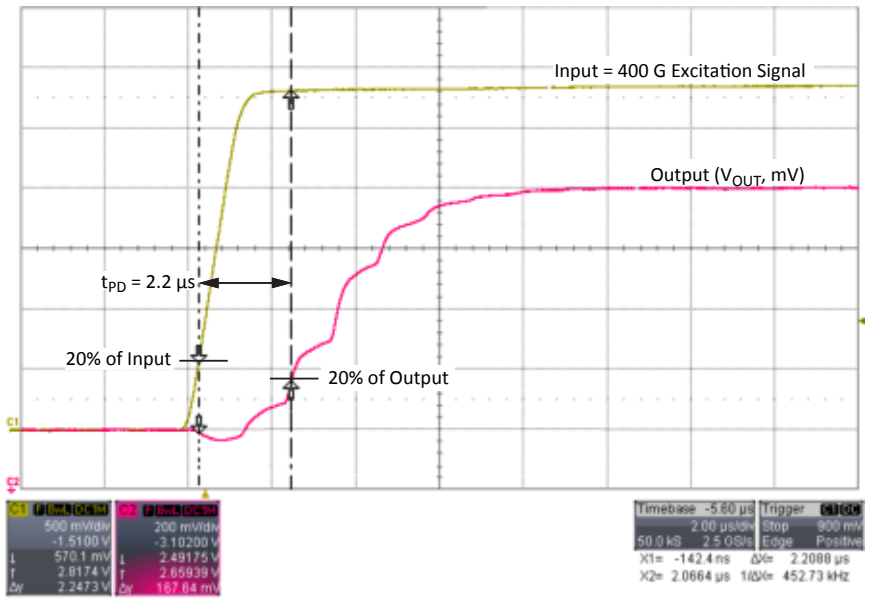
Sensitivity = 2 mV/G, C_{BYPASS}=0.1 µF, C_L=1 nF



Propagation Delay (t_{PD})

400 G excitation signal with 10%-90% rise time = 1 µs

Sensitivity = 2 mV/G, C_{BYPASS}=0.1 µF, C_L=1 nF

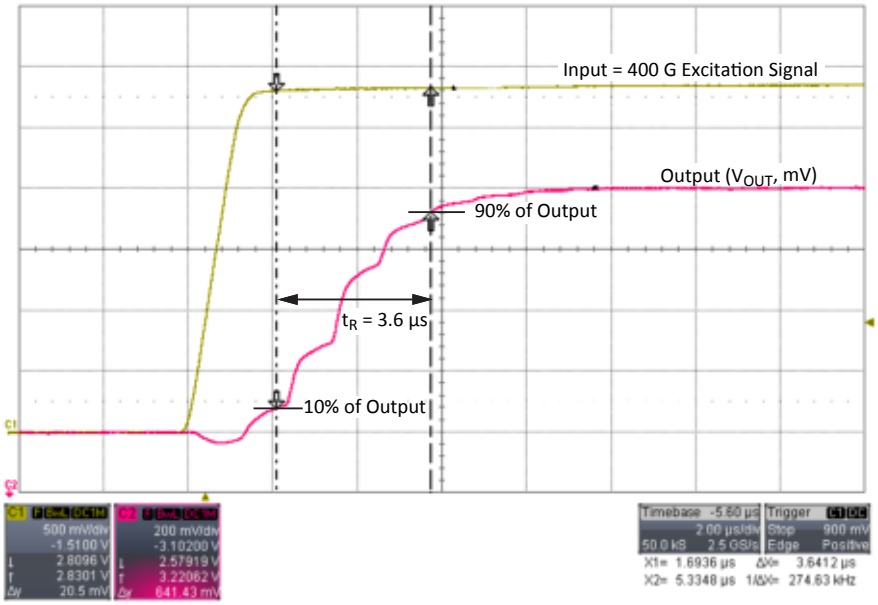


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Rise Time (t_R)

400 G excitation signal with 10%-90% rise time = 1 µs

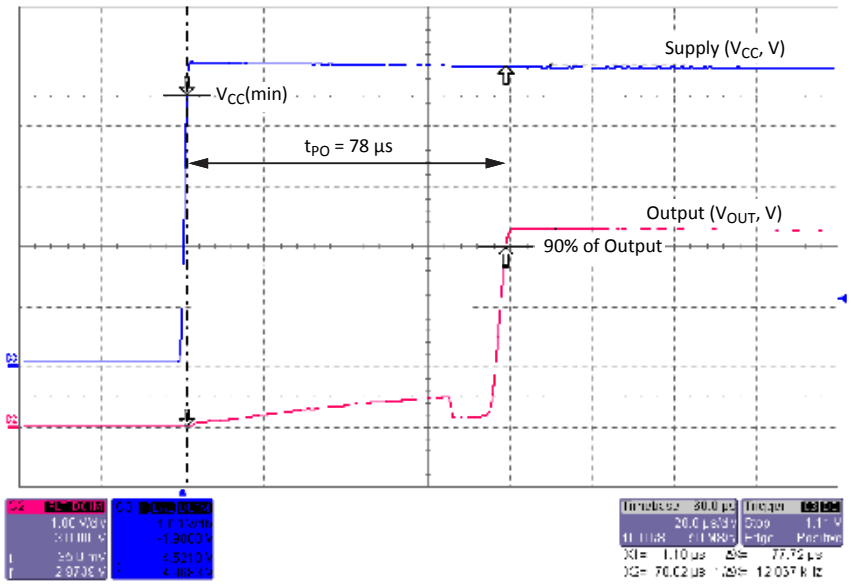
Sensitivity = 2 mV/G, C_{BYPASS}=0.1 µF, C_L=1 nF



Power-On Time(t_{PO})

400 G constant excitation signal, with V_{CC} 10%-90% rise time = 1.5 µs

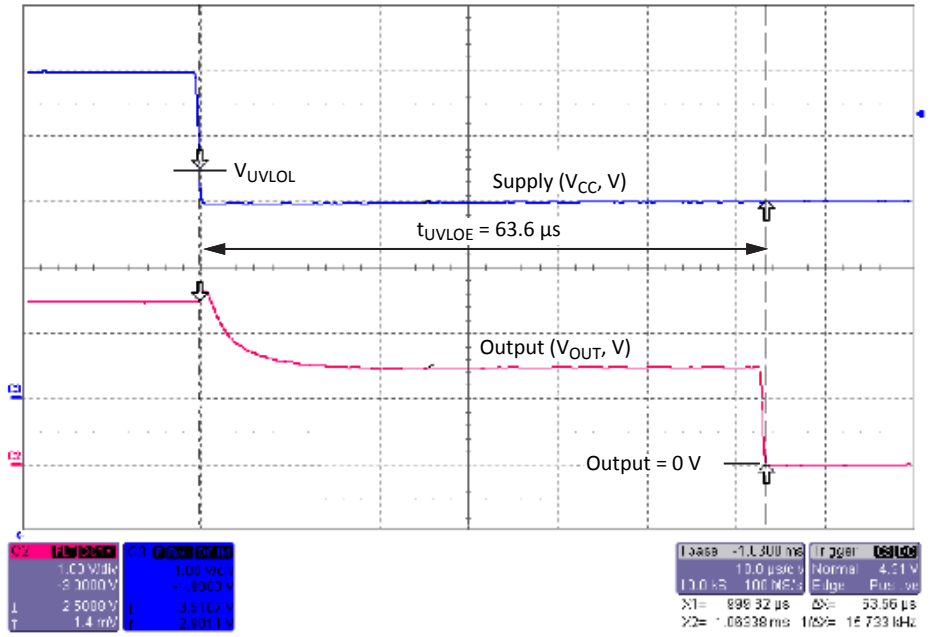
Sensitivity = 2 mV/G, C_{BYPASS}= Open, C_L=1 nF



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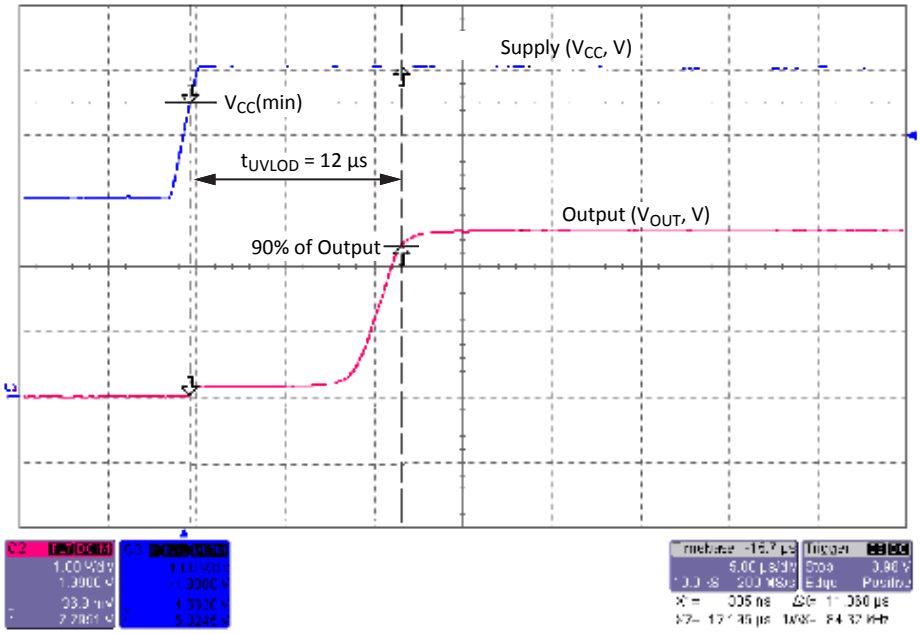
UVLO Enable Time (t_{UVLOE})

V_{CC} 5 V-3 V fall time = 1.5 µs
Sensitivity = 2 mV/G, C_{BYPASS}= Open, C_L=1 nF



UVLO Disable Time (t_{UVLOD})

V_{CC} 3 V-5 V recovery time = 1.5 µs
Sensitivity = 2 mV/G, C_{BYPASS}= Open, C_L=1 nF



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CHARACTERISTIC DEFINITIONS

Power-On Time (t_{PO}). When the supply is ramped to its operating voltage, the device requires a finite time to power its internal components before responding to an input magnetic field.

Power-On Time, t_{PO}, is defined as: the time it takes for the output voltage to settle within ±10% of its steady state value under an applied magnetic field, after the power supply has reached its minimum specified operating voltage, V_{CC}(min), as shown in figure 1.

Temperature Compensation Power-On Time (t_{TC}). After Power-On Time, t_{PO}, elapses, t_{TC} is also required before a valid temperature compensated output.

Propagation Delay (t_{PD}). The time interval between a) when the applied magnetic field reaches 20% of it's final value, and b) when the output reaches 20% of its final value (see figure 2).

Rise Time (t_R). The time interval between a) when the sensor IC reaches 10% of its final value, and b) when it reaches 90% of its final value (see Figure 2).

Response Time ($t_{RESPONSE}$). The time interval between a) when the applied magnetic field reaches 80% of its final value, and b) when the sensor reaches 80% of its output corresponding to the applied magnetic field (see Figure 3).

Quiescent Voltage Output ($V_{OUT(Q)}$). In the quiescent state (no significant magnetic field: B = 0 G), the output, $V_{OUT(Q)}$, has a

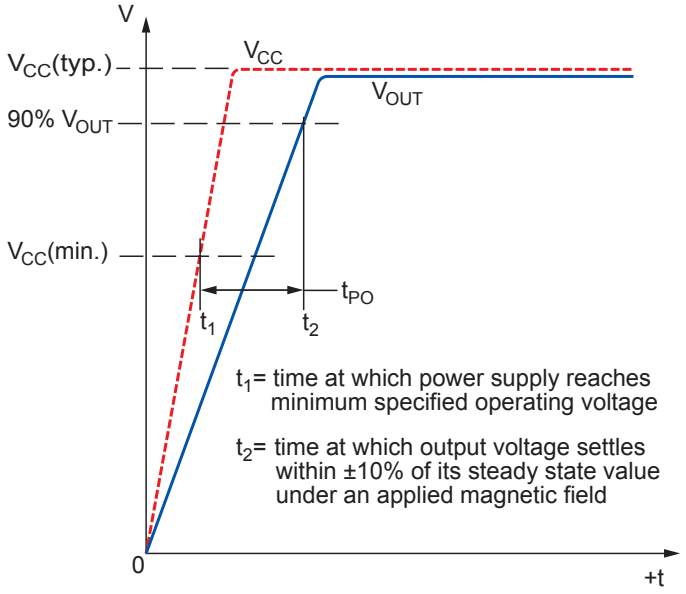


Figure 1: Power-on Time definition

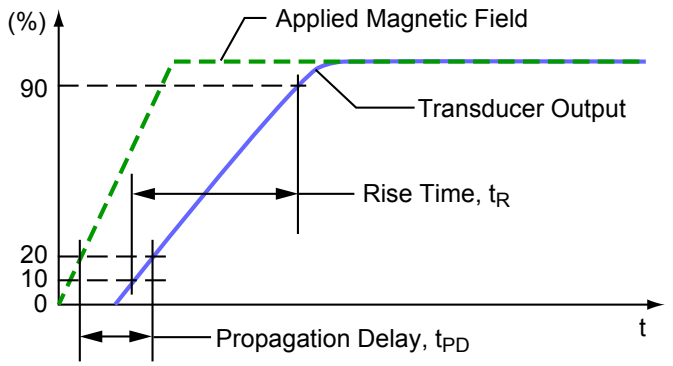


Figure 2: Propagation Delay and Rise Time definitions

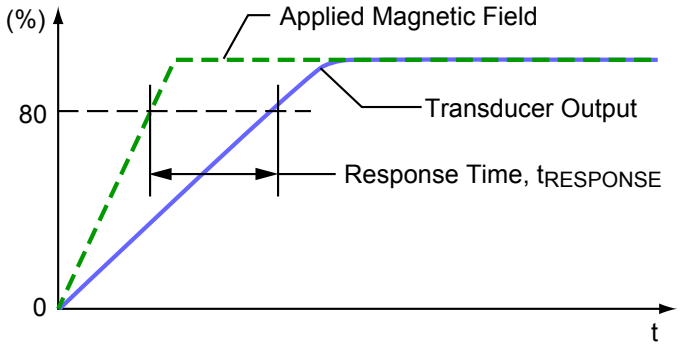


Figure 3: Response Time definition

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constant ratio to the supply voltage, V_{CC}, throughout the entire operating ranges of V_{CC} and ambient temperature, T_A.

Sensitivity (Sens). The presence of a south polarity magnetic field, perpendicular to the branded surface of the package face, increases the output voltage from its quiescent value toward the supply voltage rail. The amount of the output voltage increase is proportional to the magnitude of the magnetic field applied.

Conversely, the application of a north polarity field decreases the output voltage from its quiescent value. This proportionality is specified as the magnetic sensitivity, Sens (mv/G), of the device, and it is defined as:

$$\text{Sens} = \frac{V_{OUT(BPOS)} - V_{OUT(BNEG)}}{\text{BPOS} - \text{BNEG}} \quad , \tag{1}$$

where BPOS and BNEG are two magnetic fields with opposite polarities.

Sensitivity Drift Through Temperature Range ($\Delta Sens_{TC}$). Second order sensitivity temperature coefficient effects cause the magnetic sensitivity, Sens, to drift from its expected value over the operating ambient temperature range, T_A. The Sensitivity Drift Through Temperature Range, $\Delta Sens_{TC}$, is defined as:

$$\Delta\text{Sens}_{TC} = \frac{\text{Sens}_{TA} - \text{Sens}_{EXPECTED(TA)}}{\text{Sens}_{EXPECTED(TA)}} \times 100\% \quad . \tag{2}$$

Sensitivity Drift Due to Package Hysteresis ($\Delta Sens_{PKG}$). Package stress and relaxation can cause the device sensitivity at T_A = 25°C to change during and after temperature cycling. The sensitivity drift due to package hysteresis, $\Delta Sens_{PKG}$, is defined as:

$$\Delta\text{Sens}_{PKG} = \frac{\text{Sens}_{(25°C)2} - \text{Sens}_{(25°C)1}}{\text{Sens}_{(25°C)1}} \times 100\% \quad , \tag{3}$$

where $Sens_{(25°C)1}$ is the programmed value of sensitivity at T_A = 25°C, and $Sens_{(25°C)2}$ is the value of sensitivity at T_A = 25°C, after temperature cycling T_A up to 150°C and back to 25°C.

Linearity Sensitivity Error (Lin_{ERR}). The A1366 is designed to provide a linear output in response to a ramping applied magnetic field. Consider two magnetic fields, B1 and B2. Ideally, the sensitivity of a device is the same for both fields, for a given supply voltage and temperature. Linearity error is present when there is a difference between the sensitivities measured at B1 and B2.

Linearity Error. is calculated separately for the positive (Lin_{ERRPOS}) and negative (Lin_{ERRNEG}) applied magnetic fields. Linearity Error (%) is measured and defined as:

$$\text{Lin}_{ERRPOS} = \left(1 - \frac{\text{Sens}_{BPOS2}}{\text{Sens}_{BPOS1}}\right) \times 100\% \quad ,$$

$$\text{Lin}_{ERRNEG} = \left(1 - \frac{\text{Sens}_{BNEG2}}{\text{Sens}_{BNEG1}}\right) \times 100\% \quad , \tag{4}$$

where:

$$\text{Sens}_{Bx} = \frac{|V_{OUT(Bx)} - V_{OUT(Q)}|}{B_x} \quad , \tag{5}$$

and BPOSx and BNEGx are positive and negative magnetic fields, with respect to the quiescent voltage output such that |BPOS2| = 2 × |BPOS1| and |BNEG2| = 2 × |BNEG1|.

Then:

$$\text{Lin}_{ERR} = \max(\text{Lin}_{ERRPOS}, \text{Lin}_{ERRNEG}) \quad . \tag{6}$$

Symmetry Sensitivity Error (Sym_{ERR}). The magnetic sensitivity of an A1366 device is constant for any two applied magnetic fields of equal magnitude and opposite polarities. Symmetry Error, Sym_{ERR} (%), is measured and defined as:

$$\text{Sym}_{ERR} = \left(1 - \frac{\text{Sens}_{BPOS}}{\text{Sens}_{BNEG}}\right) \times 100\% \quad , \tag{7}$$

where $Sens_{Bx}$ is as defined in equation 7, and BPOSx and BNEGx are positive and negative magnetic fields such that |BPOSx| = |BNEGx|.

Ratiometry Error (Rat_{ERR}). The A1366 device features ratiometric output. This means that the Quiescent Voltage Output, $V_{OUT(Q)}$, and magnetic sensitivity, Sens, are proportional to the Supply Voltage, V_{CC}. In other words, when the supply voltage increases or decreases by a certain percentage, each characteristic also increases or decreases by the same percentage. Error is the difference between the measured change in the supply voltage relative to 5 V, and the measured change in each characteristic.

The ratiometric error in Quiescent Voltage Output, $Rat_{ERRVOUT(Q)}$ (%), for a given supply voltage, V_{CC}, is defined as:

$$\text{Rat}_{ERRVOUT(Q)} = \left(1 - \frac{V_{OUT(Q)(VCC)} / V_{OUT(Q)(5V)}}{V_{CC} / 5\text{ V}}\right) \times 100\% \tag{8}$$

The ratiometric error in magnetic sensitivity, $Rat_{ERRSens}$ (%), for a given Supply Voltage, V_{CC}, is defined as:

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$$Rat_{ERRSens} = \left(1 - \frac{Sens_{(VCC)} / Sens_{(5V)}}{V_{CC} / 5\ V}\right) \times 100\% \quad . \qquad (9)$$

Power-On Reset Voltage (V_{POR}). On power-up, to initialize to a known state and avoid current spikes, the A1366 is held in a Reset state. The Reset signal is disabled when V_{CC} reaches V_{UVLOH} and time t_{PORR} has elapsed, allowing the output voltage to go from a high impedance state into normal operation. During power-down, the Reset signal is enabled when V_{CC} reaches V_{PORL}, causing the output voltage to go into a high impedance state. (Note that detailed description of POR and UVLO operation can be found in the Functional Description section).

Power-On Reset Release Time (t_{PORR}). When V_{CC} rises to V_{PORH}, the Power-On Reset Counter starts. The A1366 output voltage will transition from a high impedance state to normal operation only when the Power-On Reset Counter has reached t_{PORR} and V_{CC} has exceeded V_{UVLOH}.

Undervoltage Lockout Threshold (V_{UVLO}). If V_{CC} drops below V_{UVLOL} output voltage will be locked to GND. If V_{CC} starts rising, the A1366 will come out of the Lock state when V_{CC} reaches V_{UVLOH}.

UVLO Enable/Disable Delay Time (t_{UVLO}). When a falling V_{CC} reaches V_{UVLOL}, time t_{UVLOE} is required to engage Undervoltage Lockout state. When V_{CC} rises above V_{UVLOH}, time t_{UVLOD} is required to disable UVLO and have a valid output voltage.

Broken Wire Voltage (V_{BRK}). If the GND pin is disconnected (broken wire event), the output voltage will go to $V_{BRK(HIGH)}$ (if a load resistor is connected to VCC) or to $V_{BRK(LOW)}$ (if a load resistor is connected to GND).

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FUNCTIONAL DESCRIPTION

Power-On Reset (POR) and Undervoltage Lockout (UVLO) Operation

The descriptions in this section assume: temperature = 25°C, no output load (R_L, C_L), and no significant magnetic field is present.

• ***Power-Up.*** At power-up, as V_{CC} ramps up, the output is in a high impedance state. When V_{CC} crosses V_{PORH} (location [1] in Figure 4 and [1'] in Figure 5), the POR Release counter starts counting for t_{PORR} = 64 µs. At this point, if V_{CC} exceeds V_{UVLOH} = 4 V [2'], the output will go to V_{CC} / 2 after t_{UVLOD} = 14 µs [3']. If V_{CC} does not exceed V_{UVLOH} = 4 V [2], the output will stay in the high impedance state until V_{CC} reaches V_{UVLOH} = 4 V [3] and then will go to V_{CC} / 2 after t_{UVLOD} = 14 µs [4].

• ***V_{CC} drops below V_{CC}(min)= 4.5 V.*** If V_{CC} drops below V_{UVLOL} [4', 5], the UVLO Enable Counter starts counting. If V_{CC} is still below V_{UVLOL} when counter reaches t_{UVLOE} = 64 µs, the UVLO function will be enabled and the output will be pulled near GND [6]. If V_{CC} exceeds V_{UVLOL} before the UVLO Enable Counter reaches 64 µs [5'], the output will continue to be V_{CC}/2.

• ***Coming out of UVLO.*** While UVLO is enabled [6], if V_{CC} exceeds V_{UVLOH} [7], UVLO will be disabled after t_{UVLOD} =14 µs, and the output will be V_{CC} / 2 [8].

• ***Power-Down.*** As V_{CC} ramps down below V_{UVLOL} [6', 9], the UVLO Enable Counter will start counting. If V_{CC} is higher than V_{PORL} = 2.3 V when the counter reaches t_{UVLOE} = 64 µs, the UVLO function will be enabled and the output will be pulled near GND [10]. The output will enter a high impedance state as V_{CC} goes below V_{PORL} [11]. If V_{CC} falls below V_{PORL} before the UVLO Enable Counter reaches 64 µs, the output will transition directly into a high impedance state [7'].

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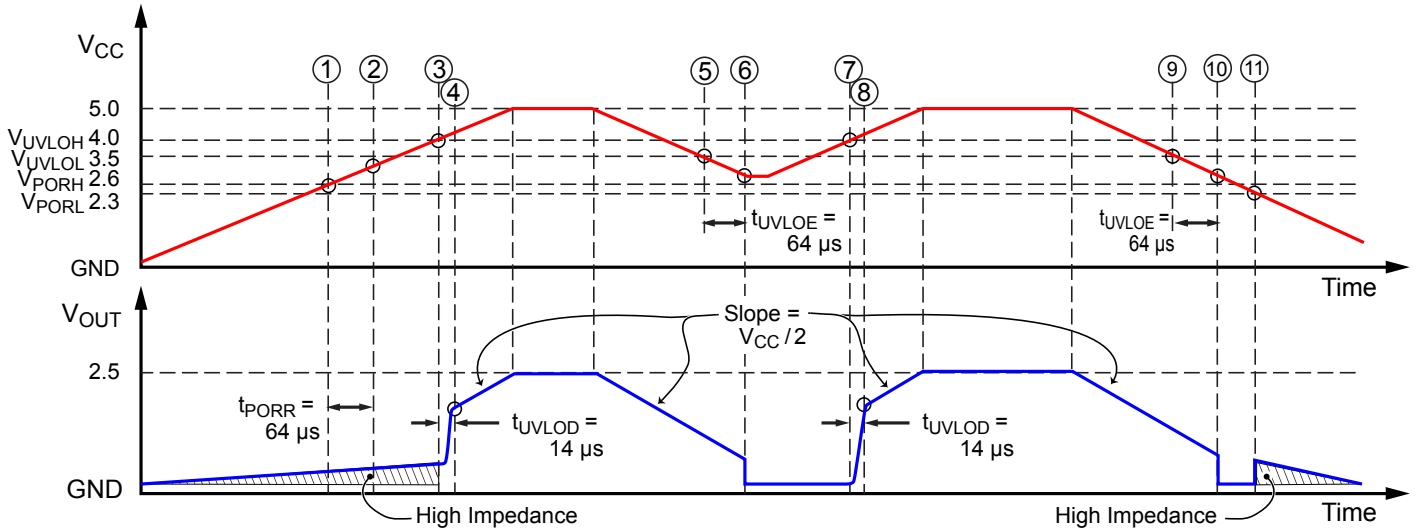


Figure 4: POR and UVLO Operation: Slow Rise Time case

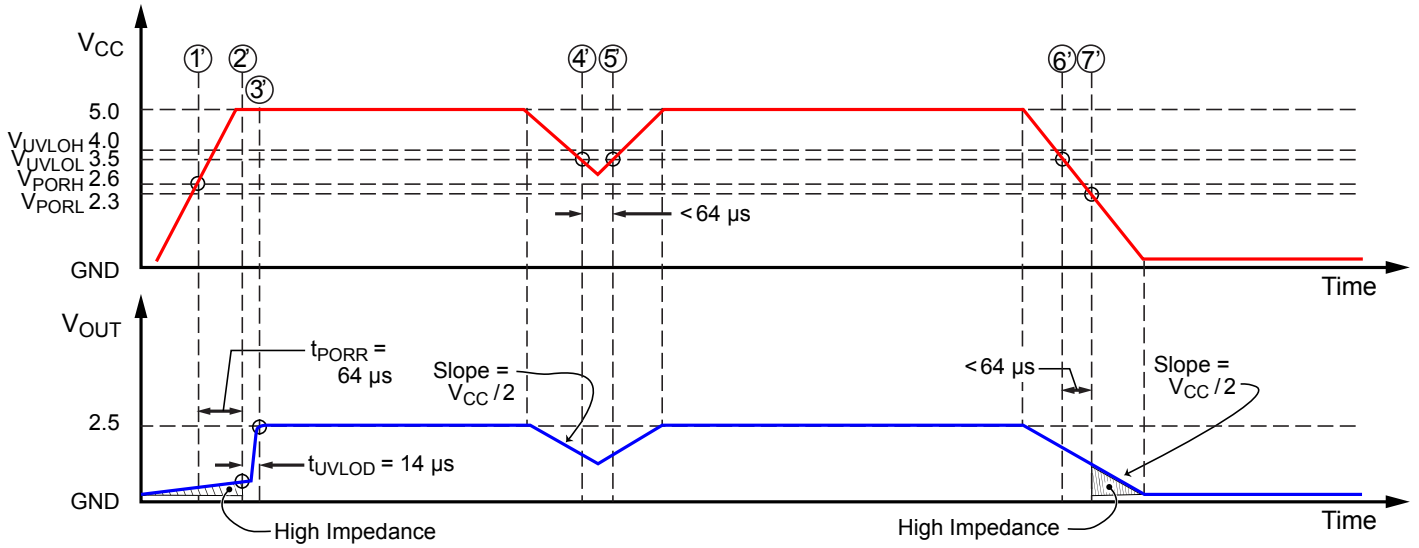


Figure 5: POR and UVLO Operation: Fast Rise Time case

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Detecting Broken Ground Wire

If the GND pin is disconnected, node A becoming open (Figure 6), the VOUT pin will go to a high impedance state. Output voltage will go to $V_{BRK(HIGH)}$ if a load resistor $R_{L(PULLUP)}$ is connected to V_{CC} or to $V_{BRK(LOW)}$ if a load resistor $R_{L(PULLDWN)}$ is connected to GND. The device will not respond to any applied magnetic field.

If the ground wire is reconnected, A1366 will resume normal operation.

EEPROM Error Checking And Correction

Hamming code methodology is implemented for EEPROM checking and correction. The device has ECC enabled after power-up. If an uncorrectable error has occurred, the VOUT pin will go to high impedance and the device will not respond to applied magnetic field.

Output voltage will go to $V_{BRK(HIGH)}$ if a load resistor $R_{L(PULLUP)}$ is connected to V_{CC} or to $V_{BRK(LOW)}$ if a load resistor $R_{L(PULLDOWN)}$ is connected to GND.

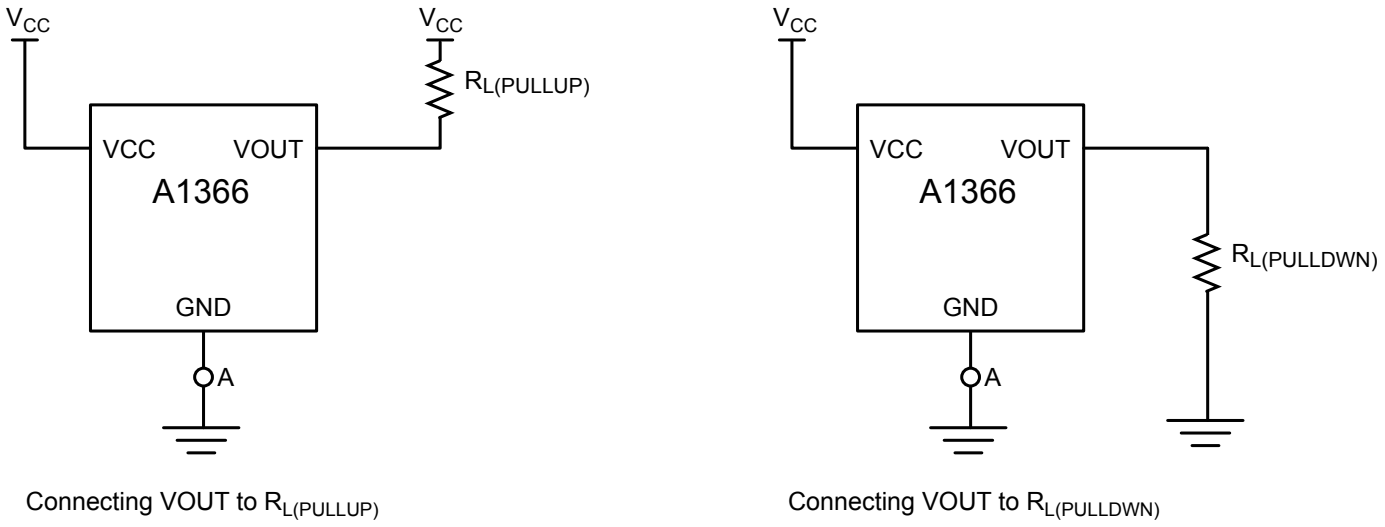


Figure 6: Connections for Detecting Broken Ground Wire

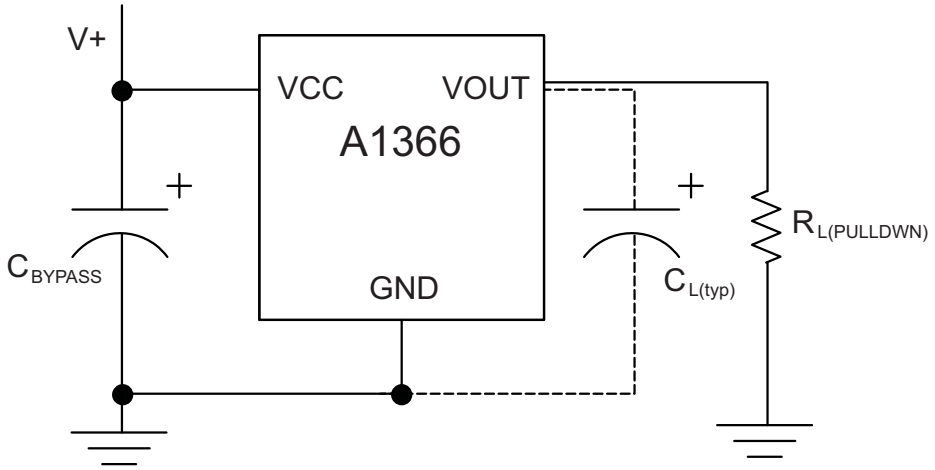


Figure 7: Typical Application Drawing

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Chopper Stabilization Technique

When using Hall-effect technology, a limiting factor for total accuracy is the small signal voltage developed across the Hall element. This voltage is disproportionally small relative to the offset that can be produced at the output of the Hall sensor. This makes it difficult to process the signal while maintaining an accurate, reliable output over the specified operating temperature and voltage ranges. Chopper stabilization is a unique approach used to minimize Hall offset on the chip.

The Allegro technique removes key sources of the output drift induced by thermal and mechanical stresses. This offset reduction technique is based on a signal modulation-demodulation process. The undesired offset signal is separated from the magnetic field-induced signal in the frequency domain, through modulation. The subsequent demodulation acts as a modulation process for the offset, causing the magnetic field-induced signal to recover its original spectrum at base band, while the DC offset becomes a high-frequency signal. The magnetic-sourced signal then can pass through a low-pass filter, while the modulated DC offset is suppressed. This high-frequency operation allows a greater sampling rate, which results in higher accuracy and faster signal-processing capability. This approach desensitizes the chip to the effects of thermal and mechanical stresses and produces devices that have extremely stable quiescent Hall output voltages and precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process, which allows the use of low-offset, low-noise amplifiers in combination with high-density logic integration and a proprietary, dynamic notch filter. The new Allegro filtering techniques are far more effective at suppressing chopper induced signal noise compared to the previous generation of Allegro chopper stabilized devices.

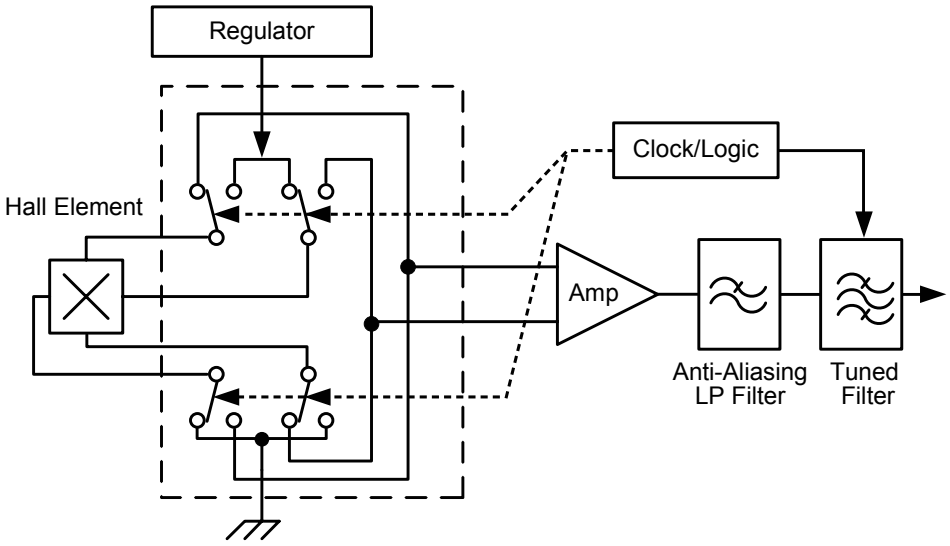


Figure 8: Concept of Chopper Stabilization

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PACKAGE OUTLINE DRAWING

For Reference Only - Not for Tooling Use

(Reference Allegro DWG-0000426, Rev. 2)
Dimensions in millimeters - NOT TO SCALE
Dimensions exclusive of mold flash, gate burs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

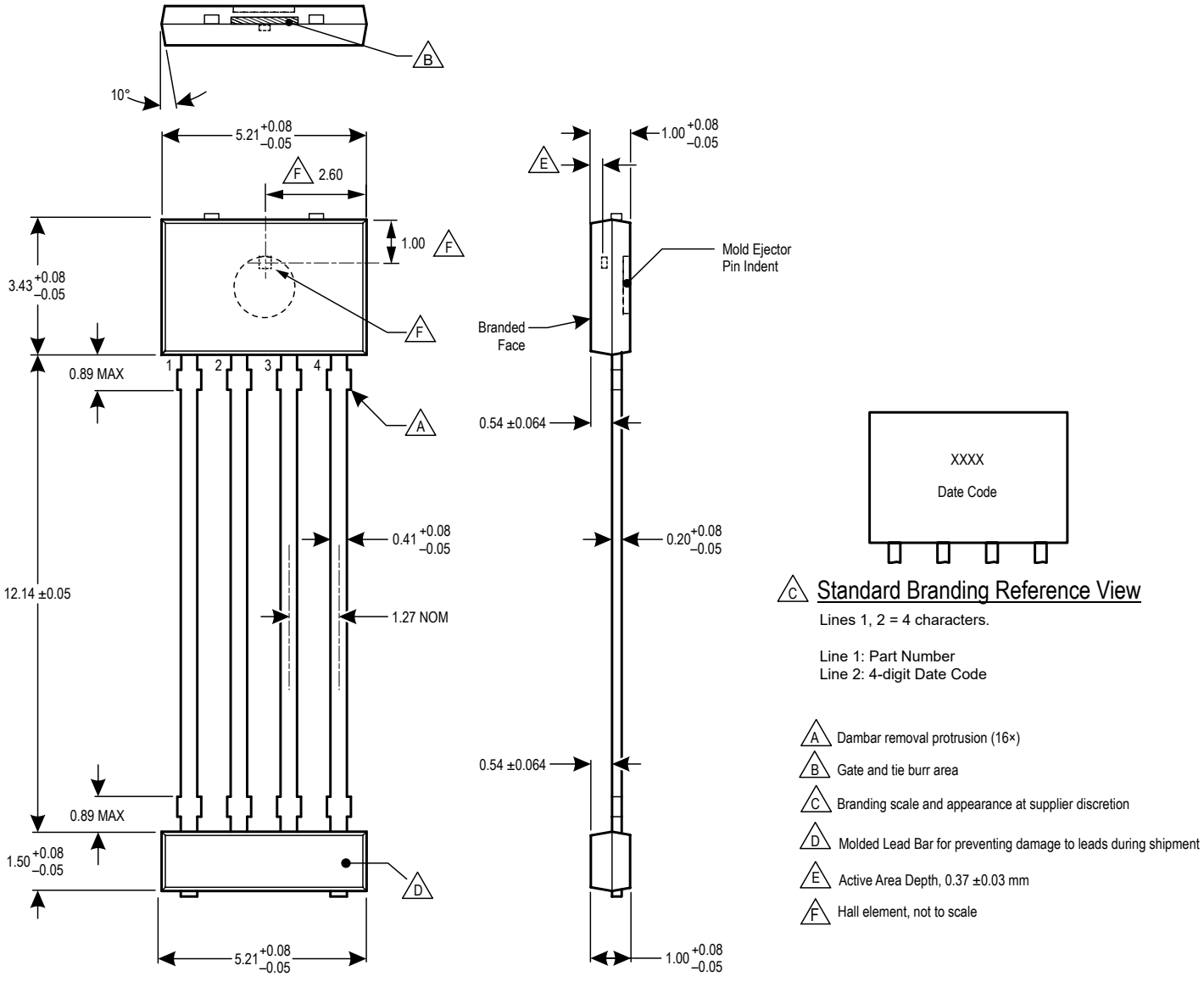
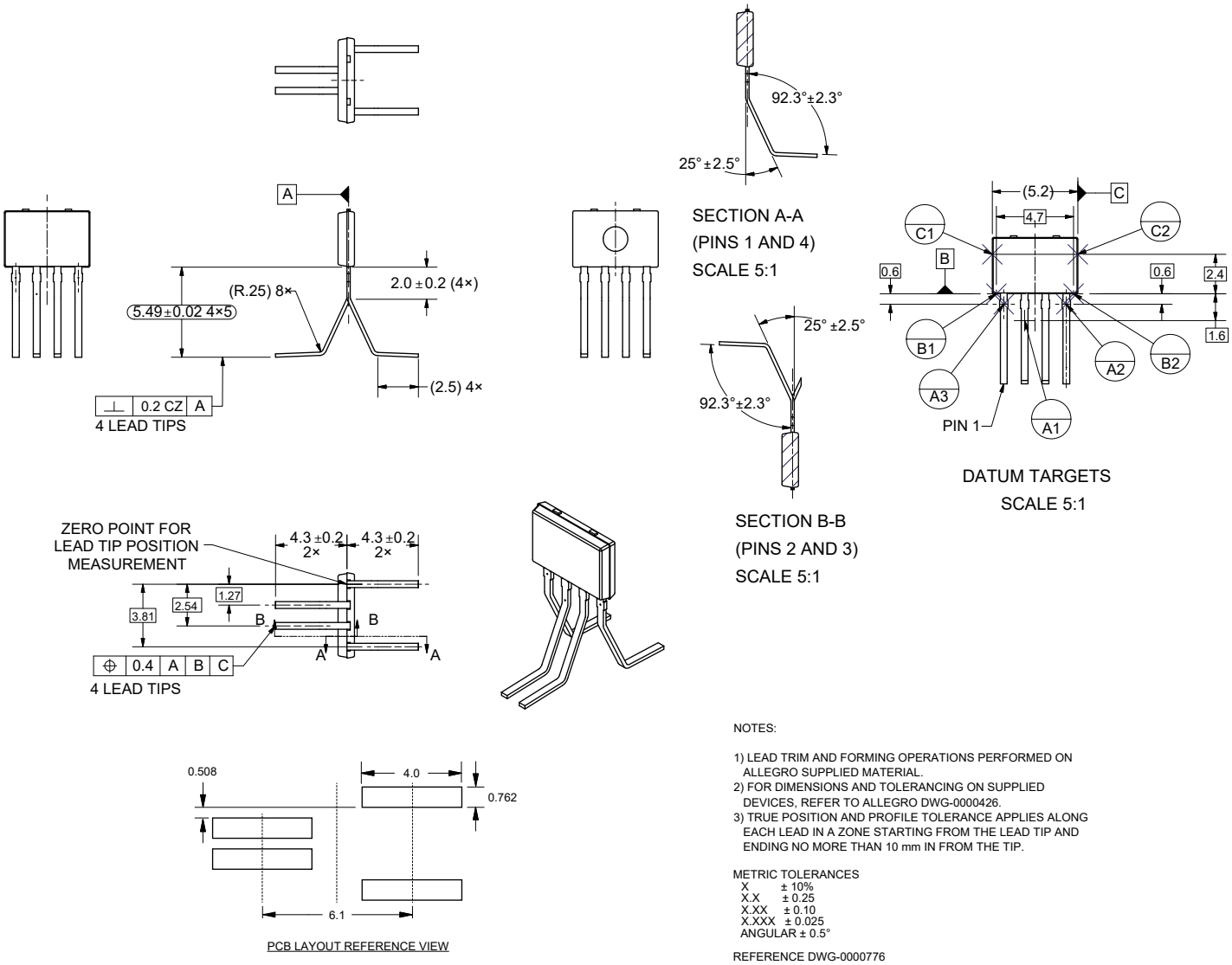


Figure 9: Package KT, 4-Pin SIP, TN Leadform

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NOTES:

1) LEAD TRIM AND FORMING OPERATIONS PERFORMED ON ALLEGRO SUPPLIED MATERIAL.
2) FOR DIMENSIONS AND TOLERANCING ON SUPPLIED DEVICES, REFER TO ALLEGRO DWG-0000426.
3) TRUE POSITION AND PROFILE TOLERANCE APPLIES ALONG EACH LEAD IN A ZONE STARTING FROM THE LEAD TIP AND ENDING NO MORE THAN 10 mm IN FROM THE TIP.

METRIC TOLERANCES
X ± 10%
X.X ± 0.25
X.XX ± 0.10
X.XXX ± 0.025
ANGULAR ± 0.5°

REFERENCE DWG-0000776

Figure 10: Package KT, 4-Pin SIP, TH Leadform

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REVISION HISTORY

Number	Date	Description
–	May 1, 2014	Initial release
1	January 30, 2018	Added EEPROM Error Checking and Correction section (page 18)
2	January 28, 2019	Minor editorial updates
3	March 18, 2019	Added TF and TG leadforms
4	April 26, 2019	Added TF and TG footprints
5	September 30, 2020	Removed TF/TG leadforms and footprints (pages 1-2, 21-22); added TH leadform and footprint (pages 1, 21); updated package outline drawing (page 20)
6	January 25, 2022	Updated package drawing (page 20)
7	March 11, 2024	Part variants A1366LKTTN-5-T and A1366LKTTN-10-T status changed to Last-Time Buy (page 2).

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