A33002

Precision Angle Sensor IC with On-Chip Linearization, SENT, SPI, and PWM Output

FEATURES AND BENEFITS

- Contactless 0° to 360° angle sensor IC for angular position, rotational speed, and direction measurement
  - Capable of sensing magnet rotational speeds targeting 12-bit effective resolution with 900 G field
  - Circular vertical Hall (CVH) technology provides a single-channel sensor system with air-gap independence
- On-chip 32-segment linearization to improve angle accuracy
  - Reduces the impact of magnet-to-sensor misalignment
  - Reduces the impact of imperfect magnetization of target magnet
- ASIL-Compliant: ASIL B safety element out-of-context (SEooC) developed in accordance with ISO 26262, when used as specified in the safety manual:
  - Single-die version designed to meet ASIL B requirements when integrated and used in conjunction with the appropriate system-level control, in the manner prescribed in the A33002 Safety Manual
  - Dual-die version designed to meet ASIL D requirements when integrated and used in conjunction with the appropriate system-level control, in the manner prescribed in the A33002 Safety Manual

ISO 26262 ASIL Compliant

Continued on next page...

DESCRIPTION

The A33002 is a 360° angle sensor IC that provides contactless high-resolution angular position data based on magnetic circular vertical Hall (CVH) technology. It has a system-on-chip (SoC) architecture that includes: a CVH front end, digital signal processing to calculate the angular position data, and selectable output protocols (SPI, SENT, or PWM). It also includes on-chip EEPROM technology capable of supporting up to 100 read/write cycles for flexible programming of calibration parameters. The A33002 is ideal for automotive applications requiring 0° to 360° angle measurements, such as electronic power steering (EPS), transmission actuators, and BLDC pumps.

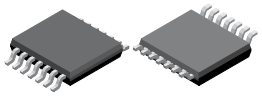
The A33002 includes on-chip 32-segment linearization. This can be used to calibrate out errors due to misalignment between the magnet and the sensor or imperfect magnetization of the target magnet (which can present itself as a misalignment of the magnet to the sensor).

The A33002 supports customer integration into safety-critical applications. This Allegro IC can support ASIL B fail-operational systems when properly integrated, though judgment of the achievement of safety is dependent on the customer's implementation and analyses.

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PACKAGE:

14-pin TSSOP
(Suffix LE)



Not to scale

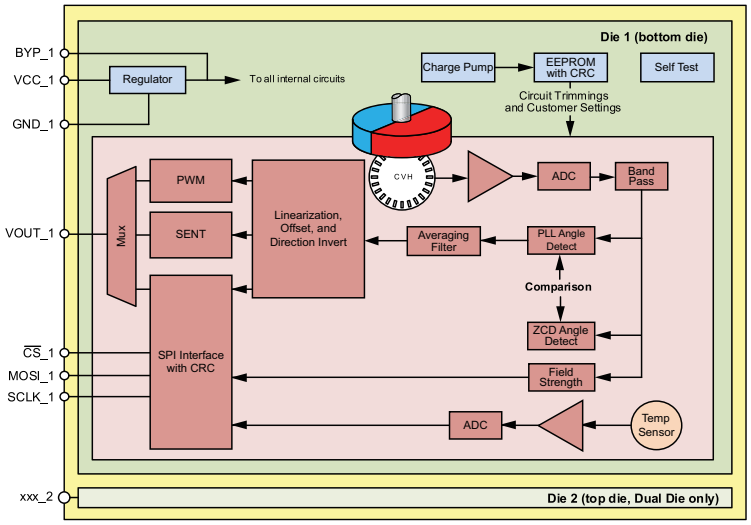


Figure 1: A33002 Magnetic Circuit and IC Diagram

FEATURES AND BENEFITS (continued)

- Digital output format selectable between SPI, SENT, or PWM
- Programmable via Manchester encoding on the V_{CC} line (user to device) and VOUT line (device to user), reducing external wiring
- SENT output is SAE J2716 JAN2010-compliant with Allegro proprietary enhancements
  - Customer-programmable SENT tick times ranging from 0.5 to 7.9 µs
- On-chip EEPROM for storing factory and customer calibration parameters
  - Integrated charge pump allows in-application programming without any requirement for high voltages to be supplied to the device during programming
  - Single-bit error correction, dual-bit error detection error correction control (ECC)
- Supports operation in harsh conditions required for automotive and industrial applications
  - Operating temperature range from –40°C to 150°C
  - Operating supply voltage range from 3.7 to 5.5 V, absolute maximum of 28 V
- Loss of power is indicated by a reset flag
- 10 MHz SPI for low-latency angle and diagnostic data; enables multiple independent ICs to be connected to the same bus
  - 4-bit CRC
- Multiple programming/configuration formats supported
  - The system can be completely controlled and programmed over SPI or Manchester protocol, including EEPROM writes
  - For system with limited pins available, writing and reading can be performed over VCC and VOUT pins.
  - 1 mm-thin, surface-mount TSSOP package to minimize air gap from target magnet to the CVH transducer for improved field strength

DESCRIPTION (continued)

The A33002 is available in a single-die or dual-die 14-pin TSSOP package (suffix LE). The package is lead (Pb) free with 100% matte tin leadframe plating. The 1 mm-thin package reduces the minimum air gap between the CVH transducer and the target magnet.

SELECTION GUIDE

Part Number	System Die	Interface Voltage	Package	Packing
A33002LLEATR	Single	3.3 V	14-pin TSSOP	4000 pieces per 13-inch reel
A33002LLEBTR-DD	Dual	3.3 V		
A33002LLEATR-5	Single	5.0 V		

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{CC}	Not sampling angles, respecting T_J(max)	28	V
Reverse Supply Voltage	V_{RCC}	Not sampling angles	–18	V
All Other Pins Forward Voltage	V_{IN}		5.5	V
All Other Pins Reverse Voltage	V_R		–0.5	V
Operating Ambient Temperature	T_A	L range	–40 to 150	°C
Maximum Junction Temperature	T_J(max)		165	°C
Storage Temperature	T_{stg}		–65 to 170	°C

THERMAL CHARACTERISTICS: May require derating at maximum conditions

Characteristic	Symbol	Test Conditions [1]	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	LE-14 package; measured on JEDEC JESD51-7 2s2p board	82	°C/W

[1] Additional thermal information is available on the Allegro website.

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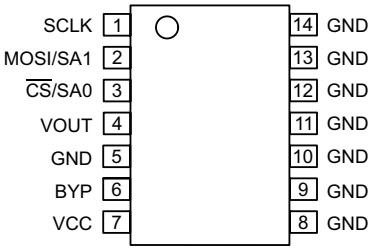
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PINOUT DIAGRAMS AND TERMINAL LIST TABLES

PINOUT DIAGRAM

LE 14-Pin TSSOP, Single Die

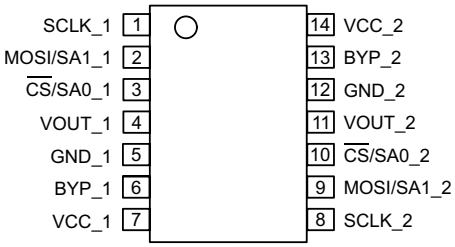


Terminal List Table, Single Die

Pin Name	Pin Number	Function
SCLK	1	SPI: Clock input terminal.
MOSI/SA1	2	SPI: Controller-Out/Peripheral-In. Die ID select: Sets bit 1 of address field. Tie to BYP for a logic 1, GND for a logic 0.
$\overline{CS}$/SA0	3	SPI chip select terminal, active low input. Die ID select: Sets bit 0 of address field. Tie to BYP for a logic 1, GND for a logic 0.
VOUT	4	SPI: Controller-In/Peripheral-Out, push-pull SENT/PWM/Manchester: Input / Output, open drain.
GND	5, 8-14	Device ground terminal. All GND pins should be connected together.
BYP	6	External bypass capacitor terminal for internal regulator.
VCC	7	Power supply.

PINOUT DIAGRAM

LE 14-Pin TSSOP, Dual Die



Terminal List Table, Dual Die

Pin Name	Pin Number	Function
SCLK_1	1	SPI: Clock input terminal. (Die 1)
MOSI/SA1_1	2	SPI: Controller-Out/Peripheral-In. Die ID select: Sets bit 1 of address field. Tie to BYP for a logic 1, GND for a logic 0. (Die 1)
$\overline{CS}$/SA0_1	3	SPI chip select terminal, active low input. Die ID select: Sets bit 0 of address field. Tie to BYP for a logic 1, GND for a logic 0. (Die 1)
VOUT_1	4	SPI: Controller-In/Peripheral-Out, push-pull. SENT/PWM/Manchester: Input / Output, open drain. (Die 1)
GND_1	5	Device ground terminal. (Die 1)
BYP_1	6	External bypass capacitor terminal for internal regulator. (Die 1)
VCC_1	7	Power supply. (Die 1)
SCLK_2	8	SPI: Clock input terminal. (Die 2)
MOSI/SA1_2	9	SPI: Controller-Out/Peripheral-In. Die ID select: Sets bit 1 of address field. Tie to BYP for a logic 1, GND for a logic 0. (Die 2)
$\overline{CS}$/SA0_2	10	SPI chip select terminal, active low input. Die ID select: Sets bit 0 of address field. Tie to BYP for a logic 1, GND for a logic 0. (Die 2)
VOUT_2	11	SPI: Controller-In/Peripheral-Out, push-pull. SENT/PWM/Manchester: Input / Output, open drain. (Die 2)
GND_2	12	Device ground terminal. (Die 2)
BYP_2	13	External bypass capacitor terminal for internal regulator. (Die 2)
VCC_2	14	Power supply. (Die 2)

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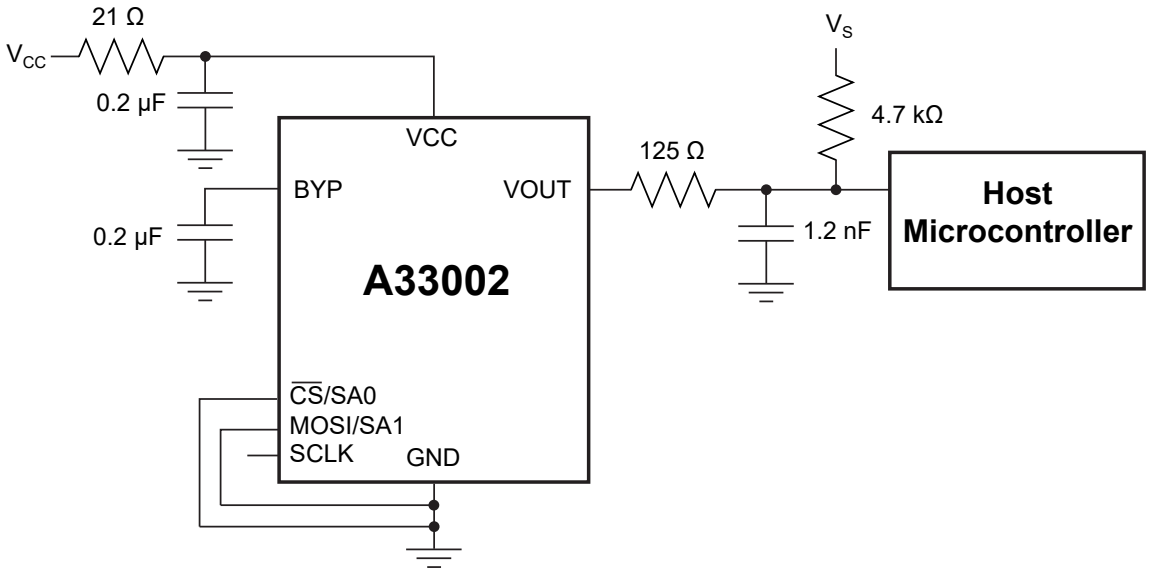


Figure 2: A33002 Reference Design for Stringent EMC Requirements

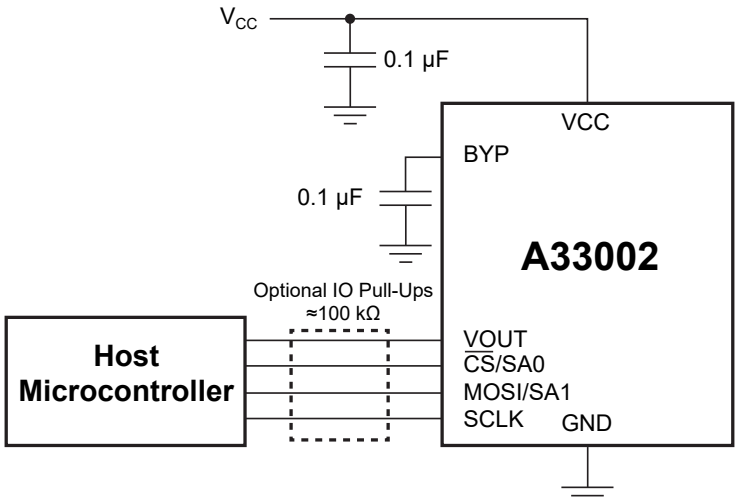


Figure 3: A33002 Typical Setup

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OPERATING CHARACTERISTICS: Valid over the full operating voltage and ambient temperature ranges, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit [1]
ELECTRICAL CHARACTERISTICS						
Supply Voltage	V_{CC}	Customer supply	3.7	–	5.5	V
Supply Current	I_{CC}	Each die	11	13	16	mA
Undervoltage Flag Threshold	V_{UVD}	dV/dt = 1 V/ms, A33002 sampling enabled	3.7	–	3.9	V
Supply Zener Clamp Voltage	V_{ZSUP}	$I_{CC} = I_{CC(max)} + 3$ mA	26.5	–	–	V
Reverse Battery Current	I_{RCC}	$V_{RCC} = –18$ V, $T_A = 25°C$	–	–	–5	mA
Power-On Time [2]	t_{PO}	Power-on diagnostics disabled	–	15	–	ms
Bypass Pin Output Voltage [3]	V_{BYP}	$T_A = 25°C$, $C_{BYP} = 0.1$ µF, 3.3 V interface	2.93	3.3	3.63	V
		$T_A = 25°C$, $C_{BYP} = 0.1$ µF, 5.0 V interface, $V_{CC} = 5$ V	4	–	5.5	V
SPI INTERFACE SPECIFICATIONS (for 3.3 V interface)						
Digital Input High Voltage	V_{IH}	MOSI, SCLK, $\overline{CS}$ pins	2.8	–	3.63	V
Digital Input Low Voltage	V_{IL}	MOSI, SCLK, $\overline{CS}$ pins	–	–	0.5	V
SPI Output High Voltage	V_{OH}	VOUT, $C_L = 20$ pF, $T_A = 25°C$, 5 V compliant	2.93	3.3	3.63	V
SPI Output Low Voltage	V_{OL}	VOUT, $C_L = 20$ pF	–	0.3	–	V
SPI INTERFACE SPECIFICATIONS (for 5.0 V interface)						
Digital Input High Voltage	V_{IH}	MOSI, SCLK, $\overline{CS}$ pins	3.75	–	5.5	V
Digital Input Low Voltage	V_{IL}	MOSI, SCLK, $\overline{CS}$ pins	–	–	0.5	V
SPI Output High Voltage	V_{OH}	VOUT, $C_L = 20$ pF, $T_A = 25°C$, 5 V compliant, V_{BYP} is in valid range, $V_{CC} \geq 5.0$ V	4	5	–	V
SPI Output Low Voltage	V_{OL}	VOUT, $C_L = 20$ pF	–	0.3	–	V
SPI INTERFACE SPECIFICATIONS						
SPI Clock Frequency [4]	f_{SCLK}	VOUT, $C_L = 20$ pF	0.1	–	10	MHz
SPI Clock Duty Cycle [4]	D_{fSCLK}	SPI_{CLKDC}	40	-	60	%
SPI Frame Rate [4]	t_{SPI}		5.8	–	588	kHz
Chip Select to First SCLK Edge [4]	t_{CS}	Time from $\overline{CS}$ going low to SCLK falling edge	50	–	–	ns
Chip Select Idle Time [4]	t_{CS_IDLE}	Time $\overline{CS}$ must be high between SPI message frames	200	–	–	ns
Data Output Valid Time [4]	t_{DAV}	Data output valid after SCLK falling edge	–	–	50	ns
MOSI Setup Time [4]	t_{SU}	Input setup time before SCLK rising edge	25	–	–	ns
MOSI Hold Time [4]	t_{HD}	Input hold time after SCLK rising edge	50	–	–	ns
SCLK to CS Hold Time [4]	t_{CHD}	Hold SCLK high time before $\overline{CS}$ rising edge	5	–	–	ns
Load Capacitance [4]	C_L	Loading on digital output (VOUT) pin	–	–	20	pF

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OPERATING CHARACTERISTICS (continued): Valid over the full operating voltage and ambient temperature ranges, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit [1]
MANCHESTER INTERFACE SPECIFICATIONS						
Bit Rate		Defined by the input message bit rate sent from the external controller	4	–	40	kbps
Bit Time	t_{BIT}	Data bit pulse width at 4 kbps	243	250	257	µs
		Data bit pulse width at 100 kbps	9.5	10	10.5	µs
Bit Time Error	err_{TBIT}	Deviation in t_{BIT} during one command frame	–11	–	+11	%
Read Delay	t_{START_READ}	Delay from trailing edge of a Read command frame to leading edge of Read Acknowledge frame	¼ × t_{BIT}	–	¾ × t_{BIT}	µs
INPUT SIGNAL VOLTAGE						
Manchester Code High Voltage	$V_{MAN(H)}$	Applied to V_{CC} line	7.8	–	–	V
Manchester Code Low Voltage	$V_{MAN(L)}$	Applied to V_{CC} line	–	–	5.4	V
OUTPUT SIGNAL VOLTAGE						
Manchester Code High Voltage	$V_{MAN(H)}$	Minimum R_{PULLUP} = 5 kΩ	0.9 × V_S	–	–	V
		Maximum R_{PULLUP} = 50 kΩ	0.7 × V_S	–	–	V
Manchester Code Low Voltage	$V_{MAN(L)}$	5 kΩ < R_{PULLUP} < 50 kΩ	–	–	0.1	V
PWM INTERFACE SPECIFICATIONS						
PWM Carrier Frequency [4]	f_{PWM}	PWM Frequency Min Setting, T_A in specification	–	98	–	Hz
		PWM Programmable Options (number of steps)	–	128	–	steps
		PWM Frequency Max Setting, T_A in specification	–	3.125	–	kHz
PWM Output Low Clamp	$D_{PWM(min)}$	Corresponding to digital angle of 0x000	–	5	–	%
PWM Output High Clamp	$D_{PWM(max)}$	Corresponding to digital angle of 0xFFF	–	95	–	%
PWM Output Resolution	RES_{PWM}		–	12	–	bit
PWM Output Saturation Voltage	$V_{SAT_LOW(PWM)}$	Output current = –1mA, V_{CC} = 5 V, output FET on	–	–	0.25	V
PWM Current Limit	$I_{LIMIT(PWM)}$	Output FET on, T_A = 25°C	13	18	25	mA
PWM Output Impedance [4]	$R_{ON(PWM)}$	PWM driver impedance when pulling to logic low; T_A = 25°C	10	–	250	Ω
SENT SPECIFICATIONS [4]						
SENT Tick Time	t_{TICK}	All SENT Modes [5]	0.5	–	7.9375	µs
SENT Tick Time Tolerance	TOL_{tTICK}	All SENT Modes	–15	–	15	%
SENT Output Trigger Thresholds	$V_{SENTtrig(L)}$	V_{OUT} falling, 3.3 V digital	–	–	1.2	V
	$V_{SENTtrig(H)}$	V_{OUT} rising, 3.3 V digital	2.3	–	–	V
	$V_{SENTtrig(L)}$	V_{OUT} falling, 5.0 V digital	–	–	1.8	V
	$V_{SENTtrig(H)}$	V_{OUT} rising, 5.0 V digital	3.6	–	–	V
SENT Output Saturation Voltage	$V_{SAT_LOW(SENT)}$	Output current = –4.7 mA, V_{CC} = 5 V, output FET on	–	–	0.45	V
SENT Output Current Limit	$I_{LIMIT(SENT)}$	Output FET on, T_A = 25°C	10	20	35	mA
SENT Output Load Resistance	$R_{L(PULLUP)}$	Output current ≥ –10 mA	1.2	–	–	kΩ
Trigger Delay Time [6]	t_{dSENT}	From end of trigger pulse to beginning of SENT message frame (TSENT and Shared SENT)	7	–	–	ticks
SENT Output Impedance [4]	$R_{ON(SENT)}$	SENT driver impedance when pulling to logic low; T_A = 25°C	30	47	95	Ω

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OPERATING CHARACTERISTICS (continued): Valid over the full operating voltage and ambient temperature ranges, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit [1]
BUILT-IN SELF TEST						
Logic BIST Time	t_{LBIST}	Configurable to run on power-up or on user request	–	30	–	ms
Circular Vertical Hall Self-Test Time	t_{CVHST}	Configurable to run on power-up or on user request	–	52	–	ms
MAGNETIC CHARACTERISTICS						
Magnetic Field	B	Range of input field	–	–	900	G
ANGLE CHARACTERISTICS						
Output [7]	RES_{ANGLE}	Both 12- and 15-bit angle values are available via SPI	–	12/15	–	bit
Angle Refresh Rate [8]	t_{ANG}	No averaging	–	2.0	–	µs
Response Time [4]	$t_{RESPONSE}$	Angular latency	–	17	–	µs
Angle Error	ERR_{ANG}	T_A = 25°C, ideal magnet alignment, B = 300 G, target rpm = 0	–1.2	±0.4	1.2	degrees
		T_A = 150°C, ideal magnet alignment, B = 300 G, target rpm = 0	–1.5	±0.5	1.5	degrees
		T_A = –40°C, ideal magnet alignment, B = 300 G, target rpm = 0	–	±0.6	–	degrees
Temperature Drift	$ANGLE_{DRIFT}$	T_A = 150°C, B = 300 G	–1.75	–	1.75	degrees
		T_A = –40°C, B = 300 G	–	±1	–	degrees
Angle Noise [9][10]	N_{ANG}	T_A = 25°C, B = 300 G, no internal filtering, target rpm = 0, 3 sigma noise	–	±0.19	–	degrees
		T_A = 150°C, no internal filtering, B = 300 G, target rpm = 0, 3 sigma noise	–	±0.25	–	degrees
Effective Resolution [11]		B = 300 G, T_A = 25°C	–	12.5	–	bits
Angle Drift Over Lifetime [12]	$ANGLE_{Drift_Life}$	B = 300 G, average maximum drift observed following AEC-Q100 qualification testing	–	0.5	–	degrees

[1] 1 G (gauss) = 0.1 mT (millitesla).
[2] During the power-on phase, the A33002 SPI transactions are valid within ≈ 300 µs of power on (with no self-tests). Angle reading requires full t_{PO} to stabilize.
[3] The output voltage specification is to aid in PCB design. The pin is not intended to drive any external circuitry. The specifications indicate the peak capacitor charging and discharging currents to be expected during typical operation.
[4] Parameter is not guaranteed at final test. Determined by design.
[5] Tick times under 0.5 µs are available, but not guaranteed.
[6] The synchronization pulse delay is a minimum of 7 ticks but can be extended to include slot marking in SSENT.
[7] RES_{ANGLE} represents the number of bits of data available for reading from the die registers.
[8] The rate at which a new angle reading becomes ready.
[9] Error and noise values are with no further signal processing. Angle noise can be reduced with internal filtering and slower angle refresh rate value.
[10] This value represents 3-sigma or three times the standard deviation of the measured samples.
[11] Effective resolution is calculated using:

$$log_2(360) - log_2\left(\sqrt{\sum_{I=1}^{n}\sigma_I}\right)$$

where σ is the standard deviation based on 30 measurements taken at each of the 32 angular positions, I = 11.25, 22.5, … 360.
[12] Maximum observed angle drift following AEC-Q100 stress was 1.03 degrees.

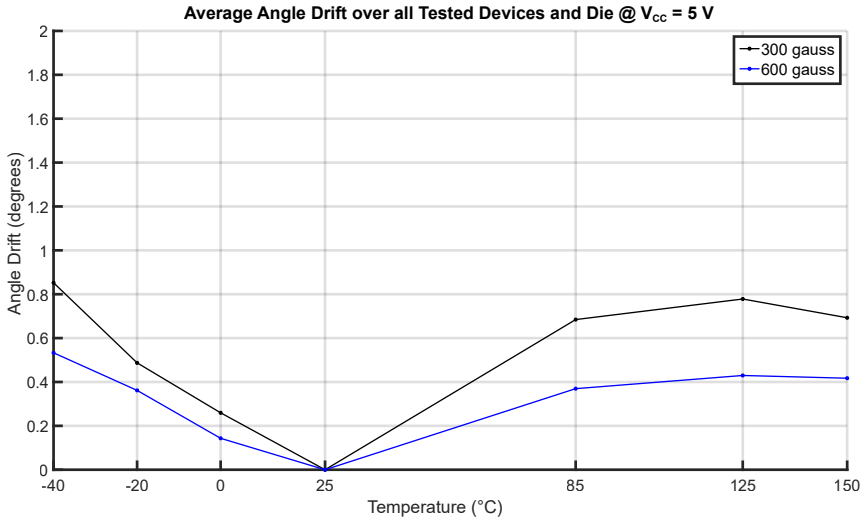
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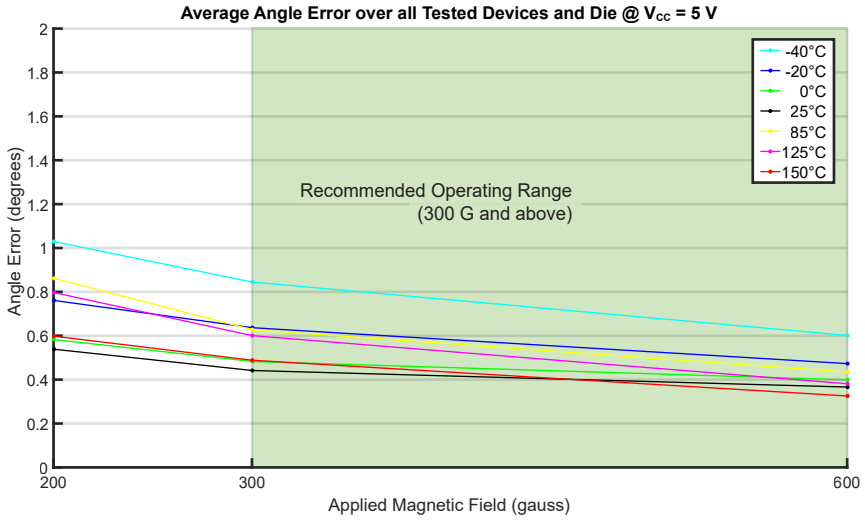
TYPICAL PERFORMANCE CHARACTERISTICS

Shown below are performance plots of actual A33002 devices measured over temperature and field strength. The plots provide typical performance expected from A33002 devices. The performance in the plots shown here is not guaranteed. Device performance may vary from these plots. For all absolute specifications, refer to the Operating Characteristics tables.

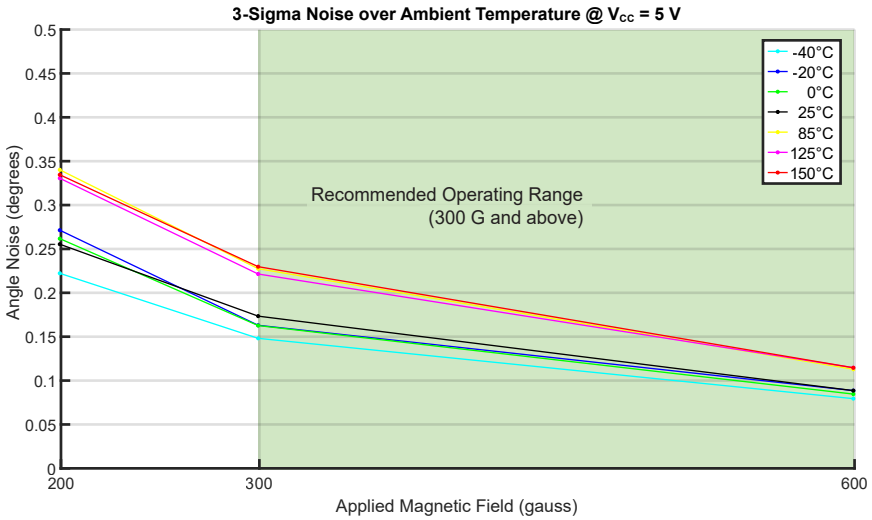
Bench Characterization

The plots shown here are based on data collected from three dual-die devices, for a total of six data sets.



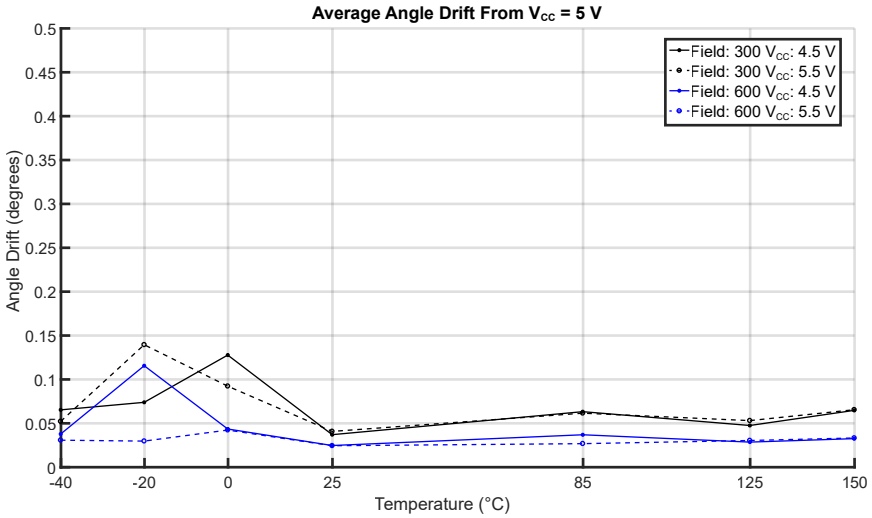


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Angle Variation due to V_{CC}

The plot below shows the maximum deviation in angle from nominal 5 V V_{CC} to 4.5 and 5.5 V.



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FUNCTIONAL DESCRIPTION

Overview

The A33002 is a rotary position Hall-sensor-based device in a surface-mount package, providing solid-state consistency and reliability, and supporting a wide variety of automotive applications. The Hall-sensor-based device measures the direction of the magnetic field vector through 360° in the x-y plane (parallel to the branded face of the device) and computes an angle measurement based on the actual physical reading, as well as any internal parameters that have been set by the user. The output is used by the host microcontroller to provide a single channel of target data.

This device is an advanced, programmable system-on-chip (SoC). The integrated circuit includes a circular vertical Hall (CVH) analog front end, a high-speed sampling analog-to-digital converter, digital filtering, and digital signal processing.

Advanced offset, gain, and linearization adjustment options are available in the A33002. These options can be configured in onboard EEPROM, providing a wide range of sensing solutions in the same device.

Angle Measurement

The A33002 is capable of tracking magnet position at high speed. Performance up to 12,000 rpm has been verified by testing. Operation up to 30,000 rpm has been verified via design simulation. The A33002 has a typical output refresh rate of 2 µs.

Readout in SPI is possible with 12-bit resolution, with error flags included in the same word, or in 15-bit resolution without included error flags. Reading out the angle requires a minimum of 16 SPI clock cycles. A 20-bit SPI packet with 4 bits of CRC is also supported.

PWM output is always resolved to a 12-bit angle value.

When using SENT output, a 12-bit or 16-bit angle packet may be selected via the DATA_MODE field in EEPROM.

The sensor readout is processed and linearized in the steps detailed in Figure 6.

System Level Timing

Internal registers are updated with a new angle value every t_{ANG}. Due to signal path delay, the angle is $t_{RESPONSE}$ old at each update. In other words, $t_{RESPONSE}$ is the delay from time of magnet sampling until generation of a processed angle value. SPI, which is asynchronously clocked, results in a varying latency depending on sampling frequency and SCLK speed. The values presented to the user are latched to the output registers on the first SCLK edge of the SPI output frame. This means that, if the SPI clock is 10 MHz, the data is clocked out after 1.6 µs. Because the data is sampled in at the first clock edge at an age of maximum $t_{RESPONSE}$, its age after the SPI transaction has finished is between 1.6 and 1.6 + $t_{RESPONSE}$ µs.

Similar to SPI, when using the PWM output, the output packet is not synchronized with the internal update rate of the sensor. The angle is latched at the beginning of the carrier frequency period (effectively at the rising edge of the PWM output). Because of this, the age of the angle value, once read by the system microcontroller, may be up to $t_{RESPONSE} + 1/f_{PWM}$.

The point within the SENT packet at which the angle value is latched varies with SENT configurations, although in all configurations, the SENT transmission time is the dominant contributor to delay. For a detailed description, see Appendix A: SENT Output Description.

Power-Up

Upon applying power to the A33002, the device automatically runs through an initialization routine. The purpose of this initialization is to ensure that the device comes up in the same predictable operating condition every power cycle. This initialization routine takes time to complete, which is referred to as power-on time, t_{PO}. Regardless of the state of the device before a power cycle, the device repowers with EEPROM shadow bits copied from the EEPROM anew, and serial registers in their default states. For example, on every power-up, the device powers with the ZERO_OFFSET that was stored in the EEPROM. The extended write access field WRITE_ADR is set back to its default value of zero.

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PWM Output

The A33002 provides a pulse-width-modulated open-drain output, with the duty cycle (DC) proportional to measured angle. The PWM duty cycle is clamped at 5% and 95% for diagnostic purposes. A 5% DC corresponds to 0°; a 95% DC corresponds to 360°.

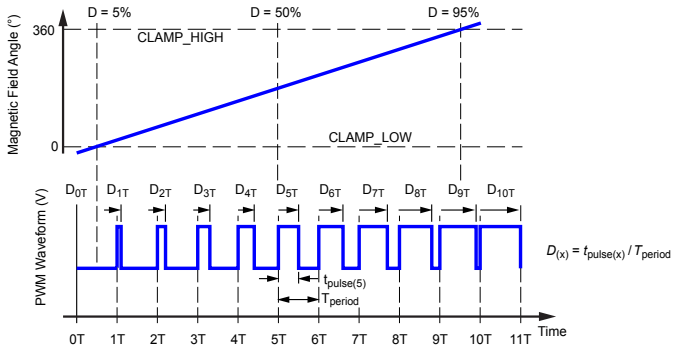


Figure 4: PWM Mode Outputs a Duty Cycle Proportional to Sensed Angle

Within each cycle, the output is high for the first 5% and low for the last 5% of each period. The middle 90% of the period is a linear interpolation of the angle as sampled from the start of the PWM period.

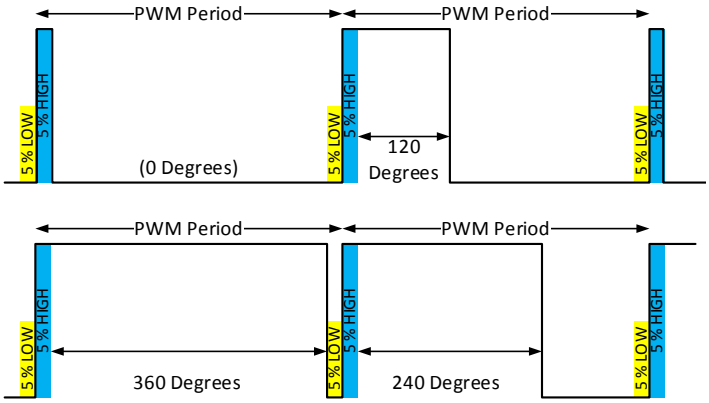


Figure 5: Pulse-Width Modulation (PWM) Examples

The angle is represented in 12-bit resolution and can never reach 360°. The maximum duty cycle high period is:

$$\text{DutyCycleMax (\%)} = (4095 / 4096) \times 90 + 5.$$

PWM CARRIER FREQUENCY

The PWM carrier frequency is controlled via two EEPROM fields, both of which are found in the PWS row.

- PWM_FREQ
- PWM_BAND

Together, these two fields allow 128 different PWM carrier frequencies to be selected.

Table 1: PWM Carrier Frequencies in Hz

		PWM_BAND							
		0	1	2	3	4	5	6	7
PWM_FREQ	0	3125	2778	2273	1667	1087	641	352	185
	1	3101	2740	2222	1613	1042	610	333	175
	2	3077	2703	2174	1563	1000	581	316	166
	3	3053	2667	2128	1515	962	556	301	157
	4	3030	2632	2083	1471	926	532	287	150
	5	3008	2597	2041	1429	893	510	275	143
	6	2985	2564	2000	1389	862	490	263	137
	7	2963	2532	1961	1351	833	472	253	131
	8	2941	2500	1923	1316	806	455	243	126
	9	2920	2469	1887	1282	781	439	234	121
	10	2899	2439	1852	1250	758	424	225	116
	11	2878	2410	1818	1220	735	410	217	112
	12	2857	2381	1786	1190	714	397	210	108
	13	2837	2353	1754	1163	694	385	203	105
	14	2817	2326	1724	1136	676	373	197	101
	15	2797	2299	1695	1111	658	362	191	98

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ERROR REPORTING IN PWM

The PWM output can be configured to change state if certain errors occur. There are three options:

- No error reporting
- Tristate the PWM
- Halve the carrier frequency and represent the error via different duty cycles

Two EEPROM bits, PEO and PES, control how errors are reported in PWM mode, both of which are in the PWS address row of EEPROM:

Table 2: PWM Error Output Enable Option (PEO)

Code	Description
0	PWM does not respond to errors.
1	PWM output responds to errors as selected with the PES field.

Table 3: PWM Error Select (PES)

Code	Description
0	PWM tristates on an error.
1	PWM carrier frequency halved and highest priority error output on PWM as selected duty cycle.

The error priority and corresponding duty cycle are shown in Table 4, with the high-priority error dictating the PWM duty cycle.

Each error may be individually masked within EEPROM to prevent losing PWM output for an event of no concern. These mask bits may be found within the PWE (0x18) EEPROM row.

Table 4: PWM Error Duty Cycle and Priority

Error	Priority	Duty Cycle %	Description / Persistence
WDE	1 (highest)	5	Watchdog error. Permanent.
EUE	2	10.625	EEPROM uncorrectable error. Permanent.
STF	3	16.25	Self-test failure. Permanent.
PLK	4	21.875	PLL not locked. Persists until PLL locks.
ZIE	5	27.5	Zero-crossing integrity error. Persists until goes away.
AVG	6	33.125	Angle averaging error. Outputs once then clears.
UV	7	38.75	Undervoltage (UVA and/or UVCC dependent on serial error masks). Persists until no unmasked undervoltage.
MSL	8	44.375	Persists until field strength higher than low threshold.
ESE	9	50	EEPROM correctable error. Outputs once then clears.
SAT	10	55.625	Persists until no saturation warnings.
MSH	11	61.25	Persists until field strength lower than high threshold.
TR	12	66.875	Persists until temperature within range.
TOV	13	72.5	Persists until cleared via the serial CTRL register.

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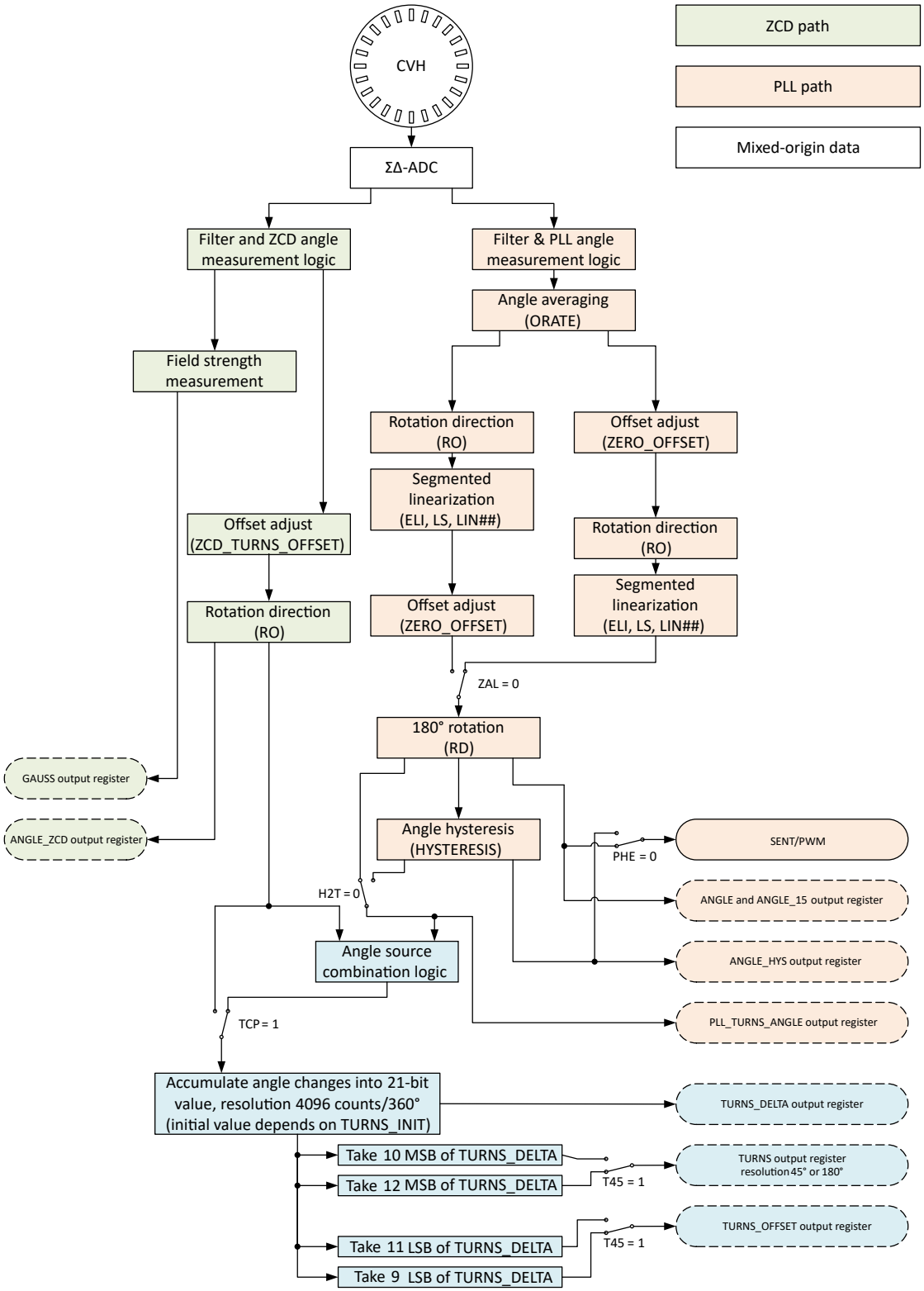


Figure 6: Angle Measurement – Sensor Readout Steps

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Linearization

The A33002 contains linearization functionality. Linearization allows for conversion of the initially sensor-measured magnetic field data into customer-desired linear output. This can be used to correct minor imperfections in the encoder signal, or to allow motor commutation in side-shaft measurement setups.

Linearization converts the electrical angles (the angle as measured by the sensor front end) into mechanical angles (the actual angle of the encoder signal).

To use the linearization feature, it is most convenient to use the Allegro A33002 Samples Programmer graphical user interface (GUI). It allows the user to measure points along the mechanical rotation, calculate all parameters that need to be written into the sensor, and write these values into the sensor. To use this function, the user must be able to read and control the mechanical angle.

The sensor performs linearization by taking the measured electrical angles and, depending on the angle measured, subtracting a linearization coefficient stored in EEPROM. There are 32 of these linearization coefficients in the EEPROM. The angle value at a sensor angle reading of 0.00, 11.25, 22.50, … 348.75 electrical degrees are modified by the values in EEPROM fields LIN0, LIN1, LIN2, … LIN31. The EEPROM LIN values are subtracted from the electrical sensor angles, as shown in Table 5.

The LIN fields are 12-bit signed values. Each LIN coefficient has a range of –2048…+2047 LSB that corresponds to a correction of the electrical angle by +22.50…–22.49 degrees (EEPROM field LS = 0) or by +45.00…–44.98 degrees (EEPROM field LS = 1). When the electrical angle is between two of the linearization points, the sensor calculates the appropriate correction value for this angle by linear interpolation between the two coefficients next to the value. For example, if the sensor measures an angle of 5.625°, the output is 5.625 – (LIN0 + LIN1) / 2.

An example of a nonlinear curve that is corrected by the sensor is shown in Figure 7. In this example, the values of LIN0 through LIN4 are positive numbers, while LIN5 and LIN6 are negative numbers. The straight line interpolation between LIN points typically gives rise to some residual error, as the device is fitting a line to a nonlinear error profile. An example of this is shown in Figure 8.

The output delay of the A33002 is not affected by enabling or disabling linearization. If linearization is disabled, the EEPROM LIN fields can be used for other customer purposes.

Table 5: Linearization Coefficients

Electrical angle (°) measured by sensor	Correction value Written in EEPROM	Output angle Visible on sensor output
0.00	LIN0	Output = 0.00 – LIN0
11.25	LIN1	Output = 11.25 – LIN1
22.50	LIN2	Output = 22.50 – LIN2
33.75	LIN3	Output = 33.75 – LIN3
45.00	LIN4	Output = 45.00 – LIN4
56.25	LIN5	Output = 56.25 – LIN5
67.50	LIN6	Output = 67.50 – LIN6
78.75	LIN7	Output = 78.75 – LIN7
90.00	LIN8	Output = 90.00 – LIN8
101.25	LIN9	Output = 101.25 – LIN9
112.50	LIN10	Output = 112.50 – LIN10
123.75	LIN11	Output = 123.75 – LIN11
135.00	LIN12	Output = 135.00 – LIN12
146.25	LIN13	Output = 146.25 – LIN13
157.50	LIN14	Output = 157.50 – LIN14
168.75	LIN15	Output = 168.75 – LIN15
180.00	LIN16	Output = 180.00 – LIN16
191.25	LIN17	Output = 191.25 – LIN17
202.50	LIN18	Output = 202.50 – LIN18
213.75	LIN19	Output = 213.75 – LIN19
225.00	LIN20	Output = 225.00 – LIN20
236.25	LIN21	Output = 236.25 – LIN21
247.50	LIN22	Output = 247.50 – LIN22
258.75	LIN23	Output = 258.75 – LIN23
270.00	LIN24	Output = 270.00 – LIN24
281.25	LIN25	Output = 281.25 – LIN25
292.50	LIN26	Output = 292.50 – LIN26
303.75	LIN27	Output = 303.75 – LIN27
315.00	LIN28	Output = 315.00 – LIN28
326.25	LIN29	Output = 326.25 – LIN29
337.50	LIN30	Output = 337.50 – LIN30
348.75	LIN31	Output = 348.75 – LIN31

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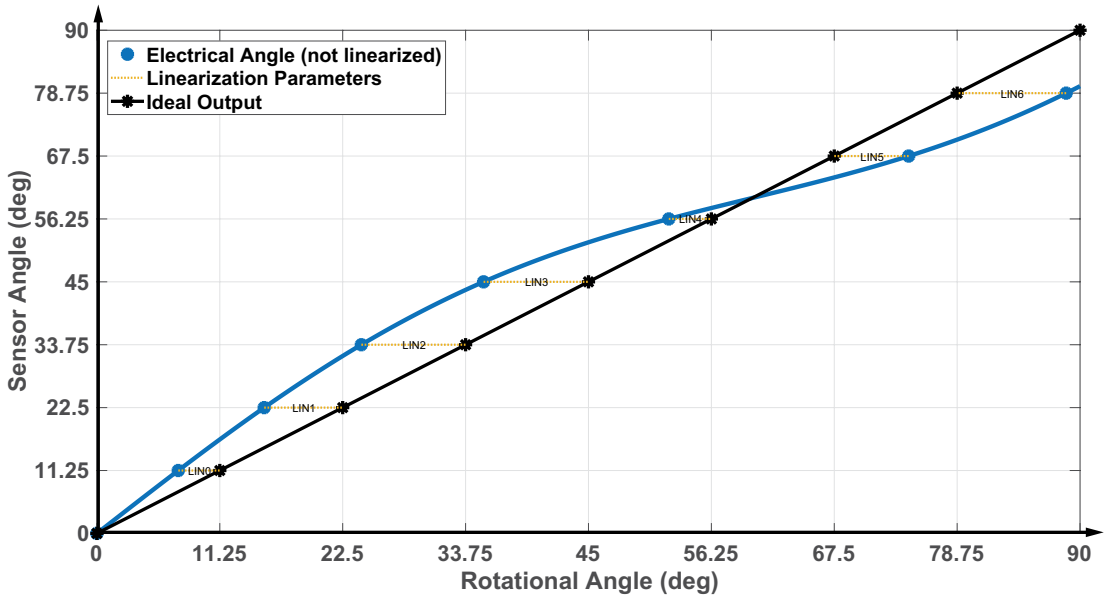


Figure 7: Linearization Example

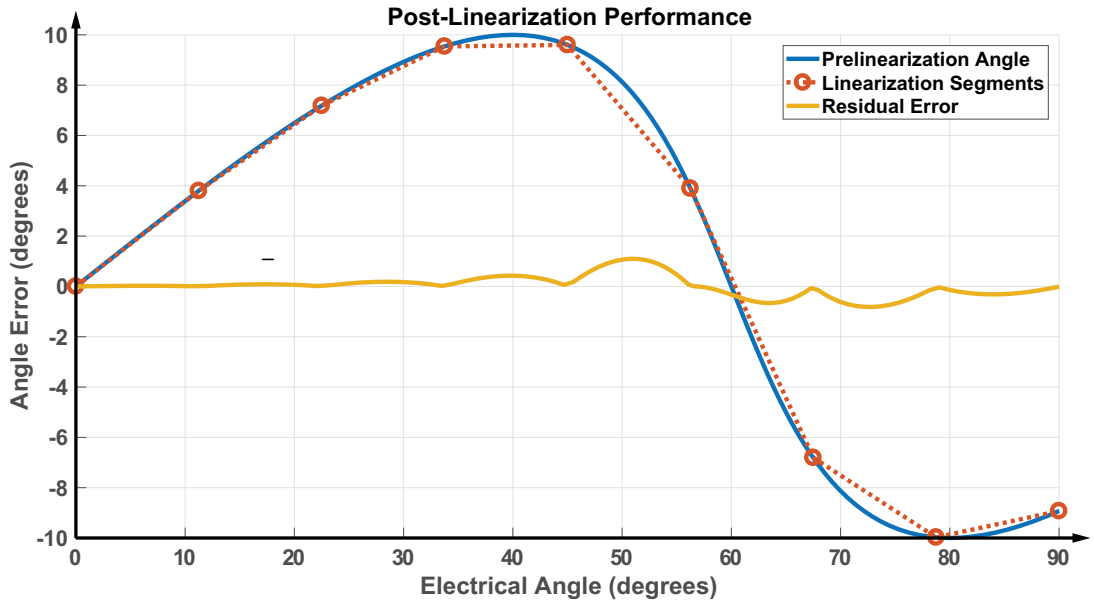


Figure 8: Post-Linearization Error

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Angle Hysteresis

Hysteresis can be applied to the compensated angle to moderate jitter in the angle output due to noise or mechanical vibration. In the A33002, the hysteresis field (ANG.HYSTERESIS) defines the width of an angle window at 14-bit resolution. Mathematically, the width of this window is:

$$ANG.HYSTERESIS \times (360 / 16384) \text{ degrees} \quad ,$$

giving a range of 0 to 1.384 degrees.

On the SPI or Manchester interface, the hysteresis-compensated angle can be read via an alternate register (HANG.ANGLE_HYS) at 12-bit resolution.

The effect of the hysteresis is shown in Figure 9. The current angle position as measured by the sensor is at the “head” of the hysteresis window. As long as the sensor (electrical) angle advances in the same direction of rotation, the output angle is the sensor angle, minimizing latency. If the sensor angle reverses direction, the output angle is held static until the sensor angle exits the hysteresis window in either direction. If the exit is in the opposite direction of rotation where the “head” was, the head flips to the opposite end of the hysteresis window and that becomes the new reference direction. The current direction of rotation, or “head” for the purposes of hysteresis, is viewable via the STA.ROT bit, where 0 is increasing angle direction and 1 is in decreasing angle direction.

This behavior has the following consequences:

1. If the hysteresis window is greater than the output resolution, the output angle skips consecutive resolution steps.
2. If there is jitter due to noise or mechanical vibration, especially at a static angle position or very slow rotation, the angle tends to bias to one side of the window, depending on the direction of rotation as the angular velocity approaches zero (i.e., toward the current “head”), rather than to the average position of the jitter.

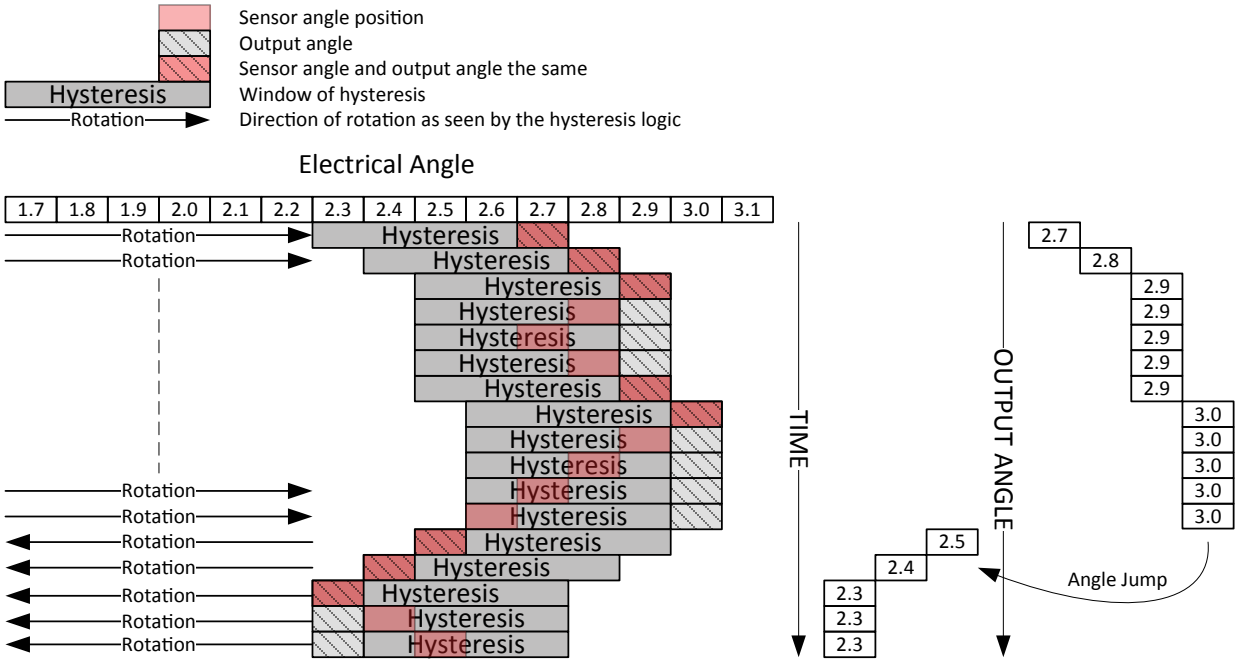


Figure 9: Effect of Hysteresis

NOTE: The rotation direction resets to 0 or increasing angle direction. At power-up or after LBIST, the hysteresis window is always behind the initial angle position. Therefore, if hysteresis is enabled, a decreasing angle direction of rotation does not register until the hysteresis window has passed.

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ESD Performance

Under certain conditions, the ESD rating of the dual-die IC may be less than 2 kV if ground pins are not tied together. For questions regarding ESD optimization, contact Allegro.

Package	ESD Rating
TSSOP-14 (single die)	5.5 kV
TSSOP-28 (dual die)	4.0 kV [1]

[1] All GND pins shorted together.

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Turns Counting

Certain automotive angle sensing applications involve the magnetic target rotating multiple times. Thus, tracking the turns of the measured magnet becomes more important than knowing the specific angle at which the target sits.

This implementation can also be used to measure exact angle in cases where the rotation is geared-up such that a slight angle rotation of the interested device results in multiple rotations of a target magnet that the sensor is measuring. For this reason, the A33002 includes a circuit that counts the rotational turns of a magnet. This feature also includes the ability to start up with a preset value, allowing the turns counter to persist through power-off periods, when combined with adequate system-level control. Traditionally, recovering the turns counter value is achieved by a combination of relatively complex mechanical and electrical components. The A33002 can help reduce system-level complexity and eliminate many system components by performing both the absolute angle measurement and the tracking of turns.

It is possible to use the ZCD signal path as the turns counter source. This is done by setting the TCP field in EEPROM to 0.

To read the total position of the magnetic encoder (angle in 12-bit resolution, as well as additional revolutions in 9 bits, sign-extended to 12 bits), a TURNS_DELTA serial register is provided. This 21-bit word accumulates the total changes in angle. The initial value of the register (zero, current angle, or current angle with TURNS_COUNT zeroed) can be controlled using the EEPROM field TURNS_INIT, as detailed in Figure 11.

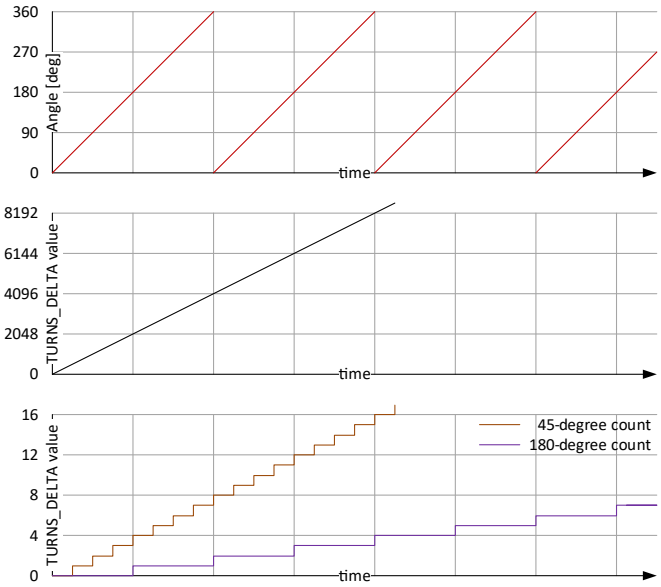


Figure 10: Turns Counting

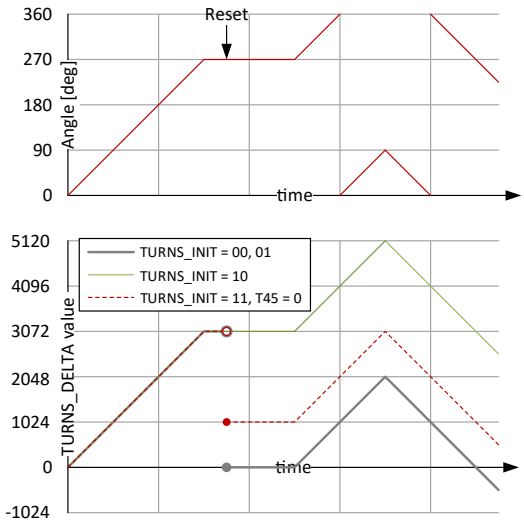


Figure 11: EEPROM field TURNS_INIT

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Turns Counting Behavior on Power-Up

Turns tracking, as measured by the IC, is derived from the TURNS_DELTA register. This is a 21-bit register that tracks absolute angle across multiple magnetic rotations, by tracking the change in angle from a reference position. The actual TURNS register (address 0x2C) is simply the upper bits from the TURNS_DELTA value. When configured in 180° turns mode (T45 set to 0), the upper 10 bits are used; if in 45° mode (T45 set to 1), the upper 12 bits are used to indicate the turns. The A33002 is capable of tracking up to –512/+511 turns in 180° mode and –2048/+2047 in 45° mode. The remaining lower bits of the TURNS_DELTA value are stored in the TURNS_OFFSET field. This value is latched when reading the TURNS value, allowing the TURNS_DELTA value to be reconstructed from a common timestamp.

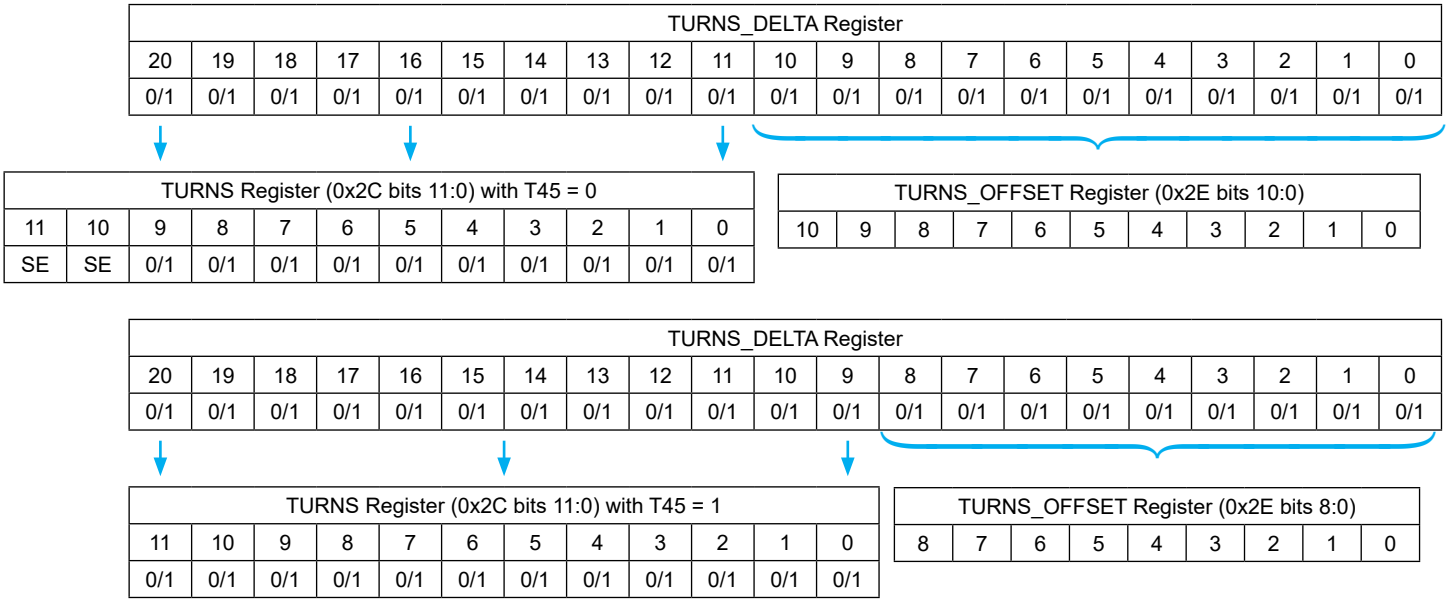


Figure 12: Turns Register

The reference position from which the TURNS_DELTA is measured impacts the initial turns count value. The TURNS_INIT field has the following options controlling this:

Table 6: TURNS_INIT (EEPROM 0x1D bits 19:18)

TURNS_INIT	Description
00	Turns counter is zeroed on power-up. Turns are tracked relative to the angle observed on power-up. TURNS_DELTA = 0 at power-up.
01	
10	Turns counter is set relative to the defined 0 position of the sensor, which may be a non-zero number. TURNS_DELTA is set to the angle observed on power-up.
11	Turns counter value initialized to zero, but increments on the 0/180 or 45 boundaries as observed by the IC (set via the T45 field). TURNS_DELTA register is initialized with an offset based on the T45 register.

Figure 11 illustrates how the TURNS_INIT field controls the starting turns count value. In Figure 11, the angle is constantly increasing, up to 270°, after which a sensor rest occurs.

For a TURNS_INIT value of 00_2 or 01_2, the TURNS_DELTA register measures the change in position relative to the observed angle on power-up. As such, the TURN value is initialized to 0 on sensor reset.

With TURNS_INIT set to 10_2, the TURNS_DELTA value represents the difference in position relative to the sensor's defined 0° position; put more simply, the TURNS_DELTA is initialized to the angle observed on power-up. As shown in Figure 11, once the reset occurs, the TURN_DELTA register is loaded with 3072 codes, which is 270° in 12-bit resolution. Depending on the T45 setting, this is reflected as a TURN value of 1 (in 180° mode) or 6 (in 45° mode).

When the TURNS_INIT field is set to 11_2, the turns count is initialized to 0, and the increment/decrement points for turns counting are fixed to either the 0/180° or the 0/45/90/135/180/225/270/315 boundaries, based on the T45 field. The TURNS_DELTA register will be loaded with the angular distance between two adjacent boundaries (0/180° or a multiple of 45°). For example, shown in Figure 11, the T45 bit is set to 0, enabling 180° mode. The TURN value in this case is 0. The angle on power-up is 270°, which is 50% between 180° and 360°; to reflect this, the TURNS_DELTA register is loaded with 1024 codes indicating it is halfway between one turn (one turn being 180° in 12-bit resolution, or 2048 codes).

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Setting the Turns Count Value

There are two ways to modify the value of the turns counter.

- Using the turns counter reset function
- By writing the TURNS_DELTA value to register EWD, and loading it into TURNS_DELTA

INVOKING A TURNS COUNTER RESET

Resetting the turns counter is a command invoked using the SPECIAL field of the CTRL register.

CHANGING OR RESTORING TURNS_DELTA VALUE

It is possible to load a desired value into the turns counter register. This may be useful if a certain externally stored value should be set again following a power loss. The turns counter register itself cannot be written directly. Instead, the writing action is an indirect one using the following steps:

1. Perform writing only when the system is stable, as indicated by the STA.AOK bit field.
2. Write the desired 21-bit value of TURNS_DELTA into the serial registers EWDH and EWDL in little-endian format. Example:
   A. To set the TURNS_DELTA to value 10441.32° (29 rotations and 1.32° current angle), write:
   (10441.32 / 360) × 4096 = 118799 = 0x01D00F.
   B. Write the lower 16 bits into register EWDL and the higher 5 bits into EWDH, with leading zeroes to make the 16-bit value to write. This results in writing 0x0001 to EWDH (0x04:0x05) and 0xD00F to EWDL (0x06:0x07).
3. Write the value 0x03 to the SPECIAL field and write 0x46 to the INITIATE_SPECIAL field.
4. The sensor behavior to process the setting depends on the setting of the TURNS_INIT EEPROM field:
   A. When TURNS_INIT = 00_2 or 01_2, the value is copied to TURNS_DELTA, and subsequent angle changes are accumulated on top of this value. Because small offset changes/noise errors accumulate every time such a write is performed, using this feature is not recommended if restoration of a saved value is desired.
   B. When TURNS_INIT = 10_2 or 11_2, the value is compared to the currently sensed angle. The TURNS_DELTA field “snaps” to the closest value matching the sensed angle. Errors in position of <180° are removed this way. This method is recommended if restoration of a saved TURNS_COUNT value is desired. However, the measured angle may have changed slightly in the meantime.

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DEVICE PROGRAMMING INTERFACE

The A33002 can be programmed in two ways:

- Using the *SPI interface* for input and output.
- Using a *Manchester protocol* on the supply pin for input, and the VOUT pin for output.

The A33002 features an internal charge pump and does not require high-voltage pulses to write EEPROM.

All setting fields and all data fields of the sensor can be read and written using both protocols. Locking the EEPROM from changes locks the EEPROM write access from both protocols.

A separate setting to completely disable the Manchester interface is available in the PWI.DM field of the EEPROM. Using this setting causes the sensor to ignore any commands entered using Manchester protocol. Disabling the Manchester interface does not disable the SPI interface.

For details regarding the programming procedures, contact your Allegro representative.

SWITCHING BETWEEN THE DIFFERENT OUTPUT PROTOCOLS

The A33002 supports four output protocols (SPI, Manchester, SENT, PWM), all of which overlap with the same pin. The hierarchy of precedence for control of the VOUT pin is:

- Manchester mode, when initiated via the VCC pin.
- SPI, when set with the SPO bit within the serial register.
- PWM, when set via the PWS.PEN in EEPROM.
- SENT, when enabled via the SENT_MODE field in EEPROM.
- SPI, when no other output is enabled.

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INTERFACE STRUCTURE

The A33002 consists of two memory blocks: Primary serial registers, and extended memory (shadow and EEPROM). The primary serial interface registers are used for direct writes and reads by the host controller for frequently required data (for example, angle data, warning flags, field strength, and temperature). All forms of communication (even to the extended locations) operate through the primary registers, whether it be via SPI or Manchester.

The primary serial registers also provide a data and address location for accessing extended memory locations. Accessing these extended locations is performed indirectly: the controller writes into the primary interface to give a command to the sensor to access the extended locations. The read/write is executed and the result is again presented in the primary interface.

This concept is shown in Figure 13 below.

For writing extended locations, the primary interface offers the registers EWCS, EWA, EWDH, and EWDL. EWA holds the extended address that should be written, and EWDH/EWDL contain the two high bytes and the two low bytes for the extended location contents. The EWCS register is used for commands and status data. For further information and other register fields associated with read transactions, refer to the Read Transaction from EEPROM and Other Extended Locations section.

For reading extended locations, the primary interface offers the registers ERCS, ERA, ERDH, and ERDL. ERA holds the extended address that should be read, and ERDH/ERDL contain the two high bytes and the two low bytes for the extended location contents. The ERCS register is used for commands and status data. For further information and other register fields associated with read transactions, refer to the Read Transaction from EEPROM and Other Extended Locations section.

EEPROM writing requires additional procedures. For more information about EEPROM and shadow memory read and write access, see the EEPROM and Shadow Memory Usage section.

The primary serial interface can be accessed using the SPI and using the Manchester interface. These two interfaces are detailed in the sections that follow.

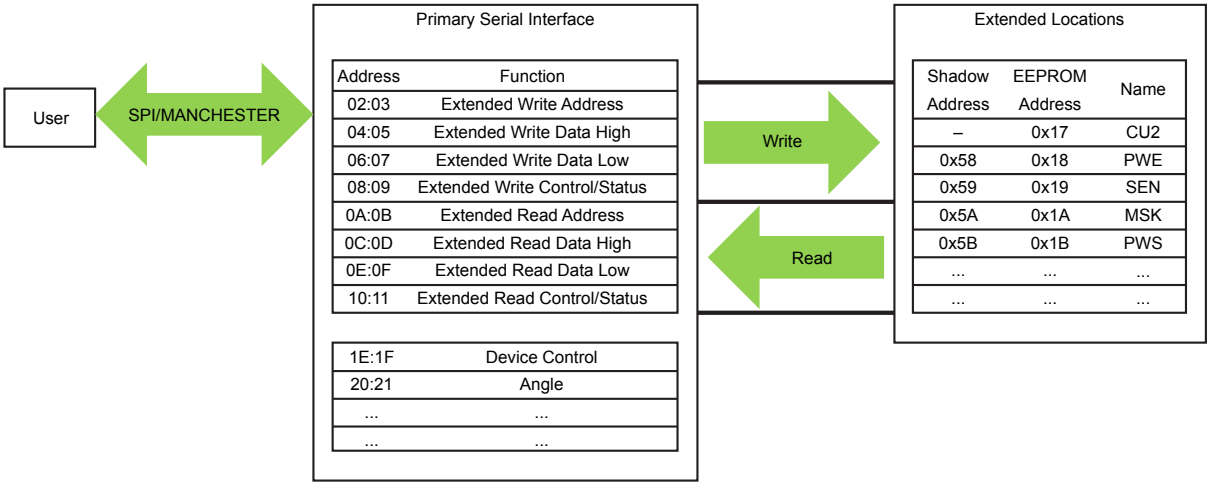


Figure 13: Serial Interface to Extended Memory (EEPROM and Shadow)

SPI INTERFACE VOLTAGE LEVELS

The A33002 is factory-programmed to operate with either 3.3 V or 5 V SPI levels. It is important that the interface voltages (both on the SPI bus and the SENT/PWM pin) match the expected level. Commutation issues may arise if a 5 V interface is used with a device programmed for 3.3 V operation (or vice versa). For more information, contact Allegro MicroSystems.

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SPI Interface

The setup for programming using the SPI interface is shown in Figure 14.

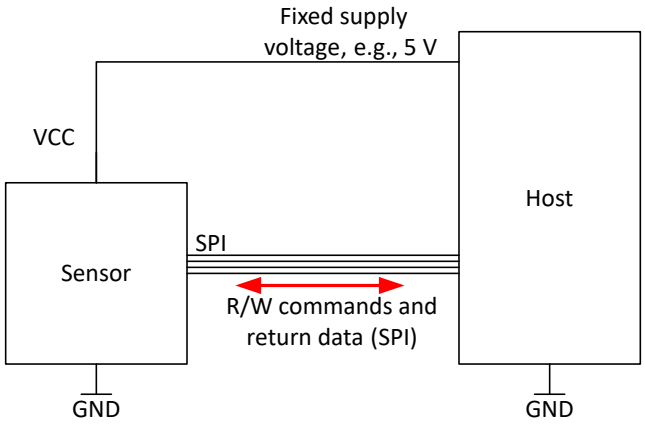


Figure 14: SPI Interface Programming Setup

SPI INTERFACE TIMING

The SPI interface operates in pure peripheral mode, with the controller controlling the SCLK, MOSI, and CS lines. The controller can maximize data throughput, up to $f_{SCLK(max)}$ of 10 MHz. The figures below show the timing for read and write cycles.

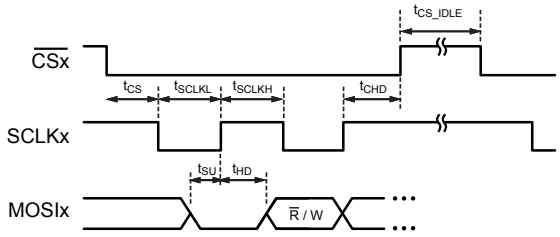


Figure 15: A33002 SPI Interface Timings Input

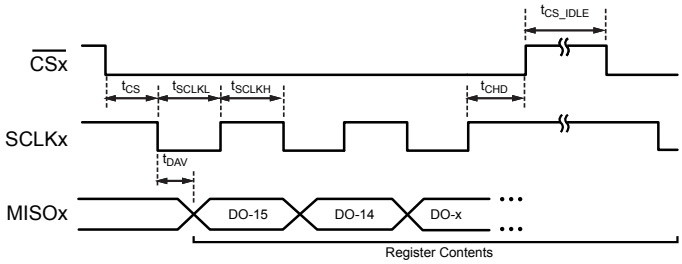


Figure 16: A33002 SPI Interface Timings Output

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SPI MESSAGE FRAME SIZE

The SPI interface requires 16-, 17-, or 20-bit packet lengths. The extended 20-bit SPI packet allows 4-bit CRC to accompany every data packet. The 17-bit packet is only allowed when the EEPROM/shadow bit S17 is set to 1.

The purpose of the 17-bit SPI option is to allow a delayed reading of the MISO line on the host side. Some hosts allow data to be sampled from the peripheral on the falling edge of SCLK. This is typically performed in the case of long interface delays caused by large line capacitances or very long cables. Due to the sampling on the falling edge, an additional 17th clock is required for the 16 bits of data.

During a SPI transaction, if the sensor detects a different number of clock pulses than expected, the interface warning WARN.IER becomes set. This is anything other than 16 or 20 when S17 = 0, or anything other than 17 when S17 = 1.

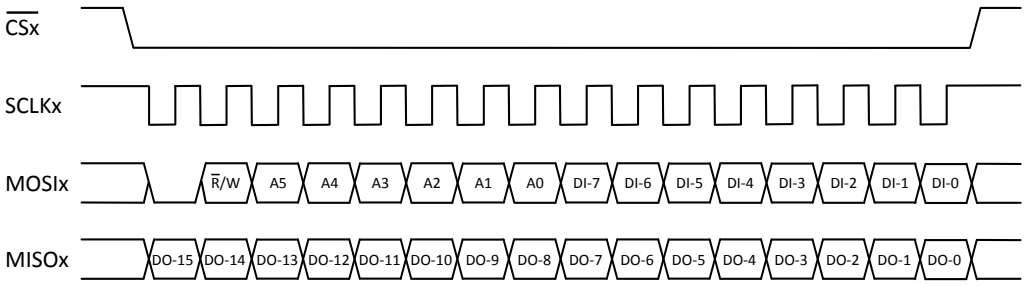


Figure 17: Sixteen-Bit SPI Transaction

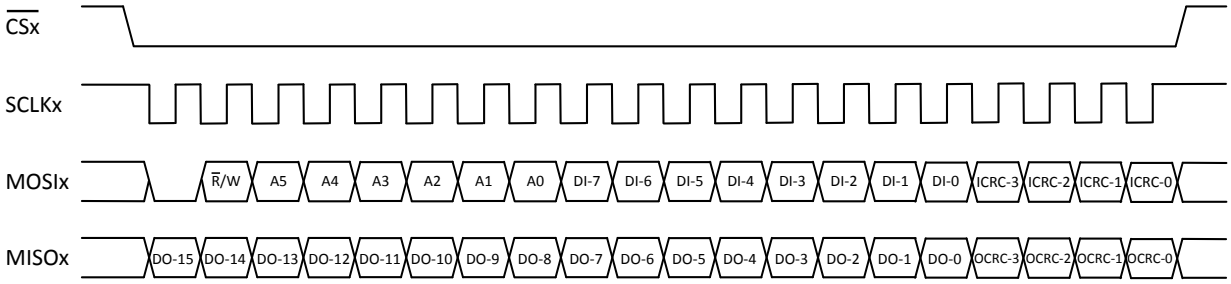


Figure 18: Twenty-Bit SPI Transaction

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WRITE CYCLE OVERVIEW

Write cycles consist of a 1-bit low, a 1-bit R/W asserted high, 6 address bits (corresponding to the primary serial register), 8 data bits, and 4 optional CRC bits. To write a full 16-bit serial register, two write commands are required (even and odd byte addresses). MOSI bits are clocked in on the rising edge of the controller-generated SCLK signal. The complete SPI packet is latched on the rising edge of the controller-generated ($\overline{CS}$) signal.

The simultaneous MISO signal output represents the contents of the corresponding die SPI read packet, including 16 data bits and 4 optional CRC bits—automatically included if a 17th SCLK edge is detected. The data bits correspond to the register contents selected during the previous read command. In the case where no previous read command has been issued, the MISO line transmits all zeroes.

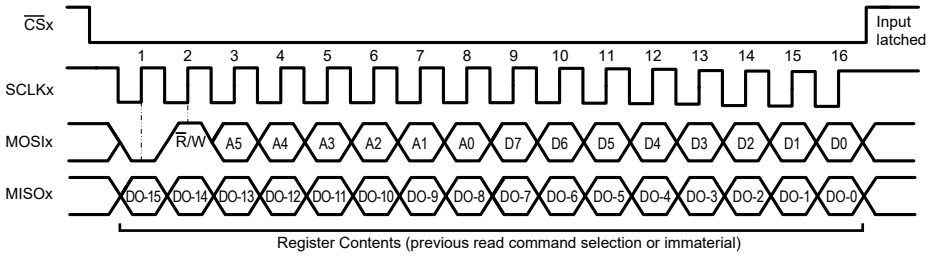


Figure 19: SPI Write Example

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READ CYCLE OVERVIEW

Read cycles have two stages: a read command, selecting a serial register address, followed by another read command to transmit the data from the selected register. Both commands consist of a 1-bit low, a 1-bit R/W asserted low, 6 address bits identifying the target register, and 8 data bits (all zeroes because no data is being written).

In the first stage, as with the write command, read command MOSI bits are clocked-in on the rising edge of the controller-generated SCLK signal, and data latched on the rising edge of the ($\overline{CS}$) signal. During the first read stage, the simultaneous MISO signal output is the content of the SPI read data from the previous read command.

In the second stage, the read command continues on the next falling edge of the controller-generated ($\overline{CS}$) signal. The MISO bits are the contents of the register selected during the first stage, read 16 bits at a time. The MISO bits transmit on the falling edge of the SCLK signal, such that the controller can sample them on the SCLK rising edges.

Because a SPI read can transmit 16 data bits at one time, the primary serial registers are built from one even and one odd byte, the entire 16-bit contents of one serial register may be transmitted with one SPI frame. This is accomplished by providing an even serial address value. If an odd-value address is sent, only the contents of the single byte are returned, with the 8 MSBs within the SPI packet set to zero.

Example: To read all 16 bits of the error register (0x24:0x25), send a SPI read request with the address bits set to 0x24. If only the 8 LSBs are desired, send an SPI read request with the address bits set to 0x25.

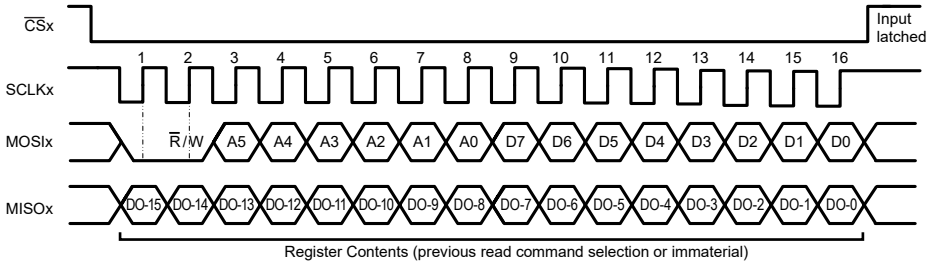


Figure 20: SPI Read Example, Register Selection

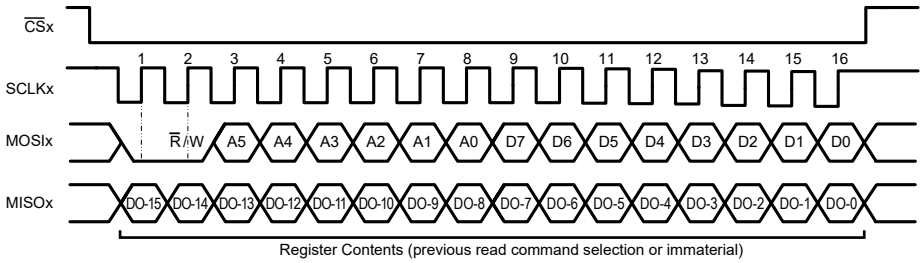


Figure 21: SPI Read Example, Data Output From Selected Register

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CRC

If the user wants to check the data coming from the sensor, it is possible to use 20-bit SPI frames. Without additional setting required, a 4-bit CRC is automatically generated and placed on the MISO line if more than 16 bits are read from the sensor.

The four additional CRC bits on the MOSI line coming from the host are ignored by the sensor, unless the PWI.SC bit is set within EEPROM (0x1B, bit 0). When the incoming CRC check is enabled, an incoming SPI packet with an incorrect CRC is discarded, and the CRC error flag is set in the WARN.CRC serial register.

The CRC is based on the polynomial $x^4 + x + 1$ with the linear feedback shift register preset to all ones. The 16-bit packet is shifted through from bit 15 (MSB) to bit 0 (LSB). The CRC logic is shown in Figure 22. Data are fed into the CRC logic with MSB first. Output is sent as C3-C2-C1-C0.

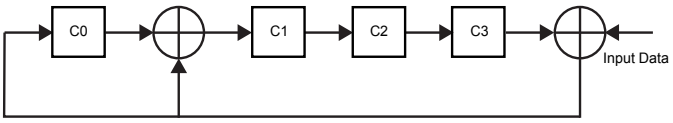


Figure 22: SPI CRC

The CRC output by the sensor on the MISO pin is always correct. The CRC from the host on the MOSI pin must be correct if the CRC enable bit PWI.SC in the EEPROM has been set.

NOTE: If the extended read data (ERD) register is read before the ERCS.ERD bit indicates a read has completed, there is a possibility of a CRC error, because the data could change during the read. Do not read the ERD register until it is known to be stable based on the completed bit indication or waiting sufficient time.

The CRC can be calculated with the following C code:

```
/*
* CalculateCRC
*
* Take the 16-bit input and generate a 4-bit CRC
* Polynomial = x^4 + x + 1
* LFSR preset to all 1's
*/
uint8_t CalculateCRC(uint16_t input)
{
    bool CRC0 = true;
    bool CRC1 = true;
    bool CRC2 = true;
    bool CRC3 = true;
    int  i;
    bool DoInvert;
    uint16_t mask = 0x8000;

    for (i = 0; i < 16; ++i)
    {
        DoInvert = ((input & mask) != 0) ^ CRC3;
        CRC3 = CRC2;
        CRC2 = CRC1;
        CRC1 = CRC0 ^ DoInvert;
        CRC0 = DoInvert;
        mask >>= 1;
    }

    return (CRC3 ? 8U : 0U) + (CRC2 ? 4U : 0U) + (CRC1 ? 2U
: 0U) + (CRC0 ? 1U : 0U);
}
```


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Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SPI INTERFACE SPECIFICATIONS (for 3.3 V SPI Mode)						
Digital Input High Voltage	V_{IH}	MOSI, SCLK, $\overline{CS}$ pins	2.8	–	3.63	V
Digital Input Low Voltage	V_{IL}	MOSI, SCLK, $\overline{CS}$ pins	–	–	0.5	V
SPI Output High Voltage	V_{OH}	MISO pins, C_L = 20 pF, T_A = 25°C, 5 V compliant	2.93	3.3	3.63	V
SPI Output Low Voltage	V_{OL}	MISO pins, C_L = 20 pF	–	0.3	–	V
SPI INTERFACE SPECIFICATIONS (for 5.0 V SPI Mode) (*Contact Allegro for 5 V SPI ordering information*)						
Digital Input High Voltage	V_{IH}	MOSI, SCLK, $\overline{CS}$ pins	3.75	–	5.5	V
Digital Input Low Voltage	V_{IL}	MOSI, SCLK, $\overline{CS}$ pins	–	–	0.5	V
SPI Output High Voltage	V_{OH}	MISO pins, C_L = 20 pF, T_A = 25°C, V_{CC} ≥ 5.0V	4	5	–	V
SPI Output Low Voltage	V_{OL}	MISO pins, C_L = 20 pF	–	0.3	–	V
SPI INTERFACE SPECIFICATIONS						
SPI Clock Frequency [1]	f_{SCLK}	MISO pins, C_L = 20 pF	0.1	–	10	MHz
SPI Clock Duty Cycle [1]	D_{fSCLK}	SPI_{CLKDC}	40	–	60	%
SPI Frame Rate [1]	t_{SPI}		5.8	–	588	kHz
Chip Select to First SCLK Edge [1]	t_{CS}	Time from $\overline{CS}$ going low to SCLK falling edge	50	–	–	ns
Chip Select Idle Time [1]	t_{CS_IDLE}	Time $\overline{CS}$ must be high between SPI message frames	200	–	–	ns
Data Output Valid Time [1]	t_{DAV}	Data output valid after SCLK falling edge	–	–	50	ns
MOSI Setup Time [1]	t_{SU}	Input setup time before SCLK rising edge	25	–	–	ns
MOSI Hold Time [1]	t_{HD}	Input hold time after SCLK rising edge	50	–	–	ns
SCLK to CS Hold Time [1]	t_{CHD}	Hold SCLK high time before $\overline{CS}$ rising edge	5	–	–	ns
Load Capacitance [1]	C_L	Loading on digital output (MISO) pin	–	–	20	pF

[1] Parameter is not guaranteed at final test. Determined by design.

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Manchester Serial Interface

The A33002 incorporates a serial interface on the VCC line. (Note: The A33002 may be programmed via the SPI, with additional wiring connections). This interface allows an external controller to read and write registers in the A33002 EEPROM and volatile memory. The device uses a point-to-point communication protocol, based on Manchester encoding per G.E. Thomas (a rising edge indicates a 0, and a falling edge indicates a 1), with address and data transmitted MSB first. The addressable Manchester code implementation uses the logic states of the SA1 pin to set address values for each die. The SA0 pin must be a logic 0 in order to communicate with the device over Manchester. For this reason, the two valid addresses are 0 and 2 ("00" and "10"). In this way, individual communication with up to two A33002 die is possible. Manchester ID options are:

SA1	SA0	ID Value
LOW	LOW	ID0
LOW	HIGH	Manchester disabled
HIGH	LOW	ID2
HIGH	HIGH	Manchester disabled

To prevent any undesired programming of the A33002, the serial interface can be disabled by setting the disable Manchester bit (PWI.DM, EEPROM address 0x1B, bit 3) to a 1. With this bit set, the A33002 ignores any Manchester input on VCC.

The setup for programming using the Manchester interface is given in Figure 23.

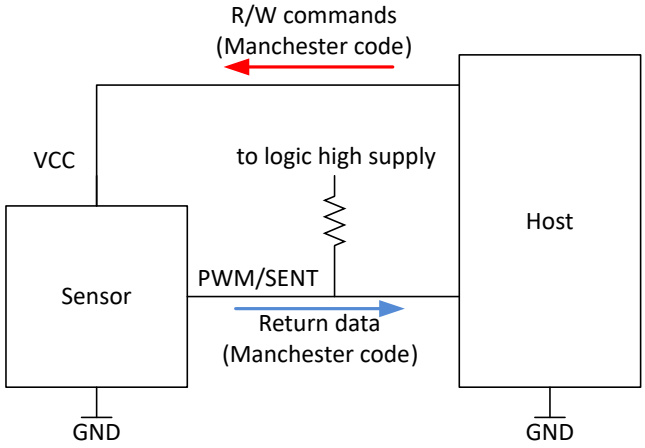


Figure 23: Manchester Interface Programming Setup

ENTERING MANCHESTER COMMUNICATION MODE

Provided the disable Manchester bit is not set in EEPROM, the A33002 continuously monitors the VCC line for valid Manchester commands. The part takes no action until a valid Manchester access code is received.

There are two special Manchester code commands used to activate or deactivate the serial interface and specify the output format used during read operations:

1. **Manchester Access Code:** Enters Manchester communication mode; Manchester code output on the PWM pin.
2. **Manchester Exit Code:** Returns the PWM pin to typical (angle data) output format.

Once the Manchester communication mode is entered, the PWM output pin ceases to provide angle data, interrupting any data transmission in progress. Both the access code and the exit code must be written to address 0x3F (address field of all ones).

TRANSACTION TYPES

As shown in Figure 23, the A33002 receives all commands via the VCC pin, and responds to read commands via the PWM pin. This implementation of Manchester encoding requires the communication pulses be within a high ($V_{MAN(H)}$) and low ($V_{MAN(L)}$) range of voltages on the VCC line.

Each transaction is initiated by a command from the controller; the A33002 does not initiate any transactions. Two commands are recognized by the A33002: write and read.

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CONTROLLER MANCHESTER MESSAGE STRUCTURE

The general format of a command message frame is shown in Figure 24. Note that, in the Manchester coding used, a bit value of 1 is indicated by a falling edge within the bit boundary, and a bit value of zero is indicated by a rising edge within the bit boundary.

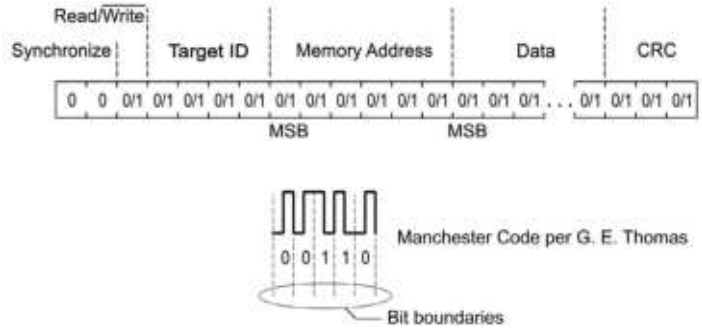


Figure 24: Manchester Message Format

A brief description of each bit is provided in Table 7.

Table 7: Manchester Command General Format

Bits	Parameter Name	Description
2	Synchronization	Value “00” sent to identify a command start and to synchronize sensor clock
1	Read/Write	0 = write, 1 = read
4	Target ID	Select the target ID for this transaction. [X, ID2, X. ID0] are each addressed/ ignored by a 1/0 at their address, so that a write to [0101] writes to ID0 and ID2. Reading from several sensors at the same time is not supported. Writing to [0000] is a broadcast write; it is written to all sensor dies.
6	Address	Serial address for read/write
16	Data	Only for writes: 16-bit write data. Omit for read commands
3	CRC	3-bit CRC, needed for all commands

Using the 4 bits of the Target ID field, die can be selected via their ID value, allowing multiple die to be individually addressed and providing for different group addressing schemes.

Example: If Target ID = [0100], the die set to ID2 is addressed. If Target ID is set to [0000], no ID comparison is made, allowing all sensors to be addressed at once.

Table 8: Target ID

Target ID			
Invalid	ID2	Invalid	ID0

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SENSOR MANCHESTER MESSAGE STRUCTURE

If a read command with the desired register number has been sent from the controller to the sensor, the device responds with a read response frame using the Manchester protocol over the PWM output.

The following command messages can be exchanged between the device and the external controller:

- Manchester access code (host to sensor)
- Manchester exit code (host to sensor)
- Manchester write command (host to sensor)
- Manchester read command (host to sensor)
- Manchester read response (sensor to host)

In addition to the contents of the requested memory location, a return status field is included with every read response. This field provides the ID used to communicate with the part and any errors which may have occurred during the transaction. These bits are:

- **ID:** ID ([SA1 SA0]) unless BC = 1 (ID is 00)
- **BC:** Broadcast; ID field was zero or SPI mode active
- **AE:** Abort error; edge detection failure after sync detect
- **OR:** Overrun error; A new Manchester command has been received before the previous request could be completed
- **CS:** Checksum error; a prior command had a checksum error

For EEPROM address information, refer to the EEPROM Reference section. For serial address locations, refer to the serial register map.

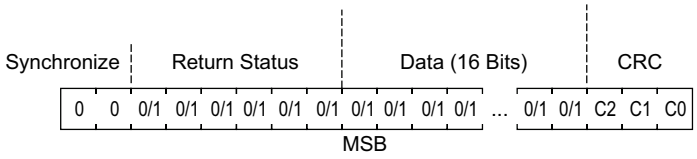


Figure 25: Manchester Message Format

Table 9: Return Status Bits

Return Status Bits (6 bits)					
5	**4**	**3**	**2**	**1**	**0**
ID		BC	AE	OR	CS

MANCHESTER ACCESS CODE

The Manchester access code must be sent before other Manchester commands.

The Manchester access code always operates as a broadcast pulse, meaning the sensor does not look at the Target ID field. For example, if two sensors configured with ID0 and ID2 respectively are sharing a common VCC line, a Manchester access code with a Target ID value of [0001] results in both sensors entering Manchester serial communication mode.

Table 10: Manchester Access Code

Bits	Parameter Name	Description
2	Synchronization	00
1	Read/Write	0
4	Target ID	0000 (this command is always a broadcast, even if it is addressed)
6	Address	111111 (fixed number for Manchester access message)
16	Data	0x62D2 (fixed number for Manchester access message)
3	CRC	3-bit CRC

An example follows, with target ID = [0001], data = access code = 0x62D2, and CRC = 110.

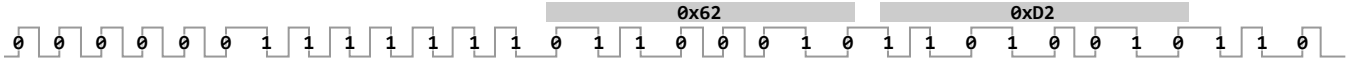


Figure 26: Target ID = [0001], Data = Access code = 0x62D2, CRC = 110

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MANCHESTER EXIT CODE

The Manchester exit code can be sent after Manchester access is complete, to avoid accidental decoding of Manchester commands.

The Manchester exit code always operates as a broadcast pulse, meaning the sensor does not look at the target ID field. For example, if two sensors configured with ID0 and ID2 respectively are sharing a common VCC line, a Manchester access code with a target ID value of [0001] results in both sensors exiting Manchester serial communication mode.

Table 11: Manchester Exit Code

Bits	Parameter Name	Description
2	Synchronization	'00'
1	Read/Write	'0'
4	Target ID	0000 (this is always a broadcast, even if it is addressed)
6	Address	111111 (fixed number for Manchester exit message)
16	Data	0x0000 (any value except 0x62D2 can be used for Manchester exit message)
3	CRC	3-bit CRC

An example follows, with target ID = [0001], data = 0x0000, and CRC = 110.

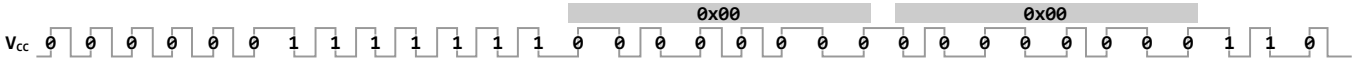


Figure 27: Target ID = [0001], Data = 0x0000, CRC = 110

MANCHESTER READ COMMAND

Determines which serial address within the sensor is the next to transmit the next read response data. The sensor must first receive a Manchester access code before responding to a read command.

This command is sent by the controller.

Table 12: Manchester Read Command

Bits	Parameter Name	Description
2	Synchronization	00
1	Read/Write	1
4	Target ID	Depends on targeted sensor ID, e.g., to target ID0, use 0001
6	Address	Serial register address, e.g. 0x10 for READ_DATA_LO, or 0x20 for ANGLE
3	CRC	3-bit CRC

An example follows where ANGLE register 0x20 is read from target ID [0001] with CRC = 111. The two synchronization pulses from the read response on the PWM return line are also shown.

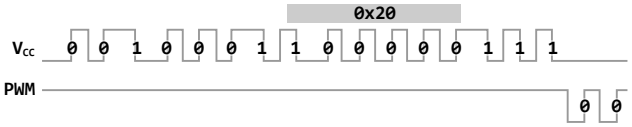


Figure 28: Target ID = [0001], angle = 0x20, CRC = 111

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MANCHESTER READ RESPONSE

The read response transmits data from the sensor to the controller after a read command. These data are sent by the sensor on the open-drain PWM pin. A pull-up resistor is needed for this to work.

Read from an even address, returns even byte [15:8] and odd byte [7:0].

Read from an odd address, returns odd byte [7:0] only. Data bits [15:8] are zeroes.

Table 13: Manchester Read Response

Bits	Parameter Name	Description
2	Synchronization	00
2	ID	Target ID of the responding sensor die. 00 for ID0, 01 for ID1, 10 for ID2, 11 for ID3.
1	BC flag	Broadcast: Value set to 1 if read command was a broadcast command (target ID set to [0 0 0 0]), 0 if not
1	AE flag	Abort error: Value set to 1 if a previous transaction was aborted and discarded, typically caused by incorrect bit lengths, 0 if there was no problem. The error is stored until it can be transmitted on the next read response and is cleared afterwards.
1	OR flag	Overrun error: If a command is sent to the sensor while the sensor is still sending a read response, and this command is completely transmitted before the read response was finished, an overrun error has occurred. This error is then stored until it can be transmitted on the next read response and is cleared afterwards.
1	CS flag	CRC error: Value set to 1 if a previous transaction had an incorrect CRC; 0 means there was no problem. The error is stored until it can be transmitted on the next read response and is cleared afterwards.
16	data	Read from an even address: even byte [15:8] and odd byte [7:0]. Read from an odd address: odd byte [7:0] only. Data bits [15:8] are zeroes.
3	CRC	3-bit CRC

An example follows where ANGLE register 0x20 is read, and the response is ID 00 (ID0), the four flags are all zeroes (no errors), the data is 0x5C34, and the CRC is 100.

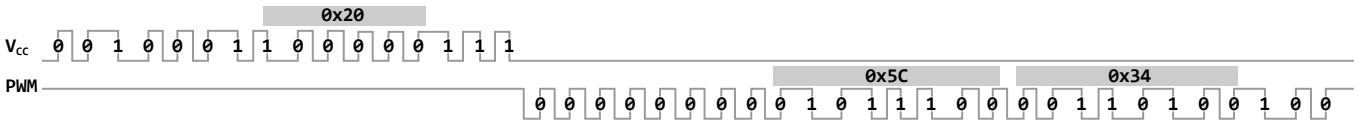


Figure 29: ID = 00, error flag = 0000, Data = 0x5C34, CRC = 100

MANCHESTER READ RESPONSE DELAY

The Manchester read response starts at the end of the read command. The response may start a ¼ bit time before the CRC finishes transmitting (overlap with last CRC bit) or a ¼ bit time after the CRC finishes transmitting.

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CRC

The serial Manchester interface uses a cyclic redundancy check (CRC) for data-bit error checking of all the bits coming after the two synchronization bits. The synchronization bits are not included in the CRC. The CRC algorithm is based on the polynomial:

$$g(x) = x^3 + x + 1.$$

The calculation is represented graphically in Figure 30. The trailing 3 bits of a message frame comprise the CRC token. The CRC is initialized at 111. Data are fed into the CRC logic with MSB first. Output is sent as C2-C1-C0.

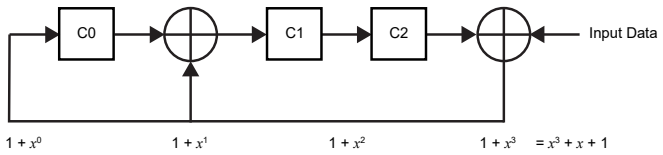


Figure 30: Manchester CRC Calculation

The 3-bit Manchester CRC can be calculated using the following C code:

```
// command: the Manchester command, right justified, does
not include the space for the CRC
// numberOfBits: number of bits in the command not includ-
ing the 2 zero sync bits at the start of the command and the
three CRC bits
// Returns: The three-bit CRC
// This code can be tested at http://codepad.org/yqTKnfmD

uint16_t ManchesterCRC(uint64_t data, uint16_t numberOfBits)
{
	bool C0 = false;
	bool C1 = false;
	bool C2 = false;
	bool C0p = true;
	bool C1p = true;
	bool C2p = true;
	uint64_t bitMask = 1;

	bitMask <<= numberOfBits - 1;

	// Calculate the state machine
	for (; bitMask != 0; bitMask >>= 1)
	{
		C2 = C1p;
		C0 = C2p ^ ((data & bitMask) != 0);
		C1 = C0 ^ C0p;

		C0p = C0;
		C1p = C1;
		C2p = C2;
	}

	return (C2 ? 4U : 0U) + (C1 ? 2U : 0U) + (C0 ? 1U :
0U);
}
```


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Table 14: Manchester Access Code

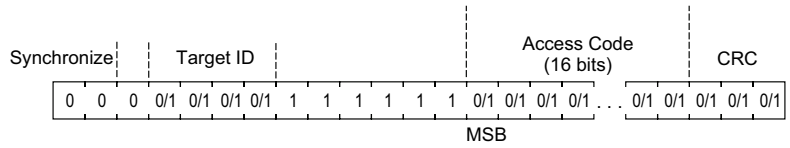
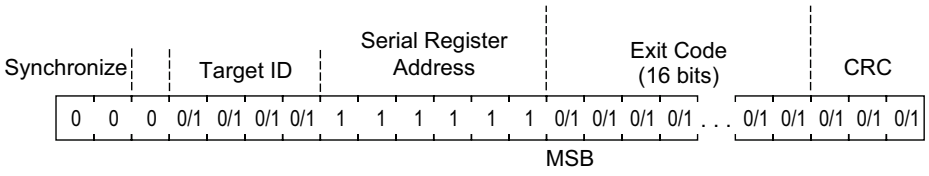
Function	Transmits the access code to the A33002. Enters serial communication mode with the desired output protocol.
Syntax	Sent by the external controller on the A33002 VCC pin.
Related Commands	Related command: serial exit code
Pulse Sequence	
Options	Access codes: Manchester access code = 0x62D2 Selects Manchester output on the PWM pin.
Examples	The Manchester access code operates as a broadcast pulse, meaning the target ID field is inconsequential. For example, if two A33002s configured with ID0 and ID2 respectively are sharing a common V_{CC} line, a Manchester access code with a target ID value of 0x1 results in both sensors entering Manchester serial communication mode.

Table 15: Manchester Exit Code

Function	Returns the A33002 to typical operation.
Syntax	Sent by the external controller on the A33002 VCC pin. Manchester exit code = Any value other than 0x62d2
Related Commands	Manchester access codes
Pulse Sequence	
Options	None
Examples	Similar to the Manchester access code, the Manchester exit code acts as a broadcast pulse. To exit the serial communication mode, the exit code can be any value besides the access code (such as 0x0000).

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Table 16: Manchester Read

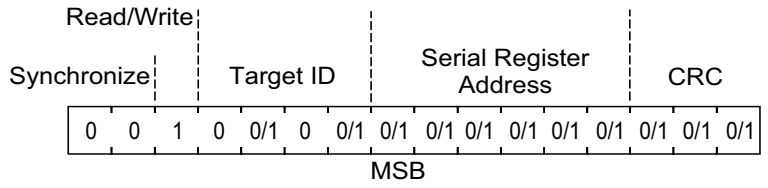
Function	Determines the serial address within the A33002 from which the next read response transmits data. The A33002 must first receive a Manchester access code before responding to a read command.
Syntax	Sent by the external controller on the A33002 VCC pin.
Related Commands	Read response
Pulse Sequence	
Options	None
Examples	–

Table 17: Manchester Read Response

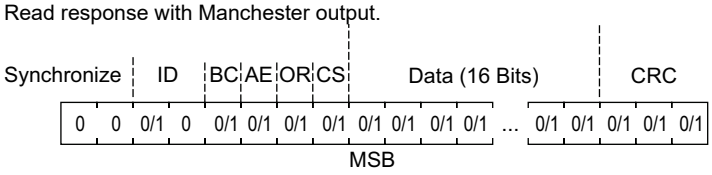
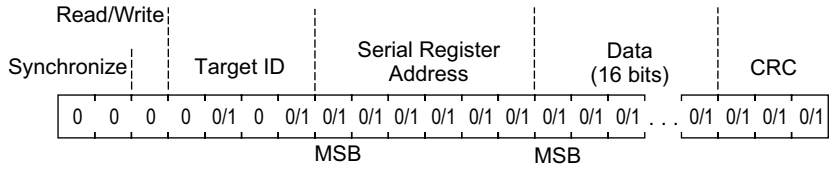
Function	Transmits to the external controller data retrieved from the A33002 serial register in response to the most recent read command.
Syntax	Sent by the A33002 on the PWM pin. Sent after a read command.
Related Commands	Read
Pulse Sequence	Read response with Manchester output. 
Options	Read from an even address, returns even byte [15:8] and odd byte [7:0]. Read from an odd address, returns odd byte [7:0] only. Data bits [15:8] become zeroes.
Examples	–

Table 18: Manchester Write

Function	Transmits to the A33002 data prepared by the external controller.
Syntax	Sent by the external controller on the A33002 VCC pin.
Related Commands	
Pulse Sequence	
Options	If the address is even, data is written to the address and the address+1 (16-bit write). If the address is odd, only 8 bits are written (LSB of 16-bit data field).
Examples	–

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EEPROM AND SHADOW MEMORY USAGE

The device uses EEPROM to permanently store configuration parameters for operation. EEPROM is user-programmable and permanently stores operation parameter values or customer information. The operation parameters are downloaded to shadow (volatile) memory at power-up. Shadow fields are initially loaded from corresponding fields in EEPROM, but can be overwritten, either by performing an extended write to the shadow addresses, or by reprogramming the corresponding EEPROM fields and power cycling the IC. Use of shadow memory is substantially faster than accessing EEPROM. In situations where many parameters need to be tested quickly, shadow memory is recommended for trying parameter values before permanently programming them into EEPROM. The shadow memory registers have the same format as the EEPROM and are accessed at extended addresses 0x40 higher than the equivalent EEPROM address. Unused bits in the EEPROM do not exist in the related shadow register and return 0 when read. Shadow registers do not contain the ECC bits. Shadow registers have the same protection restrictions as the EEPROM. All registers can be read without unlocking. For mapping of bits from register addresses in EEPROM to their corresponding register addresses in shadow, see the EEPROM Table section).

Enabling EEPROM Access

To enable EEPROM write access after power-on-reset, an unlock code needs to be written to the KEYCODE serial register. This involves five write commands, executed as follows:

1. Write 0x00 to register 0x3C [15:8]
2. Write 0x27 to register 0x3C [15:8]
3. Write 0x81 to register 0x3C [15:8]
4. Write 0x1F to register 0x3C [15:8]
5. Write 0x77 to register 0x3C [15:8]

This sequence must be performed once after power-on reset if the customer intends to write to the EEPROM.

Writing to serial registers and reading from serial registers does not require special treatment after power-on.

Reading all EEPROM cells is always possible.

The device must be unlocked when performing EEPROM margin checking.

EEPROM Write Lock

It is possible to protect the EEPROM against accidental writes.

- Setting the LOCK field in EEPROM to the value 0xC (1100 in binary) blocks any writes to the EEPROM, so that permanent changes are not possible. Temporary changes to the setting are still possible by writing to the shadow memory, but these changes are lost after a power cycle. This lock is permanent and cannot be reversed. Reading of the settings is still possible.
- Setting the LOCK field in EEPROM to the value 0x3 (0011 in binary) locks both EEPROM writes and shadow memory writes. This means none of the sensor settings can be changed. This lock is permanent and cannot be reversed. Reading of the settings is still possible.

Write Transaction to EEPROM and Other Extended Locations

Invoking an extended write access is a three-step process:

1. Write the extended address into the EWA register (using SPI or Manchester direct access). EWA is the 8-bit extended address that determines which extended memory address to access.
2. Write the data that is to be transferred into the EWD registers (using SPI or Manchester direct access). This takes four SPI writes or 2 Manchester packets to load all 32 bits of data.
3. Invoke the extended access by writing the direct EWCS.EXW bit with 1.

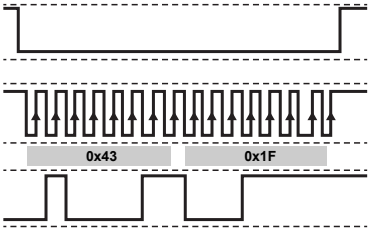
The 32-bit of data in EWD are then written to the address specified in EWA.

The bit EWCS.WDN can be polled to determine when the write completes. This is only necessary for EEPROM writes, which can take up to 24 ms to complete. Shadow register writes complete immediately in one system clock cycle after synchronization.

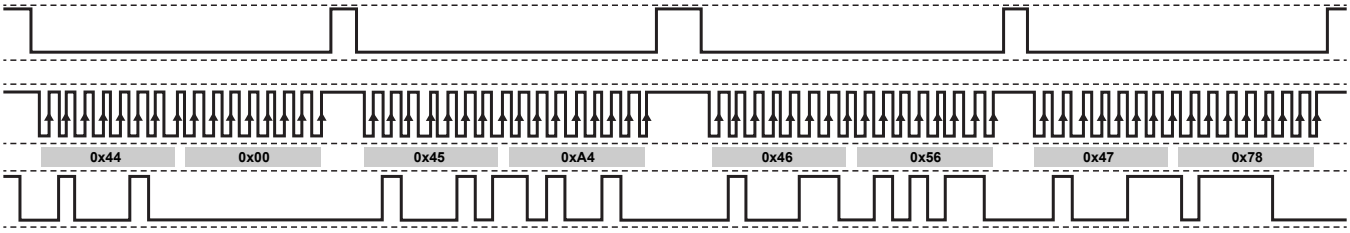
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For example, to write location 0x1F in the EEPROM with 0x00A45678:

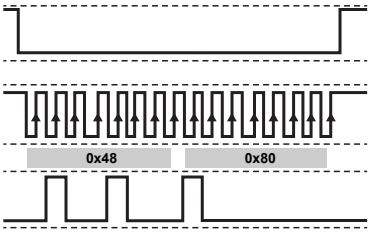
• Write 0x1F to lower 8 bits of EWA register (0x1F to EWA+1 Address 0x03)



• Write 0x00A45678 to EWD (0x00 to EWD, 0xA4 to EWD+1, 0x56 to EWD+2, 0x78 to EWD+3)

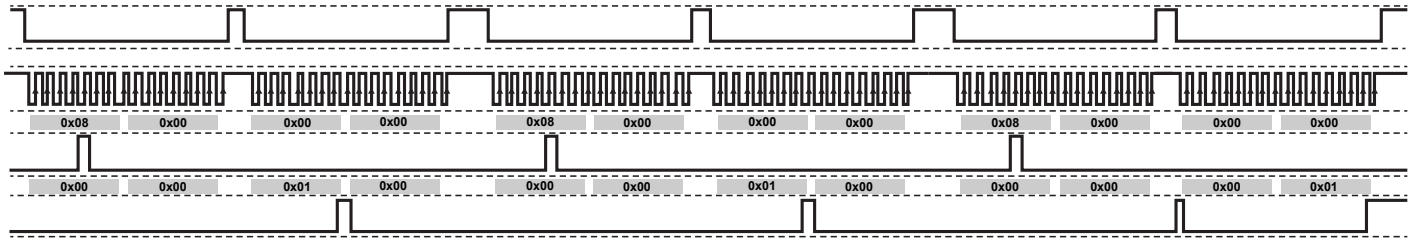


• Write 0x80 to EWCS



• Read EWCS+1 until bit 0 (WDN) is set, or wait enough time.

In the example, register 0x08 is read, so that the second output byte is from register 0x09, and we wait for bit 0 to become 1, which happens in the last read.



If an access violation occurs (address not unlocked), the transaction terminates, the corresponding RDN or WDN bit is set, and the XEE warning bit is asserted. The XEE bit in the ERR register also sets if the EEPROM write aborts.

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After writing to the EEPROM, verify that the write was successful by performing an EEPROM margin check.

EEPROM Margin Check

Due to nonidealities in transistors, current slowly leaks into or out of EEPROM cells and can, over time, cause small changes in the stored voltage level. Variances in voltage levels of the charge pump can result in a variety of stored EEPROM cell voltages when programming. If this value is marginally close to the threshold, the small drift over lifetime can cause this value to move across the threshold. This results in a corrupted EEPROM value. Because this drift happens slowly over time, if there is an issue, it may not appear for years. For this reason, it is important to perform margin testing (margining) to verify the internal voltage levels of EEPROM cells after programming and ensure future issues do not occur.

Margining is performed by Allegro on all registers at final test. Because EEPROM cell voltages are only modified when writing to the cell, it is not necessary to perform margining on registers that have not been modified.

Margining is performed in two steps: the first checks the validity of the voltage stored on digital “1” cells, and the second checks the voltage stored on digital “0” cells. It is important to perform both steps to ensure there are no issues.

To perform margining, a value of 0b0001 must be written to the SPECIAL field of the CTRL register. This reduces the internal threshold value. Once this value is written, an EEPROM read uses this lower threshold when reading EEPROM values. Perform a read on all EEPROM registers that are being tested, and confirm they read correctly. If a stored voltage is marginal to the typical operating threshold, a one appears that should be a zero.

Repeat this test with the value of 0b0010 in the SPECIAL register to raise the threshold value above typical operation. Again, read all EEPROM registers being tested. In this test, any stored high voltage that is marginal to the typical threshold appears as a zero where there should be a one.

If a bit is read incorrectly during either test, perform another EEPROM write of the desired values to the register and retest the margins.

Unlike other values in the SPECIAL field, these values persist and can be read to confirm the write was successful. As a result, the SPECIAL register must be cleared (or power-cycled) to return the threshold value to its typical level.

In Figure 30, $V_{NOM(H)}$ represents the nominal voltage programmed into EEPROM cells containing a one, and $V_{NOM(L)}$ represents the nominal voltage programmed into EEPROM cells containing a zero. The red and blue lines represent the actual voltage levels in the programmed cells for values of one and zero, respectively. As can be observed, at time 0 when the margin test is run, both high and low levels still appear to be the correct value when the threshold is moved to the margin testing levels.

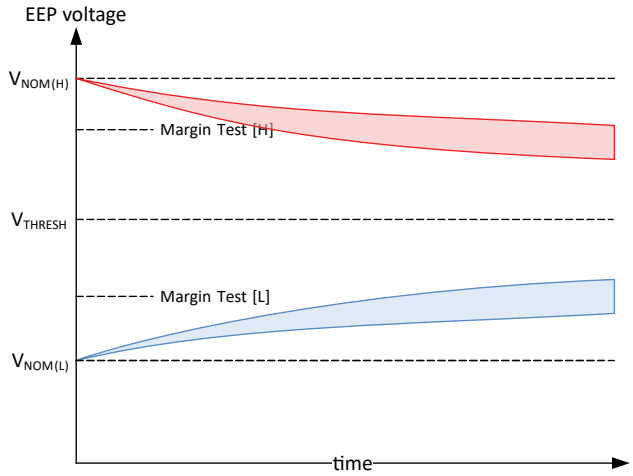


Figure 31: Example of passing programming voltages

In Figure 31, the high and low voltage levels at the time of programming are farther from their target. The drift over time results in these values crossing V_{THRESH} and becoming corrupted. At time 0 when the margin test is run, these values fail and are reported as errors to be reprogrammed.

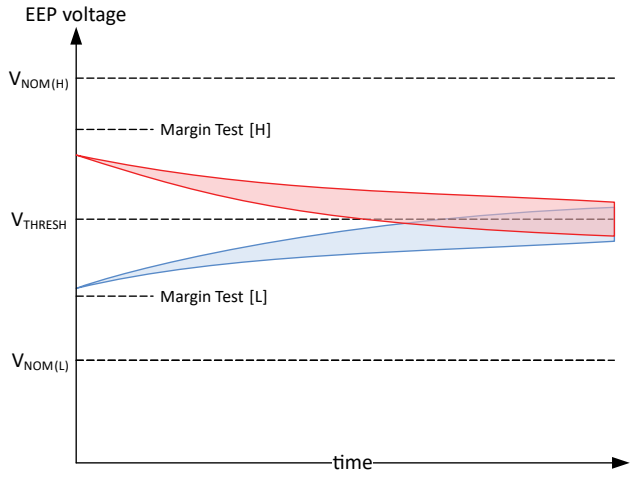


Figure 32: Example of failing programming voltages

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Margining is shown below as a list of high-level steps. For details about performing individual steps, see the associated sections.

1. Clear the ERR and WARN registers.
   A. Set the CTRL.CLW and CTRL.CLE bits.
2. Enable EEPROM access.
3. Write new data to the EEPROM as desired.
4. Check the following flags for EEPROM errors: ESE, EUE, XEE,IER, CRC, and BSY.
   A. If any are asserted, the EEPROM write may have failed.
   B. A second write attempt is recommended.
5. Set CTRL.SPECIAL to 0001b to enable low-voltage margining.
6. Read all EEPROM addresses changed in step 3 and verify their contents.
   A. Verify the ESE and EUE error flags are clear.
7. Set CTRL.SPECIAL to 0010b to enable high-voltage margining.
8. Read all EEPROM addresses changed in step 3 and verify their contents.
   A. Verify the ESE and EUE error flags are clear.
9. If any EEPROM value read with a low or high threshold differs from the desired EEPROM or if either the ESE or EUE bits are set, EEPROM margining has failed.
   A. One additional write attempt and margin check should be accomplished. If margin failures persist following a second EEPROM write, the device should be discarded.

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Read Transaction from EEPROM and Other Extended Locations

Extended access is provided to additional memory space via the direct registers. This access includes the EEPROM and EEPROM shadow registers. All extended registers are up to 32 bits wide. Invoking an extended read access is a three-step process:

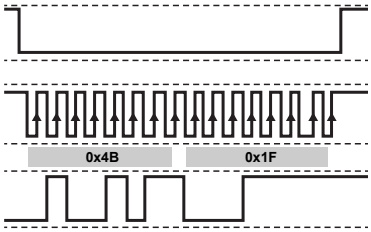
1. Write the extended address to be read into the ERA register (using SPI or Manchester direct access). ERA is the 8-bit extended address that determines which extended memory address is accessed.
2. Invoke the extended access by writing the direct ERCS.EXT bit with a one. The address specified in ERA is then read, and the data is loaded into the ERD registers.
3. Read the ERD registers (using SPI or Manchester direct access) to get the extended data. This takes multiple packets to get all 32 bits.

EEPROM read accesses may take up to 2 µs to complete. The ERCS.RDN bit can be polled to determine if the read access is complete before reading the data. Shadow register reads complete in one system clock cycle after synchronization. Do not attempt to read the ERD registers if the read access is potentially in process, as it could change during the serial access, and the data would be inconsistent. It is also possible that an SPI CRC error would be detected if the data were to change during the serial read via the SPI interface.

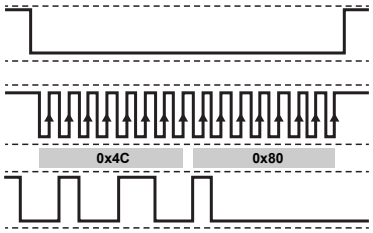
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For example, to read location 0x1F in the EEPROM:

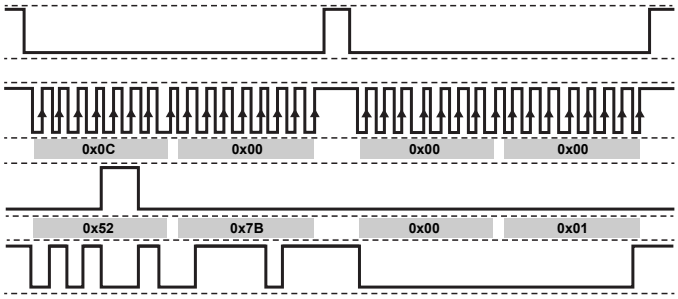
• Write 0x1F to the lower 8 bits of ERA [0x1F to (ERA + 1), address 0x0B].



• Write 0x80 to ERCS.

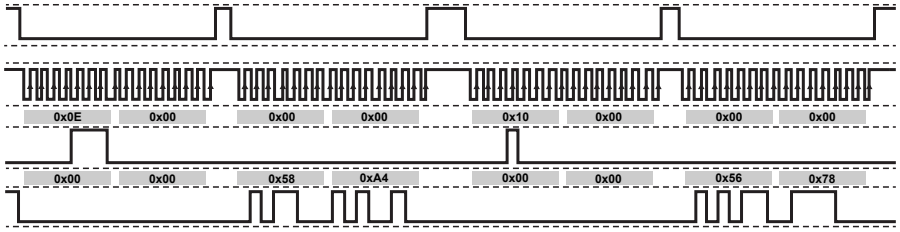


• Read (ERCS + 1) until bit 0 (RDN) is set, or wait enough time.
In the example, register 0x0C is read, so that the last bit of the second output byte contains the RDN bit.



• Read ERDH (upper 16 bits of read data).
• Read ERDL (lower 16 bits of read data).
In the example below, the result for the data at address 0x1F is 0x58A45678. In this value:

- □ Bits [31:26] are the EEPROM CRC.
- □ Bits [25:24] are unused and are zero.
- □ Bits [23:0] are the EEPROM values that can be used. These are the 24 bits containing the data 0xA45678 that was written in the EEPROM write example.



NOTE: It is possible to pipeline transactions in this example, i.e., send a new command while reading return data from the old command. Pipelining would result in 5 SPI frames to perform the transaction instead of 8.

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Shadow Memory Read and Write Transactions

Shadow memory read and write transactions are identical to those for EEPROM. Instead of addressing to the EEPROM extended address, the shadow extended addresses located at an offset of 0x40 above the EEPROM are addressed. For all addresses, refer to the EEPROM Table.

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SERIAL INTERFACE TABLE

Table 19: Primary Serial Interface Registers Bits Map

Address* (0x00)	Register Symbol	Read/ Write	Addressed Byte (MSB)								Addressed Byte + 1 (LSB)								LSB Address
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x00	NOP	RO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x01
0x02	EWA	RW	0	0	0	0	0	0	0	0	WRITE_ADR								0x03
0x04	EWDH	RW	WRITE_DATA_HI																0x05
0x06	EWDL	RW	WRITE_DATA_LO																0x07
0x08	EWCS	WO/RO	EXW	0	0	0	0	0	0	WIP	0	0	0	0	0	0	0	WDN	0x09
0x0A	ERA	RW	0	0	0	0	0	0	0	0	READ_ADR								0x0B
0x0C	ERCS	WO/RO	EXR	0	0	0	0	0	0	RIP	0	0	0	0	0	0	0	RDN	0x0D
0x0E	ERDH	RO	READ_DATA_HI																0x0F
0x10	ERDL	RO	READ_DATA_LO																0x11
0x12 0x14 0x16 0x18 0x1A 0x1C	Unused	RO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x13 0x15 0x17 0x19 0x1B 0x1D
0x1E	CTRL	RW/WO	SPECIAL				SPO	CLS	CLW	CLE	INITIATE_SPECIAL								0x1F
0x20	ANG	RO	0	EF	UV	P	ANGLE												0x21
0x22	STA	RO	1	0	0	0	EPTR	0	DIEID		ROT	0	SDN	BDN	LBR	CSTR	BIP	AOK	0x23
0x24	ERR	RO	1	0	1	0	WAR	STF	AVG	0	PLK	ZIE	EUE	WDE	UVD	UVA	MSL	RST	0x25
0x26	WARN	RO	1	0	1	1	IER	CRC	SEN	0	XEE	TR	ESE	SAT	TCW	BSY	MSH	TOV	0x27
0x28	TSEN	RO	1	1	1	1	TEMPERATURE												0x29
0x2A	SFIELD	RO	1	1	1	0	GAUSS												0x2B
0x2C	TURNS	RO	1	1	TSRC	P	TURNS												0x2D
0x2E	TOFF	RO	1	LAT	0	P	0	TURNS_OFFSET											0x2F
0x30	HANG	RO	0	EF	UV	P	ANGLE_HYS												0x31
0x32	ANG15	RO	0	ANGLE_15															0x33
0x34	ZANG	RO	0	EF	UV	P	ANGLE_ZCD												0x35
0x36	TD_ HIGH	RO	0	EF	TSRC	P	TURNS_DELTA [23:12]												0x37
0x38	TD_ LOW	RO	0	EF	LAT	P	TURNS_DELTA [11:0]												0x39
0x3A	PTANG	RO	0	EF	UV	P	PLL_TURNS_ANGLE												0x3B
0x3C	IKEY	WO/RO	KEYCODE								0	0	0	0	0	0	0	CUL	0x3D
0x3E	Unused	RO	Unused																0x3F

*Addresses that span multiple bytes are addressed by the most significant byte.

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PRIMARY SERIAL INTERFACE REGISTERS REFERENCE

Address 0x00:0x01 (NOP)—Null Register

Address	0x00								0x01							
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Address 0x02:0x03 (EWA)—Extended Write Address

Address	0x02								0x03							
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	0	0	0	0	0	0	0	0	WRITE_ADDR							
R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

WRITE_ADDR [7:0]
Address to be used for an extended write. Address ranges:
0x17:0x2F—EEPROM (requires ≈ 24 ms)
0x58:0x6F—Shadow

Address 0x04:0x05 (EWDH)—Extended Write Data High

Address	0x04								0x05							
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	WRITE_DATA_HI															
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

WRITE_DATA_HI [15:0]
Upper 16 bits of data for an extended write operation.

Address 0x06:0x07 (EWDL)—Extended Write Data Low

Address	0x06								0x07							
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	WRITE_DATA_LO															
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

WRITE_DATA_LO [15:0]
Lower 16 bits of data for an extended write operation.

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Address 0x08:0x09 (EWCS)—Extended Write Control and Status

Address	0x08								0x09							
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	EXW	0	0	0	0	0	0	WIP	0	0	0	0	0	0	0	WDN
R/W	W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

EXW [15]
Initiate extended write by writing with a 1. Sets WIP, clears WDN. Write-only, always reads back 0.

WIP [8]
Write is in progress when value is 1.

WDN [0]
Write is complete when value is 1; clears when EXR is set to 1.

Address 0x0A:0x0B (ERA)—Extended Read Address

Address	0x0A								0x0B							
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	0	0	0	0	0	0	0	0	READ_ADDR							
R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

READ_ADDR [7:0]
Address to be used for an extended read. Address ranges:
0x00:0x1F—EEPROM (requires ≈2 µs)
0x40:0x5F—Shadow

Address 0x0C:0x0D (ERCS)—Extended Read Control and Status

Address	0x0C								0x0D							
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	EXR	0	0	0	0	0	0	RIP	0	0	0	0	0	0	0	RDN
R/W	W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

EXR [15]
Initiate extended read by writing with the value 1. Sets RIP, clears RDN. Write-only, always reads back 0.

RIP [8]
Read in progress when value is 1.

RDN [0]
Read is complete when value is 1; clears when EXR is set to 1.

Address 0x0E:0x0F (ERDH)—Extended Read Data High

Address	0x0E								0x0F							
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	READ_DATA_HI															
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

READ_DATA_HI [15:0]
Upper 16 bits of data from extended read operation, valid when ERCS.RDN is set to 1.

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Address 0x10:0x11 (ERDL)—Extended Read Data Low

Address	0x10								0x11							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	READ_DATA_LO															
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

READ_DATA_LO [15:0]
Lower 16 bits of data from extended read operation, valid when ERCS.RDN is set to 1.

Address 0x1E:0x1F (CTRL)—Device Control

Address	0x1E								0x1F							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPECIAL				SPO	CLS	CLW	CLE	INITIATE_SPECIAL							
R/W	R/W	R/W	R/W	R/W	R	R/W	W	W	W	W	W	W	W	W	W	W

SPECIAL [15:12]

Defines specific actions to be taken by the IC. Many actions are only invoked after the CTRL.INITIATE_SPECIAL field is written with the correct value. Aside from EEPROM margining, this field returns 0x00 on completion.

Value	Description
0001	Enable EEPROM low voltage margin. IC must be unlocked.
0010	Enable EEPROM high voltage margin. IC must be unlocked.
0011	Turns counter load from EWD. Starts after writing 0x46 to INITIATE_SPECIAL. For a detailed description, see the Setting the Turns Count Value section.
0100	Turns counter reset. Starts after writing 0x46 to INITIATE_SPECIAL.
0101	Reload EEPROM. Requires IC to be unlocked. Starts after writing 0xA5 to INITIATE_SPECIAL.
0111	Hard reset. Requires unlock of part. Starts after writing 0x5A to INITIATE_SPECIAL.
1001	Run CVH self-test. Starts after writing 0xB9 to INITIATE_SPECIAL.
1010	Run Logic BIST. Starts after writing 0xB9 to INITIATE_SPECIAL.
1011	Run both CVH self-test and logic BIST. Tests are run in parallel. Starts after writing 0xB9 to INITIATE_SPECIAL.
1100	Force error conditions(s) using EWD (EWDH = ERR, EWDL = WARN). Starts after writing 0x67 to INITIATE_SPECIAL.
1101	Resample PWM errors (errors must have cleared for this to have an effect).
1110	Clear fatal PWM errors (EUE, WDE, STE)
1111	Clear fatal and resample all PWM errors

SPO [11]

SPI override bit. When set to 1, MISO is forced to be a SPI output. This overrides PWM and SENT.

Value	Description
0	Clears SPI override
1	MISO set to SPI output. Overrides SENT/PWM operation

CLS [10]

Clear status register bits SDN and BDN, when set to 1.
STA.SDN indicates that a “special access” task (i.e., CVH self-test) has completed.
STA.BDN indicates the IC has booted properly and completed any start-up self-tests.

CLW [9]

Clear warning (WARN) register when set to 1.
Clears bits that were previously read from the WARN (register 0x26:0x27).
Write-only, always returns 0.

CLE [8]

Clear error (ERR) register when set to 1.
Clears bits that were previously read from the ERR (register 0x24:25).
Write-only, always returns 0.

INITIATE_SPECIAL [7:0]

Write after setting certain CTRL.SPECIAL bits to initiate the selected action(s).
Always returns zeroes.

Value	Description
0xB9	Initiate self-tests
0x46	Initiate turns counter reset
0x5A	Initiate hard reset
0xA5	Initiate EEPROM reload

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Address 0x20:0x21 (ANG)—Current Angle Reading (12 bits)

Address	0x20								0x21							
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	0	EF	UV	P	ANGLE											
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

EF [14]

Error flag. If value is 1, an unmasked bit is set in ERR or WARN.

Value	Description
0	No unmasked errors
1	Unmasked error is present

UV [13]

Undervoltage flag (real time). Logical OR of analog and digital UV flags (UVD and UVA flags). Conditions are real time but may be masked by EEPROM error mask bits.

Value	Description
0	No undervoltage condition detected
1	Undervoltage condition detected

P [12]

Parity bit. Odd parity is calculated across all bits (EF, UV, ANGLE). As a result, there should always be an odd number of ones in this 16-bit word.

ANGLE [11:0]

Angle from PLL after processing.
Angle in degrees is 12-bit value × (360/4096).

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Address 0x22:0x23 (STA)—Device Status

Address	0x22								0x23							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	1	0	0	0	0	0	DIE_ID		ROT	0	SDN	BDN	LBR	CSTR	BIP	AOK
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

RIDC [15:12]

Register ID bits. Used to distinguish these registers from other serial registers. Hard-coded value.

Value	Description
1000	Register ID value

DIE_ID [9:8]

Die identifier, loaded from EEPROM (for multi-die packages). Used for identification purposes only. No impact on sensor functionality.
Set in factory by Allegro.

ROT [7]

Indicates observed rotation direction, based on the hysteresis logic. Valid only if hysteresis is enabled (see EEPROM 0x1C).

Value	Description
0	Increasing angles
1	Decreasing angles

SDN [5]

Special access (from CTRL register) done. Clears to 0 when a “special command” is triggered; sets to 1 when complete. Can clear with CTRL.CLS bit = 1.

Value	Description
0	“Special” command in progress, unless cleared previously
1	“Special” command completed

BDN [4]

Boot complete. EEPROM loaded and any startup self-tests are complete. Can clear with CTRL.CLS bit = 1.

Value	Description
0	Boot not complete, unless cleared previously.
1	Boot complete

LBR [3]

Logic BIST (LBIST) running.

Value	Description
0	LBIST not running
1	LBIST running

CSTR [2]

CVH self-test running.

Value	Description
0	CVH self-test not running
1	CVH self-test running

BIP [1]

Boot in progress. Output values may not be valid.

Value	Description
0	Boot not in progress
1	Sensor is undergoing its boot sequence

AOK [0]

Angle output is OK. Indicates the PLL is locked, and start-up sequence has completed.

Value	Description
0	Angle is not valid
1	PLL is locked, angle value is valid

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Address 0x24:0x25 (ERR)—Device Error Flags

This is the error register. All errors are latched, meaning they remain high after they occur. To remove an error, it must be read, then cleared. It is important that the user clears errors so that subsequent errors become visible. This is especially important for the RST error flag (reset), which is always enabled after power-on. Failure to remove an error creates a condition where an unexpected reset cannot be discovered afterward.

Address	0x24								0x25							
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	1	0	1	0	WAR	STF	AVG	0	PLK	ZIE	EUE	WDE	UVD	UVA	MSL	RST
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

RIDC [15:12]

Register ID bits. Used to distinguish these registers from other serial registers. Hard-coded value.

Value	Description
1010	Register ID value

WAR [11]

Warning. An unmasked bit within the WARN register is asserted.
May be masked by setting MSK.WAR bit in EEPROM.

Value	Description
0	No unmasked flag set in the WARN register (0x26:27)
1	Unmasked flag set in the WARN register

STF [10]

Self-test failure. Indicates either LBIST or CVH self-test failed.

Value	Description
0	No self-test failure
1	Self-test failure

AVG [9]

Angle averaging error. Indicates the ORATE value is too high for the rotation velocity, and the averaged angle value is corrupted.
The ORATE setting allows multiple angle values to be averaged together, for improved precision. This reduces the response time of the sensor and can result in corrupted angle values if the velocity is too high.

Value	Description
0	No Averaging error
1	Averaging error

PLK [7]

PLL lost lock. This indicates the PLL is not tracking the incoming angle properly. Angle value has been corrupted.

Value	Description
0	No PLL lock.
1	PLL lost lock. Angle value invalid.

ZIE [6]

Zero-crossing integrity error. A zero-crossing did not occur within the maximum time expected, likely indicating a missing magnet or extreme rotation.

Value	Description
0	No zero-crossing error
1	Zero-crossing error

EUE [5]

EEPROM uncorrectable error. A multibit EEPROM read occurred. EEPROM bit errors are only checked on EEPROM load (i.e., power-up or reset).

Value	Description
0	No multibit EEPROM error
1	Multibit EEPROM error

WDE [4]

Oscillator watchdog error. One of the oscillator watchdogs circuits monitoring the high-frequency and low-frequency oscillators has tripped.

Value	Description
0	No oscillator error
1	Oscillator watchdog error

UVD [3]

VCC undervoltage detector tripped. Continues to set until fault goes away (and ERR register is cleared). This is the VCC input pin voltage.

Value	Description
0	No VCC voltage error
1	VCC undervoltage error detected

UVA [2]

Undervoltage detector tripped. Continues to set until fault goes away (and ERR register is cleared). This is the analog regulator output.

Value	Description
0	No voltage error
1	Voltage error on the analog regulator output

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MSL [1]

Magnetic sense low fault. Magnetic sense was below the low limit threshold.
Low limit threshold is set via the COM.MAG_THRES_LO field in EEPROM.
By default, this is set to ≈200 G.

Value	Description
0	No magnetic field low fault
1	Magnetic field lower than threshold

RST [0]

Reset condition. Sets on power-on reset or hard reset. Does not set on LBIST. Indicates volatile registers have been reinitialized.

Value	Description
0	No reset
1	Device has been reset. Volatile registers are reinitialized.

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Address 0x26:0x27 (WARN)—Device Warning Flags

This is the warning register. All warnings are latched, meaning they remain high after they occur. To remove warnings, they must be read, then cleared. Warnings indicate either communication-type conditions or conditions that may result in a degradation of the angle accuracy but are less likely than errors to indicate a corruption of the angle.

Address	0x26								0x27							
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	1	0	1	1	IER	CRC	SEN	0	XEE	TR	ESE	SAT	TCW	BSY	MSH	TOV
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

RIDC [15:12]

Register ID bits. Used to distinguish these registers from other serial registers. Hard-coded value.

Value	Description
1011	Register ID value

IER [11]

Interface error. Invalid number of bits in SPI packet, or bit 15 of MOSI data = 1. Packet was discarded.
Also indicates a Manchester error.

Value	Description
0	No Interface Error
1	Interface Error

CRC [10]

Incoming SPI CRC error. Packet was discarded.
Incoming CRC is only checked if the PWI.SC bit in EEPROM is set.

Value	Description
0	No incoming SPI CRC error
1	Incoming SPI CRC is bad

SEN [9]

SENT contention or slot marking (sequential SENT) error.

Value	Description
0	No SENT contention error
1	SENT contention detected

XEE [7]

Extended execute error. A command initiated by an extended write failed. Write failed due to access error (not unlocked) or EEPROM write failure.

Value	Description
0	No incoming extended error
1	Extended execute error

TR [6]

Temperature out of range. The temperature sensor calculated a temperature below –60°C or above 180°C. Temperature saturates at those limits.

Value	Description
0	Temperature sensor in range
1	Sensed temperature is below –60° or above 180°C

ESE [5]

EEPROM soft error. A correctable (single bit) EEPROM read occurred. EEPROM bit errors are only checked on EEPROM load (power-on or reset).

Value	Description
0	No single bit EEPROM error
1	EEPROM single bit error detected and corrected

SAT [4]

Aggregate saturation flag. Shows that any internal signals have saturated, likely caused by extremely strong or weak fields.

Value	Description
0	No saturation detected within the signal chain
1	Saturation conditions detected within the signal chain

TCW [3]

Turns counter warning. Over 135° of angle change between updates of the turns counter (updated every ≈64µs).

Value	Description
0	No turns count warning
1	Angle difference between two update periods of the turns counter is >135°

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BSY [2]

Extended access overflow. An extended write or extended read was initiated before the previous one was complete.

Value	Description
0	No extended access error
1	extended access error

MSH [1]

Magnetic sense high fault. Magnetic sense was above the high limit threshold.
High limit threshold is set via the COM.MAG_THRES_HI field in EEPROM.
By default, this is set to ≈1344 G.

Value	Description
0	No magnetic field high fault
1	Magnetic field above threshold

TOV [0]

Turns counter overflow error.
The turns counter surpassed its maximum value of +255/–256 full rotations.
This is equivalent to a Turns register value of ±511/–512 or +2047/–2048, depending on the resolution (180° or 45°).

Value	Description
0	No turns count overflow error
1	Turns count overflow error

Address 0x28:0x29 (TSEN)—Temperature Sensor

Address	0x28								0x29							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	1	1	1	1	TEMPERATURE											
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

RIDC [15:12]

Register ID bits. Used to distinguish these registers from other serial registers. Hard-coded value.

Value	Description
1111	Register ID value

TEMPERATURE [11:0]

Current junction temperature from internal temperature sensor relative to room temperature (signed value, 2's complement). Value is in 1/8 of a degree. Temperature °C ≈ (TSEN.TEMPERATURE / 8) + 25.

Address 0x2A:0x2B (FIELD)—Field Strength (in gauss)

Address	0x2A								0x2B							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	1	1	1	0	GAUSS											
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

RIDC [15:12]

Register ID bits. Used to distinguish these registers from other serial registers. Hard-coded value.

Value	Description
1110	Register ID value

GAUSS [11:0]

Measured field strength in gauss. Updated every 128 µs.

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Address 0x2C:0x2D (TURNS)—Turns Counter

Address	0x2C								0x2D							
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	1	1	TSCR	P	TURNS											
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

RIDC [15:14]

Register ID bits. Used to distinguish these registers from other serial registers. Hard-coded value.

Value	Description
11	Register ID value

TOV [0]

Turns counter overflow error.
The turns counter surpassed its maximum value of +255/–256 full rotations.
This is equivalent to a TURNS register value of ±511/–512 or +2047/–2048, depending on the resolution (180° or 45°).

Value	Description
0	No turns count overflow error
1	Turns count overflow error

P [12]

Parity bit. Odd parity is calculated across all bits (EF, UV, TURNS). As a result, there should always be an odd number of ones in this 16-bit word.

TURNS [11:0]

Signed 2's complement value. Indicates total number of turns relative to angle observed on power-up. Turns resolution set via EEPROM to either 180° or 45°.
The A33002 is capable of tracking up to 256 full mechanical rotations, independent of the resolution selected.

Bit Value	Turns in 180° mode (Actual mechanical full rotations)	Turns in 45° mode (Actual mechanical full rotations)
0000 0000 0000	0 (0)	0 (0)
0000 0000 0001	+1 (+1/2)	+1 (+1/8)
0001 1111 1111	+511 (255.5)	+511 (+63.875)
0010 0000 0000	–	+512 (+64)
0111 1111 1111	–	+2047(+255.875)
1111 1111 1111	–1 (–1/2)	–1 (–1/8th)
1110 0000 0000	–512 (–256)	–512 (–64)
1000 0000 0000	–	–2048 (–256)

The TURNS field contains the most significant bits of the TURNS_DELTA value. When in 45° mode (LPC.T45 = 1), the TURNS field represents bits 20:9 (highest 12 bits) of the TURNS_DELTA value. When in 180° mode (LPC.T45 = 0), the TURNS field is the sign-extended representation of bits 20:11 (highest 10 bits) of the TURNS_DELTA value. TOFF.TURNS_OFFSET (serial register 0x2E:0x2F) represents the lower bits of the TURNS_DELTA value. This value is latched when reading the TURNS field.

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Address 0x2E:0x2F (TOFF)—Turns Offset

Address	0x2E								0x2F							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	1	LAT	0	P	0	TURNS_OFFSET										
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

RIDC [15]
Register ID bits. Used to distinguish these registers from other serial registers. Hard-coded value.

Value	Description
1	Register ID value

LAT [14]

Indicates if the TURN_OFFSET field is latched.
If 1, indicates the TURNS_OFFSET value was latched on an earlier read of the turns register (0x2C:2D), and is consistent with that reading.
Returns 0 after reading.

Value	Description
0	TURNS_OFFSET value not latched
1	TURNS_OFFSET value latched on an earlier read of TRNS.TURNS.

P [12]

Parity bit. Odd parity is calculated across all bits (EF, UV, TURNS). As a result, there should always be an odd number of ones in this 16-bit word.

TURNS_OFFSET [10:0]

Either the 11 or 9 lowest bits of the TURNS_DELTA value, based on the LPC.T45 setting.

Address 0x30:0x31 (HANG)—Hysteresis Angle Value (12 bits)

Address	0x30								0x31							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	EF	UV	P	ANGLE_HYS											
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

EF [14]

Error flag. If 1, an unmasked bit is set in ERR or WARN.

Value	Description
0	No unmasked errors
1	Unmasked error is present

UV [13]

Undervoltage flag (real time). Logical OR of analog and digital UV flags (UVD and UVA flags). Conditions are real time but may be masked by EEPROM error mask bits.

Value	Description
0	No undervoltage condition detected
1	Undervoltage condition detected

P [12]

Parity bit. Odd parity is calculated across all bits (EF, UV, ANGLE_HYS). As a result, there should always be an odd number of ones in this 16-bit word.

ANGLE_HYS [11:0]

Angle from PLL after hysteresis processing.
Angle in degrees is 12-bit value × (360/4096).

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Address 0x32:0x33 (ANG15)—Current Angle Reading (15 bits)

Address	0x32								0x33							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	ANGLE_15														
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

ANGLE_15 [14:0]

15-bit compensated angle (not rounded).
Angle in degrees is a 15-bit value × (360/32768)

Address 0x34:0x35 (ZANG)—ZCD Angle (low power signal path)

Angle from the ZCD signal path; used for turns counter. This angle is not compensated over temperature and does not exactly match the PLL angle value.

Address	0x34								0x35							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	EF	UV	P	ANGLE_ZCD											
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

EF [14]

Error flag. If 1, an unmasked bit is set in ERR or WARN.

Value	Description
0	No unmasked errors
1	Unmasked error is present

UV [13]

Undervoltage flag (real time). Logical OR of analog and digital UV flags (UVD and UVA flags). Conditions are real time but may be masked by EEPROM error mask bits.

Value	Description
0	No undervoltage condition detected
1	Undervoltage condition detected

P [12]

Parity bit. Odd parity is calculated across all bits (EF, UV, ANGLE_ZCD). As a result, there should always be an odd number of ones in this 16-bit word.

ANGLE_ZCD [11:0]

Angle from the ZCD signal path. Not compensated.
Angle in degrees is 12-bit value × (360/4096).

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Address 0x36:0x37 (TD_HIGH)—Turns Delta (high)

Represents the upper bits of the 21-bit, signed, TURNS_DELTA value. When read, the contents of TD_LOW (address 0x38:39) are latched and the TD_LOW.LAT bit is set. This allows all 25 bits (sign-extended) of the TURNS_DELTA value to be read at the same timestamp.
The TURNS_DELTA value represents the absolute angle position, in 12-bit resolution, from a set reference point. For a detailed discussion, refer to the Turns Counting section.

Address	0x36								0x37							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	EF	TSRC	P	TURNS_DELTA_HIGH											
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

EF [14]
Error flag. If 1, an unmasked bit is set in ERR or WARN.

Value	Description
0	No unmasked errors
1	Unmasked error is present

TSCR [13]

Turns source. Selects the signal path used to determine turns. Switches between the ZCD and PLL paths.

Value	Description
0	Turns counting uses ZCD signal path
1	Turns counting uses PLL signal path (recommended)

P [12]

Parity bit. Odd parity is calculated across all bits (EF, UV, ANGLE_ZCD). As a result, there should always be an odd number of ones in this 16-bit word.

TURNS_DELTA_HIGH [11:0]

Upper 9 bits (sign extended to 12) of the TURNS_DELTA value.
When read, contents of TD_LOW are latched.

Address 0x38:0x39 (TD_LOW)—Turns Delta (low)

Represents the lower bits of the 21-bit, signed, TURNS_DELTA value. Value is latched when reading the TD_HIGH register. This allows all 25 bits (sign-extended) of the TURNS_DELTA value to be read at the same timestamp.
The TURNS_DELTA value represents the absolute angle position, in 12-bit resolution, from a set reference point. For a detailed discussion, refer to the Turns Counting section.

Address	0x38								0x39							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	EF	LAT	P	TURNS_DELTA_LOW											
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

EF [14]

Error flag. If 1, an unmasked bit is set in ERR or WARN.

Value	Description
0	No unmasked errors
1	Unmasked error is present

P [12]

Parity bit. Odd parity is calculated across all bits (EF, UV, ANGLE_ZCD). As a result, there should always be an odd number of ones in this 16-bit word.

TURNS_DELTA_LOW [11:0]

Lower 12 bits of the TURNS_DELTA value. Latched on a read of the TURNS_DELTA_HIGH register.

LAT [13]

Indicates if the TURN_DELTA_LOW field is latched.
If 1, indicates the value was latched on an earlier read of TURNS_OFFSET_HIGH (0x36:37) and is consistent with that reading.
Return is 0 after reading.

Value	Description
0	TURN_DELTA_LOW value not latched
1	TURN_DELTA_LOW value latched on an earlier read of TD_HIGH.TURNS_DELTA_HIGH

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Address 0x3A:0x3B (PTANG)—PLL Turns Angle

This is the angle from the PLL signal path that will be used for turns counting (if LPC.TCP = 1 in EEPROM). This value differs from the standard PLL angle value (ANG.ANGLE) in that it may have hysteresis applied (controlled by the PWI.H2T bit in EEPROM).

Address	0x3A								0x3B							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	EF	UV	P	PLL_TURNS_ANGLE											
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

EF [14]

Error flag. If 1, an unmasked bit is set in ERR or WARN.

Value	Description
0	No unmasked errors
1	Unmasked error is present

UV [13]

Undervoltage flag (real time). Logical OR of analog and digital UV flags (UVD and UVA flags). Conditions are real time but may be masked by EEPROM error mask bits.

Value	Description
0	No undervoltage condition detected
1	Undervoltage condition detected

P [12]

Parity bit. Odd parity is calculated across all bits (EF, UV, ANGLE_ZCD). As a result, there should always be an odd number of ones in this 16-bit word.

PLL_TURNS_ANGLE [11:0]

Angle from the PLL signal path (compensated) to be used for turns counting (if enabled in EEPROM). Has hysteresis based on the PWI.H2T EEPROM setting.
Angle in degrees is 12-bit value × (360/4096).

Address 0x3C:0x3D (KEY)—Key Register

Address	0x3C								0x3D							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	KEYCODE								0	0	0	0	0	0	0	CUL
R/W	W	W	W	W	W	W	W	W	R	R	R	R	R	R	R	R

KEYCODE [15:8]

Unlock code is entered here. Device must be unlocked to write to EEPROM/shadow and to perform various “special” actions (such as EEPROM margin testing).
Always reads back 0.
To unlock device, write the following values to the KEYCODE field in successive writes.

Code (Hex)
0x27
0x81
0x1F
0x77

CUL [0]

Indicates the device is unlocked.

Value	Description
0	Device is not unlocked
1	Device is unlocked

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EEPROM TABLE

The EEPROM register bitmap is shown in Table 20.

All EEPROM content can be read by the user. The EEPROM ECC field in bits [31:26] of each word are not shown here.

All unallocated EEPROM fields (those not specifically discussed) should not be altered from their default value, as shipped from Allegro.

Table 20: EEPROM / Shadow Memory Map

EEPROM Address	Shadow Memory Address	Register Name	Bits																									
			25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x17	0x57	CU2	-x-	-x-	CUSTOMER 2																							
0x18	0x58	PWE	-x-	-x-	ZCD_TURNS_OFFSET											TOV	TR	MSH	SAT	ESE	MSL	UV	AVG	ZIE	PLK	STF	EUE	WDE
0x19	0x59	SEN	MAXID		SS	SENT_TICK							SM	SENT_MODE			DATA_MODE				CIS	SCN_MODE			NS	ZS	DA	FA
0x1A	0x5A	MSK	-x-	-x-	IERM	CRCM	SENM	-X-	XEEM	TRM	ESEM	SATM	TCWM	BSYM	MSHM	TOVM	WARM	STFM	AVGM	-X-	PLKM	ZIEM	EUEM	WDEM	UVCCM	UVAM	MSLM	RSTM
0x1B	0x5B	PWI	FP_ADJ		PEN	PWM_BAND			PWM_FREQ				-X-	PHE	PEO	PES	ELI	LS	ZAL	IS	PO	SDRV			DM	H2T	S17	SC
0x1C	0x5C	ANG	-x-	-x-	ORATE				RD	RO	HYSTERESIS						ZERO_OFFSET											
0x1D	0x5D	LPC	-x-	-x-	T45	TCP	-X-	-X-	TURNS_INIT		-X-						-X-	-X-										
0x1E	0x5E	COM	-x-	-x-	LOCK				LBE	CSE	DUR	DEL	-X-	CUD	DST	DHR	MAG_THRES_HI					MAG_THRES_LO						
0x1F	0x5F	CUS	-x-	-x-	CUSTOMER																							
0x20	0x60	LIN	-x-	-x-	LINEARIZATION ERROR SEGMENT 1												LINEARIZATION ERROR SEGMENT 0											
0x21	0x61	LIN	-x-	-x-	LINEARIZATION ERROR SEGMENT 3												LINEARIZATION ERROR SEGMENT 2											
…	…	…	-x-	-x-	…												---											
0x2E	0x6E	LIN	-x-	-x-	LINEARIZATION ERROR SEGMENT 29												LINEARIZATION ERROR SEGMENT 28											
0x2F	0x6F	LIN	-x-	-x-	LINEARIZATION ERROR SEGMENT 31												LINEARIZATION ERROR SEGMENT 30											

EEPROM REFERENCE

Address 0x17 (CU2)—Customer EEPROM Scratch Pad (2)

Customer EEPROM space.
This word can be written if EEPROM is locked and without the need to unlock the IC. Access is based on settings of COM.DEL, COM.DUR, and COM.CUD (see EEPROM address 0x1E).

Bit	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CUSTOMER 2																							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Address 0x18 (PWE)—PWM Error Enable

This address space contains the PWM error enable bits. When set to 1, the PWM output responds to errors, as set via the PWI.PEO and PWI.PES bits. Address also contains the ZCD offsets field, allowing the ZCD angle to be adjusted for turns counting.

Bit	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ZCD_TURNS_OFFSET											TOV	TR	MSH	SAT	ESE	MSL	UV	AVG	ZIE	PLK	STF	EUE	OFE
Default	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1

ZCD_TURNS_OFFSET [23:13]

Offset to the ZCD angle for purpose of aligning turns counting. This 11-bit angle resolution is added to the ZCD angle for turns purposes.

TOV [12]

PWM turns counter overflow error enable.
Duty cycle 72.5%, if PWI.PEO and PWI.PES are 1.

Value	Description
0	PWM does not respond to a TOV error
1	PWM output respond to a TOV error

TR [11]

PWM temperature out of range error enable.
Duty cycle 66.875%, if PWI.PEO and PWI.PES are 1.

Value	Description
0	PWM does not respond to a TR error
1	PWM output respond to a TR error

MSH [10]

PWM magnetic sense high error enable.
Duty cycle 61.25%, if PWI.PEO and PWI.PES are 1.

Value	Description
0	PWM does not respond to an MSH error
1	PWM output respond to an MSH error

SAT [9]

PWM saturation error enable.
Duty cycle 55.625%, if PWI.PEO and PWI.PES are 1.

Value	Description
0	PWM does not respond to an SAT error
1	PWM output respond to an SAT error

ESE [8]

PWM EEPROM soft error enable.
Duty cycle 50%, if PWI.PEO and PWI.PES are 1.

Value	Description
0	PWM does not respond to an ESE error
1	PWM output respond to an ESE error

MSL [7]

PWM magnetic sense low error enable.
Duty cycle 44.375%, if PWI.PEO and PWI.PES are 1.

Value	Description
0	PWM does not respond to an MSL error
1	PWM output respond to an MSL error

UV [6]

PWM undervoltage error enable.
Duty cycle 38.75%, if PWI.PEO and PWI.PES are 1.

Value	Description
0	PWM does not respond to a UV error
1	PWM output respond to a TOV error

AVG [5]

PWM averaging error enable.
Duty cycle 33.125%, if PWI.PEO and PWI.PES are 1.

Value	Description
0	PWM does not respond to an AVG error
1	PWM output respond to a TOV error

ZIE [4]

PWM zero-crossing error enable.
Duty cycle 27.5%, if PWI.PEO and PWI.PES are 1.

Value	Description
0	PWM does not respond to a ZIE error
1	PWM output respond to a ZIE error

PLK [3]

PWM PLL lost lock error enable.
Duty cycle 21.875%, if PWI.PEO and PWI.PES are 1.

Value	Description
0	PWM does not respond to a PLK error
1	PWM output respond to a PLK error

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STF [2]

PWM self-test error enable.
Duty cycle 16.25%, if PWI.PEO and PWI.PES are 1.

Value	Description
0	PWM does not respond to an STF error
1	PWM output respond to an STF error

EUE [1]

PWM EEPROM uncorrectable error enable.
Duty cycle 10.625%, if PWI.PEO and PWI.PES are 1.

Value	Description
0	PWM does not respond to an EUE error
1	PWM output respond to an EUE error

OFE [0]

PWM oscillator frequency error enable.
Duty cycle 5%, if PWI.PEO and PWI.PES are 1.

Value	Description
0	PWM does not respond to an OFE error
1	PWM output respond to an OFE error

Address 0x19 (SEN)—SENT Control

This address contains the majority of SENT configuration parameters. For further details, refer to the SENT description in Appendix A: SENT Output Description.

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAXID		SS	SENT_TICK							SM	SENT_MODE			DATA_MODE				CIS	SCN_MODE			NS	ZS	DA	FA
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MAXID [25:24]

For SSENT (SENT_MODE = 6 and SENT_MODE = 7). Defines the highest address on the bus, after which the internal slot counter wraps back to 0.

Value	Description
0	1 IC on the bus
1	2 ICs on the bus
2	3 ICs on the bus
3	4 ICs on the bus

SS [23]

Slot sync. For SSENT only. Allows the sensor to synchronize to the bus after a reset based on other sensor slot marking. Only valid if SM = 1.

Value	Description
0	Slot sync disabled. Sensor remains off the bus after a reset.
1	Slot sync enabled.

SENT_TICK [22:16]

SENT tick time, N × period of 16 MHz clock (forced to minimum of two clocks internally). Tick times shorter than 0.5 µs are not guaranteed.

Value (Binary)	Description
000 0000	0.125 µs tick time
000 0001	0.125 µs tick time
000 0010	0.125 µs tick time
000 0011	0.1875 µs tick time
…	…
000 1000	0.5 µs tick time
…	…
001 0000	1.0 µs tick time
…	…
001 1000	1.5 µs tick time
…	…
011 0000	3 µs tick time
…	…
111 1111	7.9375 µs tick time

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SM [15]

Slot marking. SSENT only.
Delay time, after an addressing pulse, is set based on IC address value. This allows differentiation of the addressed IC on the bus. Can be used in conjunction with SLOT_SYNC (SS), allowing an IC to resynchronize its slot counter following a reset.

Value	Description
0	Slot marking disabled
1	Slot marking enabled

SENT_MODE [14:12]

Selects between the various SENT operating modes. For further details, refer to Appendix A: SENT Output Description.

Value (Binary)	Description
000	SENT disabled
001	Streaming SENT. No pause pulse between frames
010	Streaming SENT. Pause pulse inserted to synchronize frame with angle update
011	Triggered SENT (TSENT). Data sampled just before data nibbles (end of SCN)
100	Triggered SENT (TSENT). Data latched on falling edge of trigger (after minimum width)
101	Addressable SENT (ASENT)
110	Sequential SENT (SSENT)
111	Long SSENT

NOTE: If PEN = 1, then PWM has precedence and SENT is disabled.

NOTE: If both PWM and SENT are disabled, MISO output is SPI (unless Manchester is active).

DATA_MODE [11:8]

Selects the quantity and content of data nibbles within the SENT message frame. For further details, refer to Appendix A: SENT Output Description.

Value (Binary)	Description
0000	Angle only (3 data nibbles)
0001	Angle (3) + rotating status (2)
0010	Angle (3) + rotating data (3)
0011	Angle (3) + turns (3)
0100	Angle (3) + rotating status (2) + alive (1)
0101	Angle (3) + alive (2) + ~first nibble (1) (secure sensor format)
0110	Angle16 (4)
0111	Angle16 (4) + rotating status (1) + alive (1)
1000	Angle (3) + ID (1)
1001	Angle (3) + rotating status (2) + ID (1)
1010	Angle (3) + rotating data (2) + ID (1)
1011	Angle (3) + rotating turns (2) + ID (1)
1100	Angle (3) + rotating status (1) + alive (1) + ID (1)
1101	Angle (3) + alive (1) + ~first nibble (1) + ID(1)
1110	Angle16 (4) + ID (1)
1111	Angle16 (4) + alive (1) + ID (1)

CIS [7]

CRC includes SCN nibble.
This bit allows the SENT frame CRC to cover the contents of the status and communication nibble (SCN)

Value	Description
0	SCN contents not included in the SENT frame CRC
1	SCN contents covered via the CRC nibble (does not conform with the SAE J2716 SENT standard)

SCN_MODE [6:4]

Defines contents of the status and communication nibble.

Value (Binary)	Bit 4	Bit 3	Bit 2	Bit 0
000	0	0	Soft Error	Hard Error
001	Serial msg sync	Serial msg data	Soft Error	Hard Error
010	ID[1]	ID[0]	Soft Error	Hard Error
011	0	0	0	Soft | Hard
100	0	0	ID[1]	ID[0]
101	Serial msg sync	Serial msg data	ID[1]	ID[0]
110	Soft Error	Hard Error	ID[1]	ID[0]
111	Serial msg sync	Serial msg data	0	Soft | Hard

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NS [3]

No sample.
If 1, the F_SAMPLE pulse does not perform a sample-and-hold.

Value	Description
0	On receipt of an F_SAMPLE pulse, sensor samples and holds angle data
1	Sensor does not sample and hold data on receipt of an F_SAMPLE pulse

ZS [2]

Zero sample. SSENT only.
If 1, the IC performs a sample-and-hold on slot 0.

Value	Description
0	No special action on slot = 0
1	Sensor performs a sample-and-hold when its slot counter resets to 0

DA [1]

Diagnostic addressing.
Allows the F_DIAG pulse to be treated as an addressing.

Value	Description
0	F_DIAG is treated as a broadcast pulse. Sensor enters diagnostic mode on any F_DIAG pulse.
1	F_DIAG is treated as an addressing pulse. Sensor enters diagnostic mode if properly addressed.

FA [0]

F_SAMPLE addressing.
Sensor treats the F_SAMPLE pulse as an addressing pulse.

Value	Description
0	F_SAMPLE is treated as a broadcast pulse. Sensor sample-and-hold angle data on any F_SAMPLE pulse (unless ns = 1)
1	F_SAMPLE is treated as an addressing pulse. Sensor only samples-and-holds angle data on an F_SAMPLE pulse if properly addressed (unless NS = 1).

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Address 0x1A (MSK)—Mask Bits

This address range contains error mask bits. When set, the applicable error condition does not assert the EF bit in the various angle and turns count registers. Errors/warning are still visible by reading serial registers 0x24 and 0x26.
Masks also prevent SENT soft error flags from asserting. SENT hard error flags assert independent of mask bits.

Bit	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IER	CRC	SEN	–	XEE	TR	ESE	SAT	TCW	BSY	MSH	TOV	WAR	STF	AVG	–	PLK	ZIE	EUE	WDE	UVD	UVA	MSL	RST
Default	0	0	0	–	0	0	0	0	0	0	0	0	0	0	0	–	1	0	0	0	0	0	0	0

IER [23]
Masks the IER flag from setting the EF bit.

CRC [22]
Masks the CRC flag from setting the EF bit.

SEN [21]
Masks the SEN flag from setting the EF bit.

XEE [19]
Masks the XEE flag from setting the EF bit.

TR [18]
Masks the TR flag from setting the EF bit.

ESE [17]
Masks the ESE flag from setting the EF bit.

SAT [16]
Masks the SAT flag from setting the EF bit.

TCW [15]
Masks the TCW flag from setting the EF bit.

BSY [14]
Masks the BSY flag from setting the EF bit.

MSH [13]
Masks the MSH flag from setting the EF bit.

TOV [12]
Masks the TOV flag from setting the EF bit.

WAR [11]
Masks the WAR flag from setting the EF bit.

STF [10]
Masks the STF flag from setting the EF bit.

AVG [9]
Masks the AVG flag from setting the EF bit.

PLK [7]
Masks the PLK flag from setting the EF bit.

If using SENT, this bit must be set to 1. This prevents spurious errors. A PLK error is still reported as a “hard” error.

If using SPI, this bit must be set to 0 (unmasking the flag). This allows proper reporting of a PLL loss of lock.

ZIE [6]
Masks the ZIE flag from setting the EF bit.

EUE [5]
Masks the EUE flag from setting the EF bit.

WDE [4]
Masks the OFE flag from setting the EF bit.

UVD [3]
Masks the UVD flag from setting the EF bit.

UVA [2]
Masks the UVA flag from setting the EF bit.

MSL [1]
Masks the MSL flag from setting the EF bit.

RST [0]
Masks the RST flag from setting the EF bit.

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Address 0x1B (PWS)—PWM Interface Control

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FP_ADJ		PEN	PWM_BAND			PWM_FREQ				–	PHE	PEO	PES	ELI	LS	ZAL	IS	PO	SDRV			DM	H2T	S17	SC
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FP_ADJ [25:24]

Function pulse adjust. For SENT_MODE 7 only (long SSENT). Increases the lower threshold of the F_OUTPUT pulse by number of ticks in this field (0 to 3).
If using fast tick times (less than 1.5 µs), this adjustment may be necessary to prevent the IC from interpreting the SENT low period as a function pulse. All devices sharing a bus should be configured with matching settings.

Value	Description
0	F_OUTPUT minimum is 9 ticks
1	F_OUTPUT minimum is 10 ticks
2	F_OUTPUT minimum is 11 ticks
3	F_OUTPUT minimum is 12 ticks

PWM_BAND [22:20]

PWM frequency band. Defines the PWM carrier frequency when combined with PWM_FREQ.

Value	Description
0	Slot sync disabled. Sensor remains off the bus after a reset.
1	Slot sync enabled.

PEN [23]

PWM enable.

Value	Description
0	PWM is disabled. SENT may be enabled based on the SENT_MODE field
1	PWM enabled, output on MISO. SENT is disabled, independent of SENT_MODE.

NOTE: If both PWM and SENT are disabled, MISO is SPI output.

PWM_FREQ [19:16]

PWM frequency select. Defines the PWM carrier frequency when combined with PWM_BAND.

PHE [14]

PWM/SENT hysteresis enable.

Value	Description
0	No hysteresis applied to PWM/SENT output
1	Hysteresis settings applied to PWM/SENT output

Table 21: Nominal PWM Carrier Frequencies (Hz)

		PWM_BAND							
		0	1	2	3	4	5	6	7
PWM_FREQ	0	3125	2778	2273	1667	1087	641	352	185
	1	3101	2740	2222	1613	1042	610	333	175
	2	3077	2703	2174	1563	1000	581	316	166
	3	3053	2667	2128	1515	962	556	301	157
	4	3030	2632	2083	1471	926	532	287	150
	5	3008	2597	2041	1429	893	510	275	143
	6	2985	2564	2000	1389	862	490	263	137
	7	2963	2532	1961	1351	833	472	253	131
	8	2941	2500	1923	1316	806	455	243	126
	9	2920	2469	1887	1282	781	439	234	121
	10	2899	2439	1852	1250	758	424	225	116
	11	2878	2410	1818	1220	735	410	217	112
	12	2857	2381	1786	1190	714	397	210	108
	13	2837	2353	1754	1163	694	385	203	105
	14	2817	2326	1724	1136	676	373	197	101
	15	2797	2299	1695	1111	658	362	191	98

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PEO [13]

PWM error output enable. If 1, PWM responds to errors as defined by the PES bit.

Value	Description
0	PWM output does not respond to error flags
1	PWM output responds to errors as defined by the PWI.PES field

PES [12]

PWM error select, if PEO = 1.

Value	Description
0	PWM output tristates for all enabled error conditions (See PWE address space)
1	For all enabled errors, the PWM carrier frequency is halved, and the highest-priority error is identified by a specific duty cycle.

ELI [11]

Enable linearization.

Value	Description
0	Linearization disabled
1	Linearization enabled

LS [10]

Linearization scale. Selects the maximum error that each linearization EEPROM field represents.

Value	Description
0	±22.5°
1	±45°

ZAL [9]

Zero offset after linearization. Controls where, relative to linearization, the ANG.ZERO_OFFSET value is applied.

Value	Description
0	Offset applied before linearization and rotation
1	Offset applied after linearization

IS [8]

Idle sync. SSENT (SENT_MODE 6 and 7) only.
When 1, if the SENT bus is idle for more than 511 ticks, resets the slot counter to 0.

Value	Description
0	No idle sync
1	Slot counter resets for SENT bus idle for greater than 511 ticks

PO [7]

POR offline. SSENT (SENT_MODE 6 and 7) only.
If 1, the IC is offline when reset. If 0, the IC goes online with slot counter 0 following reset.

Value	Description
0	After a reset, the IC goes online with a slot counter = 0.
1	Sensor stays offline following a reset. IC goes online following a slot counter synchronization via F_SYNC pulse, an idle sync (if IS = 1), or a slot sync (if SS = 1 and slot marking is enabled).

SDRV [6:4]

Sets the ramp rate on the gate of the SENT output driver, thereby adjusting the falling edge slew rate.

Code	Fall Time (80% to 20% Typical Values) (µs)	
	C_{LOAD} = 100 pF	C_{LOAD} = 1 nF
000 (default)	0.031	0.102
001	0.075	0.105
010	0.130	0.226
011	0.180	0.296
100	0.460	0.622
101	0.930	1.100
110	1.900	1.900
111	2.900	2.700

DM [3]

Disables Manchester. If 1, all Manchester commands on V_{CC} are ignored.

Value	Description
0	Manchester is not ignored
1	Manchester commands are ignored

H2T [2]

Hysteresis to turns.
Selects if the hysteresis angle is used for turns counting. Only applies if LPC.TCP = 1.
Also controls if the hysteresis value of angle is populated in the PTANG register (serial 0x3A).

Value	Description
0	PLL angle without hysteresis is used for turns (if LPC.TCP = 1).
1	PLL angle with hysteresis is used for turns (if LPC.TCP = 1).

S17 [1]

IC ignores the 17th SPI clock. Allows negative edge sampling at the MCU (host).

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SC [0]

IC monitors the incoming CRC.
If set to 1 and an incoming packet is corrupt, the last valid read request contains the following response:

Value	Description
0	No monitoring of the incoming CRC
1	A33002 monitors incoming CRC. Discards packet if corrupt.

Address 0x1C (ANG)

Bit	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ORATE				RD	RO	HYSTERESIS						ZERO_OFFSET											
Default	0	0	0	0	0*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

* ANG.RD set to 1 on die 2 of dual-die device

ORATE [23:20]

Reduces the output rate by averaging samples. 2^{ORATE} samples are averaged. ORATE values above 12 are reduced to 12 in the logic, meaning that up to 4096 samples ≈ 8 ms can be selected as averaging time.

Value	Description
0000	1 sample. 2 µs update rate.
0001	2 samples. 4 µs update rate.
0010	4 samples. 8 µs update rate.
…	…
1100	4096 samples. ≈8 ms update rate.

The majority of angle noise is composed of low-frequency content. Due to this, noticeable improvements in IC resolution are not observed until relatively high values of ORATE (8 or above, corresponding to 256 samples). Because of this, nonzero ORATE settings are not recommended, except in cases where sensor response time is not a major concern (i.e., low-rpm applications).

RD [19]

Rotates die. Rotates final angle 180°. Last step in the angle algorithm. This is a convenient setting to adjust one die in a dual-die package for conformance to the other die.

Value	Description
0	No rotation applied
1	180° added to final angle

RO [18]

Rotation direction (prelinearization). If set to 0, increasing angle movement is in the clockwise direction when looking down on the top of the die. If set to 1, increasing angle movement is in the counter-clockwise direction.

Value	Description
0	Output angle increases with a clockwise rotation (when viewed from above the magnet and device)
1	Output angle increases with a counter-clockwise rotation (when viewed from above the magnet and device)

HYSTERESIS [17:12]

Angle hysteresis threshold. In 14-bit resolution. Provides ≈0° to 1.384° of hysteresis.

Value	Description
00 0000	No hysteresis
00 0001	≈0.022° of hysteresis
…	…
11 1111	≈1.384° of hysteresis

ZERO_OFFSET [11:0]

Post-compensation zero offset (or DC adjust), at 12-bit resolution. PWS.ZAL bit determines if ZERO_OFFSET is applied before or after linearization.
ZAL = 0: ZERO_OFFSET precedes linearization
ZAL = 1: ZERO_OFFSET follows linearization

This value is subtracted from the measured angle value.

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Address 0x1D (LPC)—LP Control

Bit	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	T45	TCP	–	–	TURNS_INIT		–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Default	0	0	–	–	0	0	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–

T45 [23]

Defines the resolution of the turns counter.

Value	Description
0	Turns counter measures 180° of rotation
1	Turns counter measures 45° of rotation

TCP [22]

Turns counter PLL.
Controls which signal path feeds the turns counter.
If 1, the PLL angle is used for turns counting, except in instances of loss of PLL lock. In the case of using the PLL angle, the PWE.ZCD_TURNS_OFFSET should be set to align the ZCD angle close to the PLL angle, to prevent turns corruption when switching the source.

Value	Description
0	Turns counting uses the ZCD angle
1	Turns counting uses the PLL angle, except if PLL lock is lost.

TURNS_INIT [19:18]

Controls the turns initialization on power-on.

Value (Binary)	Description
00	Turns counter is 0 on power-on.
01	Turns counter is 0 on power-on.
10	Turns counter set to settled angle observed at power-on (turns value may be nonzero after power-on).
11	Turns counter set to settled angle offset at power-on. Turns counter is zero at power-on, and TURNS_OFFSET aligns with angle at power-on.

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Address 0x1E (COM)

Bit	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LOCK				LBE	CSE	DUR	DEL	–	CUD	DST	DHR	MAG_THES_HI						MAG_THRES_LO					
Default	0	0	0	0	1	1	0	0	–	0	0	0	1	0	1	0	1	0	0	0	0	1	1	0

LOCK [23:20]

EEPROM and shadow memory lock.
Permanent lock.

Value	Description
1100	Writing to EEPROM is locked
0011	Writing to EEPROM and shadow memory is locked

LBE [19]

Power-up logic BIST enable.
LBIST requires ≈30 ms to run.

Value	Description
0	LBIST is not run on power-up
1	LBIST is run on power-up

LBIST and CVH self-tests are run in parallel. Therefore, if both are enabled on power-up, power-on time is ≈45 ms.

CSE [18]

Power-up CVH self-test enable.
CVH self-test requires ≈45 ms to run.

Value	Description
0	CVH is not run on power-up
1	CVH is run on power-up

LBIST and CVH self-test are run in parallel. Therefore, if both are enabled on power-up, power-on time is ≈45 ms.

DUR [17]

Disable unlock requirement for CUST2 EEPROM field (0x17). Only applies if CUD = 1.

Value	Description
0	Typical unlock requirements apply to Customer 2 EEPROM field.
1	If CUD = 1, unlock code does not need to be sent to the IC prior to writing CUST2 EEPROM space.

DEL [16]

Disable EEPROM lock (bits 23:20 of this address space) on CUST2 EEPROM field (0x17). Only applies if CUD = 1.

Value	Description
0	EEPROM lock applies to Customer 2 EEPROM field
1	If CUD = 1, EEPROM lock affects writability of CUST2 EEPROM field.

CUD [14]

Customer word unlock disable. Allows COM.DEL and COM.DUR to take effect on CUST2 (0x17) EEPROM field.

Value	Description
0	COM.DEL and COM.DUR settings do not apply.
1	COM.DEL and COM.DUR settings apply to CUST2 EEPROM field.

DST [13]

Disable self-test initiation from the serial register.

Value	Description
0	Self-tests may be initiated via a “special” serial register command.
1	Prevents running either LBIST or CVH self-test from the CTRL register.

DHR [12]

Disable hard reset from the serial register.

Value	Description
0	A hard reset may be initiated via a “special” serial register command.
1	Prevents initiating a hard reset from the CTRL register.

MAG_THRES_HI [11:6]

Magnetic threshold high value. Determine set-point of the MSH flag. When set to 0, check is disabled. Limit increases in 32 G increments.

Value	Description
00 0000	High-field flag disabled
00 0001	32 G
00 0010	64 G
…	…
10 0101	1184 G
…	…
10 1010	1344 G
…	…
11 1111	2016 G

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MAG_THRES_LO [5:0]

Magnetic threshold low value. Determines set point of the MSL flag. When set to 0, check is disabled. Limit increased in 16 G increments.

Value	Description
00 0000	Low-field flag disabled
00 0001	16 G
00 0010	32 G
…	…
00 0110	96 G
…	…
00 1101	208 G
…	…
11 1111	1008 G

Address 0x1F (CUST)

Bit	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CUSTOMER																							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CUSTOMER [23:0]

Customer EEPROM space.

Address 0x20 (LIN00)

Bit	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LINEARIZATION ERROR SEGMENT 1												LINEARIZATION ERROR SEGMENT 2											
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LINEARIZATION ERROR SEGMENT 1 [23:12]

Correction value at segment boundary. Signed. Resolution is based on PWM.LS bit.

Value	LS = 0	LS = 1
0x000	0.00°	0.00°
0x001	≈0.011	≈0.022
…	…	…
0x7FF	≈22.49°	≈44.98°
0x800	–22.50	–45.00°
…	…	…
0xFFF	≈–0.011	≈–0.022°

LINEARIZATION ERROR SEGMENT 2 [11:0]

Correction value at segment boundary. Signed. Resolution is based on PWM.LS bit.

Value	LS = 0	LS = 1
0x000	0.00°	0.00°
0x001	≈0.011	≈0.022
…	…	…
0x7FF	≈22.49°	≈44.98°
0x800	–22.50	–45.00°
…	…	…
0xFFF	≈–0.011	≈–0.022°

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Address 0x21:0x2F (LIN00)

Bit	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LINEARIZATION ERROR SEGMENT N (ODD 3 THROUGH 31)												LINEARIZATION ERROR SEGMENT N (EVEN, 4 THROUGH 32)											
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LINEARIZATION ERROR SEGMENT N [23:12]

Correction value at segment boundary. Signed. Resolution is based on PWM.LS bit.

Value	LS = 0	LS = 1
0x000	0.00°	0.00°
0x001	≈0.011	≈0.022
…	…	…
0x7FF	≈22.49°	≈44.98°
0x800	–22.50	–45.00°
…	…	…
0xFFF	≈–0.011	≈–0.022°

LINEARIZATION ERROR SEGMENT N [11:0]

Correction value at segment boundary. Signed. Resolution is based on PWM.LS bit.

Value	LS = 0	LS = 1
0x000	0.00°	0.00°
0x001	≈0.011	≈0.022
…	…	…
0x7FF	≈22.49°	≈44.98°
0x800	–22.50	–45.00°
…	…	…
0xFFF	≈–0.011	≈–0.022°

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SAFETY AND DIAGNOSTICS

The A33002 was developed in accordance with the ASIL design flow. It incorporates several diagnostics.

Alive Counter

A 32-bit counter increments periodically from zero after power-on or hard reset. It is read via AUX.ALV. The alive increment period is 8.192 ms.

The alive counter can overflow. The overflow period of the counter is [$2^{32} \times 8.192$] milliseconds. This period is approximately 400 days.

Oscillator Watchdogs

The watchdogs run constantly. These watchdogs are intended to detect gross failures of either oscillator. Logic running on clocks based on each oscillator effectively counts clock periods produced in the other clock domain and compares the count to expected limits.

Logic Built-In Self-Test (LBIST)

Logic BIST is implemented to verify the integrity of the A33002 logic. It can be executed in parallel with the CVH self-test. LBIST is effectively a form of auto-driven scan. The logic to be tested is broken into 31 scan chains. The chains are fed in parallel by a 31-bit linear feedback shift register (LFSR) to generate pseudo-random data. The output of the scan chains is fed back into a multiple input shift register (MISR) that accumulates the shifted bits into a 31-bit signature.

LBIST takes approximately 30 ms to complete.

LBIST can be enabled to run on power-up by setting the COM.LBE bit in EEPROM (0x1E bit 19).

The test is complete following initialization when either:

- STA.SDN = 1 (special done) or
- STA.LBR = 0 (LBIST not running)

A failure is indicated by: ERR.STF = 1

CVH Self-Test

CVH self-test is a method of verifying the operation of the CVH transducer without applying an external magnetic field. This feature is useful for both manufacturing test and integration debug. The CVH self-test is implemented by changing the switch configuration from the typical operating mode into a test configuration, allowing a test current to drive the CVH in place of the magnetic field. By changing the direction of the test current and by changing the elements in the CVH that are driven, the self-test circuit emulates a changing angle of magnetic field. The measured angle is monitored to determine a passing or failing device.

CVH self-test typically takes 52 ms to verify.

Self-test can be run on power-up, by setting the EEPROM field COM.CSE = 1.

Self-test can also be invoked via the serial control register by issuing the corresponding “special” command.

The test is complete when:

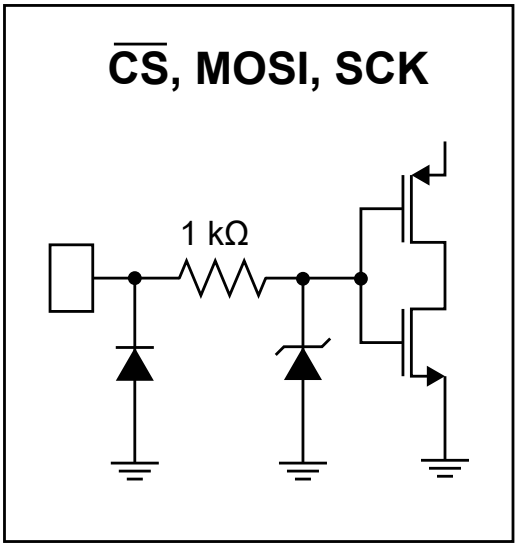
- STA.SDN = 1 (special done); or
- STA.CSTR = 0 (CVH self-test not running).

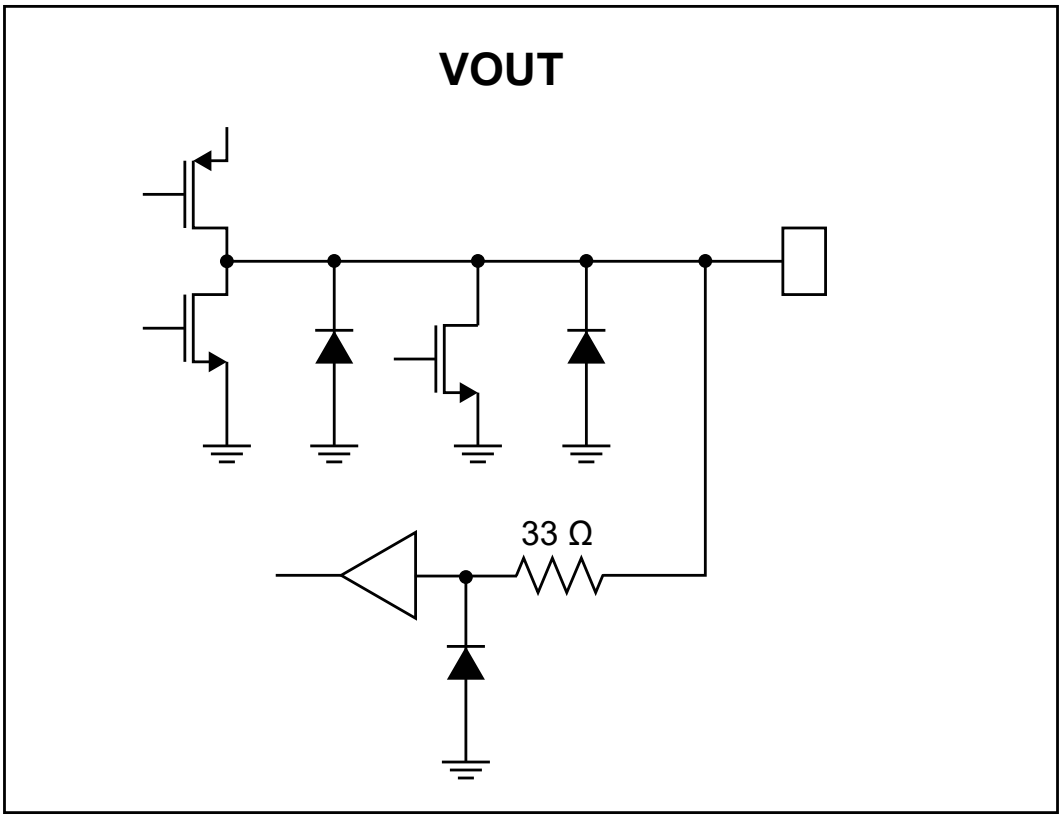
Failure is indicated by:

- ERR.STF = 1 (assuming it was cleared before the test was run).

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I/O STRUCTURES





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PACKAGE OUTLINE DRAWING

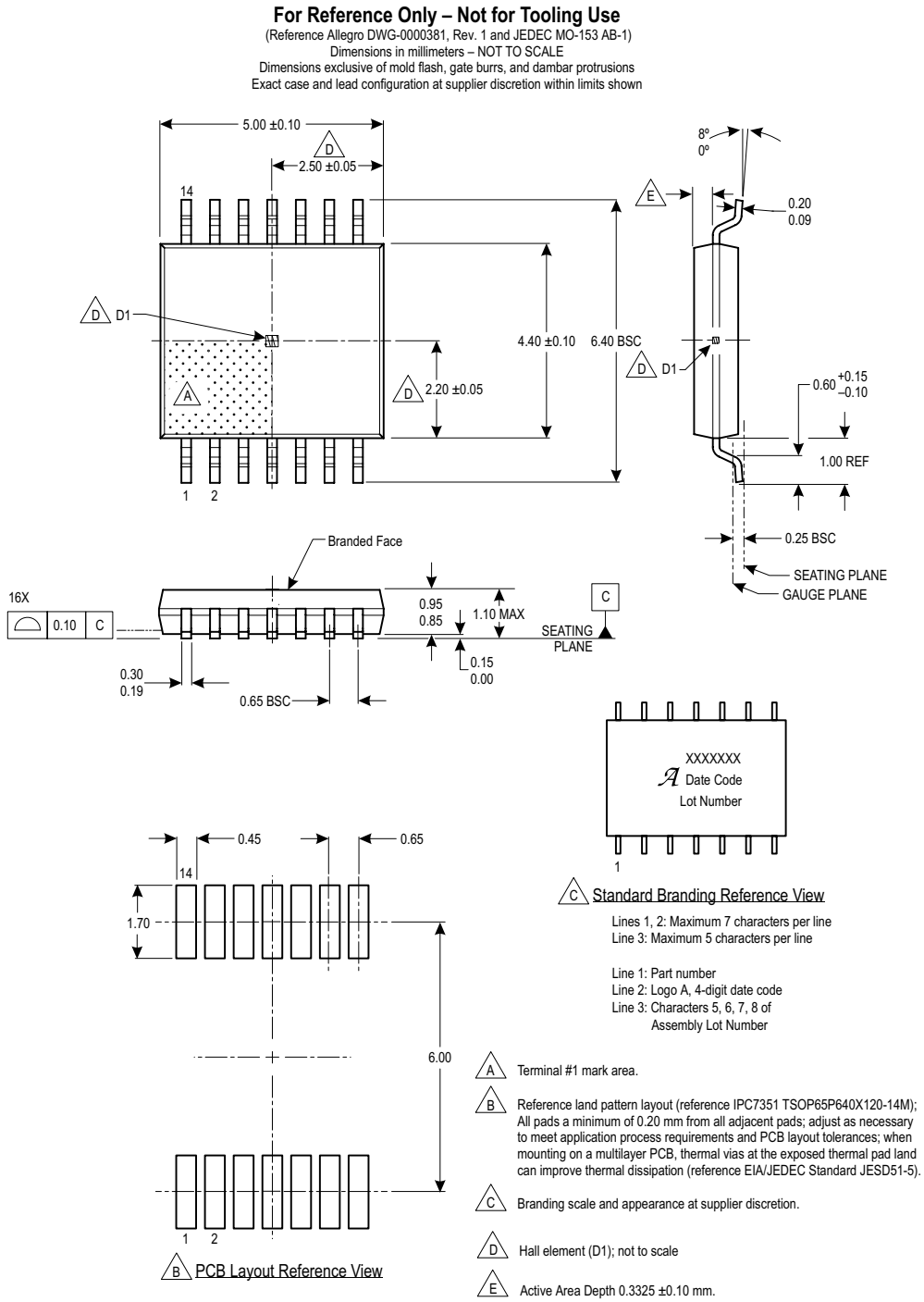


Figure 33: Package LE, 14-Pin TSSOP, single die

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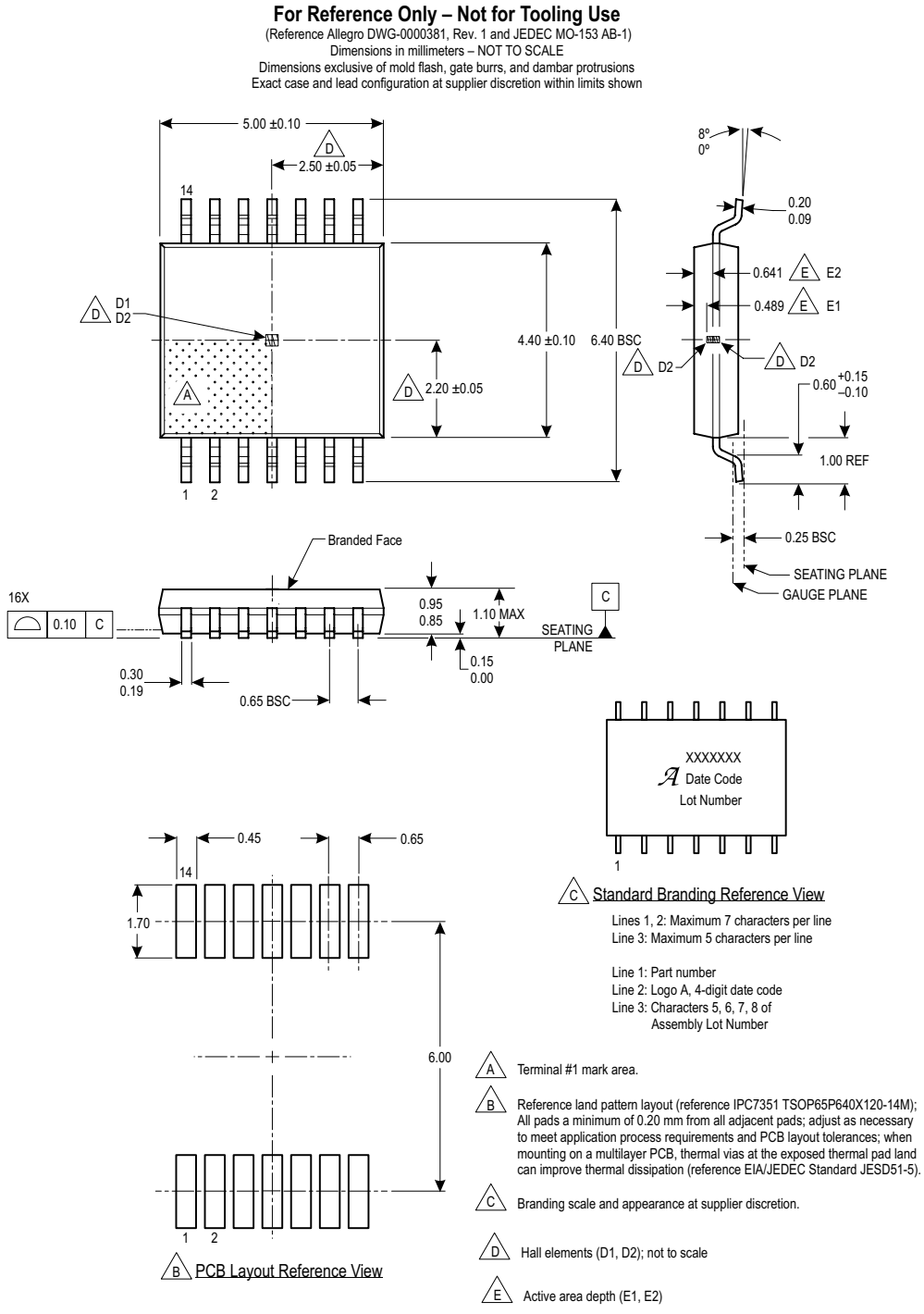


Figure 34: Package LE, 14-Pin TSSOP, dual die

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APPENDIX A: SENT OUTPUT DESCRIPTION

SENT Output Mode

The SENT output converts the measured magnetic field angle to a binary value mapped to the full-scale output (FSO) range of 0 to 4095, shown in Figure 35. This data is inserted into a binary pulse message, referred to as a frame, that conforms to the SENT data transmission specification (SAE J2716 JAN2010).

The SENT frame can be configured by setting the following parameters in EEPROM (shown in Figure 35):

- SENT_MODE
- SDRV
- DATA_MODE
- SCN_MODE
- SENT_TICK

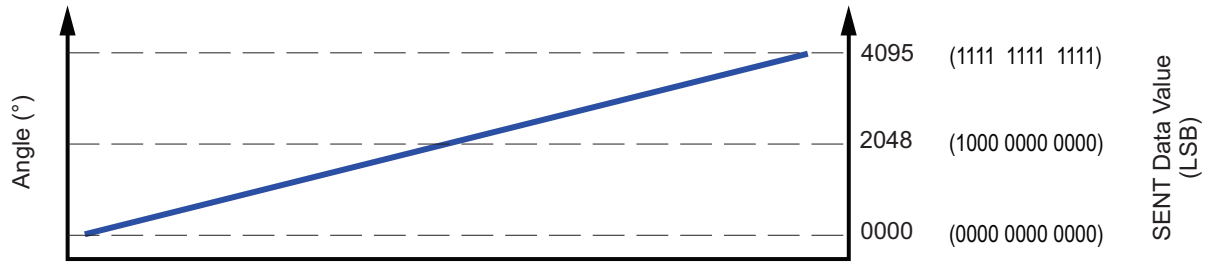


Figure 35: Angle is Represented as a 12-bit Digital Value

Table 22: Main SENT Parameter Location [1]

Address	Bits	Parameter Name	Description
0x19	22:16	SENT_TICK	Sets tick rate coefficient.
	14:12	SENT_MODE	Sets frame update rate, enables TSENT, SSENT, ASENT.
	11:8	DATA_MODE	Set data nibble format.
	7	CIS	CRC nibble includes the status and communication nibble data.
	6:4	SCN_MODE	Configure status and communication nibble contents.
0x1B	23	PEN	PWM enable. When 1, overrides the SENT_MODE setting.
	6:4	SDRV	SENT pin drive strength.

[1] For information about SSENT/ASENT configurations bits, refer to the Sequential SENT (SSENT)/Addressable SENT (ASENT) sections.

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MESSAGE STRUCTURE

Data within a SENT message frame is represented as a series of nibbles, with the following characteristics:

- Each nibble is an ordered pair of a low-voltage interval followed by a high-voltage interval.
- The low-voltage interval acts as the delimiting state, which acts as a boundary between each nibble. The length of this low-voltage interval is fixed at 5 ticks.
- The high-voltage interval performs the job of the information state and is variable in duration in order to contain the data payload of the nibble.
- The slew rate of the falling edge may be adjusted using the SDRV parameter.

The duration of a nibble is denominated in ticks. The period of a tick is set by the SENT_TICK parameter. The duration of the nibble is the sum of the low-voltage interval plus the high-voltage interval.

The parts of a SENT message are arranged in the following required sequence (see Table 22):

1. **Synchronization and Calibration:** Flags the start of the SENT message.
2. **Status and Communication Nibble:** Provides A33002 status and the optional serial data determined by the setting of the SCN_MODE parameter.
3. **Data:** Angle data and optional data.
4. **CRC:** Error checking.
5. **Pause Pulse (optional):** Fill pulse between SENT message frames.

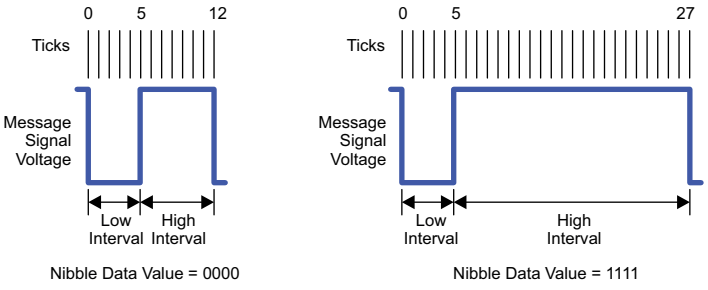


Figure 36: General Value Formation for SENT

0000 (left), 1111 (right)

Table 23: Nibble Composition and Value

Quantity of Ticks			Binary (4-bit) Value	Decimal Equivalent Value
Low-Voltage Interval	High-Voltage Interval	Total		
5	7	12	0000	0
5	8	13	0001	1
5	9	14	0010	2
⋮	⋮	⋮	⋮	⋮
5	21	26	1110	14
5	22	27	1111	15

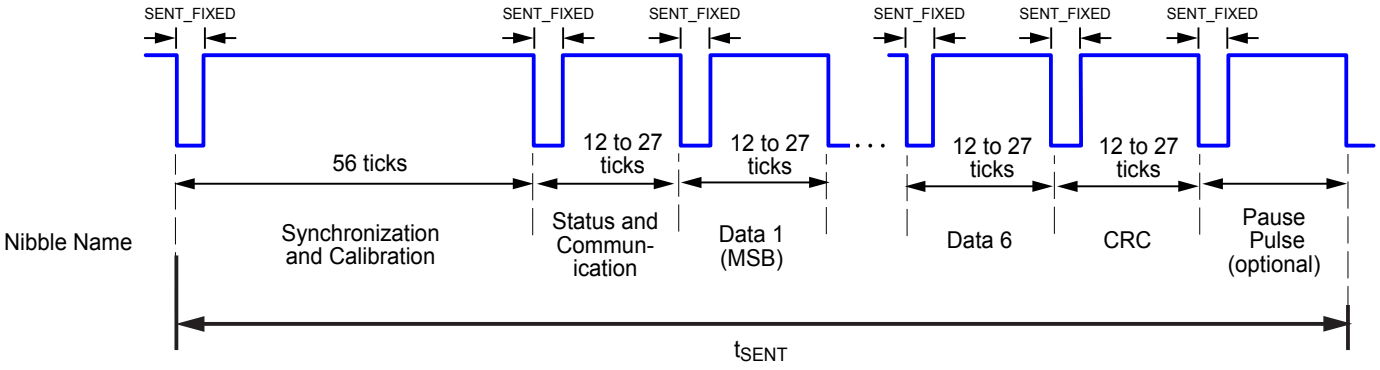


Figure 37: General Format for SENT Message Frame

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Synchronization and Calibration Pulse

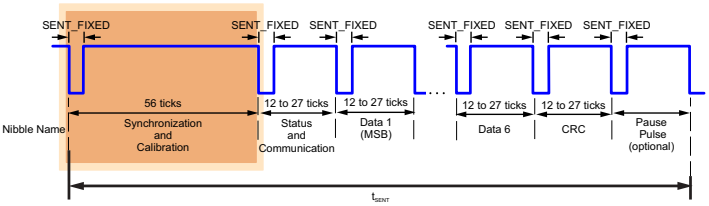


Figure 38: Synchronization and Calibration Pulse within the SENT Message Frame

The synchronization and calibration pulse is 56 ticks wide, measured from falling edge to falling edge, and it delineates the start of a new message frame. The host microcontroller uses this pulse to rescale the subsequent nibble values to correct for clock variation between the controller and the sensor.

Status and Communication Nibble

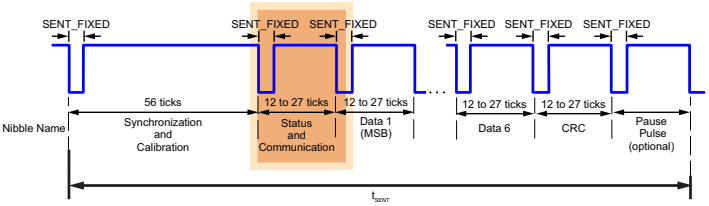


Figure 39: Status and Communication Nibble within the SENT Message Frame

The status and communication nibble (SCN) provides diagnostic data along with other status and environmental data. Nibble contents are controlled via the SCN_MODE field within EEPROM. By default, contents of the SCN are not included in the 4-bit CRC at the end of each SENT frame. The CIS bit within EEPROM enables CRC coverage of the SCN contents. It should be noted that this option is not specified in the SAE J2716 SENT standard. With the CIS bit set, the CRC is no longer compliant with that outlined in the SENT specification.

The SCN has three different types of bit values that may be present, depending on the SCN_MODE setting. These are:

A. Soft/Hard Error: Overall condition of the A33002, separated into soft and hard error flags. Detailed error data can be obtained via the expanded data nibbles, set via DATA_MODE, or through the slow serial communication.

Hard Error Flag:

Hard error flags cannot be masked and assert independent of EEPROM mask bits.

- Latched indefinitely if any of the following occur:
  - □ Watchdog timeout
  - □ EEPROM hard error (multibit fault)
  - □ Self-test error
- Temporarily sets but clears after the following conditions pass:
  - □ Reset/POR
  - □ ZCD integrity error
  - □ Angle averaging error
  - □ Temperature sensor out of range
  - □ PLL not in lock

Soft Error Flag:

Soft error flag may be masked by setting the appropriate mask bit in EEPROM address 0x1A.

- Latched temporarily, clears on next SENT frame unless condition is still asserted.
  - □ Any unmasked errors asserted

B. ID data: Die ID bits set via SA0 (SCLK) and SA1 (MOSI) pins.

- ID[0]: Value set by the logic level of the SA0 pin.
- ID[1]: Value set by the logic level of the SA1 pin.

C. Serial Data: Two bits, consisting of the SERIALSYNC and SERIALDATA bits. Together they form the short serial message (per SAE J2716, section 5.2.4.1).

- SERIALSYNC: Indicates the start of a 16-bit serial message.
- SERIALDATA: Serial data, transmitted one bit at a time, MSB first.

Table 24: SCN Bit Contents

SCN_ MODE	Bit 3	Bit 2	Bit 1	Bit 0
000	0	0	SOFT	HARD
001	SERIALSYNC	SERIALDATA	SOFT	HARD
010	ID[1]	ID[0]	SOFT	HARD
011	0	0	0	SOFT+HARD
100	0	0	ID[1]	ID[0]
101	SERIALSYNC	SERIALDATA	ID[1]	ID[0]
110	SOFT	HARD	ID[1]	ID[0]
111	SERIALSYNC	SERIALDATA	0	SOFT+HARD

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Short Serial Message Format

The SENT specification allows additional data transfer via specific bits within the SCN. This data stream is also referred to as the slow channel.

The A33002 implements short serial message format as described in paragraph 5.2.4.1 of the SAE J2716 specification. A 16-bit data packet is transmitted one bit at a time over consecutive SENT message frames, starting with the MSB. The beginning of each 16-bit packet is indicated by a 1 in the SERIALSYNC bit. The message data is transmitted bit-by-bit via the SERIALDATA bit. The 16-bit message packet is separated into three fields:

A. MESSAGE ID (4 bits):
Four leading bits of the serial data packet, used to identify data contents. Data rotates through the 16 message IDs as shown in Table 25. MESSAGE ID may be considered the 4 LSBs of a 12-bit alive counter that increments every 16 SENT frames.

B. DATA (8 bits):
Eight bits of message data.

C. CRC (4 bits):
CRC checksum, used to validate MESSAGE ID and DATA. Same CRC algorithm as that used for the SENT message frame.

Sixteen separate SENT frames are needed to construct a complete 16-bit serial message. To transmit all eight unique serial data messages (message IDs 0 through 7), a total of 128 SENT transmission are necessary. A complete rotation of the 16 message IDs requires 256 SENT transmissions.

Table 25: Short Serial Message Format in SENT Status and Communication Nibble

SNC Bit	Nibble #															
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
SERIALSYNC	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SERIALDATA	MESSAGE ID				DATA								CRC			

Table 26: Serial Output Data

Message ID (4 bits)	Data (8 bits)
0 (8)	8-bit alive counter (increments by one, every 0-to-15-degrees rotation of the MESSAGE ID field)
1 (9)	Temperature in degrees Celsius, offset by +64 (subtract 64 to get measured temperature)
2 (10)	STATUS, bits [15:8] See Table 19.
3 (11)	STATUS, bits [7:0] See Table 19.
4 (12)	Magnetic field reading in gauss, divided by 8 (multiply by 8 to obtain gauss rating)
5 (13)	Customer [23:16] from EEPROM 0x1F.
6 (14)	Customer [15:8] from EEPROM 0x1F.
7 (15)	Customer [7:0] from EEPROM 0x1F.

SENT Data Nibbles

The angle value is embedded within the first three (if using a 12-bit angle value) or four (if using a 16-bit angle value) nibbles of every SENT frame and transmitted MSB first. Additional data may be transmitted by extending the number of data nibbles, up to 6. The contents and number of data nibbles in every SENT frame is configured using the DATA_MODE field in EEPROM.

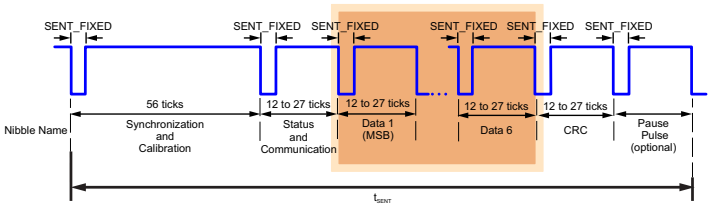
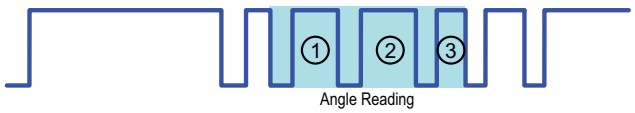
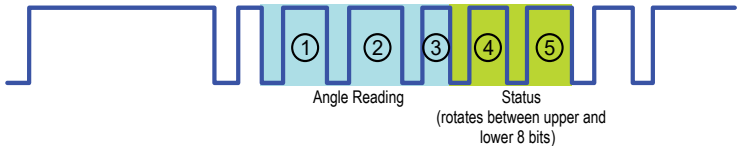
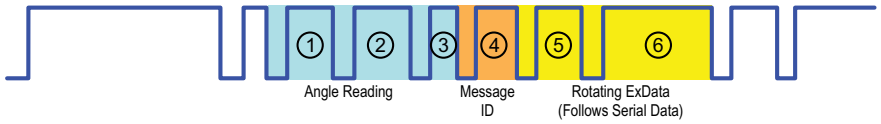
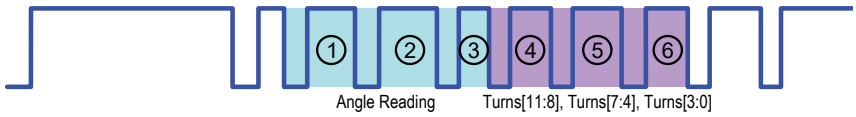
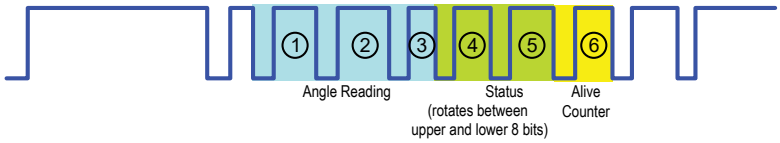
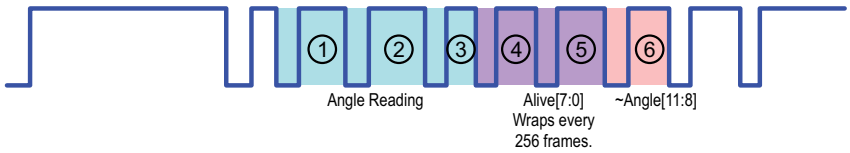
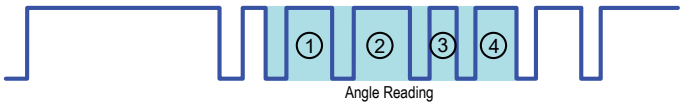
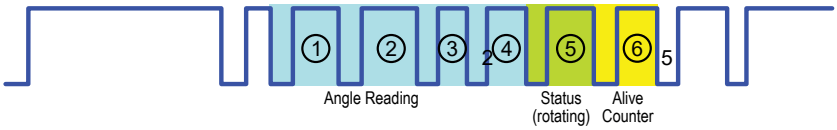


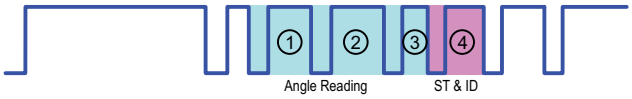
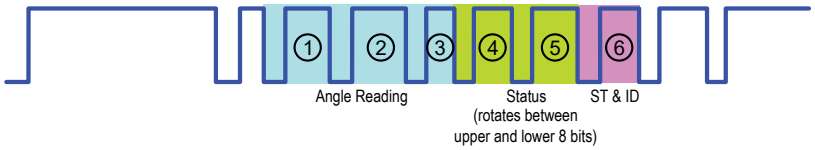
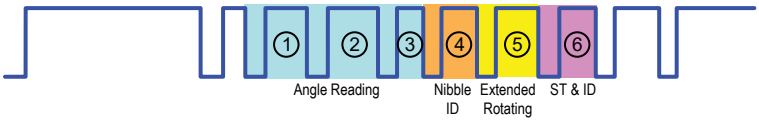
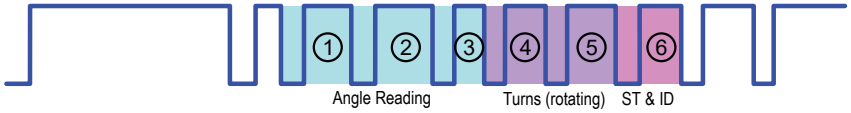
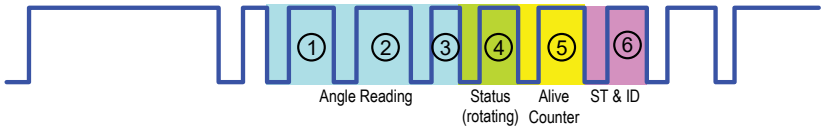
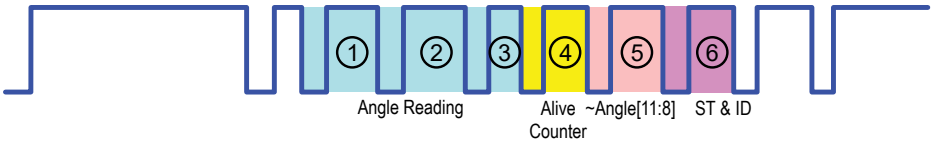
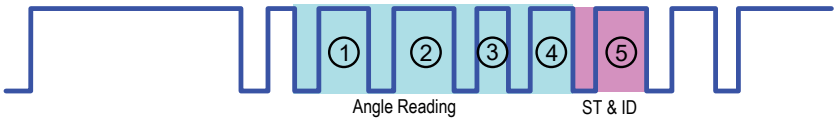
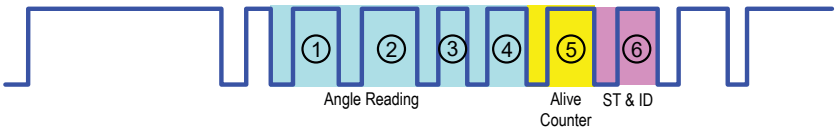
Figure 40: SENT Data Nibbles within the SENT Message Frame

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SENT Data Mode Options

DATA_MODE = 0 Data Nibble 1,2,3 = Angle	
DATA_MODE = 1 Data Nibble 1,2,3 = Angle Data Nibble 4,5 = Rotating status bits	 Status bits rotate between the upper and lower 7 bits of the SENT status flags, distinguished by the LSB. The upper 7 bits have an LSB equal to 0. The lower half have an LSB equal to 1. See description of SENT status flags.
DATA_MODE = 2 Data Nibble 1,2,3 = Angle Data Nibbles 4 = Message ID (see Short Serial Message Format section). Data Nibbles 5,6 = Rotating extended data, same sequence as serial message	 Nibbles 4,5,6 make up a rotating serial data stream following the same rotation pattern as the short serial message transmission. Allows one 12-bit packet (4 bits for ID, 8 bits for data) to be transmitted every SENT frame. Provides a faster method of obtaining extra sensor data typically supplied via the slow serial transmission.
DATA_MODE = 3 Data Nibble 1,2,3 = Angle Data Nibbles 4 = Turns counter [11:8] Data Nibble 5= Turns counter [7:4] Data Nibble 6 = Turns counter [3:0]	
DATA_MODE = 4 Data Nibble 1,2,3 = Angle Data Nibble 4,5 = Rotating status bits Data Nibble 6 = Alive counter	
DATA_MODE = 5 Data Nibble 1,2,3 = Angle Data Nibble 4,5 = 8-bit alive counter Data Nibble 6 = 1's complement of Data Nibble 1	 When combined with SCN_MODE = 3, this implements the “Single Secure Sensor” requirement outlined in SAE J2716 Appendix A.
DATA_MODE = 6 Data Nibble 1,2,3,4 = Angle value	
DATA_MODE = 7 Nibbles 1,2,3,4 = Angle value Nibble 5 = Status (rotating) Nibble 6 = Alive counter	 Status bits rotate through the 14 SENT flags over 4 SENT frames. The least significant 2 bits of the alive counter identify the quadrant of rotation.

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DATA_MODE = 8 Data Nibble 1,2,3 = Angle Data Nibble 4 = Self-test flag and ID	 Nibble 4 provides a self-test failure flag as well as the two address bits set via the SA0 and SA1 pins.
DATA_MODE = 9 Data Nibble 1,2,3 = Angle Data Nibble 4,5 = Rotating status bits Nibble 6 = Self-test flag and ID	
DATA_MODE = 10 Data Nibble 1,2,3 = Angle Data Nibble 4 = Nibble ID Data Nibble 5 = Rotating extended data Data Nibble 6 = Self-test flag and ID	 Nibbles 4,5 are a condensed version of the rotating serial data stream following the same rotation pattern as the short serial message transmission. The 8-bit message is transmitted in two successive SENT frames, MSB first. The nibble ID increments from 0 through 15, which represents message IDs 0 through 7; i.e., the 8-bit alive counter (which corresponds to Message ID 0) is identified by a nibble ID value of 0 and 1.
DATA_MODE = 11 Data Nibble 1,2,3 = Angle Data Nibble 4= Turns counter [7:4] Data Nibble 5 = Turns counter [3:0] Data Nibble 6 = Self-test flag and ID	 Turns count rotates over 2 SENT frames. MSB set to 1 identifies lower half.
DATA_MODE = 12 Data Nibble 1,2,3 = Angle Data Nibble 4 = Rotating status bits Data Nibble 5 = Alive counter Data Nibble 6 = Self-test flag and ID	 Status bits rotate through the 14 SENT status flags over 4 SENT frames. The least significant 2 bits of the alive counter identify the quadrant of rotation.
DATA_MODE = 13 Data Nibble 1,2,3 = Angle Data Nibble 3,4 = Rotating status bits (2 MSB are a counter) Data Nibble 5 = Self-test flag and ID	 Modified version to the “Single Secure Sensor” implementation as outlined in Appendix A of SAE J2716.
DATA_MODE = 14 Data Nibble 1,2,3, 4 = Angle Data Nibble 5 = Self-test flag and ID	
DATA_MODE = 15 Data Nibble 1,2,3, 4 = Angle Data Nibble 5 = Alive counter Data Nibble 6 = Self-test flag and ID	

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Self-Test and ID Nibble

The self-test and ID (ST&ID) nibble is optional. It is included as one of the extended nibbles when DATA_MODE = 4, 5, 6, or 7. This nibble consists of three data bits (MSB is always 0):

Bit 3	Bit 2	Bit 1	Bit 0
0	ST	ID[1]	ID[0]

Figure 41: ST & ID Nibble

The ST bit indicates a failure of one of the three internal self-tests (CVH self-test and logic BIST). If set, this indicates significant failure of the sensor, and a reset should be initiated.

ID[0] and ID[1] provide the sensor ID value as determined via the logic values of the SA0 and SA1 pins.

This nibble is particularly useful when sharing SENT lines, as it allows the self-test diagnostic results and corresponding sensor ID to be quickly determined without a significant latency penalty (only one nibble to the SENT frame).

SENT Status Bit Description

The A33002 has extensive status and error flags that may be read at any time via SPI or by entering Manchester communication mode. To facilitate error/status flag reporting by way of the unidirectional SENT protocol, a selection of these flags is communicated via extra data nibbles when DATA_MODE = 1, 4, 7, 9, or 12. These status flags are also transmitted via the slow serial protocol through the SCN.

The flags are 0 if the condition is clear and 1 if the condition is true. For transient conditions, the flag clears after the bit is presented on the SENT output.

EEPROM error masks do not apply to error/warning flags within the SENT status.

Table 27: SENT Status Flag Definitions

Bit	Symbol	Definition
15	PLK	PLL not in lock.
14	AVG	Angle averaging (ORATE) or zero-crossing integrity error.
13	RST	POR (power-on-reset) occurred.
12	TR	Temperature sensor out of range.
11	STF	Self-test error (CVH self-test or LBIST).
10	EUE	EEPROM hard error.
9	WDE	Oscillator watchdog error.
8	R	Always 0. Indicates MSB byte.
7	MSL	Magnetic Sense Low.
6	UVD	Undervoltage, on V_{CC} line or analog regulator output.
5	ESE	EEPROM soft error.
4	SAT	Saturation in math computations.
3	SEN	SENT contention.
2	MSH	Magnetic sense high.
1	TOV	Turns counter overflow.
0	R	Always 1. Indicates LSB byte.

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Status Flag Locations for SENT DATA_MODE = 1, 4, or 9 (over 2 SENT Frames)

Nibble 4				Nibble 5			
PLK	AVG	RST	TR	STF	EUE	WDE	R (0)

Nibble 4				Nibble 5			
MSL	UVD	ESE	SAT	SEN	MSH	TOV	R (1)

Status Flag Locations for SENT DATA_MODE = 7 or 12 (over 4 SENT Frames)

Nibble 4 (Status Nibble)				Nibble 5 (Alive Counter)			
PLK	AVG	RST	TR	X	X	0	0

Nibble 4 (Status Nibble)				Nibble 5 (Alive Counter)			
STF	EUE	WDE	R(0)	X	X	0	1

Nibble 4 (Status Nibble)				Nibble 5 (Alive Counter)			
MSL	UVD	ESE	SAT	X	X	1	0

Nibble 4 (Status Nibble)				Nibble 5 (Alive Counter)			
SEN	MSH	TOV	R(1)	X	X	1	1

Turns Count Information for SENT DATA_MODE = 11 (over 2 SENT Frames)

Nibble 4			Nibble 5
0	0	TURNS [11:10]	TURNS [9:6]

Nibble 4			Nibble 5
1	0	TURNS [5:4]	TURNS [3:0]

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Rotating Data Information for SENT DATA_MODE = 10 (rotates over 16 SENT frames)

Nibble 4 (Rotating Data)				Nibble 5 (Rotating Data)			
NibID				NibData			
0	0	0	0	8-bit Alive counter MSBs [7:4]			
0	0	0	1	8-bit Alive counter LSBs [3:0]			
0	0	1	0	Temperature MSBs [7:4]			
0	0	1	1	Temperature LSBs [3:0]			
0	1	0	0	PLK	AVG	RST	TR
0	1	0	1	STF	EUE	WDE	0
0	1	1	0	MSL	UVD	ESE	SAT
0	1	1	1	SEN	MSH	TOV	1
1	0	0	0	Magnetic Field [7:4]			
1	0	0	1	Magnetic Field [3:0]			
1	0	1	0	CUSTOMER [23:20]			
1	0	1	1	CUSTOMER [19:16]			
1	1	0	0	CUSTOMER [15:12]			
1	1	0	1	CUSTOMER [11:8]			
1	1	1	0	CUSTOMER [7:4]			
1	1	1	1	CUSTOMER [3:0]			

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SENT CRC Nibble

The CRC nibble is a 4-bit error checking code, implemented per the SAE J2716 SENT "recommended" specification.

The CRC is calculated using the polynomial $x^4 + x^3 + x^2 + 1$, initialized to 0101.

By default, the checksum covers only the contents of the data nibbles (3 to 6 nibbles). By setting the CIS bit within EEPROM, the contents of the SCN are included within the CRC nibble, which deviates from the SENT standard.

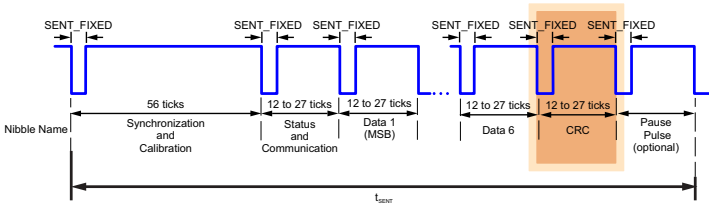


Figure 42: CRC Nibble within the SENT Message Frame

SENT Pause Pulse (Optional)

The pause pulse is an optional addition to the SENT message frame, transmitted following the CRC nibble. It acts to "fill-in" the frame until the beginning of the next SENT transmission. The pulse may behave in one of two ways, based on the SENT_MODE setting:

- If SENT_MODE = 2, a pause pulse is inserted until new angle data is available. The length of the inserted pause pulse is at least 12 ticks. If a pause longer than 768 ticks is required, the pulse restarts, requiring at least 12 more ticks.
- If SENT_MODE > 2, the sensor operates in either triggered or addressable/sequential SENT mode. In these modes, the sensor outputs a SENT message frame in response to a host action (either a trigger or a function pulse). When not responding to the host, the sensor outputs a pause pulse of indefinite length (i.e., remains high until a host request).

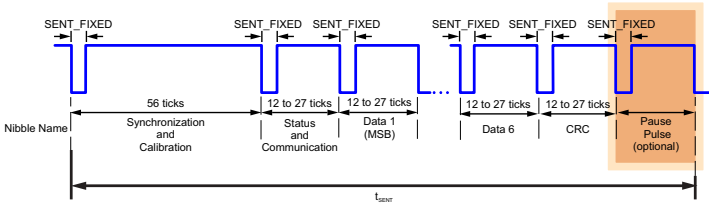


Figure 43: Pause Pulse within the SENT Message Frame

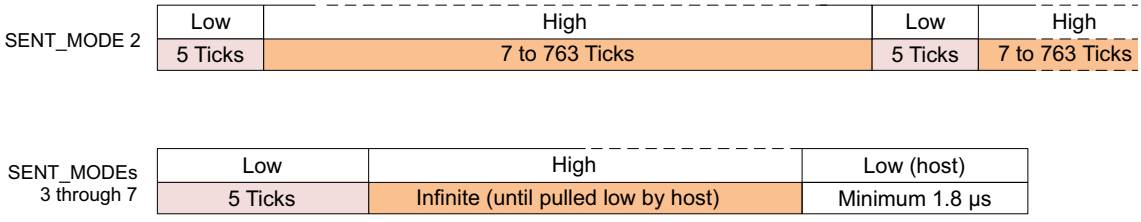


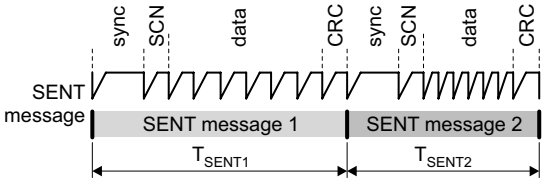
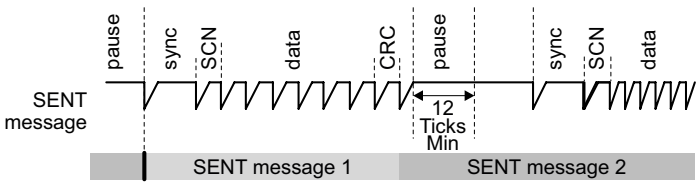
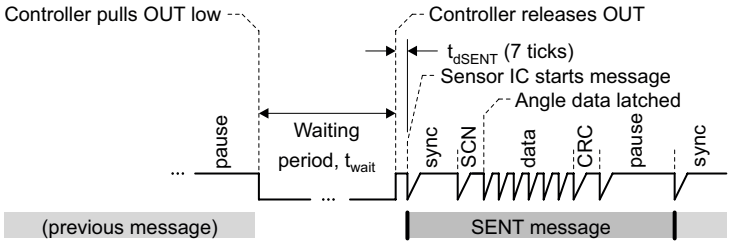
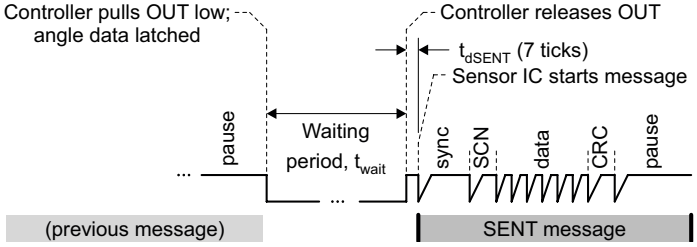
Figure 44: SENT Pause Pulse

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SENT OUTPUT MODE

The timing and method of SENT transmission may be configured using the SENT_MODE field within EEPROM. The method of SENT transmission falls within one of three categories:

6. Free Running SENT:
   Angle data is automatically placed on the SENT line with no prompting from the host. Depending on settings, the SENT message frames may be transmitted back-to-back, or synchronized with each update of the angle value.
7. Triggered SENT (TSENT):
   A SENT message frame occurs only when initiated by the host. The A33002 sensor outputs a continuous pause pulse, during which the host triggers a SENT frame by pulling the SENT line low for a minimum of $T_{Trig(MIN)}$. Once released, the sensor responds with a SENT message frame.
8. Shared SENT:
   Two distinct formats. Sequential SENT (SSENT) and addressable SENT (ASENT). Allow sharing a single SENT line among four compatible devices.

SENT_MODE	Visual	Description
000_2 (0)	–	SENT disabled.
001_2 (1)		Streaming output with variable message duration and no pause pulse. Angle data is sampled near the end of the status and communication nibble. Maximum age at time of sampling is 2^{ORATE} × 2 µs. Depending on tick time and ORATE setting, same data may be transmitted multiple times. This mode provides the quickest data delivery rate.
010_2 (2)		SENT message frames are synchronized with the device internal update rate. Pause pulse is inserted until fresh data becomes available. Angle data is sampled between 1 to 2 tick times of the synchronization pulse. Pause pulse varies in length between 12 to 2^{ORATE} × 2 µs (pulse restarts after 768 ticks).
011_2 (3)		TSENT SCN sampling: Controller initiates a SENT transmission by pulling the line low, during a pause pulse. When the controller releases the output, after a delay of t_{dSENT} the SENT message begins. Angle data is latched at the end of the SCN. Data age may be up to (2^{ORATE} + 2 µs) + $t_{RESPONSE}$ when latched. This option is useful when the controller requires a prompt with minimum “age” of the angle data.
100_2 (4)		TSENT falling-edge sampling: Similar to SENT_MODE = 3, except angle data is latched once the output line is pulled low. Useful when multiple ICs are connected to a single controller. Allows synchronous sampled data to be retrieved one device at a time, by releasing the trigger for each individual sensor. Data age may vary by up to (2^{ORATE} + 2 µs) + $t_{RESPONSE}$ when latched.
101_2 (5)	–	Addressable SENT (ASENT). See Shared SENT Protocol section.
110_2 (6)	–	Sequential SENT (SSENT). See Shared SENT Protocol section.
111_2 (7)	–	Long sequential SENT. See Shared SENT Protocol section.

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SHARED SENT PROTOCOL

Addressable SENT (ASENT) and sequential SENT (SSENT) are extensions of the Allegro Triggered SENT (TSENT) protocol. ASENT and SSENT allow multiple Allegro sensors with SENT output capability to coexist on a single shared SENT bus. The host (ECU) is able to select one sensor at a time, addressing that sensor to respond with a SENT output packet, and thus poll each sensor on the bus over some period of time.

ASENT and SSENT, like triggered SENT, require an open-drain system configuration, in which any sensor, or the host, can pull the SENT line low. The SENT line is pulled high by an external resistor to a known V_{CC}. A high level is attainable on the bus only when no device is actively pulling the line low.

In ASENT and SSENT, each sensor on the bus is assigned a unique sensor ID number between 0 and 3, allowing up to four sensors to coexist on the bus. This sensor ID number is assigned by the logic state of the SA0 and SA1 pins.

Although up to four devices function properly on a single SENT line (that is, with die ID values of 0 through 3), Manchester communication is only possible with address values of 0 and 2 (SA1/SA0 set to 00_2 and 10_2). For more information, refer to the Manchester Serial Interface section.

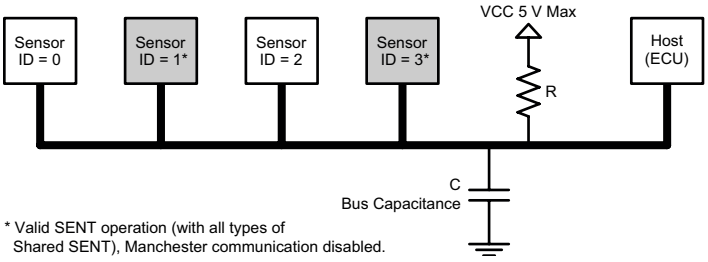


Figure 45: Shared SENT Bus Example

Function Pulses

This section describes the different function pulses that are referenced later in the Addressable SENT (ASENT) and Sequential SENT (SSENT) sections.

The host communicates to a sensor or sensors via different function pulses, which are equivalent in nature to a TSENT trigger pulse, but with defined widths. A function pulse is placed on the SENT bus by the host pulling the SENT line low for a defined number of ticks greater than a typical SENT pulse low period.

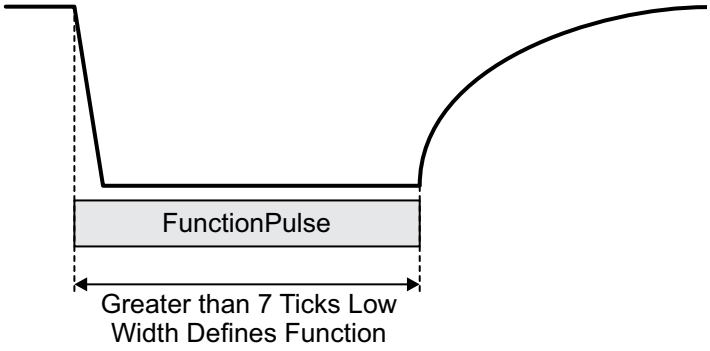


Figure 46: Function Pulse (Output by Host)

The duration of the low time is measured by the sensors and interpreted as a designated function.

Functions that are acted upon by all sensors simultaneously are designated broadcast pulses. Functions that are acted upon by only one sensor are designated addressing pulses and are associated with a target sensor ID. A function pulse may be defined as both a broadcast pulse and an addressing pulse. For instance, all sensors sample-and-hold the data, but only one transmits a SENT packet.

A sensor that does not support a specific function does not respond to the function pulse.

Function pulses must be greater in duration than the SENT pulse low time (5 ticks), not to be mistaken for part of a typical SENT transmission.

The duration of function pulses is defined in SENT ticks in order to scale with the SENT frame itself. Minimum and maximum pulse durations are set such that they satisfy electrical and timing characteristics.

The various function pulses with their expected tick ranges are shown in Table 28 through Table 30.

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Table 28: ASENT Functional Pulses

Function	Type	Related Options	Min Tick	Nom Tick	Max Tick	Description
F_OUTPUT	Addressing/ Broadcast	SEN.NS	15	17	19	Addressed sensor responds with SENT frame, containing either held data (from F_SAMPLE) or current data.
F_SAMPLE	Addressing/ Broadcast	SEN.NS SEN.FA	31	35	39	Sensors sample and hold their magnetic data, unless SEN.NS = 1. If SEN.FA = 1, this is also an addressing pulse, and the addressed sensor responds with SENT frame.
F_DIAG	Addressing/ Broadcast	SEN.DA	56	63	70	Sensor(s) enter diagnostics as determined by EEPROM settings.

Table 29: SSENT Functional Pulses. SENT_MODE = 6

Function	Type	Related Options	Min Tick	Nom Tick	Max Tick	Description
F_OUTPUT	Addressing/ Broadcast	SEN.NS SEN.ZS	15	17	19	Addressed sensor responds with SENT frame, containing either held data (from slot 0 sampling or F_SAMPLE) or current data. If SEN.ZS = 1 and SLOT = 0, sensors sample-and-hold their magnetic data.
F_SAMPLE	Addressing/ Broadcast	SEN.NS SEN.FA	31	35	39	Sensors sample-and-hold their magnetic data, unless SEN.NS = 1. If SEN.DA = 1, this is also an addressing pulse, and the addressed sensor responds with SENT frame.
F_SYNC	Broadcast		93	104	115	All sensors synchronize their slot counters such that the next slot is for sensor ID 0.
F_DIAG	Addressing/ Broadcast	SEN.DA	56	63	70	Sensor(s) enter diagnostics as determined by EEPROM settings.

Table 30: Long SSENT Functional Pulses. SENT_MODE = 7

Function	Type	Related Options	Min Tick	Nom Tick	Max Tick	Description
F_OUTPUT	Addressing/ Broadcast	SEN.NS SEN.ZS	9	Per micro controller spec	81	Addressed sensor responds with SENT frame, containing either held data (from slot 0 sampling) or current data. If SEN.ZS = 1 and SLOT = 0, sensors sample-and-hold their magnetic data.
F_SYNC	Broadcast		105	140	171	All sensors synchronize their slot counters such that the next slot is for sensor ID 0.
F_DIAG	Addressing/ Broadcast	SEN.DA	56	63	70	Sensor(s) enter diagnostics as described in the user-initiated diagnostic support.

NOTE: When using SENT_MODE = 7, tick times shorter than 1.5 µs are not recommended. With tick times less than 1.5 µs, the nominal 5-tick low portion of a SENT pulse may be interpreted as 9 ticks, overlapping with the F_OUTPUT range. PWS.FP_ADJ may be used to increase the minimum tick level of the F_OUTPUT pulse to alleviate possible bus conflicts.

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SEQUENTIAL SENT (SSENT)

SSENT Addressing Protocol

The SSENT protocol requires sensors on the bus to be polled in sequential order, meaning increasing, consecutive, and rotating order by sensor ID, starting with sensor ID 0. The slot for a sensor is the time at which that sensor is expected to respond to an addressing pulse and other sensors are expected to not respond.

Each sensor independently maintains a slot counter that is incremented each time the sensor detects an addressing pulse. This slot counter becomes the slot number, which is used by the sensor to decide which sensor is being polled by the host. The slot counter is compared to the sensor ID, and if they match, that sensor responds with the SENT frame, and all other sensors do not respond, although each increments its own slot counter.

If the slot counter is incremented past the total number of sensors on the bus (SEN.MAXID option), the slot counter is returned to 0. Each sensor must be programmed consistently with the total number of sensors so they all roll over to 0 at the same count. Sensors do not increment their slot counter on a broadcast pulse.

The SSENT protocol relies on each sensor maintaining the exact same slot number by counting the addressing pulses. To synchronize all sensors to the same slot number, the SSENT protocol has a broadcast F_SYNC pulse that is used by the host to force all sensors to reset their slot counter to 0.

Long SSENT (SENT_MODE = 7) allows the A33002 to work with existing shared SENT methodologies. The added overhead decreases the rate at which messages may be transmitted.

To reduce the burden on the host and to improve detection and recovery from bus contention or system errors affecting the SENT bus, the SSENT protocol has the following configuration options that can be selected.

- Slot marking (enabled by SEN.SM). When enabled, each sensor waits a different length of time following an addressing pulse, based on their sensor ID. This leaves the SENT bus in a high state for a varying duration before the sensor pulls the line low to begin the SENT frame. All sensors on the bus (including the addressed sensor) measure this time to interpret the sensor ID of the transmitting sensor. By comparing this to the slot counter, each sensor can recognize if an unexpected sensor responded to the addressing pulse. By default, the sensor would then go offline, because it cannot be known which sensor is out of sync. This option increases the overhead on the bus and therefore reduces the maximum rate at which sensors can be polled. Slot marking increases the polling time of a sensor by the slot marking time for that sensor. All sensors on a bus must be configured with the same choice for this option.

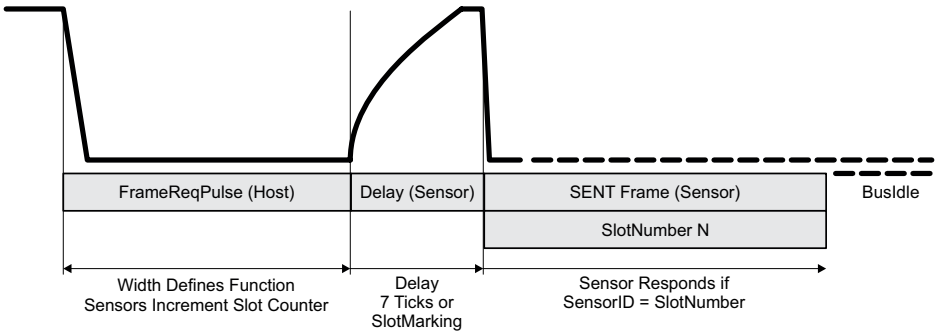


Figure 47: SSENT Sensor Addressing

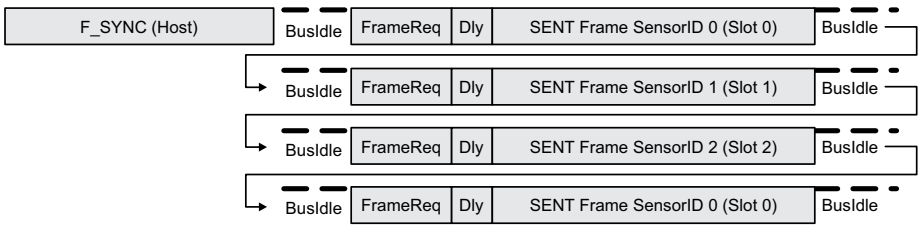


Figure 48: SSENT Sensor Addressing—No Slot Marking (Three Sensors on Bus)

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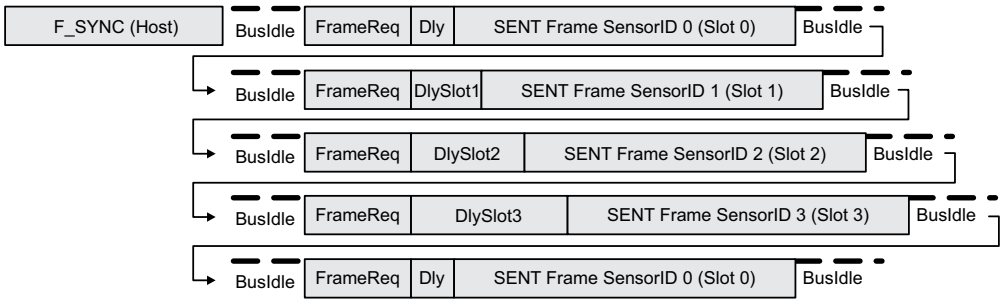


Figure 49: SSENT Sensor Addressing—With Slot Marking (Four Sensors on Bus)

Table 31: Slot Marking Delay Time

Sensor ID	Delay Time in Ticks (Nominal) [1]
0	7
1	18
2	36
3	62

[1] Delay time not intended for use by host. Tick values are approximate and differ from part to part due to oscillator variance.

- POR offline (set via PWS.PO). When enabled, a sensor stays offline until the host issues F_SYNC, or one of the other synchronization options takes effect (C_IDLE_SYNC). If disabled, a sensor powers-up with its slot counter set to 0 and goes directly online. This allows the sensors to initialize without any host interaction. However, if a sensor undergoes a power-on-reset after the bus is in operation, its counter may be out of sync with other sensors, and this could result in bus contention.
- Idle sync (set via PWS.IS). When enabled, a sensor monitors the bus for a long high (bus idle) period greater than 510 ticks and resets its slot counter to 0. This option can be used if sensor polling is expected to always be periodic and continuous, such that the only extended bus idle time follows power-up.

SSENT FUNCTION PULSES

- F_OUTPUT: Addressed sensor returns a SENT frame with sampled magnetic data. If data from a sample-and-hold operation is available (F_SAMPLE or via SEN.ZS = 1), that data is returned. Otherwise, current data is sampled and returned. A sensor configured with SEN.ZS = 1 performs a sample-and-hold on the rising edge of the F_OUTPUT pulse for slot 0. A sensor configured with SEN.NS = 1 and SEN.ZS = 0 never performs a sample-and-hold, so it always returns current data in response to F_OUTPUT.
- F_SAMPLE: All sensors except those configured for SEN.NS = 1 sample-and-hold their data at the rising edge of the pulse. If SEN.FA = 0, this is a broadcast pulse to a sensor, and that sensor does not respond. If SEN.FA = 1, this is also an addressing pulse to a sensor, and the addressed sensor returns a SENT frame with either the sampled or current data. SAMPLE_ADR must be configured the same for all parts on the bus.
- F_SYNC: All sensors synchronize their slot numbers by setting their slot counters such that the next addressing pulse is for slot 0.

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ADDRESSABLE SENT (ASENT)

ASENT Addressing Protocol

The ASENT protocol allows sensors to be polled in an arbitrary order. Following any addressing pulse, the sensor ID is transmitted by the host as a series of 0, 1, 2, or 3 incremental address (IncAdr) pulses. After this sequence, the SENT line is left in a high state, and—after a time period of approximately 18 nominal ticks—each sensor recognizes that no more incremental address pulses are coming. The sensor whose ID matches the number of incremental address pulses received responds.

ASENT Function Pulses

- F_OUTPUT: Addressed sensor returns a SENT frame with sampled magnetic data. If data is available from a sample-and-hold operation (F_SAMPLE), that data is returned. Otherwise, current data is sampled and returned. A sensor configured with SEN.NS = 1 does not perform a sample-and-hold, so it always returns current data in response to F_OUTPUT.
- F_SAMPLE: All sensors except those configured for SEN.NS = 1 sample-and-hold their data at the rising edge of the pulse. If SEN.FA = 0, this is a broadcast pulse to a sensor, and that sensor does not respond. If SEN.FA = 1, this is also an addressing pulse to a sensor, and the addressed sensor returns a SENT frame with either the sampled or current data. SAMPLE_ADR must be configured the same for all parts on the bus.
- F_DIAG: Sensor(s) enter self-test diagnostics based on SEN.DA. If configured with SEN.DA = 0, the sensor treats F_DAIG as a broadcast pulse, does not respond, and immediately enters diagnostics. If configured with SEN.DA = 1, the sensor treats F_DIAG as an addressing pulse. The addressed sensor does not respond but enters diagnostic mode.

ASENT Host Requirements

- The host must initiate SENT frame output by selecting appropriate function pulses.
- The host must detect timeouts or SENT frame contention following any function pulse and must take appropriate recovery action.

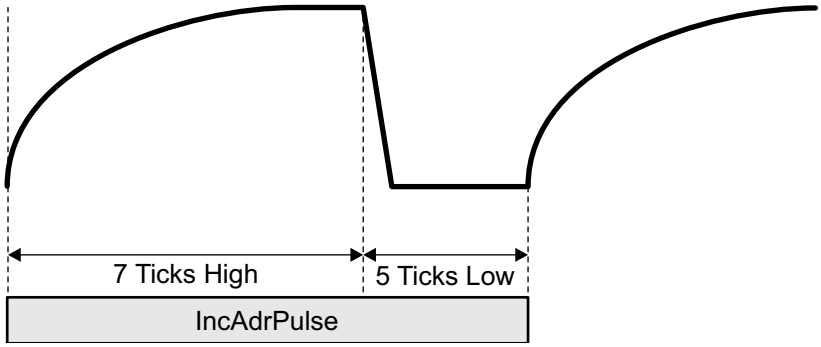


Figure 50: ASENT Incremental Address Pulse (IncAdrPulse) (Output by Host)

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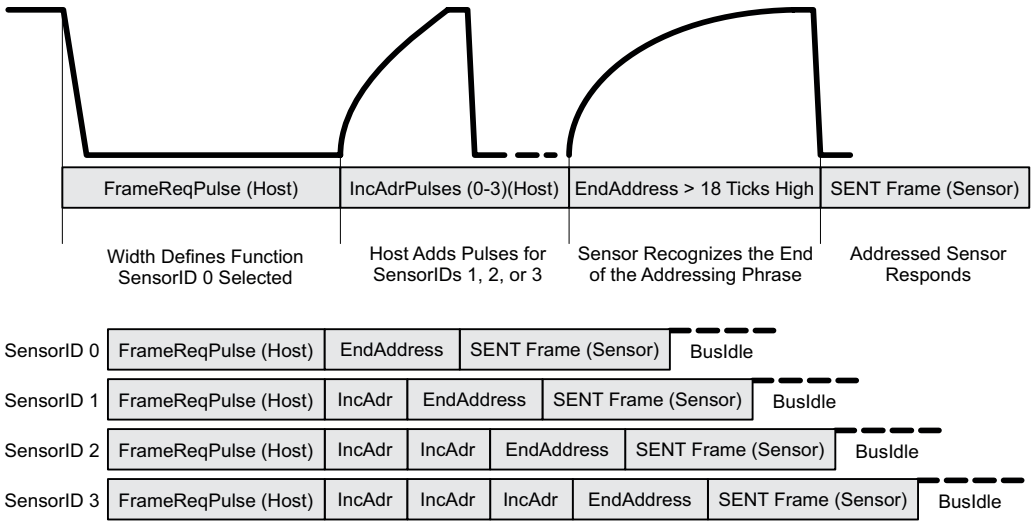


Figure 51: ASENT Sensor Addressing

SENSOR MAGNETIC DATA SAMPLING

Sensors sample their magnetic data based on a combination of the function pulse and the configuration options. Two types of sampling are supported: sample-on-output and sample-and-hold.

Sample-on-Output

Sample-on-output is when the sensor samples magnetic data within a short time period preceding the transmission of that data in the SENT frame. This provides the host with a minimal latency between the data sample and its reception at the host. The sensor uses sample-on-output in the following case:

- An F_OUTPUT function is addressed to that sensor and no held data is present.

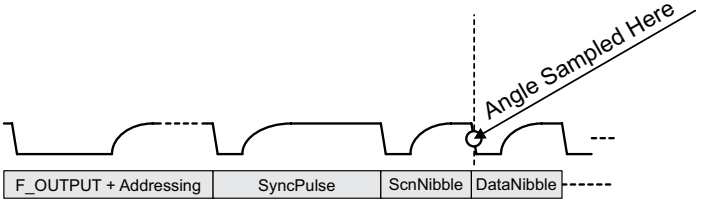


Figure 52: Sample-on-Output Example

Sample-and-Hold

Sample-and-hold is when the sensor samples magnetic data on the rising edge of a specific function pulse and holds it for output in a SENT frame later in time, when addressed. This allows the data sampling from multiple sensors to be synchronized, with the tradeoff in latency. The sensor performs a sample-and-hold of its magnetic data in the following cases:

- An F_SAMPLE function is broadcast, unless the sensor is configured with SEN.NS = 1.
- The host initiates an F_OUTPUT function in SSENT mode, the slot number is for sensor ID 0, and the sensor is configured with SEN.ZS = 1.

Once the sensor has data held from a sample-and-hold, it transmits it in the SENT frame the next time it is addressed. If the sensor is again polled before another sample-and-hold, that sensor returns the same data unless certain events intervene, in which case the sample-and-hold data is discarded. These events are:

- A diagnostic is executed that prevents the SENT interface from obtaining valid magnetic data from sensor logic (CVH_SELFTEST).
- If the SENT line is taken over by the receipt of a Manchester access code, the SENT interface is disabled.

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If a sensor is polled and sample-and-hold data is not available (for instance, if the part comes online after a sample-and-hold has been issued), it samples current data. It is not required that all sensors on a shared bus be configured the same for sampling. This allows a subset of the sensors on a shared bus to be synchronized for data sample, while others always perform sample-on-output.

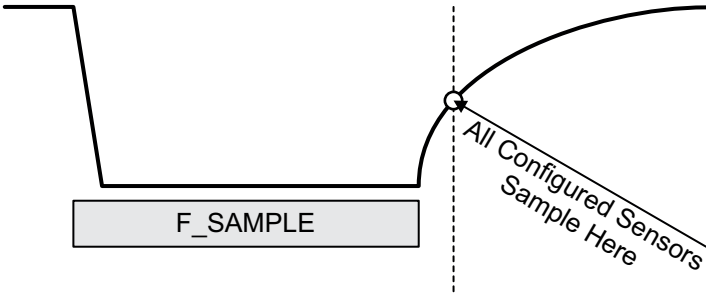


Figure 53: Sample-and-Hold (SSENT or ASENT)

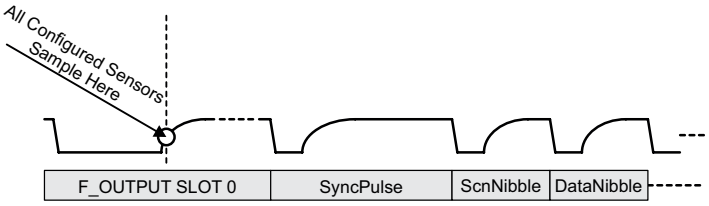


Figure 54: Sample-and-Hold

SSENT with ZERO_SAMPLE = 1

SENSOR STATES: OFFLINE, BUS SYNC, AND ONLINE

Offline

Offline is when the sensor is not actively interpreting the state of a shared SENT bus. In the offline state, the sensor does not drive the SENT bus. A sensor is offline:

- When unpowered.
- After power-up.
- After a reset that would reset the SENT logic (POR).
- During CVH self-test.
- After a bus contention is detected (unless stated otherwise).

The sensor exits the offline state into the bus synchronization state once its SENT logic becomes functional, after it monitors the SENT bus long enough to flush any internal synchronization or filtering pipelines and observes the SENT bus high. This is necessary to guarantee that any subsequent low pulses are measured as their full duration.

Bus Synchronization

Bus synchronization is the state in which the sensor determines to which addressing pulse it should respond. For ASENT, this state is unnecessary, and the sensor immediately transitions from offline to online. For SSENT, the sensor first monitors the SENT bus until it can synchronize its slot counter to the other sensors on the bus before responding to any addressing pulses, but always responds to broadcast pulses, even in the bus synchronization state.

A sensor configured for SSENT sets its slot counter, exits the bus synchronization state, and enters the online state when:

- The host issues an F_SYNC pulse. The sensor immediately knows the next slot is for sensor ID 0 and can then respond correctly.
- IDLE_SYNC is enabled, and the bus is high (bus idle state) for at least a fixed (greater than 510 ticks) period of time.
- PWS.PO = 0, and the sensor exits power-on-reset.
- Slot synchronization is enabled (SEN.SS = 1) with slot marking enabled for all other devices on the bus.
- The IC synchronizes its slot counter based on the observed slot marking of the other die on the bus.

Online

In the online state, the sensor actively interprets the shared bus, looking for and responding to function pulses. From online, a sensor goes offline when:

- It is powered-down or reset.
- It responds to a CVH self-test diagnostic request.
- It detects a bus contention (SSENT mode).

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SENT Message Frame Descriptions

The general format of a SENT message frame is shown in Figure 37. The individual sections of a SENT message are described in Table 32.

Table 32: SENT Message Frame Section Definitions

Section	Description
Synchronization and Calibration	
Function	Provide the external controller with a detectable start of the message frame. The large quantity of ticks distinguishes this section, for ease of distinction by the external controller.
Syntax	Tick count: 56
Status and Communication	
Function	Provides the external controller with the status of the A33002 and indicates the format and contents of the data section.
Syntax	Nibbles: 1 Tick count: 12 to 27; Field width: 4 bits 1:0 Device status (indicates either a hard or soft error condition) 3:2 Message serial data protocol (set by SCN_MODE parameter)
Data	
Function	Provides the external controller with data selected by the SENT_DATA parameter.
Syntax	Nibbles: 3 to 6 Tick count: 12 to 27 (each nibble) Field width: 4 bits (each nibble)
CRC	
Function	Provides the external controller with cyclic redundancy check (CRC) data for certain error detection routines applied to the data nibbles.
Syntax	Nibbles: 1 Tick count: 12 to 27 (each nibble) Field width: 4 bits
Pause Pulse	
Function	Additional time can be added at the end of a SENT message frame to synchronize each SENT message with the internal angle measurement updates.
Syntax	Quantity of ticks: 12 tick minimum and 768 tick maximum (If a pause pulse reaches 768 ticks, it restarts with a minimum length of 12 ticks) Quantity of bits: n/a

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SENT Data Programming Parameters

Table 33: SCN_MODE (Register Address: 0x19, bits 6:4)

Function	Status and communication nibble (SCN) format Defines role of bits within the status and communication nibble
Syntax	Field width: 3 bits
Related Commands	–
Values	

SCN_MODE	Bit 3	Bit 2	Bit 1	Bit 0
000	0	0	SOFT	HARD
001	SERIALSYNC	SERIALDATA	SOFT	HARD
010	ID[1]	ID[0]	SOFT	HARD
011	0	0	0	SOFT+HARD
100	0	0	ID[1]	ID[0]
101	SERIALSYNC	SERIALDATA	ID[1]	ID[0]
110	SOFT	HARD	ID[1]	ID[0]
111	SERIALSYNC	SERIALDATA	0	SOFT+HARD

Options	–
Examples	The SERIALSYNC and SERIALDATA bits form a 16-bit message, transmitted over 16 consecutive SENT frames. The message contents are arranged as:

SCN Bit	Nibble #															
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
SERIALSYNC	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SERIALDATA	MESSAGE ID				DATA								CRC			

Short Serial Message

Table 34: SDRV (Register Address: 0x1B, bits 6:4)

Function	Output signal configuration Sets configuration of the output signal slew-rate control. Sets the ramp rate on the gate of the output driver, thereby changing slew rate at the output.
Syntax	Field width: 3 bits
Related Commands	–
Values	

Code	Fall Time (80% to 20% Typical Values) (µs)	
	C_{LOAD} = 100 pF	C_{LOAD} = 1 nF
000 (Default)	0.031	0.102
001	0.075	0.105
010	0.130	0.226
011	0.180	0.296
100	0.460	0.622
101	0.930	1.100
110	1.900	1.900
111	2.900	2.700

Options	–
Examples	–

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Table 35: DATA_MODE (Register Address: 0x19, bits 11:8)

Function	DATA nibble format Quantity and contents of DATA nibbles in message. (Does not relate to data contained in the status and communication nibble.)
Syntax	Field width: 4 bits
Related Commands	–
Values	0: Nibbles 1,2,3: Angle data (Nibbles 4,5,6 skipped) 1: Nibbles 1,2,3: Angle data Nibbles 4,5: Status bits; alternates between two 8-bit words 2: Nibbles 1,2,3: Angle data Nibbles 4,5,6: Rotating extended data (see the Short Serial Message Format section) 3: Nibbles 1,2,3: Angle data Nibbles 4,5,6: Turns count data 4: Nibbles 1,2,3: Angle data Nibbles 4,5: Status bits; alternates between two 8-bit words Nibble 6: Alive counter 5: Nibbles 1,2,3: Angle data Nibbles 4,5: Eight-bit alive counter Nibble 6: One's complement of Nibble 1 6: Nibbles 1,2,3,4: Angle data 7: Nibbles 1,2,3,4: Angle data Nibble 5: Status bits; alternates between four 4-bit words. Nibble 6: Alive counter 8: Nibbles 1,2,3: Angle data Nibble 4: Self-test and ID 9: Nibbles 1,2,3: Angle data Nibbles 4,5: Status bits; alternates between two 8-bit words. 10: Nibbles 1,2,3: Angle data Nibbles 4,5: Rotating extended data (see the Short Serial Message Format section) Nibble 6: Self-test and ID 11: Nibbles 1,2,3: Angle data Nibbles 4,5: Eight-bit turns counter Nibble 6: Self-test and ID 12: Nibbles 1,2,3: Angle data Nibbles 4,5: Status bits; alternates between two 8-bit words. Nibble 6: Self-test and ID 13: Nibbles 1,2,3: Angle data Nibble 4: Alive counter Nibble 5: One's complement of Nibble 1 Nibble 6: Self-test and ID 14: Nibbles 1,2,3,4: Angle data Nibble 5: Self-test and ID 15: Nibbles 1,2,3,4: Angle data Nibble 5: Alive counter Nibble 6: Self-test and ID
Options	–
Examples	–

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Table 36: SENT_MODE (Register Address: 0x19, bits 14:12)

Function	Selects between the various SENT update rates. Also used to select various modes of triggerable SENT.
Syntax	Field width: 3 bits
Related Commands	–
Values	000: Disable, no SENT output. 001: No pause pulse; new frame immediately follows previous frame. 010: SENT message frame synchronized to internal angle update rate. Pause pulse inserted to ensure each new SENT transmission corresponds to a fresh angle sample. 011: Triggered SENT mode (TSENT). Pause pulse held indefinitely until receipt of trigger pulse (OUT pulled low) from the controller. SENT message begins once output is released. Data latched near end of SCN. 100: Triggered SENT mode (TSENT). Pause pulse held indefinitely until receipt of trigger pulse (OUT pulled low) from the controller. SENT message begins once output is released. Data latched on falling edge of trigger. 101: Addressable SENT mode (ASENT). See the Shared SENT Protocol section. 110: Sequential SENT mode (SSENT). See the Shared SENT Protocol section. 111: Long SSENT. Supports alternative SENT line sharing protocol. See the Shared SENT Protocol section.
Options	–
Examples	–

Table 37: SENT_TICK (Register Address: 0x19, bits 22:16)

Function	Tick Duration Sets the SENT tick time: SENT_TICK/16 MHz = tick (µs)		
Syntax	Field width: 7 bits Any value from 0 to 127 can be used (although an internal limit of one clock period is forced).		
Related Commands	–		
Values	Code	Tick Time (µs)	Coefficient
	000 0000 [1]	0.0625	1/16 (a minimum of one clock period is forced internally)
	000 0001 [1]	0.0625	1/16
	000 0010 [1]	0.125	2/16
	000 0011 [1]	0.1875	3/16
	000 0100 [1]	0.25	4/16
	000 1000	0.5	8/16
	001 0000	1	16/16
	001 1000	1.5	24/16
	011 0000	3	48/16
	110 0000	6	96/16
	111 1110	7.875	126/16
	111 1111	7.9375	127/16
Options	–		
Examples	–		

[1] Tick times shorter than 0.5 µs are not guaranteed.

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Table 38: CIS (Register Address: 0x19, bit 7)

Function	SENT CRC includes the status and communication nibble (SCN)
Syntax	Field width: 1 bit
Related Commands	–
Values	0: SCN is not included in the CRC nibble. 1: SCN bits are covered via the CRC nibble (does not conform to the SAE J2716 SENT standard)
Options	–
Examples	–

ASENT/SSENT SPECIFIC FIELDS

Table 39: DA (Register Address: 0x19 bit 1)

Function	Treat F_DIAG as an addressing pulse.
Syntax	Field width: 1 bit
Related Commands	–
Values	0: F_DIAG is treated as a broadcast pulse. Sensor enters diagnostic mode on any F_DIAG pulse (if UI = 1) 1: F_DIAG is treated as an addressing pulse. Sensor only enters diagnostic mode if properly addressed
Options	–
Examples	–

Table 40: MAXID (Register Address: 0x19, bits 25:24)

Function	Specifies highest sensor ID number on the shared SENT bus
Syntax	Field width: 2 bits
Related Commands	–
Values	00: Highest ID value is 0. Sensor is not sharing the SENT line 01: Highest ID value is 1. Two sensors are sharing the SENT line 10: Highest ID value is 2. Three sensors are sharing the SENT line 11: Highest ID value is 3. Four sensors are sharing the SENT line
Options	–
Examples	–

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Table 41: NS (Register Address: 0x19, bit 3)

Function	No sample. Sensor does not sample angle on receipt of an F_SAMPLE pulse
Syntax	Field width: 1 bit
Related Commands	–
Values	0: On receipt of an F_SAMPLE pulse, sensor samples-and-holds angle data 1: Sensor does not sample-and-hold data on receipt of an F_SAMPLE pulse
Options	–
Examples	–

Table 42: FA (Register Address: 0x19, bit 0)

Function	F_SAMPLE addressing. Sensor treats the F_SAMPLE pulse as an addressing pulse
Syntax	Field width: 1 bit
Related Commands	–
Values	0: F_SAMPLE is treated as a broadcast pulse. Sensor samples-and-holds angle data on any F_SAMPLE pulse (unless NS = 1) 1: F_SAMPLE is treated as an addressing pulse. Sensor only samples-and-holds angle data on an F_SAMPLE pulse if properly addressed (unless NS = 1)
Options	–
Examples	–

SSENT SPECIFIC FIELDS

Table 43: IS (Register Address: 0x1B, bit 8)

Function	IDLE_SYNC. Sensor resets slot counter if SENT bus idle persists for more than 510 ticks (SSENT only).
Syntax	Field width: 1 bit
Related Commands	–
Values	0: Sensor takes no action for an idle SENT line 1: If SENT line is idle for greater than 510 ticks, internal slot counter is reset to 0. All sensors sharing a SENT line should have matching IS settings
Options	–
Examples	–

Table 44: PO (Register Address: 0x1B, bit 7)

Function	POR_OFFLINE. Sensor stays offline after power-on-reset (SSENT only).
Syntax	Field width: 1 bit
Related Commands	–
Values	0: After a power-on-reset, sensor goes online with a slot counter of 0 1: Sensor stays offline following a power-on-reset. Sensor goes online after slot counter synchronization via an F_SYNC pulse or IDLE_SYNC
Options	–
Examples	–

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Table 45: SM (Register Address: 0x19, bit 15)

Function	SLOT_MARKING enable (SSENT only).
Syntax	Field width: 1 bit
Related Commands	–
Values	0: No slot marking pulses 1: Sensor outputs a bus high delay after an addressing pulse, based on sensor ID
Options	–
Examples	–

Table 46: ZS (Register Address: 0x19, bit 2)

Function	ZERO_SAMPLING. Sensor performs sample-and-hold data at slot 0 (SSENT only)
Syntax	Field width: 1 bit
Related Commands	–
Values	0: No special action at slot = 0 1: Sensor performs a sample-and-hold when its slot counter resets to 0
Options	–
Examples	–

Table 47: FP_ADJ (Register Address: 0x1B, bits 25:24)

Function	Function pulse adjust. Only for long SSENT (SENT_MODE = 7). Increases the lower threshold of F_OUTPUT pulse by zero to three ticks. Reduces possible misinterpretation of F_OUTPUT pulses at sub-1.5 µs tick times
Syntax	Field width: 2 bits
Related Commands	–
Values	00: No change to F_OUTPUT pulse width. Minimum width = 9 ticks 01: Minimum width of F_OUTPUT increased by 1 Tick. Min = 10 ticks 10: Minimum width of F_OUTPUT increased by 2 Ticks. Min = 11 ticks 11: Minimum width of F_OUTPUT increased by 3 Ticks. Min = 12 ticks
Options	–
Examples	–

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APPENDIX B: ANGLE ERROR AND DRIFT DEFINITION

Angle error is the difference between the actual position of the magnet and the position of the magnet as measured by the angle sensor IC (without noise). This measurement is performed by reading the angle sensor IC output and comparing it with a high-resolution encoder. Refer to Figure 55.

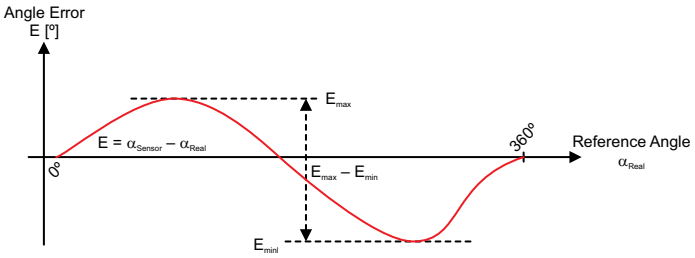


Figure 55: Angle Error Definition

Angle Error Definition

Throughout this document, the term “angle error” is used extensively. Thus, it is necessary to introduce a single angle error definition for a full magnetic rotation. The term “angle error” is calculated according to:

$$AngleError = max(|E_{max}| , |E_{min}|)$$

In other words, it is the amplitude of the deviation from a perfect straight line between 0 degrees and 360 degrees. For the purpose of a generic definition, the offset of the IC angle profile is removed prior to the error calculation, as shown in Figure 55. The offset itself depends on the starting IC angle position relative to 0 degrees of the encoder and, thus, can differ anywhere from 0 degrees to 360 degrees.

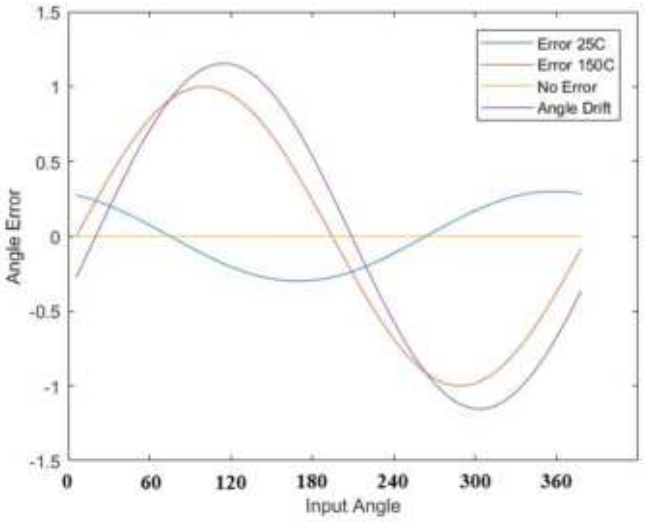
Angle Drift

Angle drift is the change in the observed angular position over temperature, relative to 25°C.

During Allegro’s factory trim, drift is measured at 150°C. The value is calculated using:

$$Angle_{Drift} = Angle_{25°C} - Angle_{150°C}$$

where each angle value is an array corresponding to 16 angular positions around a circle.



NOTE 1: Simple angle drift is represented, not real data.

NOTE 2: Error at 25°C and 150°C is often out of phase. This can cause a drift larger than the maximum error specification of the part.

Figure 56: Angle Drift of 150°C in Reference to 25°C

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REVISION HISTORY

Number	Date	Description
–	October 12, 2018	Initial release
1	December 17, 2018	Updated dual die pinout diagram (page 4), Supply Current (page 6), SENT Output Trigger Thresholds (page 7), Magnetic Field (page 8), Figure 6 (page 14), Turns Counting Behavior on Power-Up (page 20), Oscillator Watchdogs (page 50), and Package Outline Drawings (pages 52-53)
2	June 17, 2019	Updated SPI Output High Voltage test conditions (page 6) and Table 16 (page A-2); Added PWM Output Impedance and SENT Output Impedance characteristics (page 7)
3	October 18, 2019	Updated Figure 6 (page 14), Turns Counting section (page 19), PWS.h2t (page 45), and PWS.phe (page 46) EEPROM references.
4	May 1, 2020	Updated Magnetic Field unit and footnote 11 (page 8); Updated Linearization section (pages 15-16); Updated Turns Counting Behavior on Power-Up section (page 20); Updated Interface Structure section (page 23); Updated SPI Interface Voltage Levels section (page 23); Updated CRC section (page 28); Added SPI Interface characteristics table (page 29); Updated Figure 23 (page 30); Added Controller Manchester Message Structure section (page 31); Added Sensor Manchester Message Structure section (page 32); Added Manchester Access Code section (page 32); Added Manchester Exit Code section (page 33); Added Manchester Read Command section (page 33); Added Manchester Read Response section (page 34); Added Manchester Read Response Delay section (page 34); Added CRC section (page 35); Updated EEPROM and Shadow Memory Usage section (pages 38-44); Updated Primary Serial Interface Registers Reference (pages 46-59); Updated EEPROM Table and Reference (pages 60-72); Updated Safety and Diagnostics section (page 73); Updated Active Area Depth values in Package Outline Drawings (pages 75-76); Updated Appendix A; Removed Appendix B and updated Appendix C to Appendix B; Updated Appendix B Angle Error Definition equation (page B-1).
5	October 14, 2020	Updated sent_mode[14:12] table (page 63) and fp_adj[25:24] description (page 66).
6	March 26, 2021	Updated ASIL status (page 1).
7	April 20, 2021	Updated Features and Benefits (page 2), Angle Measurement section (page 11), Table 9 (page 32), Address 0x34:0x35 (zang) description (page 57), Sent_tick[22:16] description (page 62), and SENT Output Mode table (page A-11)

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8	March 11, 2022	Updated Figure 1 (page 1), Address 0x1A PLK[7] (page 65), Address 0x1C RO[18] (page 68).
9	April 12, 2023	Updated reference design (page 5) and package outline drawings (pages 75 and 76), and made minor branding, editorial, and formatting updates throughout, including addition of hyperlinks/ cross-references and changes to archaic language (MOSI [MISO] redefined as Controller In [Out], Peripheral Out [In]), capitalization (minimized for most nouns, but all capitals for bit addresses), quotation marks (minimized or removed), and register addresses (all capitalized, no quotes).
10	May 14, 2024	Corrected reverse voltage specification (page 2), updated EEPROM margin test (page 41), and made minor editorial corrections, including changing the term "normal" to "typical" throughout.
11	June 9, 2025	Updated ASIL language and branding (page 1)
12	July 8, 2026	Updated footnotes of thermal characteristic table (page 2), made formatting changes throughout (content not changed), and made minor editorial corrections

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