A6217 and A6217-1

Automotive-Grade, Constant-Current PWM Dimmable Buck Regulator LED Driver

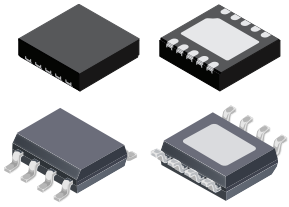
FEATURES AND BENEFITS

- AEC-Q100 qualified
- 6 to 48 V supply voltage
- True average output current control
- 3 A maximum output over operating temperature range (1.5 A for A6217-1)
- Cycle-by-cycle current limit
- Integrated MOSFET switch
- Enable / PWM dimming via direct logic input or power supply voltage
- Internal control loop compensation
- Undervoltage lockout (UVLO) and thermal shutdown protection
- Low power shutdown (1 µA typical)
- Robust protection against:
  - Adjacent pin-to-pin short
  - Pin-to-GND short
  - Component open/short faults
- Enhancements over A6213:
  - Dithering of switching frequency to reduce EMI
  - Able to drive single white LED from 18 V supply at 2.2 MHz
  - Smaller package option

PACKAGES:

10-pin DFN with wettable flank (suffix EJ)

8-pin SOICN (suffix LJ)



Not to scale

DESCRIPTION

The A6217 is a single IC switching regulator that provides constant-current output to drive high-power LEDs. It integrates a high-side N-channel DMOS switch for DC-to-DC step- down (buck) conversion. A true average current is output using a cycle-by-cycle, controlled on-time method.

Output current is user-selectable by an external current sense resistor. Output voltage is automatically adjusted to drive various numbers of LEDs in a single string. This ensures the optimal system efficiency.

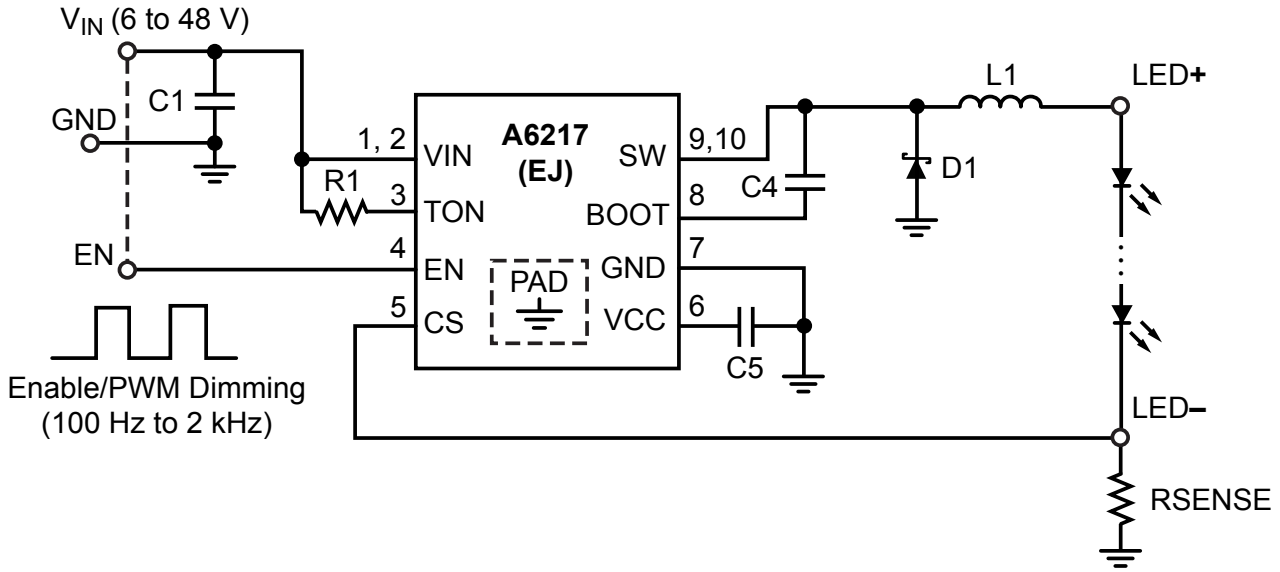
LED dimming is accomplished by a direct logic input pulse-width-modulation (PWM) signal at the enable pin.

The device is provided in a 3 mm × 3 mm wettable flank 10-pin DFN (suffix EJ) or an 8-pin narrow SOIC (suffix LJ), both with exposed pad for enhanced thermal dissipation. Both packages are lead (Pb) free, with 100% matte-tin leadframe plating.

APPLICATIONS:

Automotive lighting
- Daytime running lights
- Front and rear fog lights
- Turn/stop lights
- Map light
- Dimmable interior lights

TYPICAL APPLICATION CIRCUIT



SELECTION GUIDE

Part Number	Maximum Output Current (A)	Package	Packing
A6217KEJTR-J [1]	3	Wettable flank 10-pin DFN with exposed thermal pad	Contact Factory
A6217KEJTR-1-J	1.5	Wettable flank 10-pin DFN with exposed thermal pad	Contact Factory
A6217KLJTR-T	3	8-pin SOICN with exposed thermal pad	3000 pieces per 13-in. reel
A6217KLJTR-1-T	1.5	8-pin SOICN with exposed thermal pad	3000 pieces per 13-in. reel

[1] Part variant A6217KEJTR-J is no longer in production. This device should not be purchased for new design applications. Samples are no longer available. Status change date: September 30, 2024. Suggested replacement: A6217KEJTR-1-J.

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	V_{IN}		–0.3 to 50	V
Bootstrap Drive Voltage	V_{BOOT}		–0.3 to V_{IN} + 8	V
Switching Voltage	V_{SW}		–1.5 to V_{IN} + 0.3	V
Linear Regulator Terminal	V_{CC}	VCC to GND	–0.3 to 7	V
Enable and TON Voltage	V_{EN}, V_{TON}		–0.3 to V_{IN} + 0.3	V
Current Sense Voltage	V_{CS}		–0.3 to 7	V
Maximum Junction Temperature	T_J(max)		150	ºC
Storage Temperature	T_{stg}		–55 to 150	ºC

THERMAL CHARACTERISTICS*: May require derating at maximum conditions; see application section for optimization

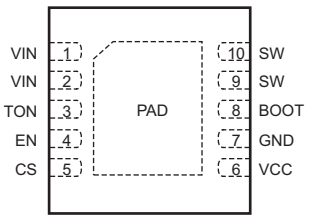
Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance (Junction to Ambient)	$R_{\theta JA}$	DFN-10 (EJ) package on 4-layer PCB based on JEDEC standard	45	ºC/W
		SOICN-8 (LJ) package on 4-layer PCB based on JEDEC standard	35	ºC/W
Package Thermal Resistance (Junction to Pad)	$R_{\theta JP}$		2	ºC/W

*Additional thermal information available on the Allegro™ website.

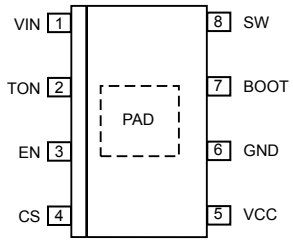
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PINOUT DIAGRAMS AND TERMINAL LIST

Pinout Diagrams



Package EJ Pinouts



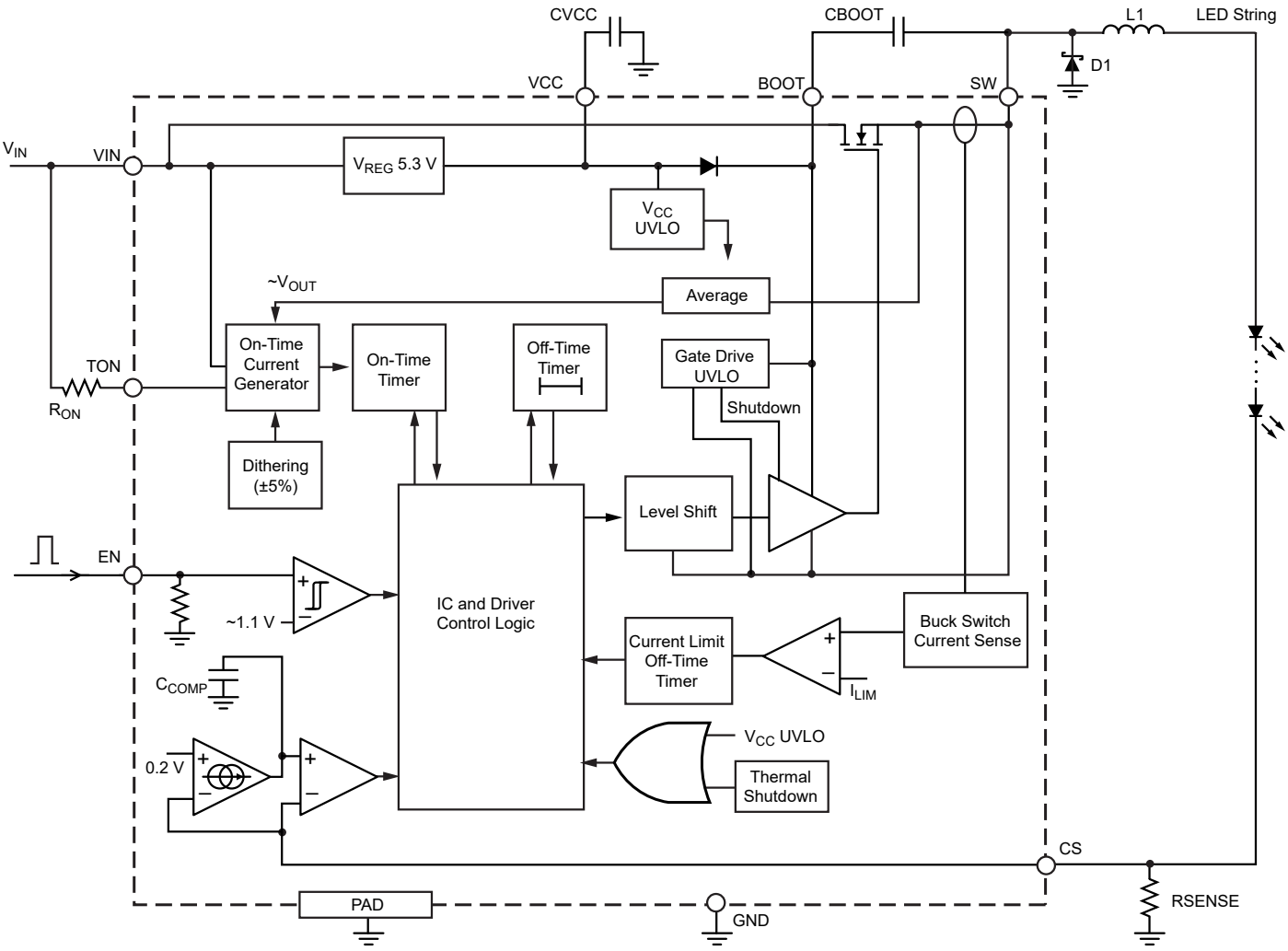
Package LJ Pinouts

Terminal List

Number		Name	Function
EJ	LJ		
1, 2	1	VIN	Supply voltage input terminals
3	2	TON	Regulator on-time setting resistor terminal; determines the switching frequency of the converter
4	3	EN	Input for Enable and PWM dimming; rated up to V_{IN} and logic-level compatible
5	4	CS	Drive output current sense feedback
6	5	VCC	Internal linear regulator output; add filter capacitor of 0.1 µF from this pin to GND
7	6	GND	Ground terminal
8	7	BOOT	DMOS gate driver bootstrap terminal
9, 10	8	SW	Switched output terminals
–	–	PAD	Exposed pad for enhanced thermal dissipation; connect to GND

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FUNCTIONAL BLOCK DIAGRAM



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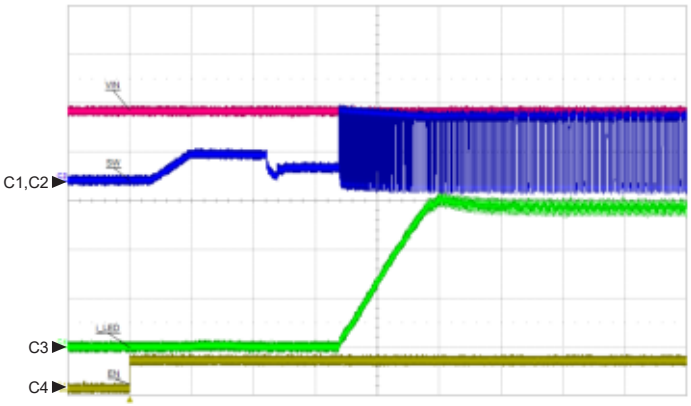
ELECTRICAL CHARACTERISTICS: Valid at V_{IN} = 12 V, T_J = –40°C to 125°C, typical values at T_J = 25°C, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input Supply Voltage	V_{IN}		6	–	48	V
V_{IN} Undervoltage Lockout Threshold	V_{UVLO}	V_{IN} increasing	–	5.3	–	V
V_{IN} Undervoltage Lockout Hysteresis	V_{UVLO_HYS}	V_{IN} decreasing	–	150	–	mV
VIN Pin Supply Current	I_{IN}	VCS = 0.5 V, EN = High	–	2.5	–	mA
VIN Pin Standby Current	I_{INSB}	V_{CS} = 0.5 V, EN = high to low, within 10 ms	–	1	–	mA
VIN Pin Shutdown Current	I_{INSD}	EN shorted to GND	–	1	10	µA
Buck Switch Current Limit Threshold	I_{SWLIM}	A6217	3.0	4.0	5.0	A
		A6217-1	1.9	2.2	2.7	A
Buck Switch On-Resistance	$R_{DS(on)}$	V_{BOOT} = V_{IN} + 4.3 V, T_A = 25°C, I_{SW} = 1 A	–	0.25	0.4	Ω
BOOT Undervoltage Lockout Threshold	V_{BOOTUV}	V_{BOOT} to V_{SW} increasing	2.7	3.5	4.3	V
BOOT Undervoltage Lockout Hysteresis	$V_{BOTUVHYS}$	V_{BOOT} to V_{SW} decreasing	–	370	–	mV
Switching Minimum Off-Time	t_{OFFmin}	V_{CS} = 0 V	–	110	150	ns
Switching Minimum On-Time	t_{ONmin}		–	75	100	ns
Selected On-Time	t_{ON}	V_{IN} = 12 V, V_{OUT} = 6 V, R_{ON} = 31.6 kΩ	200	250	300	ns
Oscillator Frequency Dithering Range	f_{SW_DITH}	R_{ON} = 31.6 kΩ	–	±5	–	%
Dithering Modulation Frequency	f_{SW_MOD}	R_{ON} = 31.6 kΩ	–	11	–	kHz
REGULATION COMPARATOR AND ERROR AMPLIFIER						
Load Current Sense Regulation Threshold [1]	V_{CSREG}	V_{CS} decreasing, SW turns on	187.5	200	210	mV
Load Current Sense Bias Current	I_{CSBIAS}	V_{CS} = 0.2 V, EN = low	–	0.9	–	µA
INTERNAL LINEAR REGULATOR						
VCC Regulated Output	V_{CC}	0 mA < I_{CC} < 5 mA, V_{IN} > 6 V	5.1	5.4	5.7	V
VCC Current Limit [2]	I_{CCLIM}	V_{CC} = 0 V	5	20	–	mA
ENABLE INPUT						
Logic High Voltage	V_{IH}	V_{EN} increasing	1.8	–	–	V
Logic Low Voltage	V_{IL}	V_{EN} decreasing	–	–	0.4	V
EN Pin Pull-Down Resistance	R_{ENPD}	V_{EN} = 5 V	–	100	–	kΩ
Maximum PWM Dimming Off-Time	t_{PWML}	Measured while EN = low, during dimming control, and internal references are powered on (exceeding t_{PWML} results in shutdown)	12	20	–	ms
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	T_{SD}		–	165	–	°C
Thermal Shutdown Hysteresis	T_{SDHYS}		–	25	–	°C

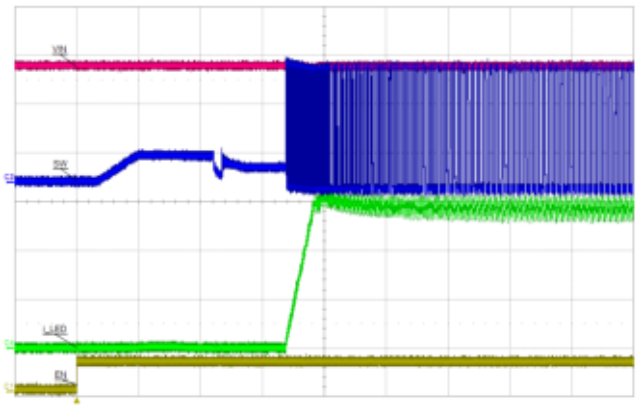
[1] In test mode, a ramp signal is applied at CS pin to determine the CS pin regulation threshold voltage. In actual application, the *average* CS pin voltage is regulated at V_{CSREG} regardless of ripple voltage.
[2] The internal linear regulator is not designed to drive an external load

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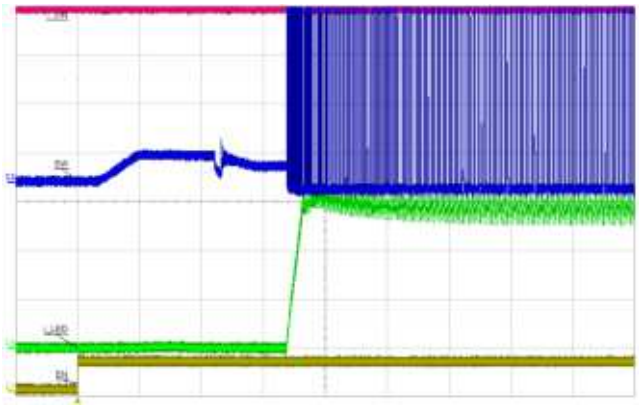
CHARACTERISTIC PERFORMANCE



Panel 1A. V_{IN} = 7 V



Panel 1B. V_{IN} = 12 V

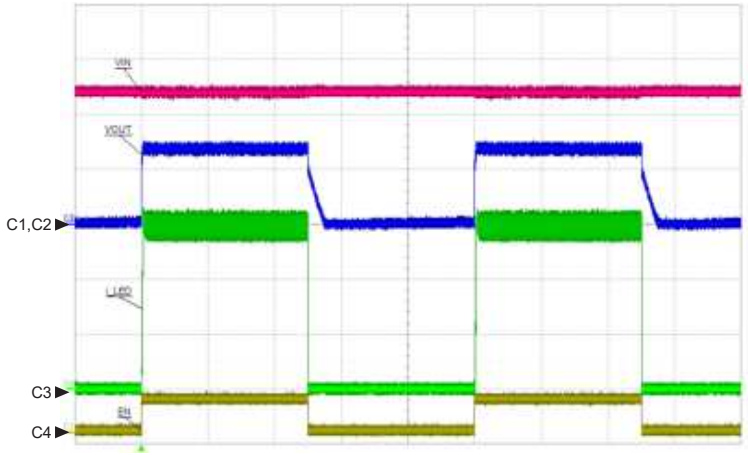


Panel 1C. V_{IN} = 18 V

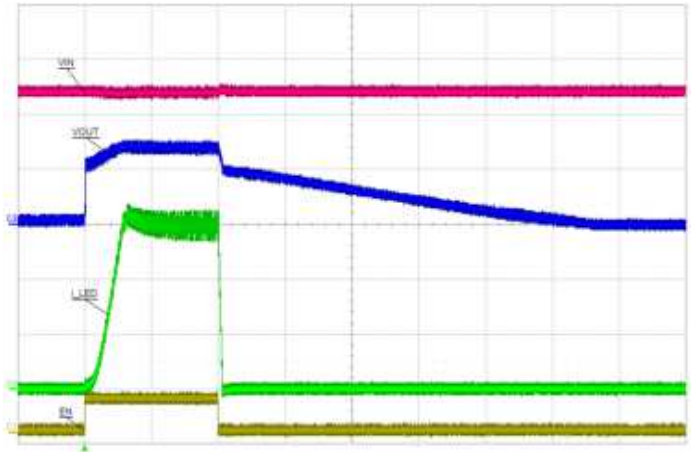
Figure 1: Startup waveforms from off-state at various input voltages. Note that there is a fixed startup delay of ~70 µs before switching starts. Subsequent rise time of the LED current depends on input/output voltages, inductor value, and switching frequency.

- Operating conditions: LED voltage = 3.5 V, LED current = 1.5 A, R_1 = 73.2 kΩ (frequency = 1 MHz in steady state), L1 = 15 µH, V_{IN} = 7 V (panel 1A), 12 V (panel 1B), and 18 V (panel 1C)
- Oscilloscope settings: CH1 (Red) = V_{IN} (5 V/div), CH2 (Blue) = V_{SW} (5 V/div), CH3 (Green) = i_{LED} (500 mA/div), CH4 (Yellow) = Enable (5 V/div), time scale = 20 µs/div

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Panel 2A. Duty cycle = 50% and time scale = 1 ms/div



Panel 2B. Duty cycle = 2% and time scale = 50 µs/div

Figure 2: PWM operation at various duty cycles; note that there is no startup delay during PWM dimming operation

- Operating conditions: PWM dimming at 200 Hz, V_{IN} = 12 V, V_{OUT} = 7 V, R1 = 73.2 kΩ, duty cycle = 50% (panel 2A) and 2% (panel 2B)
- CH1 (Red) = V_{IN} (5 V/div), CH2 (Blue) = V_{OUT} (5 V/div),
  CH3 (Green) = i_{LED} (500 mA/div), CH4 (Yellow) = Enable (5 V/div), time scale = 1 ms/div (panel 2A) and 50 µs/div (panel 2B)

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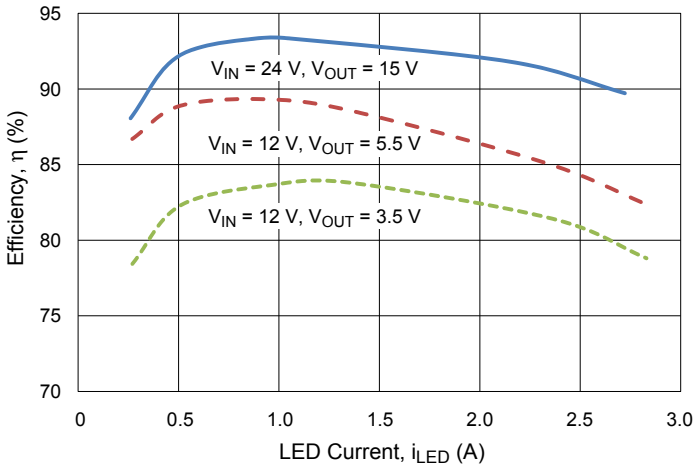


Figure 3: Efficiency versus LED Current at various LED voltages
Operating conditions: f_{SW} = 1 MHz

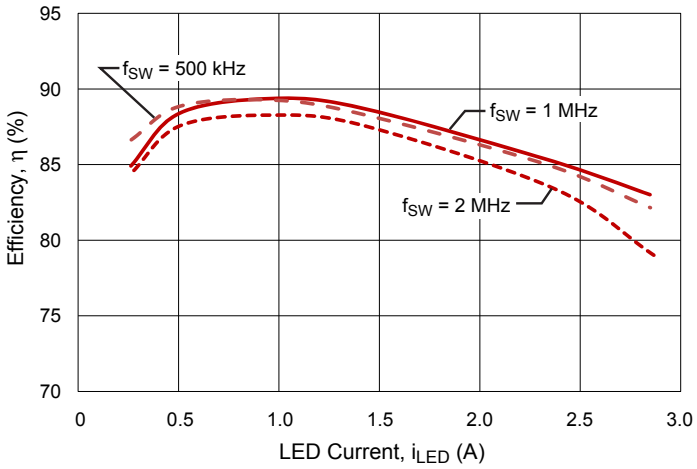


Figure 4: Efficiency versus LED Current at various switching frequencies. Operating conditions: V_{IN} = 12 V, V_{OUT} = 5.5 V

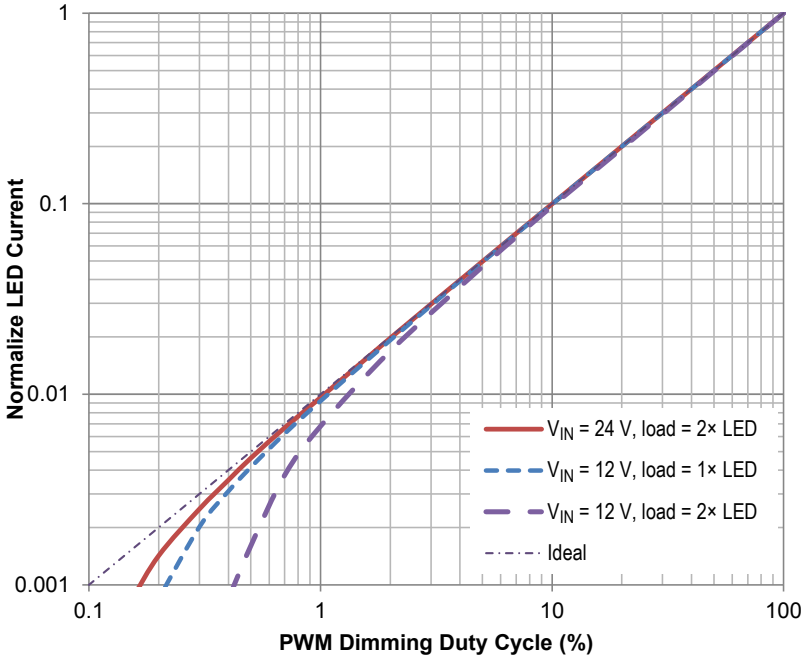


Figure 5. Average LED Current versus PWM dimming percentage
Operating conditions: V_{IN} = 12 or 24 V, V_{OUT} = 3.7 V (1× LED) or 7 V (2× LED), i_{LED} = 1.5 A, R_{ON} = 73.2 kΩ, f_{SW} = 1 MHz, L = 15 µH

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FUNCTIONAL DESCRIPTION

The A6217 is a buck regulator designed for driving a high-current LED string. It uses average current mode control to maintain constant LED current and consistent brightness. The LED current level is easily programmable by selection of an external sense resistor, with a value determined as follows:

$$i_{LED} = V_{CSREG} / R_{SENSE}$$

where V_{CSREG} = 0.2 V typical.

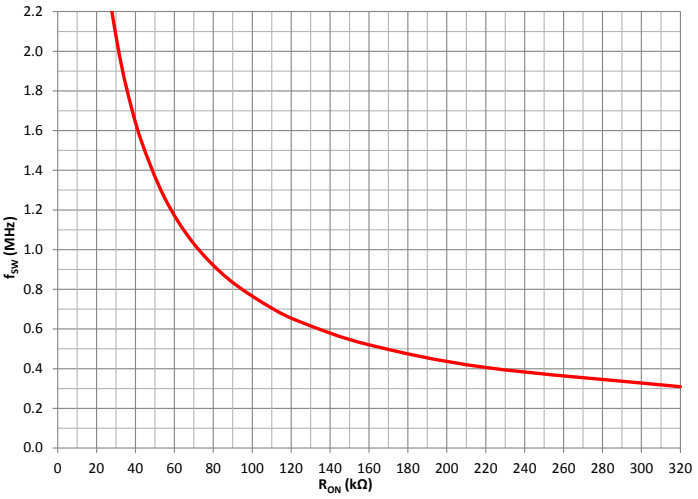


Figure 6: Average Switching Frequency versus R_{ON} Resistance (V_{IN} = 12 V, V_{OUT} = ~7 V, i_{LED} = 1 A)

Switching Frequency

The A6217 operates in fixed on-time mode during switching. The on-time (and hence switching frequency) is programmed using an external resistor connected between the VIN and TON pins, as given by the following equations:

$$t_{ON} = k \times (R_{ON} + R_{INT}) \times (V_{OUT} / V_{IN})$$

$$f_{SW} = 1 / [k \times (R_{ON} + R_{INT})] + c$$

where k = 0.014 and c = 0.09, with f_{SW} in MHz, t_{ON} in µs, and R_{ON} and R_{INT} (internal resistance, 6 kΩ) in kΩ (see figure 6).

To minimize the peaks of switching frequency harmonics in EMC measurement, a dithering feature is implemented. The dithering range is internally set at ±5%. The actual switching frequency is swept linearly between 0.95 × f_{SW} and 1.05 × f_{SW}, where f_{SW} is the programmed switching frequency. The rate of modulation for f_{SW} is fixed internally at ~11 kHz.

Enable and Dimming

The IC is activated when a logic high signal is applied to the EN (enable) pin. The buck converter ramps up the LED current to a target level set by RSENSE.

When the EN pin is forced from high to low, the buck converter is turned off, but the IC remains in standby mode for up to 12 ms. If EN goes high again within this period, the LED current is turned on immediately. Active dimming of the LED is achieved by sending a PWM (pulse-width modulation) signal to the EN pin. The resulting LED brightness is proportional to the duty cycle (t_{ON}/Period) of the PWM signal. A practical range for PWM dim-

• During SW on-time:

$$i_{RIPPLE} = [(V_{IN} - V_{OUT}) / L] \times t_{ON} = [(V_{IN} - V_{OUT}) / L] \times t_{SW} \times D$$

where D = t_{ON} / t_{SW}.

• During SW off-time:

$$i_{RIPPLE} = [(V_{OUT} - V_D) / L] \times t_{OFF} = [(V_{OUT} - V_D) / L] \times t_{SW} \times (1 - D)$$

Therefore (simplified equation for Output Voltage):

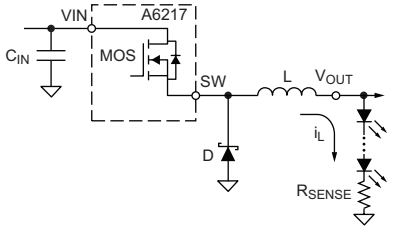
$$V_{OUT} = V_{IN} \times D - V_D \times (1 - D)$$

If V_D << V_{OUT}, then $V_{OUT} \approx V_{IN} \times D$.

More precisely:

$$V_{OUT} = (V_{IN} - i_{av} \times R_{DS(on)}) \times D - V_D \times (1 - D) - R_L \times i_{av}$$

Where R_L is the resistance fo the inductor.



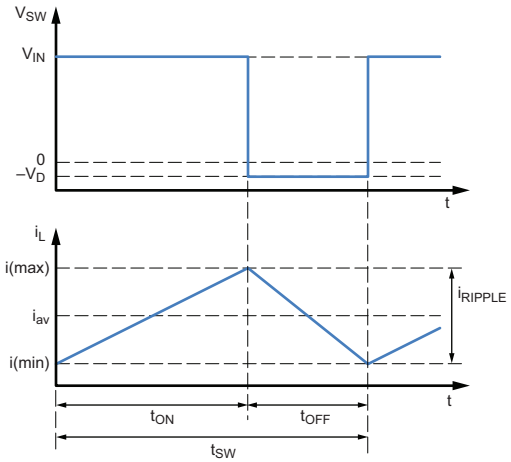


Figure 7: Simplified Buck Controller Equations

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ming frequency is between 100 Hz (Period = 10 ms) and 2 kHz. At a 200 Hz PWM frequency, the dimming duty cycle can be varied from 100% down to 1% or lower.

If EN is low for more than 20 ms, the IC enters shutdown mode to reduce power consumption. The next high signal on EN will initialize a full startup sequence, which includes a startup delay of approximately 70 µs. This startup delay is not present during PWM operation.

The EN pin is high-voltage tolerant and can be directly connected to a power supply. However, if EN is higher than the V_{IN} voltage at any time, a series resistor (1 kΩ) is required to limit the current flowing into the EN pin. This series resistor is not necessary if EN is driven from a logic input.

PWM Dimming Ratio

The brightness of the LED string can be reduced by adjusting the PWM duty cycle at the EN pin as follows:

Dimming ratio = PWM on-time / PWM period

For example, by selecting a PWM period of 5 ms (200 Hz PWM frequency) and a PWM on-time of 50 µs, a dimming ratio of 1% can be achieved.

In an actual application, the minimum dimming ratio is determined by various system parameters, including: V_{IN}, V_{OUT}, inductance, LED current, switching frequency, and PWM frequency. As a general guideline, the minimum PWM on-time should be kept at 50 µs or longer. A shorter PWM on-time is acceptable under more favorable operating conditions.

Output Voltage and Duty Cycle

Figure 7 provides simplified equations for approximating output voltage. Essentially, the output voltage of a buck converter is approximately given as:

$$V_{OUT} = V_{IN} \times D - V_{D1} \times (1 - D) \approx V_{IN} \times D, \text{ if } V_{D1} << V_{OUT}$$

$$D = t_{ON} / (t_{ON} + t_{OFF})$$

where D is the duty cycle, and V_{D1} is the forward drop of the Schottky diode D1 (typically under 0.5 V).

Minimum and Maximum Output Voltages

For a given input voltage, the maximum output voltage depends on the switching frequency and minimum t_{OFF}. For example, if t_{OFF}(min) = 150 ns and f_{SW} = 1 MHz, then the maximum duty cycle is 85%. So for a 24 V input, the maximum output is 20.3 V. This means up to 6 LEDs can be operated in series, assuming V_f = 3.3 V or less for each LED.

The minimum output voltage depends on minimum t_{ON} and switching frequency. For example, if the minimum t_{ON} = 100 ns and f_{SW} = 1 MHz, then the minimum duty cycle is 10%. That means with V_{IN} = 24 V, the minimum V_{OUT} = 2.4 V (one LED).

To a lesser degree, the output voltage is also affected by other factors such as LED current, on-resistance of the high-side switch, DCR of the inductor, and forward drop of the low-side diode. The more precise equation is shown in figure 7.

As a general rule, switching at lower frequencies allows a wider range of V_{OUT}, and hence more flexible LED configurations. This is shown in figure 8.

Figure 9 shows how the minimum and maximum output volt-

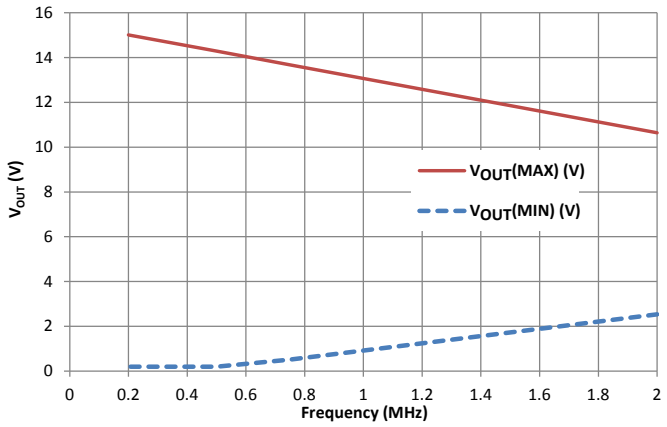


Figure 8: Minimum and Maximum Output Voltage versus Switching Frequency (V_{IN} = 16 V, i_{LED} = 1 A, minimum t_{ON} = 100 ns and t_{OFF} = 150 ns)

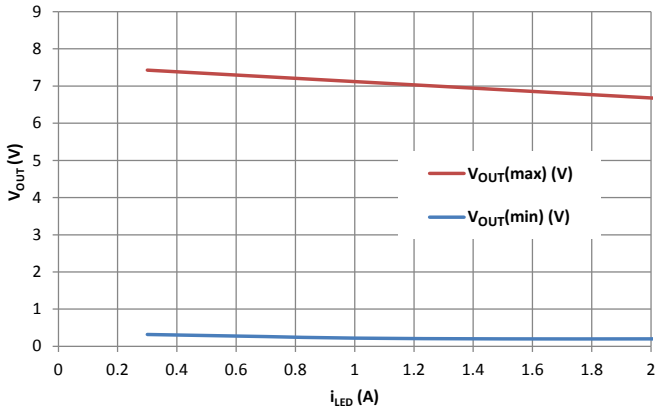


Figure 9: Minimum and Maximum Output Voltage versus i_{LED} current (V_{IN} = 9 V, f_{SW} = 1 MHz, minimum t_{ON} = 100 ns and t_{OFF} = 150 ns)

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ages vary with LED current (assuming $R_{DS(on)}$ = 0.4 Ω, inductor DCR = 0.1 Ω, and diode V_f = 0.6 V).

If the required output voltage is lower than that permitted by the minimum t_{ON}, the controller will automatically extend the t_{OFF}, in order to maintain the correct duty cycle. This means that the switching frequency will drop lower when necessary, while the LED current is kept in regulation at all times.

Fault Handling

The A6217 is designed to handle the following faults:

- Pin-to-ground short
- Pin-to-neighboring pin short
- Pin open
- External component open or short
- Output short to GND

The waveform in Figure 10 illustrates how the A6217 responds in the case in which the current sense resistor or the CS pin is shorted to GND. Note that the SW pin overcurrent protection is tripped at around 4.2 A, and the part shuts down immediately. The part then goes through startup retry after approximately 360 µs of cool-down period.

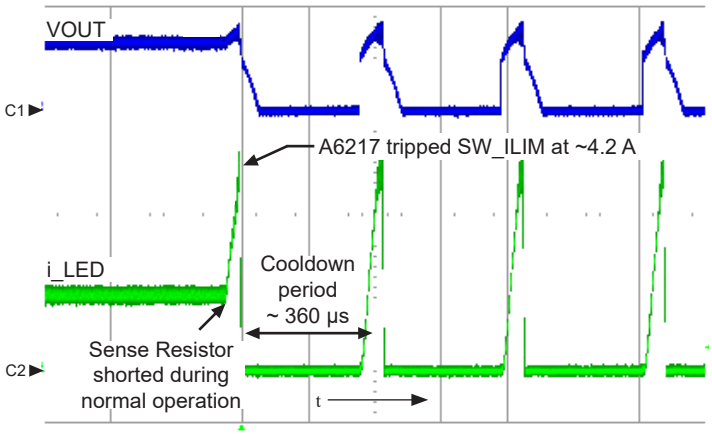


Figure 10: A6217 during fault condition where the sense resistor or CS pin is shorted to GND. Ch1 = VOUT (5 V/div), Ch2 = i_LED (500 mA/div), t = 200 µs/div.

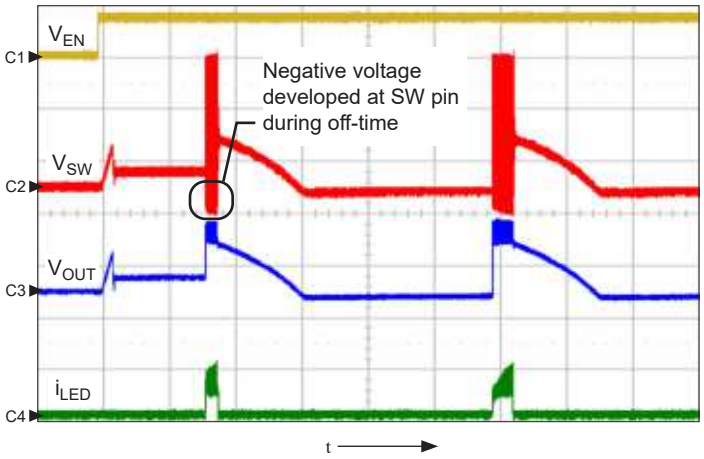


Figure 11: Startup waveform with a missing Schottky diode; shows Enable, V_{EN} (ch1, 5 V/div.), switch node, V_{SW} (ch2, 5 V/div.), output voltage, V_{OUT} (ch3, 5 V/div.), LED current, i_{LED} (ch4, 500 mA/div.), t = 100 µs/div.

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As another example, the waveform in Figure 11 shows the fault case where external Schottky diode D1 is missing or open. As LED current builds up, a larger-than-normal negative voltage is developed at the SW node during off-time. This voltage trips the missing Schottky detection function of the IC. The IC then shuts down immediately and waits for a cool-down period before retry.

Component Selections

The inductor is often the most critical component in a buck converter. Follow the procedure below to derive the correct parameters for the inductor:

1. Determine the saturation current of the inductor. This can be done by simply adding 20% to the average LED current:

$$i_{SAT} \geq i_{LED} \times 1.2.$$

2. Determine the ripple current amplitude (peak-to-peak value). As a general rule, ripple current should be kept between 10% and 30% of the average LED current:

$$0.1 < i_{RIPPLE(pk\text{-}pk)} / i_{LED} < 0.3.$$

3. Calculate the inductance based on the following equations:

$$L = (V_{IN} - V_{OUT}) \times D \times t / i_{RIPPLE}, \text{ and}$$

$$D = (V_{OUT} + V_{D1}) / (V_{IN} + V_{D1}),$$

where

D is the duty cycle,
t is the period $1/f_{SW}$, and

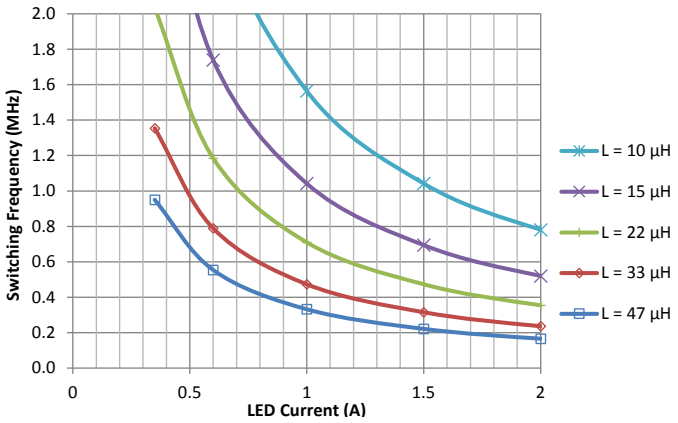
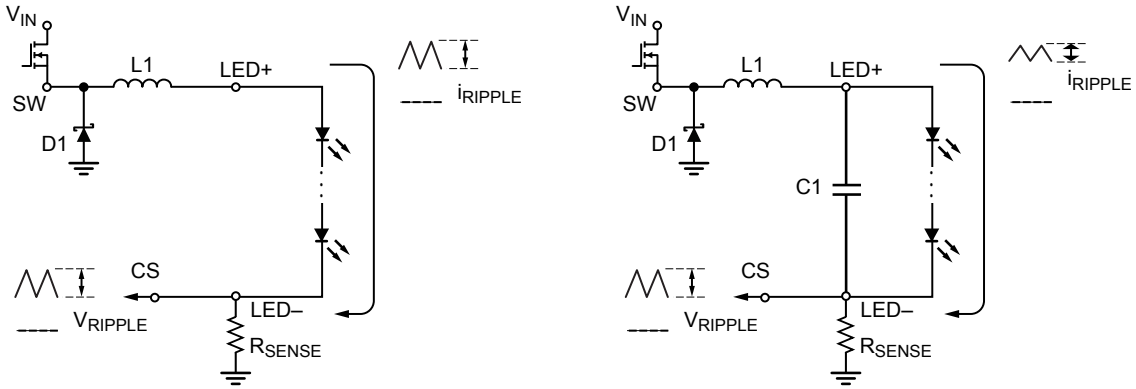


Figure 12: Inductance selection based on i_{LED} and f_{SW}; V_{IN} = 12 V, V_{OUT} = 6 V, ripple current = 20%

V_{D1} is the forward voltage drop of the Schottky diode D1 (see figure 7).

Inductor Selection Chart

The chart in Figure 12 summarizes the relationship between LED current, switching frequency, and inductor value. Based on



Without output capacitor:
Ripple current through LED string is proportional to ripple voltage at CS pin.

With a small capacitor across LED string:
Ripple current through LED string is reduced, while ripple voltage at CS pin remains high.

Figure 13. Ripple current and voltage, with and without shunt capacitor

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this chart: Assuming LED current = 1 A and f_{SW} =1 MHz, then the minimum inductance required is L = 22 µH in order to keep the ripple current at 30% or lower. (Note: $V_{OUT} = V_{IN} / 2$ is the worst case for ripple current). If the switching frequency is lower, then either a larger inductance must be used, or the ripple current requirement must be relaxed.

Additional Notes on Ripple Current

• For consistent switching frequency, it is recommended to choose the inductor and switching frequency to ensure the inductor ripple current percentage is at least 10% over normal operating voltage range (ripple current is lowest at lowest V_{IN}).

If ripple current is less than 10%, the switching frequency may jitter due to insufficient ripple voltage at CS pin. However, the average LED current is still regulated.

• There is no hard limit on the highest ripple current percentage allowed. A 60% ripple current is still acceptable, as long as both the inductor and LEDs can handle the peak current (average current × 1.3 in this case). However, care must be taken to ensure the valley of the inductor ripple current never drops to zero at the highest input voltage (which implies a 200% ripple current).

• In general, allowing a higher ripple current percentage enables lower-inductance inductors to be used, which results in smaller size and lower cost. The only downside is the core loss of the inductor increases with larger ripple currents, but this is typically a small factor.

• If lower ripple current is required for the LED string, one solution is to add a small capacitor (such as 2.2 µF) across the LED string from LED+ to LED–. In this case, the inductor ripple current remains high while the LED ripple current is greatly reduced.

Output Filter Capacitor

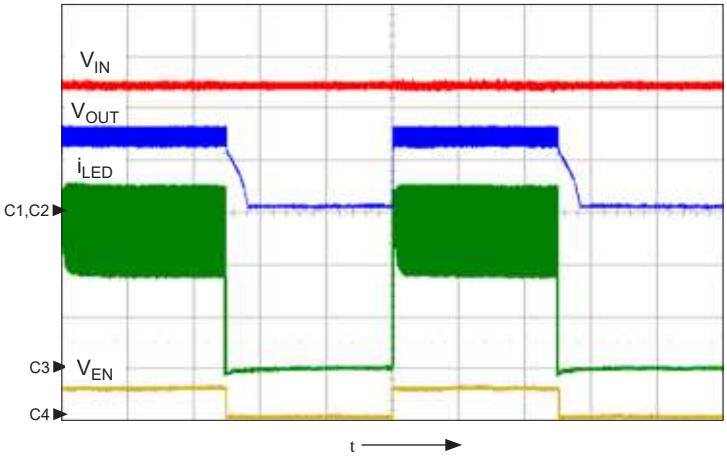
The A6217 is designed to operate without an output filter capacitor, in order to save cost. Adding a large output capacitor is not recommended.

In some applications, it may be required to add a small filter capacitor (up to several µF) across the LED string (between LED+ and LED–) to reduce output ripple voltage and current. It is important to note that:

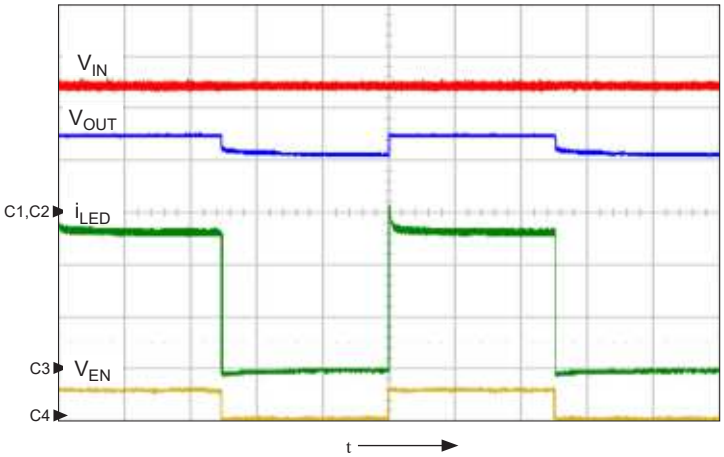
• The effectiveness of this filter capacitor depends on many factors, such as: switching frequency, inductors used, PCB layout, LED voltage and current, and so forth.

• The addition of this filter capacitor introduces a longer delay in LED current during PWM dimming operation. Therefore, the maximum PWM dimming ratio is reduced.

• The filter capacitor should NOT be connected between LED+ and GND. Doing so may create instability because the control loop must detect a certain amount of ripple current at the CS pin for regulation.



Panel 14A: Operation without using any output capacitor across the LED string



Panel 14B: Operation with a 0.68 µF ceramic capacitor connected across the LED string

Figure 14: Waveforms showing the effects of adding a small filter capacitor across the LED string

• Operating conditions: at 200 Hz, V_{IN} = 24 V, V_{OUT} = 15 V, f_{SW} = 500 kHz, L = 10 µH, duty cycle = 50%

• CH1 (Red) = V_{IN} (10 V/div), CH2 (Blue) = V_{OUT} (10 V/div), CH3 (Green) = i_{LED} (500 mA/div), CH4 (Yellow) = Enable (5 V/div), time scale = 1 ms/div

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Application Circuit

The application circuit in Figure 15 shows a design for driving a 15 V LED string at 1.3 A (set by R_{SENSE}). The switching frequency is 500 kHz, as set by R1. A 0.68 µF ceramic capacitor is added across the LED string to reduce the ripple current through the LEDs (as shown in Figure 14B).

Suggested Components

Symbol	Part Number	Manufacturer
C1	EMZA500ADA470MF80G	United Chemi-Con
C2	UMK316BJ475KL-T	Taiyo Yuden
C3	CGA5L2X5R1H684K160AA	TDK
L1	NR8040T100M	Taiyo Yuden
D1	B250A-13-F	Diodes, Inc.
R_{SENSE}	RL1632R-R150-F	Susumu

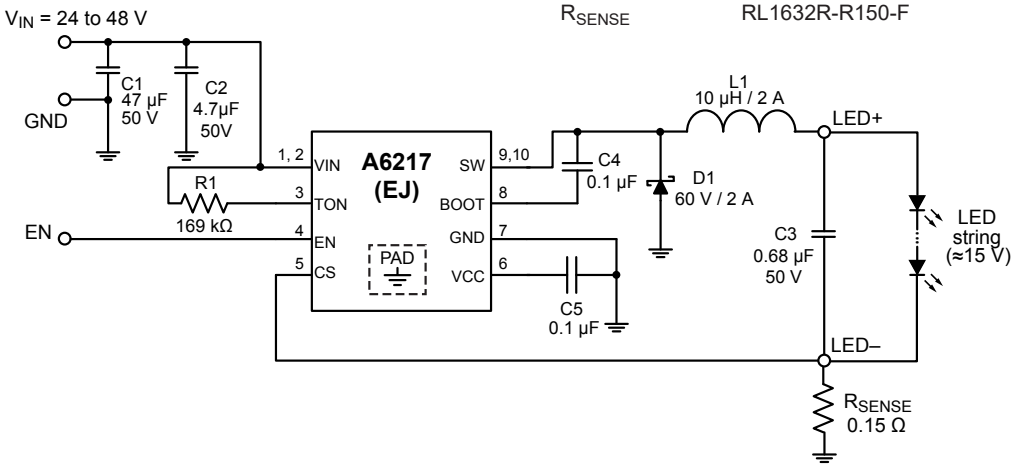


Figure 15: Application Circuit Diagram

Additional Application Circuits

The following are some application examples to expand the capability of the A6217:

- Figure 16 shows PWM dimming of LED current by pulsing the power supply line
- Figure 17 shows analog dimming of LED current by an external DC voltage
- Figure 18 shows thermal de-rating of LED current by an NTC resistor

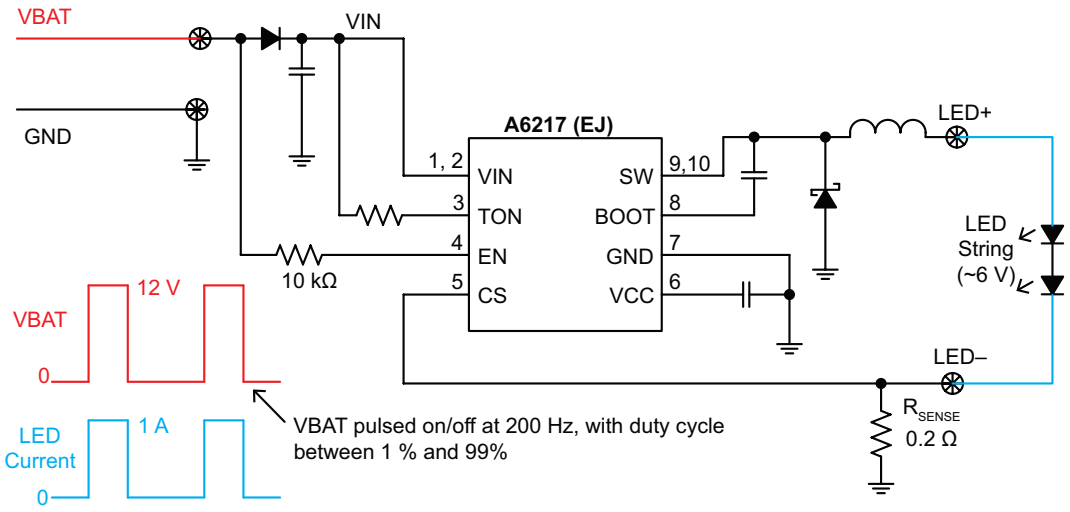


Figure 16: PWM Dimming of LED Current by Using Pulsed Power Supply Line

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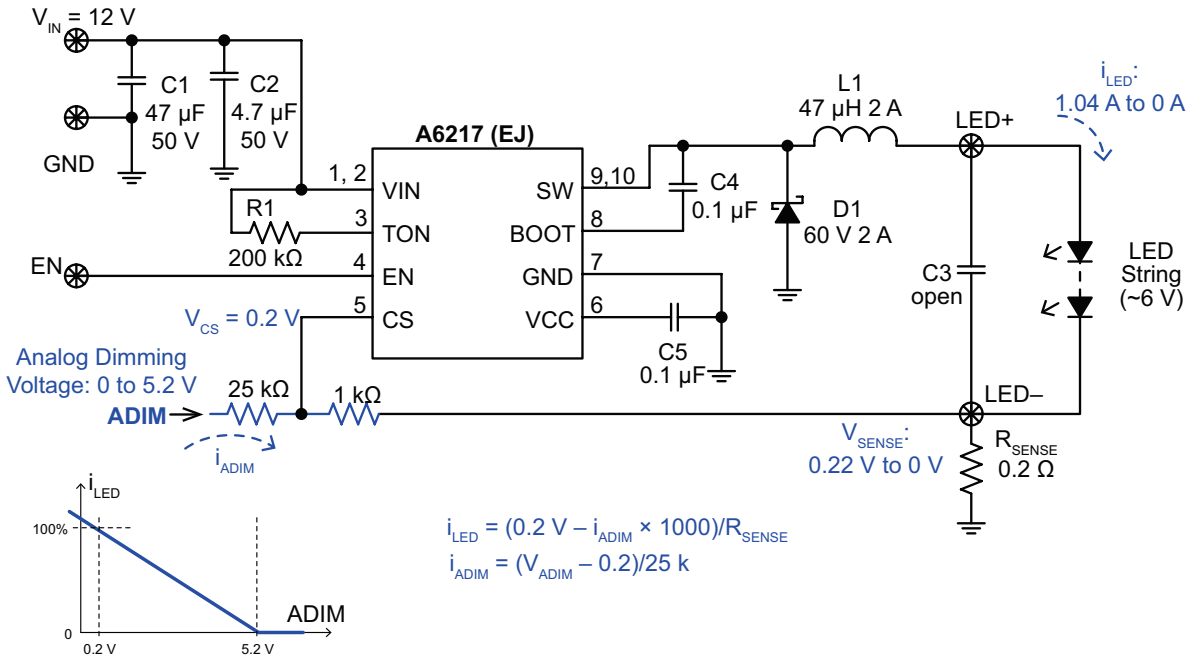


Figure 17: Analog Dimming of LED Current with an External DC Voltage

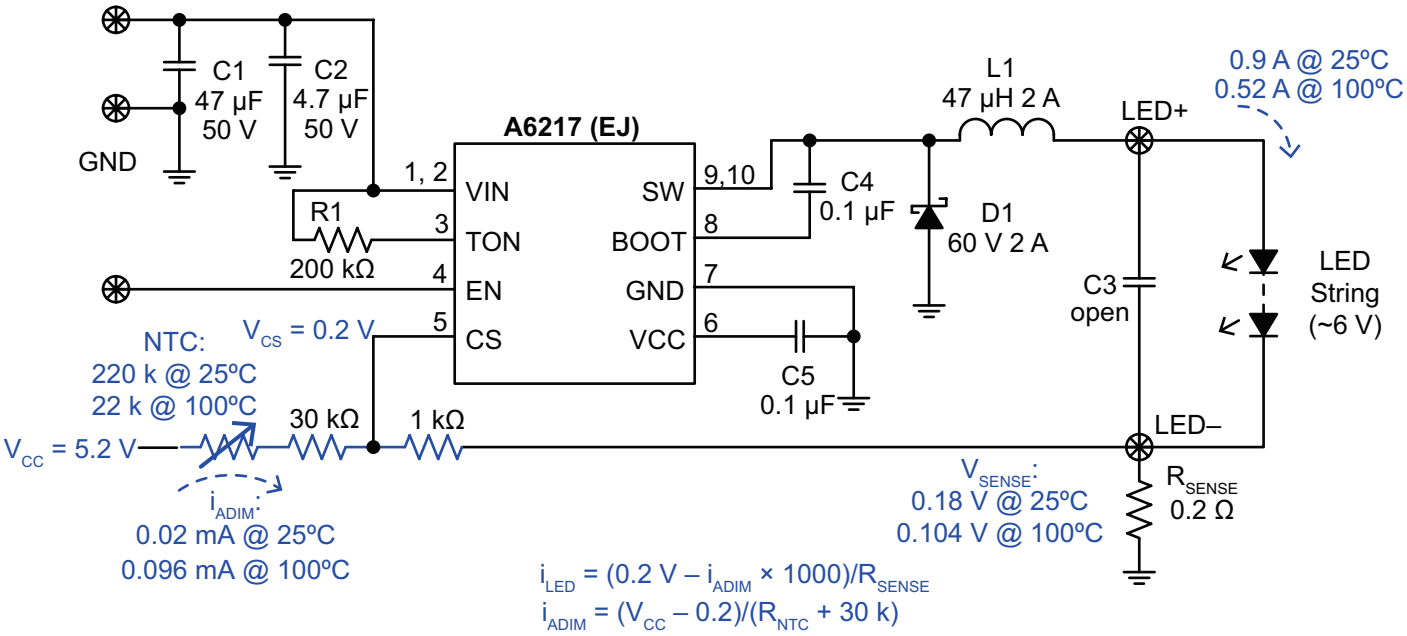


Figure 18: Thermal Foldback of LED Current Using NTC Resistor

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Component Placement and PCB Layout Guidelines

PCB layout is critical in designing any switching regulator. A good layout reduces emitted noise from the switching device and ensures better thermal performance and higher efficiency. The following guidelines help to obtain a high-quality PCB layout. Figure 19 shows an example for components placement. Figure 20 shows the three critical current loops that should be minimized and connected by relatively wide traces.

1) When the upper FET (integrated inside the A6217) is on, current flows from the input supply/capacitors, through the upper FET, into the load via the output inductor, and back to ground as shown in loop 1. This loop should have relatively wide traces. Ideally this connection is made on both the top (component) layer and via the ground plane.

2) When the upper FET is off, free-wheeling current flows from ground through the asynchronous diode D1, into the load via the output inductor, and back to ground as shown in loop 2. This loop should also be minimized and have relatively wide traces. Ideally this connection is made on both the top (component) layer and via the ground plane.

3) The highest di/dt occurs at the instant the upper FET turns on and the asynchronous diode D1 undergoes reverse recovery as shown in loop 3. The ceramic input capacitors C2 must deliver this high instantaneous current. C1 (electrolytic capacitor) should not be too far off C2. Therefore, the loop from the ceramic input capacitor through the upper FET and asynchronous diode to ground should be minimized. Ideally this connection is made on both the top (component) layer and via the ground plane.

4) The voltage on the SW node (pin 8) transitions from 0 V to V_{IN} very quickly and may cause noise issues. It is best to place the asynchronous diode and output inductor close to the A6217 to minimize the size of the SW polygon.

Keep sensitive analog signals (CS, and R1 of switching frequency setting) away from the SW polygon.

6) For accurate current sensing, the LED current sense resistor R_{SENSE} should be placed close to the IC.

7) Place the bootstrap capacitor C4 near the BOOT node (pin 7) and keep the routing to this capacitor short.

8) When routing the input and output capacitors (C1, C2, and C3 if used), use multiple vias to the ground plane and place the vias as close as possible to the A6217 pads.

9) To minimize PCB losses and improve system efficiency, the input (VIN) and output (VOUT) traces should be wide and duplicated on multiple layers, if possible.

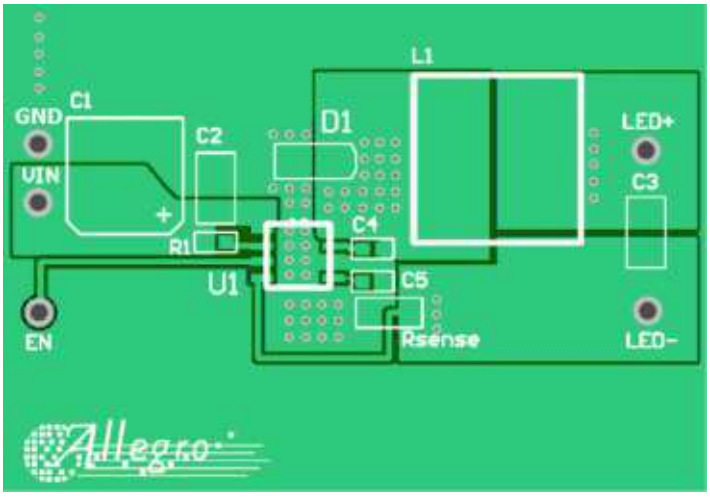


Figure 19: Example layout for the A6217 evaluation board (package LJ)

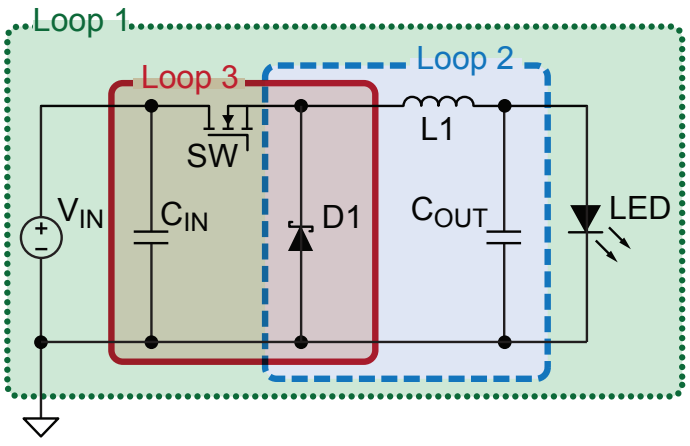


Figure 20: Three different current loops in a buck converter

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10) Connection to the LED array should be kept short. Excessively long wires can cause ringing or oscillation. When the LED array is separated from the converter board and an output capacitor is used, the capacitor should be placed on the converter board to reduce the effect of stray inductance from long wires.

Thermal Dissipation

The amount of heat that can pass from the silicon of the A6217 to the surrounding ambient environment depends on the thermal resistance of the structures connected to the A6217. The thermal resistance, $R_{\theta JA}$, is a measure of the temperature rise created by power dissipation and is usually measured in degrees Celsius per watt (°C/W).

The temperature rise, ΔT, is calculated from the power dissipated, P_D, and the thermal resistance, $R_{\theta JA}$, as:

$$\Delta T = P_D \times R_{\theta JA}$$

A thermal resistance from silicon to ambient, $R_{\theta JA}$, of approximately 35°C/W (LJ package) or 45°C/W (EJ package) can be achieved by mounting the A6217 on a standard FR4 double-sided printed circuit board (PCB) with a copper area of a few square inches on each side of the board under the A6217. Additional improvements in the range of 20% may be achieved by optimizing the PCB design.

Optimizing Thermal Layout

The features of the printed circuit board, including heat conduction and adjacent thermal sources such as other components, have a very significant effect on the thermal performance of the device. To optimize thermal performance, the following should be considered:

- The device exposed thermal pad should be connected to as much copper area as is available.
- Copper thickness should be as high as possible (for example, 2 oz. or greater for higher power applications).
- The greater the quantity of thermal vias, the better the dissipation. If the expense of vias is a concern, studies have shown that concentrating the vias directly under the device in a tight pattern, as shown in Figure 21, has the greatest effect.
- Additional exposed copper area on the opposite side of the board should be connected by means of the thermal vias. The copper should cover as much area as possible.
- Other thermal sources should be placed as remote from the device as possible
- Place as many vias as possible to the ground plane around the anode of the asynchronous diode.

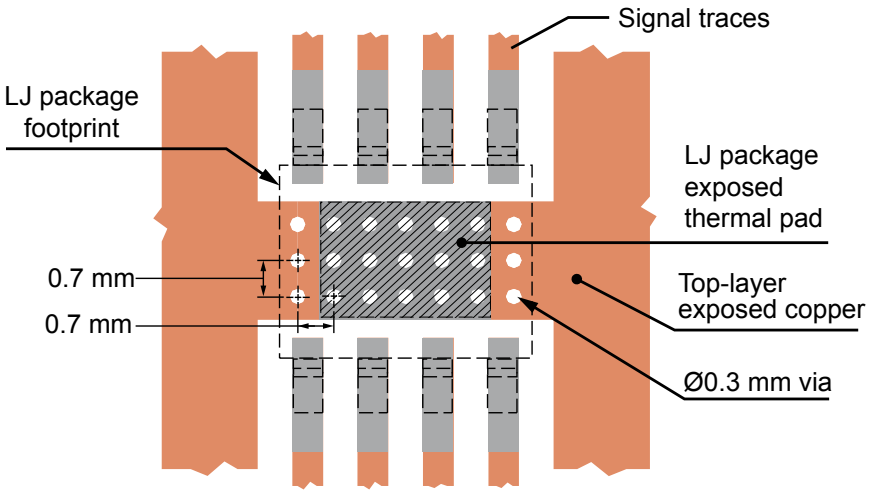


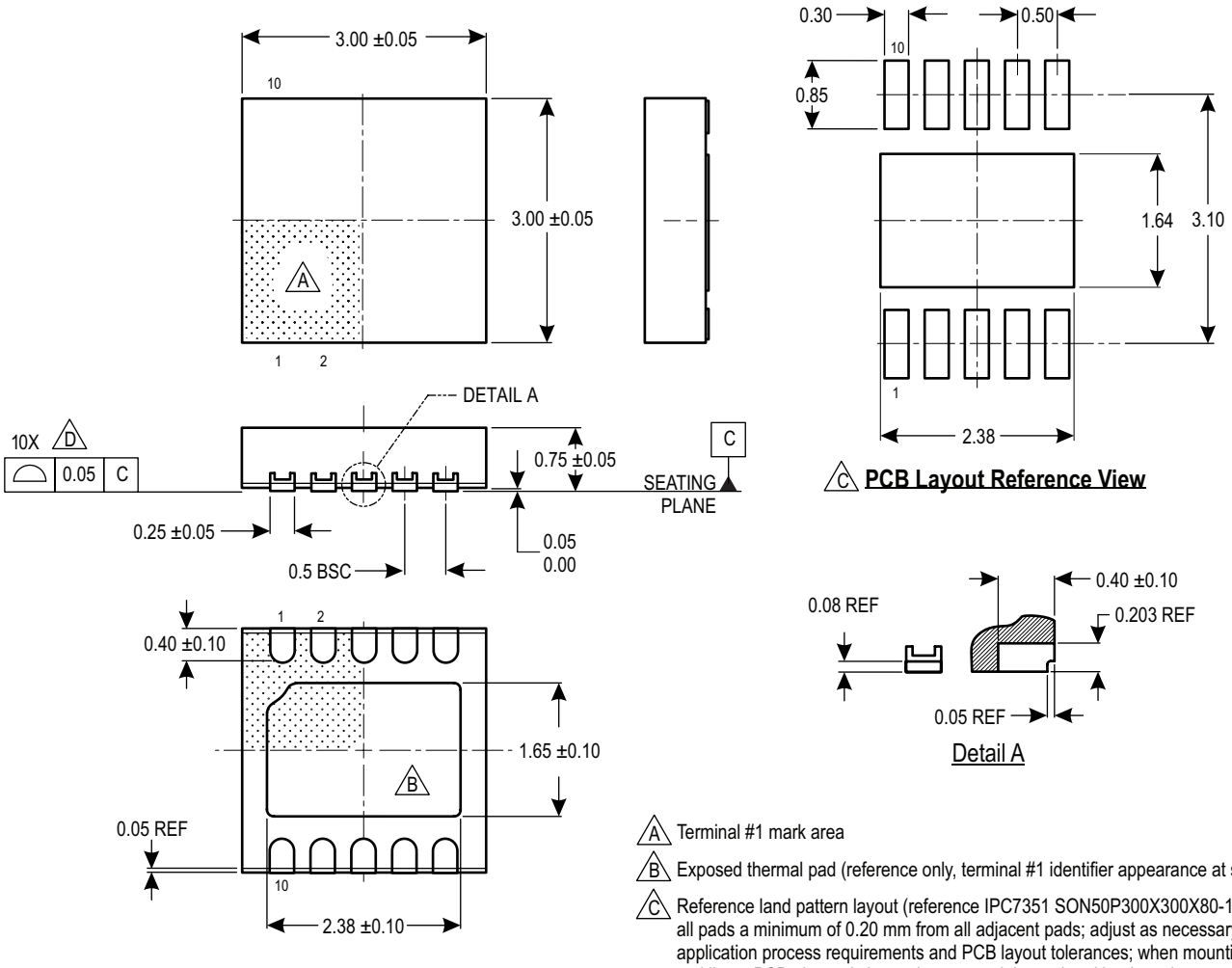
Figure 21: Suggested PCB layout for thermal optimization (maximum available bottom-layer copper recommended)

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PACKAGE OUTLINE DRAWINGS

For Reference Only – Not for Tooling Use

(Reference JEDEC MO-229)
Dimensions in millimeters – NOT TO SCALE
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 SON50P300X300X80-11WEED3M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

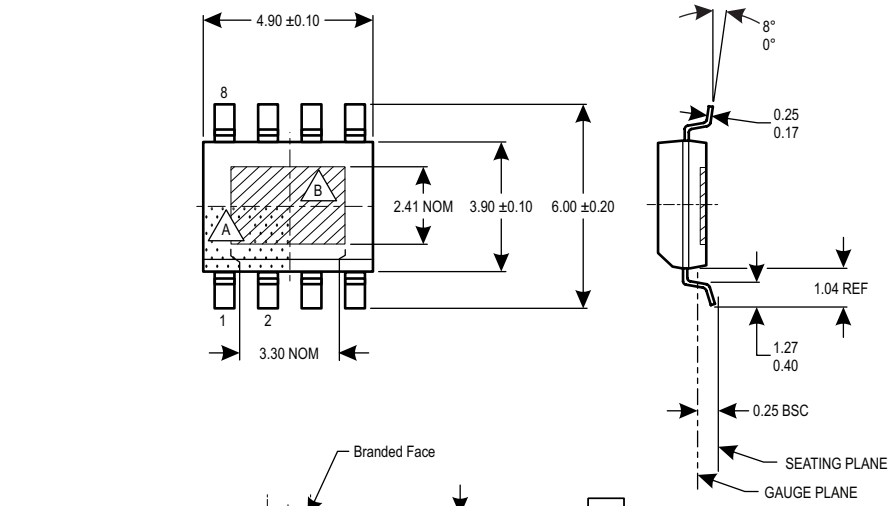
D Coplanarity includes exposed thermal pad and terminals

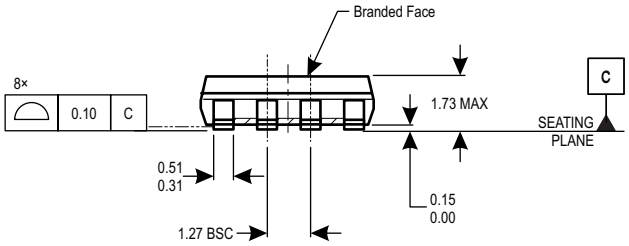
Package EJ, 10-Pin DFN
with Exposed Thermal Pad and Wettable Flank

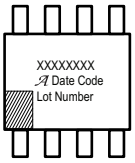
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Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

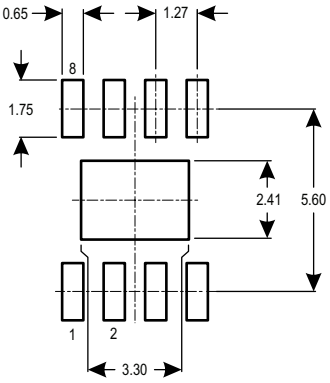






D **Standard Branding Reference View**

Line 1: Part Number
Line 2: Logo A, 4 digit Date Code
Line 3: Characters 5, 6, 7, 8 of
Assembly Lot Number



C PCB Layout Reference View

A Terminal #1 mark area

B Exposed thermal pad (bottom surface)

C Reference land pattern layout (reference IPC7351 SOIC127P600X175-9AM); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Branding scale and appearance at supplier discretion

Package LJ, 8-Pin SOICN
with Exposed Thermal Pad

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Revision History

Number	Date	Description
–	August 8, 2016	Initial release
1	June 1, 2020	Minor editorial updates
2	June 20, 2022	Updated LJ-8 package drawing (page 18) and minor editorial updates
3	December 12, 2023	Updated Functional Block Diagram (page 3)
4	March 11, 2024	Part variant A6217KEJTR-J status changed to Last-Time Buy (page 2).
5	September 12, 2024	Part variant A6217KEJTR-J status changed to Discontinued (page 2).

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