IDT™ 89EB-LOGAN-19 Evaluation Board Manual

(Evaluation Board: 18-692-001)

February 2011

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Printed in U.S.A.
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Description of the EB-LOGAN-19 Evaluation Board

Notes

Introduction

The 89HPES24NT24G2 switch is a member of the IDT PCI Express® Inter-Domain Switch family of products. It is a PCIe® Base Specification 2.1 compliant (Gen2) 24-lane, 24-port switch. The EB-LOGAN-19 Evaluation Board provides an evaluation platform for the PES24NT24G2 switch and for other members of this switch family including PES16NT16G2 and PES12NT12G2.

Detailed information related to configuration of number of ports and lanes in the switch device can be found in the Device User Manual and the Device Datasheet. The evaluation board, along with additional adapters and daughter boards provided by IDT, can be configured to test every possible combination of the number of lanes and ports offered by the switch. Advanced capabilities such as switch partitioning, NTB, DMA and local port clocking can be evaluated with the evaluation board.

The EB-LOGAN-19 brings out all 24 lanes of the device to two Mezzanine connectors and two SAS connectors (see Figure 1.1) located close to the device - one connector per stack of 4 lanes. Various types of daughter cards (provided by IDT) can then be plugged into the Mezzanine connectors to facilitate connectivity to one x8 or two x4 or four x2 or eight x1 link partners. Link partners may be plugged directly into these daughter cards or they can be connected to these daughter cards via SAS or SATA cables and a different board with PCIe slots known as the 12-PACK board (provided by IDT). Given that majority of the hosts / servers offer PCIe standard slots, IDT provides the necessary adapter cards that may be plugged into these host / server slots as well as the cables that connect such adapters to the daughter cards which in turn are plugged into the main evaluation board on which the IDT PCIe switch device is populated.

The EB-LOGAN-19 is also used by IDT to reproduce system-level hardware or software issues reported by customers. Figure 1.1 illustrates the functional block diagram representing the main parts of the EB-LOGAN-19 board.

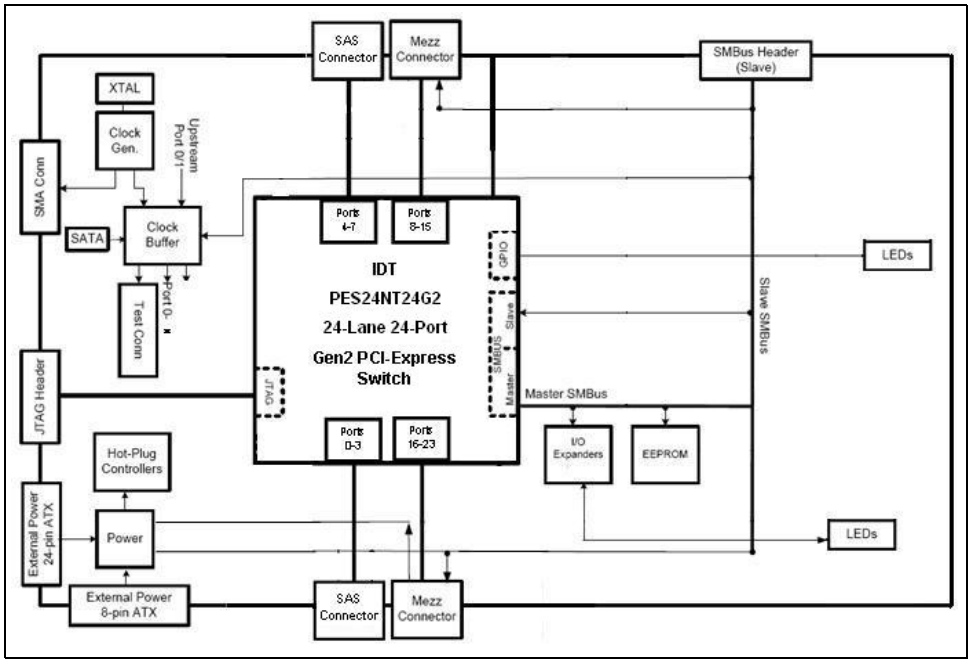


Figure 1.1 Function Block Diagram of the EB-LOGAN-19 Evaluation Board

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Notes

Board Features

Hardware

- PES24NT24G2 PCIe 24-port switch
  - *Twenty four ports (each x1) - for port 8 and higher, adjacent ports may be combined to create x2, x4 or x8 ports*
  - *PCIe Base Specification Revision 2.1 compliant (Gen2 SerDes speeds of 5 GT/S)*
  - *Up to 2048 byte maximum Payload Size*
  - *Automatic lane reversal and polarity inversion supported on all lanes*
  - *Automatic per port link width negotiation to x8, x4, x2, x1*
  - *Power on reconfiguration via optional serial EEPROM connected to the SMBUS Master interface*
- Upstream, Downstream Ports
  - *The EB-LOGAN-19 has minimum of one port configured as upstream port to be plugged into a host slot through an adaptor and a cable.*
  - *Up to 23 ports can be configured as downstream ports, for PCIe endpoint add-on cards to be plugged in. The slot connectors can be configured to be x1, x2, x4 or x8, but are mechanically open-ended on one side to allow card widths greater than x8 (e.g. x16) to be populated.*
  - *When used in multi-partition mode, the device can be programmed through the serial EEPROM to generate the appropriate number of upstream and downstream ports per partition.*
- Numerous user selectable configurations set using onboard jumpers and DIP-switches
  - *Source of clock - host clock or onboard clock generator*
  - *Two clock rates (100/125 MHz) from an onboard clock generator*
  - *Flexible clocking modes*
    - *Common clock*
    - *Non-common clock*
    - *Local port clocking on ports that support this feature*
  - *Boot mode selection*
- SMBUS Slave Interface (4 pin header)
- SMBUS Master Interface connected to the Serial EEPROMs through I/O expander
- Push button for Warm Reset
- Many LEDs to display status, reset, power, hotplug, etc.
- JTAG connector to the PES24NT24G2 JTAG pins.

Software

There is no software or firmware executed on the board. However, useful software is provided along with the Evaluation Board to facilitate configuration and evaluation of the PES24NT24G2 within host systems running popular operating systems.

- Installation programs
  - *Operating Systems Supported: WindowsServer200x, WindowsXP, Vista, Linux*
- GUI based application for Windows and Linux
  - *Allows users to view and modify registers in the PES24NT24G2*
  - *Binary file generator for programming the serial EEPROMs attached to the SMBUS.*

Other

- SMBUS cable may be required for certain evaluation exercises.
- SMA connectors are provided on the EB-LOGAN-19 board for clock outputs.

Revision History

April 13, 2010: Initial publication of evaluation board manual.

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Notes

April 23, 2010: Updated Schematics in Chapter 4.

August 18, 2010: Updated the manual for Rev. 2.0 board

February 16, 2011: Changed default settings from Off to On in Tables 2.3 and 2.4.

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Installation of the EB-LOGAN-19 Evaluation Board

Notes

EB-LOGAN-19 Installation

This chapter discusses the steps required to configure and install the EB-LOGAN-19 evaluation board. All available DIP switches and jumper configurations are explained in detail.

The primary installation steps are:

1. Configure jumper/switch options suitable for the evaluation or application requirements.
2. Connect PCI Express endpoint cards to the downstream port PCIe slots on the evaluation board.
3. Make sure that the host system (motherboard with root complex chipset) is powered off.
4. Connect the evaluation board to the host system.
5. Apply power to the host system.

The EB-LOGAN-19 board is typically shipped with all jumpers and switches configured to their default settings. In most cases, the board does not require further modification or setup however please visit IDT website and fill out the Technical Support Request form at http://www.idt.com/?app=TechSupport for other configurations.

PCI Express Mezzanine and Edge Adapters

The PCI Express lanes are broken out to four Mezzanine connectors on EB-LOGAN-19 Evaluation Board. The adapter cards are used to convert Mezzanine connector into PCI Express slot connector(s) or Internal mini SAS (iSAS) connectors or both. A Bifurcated Mezzanine Card has two mechanical x8 PCIe Slots (x4 electrically) while a Merged Mezzanine Card has single x8 PCIe Slot. Pictured in Figure 2.1.

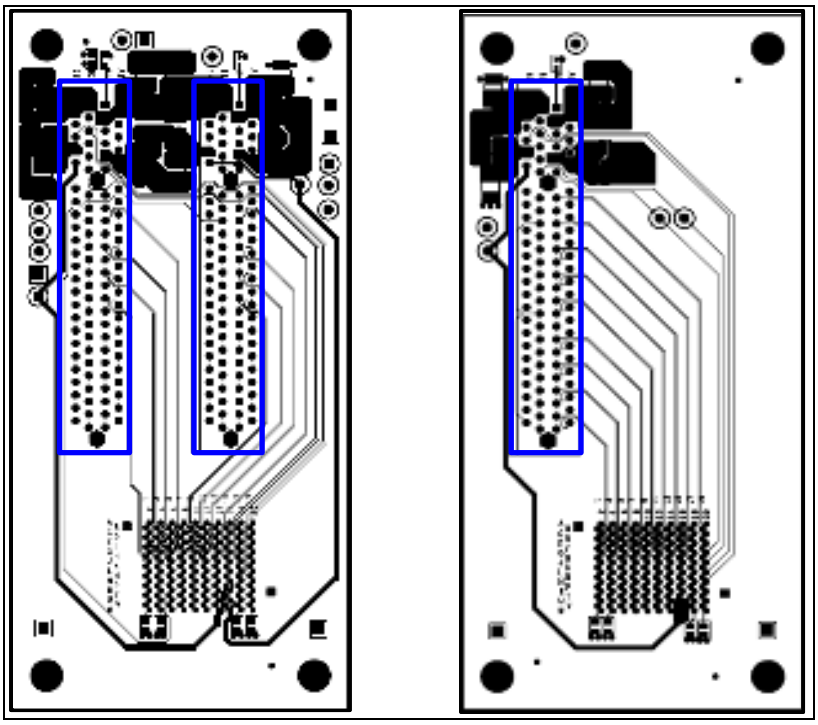


Figure 2.1 Bifurcated and Merged Mezzanine Cards

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Pictured in Figure 2.2 is the mini-SAS Mezzanine card which consists of two iSAS and two SATA connectors. Each iSAS connector supports up to PCI Express x4 width and the SATA connectors are used for clock and reset signals of each x4 or less stack/port. An iSAS-to-SATA breakout cable shown in Figure 2.3 is used connect from iSAS to edge adapter and/or 12PACK.

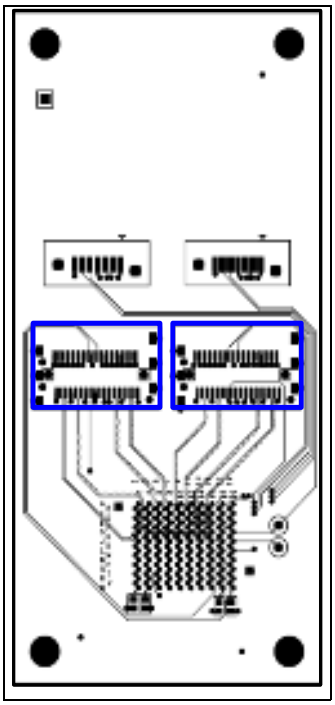


Figure 2.2 MiniSAS Mezzanine Adapter

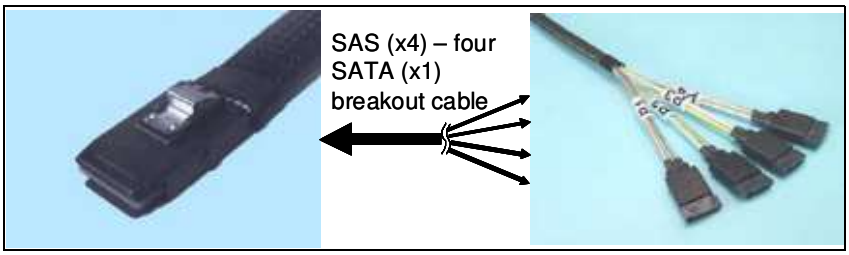


Figure 2.3 EB-LOGAN-19 iSAS-to-SATA Breakout Cable

The PCI Express Edge to SATA Adapter, pictured in Figure 2.4, can be inserted into any physical PCIe slot on a host system and in combination with mini-SAS Mezzanine Card, such as the one in Figure 2.2, to form a link between evaluation main board and the host system. There are 5 SATA connectors which one connector (J7) is for clock and reset, and the rest supports one PICe lane per SATA connector. The edge adapters can be inserted into a mechanical x1 or greater slot.

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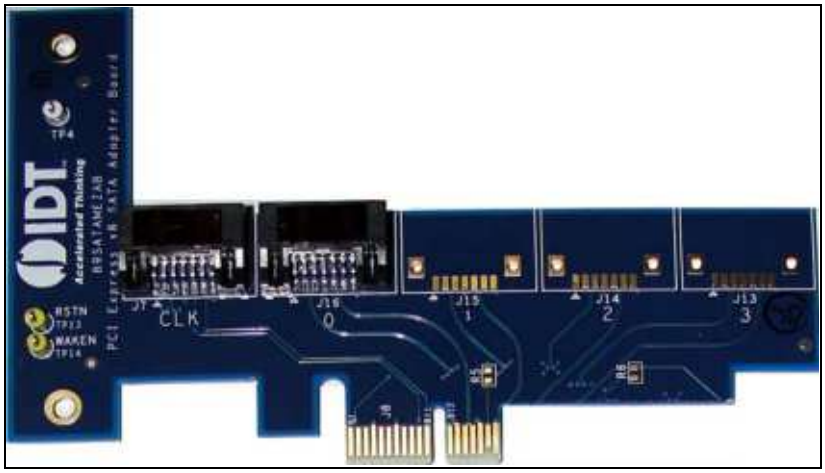


Figure 2.4 PCIe x1 Edge-to-SATA Adapter

Hardware Description

The PES24NT24G2 is a 24-lane, 24-port PCI Express® switch. It is a peripheral chip that performs PCI Express based switching with a feature set optimized for high performance applications such as servers and storage. It provides fan-out and switching functions between a PCI Express upstream port and downstream ports or peer-to-peer switching between downstream ports. Furthermore, up to eight ports can be configured as NTB ports for multi-root application.

The EB-LOGAN-19 Main Board, shown in Figure 2.5, will support up to 4 PCI Express downstream ports and up to 23 ports when using two 12PACK Daughter Boards.

Basic requirements for the board to run are:

- *Host system with a PCI Express root complex supporting x1 configuration through a PCI Express x1 slot.*
- *– x1, x2, x4, or x8 PCI Express Endpoint Cards.*

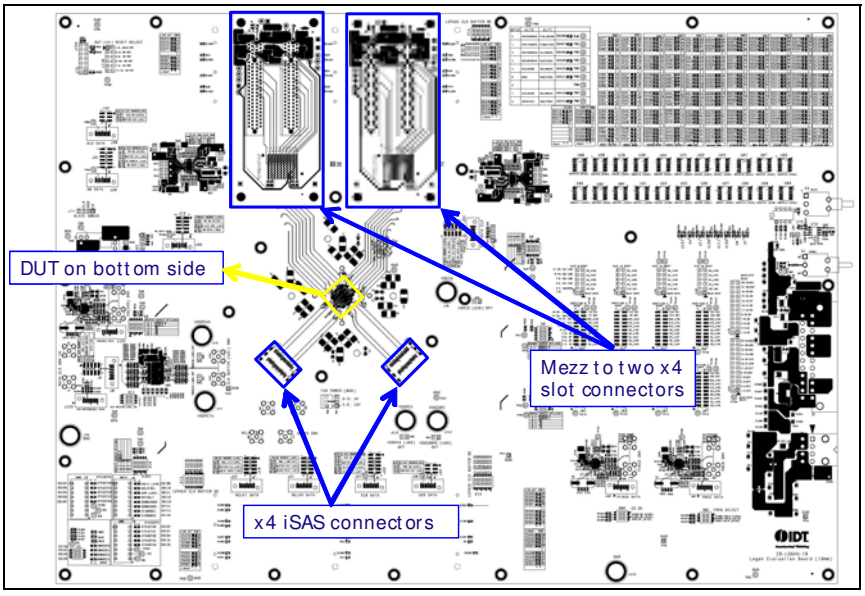


Figure 2.5 EB-LOGAN-19 Evaluation Main Board

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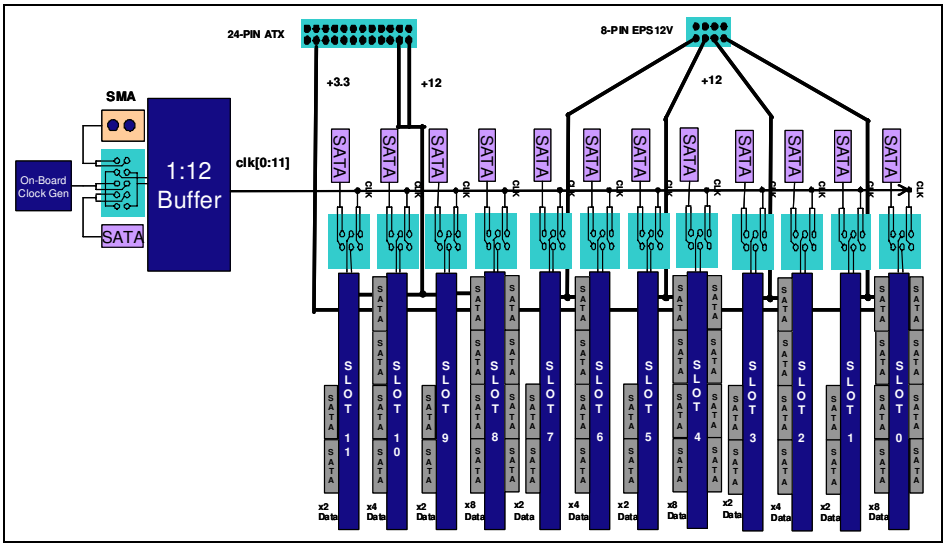


Figure 2.6 12PACK PCIe Slots Breakout Daughter Board

Reference Clocks

Global Reference Input Clocks

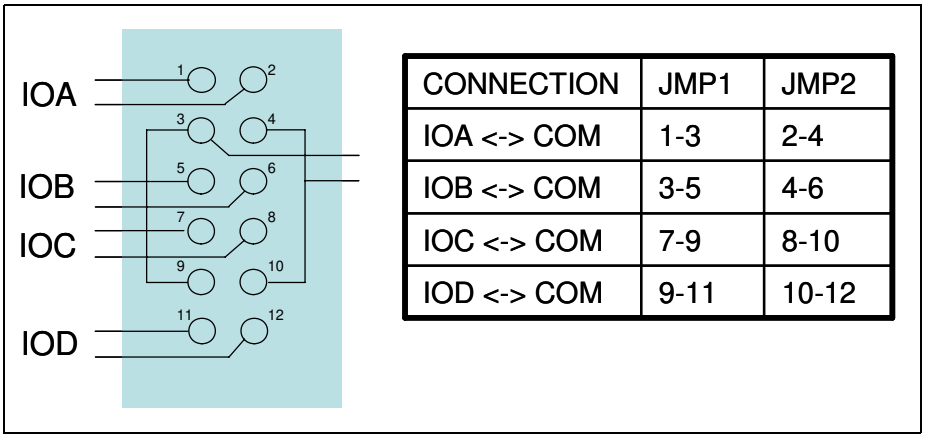
The PES24NT24G2 requires two differential reference clocks. The EB-LOGAN-19 derives these clocks from SMA connectors (J17, J20, J66, J67), clock buffer (U50), or SATA connectors (J21, J22) as described in Table 2.1 and Figures 2.7 and 2.8. Both reference clocks are mandatory and must come from the same reference clock source. The switch will not function normally if only one clock is used.

Global Clock#	Jumper	Selection
0	J18	[1-3 / 2-4] SMA (J66/J67) [5-7 /6-8] From Clock Buffer U51 [7-9 / 8-10] SATA, J21
1	J19	[1-3 / 2-4] SMA (J17/J20) [5-7 /6-8] From Clock Buffer U51 [7-9 / 8-10] SATA, J22

Table 2.1 EB-LOGAN-19 Global Clock Select

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Notes



CONNECTION	JMP1	JMP2
IOA <-> COM	1-3	2-4
IOB <-> COM	3-5	4-6
IOC <-> COM	7-9	8-10
IOD <-> COM	9-11	10-12

Figure 2.7 Differential Jumper Arrangement

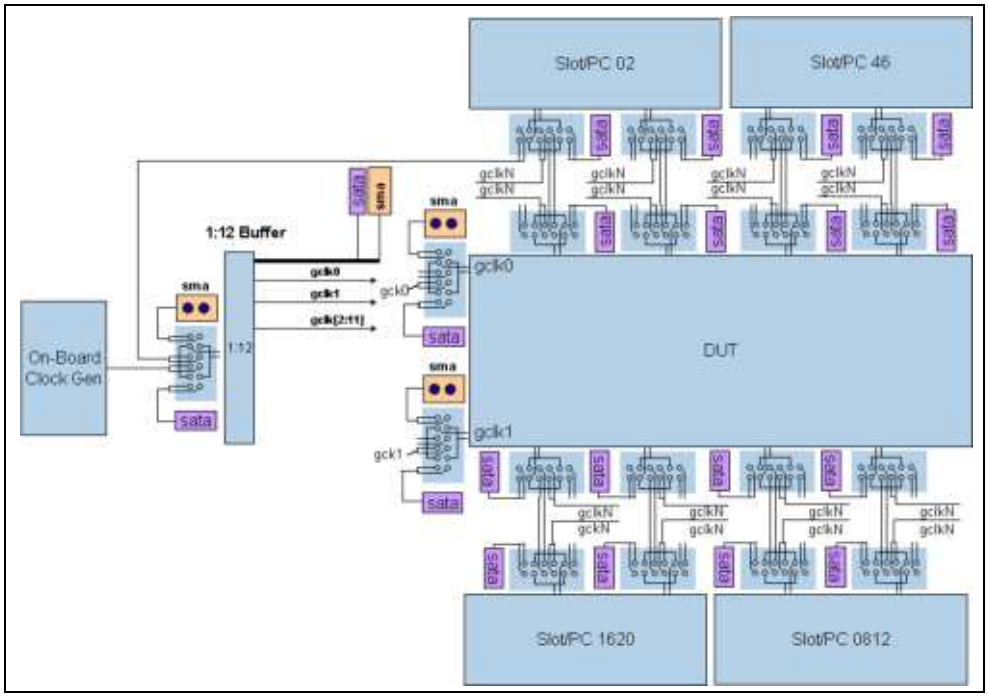


Figure 2.8 Reference Clock Configuration

By default the clock buffer derives its clock from a common source. The common source can be the host system's reference clock, the onboard clock generator, or SATA connector (J8). See Table 2.2.

.

Jumper	Selection
J6	[1-3 / 2-4] SMA (J5/J7) [5-7 / 6-8] Onboard Clock Generator (U49) [7-9 / 8-10] SATA (J8)

Table 2.2 Clock Buffer Input Sources

The frequency of the global reference clock input may be selected by the Clock Frequency Select (GCLKFEL) pin to be either 100 MHz or 125 MHz as described in Table 2.3.

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Notes

Global Clock Frequency Switch - SW10[2	
SW10[2]	Clock Frequency
ON	100 MHz (Default)
OFF	125 MHz

Table 2.3 Global Reference Input Clock Frequency Select

The source for the onboard clock is the ICS841484 clock generator device (U49) connected to a 25MHz oscillator (X1). When using the onboard clock generator, the output frequency is fixed at 100MHz. Therefore, ICS_FS (S10, bit 1) is ON as the default setting. See Table 2.4.

Onboard Clock Frequency Switch - S10[1]	
S10[1]	Clock Frequency
ON	100 MHz (Default)
OFF	125 MHz

Table 2.4 Onboard Clock Generator Frequency Select

The output of the onboard clock generator is accessible through two yellow colored loop connectors located on the Evaluation Board. See Table 2.5. This can be used to connect a scope for probing or capturing purposes and cannot be used to drive the clock from an external source.

Onboard Reference Clock Output (Differential)	
J119	Positive Reference Clock (SMA)
J120	Negative Reference Clock (SMA)
J121	Differential Reference Clock (SATA)

Table 2.5 Onboard Reference Clock Generator Access Points

Local Port Input Clocks

Associated with some ports is a port reference clock input (PxCLK). Depending on the port clocking mode, a differential reference clock is driven into the device on the corresponding PxCLKP and PxCLKN pins. The frequency of a port reference clock input MUST always be 100 MHz. Table 2.6 and Table 2.7 list the possible sources for ports 8 and 16 reference clock input, and Table 2.8 lists the possible sources for the slot clock input. Additional information on port clocking usage and configuration can be found in the Device User Manuals and in IDT's Application Note AN-715. Local port clock sources for ports 8 and 16 are selected by DIP Switch (S17 and S19) via clock mux/buffer.

Port 8 Clock Source Select - S19[1]	
S19[1]	Clock Source
OFF	SATA J62
ON	Port 8 Clock Generator (U118)

Table 2.6 EB-LOGAN-23 Port 8 Clock Source Select

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Notes

Port 16 Clock Source Select - S17[1]	
S17[1]	Clock Source
OFF	SATA J64
ON	Port 16 Clock Generator (U120)

Table 2.7 EB-LOGAN-23 Port 16 Clock Source Select

Slot #	Header	Selection
8	J31	[1-3 / 2-4] Onboard Clock Generator (U118) [3-5 / 4-6] From Clock Buffer [7-9 / 8-10] P16CLK Clock Mux (U16) [9-11 / 10-12] SATA (J35)
12	J32	[1-3 / 2-4] P08CLK Clock Mux (U18) [3-5 / 4-6] From Clock Buffer [7-9 / 8-10] P16CLK Clock Mux (U16) [9-11 / 10-12] SATA (J36)
16	J33	[1-3 / 2-4] P16CLK Clock Mux (U16) [3-5 / 4-6] From Clock Buffer [7-9 / 8-10] Onboard Clock Generator (U120) [9-11 / 10-12] SATA (J37)
20	J34	[1-3 / 2-4] P08CLK Clock Mux (U18) [3-5 / 4-6] From Clock Buffer [7-9 / 8-10] P16CLK Clock Mux (U16) [9-11 / 10-12] SATA (J38)

Table 2.8 EB-LOGAN-19 Slot Clock Select

CLKMODE Selection

All ports in the PES24NT24G2 device (upstream and downstream) use global clocked mode. The port clocking mode of a port is determined by the state of the CLKMODE[1:0] pins in the boot configuration vector as shown in Table 2.9. This field determines the initial value of the Slot Clock Configuration (SCLK) field in each port's PCI Express Link Status (PCIELSTS) register. The SCLK field controls the advertisement of whether or not the port uses the same reference clock source as the link partner. A one in the SCLK field indicates that the port and its link partner use the same reference clock source. This is defined as Common Clock Configuration by the PCI Express Base Specification. A zero in the SCLK field indicates that the port and its link partner do not use the same reference clock source.

SW10[8] CLKMODE[0]	SW10[7] CLKMODE[1]	Port 0 SCLK	Port[23:1] SCLK
ON	ON	0	0
OFF	ON	1	0
ON	OFF	0	1
OFF	OFF	1	1

Table 2.9 CLKMODE Selection PES24NT24G2

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Notes

Power Sources

Power for the PES24NT24G2 and all downstream ports will be generated from the 12V from an external power connector. See Table 2.10. A 12V to 3.3V DC-DC converter will be used to provide power to five switching regulators to generate V_{DD}CORE, V_{DD}PEA, V_{DD}PETA, V_{DD}PEHA, and V_{DD}IO voltages. The 3.3V from the DC-DC converter will be used to power the clock buffers and circuitries.

The external power supply connector is a 24-pin (J69) molex connector as described in Tables 2.10.

Pin	Signal	Pin	Signal
1	+3.3V	13	+3.3V
2	+3.3V	14	-12V
3	GND	15	GND
4	+5V	16	PS_ON
5	GND	17	GND
6	+5V	18	GND
7	GND	19	GND
8	PWR_OK	20	NC
9	5VSB	21	+5V
10	+12V3	22	+5V
11	+12V3	23	+5V
12	+3.3V	24	GND

Table 2.10 EPS12V 24-pin Power Connector - J69

The power on switch located at S1 can be used to control the supply power from the external power supply connector. Add a shunt to W27 to enable power on switch.

PCI Express Analog Power Voltage Regulator

A voltage regulator (U65) provides a 2.5V PCI Express analog power voltage (shown as VDDPEHA) to the PES24NT24G2.

PCI Express Digital Power Voltage Converter

A separate voltage regulator (U62) provides a 1.0V PCI Express analog power voltage (shown as VDDPEA) to the PES24NT24G2.

PCI Express Transmitter Analog Voltage Converter

A separate voltage regulator (U68) provides a 1.0V PCI Express transmitter analog voltage (shown as VDDPETA) to the PES24NT24G2.

Core Logic Voltage Converter

A separate voltage regulator (U59) provides the 1.0V core voltage (VDDCORE) to the PES24NT24G2.

3.3V I/O Voltage Regulator

A separate voltage regulator (U56) provides the 3.3V I/O voltage (VDDIO) to the PES24NT24G2.

Power-up Sequence for PES24NT24G2

During power supply ramp-up, VDDCORE must remain at least 1.0V below VDDIO at all times. There are no other power-up sequence requirements for the various operating supply voltages.

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Notes

Heatsink Requirement

The EB-LOGAN-19 evaluation board utilizes a heatsink with integrated fan.

Reset

The PES24NT24G2 supports two types of reset mechanisms as described in the PCI Express specification:

– *Fundamental Reset: This is a system-generated reset that propagates along the PCI Express tree through a single side-band signal PERST# which is connected to the Root Complex, the PES24NT24G2, and the endpoints.*

– *Hot Reset: This is an In-band Reset, communicated downstream via a link from one device to another. Hot Reset may be initiated by software. This is further discussed in the PES24NT24G2 User Manual. The EB-LOGAN-19 evaluation board provides seamless support for Hot Reset.*

Fundamental Reset

There are two types of Fundamental Resets which may occur on the EB-LOGAN-19 evaluation board:

– *Cold Reset: During initial power-on, the onboard voltage monitor (TLC7733D) will assert the PCI Express Reset (PERSTN) input pin of the PES24NT24G2.*

– *Warm Reset: This is triggered by hardware while the device is powered on. Warm Reset can be initiated by two methods:*

- *Pressing a push-button switch (S3) located on EB-LOGAN-19 board*
- *The host system board IO Controller Hub asserting PERST# signal, which propagates through the PCIe upstream edge connector of the EB-LOGAN-19.*

Both events cause the onboard voltage monitor (TLC7733D) to assert the PCI Express Reset (PERSTN) input of the PES24NT24G2 while power is on.

Downstream Reset

Single Partition Mode without Hot Plug:

When the evaluation board initially powers on is assumes the following:

- The switch is configured in single partition mode.
- Port 0 is the root port and controls the downstream port resets.
- Ports 1-23 are downstream ports.
- Hot Plug is disabled.

The following behavior should be observed:

- The resets to slots 1-23 should initially be asserted and remain this way until after the fundamental reset is initially de-asserted.
- The assertion of a fundamental reset should propagate to slots 1-23.

Stack Configuration

The PES24NT24G2 contains four stack blocks labeled Stack 0, Stack 1, Stack 2, and Stack 3. Stacks 0 and 1 have four x1 ports each, and stacks 2 and 3 have eight x1 ports each. This provides a total of 24 ports in the device labeled port 0 through port 23. Table 2.11 lists the ports associated with each stack.

Stacks 0 and 1 have non-mergeable x1 ports. Stacks 2 and 3 may be configured as eight x1 ports, four x2 ports, two x4 ports, one x8 port, and any combinations in between. The configuration of each stack is controlled by the Stack Configuration (STK[3:2]CFG) registers. For possible configurations please refer to the device user manual.

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Notes

Stack	Ports Associated with the Stack
Stack 0	0, 1, 2, 3
Stack 1	4, 5, 6, 7
Stack 2	8, 9, 10, 11, 12, 13, 14, 15
Stack 3	16, 17, 18, 19, 20, 21, 22, 23

Table 2.11 Ports in Each Stack

Boot Configuration Vector

A boot configuration vector consisting of the signals listed in Table 2.12 is sampled by the PES24NT24G2 during a fundamental reset (while PERSTN is active). The boot configuration vector defines the essential parameters for switch operation and is set using DIP switches S5, SW8, SW9 and SW10 as defined in Table 2.13.

Signal	Description
GCLKFSEL	Global Clock Frequency Select. This pin specifies the frequency of the GCLKP and GCLKN signals.. Default: low
CLKMODE[1:0]	Clock Mode. These pins specify the clocking mode used by switch ports. See Table 2.9 for a definition of the encoding of these signals. The value of these signals may be overridden by modifying the Port Clocking Mode (PCLKMODE) register.
RSTHALT	Reset Halt. When this pin is asserted during a switch fundamental reset sequence, the switch remains in a quasi-reset state with the Master and Slave SMBuses active. This allows software to read and write registers internal to the device before normal device operation begins. The device exits the quasi-reset state when the RSTHALT bit is cleared in the SWCTL register by an SMBus master. Refer to section Switch Fundamental Reset on page 3-2 for further details. Default: low
SSMBADDR[2:1]	Slave SMBus Address. SMBus address of the switch on the slave SMBus. Default: 0x3
SWMODE[3:0]	Switch Mode. These pins specify the switch operating mode.
STK2CFG[4:0]	Stack 2 Configuration. These pins select the configuration of stack 2 during a switch fundamental reset.
STK3CFG[4:0]	Stack 3 Configuration. These pins select the configuration of stack 3 during a switch fundamental reset.

Table 2.12 Boot Configuration Vector Signals

Location	Signal	Default
SW10[2]	GCLKFSEL	ON
SW10[4]	RSTHALT	ON
SW10[5]	SSMBADDR[2]	OFF
SW10[6]	SSMBADDR[1]	OFF

Table 2.13 Boot Configuration Vector Switch SW10

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Notes

SMBus Interfaces

The System Management Bus (SMBus) is a two-wire interface through which various system component chips can communicate. It is based on the principles of operation of I^2C. Implementation of the SMBus signals in the PCI Express connector is optional and may not be present on the host system. The SMBus interface consists of an SMBus clock pin and an SMBus data pin.

The PES24NT24G2 contains two SMBus interfaces: a slave SMBus interface and a master SMBus interface. The slave SMBus interface allows a SMBus Master device full access to all software-visible registers. The Master SMBus interface provides a connection to the external serial EEPROM used for initialization and the I/O expanders used for hot-plug signals.

SMBus Slave Interface

On the PES24NT24G2 board, the slave SMBus interface is accessible through a 4-pin header as described in Table 2.14.

.

Slave SMBus Interface Connector J71	
Pin	Signal
1	SDA
2	GND
3	SCL
4	NC

Table 2.14 Slave SMBus Interface Connector

For a fixed address, the SMBus address of the PES24NT24G2 slave interface is 0b1110111 by default and is configurable using DIP Switches SW10[5] and SW10[6] as described in Table 2.15.

Slave Interface Address Configuration	
Address Bit	Signal
1	SSMBUSADDR[1]
2	SSMBUSADDR[2]
3	1
4	0
5	1
6	1
7	1

Table 2.15 SMBus Slave Interface Address Configuration

The slave SMBus interface responds to the following SMBus transactions initiated by an SMBus master. Initiation of any SMBus transaction other than those listed above produces undefined results. See the SMBus 2.0 specification for a detailed description of the following transactions:

- *Byte and Word Write/Read*
- *Block Write/Read*

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Notes

SMBus Master Interface

Connected to the master SMBus interface are twenty-two 16-bit I/O Expanders (MAX7311AUG) and a serial EEPROM, U77 (24LC512). The I/O Expanders are used as the interface for the onboard hot-plug controllers (MIC2591B). The lower three bits of the bus address for the I/O Expander 0 through I/O Expander 20 are fixed through the stuffing resistor as 0x20, 0x22, 0x24, 0x26, 0x28, 0x2A, 0x2C, 0x2E, 0x50, 0x52, x54, 0x56, 0x58, 0x5A, 0x5C, 0x5E, 0xB0, 0xA2, 0xA4, 0xA6, 0xA8, and 0xAA, respectively.

Note: Hot-plug is not implemented when the PES24NT24G2 is installed.

The seven bits address for the selected EEPROM device is fixed at **0b1010_000** by default.

JTAG Header

The EB-LOGAN-19 provides a JTAG connector J73 for access to the PES24NT24G2 JTAG interface. The connector is a 2.54 x 2.54 mm pitch male 14-pin connector. Refer to Table 2.16 for the JTAG Connector J73 pin out.

JTAG Connector J73					
Pin	Signal	Direction	Pin	Signal	Direction
1	/TRST - Test reset	Input	2	GND	—
3	TDI - Test data	Input	4	GND	—
5	TDO - Test data	Output	6	GND	—
7	TMS - Test mode select	Input	8	GND	—
9	TCK - Test clock	Input	10	GND	—
11	3.3V		12	N/C	—
13	GND	—	14	3.3V	

Table 2.16 JTAG Connector Pin Out

PCI Express Connectors

Pin	Side A		Side B	
1	+12V	12V power	PRSNT1#	Hot-Plug presence detect
2	+12V	12V power	+12V	12V power
3	RSVD	Reserved	+12V	12V power
4	GND	Ground	GND	Ground
5	SMCLK	SMBus clock	JTAG2	TCK (Test Clock) JTAG i/f clk i/p
6	SMDAT	SMBus Data	JTAG	TDI (Test Data Input)
7	GND	Ground	JTAG	TDO (Test Data Output)
8	+3.3V	3.3V power	JTAG	TMS (Test Mode Select)
9	JTAG1	TRST# (Test/Reset) resets JTAG i/f	+3.3V	3.3V power
10	3.3Vaux	3.3V auxiliary power	+3.3V	3.3V power
11	WAKE#	Signal for Link reactivation	PERST#	Fundamental Reset
Mechanical Key				

Table 2.17 PCI Express x8 Connector Pinout (Part 1 of 3)

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Notes

Pin	Side A		Side B	
12	RSVD	Reserved	GND	Ground
13	GND	Ground	REFCLK+	REFCLK Reference clock
14	PETp0	Transmitter differential	REFCLK-	(differential pair)
15	PETn0	pair, Lane 0	GND	Ground
16	GND	Ground	PERp0	Receiver differential
17	PRSNT2#	Hot-Plug presence detect	PERn0	pair, Lane 0
18	GND	Ground	GND	Ground
19	PETp1	Transmitter differential	RSVD	Reserved
20	PETn1	pair, Lane 1	GND	Ground
21	GND	Ground	PERp1	Receiver differential
22	GND	Ground	PERn1	pair, Lane 1
23	PETp2	Transmitter differential	GND	Ground
24	PETn2	pair, Lane 2	GND	Ground
25	GND	Ground	PERp2	Receiver differential
26	GND	Ground	PERn2	pair, Lane 2
27	PETp3	Transmitter differential	GND	Ground
28	PETn3	pair, Lane 3	GND	Ground
29	GND	Ground	PERp3	Receiver differential
30	RSVD	Reserved	PERn3	pair, Lane 3
31	PRSNT2#	Hot-Plug presence detect	GND	Ground
32	GND	Ground	RSVD	Reserved
33	PETp4	Transmitter differential	RSVD	Reserved
34	PETn4	pair, Lane 4	GND	Ground
35	GND	Ground	PERp4	Receiver differential
36	GND	Ground	PERn4	pair, Lane 4
37	PETp5	Transmitter differential	GND	Ground
38	PETn5	pair, Lane 5	GND	Ground
39	GND	Ground	PERp5	Receiver differential
40	GND	Ground	PERn5	pair, Lane 5
41	PETp6	Transmitter differential	GND	Ground
42	PETn6	pair, Lane 6	GND	Ground
43	GND	Ground	PERp6	Receiver differential
44	GND	Ground	PERn6	pair, Lane 6
45	PETp7	Transmitter differential	GND	Ground
46	PETn7	pair, Lane 7	GND	Ground

Table 2.17 PCI Express x8 Connector Pinout (Part 2 of 3)

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Notes

Pin	Side A		Side B	
47	GND	Ground	PERp7	Receiver differential
48	PRSNT2#	Hot-Plug presence detect	PERn7	pair, Lane 7
49	GND	Ground	GND	Ground

Table 2.17 PCI Express x8 Connector Pinout (Part 3 of 3)

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Notes

EB-LOGAN-19 Board Figure

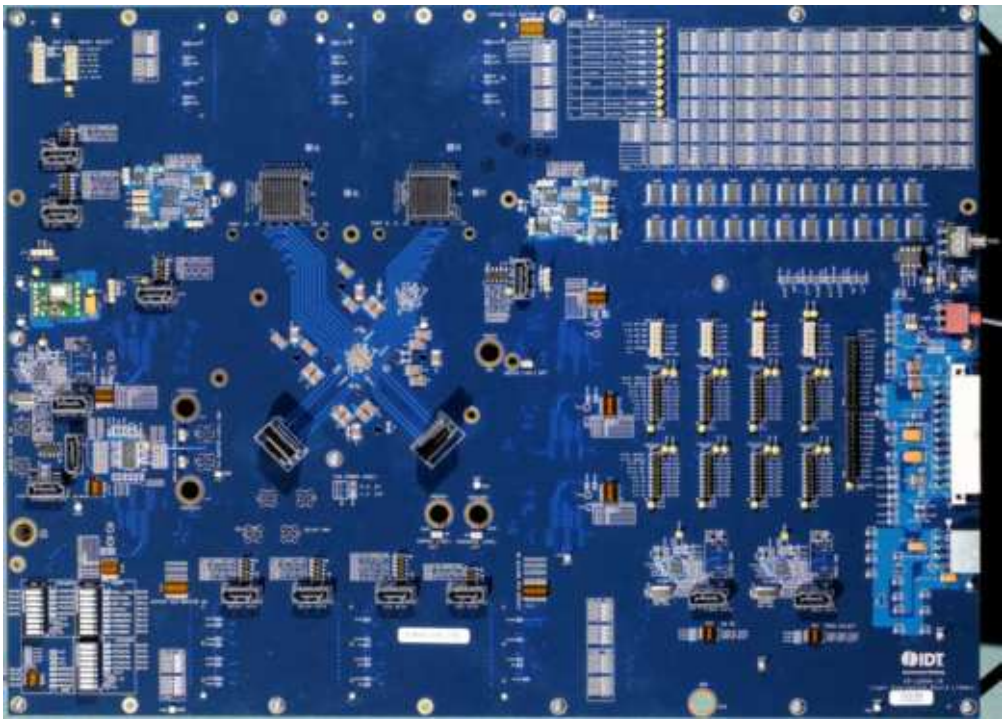


Figure 2.9 EB24NT24G2 Evaluation Board

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Notes

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Software for the EB-LOGAN-19 Eval Board

Notes

Introduction

This chapter discusses some of the main features of the available software to give users a better understanding of what can be achieved with the EB-LOGAN-19 evaluation board using the device management software.

Device management software and related user documentation are available on a CD which is included in the Evaluation Board Kit. This information is also available on IDT FTP site and also at my.idt.com. For more information, please go to: http://www.idt.com/?app=TechSupport&prodFamily=PCIe%20Switches or email IDT at ssdhelp@idt.com.

Device Management Software

The primary use of the Device Management Software package is to enable users of the evaluation board to access all the registers in the PES24NT24G2 device. This access can be achieved using the PCI Express in-band configuration cycles through the upstream port on the PES24NT24G2 or through the SMBUS salve interface available on the IDT PCIe switch.

This software also enables users to save a snapshot of the current register set into a dump file which can be used for debugging purposes. An export/import facility is also available to create and use “Configuration” files which can be used to initialize the switch device with specific values in specific registers.

A conversion utility is also provided to translate a configuration file into an EEPROM programmable data structure. This enables the user to program an appropriate serial EEPROM with desirable register settings for the PES24NT24G2, and then to populate that EEPROM onto the Evaluation Board. It is also possible to program the EEPROM directly on the Evaluation Board using a feature provided by the software package.

The front-end of the Device Management Software is a user-friendly Graphical User Interface which allows the user to quickly read or write the registers of interest. The GUI also permits the user to run the software in “simulation” mode with no real hardware attached, allowing the creation of configuration files for the PES24NT24G2 in the absence of the actual device.

Much of the Device Management Software is written with device-independent and OS-independent code. The software is expected to work on Linux (/sys interface) and MS Windows XP. It may function well on various flavors of MS Windows, but may not be validated on all. The fact that the software is device-independent assures its scalability to future PCIe parts from IDT. Once users are familiar with the GUI, they will be able to use the same GUI on all PCIe parts from IDT. This software is customized for each device through an XML device description file which includes information on the number of ports, registers, types of registers, information on bit-fields within each register, etc.

The actual program name of the Device Management Software is “PCIeBrowser” (an executable file under Windows or Linux). Revision 5.0.1 or later is required for devices in the PES24NT24G2 product family family.

Device Drivers

The PES24NT24G2 and other members of this switch family offer Non-Transparent Bridging and built-in DMA capability inside the device. Device drivers are needed to take advantage of these features. Sample code for these drivers is available from IDT for the Linux operating system. Additionally, there a few other software packages available from IDT. These packages are not related to the evaluation board per se, and therefore not listed here. However, several of these packages may prove to be useful for specific device or system functionality. For more information, please go to http://www.idt.com/?app=TechSupport&prodFamily=PCIe%20Switches or email IDT at ssdhelp@idt.com.

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Notes

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Schematics

Notes

Schematics

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REVISIONS				
DCN	REV	DESCRIPTION	DATE	CHANGE BY
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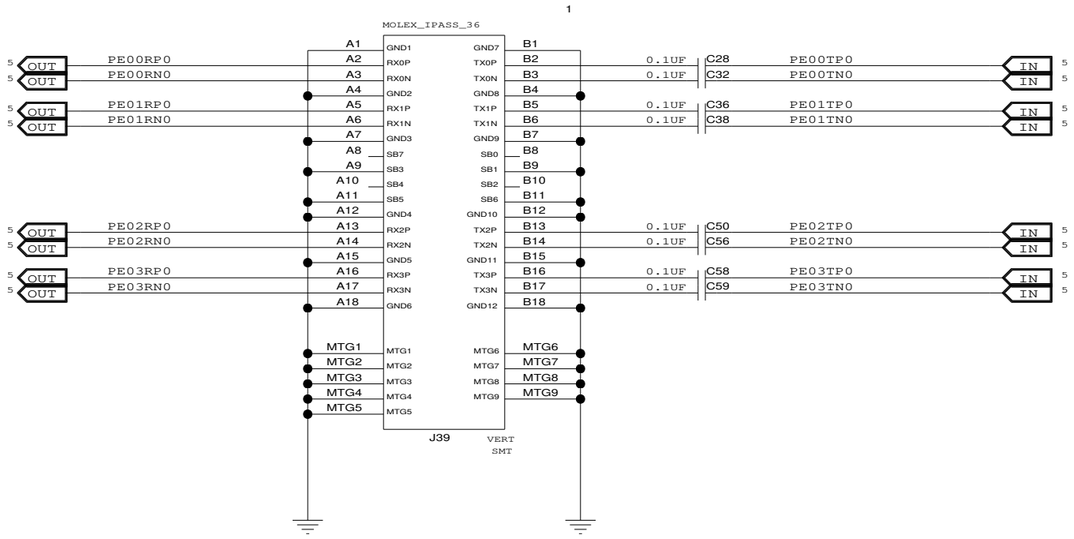
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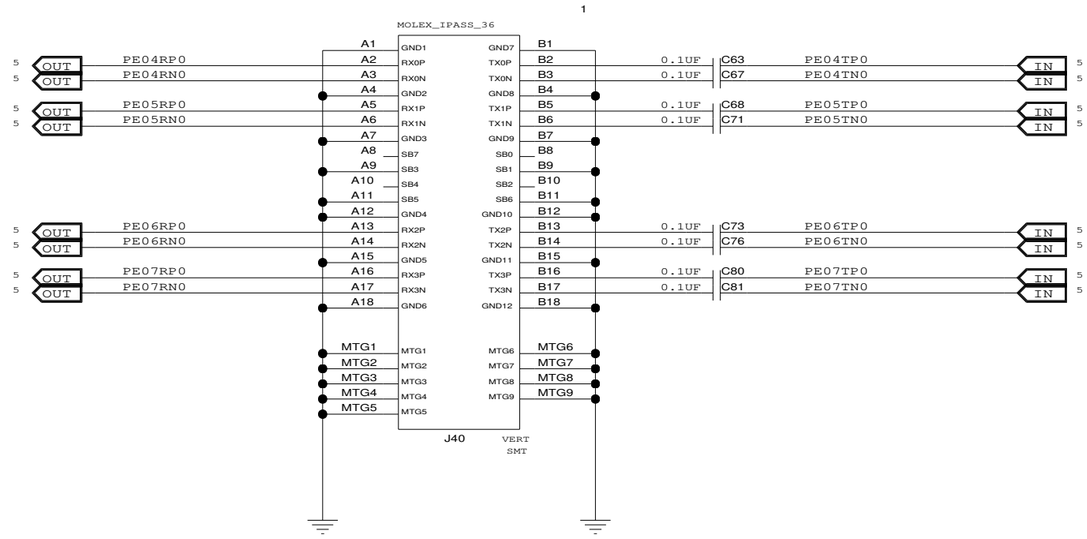
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3. MEZZANINE CONNECTOR PORTS 8, 12
4. MEZZANINE CONNECTOR PORTS 16, 20
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6. 24NT24G2 - CLK, CONFIG, GPIO
7. 24NT24G2 - POWER, GND
8. IOEXPANDER 0-3
9. IOEXPANDER 4-7
10. IOEXPANDER 8-11
11. IOEXPANDER 12-13
12. IOEXPANDER 16-19
13. IOEXPANDER 20-21
14. HOT PLUG CONTROL PORTS 8-12
15. HOT PLUG CONTROL PORTS 16-20
16. SLOT RESETS AND WAKE PULL-UPS
17. CLOCK
18. CLOCK BUFFER
19. CLOCK SELECTOR - DUT PCLK 8
20. CLOCK SELECTOR - DUT PCLK 16
21. CLOCK SELECTOR - SLOTS 0-20, GCLK
22. POWER CONNECTORS, MIN LOAD RESISTORS
23. POWER REGULATOR - VDDIO
24. POWER REGULATOR - VDDCORE
25. POWER REGULATOR - VDDPEA
26. POWER REGULATOR - VDDPEHA
27. POWER REGULATOR - VDDPETA
28. RESET, SMBUS, EEPROM, JTAG
29. DIP SWITCHES
30. LED - PORT STATUS (1 OF 7)
31. LED - PORT STATUS (2 OF 7)
32. LED - PORT STATUS (3 OF 7)
33. LED - PORT STATUS (4 OF 7)
34. LED - PORT STATUS (5 OF 7)
35. LED - PORT STATUS (6 OF 7)
36. LED - PORT STATUS (7 OF 7)
37. 12PK RIBBON CONNECTORS
38 PARTITION RESET SELECT HEADERS
39. SLOT RESET SELECT HEADERS
40. PORT 8 CLOCK GENERATOR
41. PORT 16 CLOCK GENERATOR

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AUTHOR: Tony Tran		CHECKED BY: Derek Huang	
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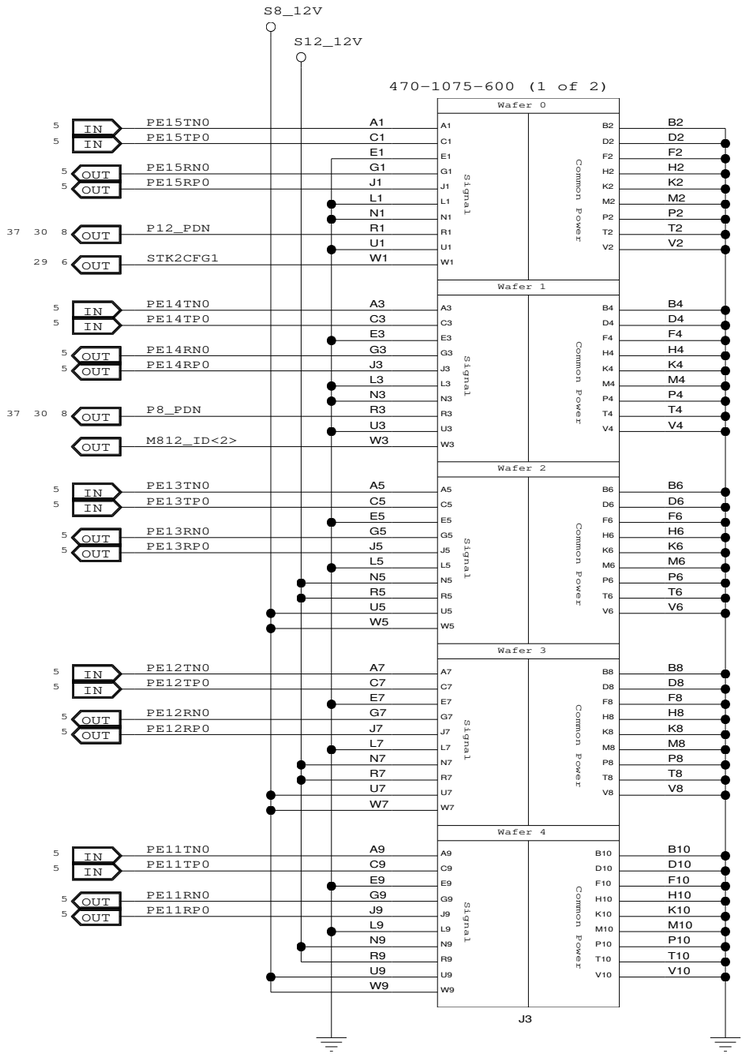
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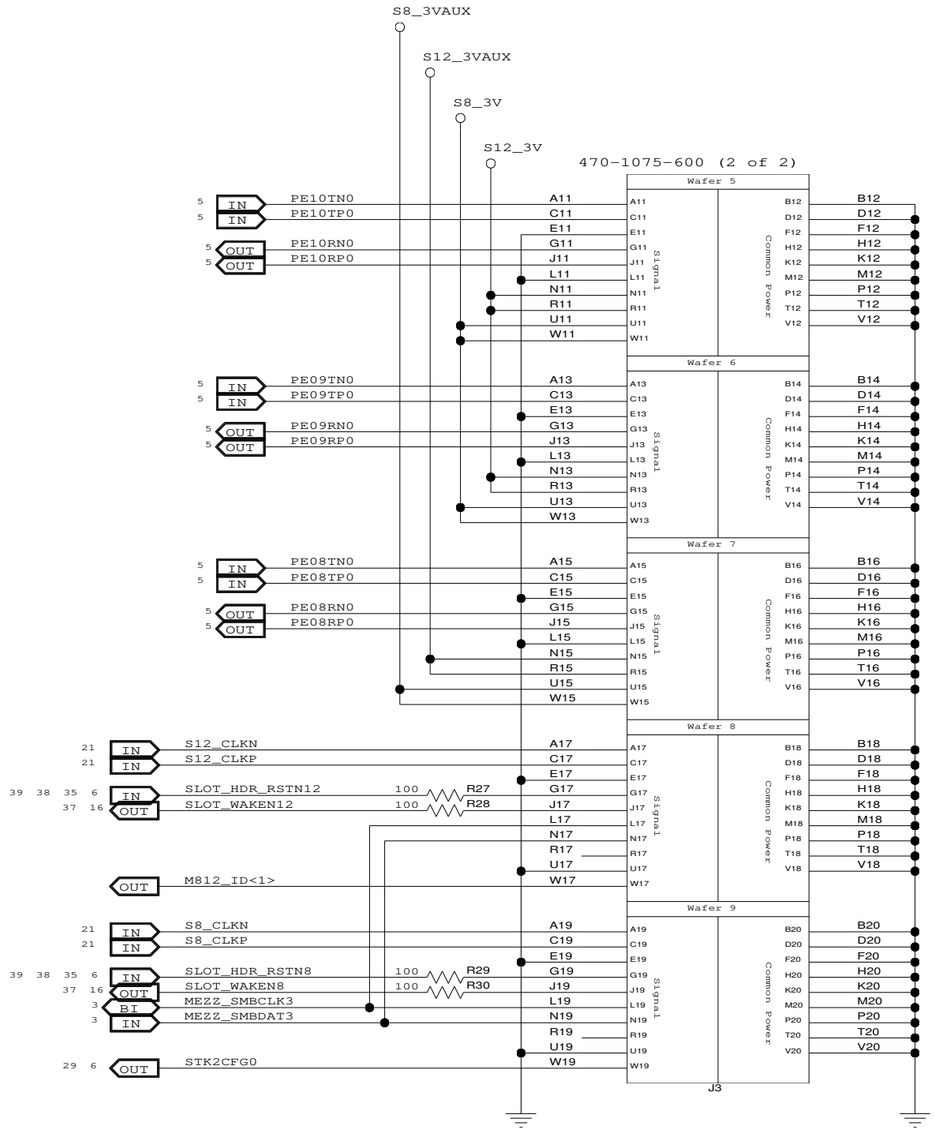
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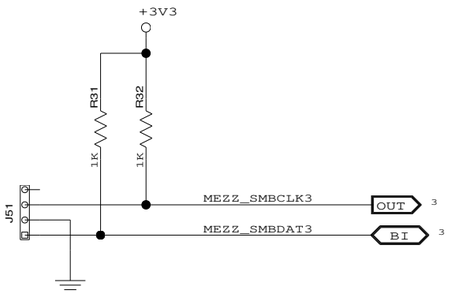
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STK2CFG1 & STK2CFG0 SET BY MEZZ CARDS
X8 – STK2CFG1 = 0, STK2CFG0 = 0
X4 – STK2CFG1 = 0, STK2CFG0 = 1



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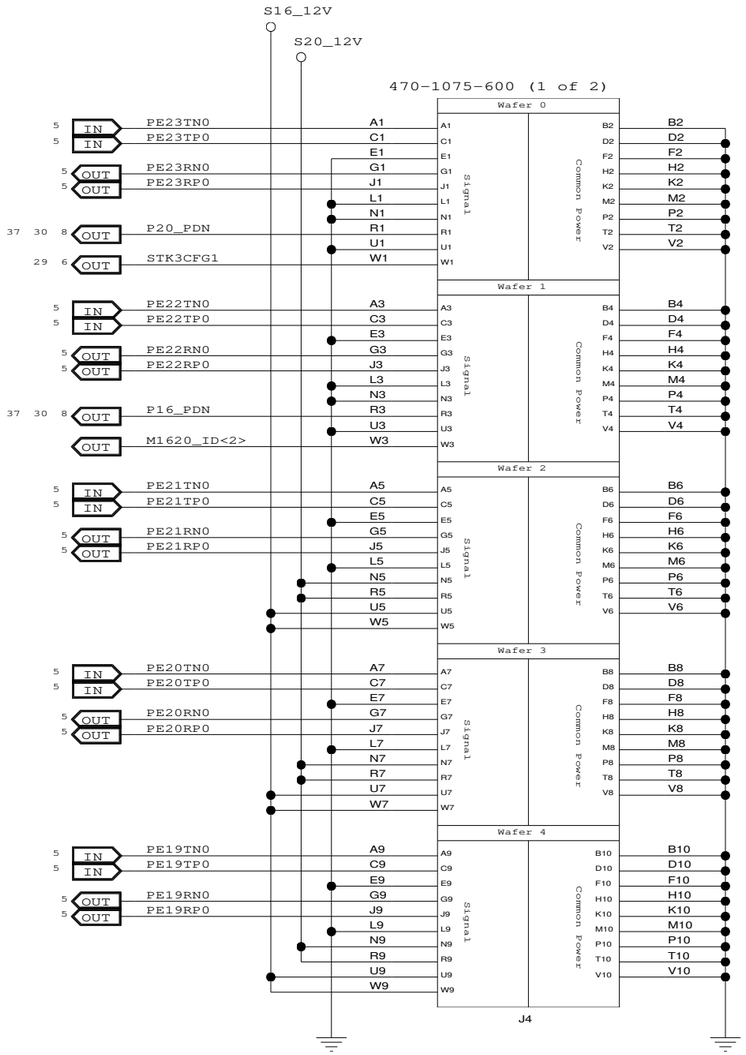
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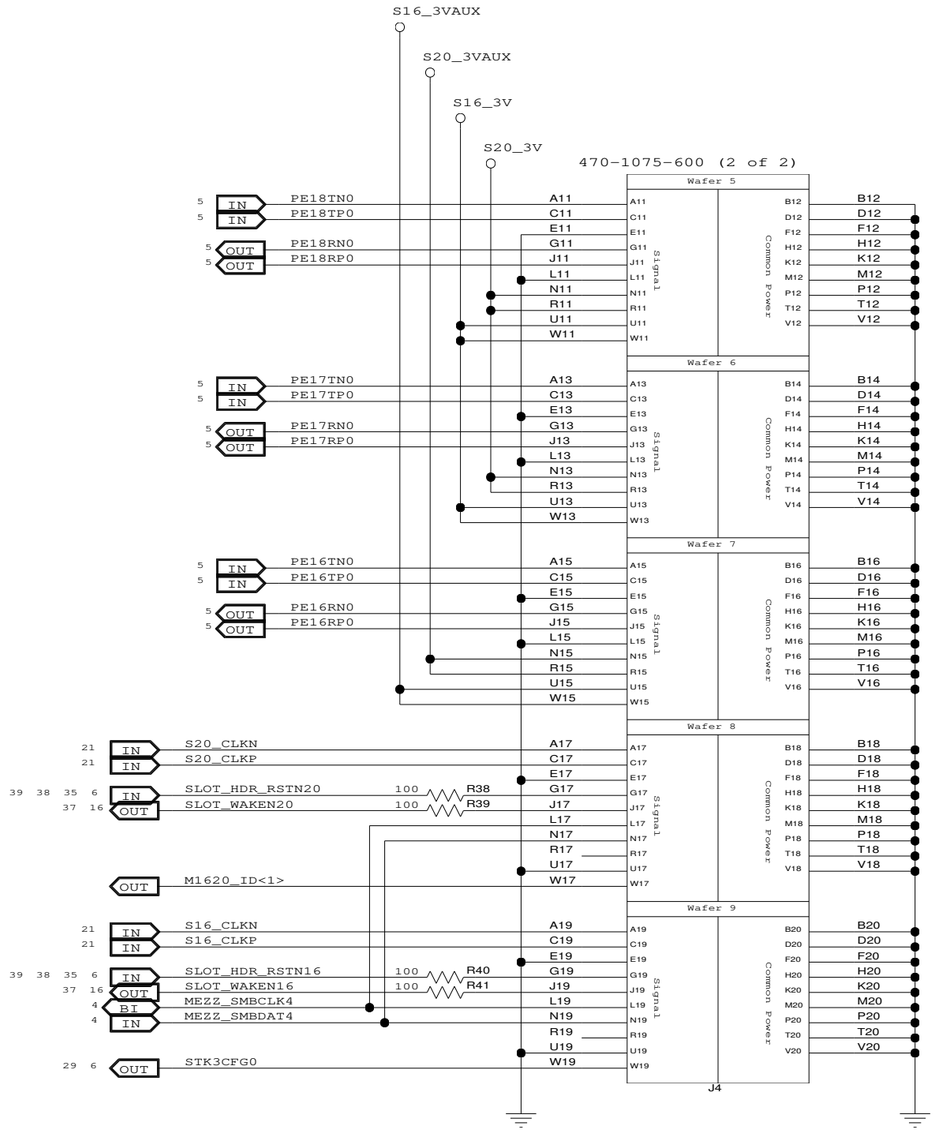
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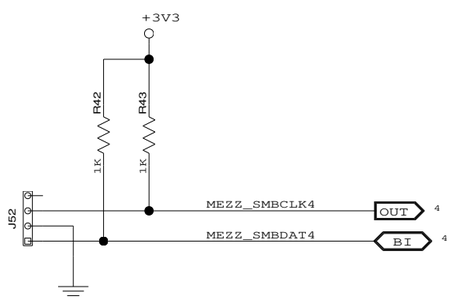
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X4 – STK3CFG1 = 0, STK3CFG0 = 1



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MEZZANINE CONNECTOR PORTS 16/20

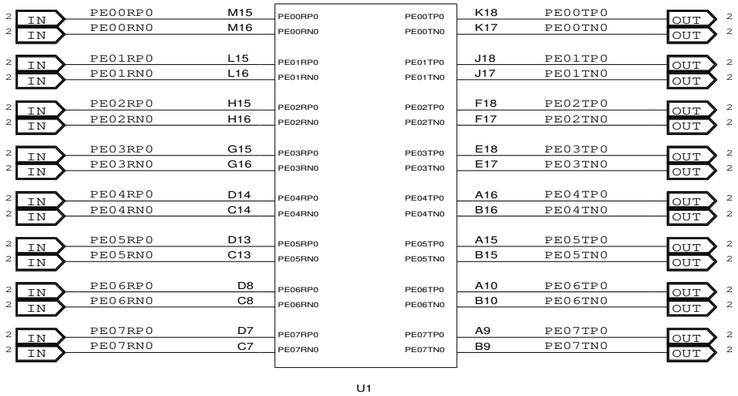
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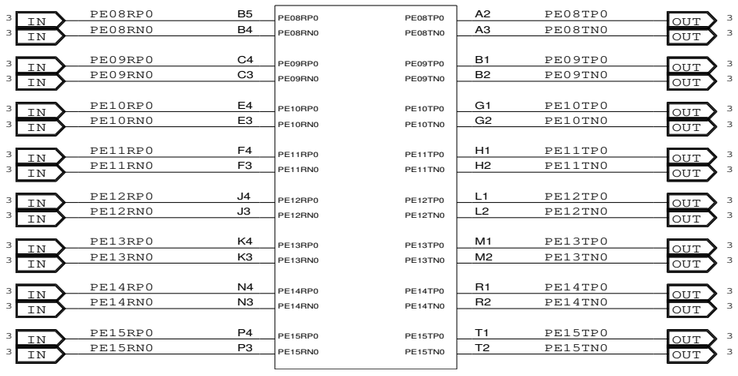
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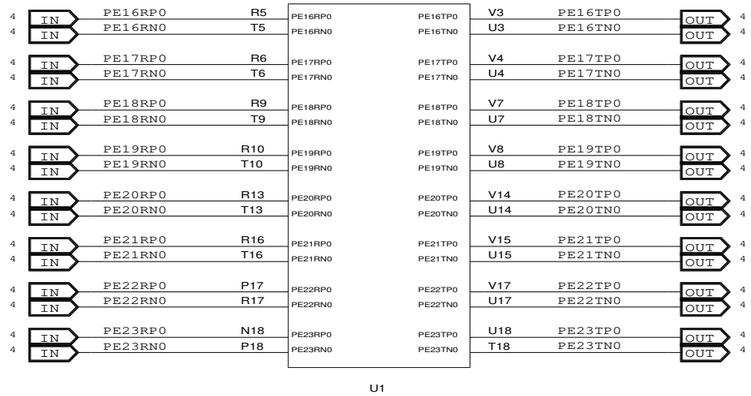
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U1

89HPES24NT24G2 (5/8)



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DUT RESET

HDR_2x6

MAIN_RSTN
SLOT_HDR_RSTN8
SLOT_HDR_RSTN12
SLOT_HDR_RSTN16
SLOT_HDR_RSTN20
TP108
J118

89HPES24NT24G2 (1/8)

GCLK0P
GCLK0N
GCLK1P
GCLK1N
GCLKFSEL
PERSTN
RSTHALT
STK2CFG0
STK2CFG1
STK2CFG2
STK2CFG3
STK2CFG4
STK3CFG0
STK3CFG1
STK3CFG2
STK3CFG3
STK3CFG4
SWMODE0
SWMODE1
SWMODE2
SWMODE3
CLKMODE0
CLKMODE1

P08CLKP
P08CLKN
P16CLKP
P16CLKN
G3
G2
G1

PLACE RESISTORS AS CLOSE TO U1 AS POSSIBLE

REFRES00
REFRES01
REFRES02
REFRES03
REFRES04
REFRES05
REFRES06
REFRES07
REFRESPLL

U1

+3V3

R24 1K
R55 1K

89HPES24NT24G2 (2/8)

MSMBCLK
MSMBDAT
R45 0
SSMBADDR1
SSMBADDR2
SSMBCLK
SSMBDAT
NC1
NC2

JTAG_TCK
JTAG_TDI
JTAG_TDO
JTAG_TMS
JTAG_TRST_N
GPIO_00
GPIO_01
GPIO_02
GPIO_03
GPIO_04
GPIO_05
GPIO_06
GPIO_07
GPIO_08

U1

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24NT24G2 – CLK, CONFIG, GPIO

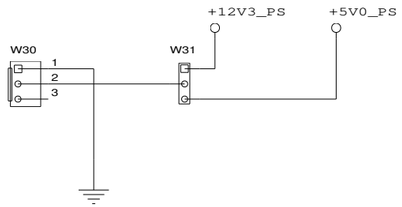
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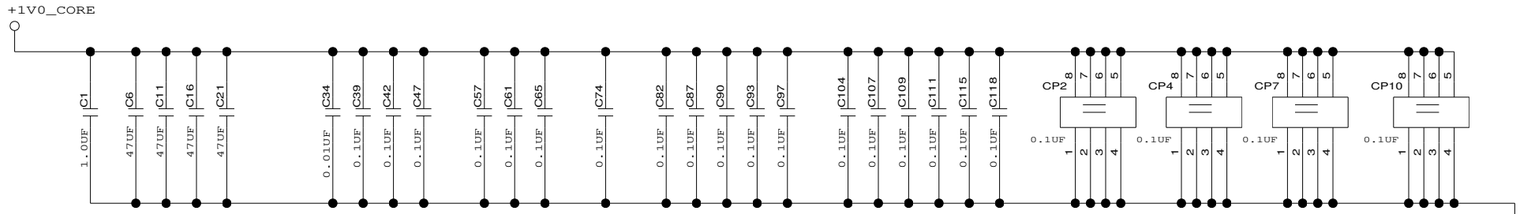
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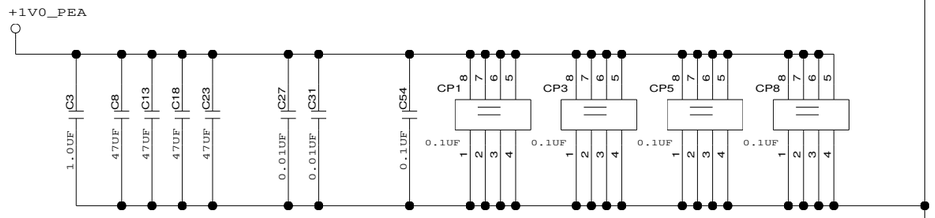
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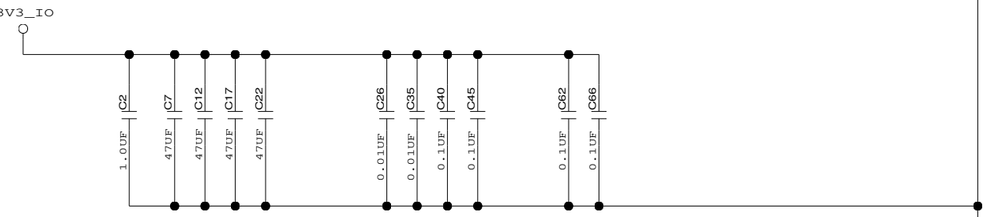
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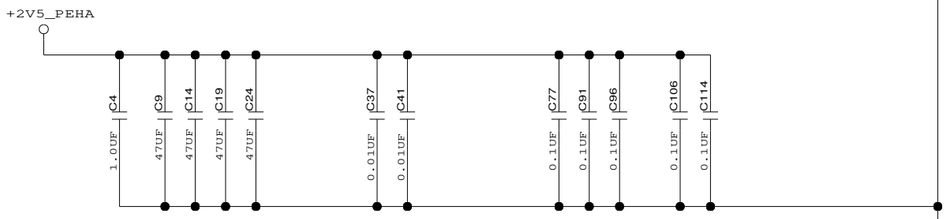
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3 NC

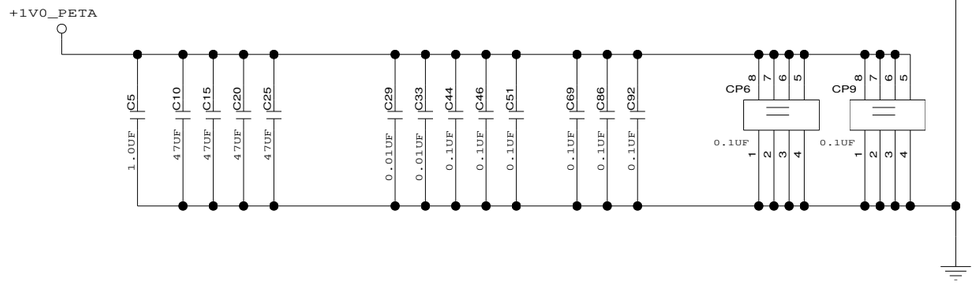


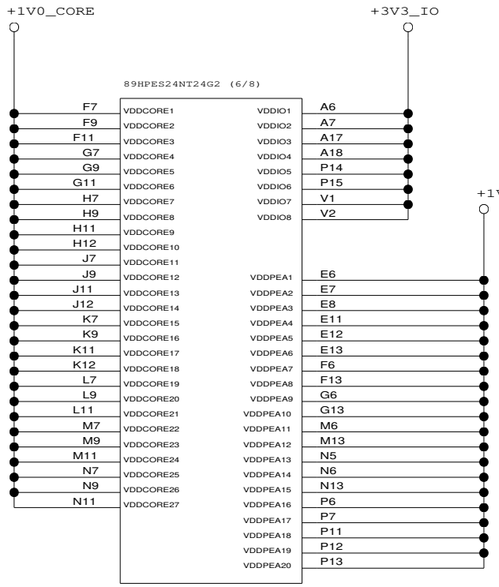


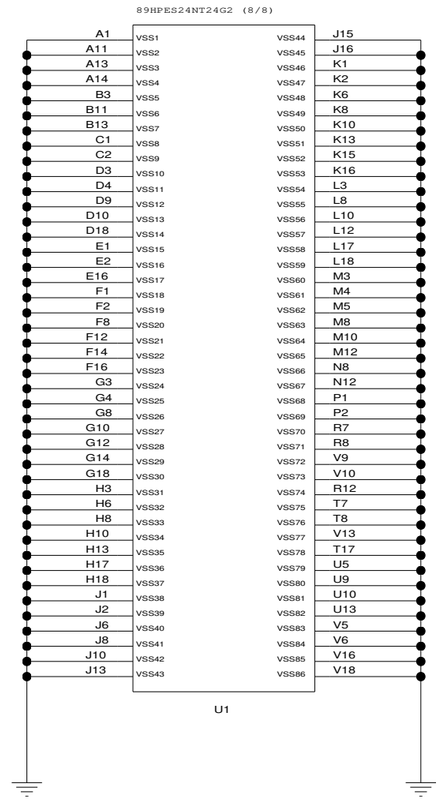


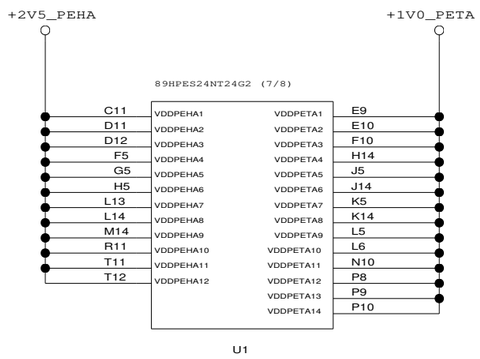












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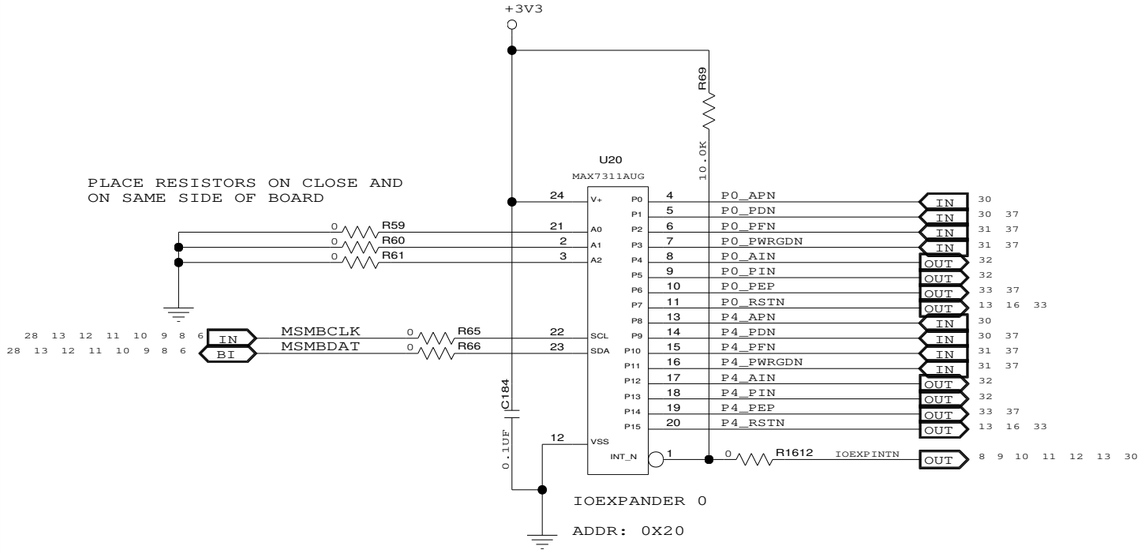
24NT24G2 - POWER

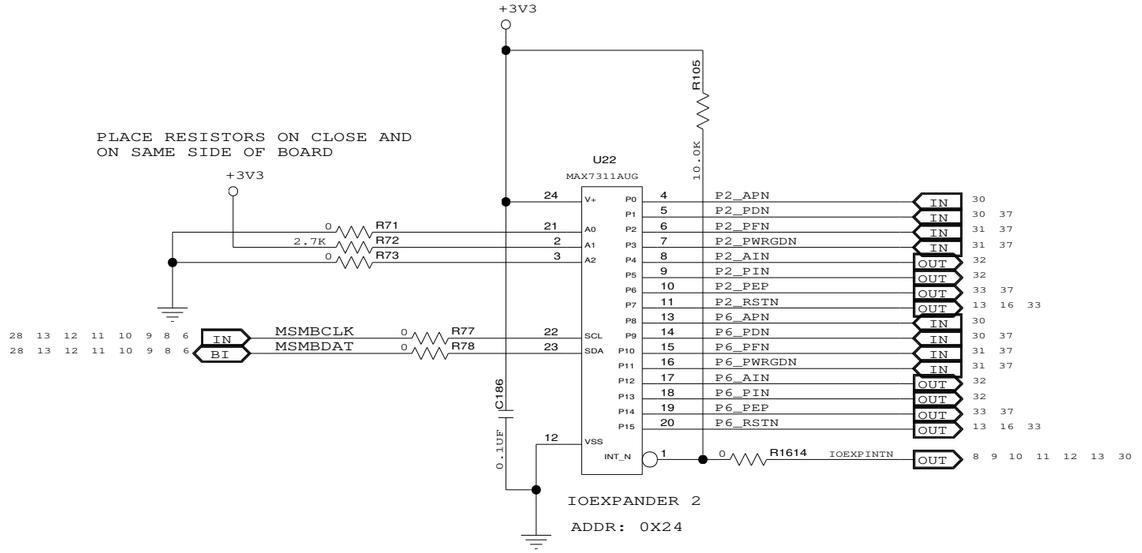
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B	SCH-PESEB-002	18-692-001	2.0

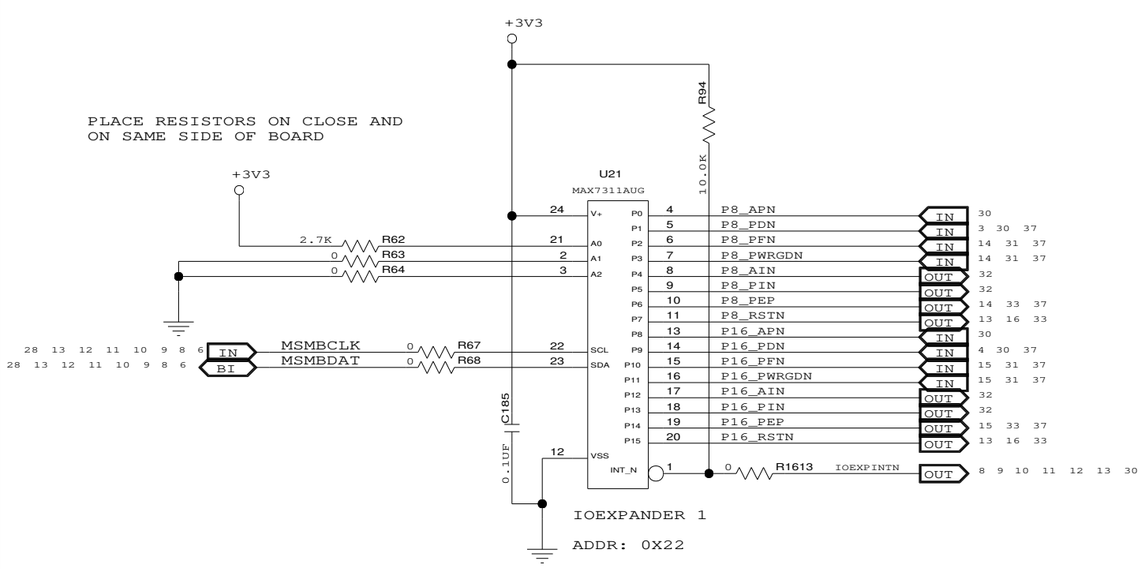
AUTHOR	CHECKED BY
Tony Tran	Derek Huang

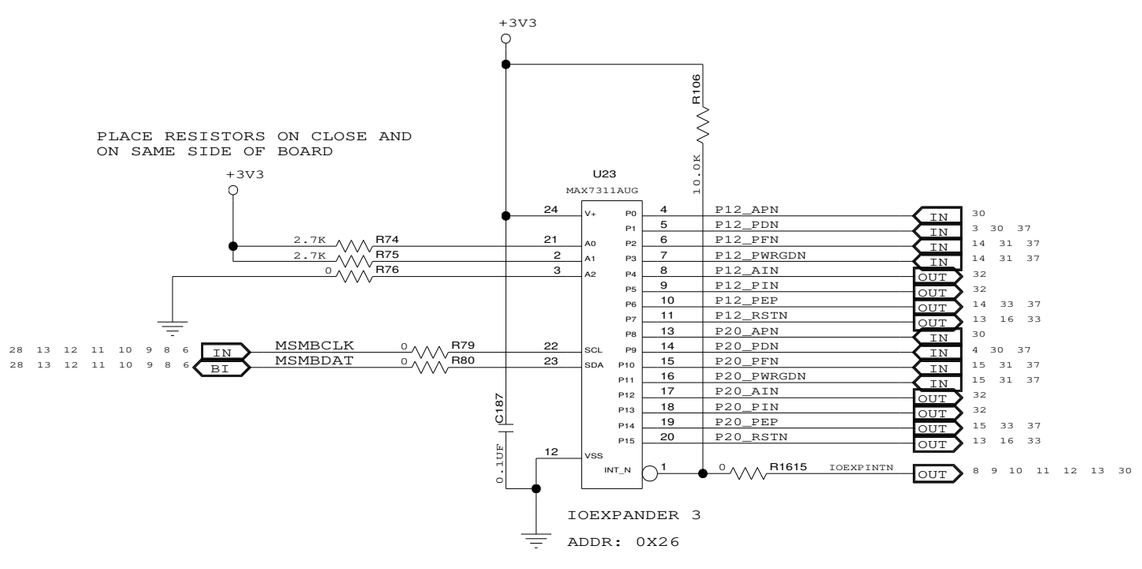
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IOEXPANDER 0-3

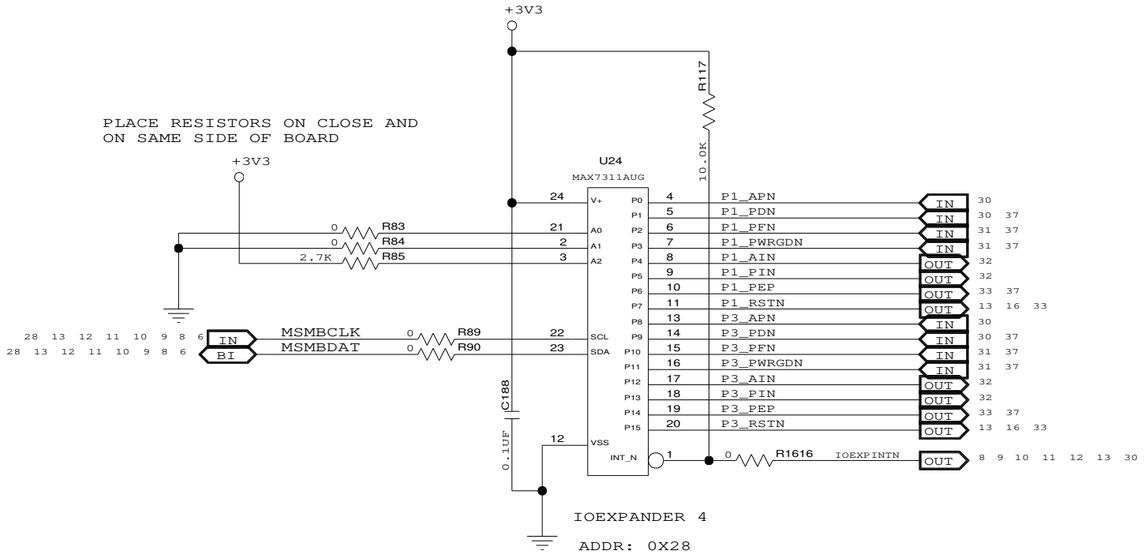
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0

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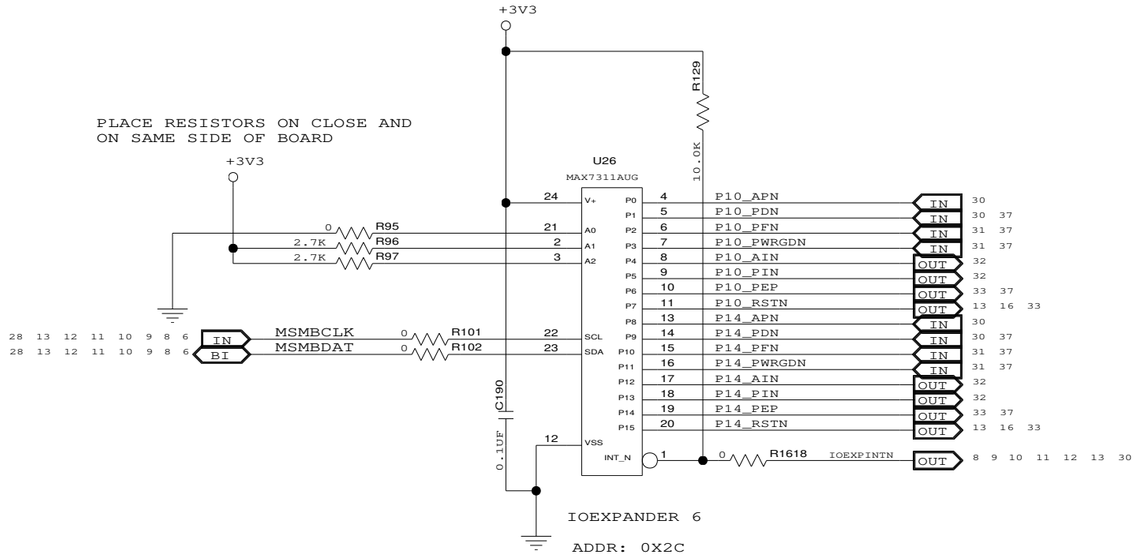
PLACE RESISTORS ON CLOSE AND
ON SAME SIDE OF BOARD



IOEXPANDER 4

ADDR: 0X28

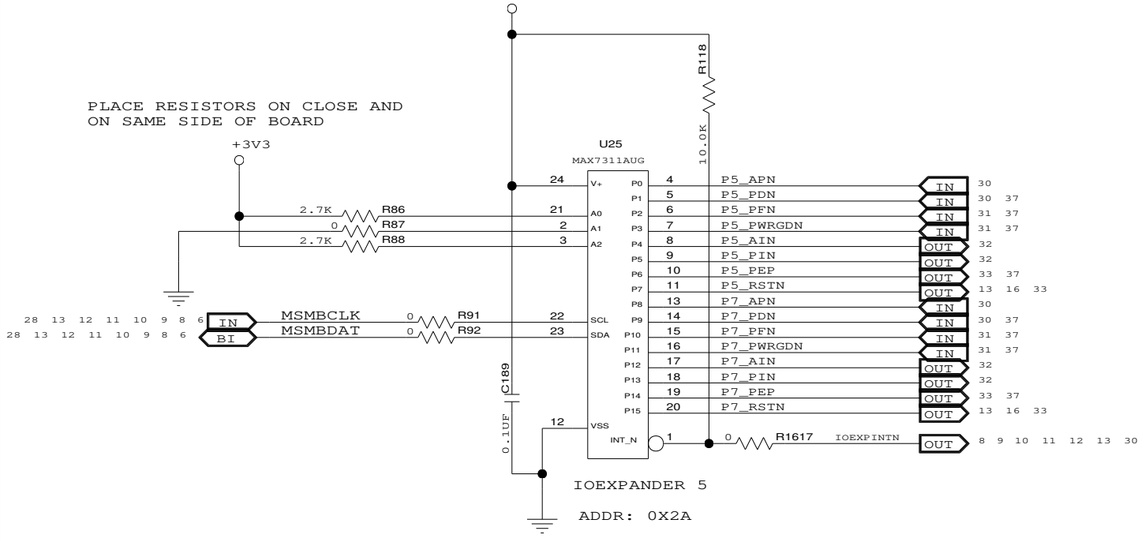
PLACE RESISTORS ON CLOSE AND
ON SAME SIDE OF BOARD



IOEXPANDER 6

ADDR: 0X2C

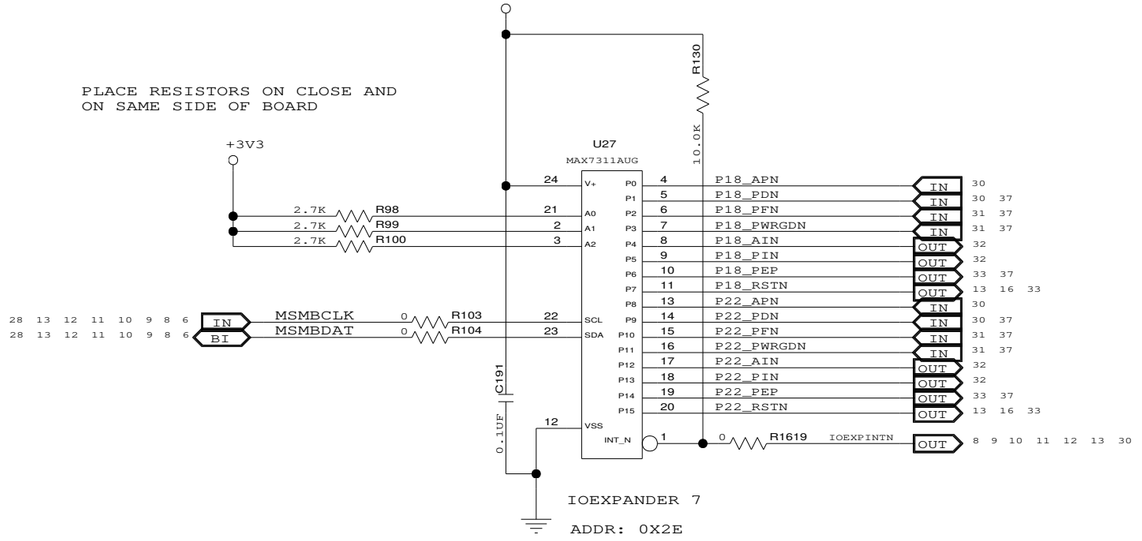
PLACE RESISTORS ON CLOSE AND
ON SAME SIDE OF BOARD



IOEXPANDER 5

ADDR: 0X2A

PLACE RESISTORS ON CLOSE AND
ON SAME SIDE OF BOARD



IOEXPANDER 7

ADDR: 0X2E

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IOEXPANDER 4-7

SIZE	DRAWING NO.	FAB P/N	REV.
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PLACE RESISTORS ON CLOSE AND ON SAME SIDE OF BOARD

+3V3

R141 10.0K

U28 MAX7311AUG

R107 0, R108 0, R109 0

MSMBCLK 0 R113 0, MSMBDAT 0 R114 0

C192 0.1UF

R1620 0

IOEXPINTN

V+	24				
A0	21	P0	4	P9_APN	IN 30
A1	2	P1	5	P9_PDN	IN 30 37
A2	3	P2	6	P9_PFN	IN 31 37
SCL	22	P3	7	P9_PWRGDN	IN 31 37
SDA	23	P4	8	P9_AIN	OUT 32
VSS	12	P5	9	P9_PIN	OUT 32
INT_N	1	P6	10	P9_PEP	OUT 33 37
		P7	11	P9_RSTN	OUT 13 16 33
		P8	13	P11_APN	IN 30
		P9	14	P11_PDN	IN 30 37
		P10	15	P11_PFN	IN 31 37
		P11	16	P11_PWRGDN	IN 31 37
		P12	17	P11_AIN	OUT 32
		P13	18	P11_PIN	OUT 32
		P14	19	P11_PEP	OUT 33 37
		P15	20	P11_RSTN	OUT 13 16 33

IOEXPINTN: OUT 8 9 10 11 12 13 30

IOEXPANDER 8

ADDR: 0X50

PLACE RESISTORS ON CLOSE AND ON SAME SIDE OF BOARD

+3V3

R143 10.0K

U30 MAX7311AUG

R119 0, R120 2.7K, R121 0

MSMBCLK 0 R125 0, MSMBDAT 0 R126 0

C194 0.1UF

R1622 0

IOEXPINTN

V+	24				
A0	21	P0	4	P17_APN	IN 30
A1	2	P1	5	P17_PDN	IN 30 37
A2	3	P2	6	P17_PFN	IN 31 37
SCL	22	P3	7	P17_PWRGDN	IN 31 37
SDA	23	P4	8	P17_AIN	OUT 32
VSS	12	P5	9	P17_PIN	OUT 32
INT_N	1	P6	10	P17_PEP	OUT 33 37
		P7	11	P17_RSTN	OUT 13 16 33
		P8	13	P19_APN	IN 30
		P9	14	P19_PDN	IN 30 37
		P10	15	P19_PFN	IN 31 37
		P11	16	P19_PWRGDN	IN 31 37
		P12	17	P19_AIN	OUT 32
		P13	18	P19_PIN	OUT 32
		P14	19	P19_PEP	OUT 33 37
		P15	20	P19_RSTN	OUT 13 16 33

IOEXPINTN: OUT 8 9 10 11 12 13 30

IOEXPANDER 10

ADDR: 0X54

PLACE RESISTORS ON CLOSE AND ON SAME SIDE OF BOARD

+3V3

R142 10.0K

U29 MAX7311AUG

R110 0, R111 0, R112 0

MSMBCLK 0 R115 0, MSMBDAT 0 R116 0

C193 0.1UF

R1621 0

IOEXPINTN

V+	24				
A0	21	P0	4	P13_APN	IN 30
A1	2	P1	5	P13_PDN	IN 30 37
A2	3	P2	6	P13_PFN	IN 31 37
SCL	22	P3	7	P13_PWRGDN	IN 31 37
SDA	23	P4	8	P13_AIN	OUT 32
VSS	12	P5	9	P13_PIN	OUT 32
INT_N	1	P6	10	P13_PEP	OUT 33 37
		P7	11	P13_RSTN	OUT 13 16 33
		P8	13	P15_APN	IN 30
		P9	14	P15_PDN	IN 30 37
		P10	15	P15_PFN	IN 31 37
		P11	16	P15_PWRGDN	IN 31 37
		P12	17	P15_AIN	OUT 32
		P13	18	P15_PIN	OUT 32
		P14	19	P15_PEP	OUT 33 37
		P15	20	P15_RSTN	OUT 13 16 33

IOEXPINTN: OUT 8 9 10 11 12 13 30

IOEXPANDER 9

ADDR: 0X52

PLACE RESISTORS ON CLOSE AND ON SAME SIDE OF BOARD

+3V3

R144 10.0K

U31 MAX7311AUG

R122 0, R123 2.7K, R124 0

MSMBCLK 0 R127 0, MSMBDAT 0 R128 0

C195 0.1UF

R1623 0

IOEXPINTN

V+	24				
A0	21	P0	4	P21_APN	IN 30
A1	2	P1	5	P21_PDN	IN 30 37
A2	3	P2	6	P21_PFN	IN 31 37
SCL	22	P3	7	P21_PWRGDN	IN 31 37
SDA	23	P4	8	P21_AIN	OUT 32
VSS	12	P5	9	P21_PIN	OUT 32
INT_N	1	P6	10	P21_PEP	OUT 33 37
		P7	11	P21_RSTN	OUT 13 16 33
		P8	13	P23_APN	IN 30
		P9	14	P23_PDN	IN 30 37
		P10	15	P23_PFN	IN 31 37
		P11	16	P23_PWRGDN	IN 31 37
		P12	17	P23_AIN	OUT 32
		P13	18	P23_PIN	OUT 32
		P14	19	P23_PEP	OUT 33 37
		P15	20	P23_RSTN	OUT 13 16 33

IOEXPINTN: OUT 8 9 10 11 12 13 30

IOEXPANDER 11

ADDR: 0X56

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IOEXPANDER 8-11

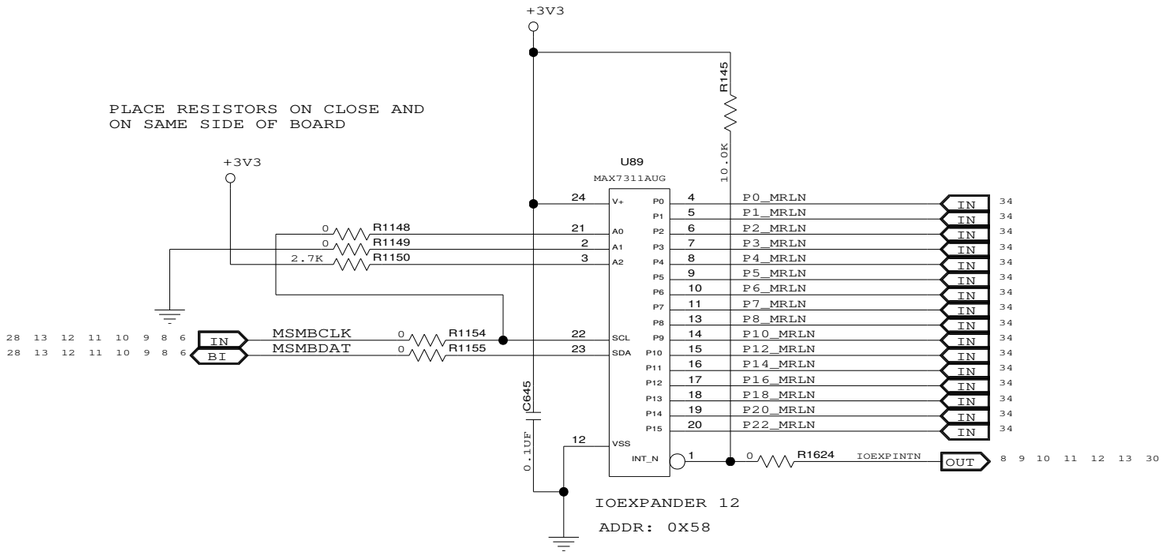
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B	SCH-PESEB-002	18-692-001	2.0

AUTHOR	CHECKED BY
Tony Tran	Derek Huang

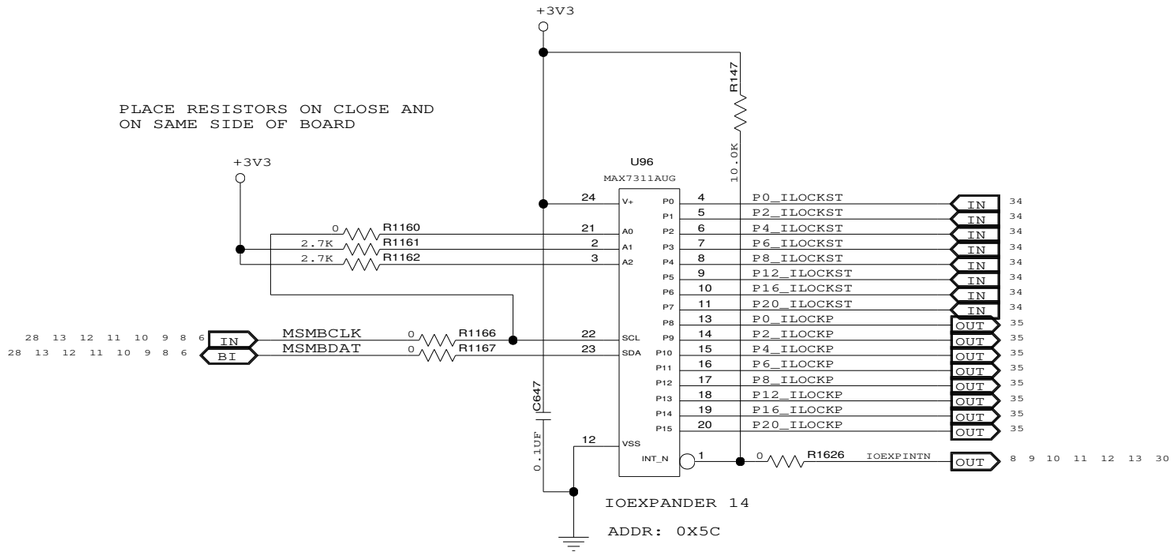
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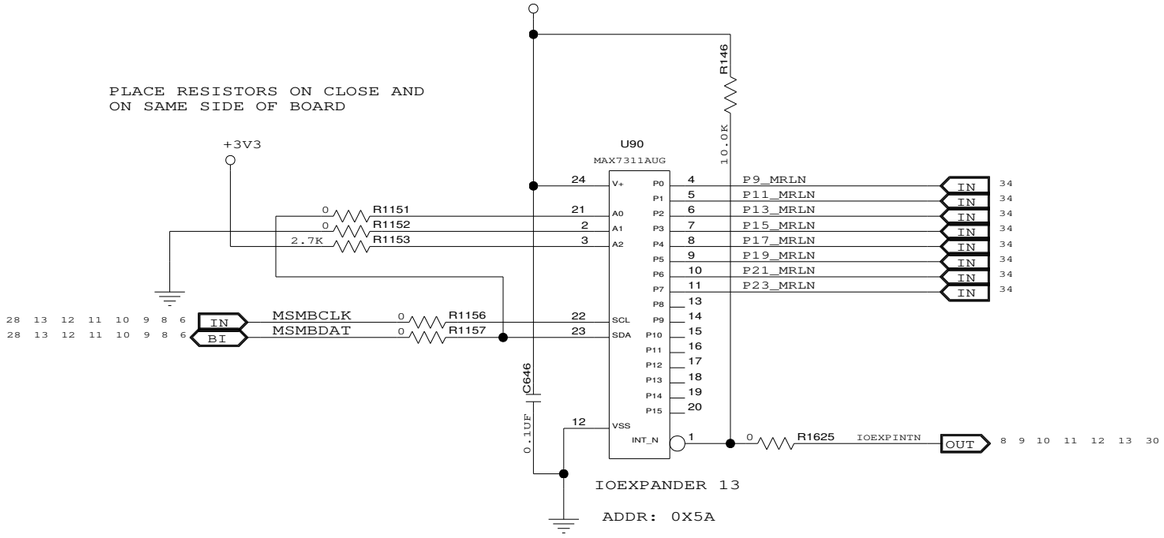
PLACE RESISTORS ON CLOSE AND
ON SAME SIDE OF BOARD



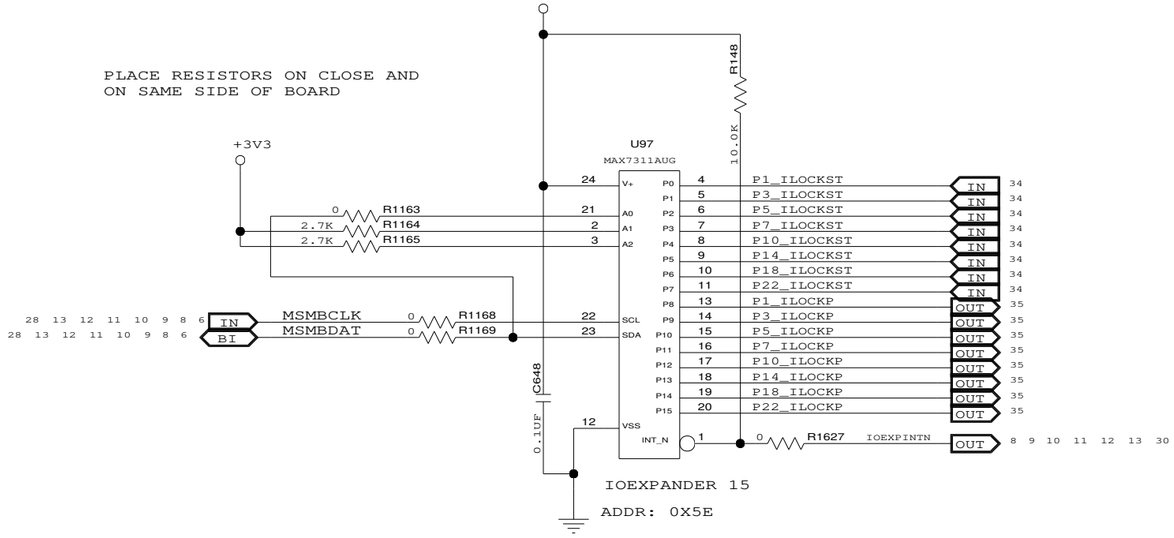
PLACE RESISTORS ON CLOSE AND
ON SAME SIDE OF BOARD



PLACE RESISTORS ON CLOSE AND
ON SAME SIDE OF BOARD



PLACE RESISTORS ON CLOSE AND
ON SAME SIDE OF BOARD



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IOEXPANDER 12-15

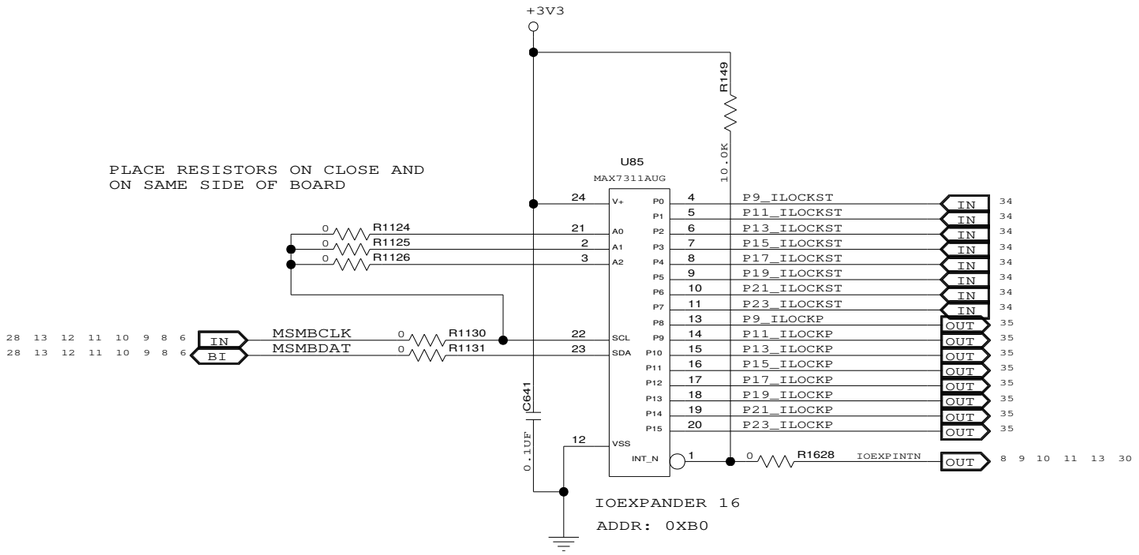
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0

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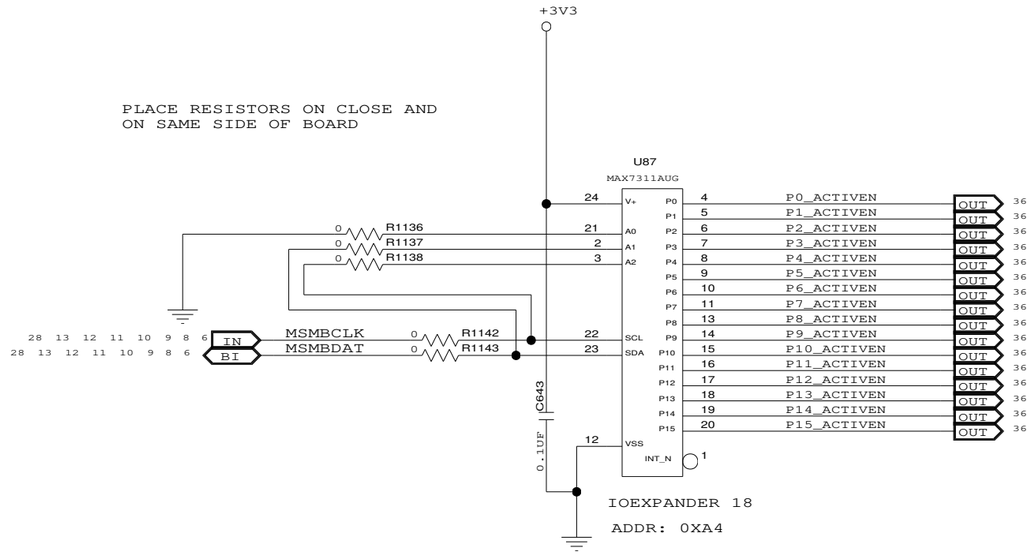
PLACE RESISTORS ON CLOSE AND
ON SAME SIDE OF BOARD



IOEXPANDER 16

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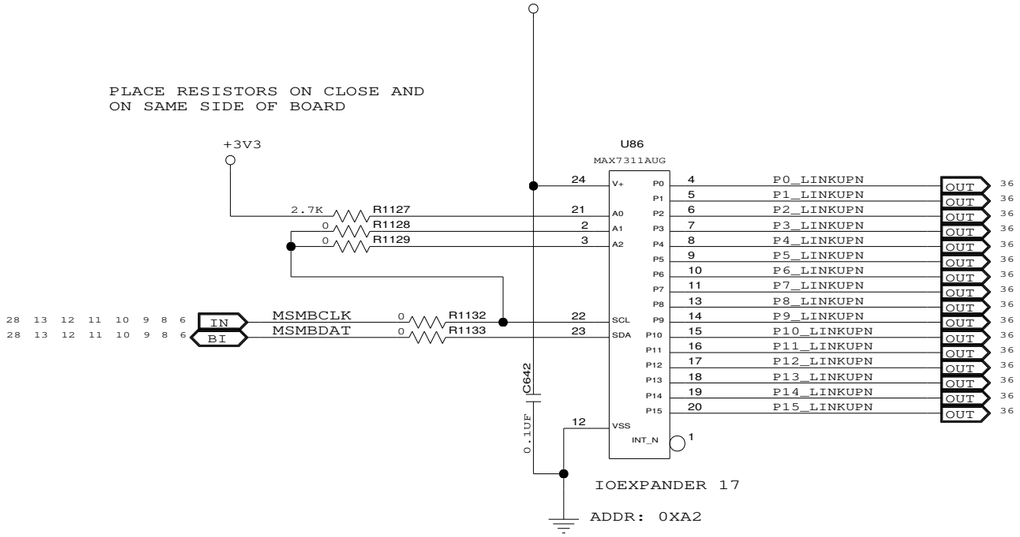
PLACE RESISTORS ON CLOSE AND
ON SAME SIDE OF BOARD



IOEXPANDER 18

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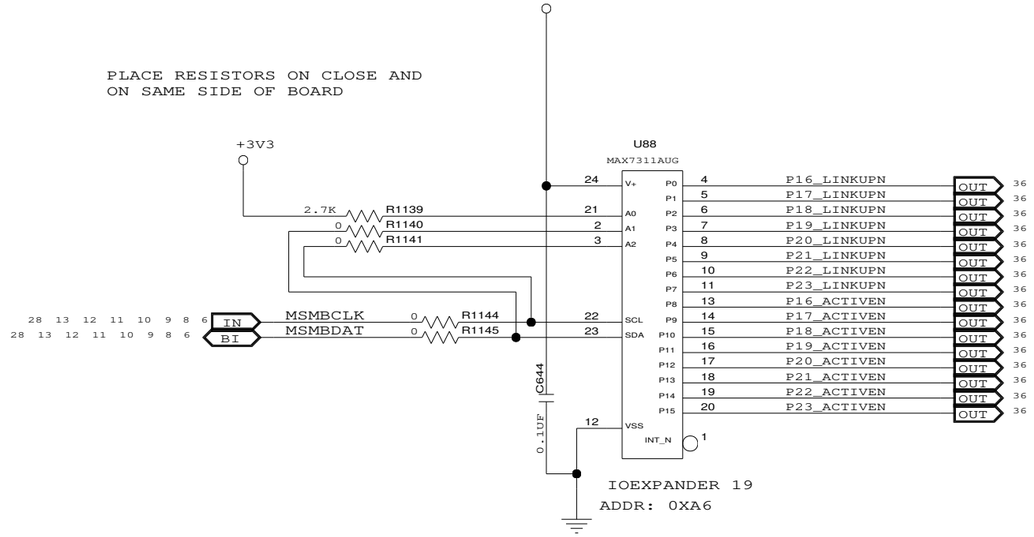
PLACE RESISTORS ON CLOSE AND
ON SAME SIDE OF BOARD



IOEXPANDER 17

ADDR: 0XA2

PLACE RESISTORS ON CLOSE AND
ON SAME SIDE OF BOARD



IOEXPANDER 19

ADDR: 0XA6

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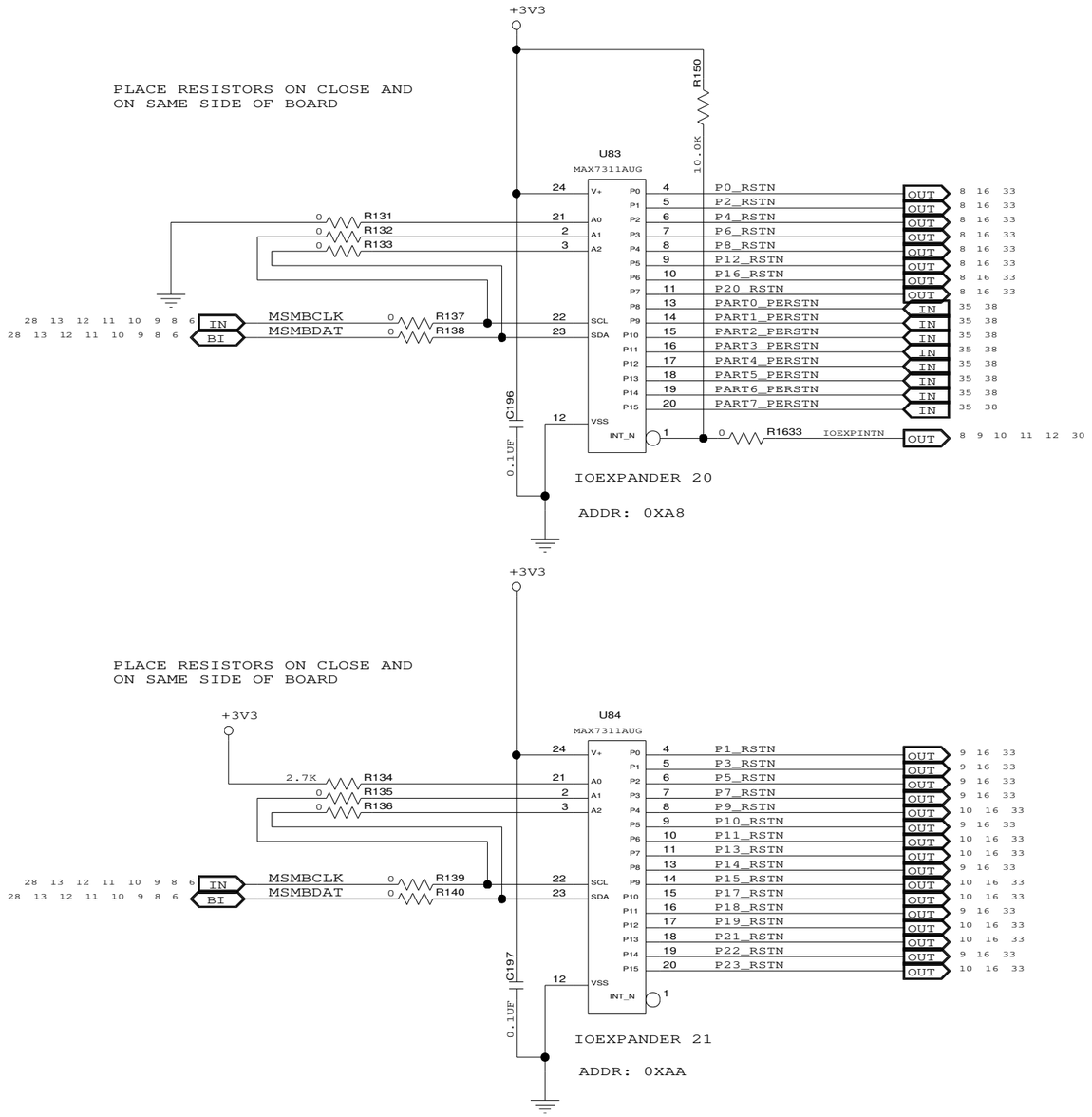
IOEXPANDER 16-19

SIZE	DRAWING NO.	FAB P/N	REV.
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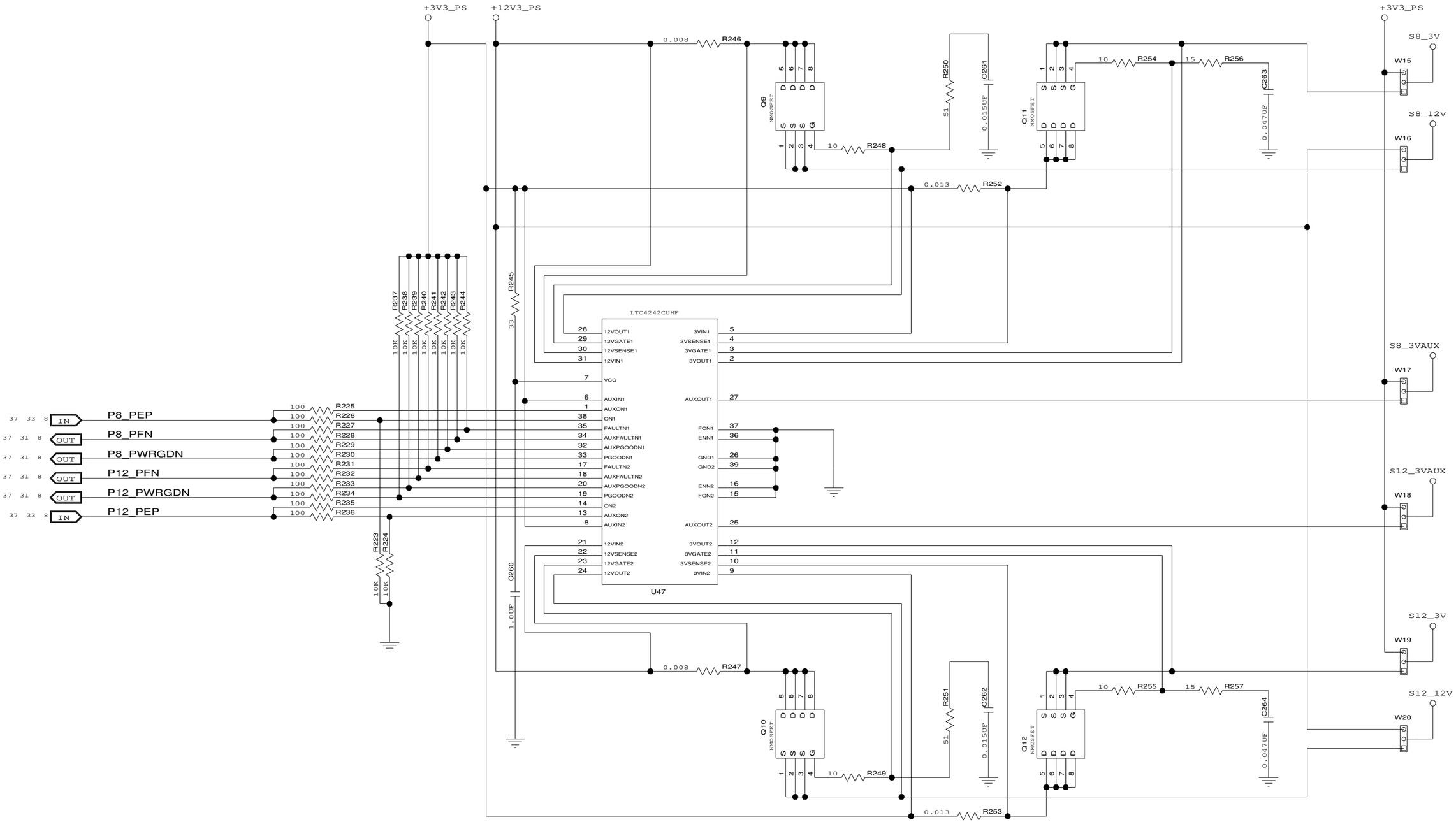
IOEXPANDER 20-21

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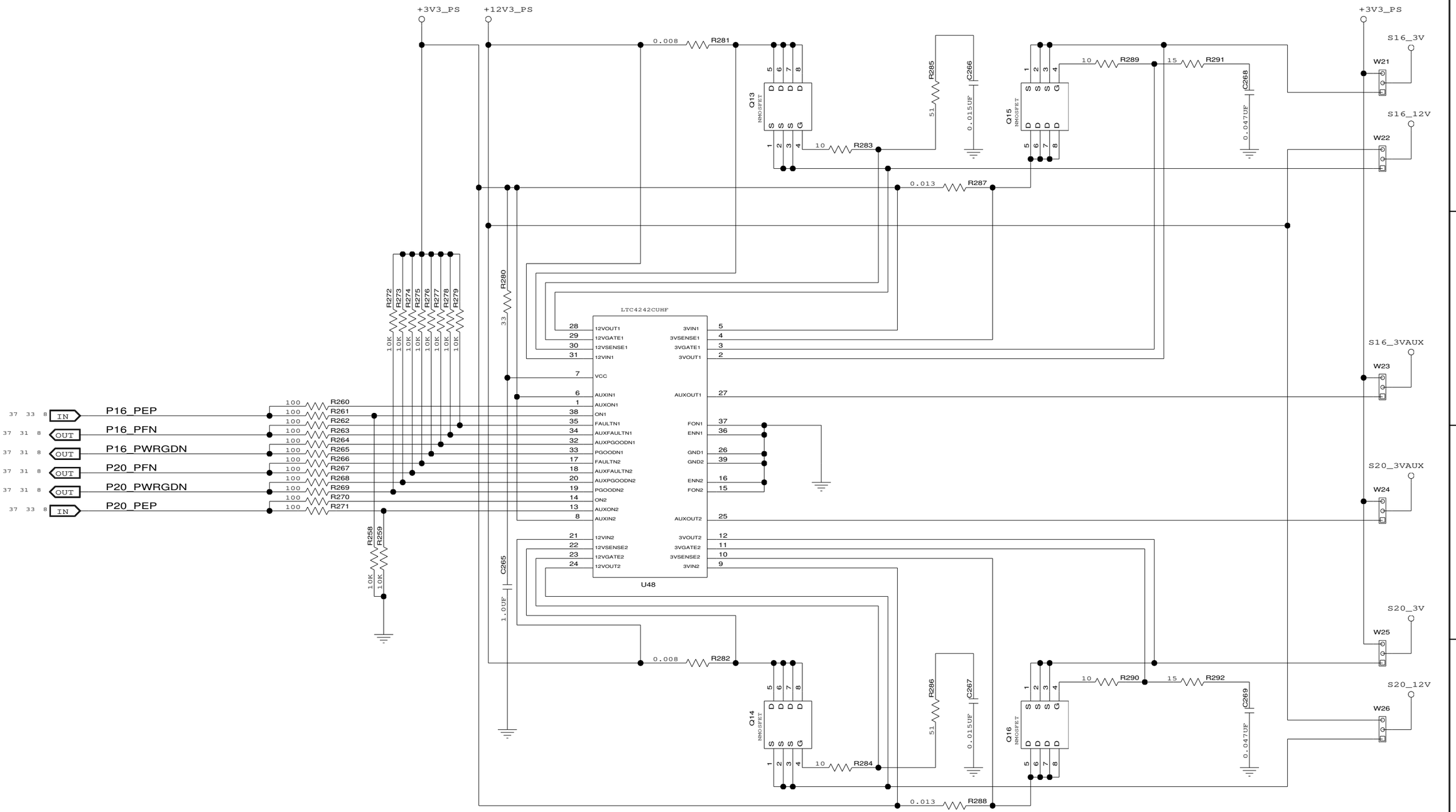
HOT PLUG CONTROL PORTS 8-12

SIZE	DRAWING NO.	FAB P/N	REV.
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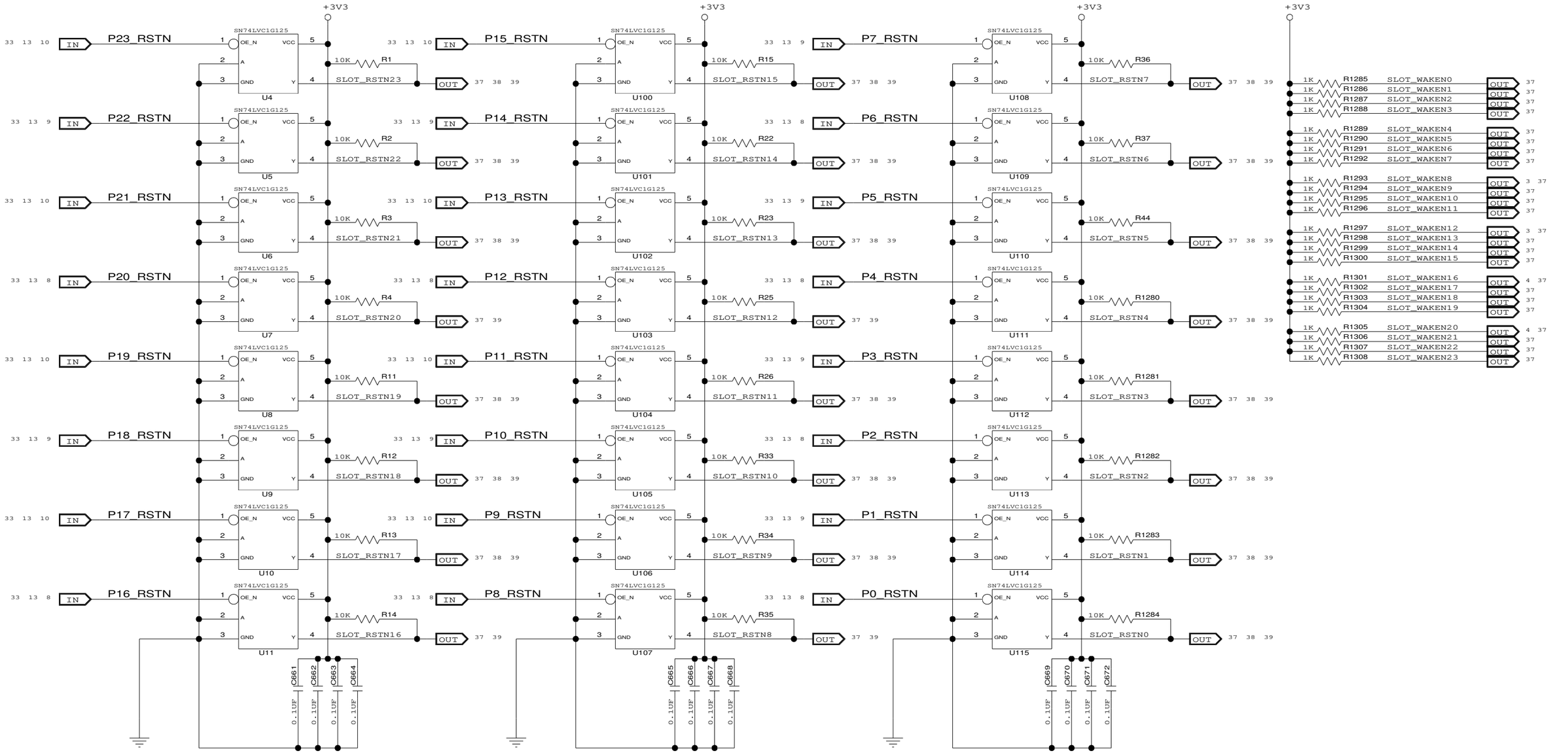
HOT PLUG CONTROL PORTS 16-20

SIZE	DRAWING NO.	FAB P/N	REV.
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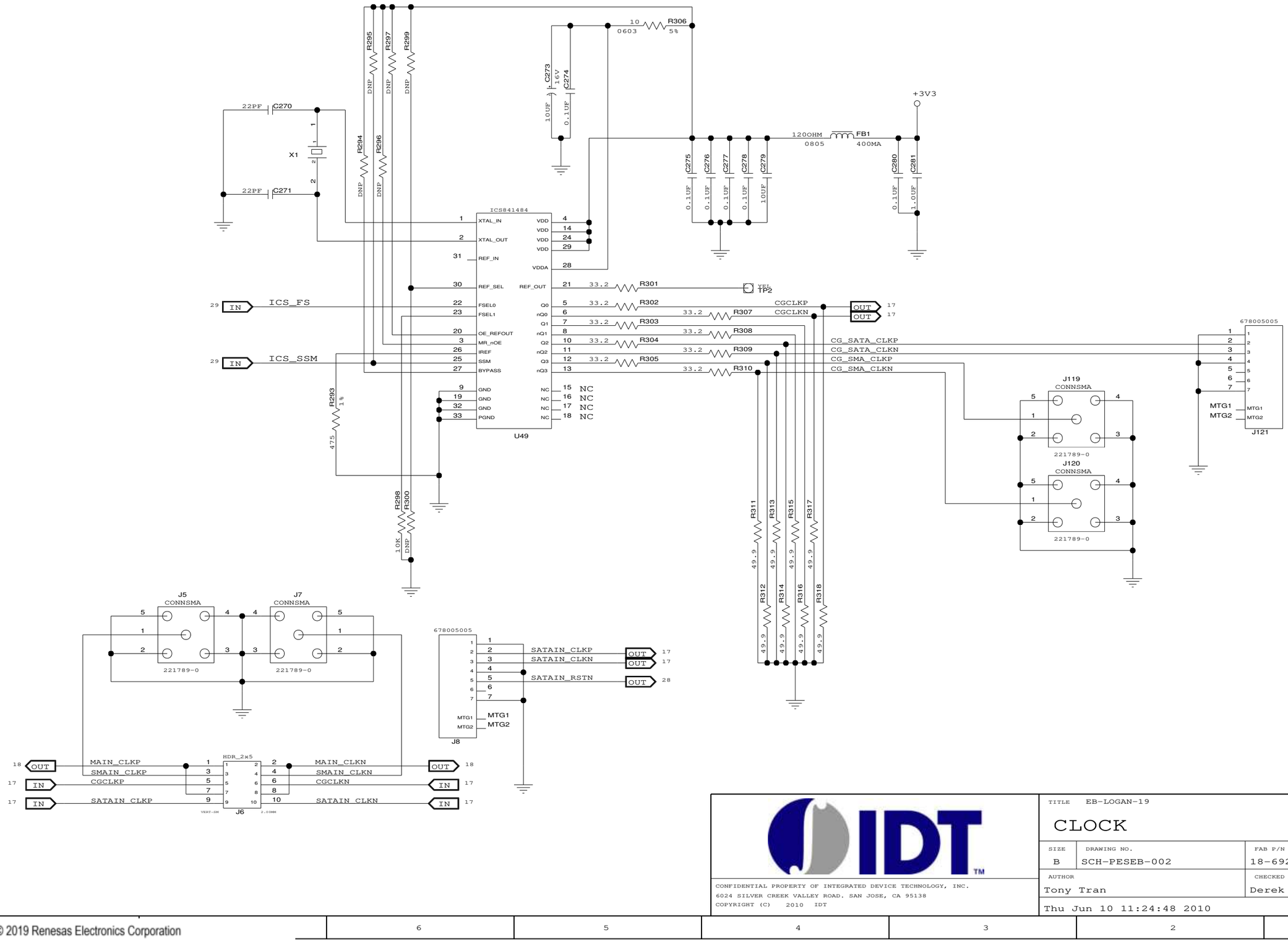
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TITLE: EB-LOGAN-19			
SLOT RESETS AND WAKE PULL-UPS			
SIZE: B	DRAWING NO.: SCH-PESEB-002	FAB P/N: 18-692-001	REV.: 2.0
AUTHOR: Tony Tran		CHECKED BY: Derek Huang	
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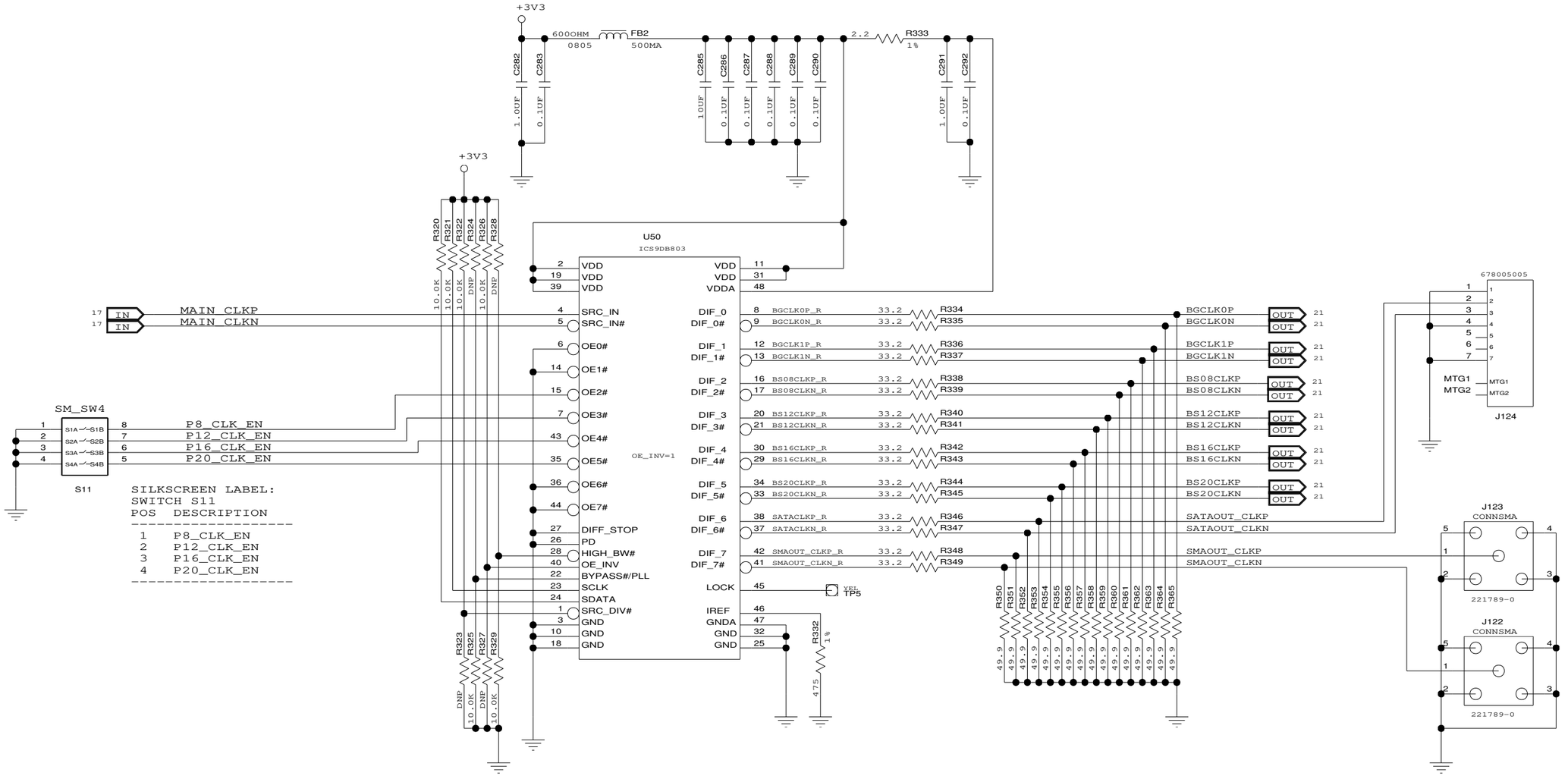
CLOCK

SIZE	DRAWING NO.	FAB P/N	REV.
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CLOCK BUFFER

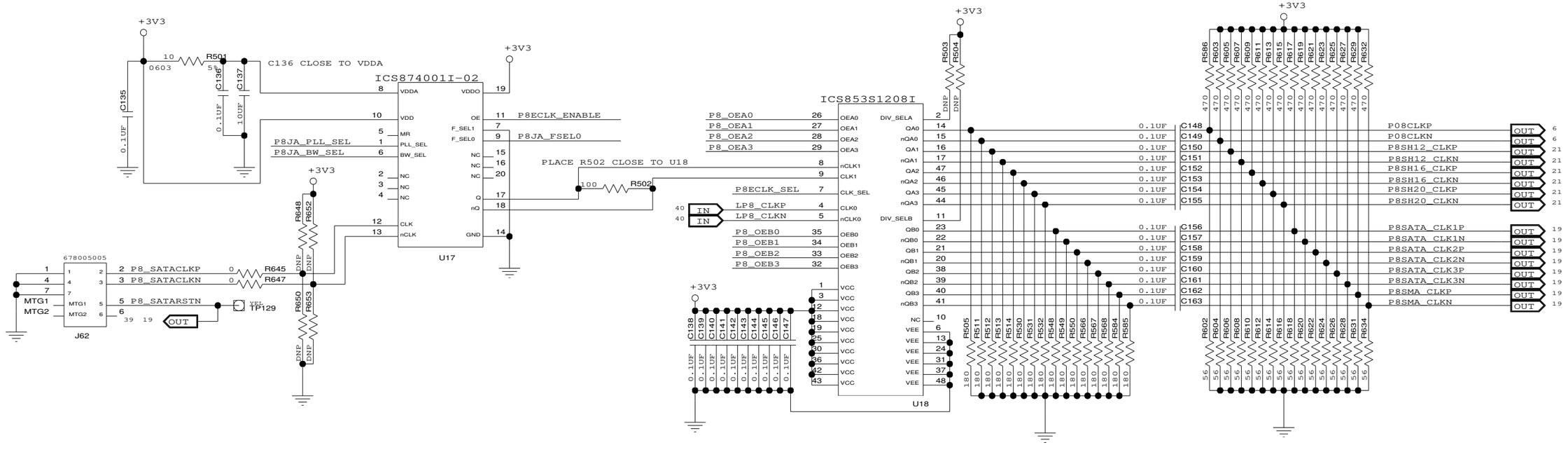
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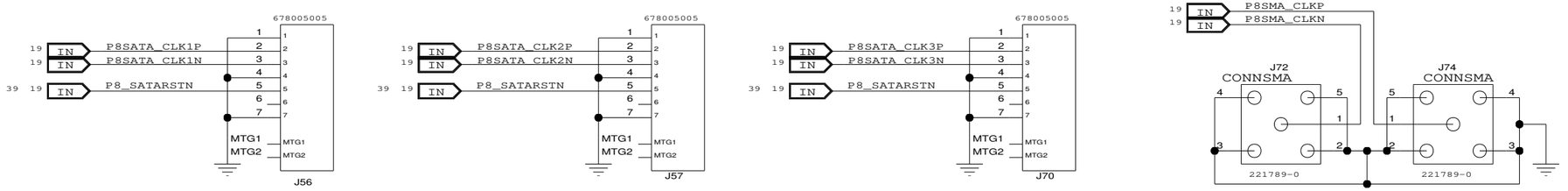
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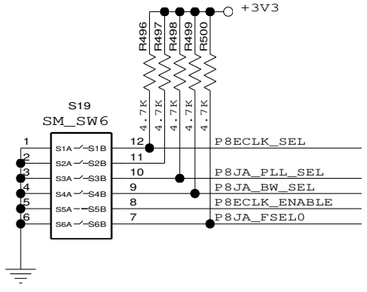
P08CLK – DUT PORT 8 CLK
LP8CLK – LOCAL CLOCK GEN. PORT 8 CLK
P8SHXXCLK – TO SLOT CLK HEADERS



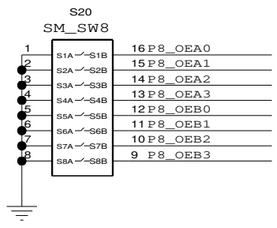


DEFAULT DIPSW SETTING

S19:1 OFF (SATACLK)
S19:3 OFF (PLL)
S19:4 OFF (2.2MHZ)
S19:5 OFF (U15 OUT ON)
S19:6 ON (100MHZ)



U18 OUTPUTS
OFF (ENABLE)
ON (DISABLE)



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CLOCK SELECTOR DUT PCLK 8

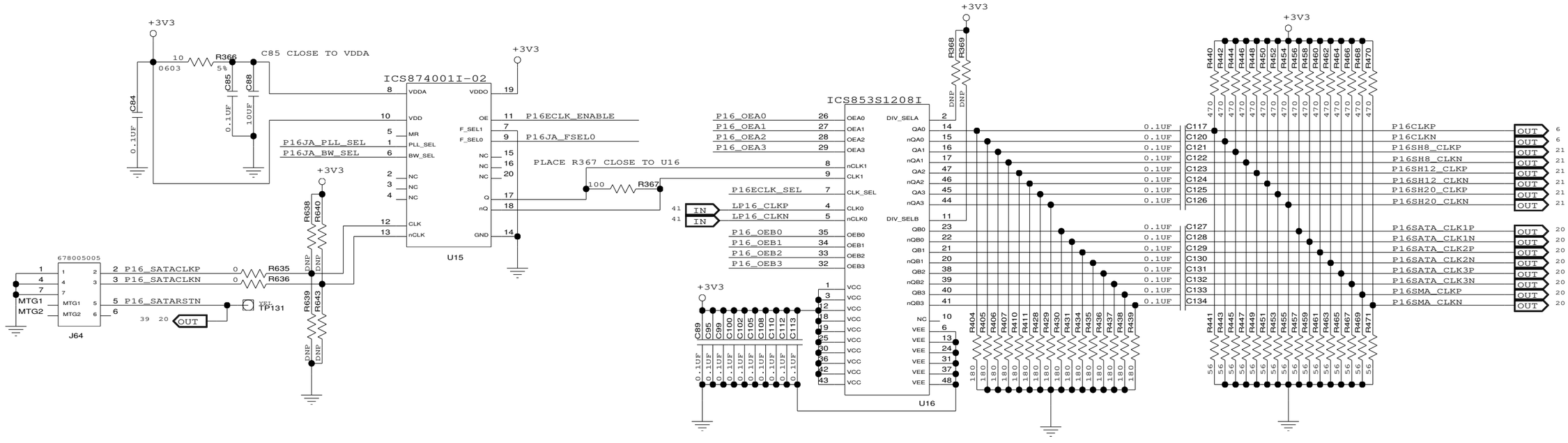
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0

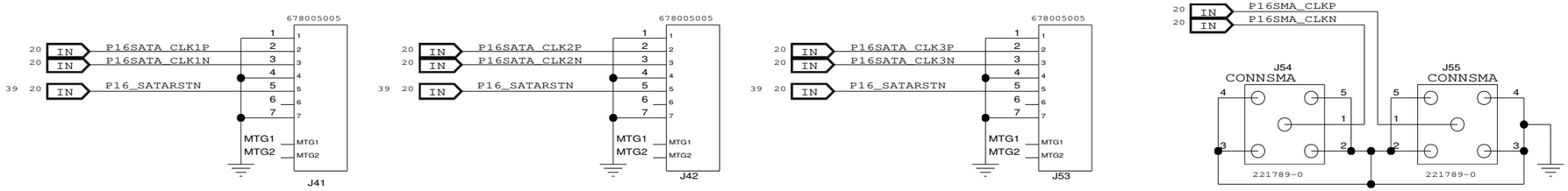
AUTHOR	CHECKED BY
Tony Tran	Derek Huang

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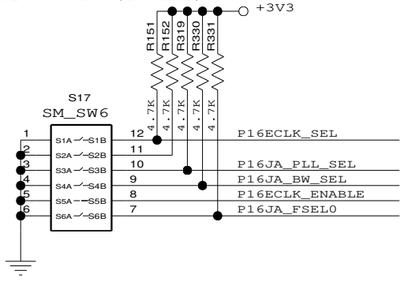
P16CLK – DUT PORT 16 CLK
LP16CLK – LOCAL CLOCK GEN. PORT 16 CLK
P16SHXXCLK – TO SLOT CLK HEADERS



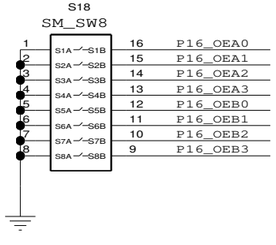


DEFAULT DIPSW SETTING

S17:1 OFF (SATACLK)
S17:3 OFF (PLL)
S17:4 OFF (2.2MHZ)
S17:5 OFF (U15 OUT ON)
S17:6 ON (100MHZ)



U16 OUTPUTS
OFF (ENABLE)
ON (DISABLE)



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TITLE EB-LOGAN-19

CLOCK SELECTOR DUT PCLK 16

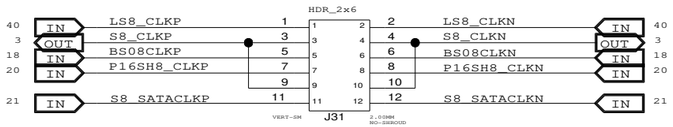
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0

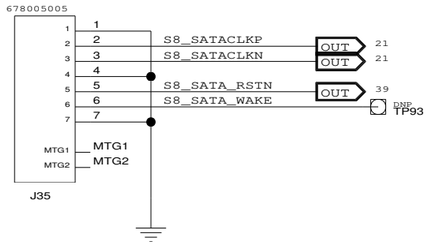
AUTHOR	CHECKED BY
Tony Tran	Derek Huang

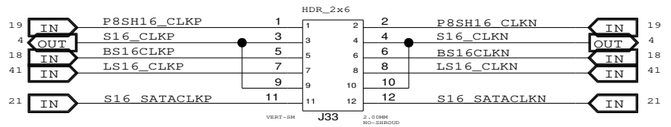
Thu Jun 10 11:28:19 2010 SHEET 20 OF 41

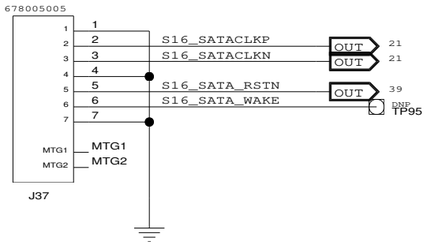
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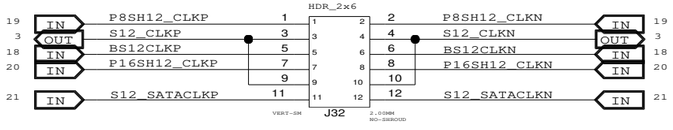
SXXCLK – SLOT CLK
BSXXLCK – BUFFER SLOT CLK
LSXXCLK – LOCAL CLOCK GEN. SLOT CLK
SHXXCLK – SLOT HDR.CLK

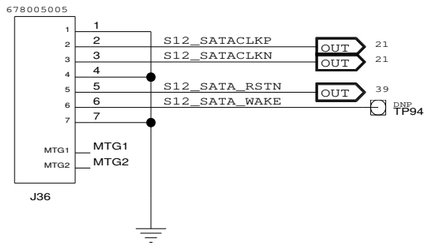


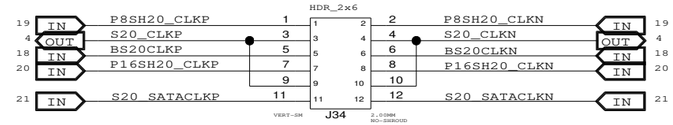


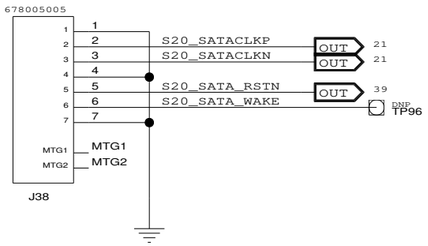


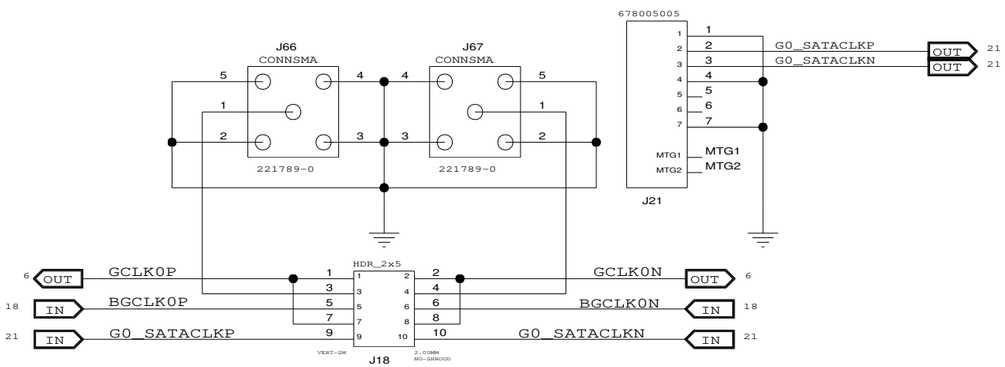


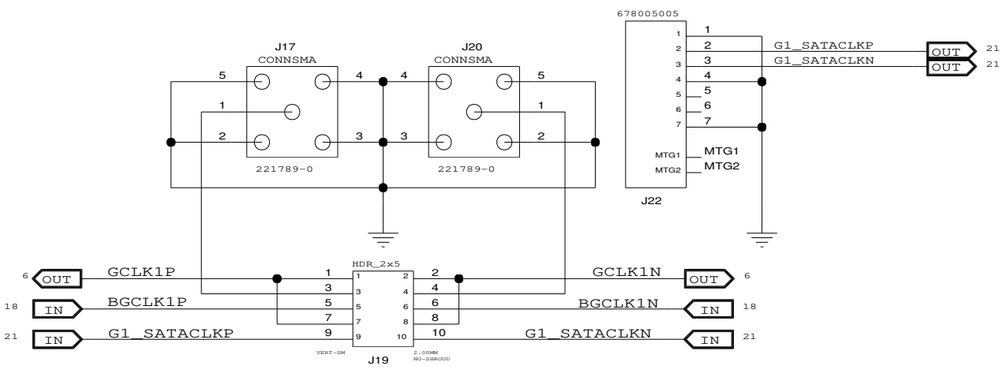












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TITLE EB-LOGAN-19

CLOCK SELECTOR SLOTS 8-20, GCLK

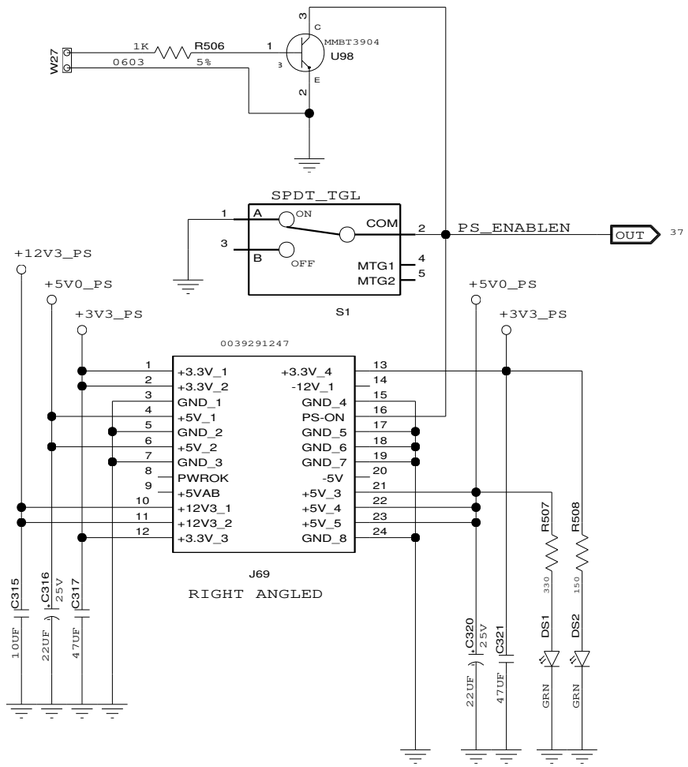
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0

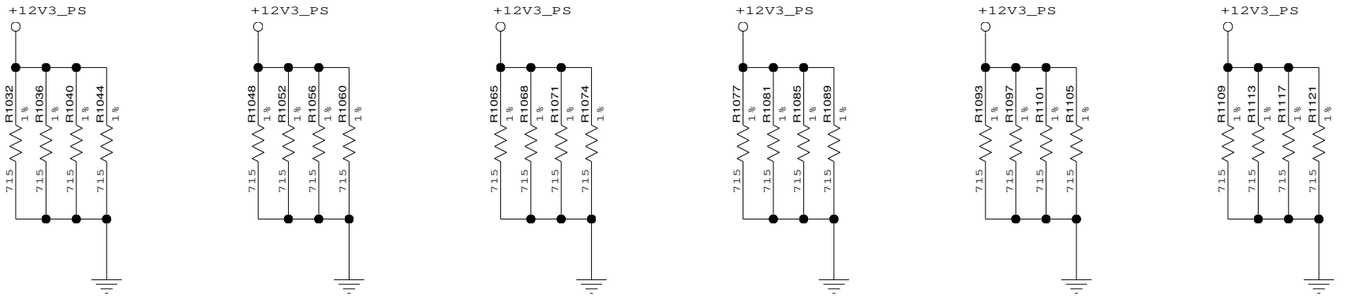
AUTHOR	CHECKED BY
Tony Tran	Derek Huang

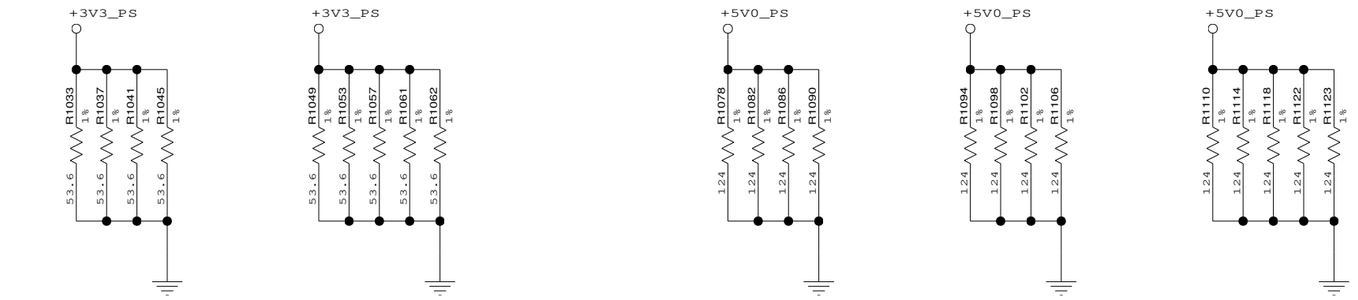
Thu Jun 10 11:24:49 2010 — SHEET 21 OF 41

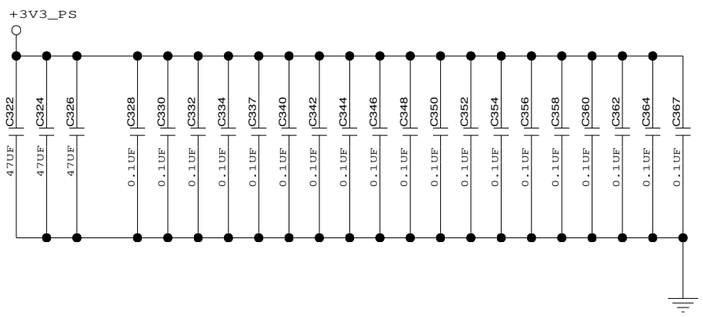
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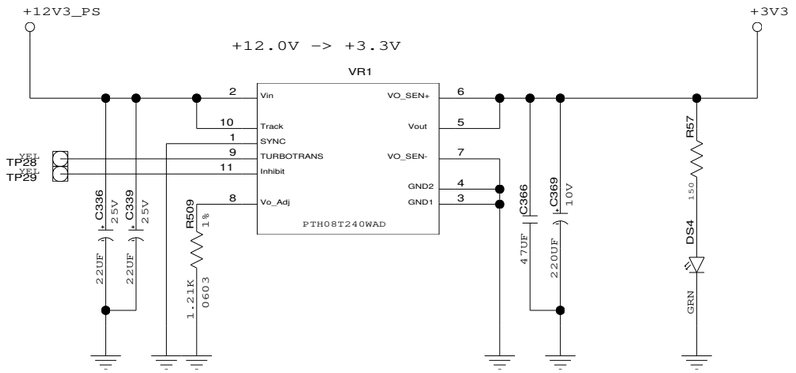
MINIMUM POWER SUPPLY LOADS



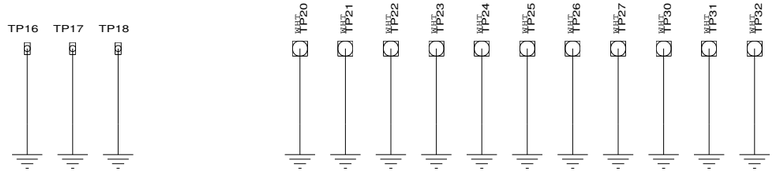








GND TEST POINTS
SCATTER AROUND BOARD



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TITLE	EB-LOGAN-19		
	POWER CONNECTORS, MIN LOAD RESISTORS		
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jun 10 11:24:50 2010		SHEET 22 OF 41	

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+12V3_PS

+3V3

LTM4603

C380 10UF, C381 10UF

R515 100K, R516 100K

A1 VIN1, A2 VIN2, A3 VIN3, A4 VIN4, A5 VIN5, A6 VIN6, B1 VIN7, B2 VIN8, B3 VIN9, B4 VIN10, B5 VIN11, B6 VIN12, C1 VIN13, C2 VIN14, C3 VIN15, C4 VIN16, C5 VIN17, C6 VIN18

A10 RUN

G12 PGOOD

A11 COMP — TP37 DNP

A7 INTVCC

E12 DRVCC

A8 PLLIN — TP38 DNP

K12 DIFFVOUT

L12 VOUT_LCL

A9 TRACK/SS

C12 MARG0

D12 MARG1

A12 MPGM

H12 SGND

D1 GND1, D2 GND2, D3 GND3, D4 GND4, D5 GND5, D6 GND6, E1 GND7, E2 GND8, E3 GND9, E4 GND10, E5 GND11, E6 GND12, E7 GND13, F1 GND14, F2 GND15, F3 GND16, F4 GND17, F5 GND18, F6 GND19, F7 GND20, F8 GND21, F9 GND22, G1 GND23, G2 GND24, G3 GND25

VFB F12

VOSNSP J12, VOSNSN M12

FSET B12

GND26 G4, GND27 G5, GND28 G6, GND29 G7, GND30 G8, GND31 G9, GND32 H1, GND33 H2, GND34 H3, GND35 H4, GND36 H5, GND37 H6, GND38 H7, GND39 H8, GND40 H9

VOUT1 J1, VOUT2 J2, VOUT3 J3, VOUT4 J4, VOUT5 J5, VOUT6 J6, VOUT7 J7, VOUT8 J8, VOUT9 J9, VOUT10 J10, VOUT11 K1, VOUT12 K2, VOUT13 K3, VOUT14 K4, VOUT15 K5, VOUT16 K6, VOUT17 K7, VOUT18 K8, VOUT19 K9, VOUT20 K10, VOUT21 K11, VOUT22 L1, VOUT23 L2, VOUT24 L3, VOUT25 L4, VOUT26 L5, VOUT27 L6, VOUT28 L7, VOUT29 L8, VOUT30 L9, VOUT31 L10, VOUT32 L11, VOUT33 M1, VOUT34 M2, VOUT35 M3, VOUT36 M4, VOUT37 M5, VOUT38 M6, VOUT39 M7, VOUT40 M8, VOUT41 M9, VOUT42 M10, VOUT43 M11

U56

+3V3

R1389 10K, R1390 10K

W33 0

PLACE W33 CLOSE TO J112

C384 100PF

C386 100UF 16V

C383 DNP

R523 18.2K, R524 51.1K, R525 191K

C385 0.01UF

MARG1	MARG0	MODE
LOW	LOW	NO MARGIN
LOW	HIGH	MARGIN UP
HIGH	LOW	MARGIN DOWN
HIGH	HIGH	NO MARGIN

S9 SM_SW6

1 S1A–S1B 12 PS_IO_MARG0
2 S2A–S2B 11 PS_IO_MARG1
3 S3A–S3B 10 PS_IO_CTRL3
4 S4A–S4B 9 PS_IO_CTRL2
5 S5A–S5B 8 PS_IO_CTRL1
6 S6A–S6B 7 PS_IO_CTRL0

MARGINING CONTROL

487K R517, 487K R518 — 8%
487K R519 — 4%
1.96M R520, 1.96M R521 — 2%
1.96M R522 — 1%

ROUTE AS POWER NET OR ISLAND

REG_2V5_VDDIO

C387 47UF, C388 47UF, C389 47UF, C390 47UF, C391 1.0UF

C392 1.0UF, C394 0.1UF

R58 150, DS101 GRN

26NH FB5 6.5A

PLACE CLOSE TO U1

C395 10UF, C396 1.0UF

+3V3_IO

VDD_IO, 3.3V

CONN BANANA RED J78 1

CONN BANANA BLK J79 1

0 R526, 0 R527

0 R528, 0 R529

PLACE R526 & R527 CLOSE TO U57, NOISE-FREE ROUTING
PLACE R528 & R529 CLOSE TO U1, NOISE-FREE ROUTING

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TITLE EB-LOGAN-19

POWER REGULATOR – VDDIO

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0

AUTHOR	CHECKED BY
Tony Tran	Derek Huang

Thu Jun 10 11:24:50 2010 SHEET 23 OF 41

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+12V3_PS

+3V3

LTM4603

A1	VIN1	VOUT1	J1
A2	VIN2	VOUT2	J2
A3	VIN3	VOUT3	J3
A4	VIN4	VOUT4	J4
A5	VIN5	VOUT5	J5
A6	VIN6	VOUT6	J6
B1	VIN7	VOUT7	J7
B2	VIN8	VOUT8	J8
B3	VIN9	VOUT9	J9
B4	VIN10	VOUT10	J10
B5	VIN11	VOUT11	K1
B6	VIN12	VOUT12	K2
C1	VIN13	VOUT13	K3
C2	VIN14	VOUT14	K4
C3	VIN15	VOUT15	K5
C4	VIN16	VOUT16	K6
C5	VIN17	VOUT17	K7
C6	VIN18	VOUT18	K8
A10	RUN	VOUT19	K9
G12	PGOOD	VOUT20	K10
A11	COMP	VOUT21	K11
A7	INTVCC	VOUT22	L1
E12	DRVCC	VOUT23	L2
A8	PLLIN	VOUT24	L3
K12	DIFFVOUT	VOUT25	L4
L12	VOUT_LCL	VOUT26	L5
A9	TRACK/SS	VOUT27	L6
C12	MARG0	VOUT28	L7
D12	MARG1	VOUT29	L8
A12	MPGM	VOUT30	L9
H12	SGND	VOUT31	L10
D1	GND1	VOUT32	L11
D2	GND2	VOUT33	M1
D3	GND3	VOUT34	M2
D4	GND4	VOUT35	M3
D5	GND5	VOUT36	M4
D6	GND6	VOUT37	M5
E1	GND7	VOUT38	M6
E2	GND8	VOUT39	M7
E3	GND9	VOUT40	M8
E4	GND10	VOUT41	M9
E5	GND11	VOUT42	M10
E6	GND12	VOUT43	M11
E7	GND13	VFB	F12
F1	GND14	VOSNSP	J12
F2	GND15	VOSNSN	M12
F3	GND16	FSET	B12
F4	GND17	GND26	G4
F5	GND18	GND27	G5
F6	GND19	GND28	G6
F7	GND20	GND29	G7
F8	GND21	GND30	G8
F9	GND22	GND31	G9
G1	GND23	GND32	H1
G2	GND24	GND33	H2
G3	GND25	GND34	H3
		GND35	H4
		GND36	H5
		GND37	H6
		GND38	H7
		GND39	H8
		GND40	H9

U59

C397 10UF, C398 10UF

R533 100K, R534 100K

+3V3

R1391 10K, R1392 10K

W34 0

TP41 DNP, TP42 DNP

PLACE W34 CLOSE TO J114

C400 DNP

C401 100PF

C403 100UF 16V

C402 0.01UF

R541 127K 1%, R542 316K 1%, R543 191K

MARG1	MARG0	MODE
LOW	LOW	NO MARGIN
LOW	HIGH	MARGIN UP
HIGH	LOW	MARGIN DOWN
HIGH	HIGH	NO MARGIN

S6
SM_SW6

1	S1A–S1B	12	PS_CORE_MARG0
2	S2A–S2B	11	PS_CORE_MARG1
3	S3A–S3B	10	PS_CORE_CTRL3
4	S4A–S4B	9	PS_CORE_CTRL2
5	S5A–S5B	8	PS_CORE_CTRL1
6	S6A–S6B	7	PS_CORE_CTRL0

487K R535, 487K R536 — 8%
487K R537 — 4%
1.96M R538, 1.96M R539 — 2%
1.96M R540 — 1%

MARGINING CONTROL

VDD_CORE, 1.0V

+3V3

330 R70 GRN DS117

MMBT3904 U3

CONN BANANA RED J114

CONN BANANA BLK J113

ROUTE AS POWER NET OR ISLAND

REG_1V0_CORE

C404 47UF, C405 47UF, C406 47UF, C407 47UF, C408 1.0UF

C409 1.0UF, C411 0.1UF

26NH FB6 6.5A

PLACE CLOSE TO U1

+1V0_CORE

C412 10UF, C413 1.0UF

0 R544, 0 R545

0 R546, 0 R547

PLACE R544 & R545 CLOSE TO U57, NOISE-FREE ROUTING
PLACE R546 & R547 CLOSE TO U1, NOISE-FREE ROUTING

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TITLE EB-LOGAN-19

POWER REGULATOR – VDDCORE

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0

AUTHOR	CHECKED BY
Tony Tran	Derek Huang

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+12V3_PS

+3V3

LTM4603

C414 10UF C415 10UF

R551 100K R552 100K

A1 VIN1 A2 VIN2 A3 VIN3 A4 VIN4 A5 VIN5 A6 VIN6 B1 VIN7 B2 VIN8 B3 VIN9 B4 VIN10 B5 VIN11 B6 VIN12 C1 VIN13 C2 VIN14 C3 VIN15 C4 VIN16 C5 VIN17 C6 VIN18

A10 RUN

G12 PGOOD

A11 COMP — DNP TP45

A7 INTVCC

E12 DRVCC

A8 PLLIN — DNP TP46

K12 DIFFVOUT

L12 VOUT_LCL

A9 TRACK/SS

C12 MARG0

D12 MARG1

A12 MPGM

H12 SGND

D1 GND1 D2 GND2 D3 GND3 D4 GND4 D5 GND5 D6 GND6 E1 GND7 E2 GND8 E3 GND9 E4 GND10 E5 GND11 E6 GND12 E7 GND13 F1 GND14 F2 GND15 F3 GND16 F4 GND17 F5 GND18 F6 GND19 F7 GND20 F8 GND21 F9 GND22 G1 GND23 G2 GND24 G3 GND25

VOUT1 J1 VOUT2 J2 VOUT3 J3 VOUT4 J4 VOUT5 J5 VOUT6 J6 VOUT7 J7 VOUT8 J8 VOUT9 J9 VOUT10 J10 VOUT11 K1 VOUT12 K2 VOUT13 K3 VOUT14 K4 VOUT15 K5 VOUT16 K6 VOUT17 K7 VOUT18 K8 VOUT19 K9 VOUT20 K10 VOUT21 K11 VOUT22 L1 VOUT23 L2 VOUT24 L3 VOUT25 L4 VOUT26 L5 VOUT27 L6 VOUT28 L7 VOUT29 L8 VOUT30 L9 VOUT31 L10 VOUT32 L11 VOUT33 M1 VOUT34 M2 VOUT35 M3 VOUT36 M4 VOUT37 M5 VOUT38 M6 VOUT39 M7 VOUT40 M8 VOUT41 M9 VOUT42 M10 VOUT43 M11

VFB F12

VOSNSP J12

VOSNSN M12

FSET B12

GND26 G4 GND27 G5 GND28 G6 GND29 G7 GND30 G8 GND31 G9 GND32 H1 GND33 H2 GND34 H3 GND35 H4 GND36 H5 GND37 H6 GND38 H7 GND39 H8 GND40 H9

U62

C417 DNP

C418 100PF

C420 100UF 16V

R559 127K 1% R560 316K 1% R561 191K

C419 0.01UF

+3V3

R1393 10K R1394 10K

W35

PLACE W35 CLOSE TO J115

MARG1	MARG0	MODE
LOW	LOW	NO MARGIN
LOW	HIGH	MARGIN UP
HIGH	LOW	MARGIN DOWN
HIGH	HIGH	NO MARGIN

S7
SM_SW6

1 S1A 12 S1B PS_PEA_MARG0
2 S2A 11 S2B PS_PEA_MARG1
3 S3A 10 S3B PS_PEA_CTRL3
4 S4A 9 S4B PS_PEA_CTRL2
5 S5A 8 S5B PS_PEA_CTRL1
6 S6A 7 S6B PS_PEA_CTRL0

487K R553 487K R554 8%
487K R555 4%
1.96M R556 1.96M R557 2%
1.96M R558 1%

MARGINING CONTROL

+3V3

330 R81 GRN DS133

MMBT3904 U12

CONN BANANA RED J115

VDD_PEA, 1.0V

ROUTE AS POWER NET OR ISLAND

REG_1V0_PEA

C421 47UF C422 47UF C423 47UF C424 47UF C425 1.0UF

C426 1.0UF C428 0.1UF

26NH FB7 6.5A

PLACE CLOSE TO U1

+1V0_PEA

C429 10UF C430 1.0UF

0 R562 0 R563 0 R564 0 R565

PLACE R562 & R563 CLOSE TO U60, NOISE-FREE ROUTING
PLACE R564 & R565 CLOSE TO U1, NOISE-FREE ROUTING

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TITLE EB-LOGAN-19

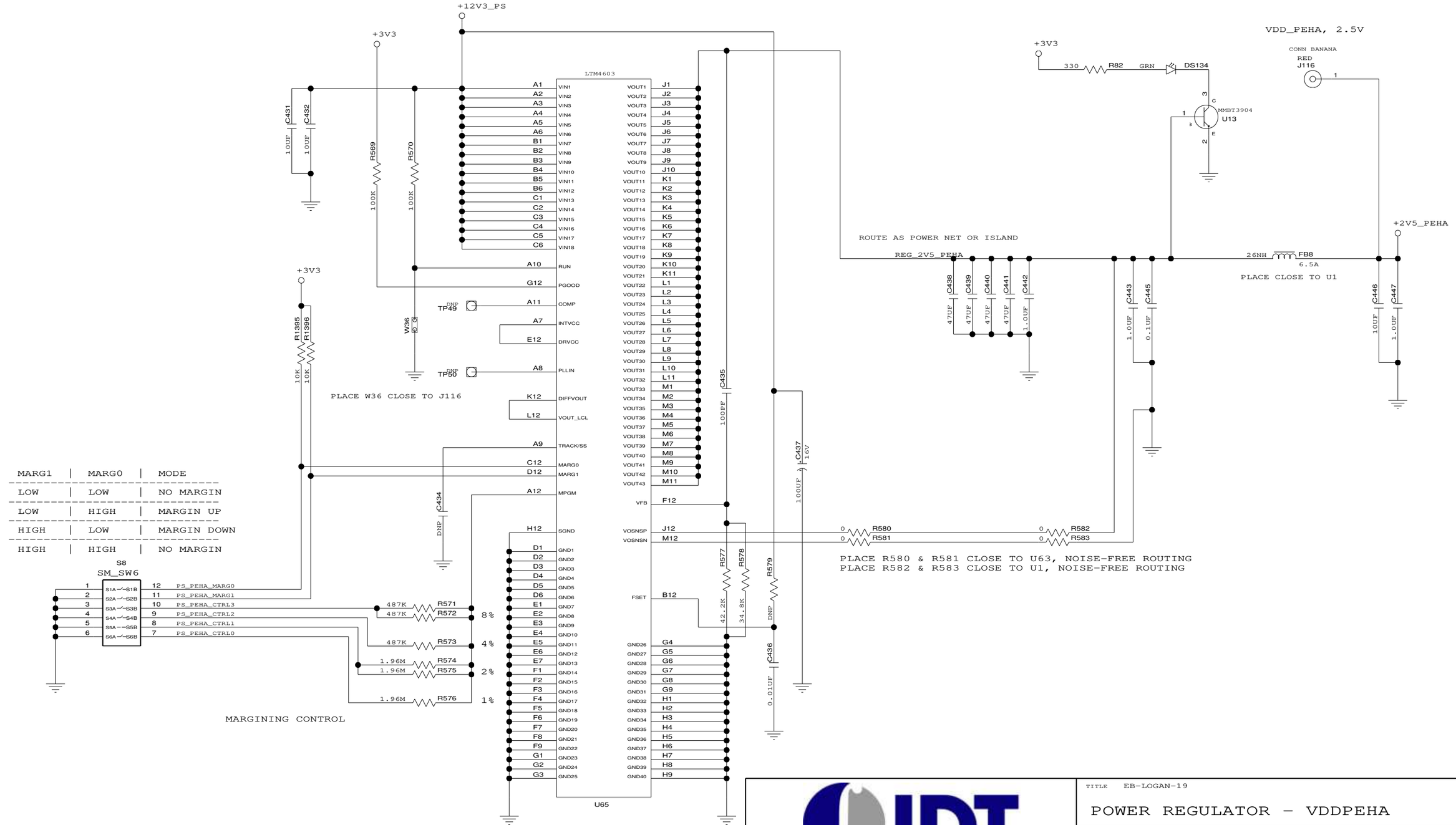
POWER REGULATOR – VDDPEA

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0

AUTHOR	CHECKED BY
Tony Tran	Derek Huang

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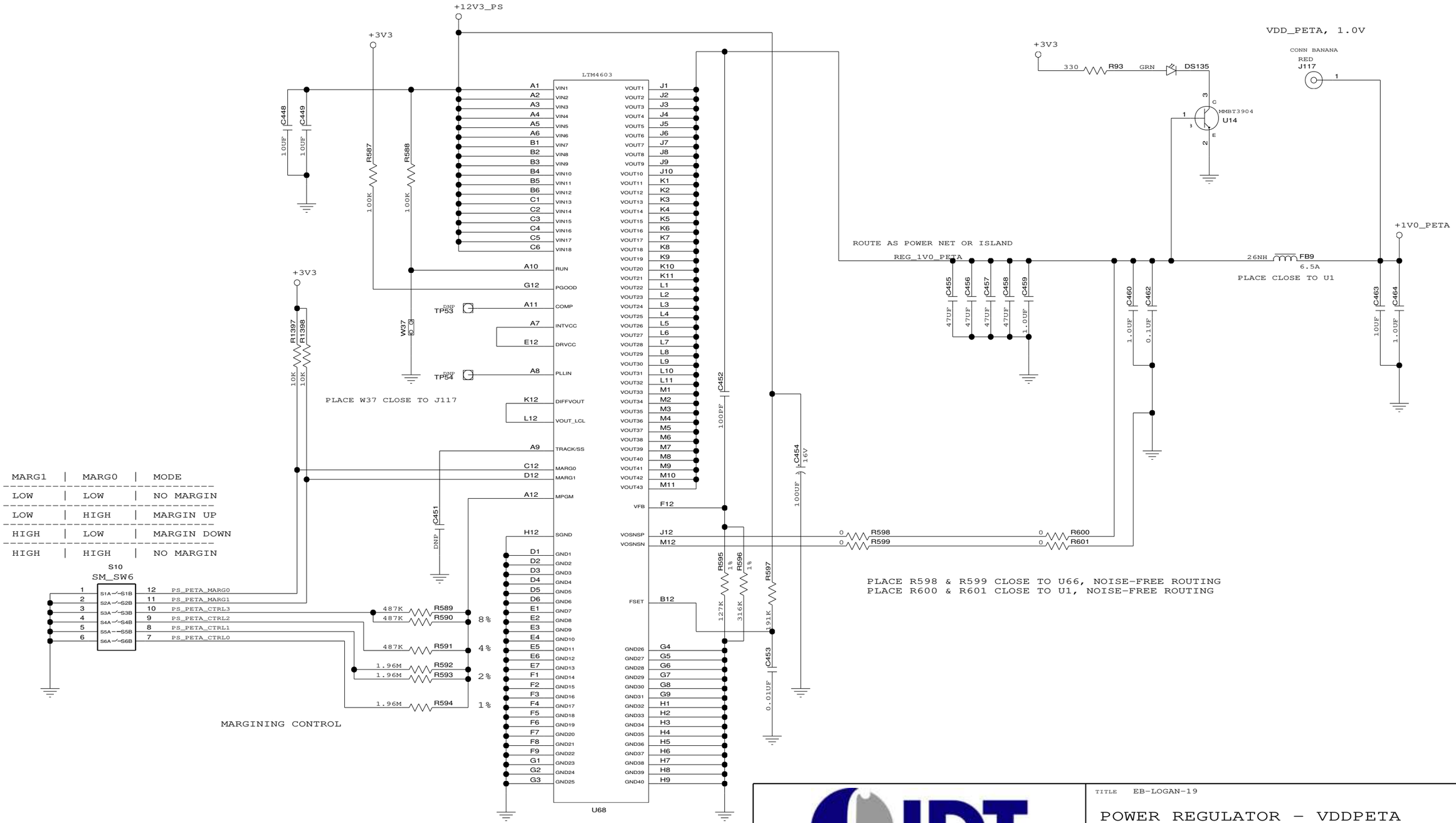
POWER REGULATOR – VDDPEHA

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0

AUTHOR	CHECKED BY
Tony Tran	Derek Huang

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TITLE EB-LOGAN-19

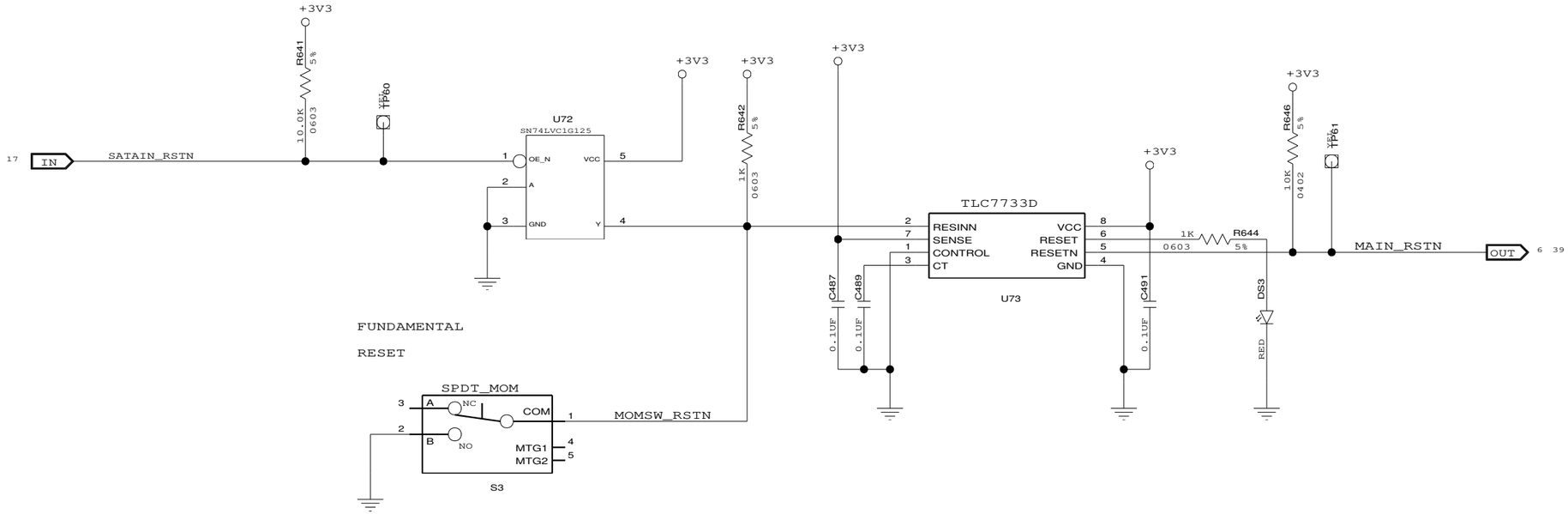
POWER REGULATOR – VDDPETA

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0

AUTHOR	CHECKED BY
Tony Tran	Derek Huang

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RESET, SMBUS, EEPROM, JTAG

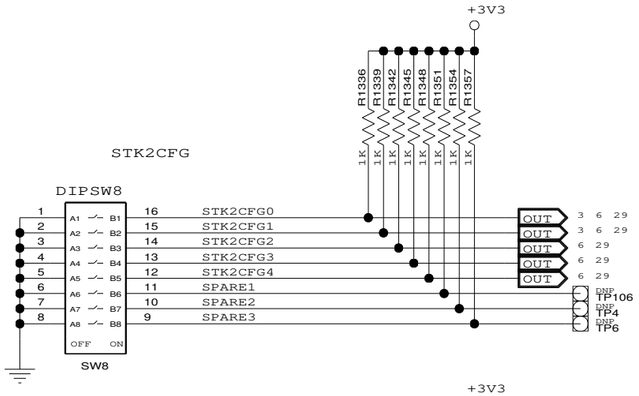
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0

AUTHOR	CHECKED BY
Tony Tran	Derek Huang

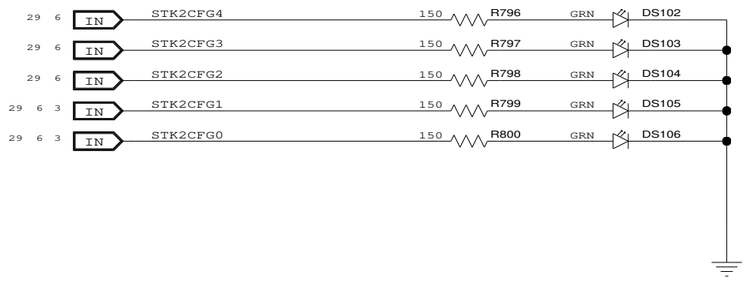
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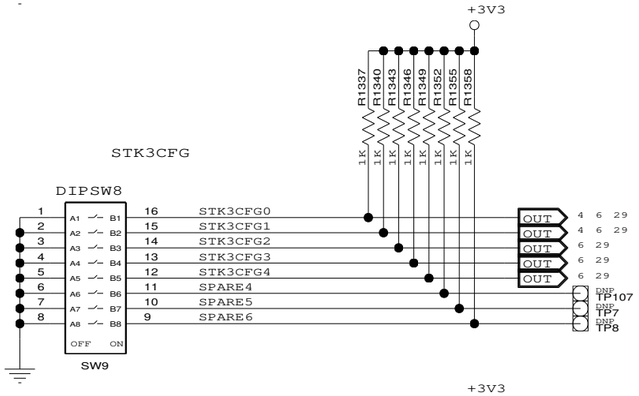
STK2CFG



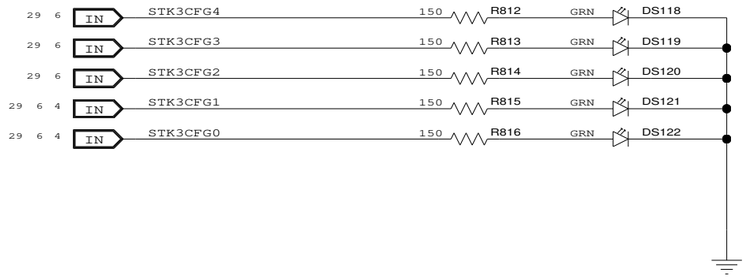
(GREEN) ACTIVE HIGH – DIP STK2CFG



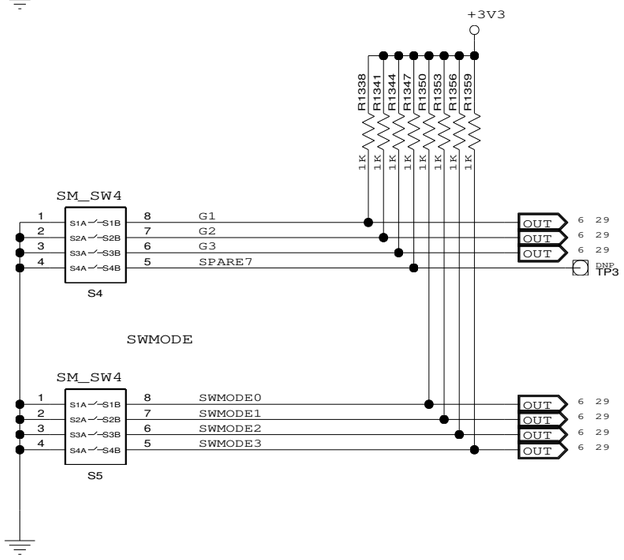
STK3CFG



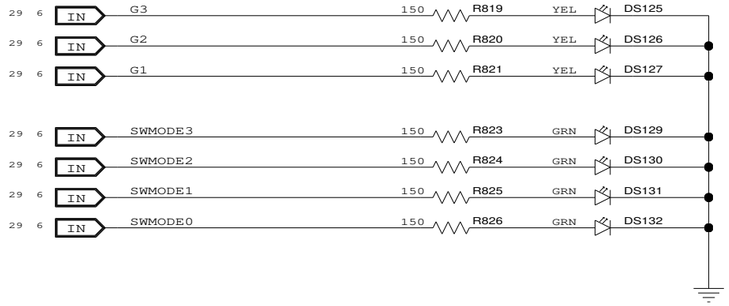
(GREEN) ACTIVE HIGH – DIP STK3CFG

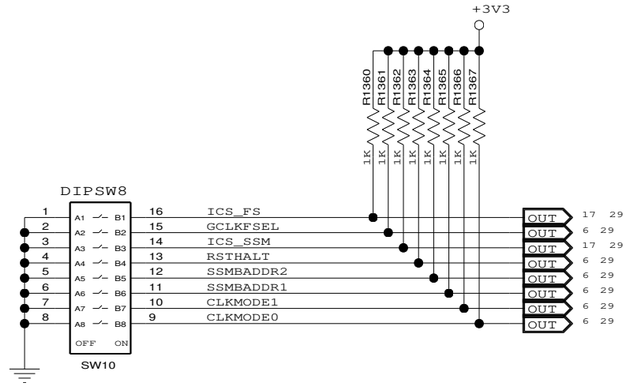


SWMODE

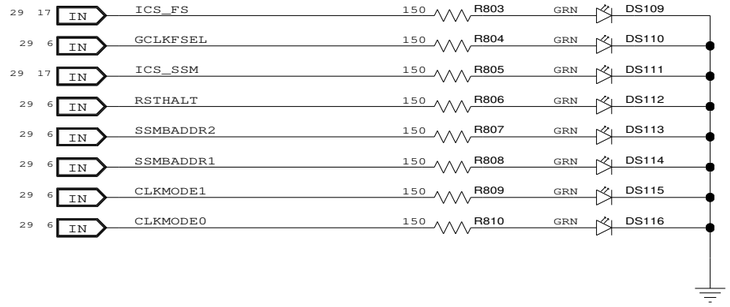


(GREEN) ACTIVE HIGH – DIP MODE





(GREEN) ACTIVE HIGH – DIP CLOCK



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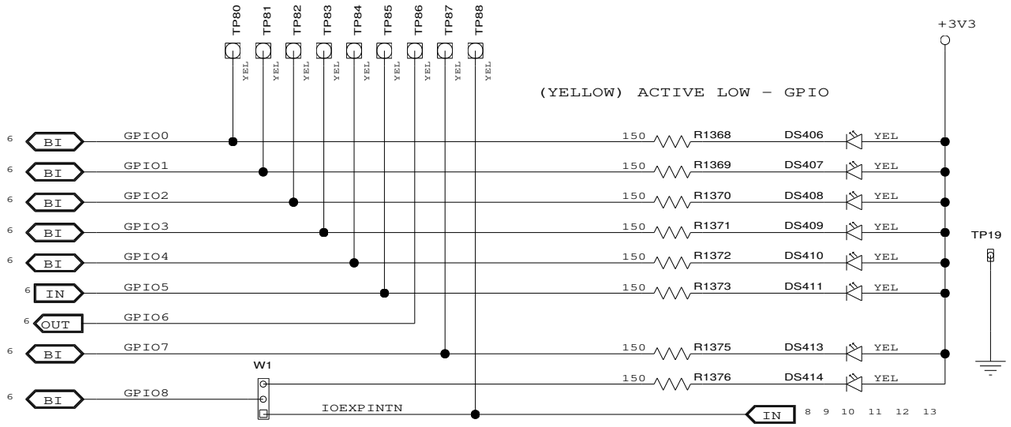
DIP SWITCHES

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0

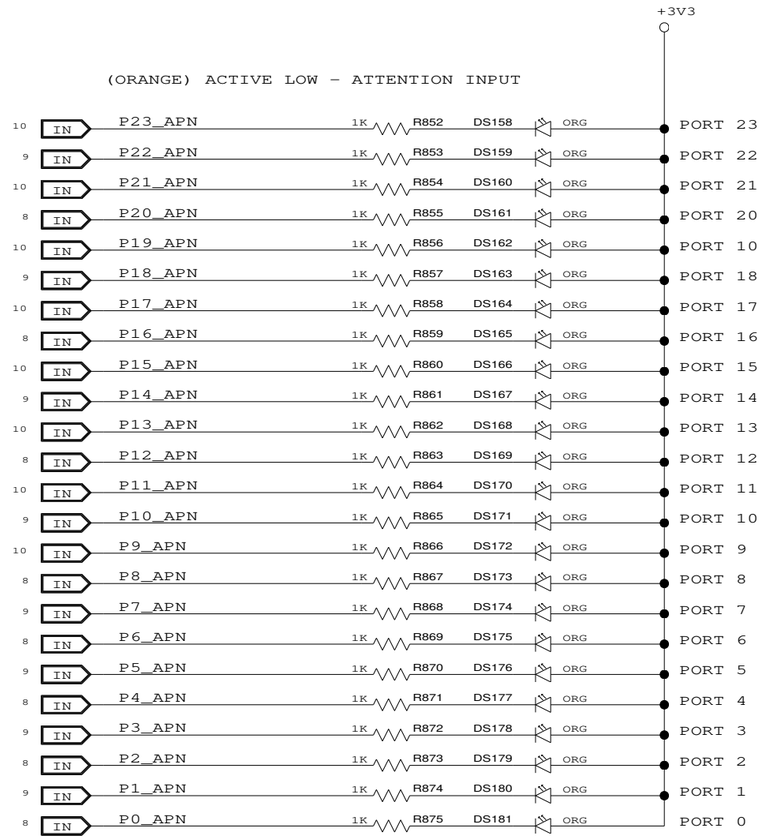
AUTHOR	CHECKED BY
Tony Tran	Derek Huang

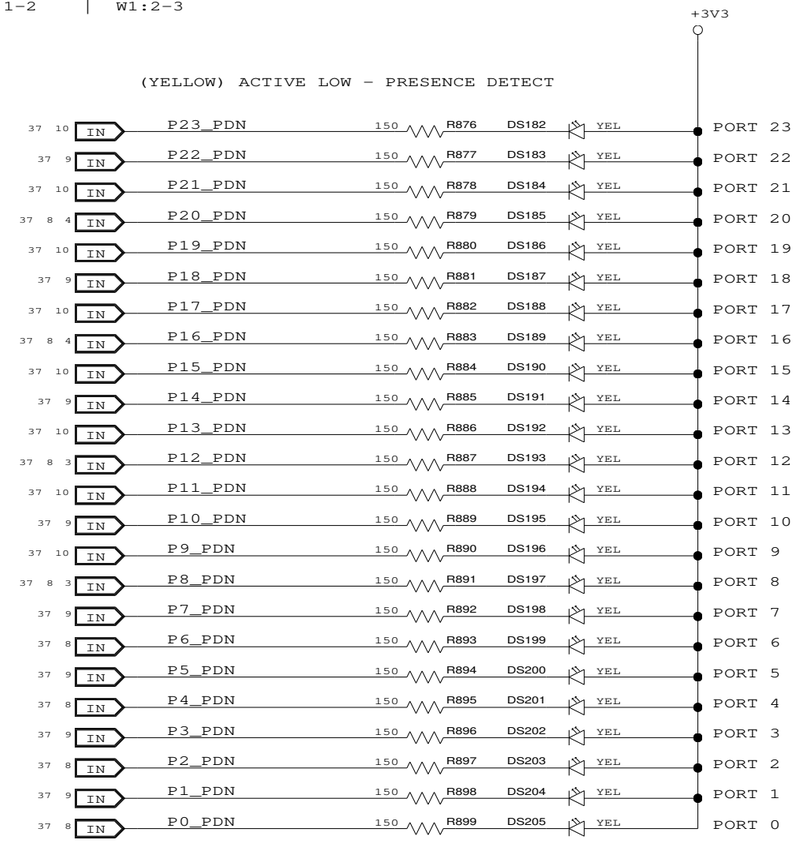
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GPIO	ALT0	ALT1
0	PART0PERSTN	P16LINKUPN
1	PART1PERSTN	P16ACTIVEN
2	PART2PERSTN	P4LINKUPN
3	PART3PERSTN	P4ACTIVEN
4	FAILOVER0	P0LINKUPN
5	GPEN	P0ACTIVEN
6	FAILOVER1	FAILOVER3
7	FAILOVER2	P8LINKUPN
8	IOEXPINTN W1:1–2	P8ACTIVEN W1:2–3





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TITLE EB-LOGAN-19

LED – PORT STATUS (1 OF 7)

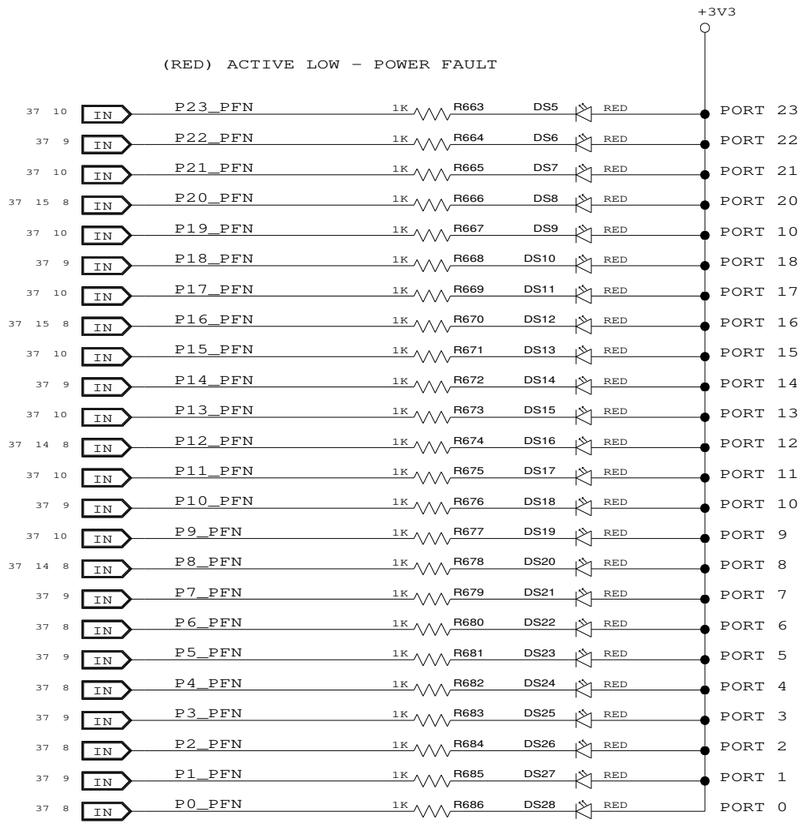
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0

AUTHOR	CHECKED BY
Tony Tran	Derek Huang

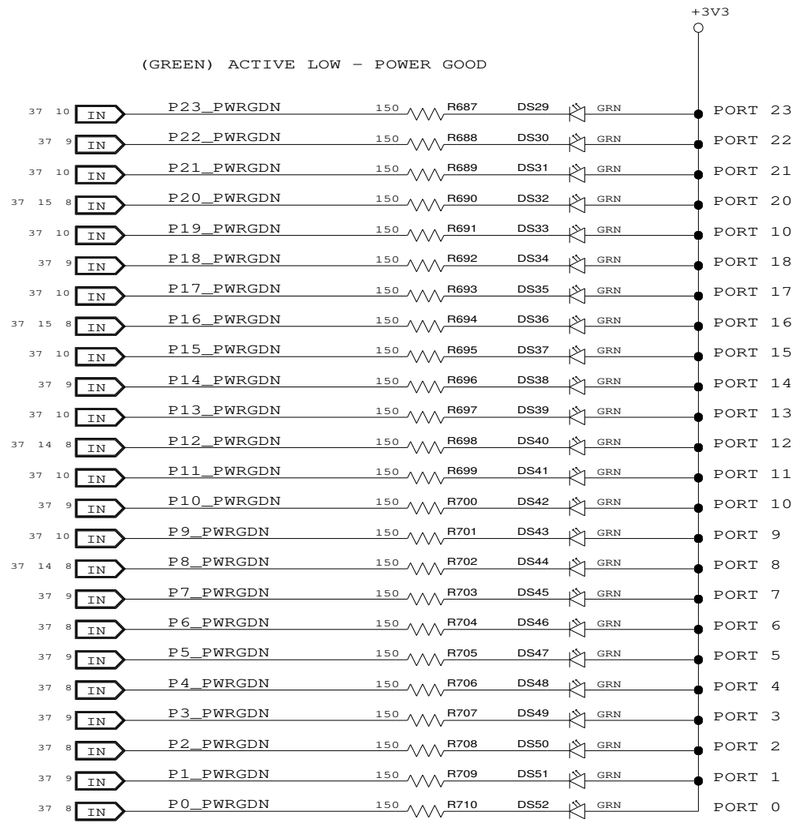
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(RED) ACTIVE LOW – POWER FAULT



(GREEN) ACTIVE LOW – POWER GOOD



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LED – PORT STATUS (2 OF 7)

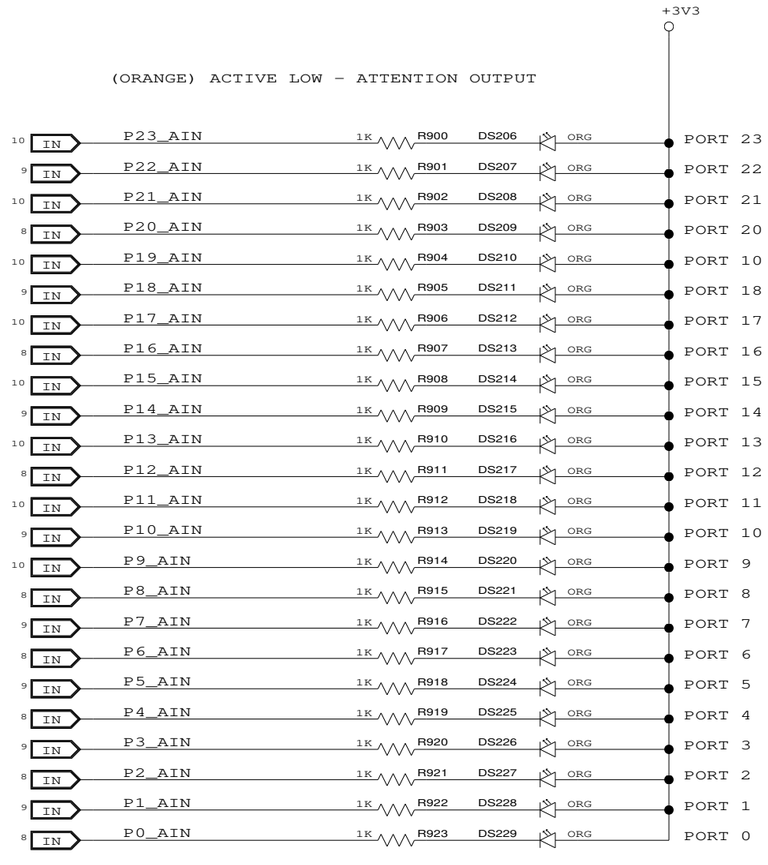
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0

AUTHOR	CHECKED BY
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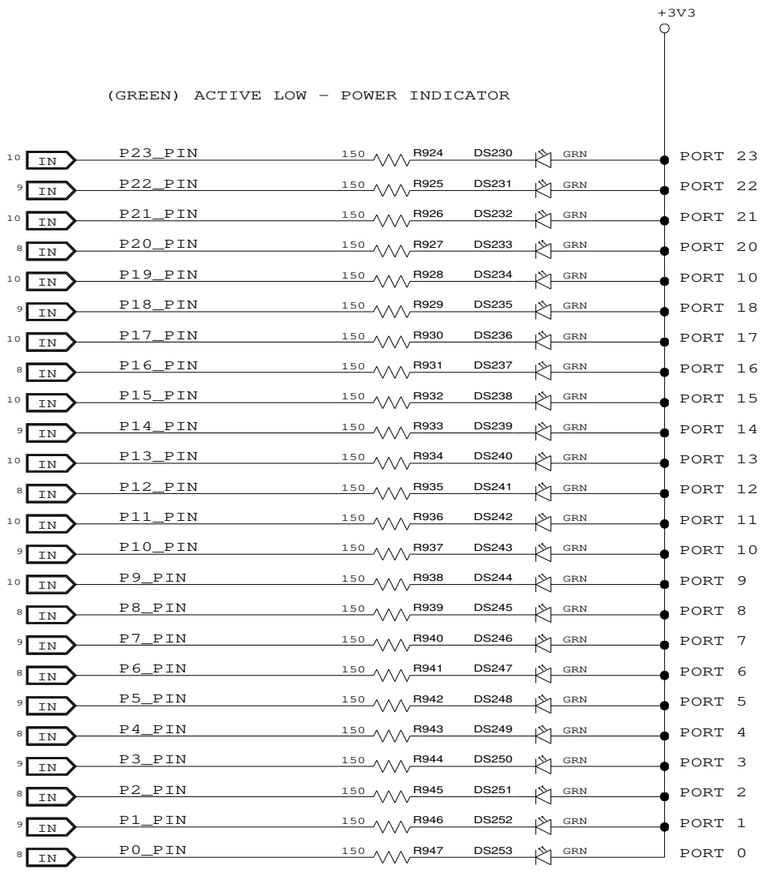
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(ORANGE) ACTIVE LOW – ATTENTION OUTPUT



(GREEN) ACTIVE LOW – POWER INDICATOR



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LED – PORT STATUS (3 OF 7)

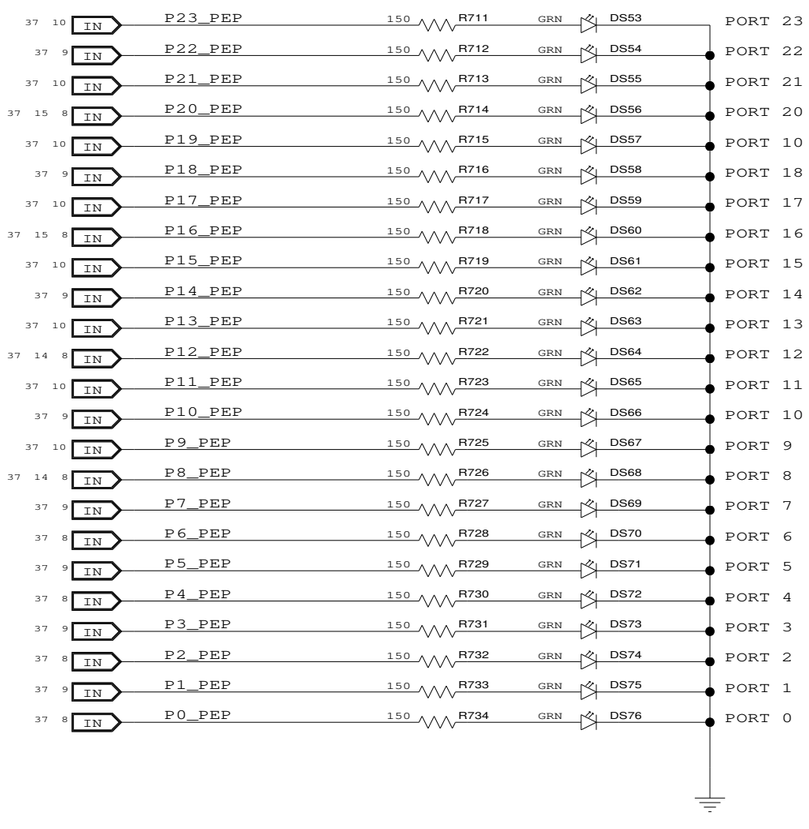
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0

AUTHOR	CHECKED BY
Tony Tran	Derek Huang

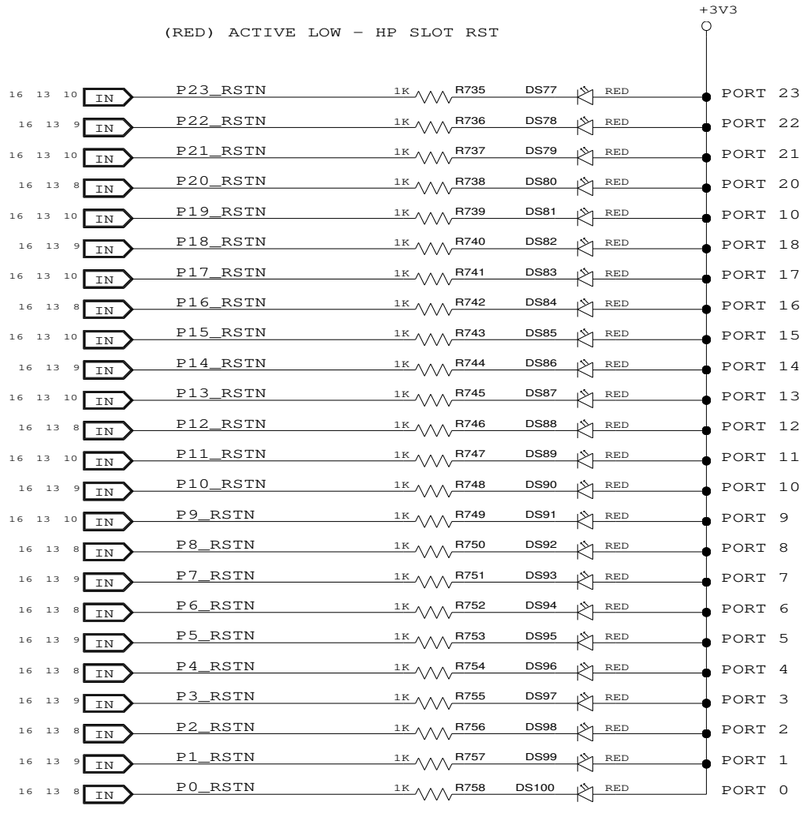
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(GREEN) ACTIVE HIGH – POWER ENABLE



(RED) ACTIVE LOW – HP SLOT RST



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LED – PORT STATUS (4 OF 7)

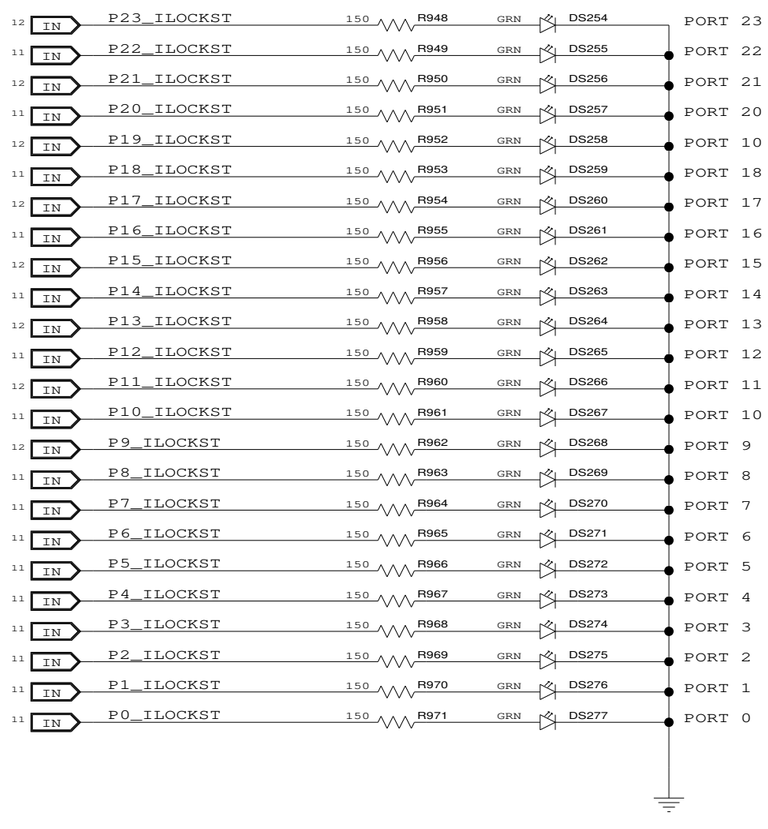
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AUTHOR	CHECKED BY
Tony Tran	Derek Huang

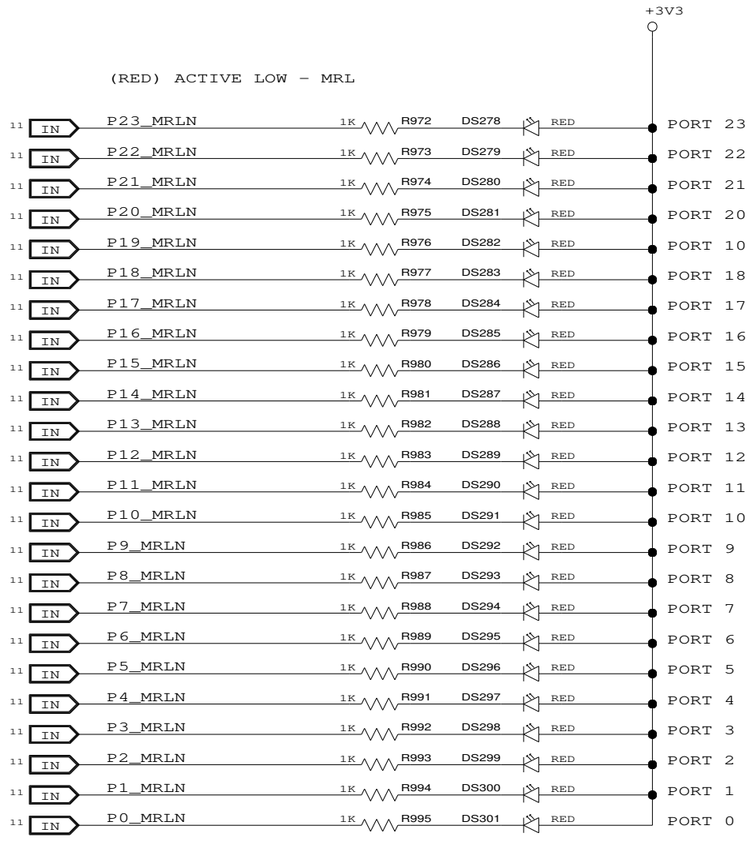
Thu Jun 10 11:24:54 2010 SHEET 33 OF 41

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(GREEN) ACTIVE HIGH – INTERLOCK INPUT



(RED) ACTIVE LOW – MRL



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LED – PORT STATUS (5 OF 7)

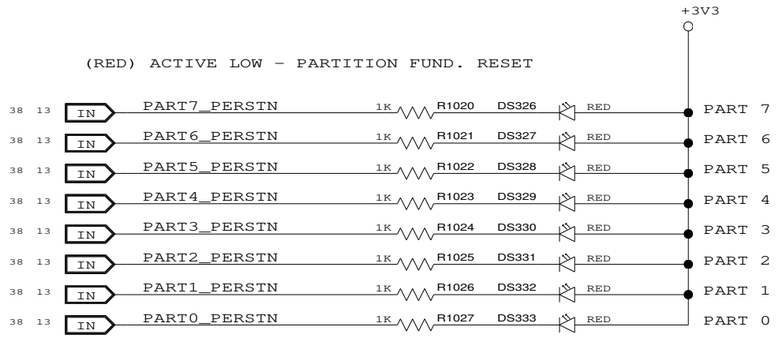
SIZE	DRAWING NO.	FAB P/N	REV.
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AUTHOR	CHECKED BY
Tony Tran	Derek Huang

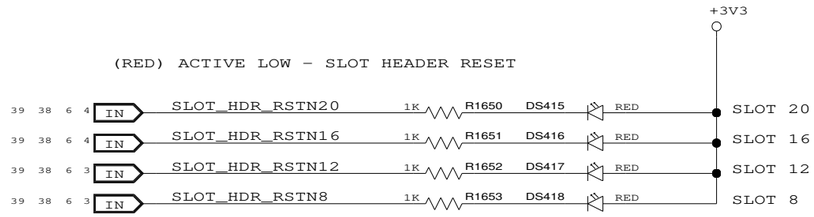
Thu Jun 10 11:24:54 2010 SHEET 34 OF 41

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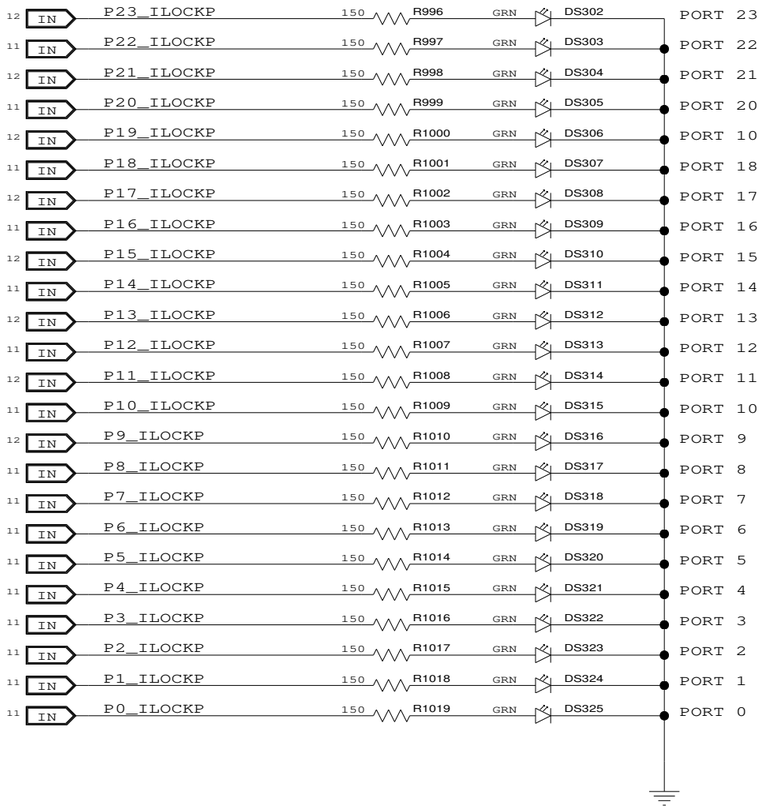
(RED) ACTIVE LOW – PARTITION FUND. RESET



(RED) ACTIVE LOW – SLOT HEADER RESET



(GREEN) ACTIVE HIGH – INTERLOCK OUTPUT



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LED – PORT STATUS (6 OF 7)

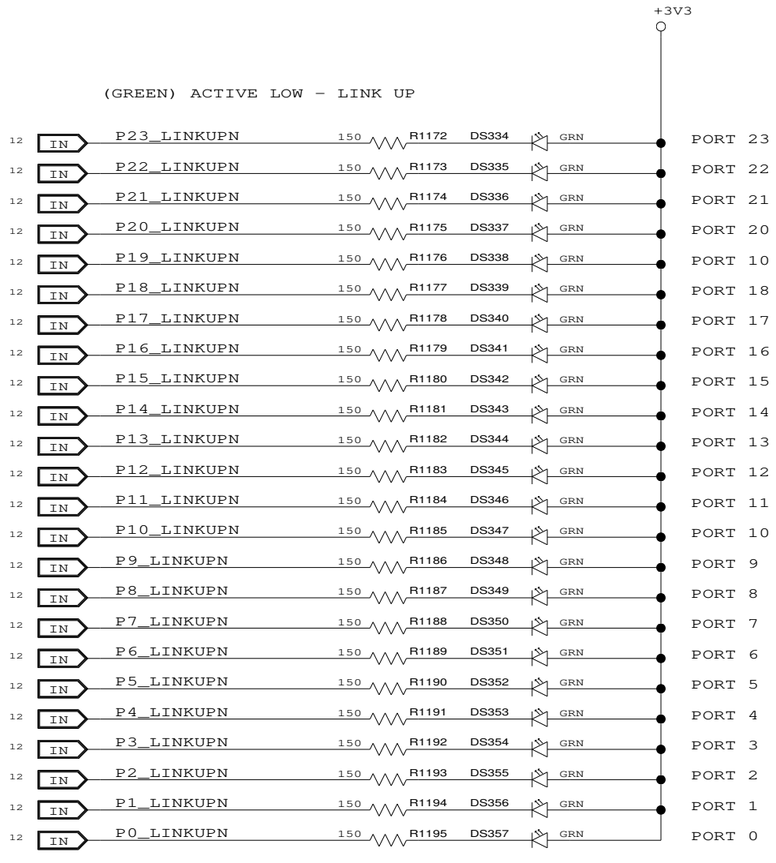
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0

AUTHOR	CHECKED BY
Tony Tran	Derek Huang

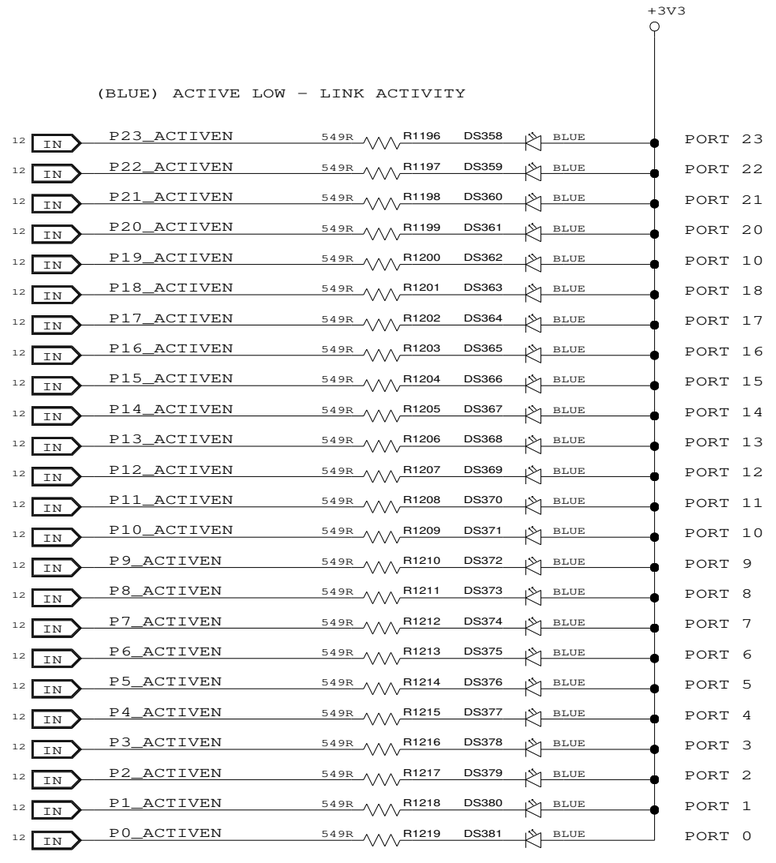
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(GREEN) ACTIVE LOW – LINK UP



(BLUE) ACTIVE LOW – LINK ACTIVITY



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LED – PORT STATUS (7 OF 7)

SIZE	DRAWING NO.	FAB P/N	REV.
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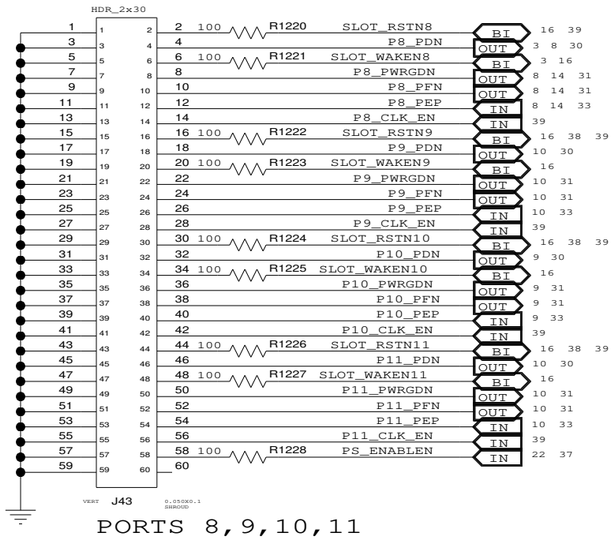
AUTHOR	CHECKED BY
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Thu Jun 10 11:24:55 2010 SHEET 36 OF 41

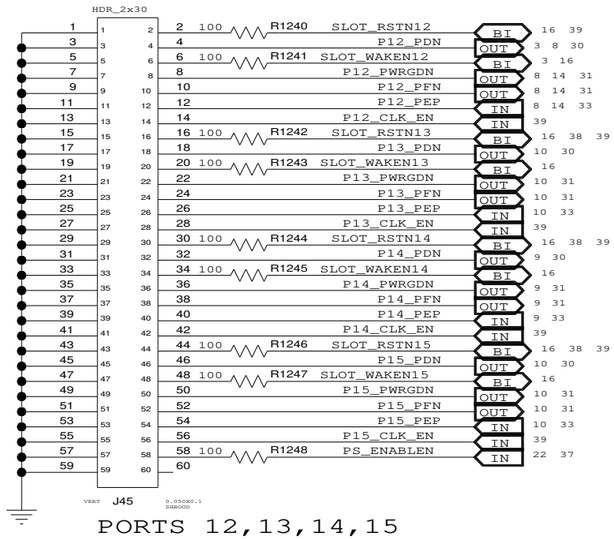
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SLOT_RESETN
CARD_PRESENTN
WAKEN
POWERGOOD
PWR_FLTN
PWR_ENABLE
CLOCK_ENABLEN

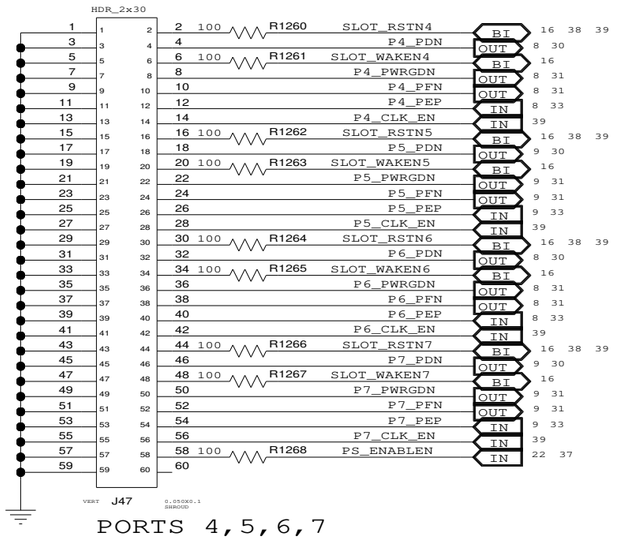
PS_ENABLEN
CABLE SENSE



PORTS 8,9,10,11



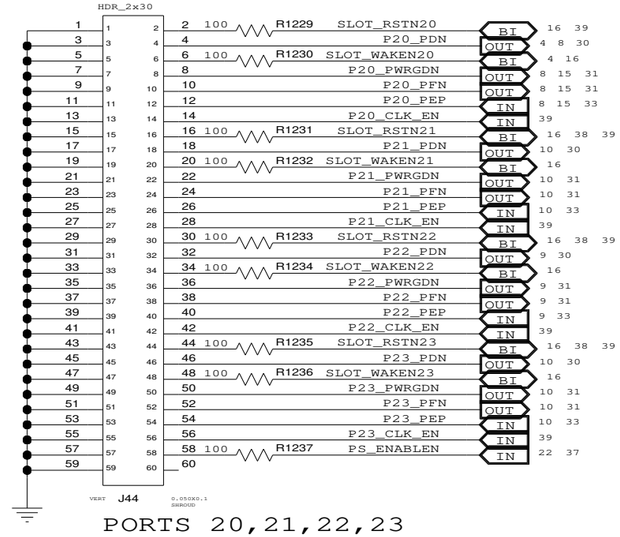
PORTS 12,13,14,15



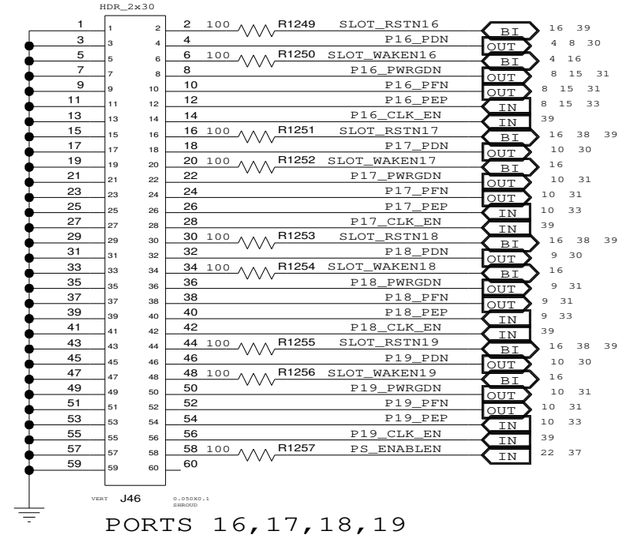
PORTS 4,5,6,7

SLOT_RESETN
CARD_PRESENTN
WAKEN
POWERGOOD
PWR_FLTN
PWR_ENABLE
CLOCK_ENABLEN

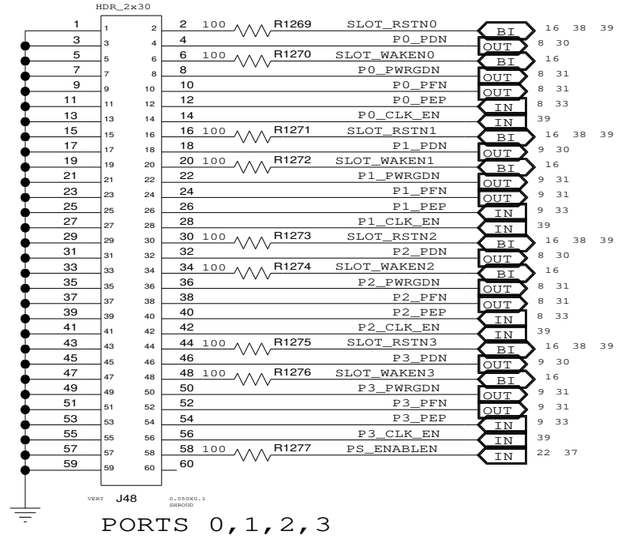
PS_ENABLEN
CABLE SENSE



PORTS 20,21,22,23



PORTS 16,17,18,19



PORTS 0,1,2,3

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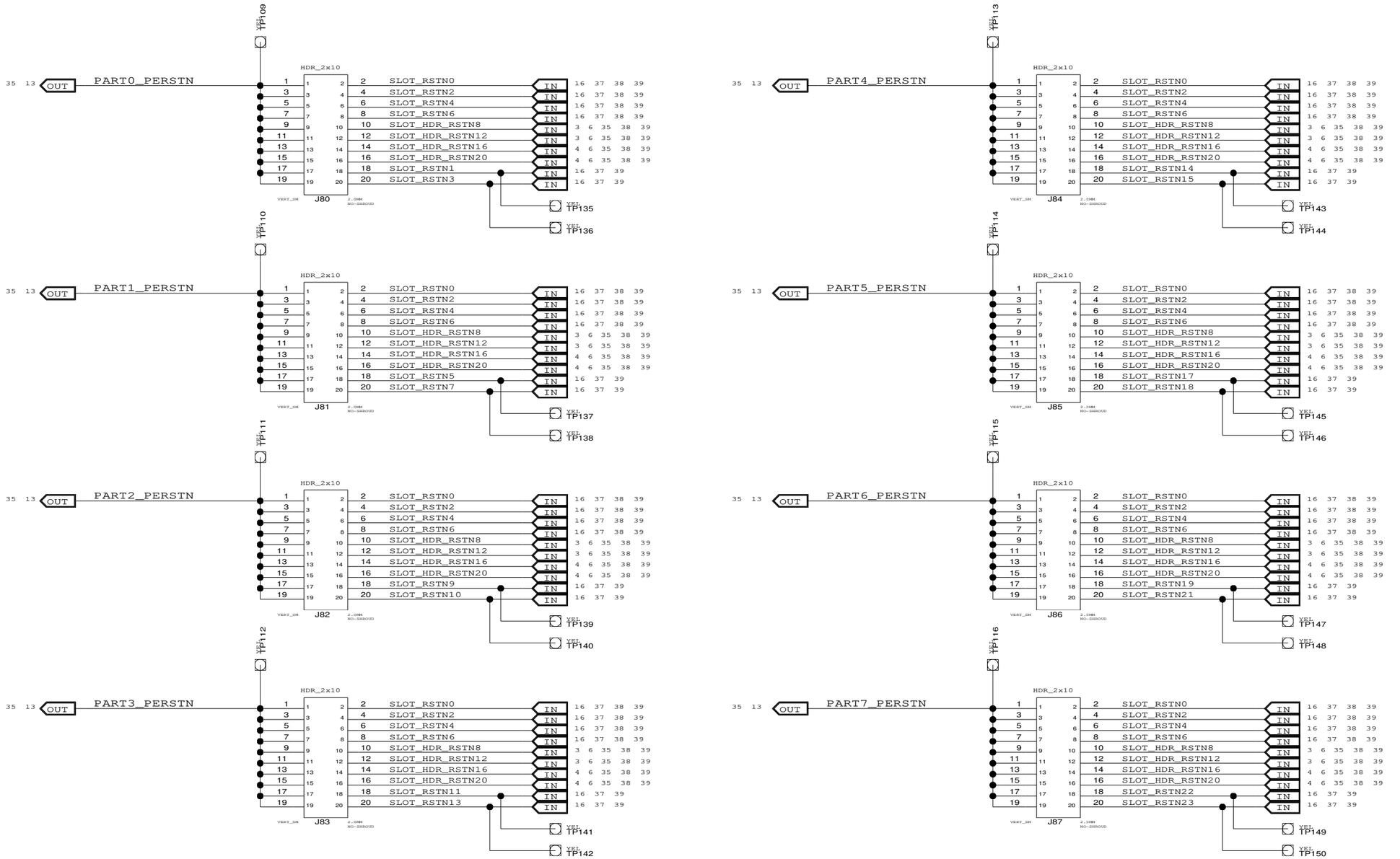
SIDEBAND CONNECTORS

SIZE	DRAWING NO.	FAB P/N	REV.
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PARTITION RESET SELECT HEADERS

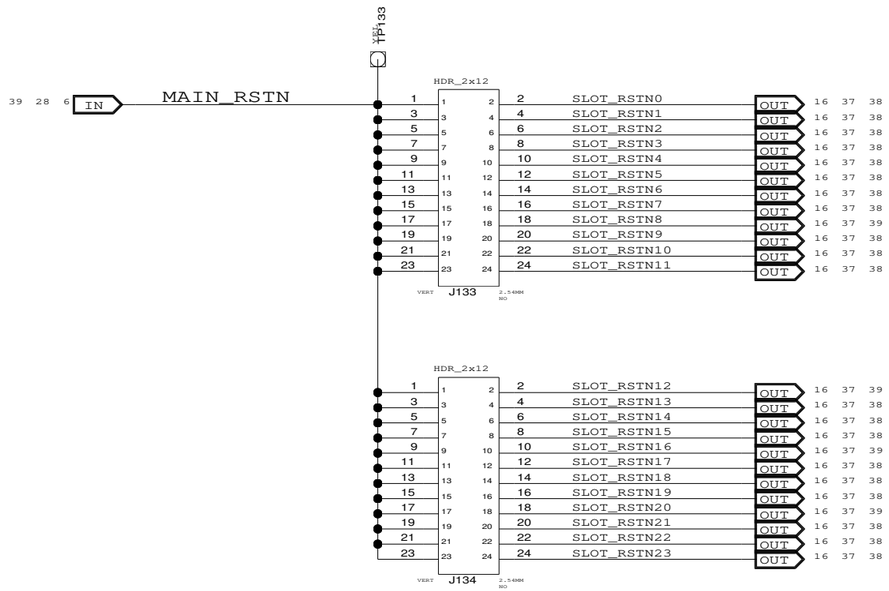
SIZE	DRAWING NO.	FAB P/N	REV.
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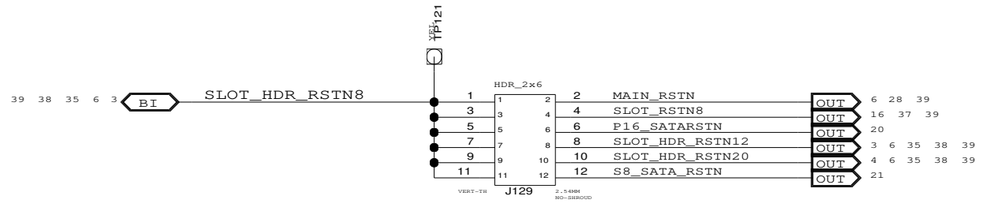
AUTHOR	CHECKED BY
Tony Tran	Derek Huang

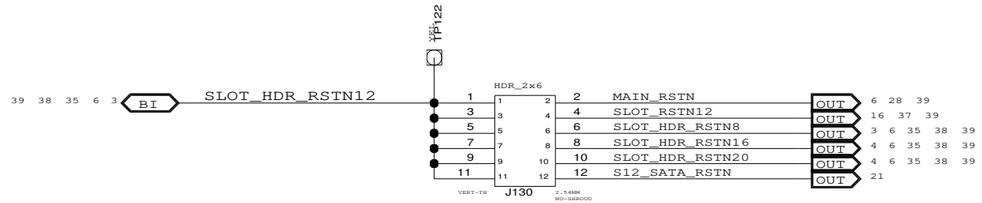
Thu Jun 10 11:24:56 2010 SHEET 38 OF 41

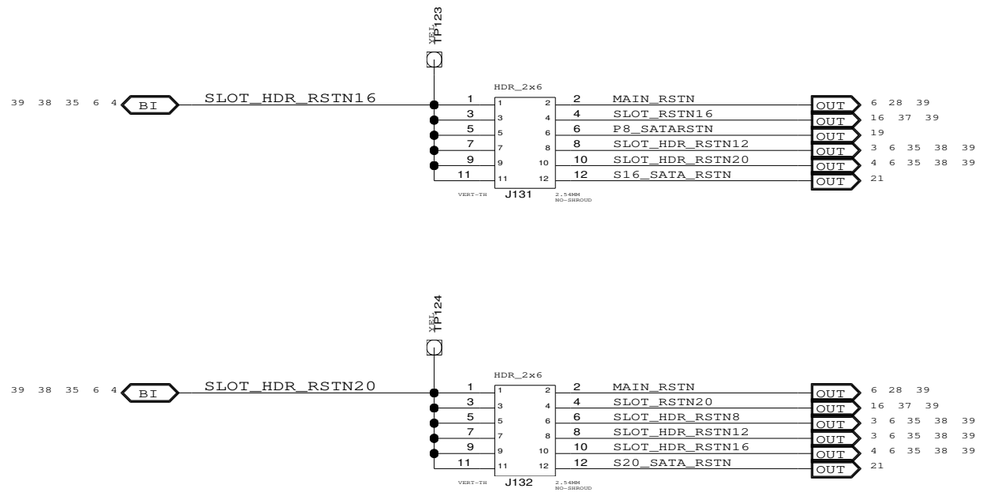
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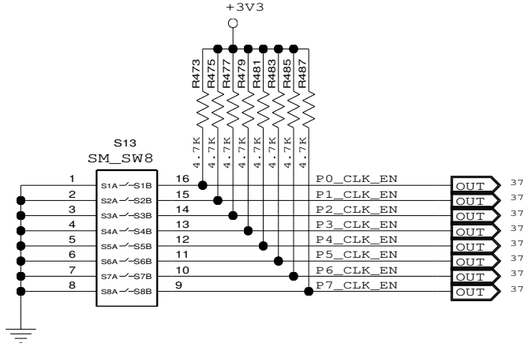
NOTE: DNP JUMPERS WHEN IOEXPANDER IS ENABLED

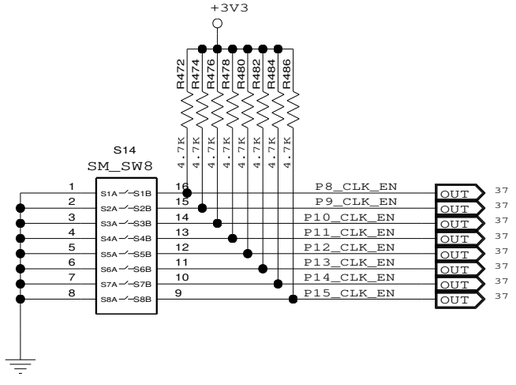


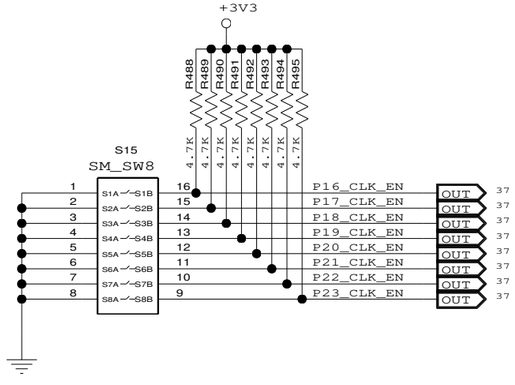












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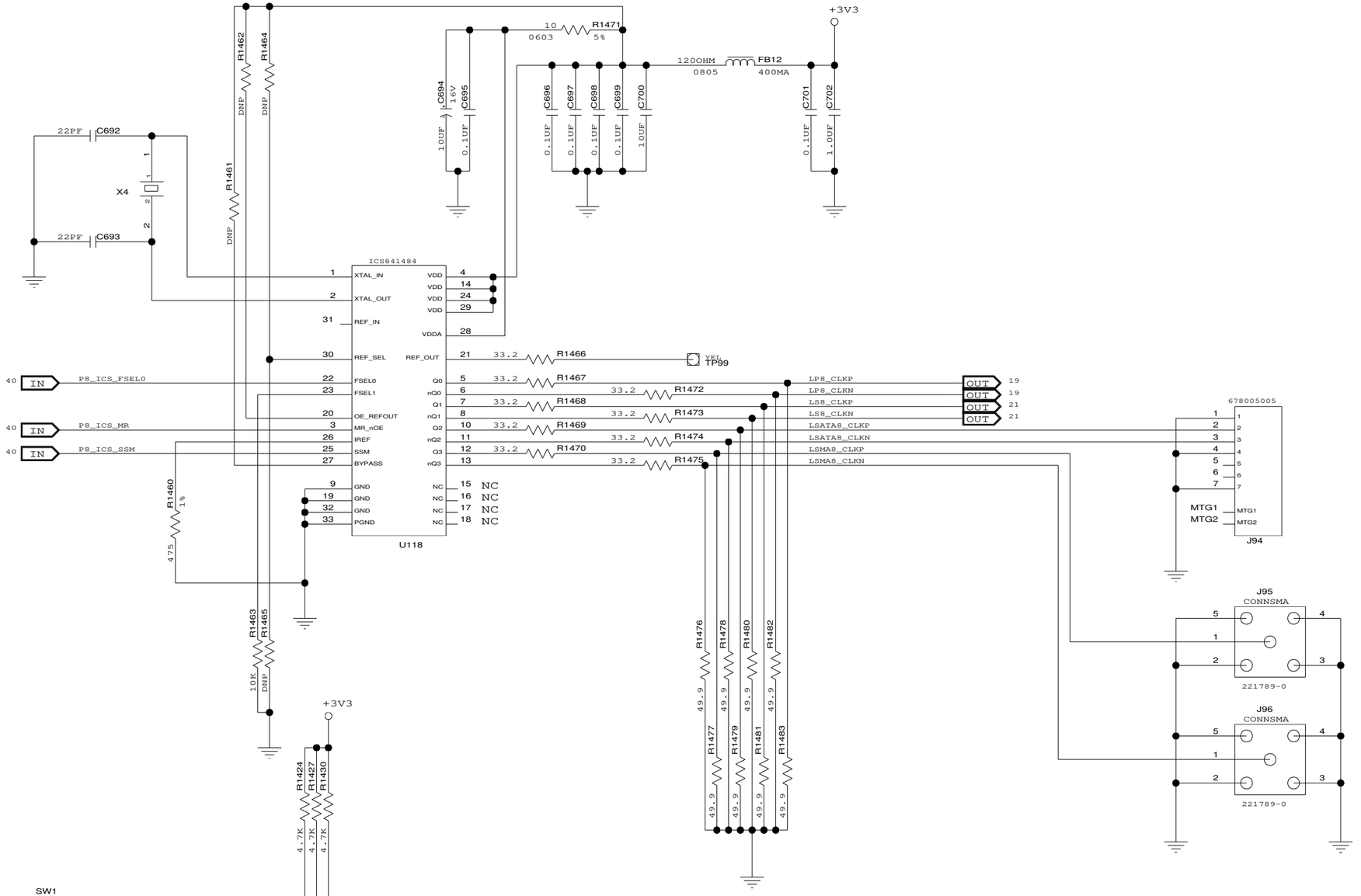
SLOT RESET SELECT HEADERS

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0

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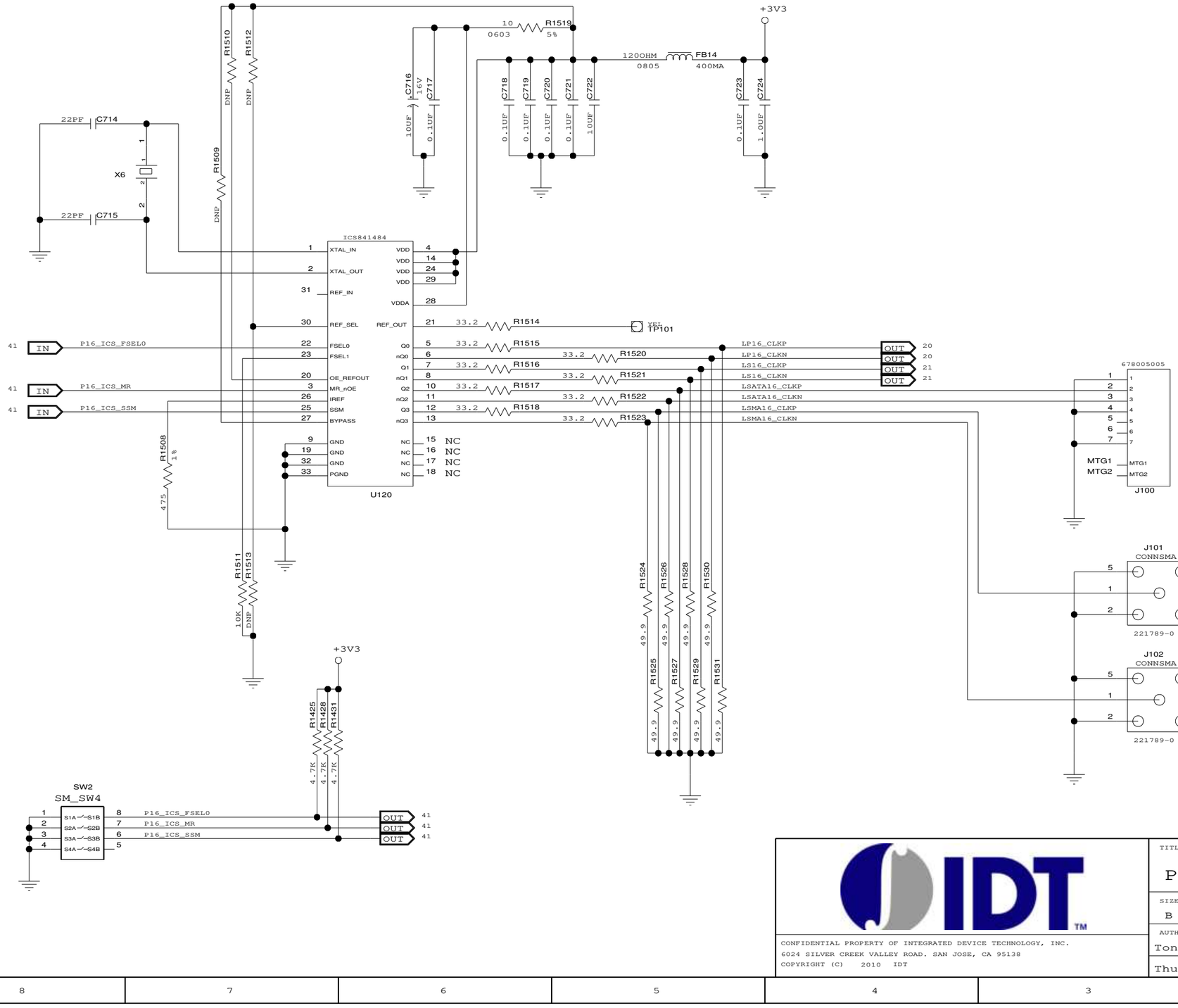
PORT 8 CLOCK GENERATOR

SIZE	DRAWING NO.	FAB P/N	REV.
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TITLE EB-LOGAN-19

PORT 16 CLOCK GENERATOR

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0

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