3.3V HIGH-DENSITY SUPERSYNC™ II 36-BIT FIFO

1,024 x 36, 2,048 x 36
4,096 x 36, 8,192 x 36
16,384 x 36, 32,768 x 36

IDT72V3640, IDT72V3650
IDT72V3660, IDT72V3670
IDT72V3680, IDT72V3690

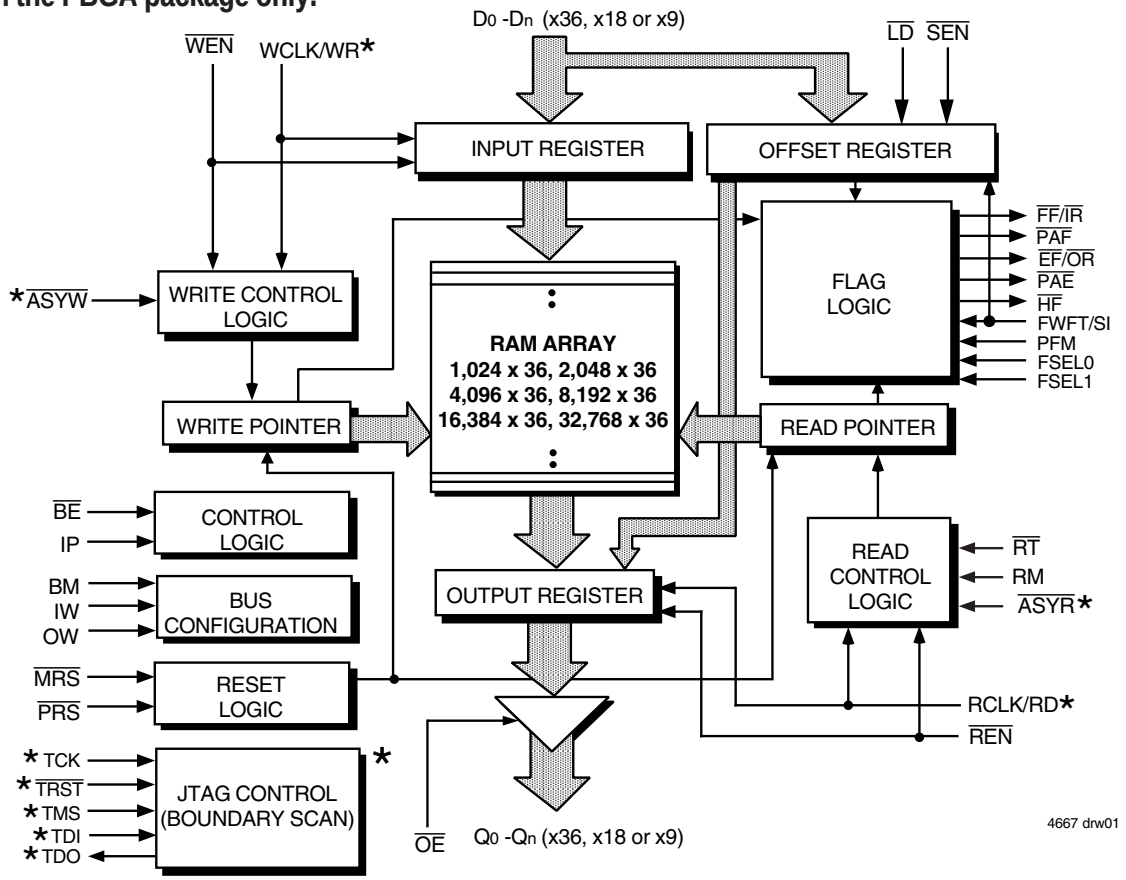
LEAD FINISH (SnPb) ARE IN EOL PROCESS - LAST TIME BUY EXPIRES JUNE 15, 2018

FEATURES:

- **Choose among the following memory organizations:**
  - **IDT72V3640 — 1,024 x 36**
  - **IDT72V3650 — 2,048 x 36**
  - **IDT72V3660 — 4,096 x 36**
  - **IDT72V3670 — 8,192 x 36**
  - **IDT72V3680 — 16,384 x 36**
  - **IDT72V3690 — 32,768 x 36**
- **Up to 166 MHz Operation of the Clocks**
- **User selectable Asynchronous read and/or write ports (PBGA Only)**
- **User selectable input and output port bus-sizing**
  - *x36 in to x36 out*
  - *x36 in to x18 out*
  - *x36 in to x9 out*
  - *x18 in to x36 out*
  - *x9 in to x36 out*
- **Pin to Pin compatible to the higher density of IDT72V36100 and IDT72V36110**
- **Big-Endian/Little-Endian user selectable byte representation**
- **5V input tolerant**
- **Fixed, low first word latency**
- **Zero latency retransmit**
- **Auto power down minimizes standby power consumption**
- **Master Reset clears entire FIFO**
- **Partial Reset clears data, but retains programmable settings**
- **Empty, Full and Half-Full flags signal FIFO status**
- **Programmable Almost-Empty and Almost-Full flags, each flag can default to one of eight preselected offsets**
- **Selectable synchronous/asynchronous timing modes for Almost-Empty and Almost-Full flags**
- **Program programmable flags by either serial or parallel means**
- **Select IDT Standard timing (using $\overline{EF}$ and $\overline{FF}$ flags) or First Word Fall Through timing (using $\overline{OR}$ and $\overline{IR}$ flags)**
- **Output enable puts data outputs into high impedance state**
- **Easily expandable in depth and width**
- **JTAG port, provided for Boundary Scan function (PBGA Only)**
- **Independent Read and Write Clocks (permit reading and writing simultaneously)**
- **Available in a 128-pin Thin Quad Flat Pack (TQFP) or a 144-pin Plastic Ball Grid Array (PBGA) (with additional features)**
- **High-performance submicron CMOS technology**
- **Industrial temperature range (–40°C to +85°C) is available**
- **Green parts available, see ordering information**

FUNCTIONAL BLOCK DIAGRAM

***Available on the PBGA package only.**



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DESCRIPTION:

The IDT72V3640/72V3650/72V3660/72V3670/72V3680/72V3690 are exceptionally deep, high speed, CMOS First-In-First-Out (FIFO) memories with clocked read and write controls and a flexible Bus-Matching x36/x18/x9 data flow. These FIFOs offer several key user benefits:

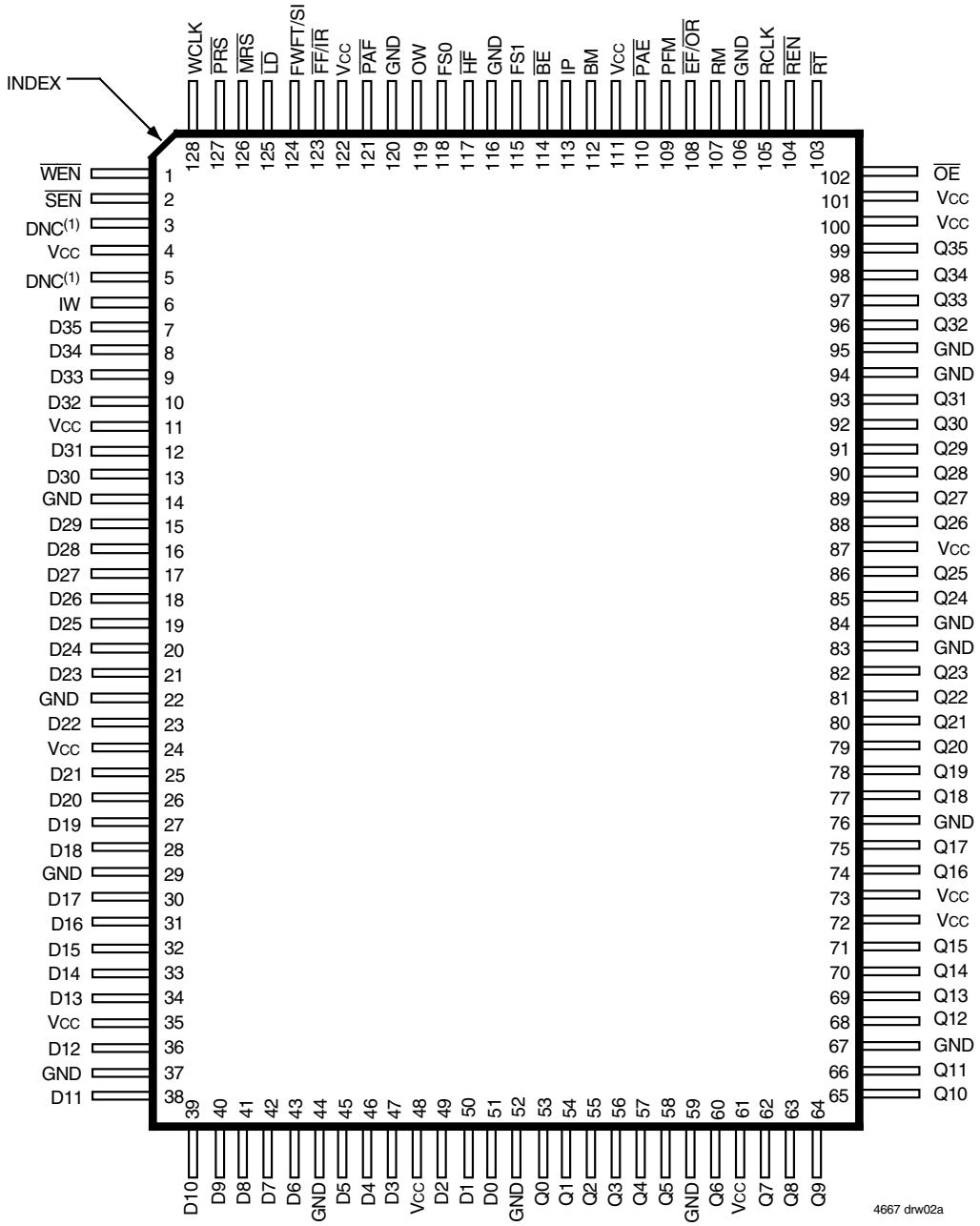
- Flexible x36/x18/x9 Bus-Matching on both read and write ports
- The period required by the retransmit operation is fixed and short.
- The first word data latency period, from the time the first word is written to an empty FIFO to the time it can be read, is fixed and short.
- Asynchronous/Synchronous translation on the read or write ports
- High density offerings up to 1 Mbit

Bus-Matching Sync FIFOs are particularly appropriate for network, video, telecommunications, data communications and other applications that need to buffer large amounts of data and match busses of unequal sizes.

Each FIFO has a data input port (D_n) and a data output port (Q_n), both of which can assume either a 36-bit, 18-bit or a 9-bit width as determined by the state of external control pins Input Width (IW), Output Width (OW), and Bus-Matching (BM) pin during the Master Reset cycle.

The input port can be selected as either a Synchronous (clocked) interface, or Asynchronous interface. During Synchronous operation the input port is controlled by a Write Clock (WCLK) input and a Write Enable ($\overline{WEN}$) input. Data present on the Dn data inputs is written into the FIFO on every rising edge of

PIN CONFIGURATIONS



TQFP (PK128, order code: PF)
TOP VIEW

NOTE:
1. DNC = Do Not Connect.

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WCLK when $\overline{WEN}$ is asserted. During Asynchronous operation only the WR input is used to write data into the FIFO. Data is written on a rising edge of WR, the $\overline{WEN}$ input should be tied to its active state, (LOW).

The output port can be selected as either a Synchronous (clocked) interface, or Asynchronous interface. During Synchronous operation the output port is controlled by a Read Clock (RCLK) input and Read Enable ($\overline{REN}$) input. Data is read from the FIFO on every rising edge of RCLK when $\overline{REN}$ is asserted. During Asynchronous operation only the RD input is used to read data from the FIFO. Data is read on a rising edge of RD, the $\overline{REN}$ input should be tied to its active state, LOW. When Asynchronous operation is selected on the output port the FIFO must be configured for Standard IDT mode, and the $\overline{OE}$ input used to provide three-state control of the outputs, Qn.

The frequencies of both the RCLK and the WCLK signals may vary from 0 to f_{MAX} with complete independence. There are no restrictions on the frequency of the one clock input with respect to the other.

There are two possible timing modes of operation with these devices: IDT Standard mode and First Word Fall Through (FWFT) mode.

In *IDT Standard mode*, the first word written to an empty FIFO will not appear on the data output lines unless a specific read operation is performed. A read operation, which consists of activating $\overline{REN}$ and enabling a rising RCLK edge, will shift the word from internal memory to the data output lines.

In *FWFT mode*, the first word written to an empty FIFO is clocked directly to the data output lines after three transitions of the RCLK signal. A $\overline{REN}$ does not have to be asserted for accessing the first word. However, subsequent

PIN CONFIGURATIONS (CONTINUED)

A1 BALL PAD CORNER

	1	2	3	4	5	6	7	8	9	10	11	12
A	$\overline{ASYW}$	$\overline{WEN}$	WCLK	$\overline{PAF}$	$\overline{FF/IR}$	$\overline{HF}$	BM	$\overline{EF}$	RCLK	$\overline{REN}$	$\overline{OE}$	Q35
B	$\overline{SEN}$	IW	$\overline{PRS}$	$\overline{LD}$	$\overline{MRS}$	FS0	FS1	$\overline{ASYR}$	IP	PFM	$\overline{RT}$	Q34
C	D35	D34	D33	FWFT/SI	OW	VCC	VCC	$\overline{BE}$	$\overline{PAE}$	RM	Q32	Q33
D	D32	D31	D30	VCC	VCC	GND	GND	VCC	VCC	Q29	Q30	Q31
E	D29	D28	D27	VCC	GND	GND	GND	GND	VCC	Q26	Q27	Q28
F	D26	D25	D24	VCC	GND	GND	GND	GND	VCC	Q23	Q24	Q25
G	D21	D22	D23	VCC	GND	GND	GND	GND	VCC	Q22	Q21	Q20
H	D18	D19	D20	VCC	GND	GND	GND	GND	VCC	Q19	Q18	Q17
J	D15	D16	D17	VCC	VCC	GND	GND	VCC	VCC	Q16	Q15	Q14
K	D12	D13	D14	D3	D0	VCC	VCC	TDO	Q2	Q13	Q12	Q11
L	D10	D11	D6	D4	D1	TMS	TCK	Q0	Q3	Q5	Q10	Q9
M	D9	D8	D7	D5	D2	$\overline{TRST}$	TDI	Q1	Q4	Q6	Q7	Q8

4667 drw02b

PBGA: 1mm pitch, 13mm x 13mm (BB144, order code: BB)
TOP VIEW

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words written to the FIFO do require a LOW on $\overline{REN}$ for access. The state of the FWFT/SI input during Master Reset determines the timing mode in use.

For applications requiring more data storage capacity than a single FIFO can provide, the FWFT timing mode permits depth expansion by chaining FIFOs in series (i.e. the data outputs of one FIFO are connected to the corresponding data inputs of the next). No external logic is required.

These FIFOs have five flag pins, $\overline{EF}/\overline{OR}$ (Empty Flag or Output Ready), $\overline{FF}/\overline{IR}$ (Full Flag or Input Ready), $\overline{HF}$ (Half-full Flag), $\overline{PAE}$ (Programmable Almost-Empty flag) and $\overline{PAF}$ (Programmable Almost-Full flag). The $\overline{EF}$ and $\overline{FF}$ functions are selected in IDT Standard mode. The $\overline{IR}$ and $\overline{OR}$ functions are selected in FWFT mode. $\overline{HF}$, $\overline{PAE}$ and $\overline{PAF}$ are always available for use, irrespective of timing mode.

$\overline{PAE}$ and $\overline{PAF}$ can be programmed independently to switch at any point in memory. Programmable offsets determine the flag switching threshold and can be loaded by two methods: parallel or serial. Eight default offset settings are also provided, so that $\overline{PAE}$ can be set to switch at a predefined number of locations from the empty boundary and the $\overline{PAF}$ threshold can also be set at similar predefined values from the full boundary. The default offset values are set during Master Reset by the state of the FSEL0, FSEL1, and $\overline{LD}$ pins.

For serial programming, $\overline{SEN}$ together with $\overline{LD}$ on each rising edge of WCLK, are used to load the offset registers via the Serial Input (SI). For parallel programming, $\overline{WEN}$ together with $\overline{LD}$ on each rising edge of WCLK, are used to load the offset registers via D_n. $\overline{REN}$ together with $\overline{LD}$ on each rising edge of RCLK can be used to read the offsets in parallel from Q_n regardless of whether serial or parallel offset loading has been selected.

During Master Reset ($\overline{MRS}$) the following events occur: the read and write pointers are set to the first location of the FIFO. The FWFT pin selects IDT Standard mode or FWFT mode.

The Partial Reset ($\overline{PRS}$) also sets the read and write pointers to the first location of the memory. However, the timing mode, programmable flag programming method, and default or programmed offset settings existing before Partial Reset remain unchanged. The flags are updated according to the timing mode and offsets in effect. $\overline{PRS}$ is useful for resetting a device in mid-operation, when reprogramming programmable flags would be undesirable.

It is also possible to select the timing mode of the $\overline{PAE}$ (Programmable Almost-Empty flag) and $\overline{PAF}$ (Programmable Almost-Full flag) outputs. The timing modes can be set to be either asynchronous or synchronous for the $\overline{PAE}$ and $\overline{PAF}$ flags.

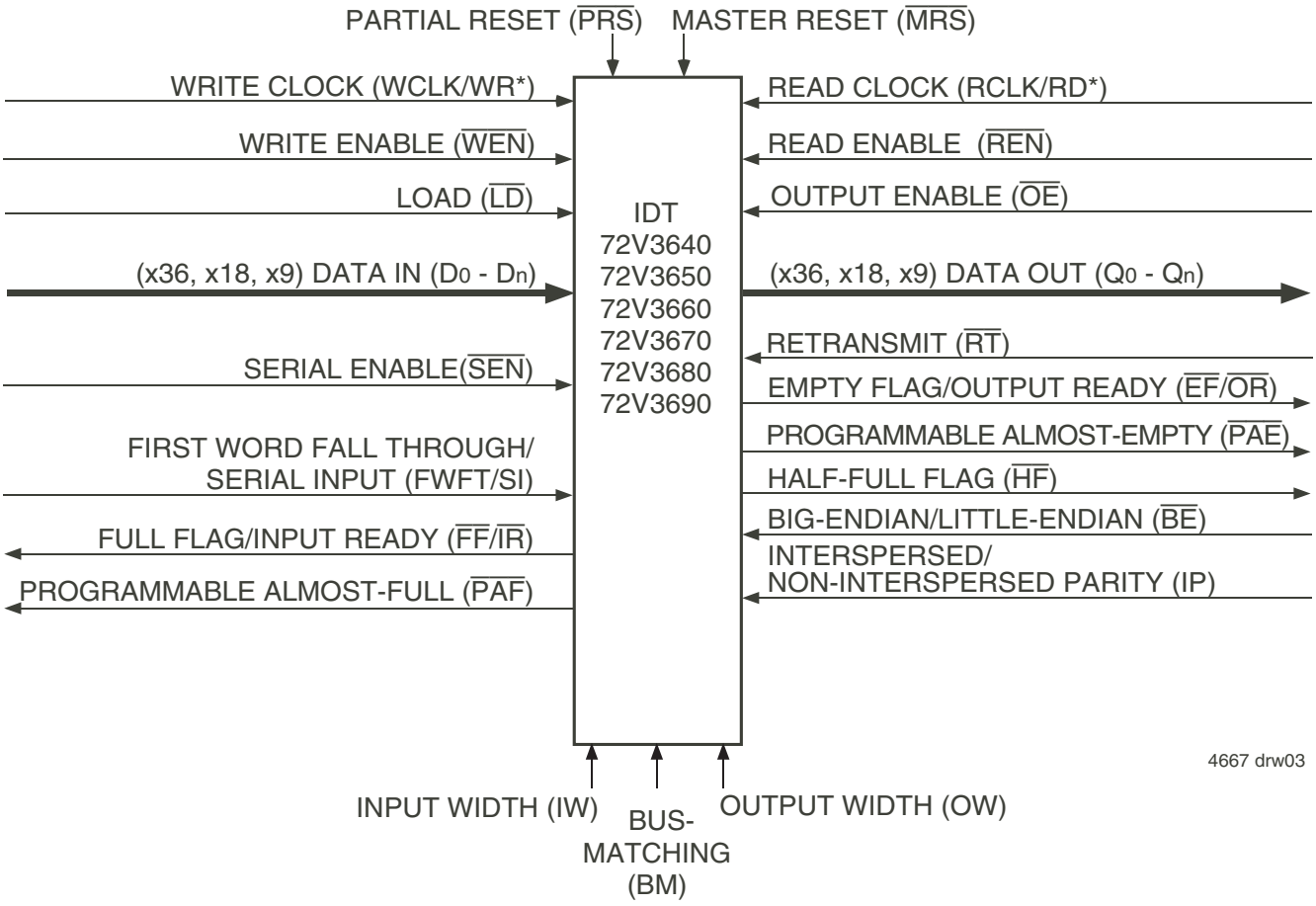


Figure 1. Single Device Configuration Signal Flow Diagram

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If asynchronous $\overline{PAE}$/$\overline{PAF}$ configuration is selected, the $\overline{PAE}$ is asserted LOW on the LOW-to-HIGH transition of RCLK. $\overline{PAE}$ is reset to HIGH on the LOW-to-HIGH transition of WCLK. Similarly, the $\overline{PAF}$ is asserted LOW on the LOW-to-HIGH transition of WCLK and $\overline{PAF}$ is reset to HIGH on the LOW-to-HIGH transition of RCLK.

If synchronous $\overline{PAE}$/$\overline{PAF}$ configuration is selected, the $\overline{PAE}$ is asserted and updated on the rising edge of RCLK only and not WCLK. Similarly, $\overline{PAF}$ is asserted and updated on the rising edge of WCLK only and not RCLK. The mode desired is configured during Master Reset by the state of the Programmable Flag Mode (PFM) pin.

The Retransmit function allows data to be reread from the FIFO more than once. A LOW on the $\overline{RT}$ input during a rising RCLK edge initiates a retransmit operation by setting the read pointer to the first location of the memory array. A zero-latency retransmit timing mode can be selected using the Retransmit timing Mode pin (RM). During Master Reset, a LOW on RM will select zero latency retransmit. A HIGH on RM during Master Reset will select normal latency.

If zero latency retransmit operation is selected, the first data word to be retransmitted will be placed on the output register with respect to the same RCLK edge that initiated the retransmit based on RT being LOW.

Refer to Figure 11 and 12 for *Retransmit Timing* with normal latency. Refer to Figure 13 and 14 for *Zero Latency Retransmit Timing*.

The device can be configured with different input and output bus widths as shown in Table 1.

A Big-Endian/Little-Endian data word format is provided. This function is useful when data is written into the FIFO in long word format (x36/x18) and read out of the FIFO in small word (x18/x9) format. If Big-Endian mode is selected, then the most significant byte (word) of the long word written into the FIFO will be read out of the FIFO first, followed by the least significant byte. If Little-Endian format is selected, then the least significant byte of the long word written into the FIFO will be read out first, followed by the most significant byte. The mode desired is configured during master reset by the state of the Big-Endian ($\overline{BE}$) pin. See Figure 4 for *Bus-Matching Byte Arrangement*.

The Interspersed/Non-Interspersed Parity (IP) bit function allows the user to select the parity bit in the word loaded into the parallel port (D_0-Dn) when programming the flag offsets. If Interspersed Parity mode is selected, then the FIFO will assume that the parity bit is located in bit positions D8, D17, D26 and D35 during the parallel programming of the flag offsets. If Non-Interspersed Parity mode is selected, then D8, D17 and D26 are assumed to be valid bits and D32, D33, D34 and D35 are ignored. IP mode is selected during Master Reset by the state of the IP input pin. Interspersed Parity control only has an effect during parallel programming of the offset registers. It does not effect the data written to and read from the FIFO.

A JTAG test port is provided, here the FIFO has fully functional Boundary Scan feature, compliant with IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture.

If, at any time, the FIFO is not actively performing an operation, the chip will automatically power down. Once in the power down state, the standby supply current consumption is minimized. Initiating any operation (by activating control inputs) will immediately take the device out of the power down state.

The IDT72V3640/72V3650/72V3660/72V3670/72V3680/72V3690 are fabricated using IDT's high speed submicron CMOS technology.

TABLE 1 — BUS-MATCHING CONFIGURATION MODES

BM	IW	OW	Write Port Width	Read Port Width
L	L	L	x36	x36
H	L	L	x36	x18
H	L	H	x36	x9
H	H	L	x18	x36
H	H	H	x9	x36

NOTE:
1. Pin status during Master Reset.

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PIN DESCRIPTION (TQFP AND PBGA PACKAGES)

Symbol	Name	I/O	Description
BM[1]	Bus-Matching	I	BM works with IW and OW to select the bus sizes for both write and read ports. See Table 1 for bus size configuration.
$\overline{BE}$[1]	Big-Endian/ Little-Endian	I	During Master Reset, a LOW on $\overline{BE}$ will select Big-Endian operation. A HIGH on $\overline{BE}$ during Master Reset will select Little-Endian format.
D_0–D_{35}	Data Inputs	I	Data inputs for a 36-, 18- or 9-bit bus. When in 18- or 9-bit mode, the unused input pins are in a don't care state.
$\overline{EF}$/$\overline{OR}$	Empty Flag/ Output Ready	O	In the IDT Standard mode, the $\overline{EF}$ function is selected. $\overline{EF}$ indicates whether or not the FIFO memory is empty. In FWFT mode, the $\overline{OR}$ function is selected. $\overline{OR}$ indicates whether or not there is valid data available at the outputs.
$\overline{FF}$/$\overline{IR}$	Full Flag/ Input Ready	O	In the IDT Standard mode, the $\overline{FF}$ function is selected. $\overline{FF}$ indicates whether or not the FIFO memory is full. In the FWFT mode, the $\overline{IR}$ function is selected. $\overline{IR}$ indicates whether or not there is space available for writing to the FIFO memory.
FSEL0[1]	Flag Select Bit 0	I	During Master Reset, this input along with FSEL1 and the $\overline{LD}$ pin, will select the default offset values for the programmable flags $\overline{PAE}$ and $\overline{PAF}$. There are up to eight possible settings available.
FSEL1[1]	Flag Select Bit 1	I	During Master Reset, this input along with FSEL0 and the $\overline{LD}$ pin will select the default offset values for the programmable flags $\overline{PAE}$ and $\overline{PAF}$. There are up to eight possible settings available.
FWFT/SI	First Word Fall Through/Serial In	I	During Master Reset, selects First Word Fall Through or IDT Standard mode. After Master Reset, this pin functions as a serial input for loading offset registers.
$\overline{HF}$	Half-Full Flag	O	$\overline{HF}$ indicates whether the FIFO memory is more or less than half-full.
IP[1]	Interspersed Parity	I	During Master Reset, a LOW on IP will select Non-Interspersed Parity mode. A HIGH will select Interspersed Parity mode. Interspersed Parity control only has an effect during parallel programming of the offset registers. It does not effect the data written to and read from the FIFO.
IW[1]	Input Width	I	This pin, along with OW and MB, selects the bus width of the write port. See Table 1 for bus size configuration.
$\overline{LD}$	Load	I	This is a dual purpose pin. During Master Reset, the state of the $\overline{LD}$ input along with FSEL0 and FSEL1, determines one of eight default offset values for the $\overline{PAE}$ and $\overline{PAF}$ flags, along with the method by which these offset registers can be programmed, parallel or serial (see Table 2). After Master Reset, this pin enables writing to and reading from the offset registers.
$\overline{OE}$	Output Enable	I	$\overline{OE}$ controls the output impedance of Q_n.
OW[1]	Output Width	I	This pin, along with IW and BM, selects the bus width of the read port. See Table 1 for bus size configuration.
$\overline{MRS}$	Master Reset	I	$\overline{MRS}$ initializes the read and write pointers to zero and sets the output register to all zeroes. During Master Reset, the FIFO is configured for either FWFT or IDT Standard mode, Bus-Matching configurations, one of eight progammable flag default settings, serial or parallel programming of the offset settings, Big-Endian/Little-Endian format, zero latency timing mode, interspersed parity, and synchronous versus asynchronous programmable flag timing modes.
$\overline{PAE}$	Programmable Almost-Empty Flag	O	$\overline{PAE}$ goes LOW if the number of words in the FIFO memory is less than offset n, which is stored in the Empty Offset register. $\overline{PAE}$ goes HIGH if the number of words in the FIFO memory is greater than or equal to offset n.
$\overline{PAF}$	Programmable Almost-Full Flag	O	$\overline{PAF}$ goes HIGH if the number of free locations in the FIFO memory is more than offset m, which is stored in the Full Offset register. $\overline{PAF}$ goes LOW if the number of free locations in the FIFO memory is less than or equal to m.
PFM[1]	Programmable Flag Mode	I	During Master Reset, a LOW on PFM will select Asynchronous Programmable flag timing mode. A HIGH on PFM will select Synchronous Programmable flag timing mode.
$\overline{PRS}$	Partial Reset	I	$\overline{PRS}$ initializes the read and write pointers to zero and sets the output register to all zeroes. During Partial Reset, the existing mode (IDT or FWFT), programming method (serial or parallel), and programmable flag settings are all retained.
Q_0–Q_{35}	Data Outputs	O	Data outputs for an 36-, 18- or 9-bit bus. When in 18- or 9-bit mode, the unused output pins are in a don't care state. Outputs are not 5V tolerant regardless of the state of $\overline{OE}$.
RCLK/ RD	Read Clock/ Read Strobe	I	If Synchronous operation of the read port has been selected, when enabled by $\overline{REN}$, the rising edge of RCLK reads data from the FIFO memory and offsets from the programmable registers. If $\overline{LD}$ is LOW, the values loaded into the offset registers is output on a rising edge of RCLK. If Asynchronous operation of the read port has been selected, a rising edge on RD reads data from the FIFO in an Asynchronous manner. $\overline{REN}$ should be tied LOW. Asynchronous operation of the RCLK/RD input is only available in the PBGA package.
$\overline{REN}$	Read Enable	I	$\overline{REN}$ enables RCLK for reading data from the FIFO memory and offset registers.
RM[1]	Retransmit Timing Mode	I	During Master Reset, a LOW on RM will select zero latency Retransmit timing Mode. A HIGH on RM will select normal latency mode.
$\overline{RT}$	Retransmit	I	$\overline{RT}$ asserted on the rising edge of RCLK initializes the READ pointer to zero, sets the $\overline{EF}$ flag to LOW ($\overline{OR}$ to HIGH in FWFT mode) and does not disturb the write pointer, programming method, existing timing mode or programmable flag settings. $\overline{RT}$ is useful to reread data from the first physical location of the FIFO.

NOTE:
1. Inputs should not change state after Master Reset.

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PIN DESCRIPTION-CONTINUED (TQFP & PBGA PACKAGES)

Symbol	Name	I/O	Description
$\overline{SEN}$	Serial Enable	I	$\overline{SEN}$ enables serial loading of programmable flag offsets.
WCLK/ WR	Write Clock/ Write Strobe	I	If Synchronous operation of the write port has been selected, when enabled by $\overline{WEN}$, the rising edge of WCLK writes data into the FIFO. If Asynchronous operation of the write port has been selected, WR writes data into the FIFO on a rising edge in an Asynchronous manner, ($\overline{WEN}$ should be tied to its active state). Asynchronous operation of the WCLK/WR input is only available in the PBGA package.
$\overline{WEN}$	Write Enable	I	$\overline{WEN}$ enables WCLK for writing data into the FIFO memory and offset registers.
VCC	+3.3V Supply	I	These are VCC supply inputs and must be connected to the 3.3V supply rail.

NOTE:
1. Inputs should not change state after Master Reset.

PIN DESCRIPTION (PBGA PACKAGE ONLY)

Symbol	Name	I/O	Description
$\overline{ASYR}$[1]	Asynchronous Read Port	I	A HIGH on this input during Master Reset will select Synchronous read operation for the output port. A LOW will select Asynchronous operation. If Asynchronous is selected the FIFO must operate in IDT Standard mode.
$\overline{ASYW}$[1]	Asynchronous Write Port	I	A HIGH on this input during Master Reset will select Synchronous write operation for the input port. A LOW will select Asynchronous operation.
TCK[2]	JTAG Clock	I	Clock input for JTAG function. One of four terminals required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to TCK. Data from TMS and TDI are sampled on the rising edge of TCK and outputs change on the falling edge of TCK. If the JTAG function is not used this signal needs to be tied to GND.
TDI[2]	JTAG Test Data Input	I	One of four terminals required by IEEE Standard 1149.1-1990. During the JTAG boundary scan operation, test data serially loaded via the TDI on the rising edge of TCK to either the Instruction Register, ID Register and Bypass Register. An internal pull-up resistor forces TDI HIGH if left unconnected.
TDO[2]	JTAG Test Data Output	O	One of four terminals required by IEEE Standard 1149.1-1990. During the JTAG boundary scan operation, test data serially loaded output via the TDO on the falling edge of TCK from either the Instruction Register, ID Register and Bypass Register. This output is high impedance except when shifting, while in SHIFT-DR and SHIFT-IR controller states.
TMS[2]	JTAG Mode Select	I	TMS is a serial input pin. One of four terminals required by IEEE Standard 1149.1-1990. TMS directs the device through its TAP controller states. An internal pull-up resistor forces TMS HIGH if left unconnected.
$\overline{TRST}$[2]	JTAG Reset	I	$\overline{TRST}$ is an asynchronous reset pin for the JTAG controller. The JTAG TAP controller does not automatically reset upon power-up, thus it must be reset by either this signal or by setting TMS= HIGH for five TCK cycles. If the TAP controller is not properly reset then the FIFO outputs will always be in high-impedance. If the JTAG function is used but the user does not want to use $\overline{TRST}$, then $\overline{TRST}$ can be tied with $\overline{MRS}$ to ensure proper FIFO operation. If the JTAG function is not used then this signal needs to be tied to GND.

NOTE:
1. Inputs should not change state after Master Reset.
2. These pins are for the JTAG port. Please refer to pages 42-45 and Figures 31-33.

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ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Com'l & Ind'l	Unit
V_{TERM}[2]	Terminal Voltage with respect to GND	–0.5 to +4.5	V
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	–50 to +50	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{CC} terminal only.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}[1]	Supply Voltage Com'l/Ind'l	3.15	3.3	3.45	V
GND	Supply Voltage Com'l/Ind'l	0	0	0	V
V_{IH}[2]	Input High Voltage Com'l/Ind'l	2.0	—	5.5	V
V_{IL}[3]	Input Low Voltage Com'l/Ind'l	—	—	0.8	V
T_A	Operating Temperature Commercial	0	—	70	°C
T_A	Operating Temperature Industrial	-40	—	85	°C

NOTES:

1. V_{CC} = 3.3V ± 0.15V, JEDEC JESD8-A compliant.
2. Outputs are not 5V tolerant.
3. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 3.3V ± 0.15V, T_A = 0°C to +70°C;Industrial: V_{CC} = 3.3V ± 0.15V, T_A = -40°C to +85°C; JEDEC JESD8-A compliant)

Symbol	Parameter	IDT72V3640L IDT72V3650L IDT72V3660L IDT72V3670L IDT72V3680L IDT72V3690L Commercial and Industrial[1] t_{CLK} = 6, 7-5, 10, 15 ns		Unit
		Min.	Max.	
I_{LI}[2]	Input Leakage Current	–1	1	µA
I_{LO}[3]	Output Leakage Current	–10	10	µA
V_{OH}	Output Logic "1" Voltage, I_{OH} = –2 mA	2.4	—	V
V_{OL}	Output Logic "0" Voltage, I_{OL} = 8 mA	—	0.4	V
I_{CC1}[4,5,6]	Active Power Supply Current	—	40	mA
I_{CC2}[4,7]	Standby Current	—	15	mA

NOTES:

1. Industrial temperature range product for the 7-5ns and 15ns speed grades are available as a standard device. All other speed grades are available by special order.
2. Measurements with 0.4 ≤ V_{IN} ≤ V_{CC}.
3. $\overline{OE}$ ≥ V_{IH}, 0.4 ≤ V_{OUT} ≤ V_{CC}.
4. Tested with outputs open (I_{OUT} = 0).
5. RCLK and WCLK toggle at 20 MHz and data inputs switch at 10 MHz.
6. Typical I_{CC1} = 4.2 + 1.4*fs + 0.002*C_L*fs (in mA) with V_{CC} = 3.3V, t_A = 25°C, fs = WCLK frequency = RCLK frequency (in MHz, using TTL levels), data switching at fs/2, C_L = capacitive load (in pF).
7. All Inputs = V_{CC} - 0.2V or GND + 0.2V, except RCLK and WCLK, which toggle at 20 MHz.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}[2]	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}[1,2]	Output Capacitance	V_{OUT} = 0V	10	pF

NOTES:

1. With output deselected, ($\overline{OE}$ ≥ V_{IH}).
2. Characterized values, not currently tested.

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AC ELECTRICAL CHARACTERISTICS[1] — SYNCHRONOUS TIMING

(Commercial: V_{CC} = 3.3V ± 0.15V, T_A = 0°C to +70°C;Industrial: V_{CC} = 3.3V ± 0.15V, T_A = -40°C to +85°C; JEDEC JESD8-A compliant)

		Commercial PBGA & TQFP		Com'l & Ind'l[2] PBGA & TQFP		Commercial TQFP Only		Com'l & Ind'l[2] TQFP Only		
		IDT72V3640L6 IDT72V3650L6 IDT72V3660L6 IDT72V3670L6 IDT72V3680L6 IDT72V3690L6		IDT72V3640L7-5 IDT72V3650L7-5 IDT72V3660L7-5 IDT72V3670L7-5 IDT72V3680L7-5 IDT72V3690L7-5		IDT72V3640L10 IDT72V3650L10 IDT72V3660L10 IDT72V3670L10 IDT72V3680L10 IDT72V3690L10		IDT72V3640L15 IDT72V3650L15 IDT72V3660L15 IDT72V3670L15 IDT72V3680L15 IDT72V3690L15		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
f_S	Clock Cycle Frequency	—	166	—	133.3	—	100	—	66.7	MHz
t_A	Data Access Time[5]	1	4	1[5]	5	1[5]	6.5	1[5]	10	ns
t_{CLK}	Clock Cycle Time	6	—	7.5	—	10	—	15	—	ns
t_{CLKH}	Clock High Time	2.7	—	3.5	—	4.5	—	6	—	ns
t_{CLKL}	Clock Low Time	2.7	—	3.5	—	4.5	—	6	—	ns
t_{DS}	Data Setup Time	2	—	2.5	—	3.5	—	4	—	ns
t_{DH}	Data Hold Time	0.5	—	0.5	—	0.5	—	1	—	ns
t_{ENS}	Enable Setup Time	2	—	2.5	—	3.5	—	4	—	ns
t_{ENH}	Enable Hold Time	0.5	—	0.5	—	0.5	—	1	—	ns
t_{LDS}	Load Setup Time	3	—	3.5	—	3.5	—	4	—	ns
t_{LDH}	Load Hold Time	0.5	—	0.5	—	0.5	—	1	—	ns
t_{RS}	Reset Pulse Width[3]	10	—	10	—	10	—	15	—	ns
t_{RSS}	Reset Setup Time	15	—	15	—	15	—	15	—	ns
t_{RSR}	Reset Recovery Time	10	—	10	—	10	—	15	—	ns
t_{RSF}	Reset to Flag and Output Time	—	15	—	15	—	15	—	15	ns
t_{RTS}	Retransmit Setup Time	3	—	3.5	—	3.5	—	4	—	ns
t_{OLZ}	Output Enable to Output in Low Z[4]	0	—	0	—	0	—	0	—	ns
t_{OE}	Output Enable to Output Valid[5]	1	4	1[5]	6	1[5]	6	1[5]	8	ns
t_{OHZ}	Output Enable to Output in High-Z[4,5]	1	4	1[5]	6	1[5]	6	1[5]	8	ns
t_{WFF}	Write Clock to $\overline{FF}$ or $\overline{IR}$	—	4	—	5	—	6.5	—	10	ns
t_{REF}	Read Clock to $\overline{EF}$ or $\overline{OR}$	—	4	—	5	—	6.5	—	10	ns
t_{PAFA}	Clock to Asynchronous Programmable Almost-Full Flag	—	10	—	12.5	—	16	—	20	ns
t_{PAFS}	Write Clock to Synchronous Programmable Almost-Full Flag	—	4	—	5	—	6.5	—	10	ns
t_{PAEA}	Clock to Asynchronous Programmable Almost-Empty Flag	—	10	—	12.5	—	16	—	20	ns
t_{PAES}	Read Clock to Synchronous Programmable Almost-Empty Flag	—	4	—	5	—	6.5	—	10	ns
t_{HF}	Clock to $\overline{HF}$	—	10	—	12.5	—	16	—	20	ns
t_{SKEW1}	Skew time between RCLK and WCLK for $\overline{EF}$/$\overline{OR}$ and $\overline{FF}$/$\overline{IR}$	4	—	5	—	7	—	9	—	ns
t_{SKEW2}	Skew time between RCLK and WCLK for $\overline{PAE}$ and $\overline{PAF}$	5	—	7	—	10	—	14	—	ns

NOTES:
1. All AC timings apply to both Standard IDT mode and First Word Fall Through mode.
2. Industrial temperature range product for 7-5ns and 15ns speed grades are available as standard device. All other speed grades are available by special order.
3. Pulse widths less than minimum values are not allowed.
4. Values guaranteed by design, not currently tested.
5. TQFP package only: for speed grades 7.5ns, 10ns and 15ns, the minimum for t_A, t_{OE}, and t_{OHZ} is 2ns.

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AC ELECTRICAL CHARACTERISTICS(1) — ASYNCHRONOUS TIMING

(Commercial: V_{CC} = 3.3V ± 0.15V, T_A = 0°C to +70°C;Industrial: V_{CC} = 3.3V ± 0.15V, T_A = -40°C to +85°C; JEDEC JESD8-A compliant)

		Commercial		Com'l & Ind'l		
		IDT72V3640L6 IDT72V3650L6 IDT72V3660L6 IDT72V3670L6 IDT72V3680L6 IDT72V3690L6		IDT72V3640L7-5 IDT72V3650L7-5 IDT72V3660L7-5 IDT72V3670L7-5 IDT72V3680L7-5 IDT72V3690L7-5		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
f_A(4)	Cycle Frequency (Asynchronous mode)	—	100	—	83	MHz
t_{AA}(4)	Data Access Time	0.6	8	0.6	10	ns
t_{CYC}(4)	Cycle Time	10	—	12	—	ns
t_{CYH}(4)	Cycle HIGH Time	4.5	—	5	—	ns
t_{CYL}(4)	Cycle LOW Time	4.5	—	5	—	ns
t_{RPE}(4)	Read Pulse after $\overline{EF}$ HIGH	8	—	10	—	ns
t_{FFA}(4)	Clock to Asynchronous $\overline{FF}$	—	8	—	10	ns
t_{EFA}(4)	Clock to Asynchronous $\overline{EF}$	—	8	—	10	ns
t_{PAFA}(4)	Clock to Asynchronous Programmable Almost-Full Flag	—	8	—	10	ns
t_{PAEA}(4)	Clock to Asynchronous Programmable Almost-Empty Flag	—	8	—	10	ns

NOTES:
1. All AC timings apply to both Standard IDT mode and First Word Fall Through mode.
2. Pulse widths less than minimum values are not allowed.
3. Values guaranteed by design, not currently tested.
4. Paramaeters apply to the PBGA package only.

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AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns[1]
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load for t_{CLK} = 10ns, 15 ns	See Figure 2a
Output Load for t_{CLK} = 6ns, 7.5ns	See Figure 2b & 2c

NOTE:
1. For 166MHz and 133MHz operation input rise/fall times are 1.5ns.

AC TEST LOADS - 6ns, 7.5ns Speed Grades

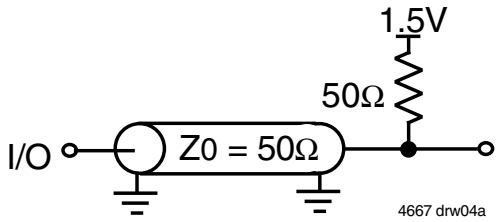


Figure 2b. AC Test Load

AC TEST LOADS - 10ns, 15ns Speed Grades

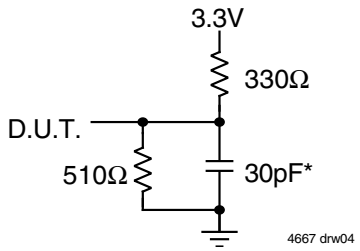


Figure 2a. Output Load
* Includes jig and scope capacitances.

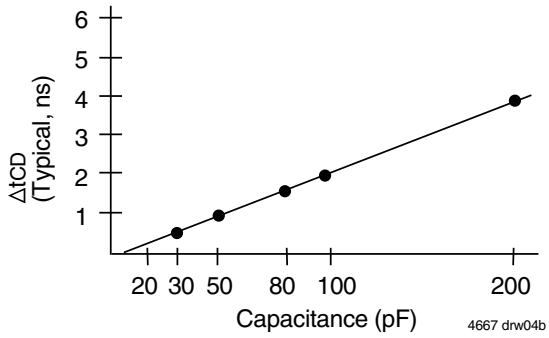
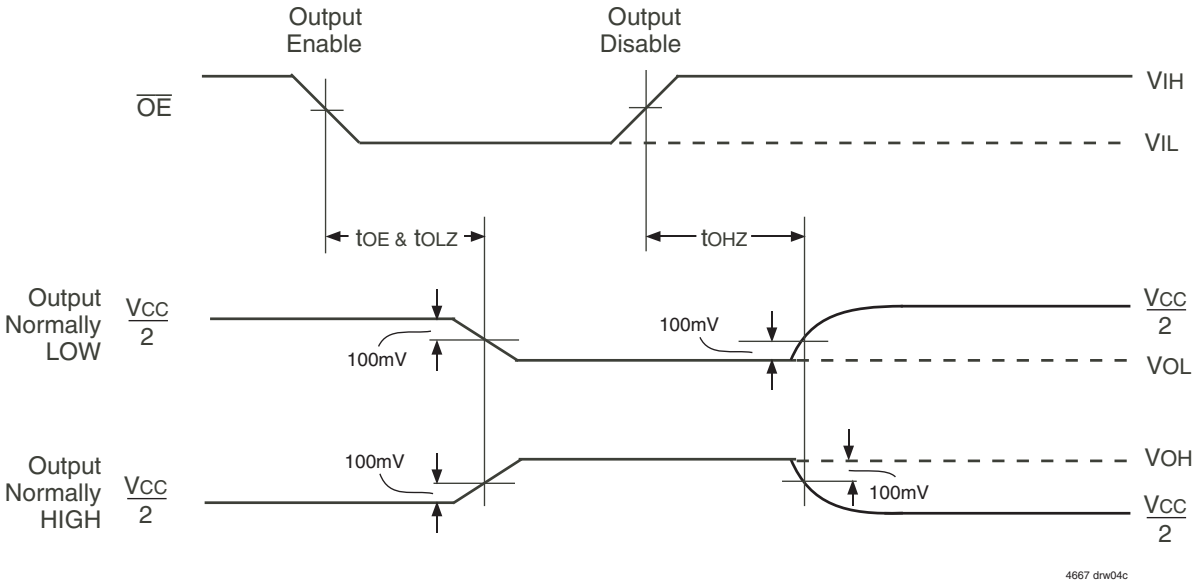


Figure 2c. Lumped Capacitive Load, Typical Derating

OUTPUT ENABLE & DISABLE TIMING



NOTE:
1. $\overline{REN}$ is HIGH.

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FUNCTIONAL DESCRIPTION

TIMING MODES: IDT STANDARD vs FIRST WORD FALL THROUGH (FWFT) MODE

The IDT72V3640/72V3650/72V3660/72V3670/72V3680/72V3690 support two different timing modes of operation: IDT Standard mode or First Word Fall Through (FWFT) mode. The selection of which mode will operate is determined during Master Reset, by the state of the FWFT/SI input.

If, at the time of Master Reset, FWFT/SI is LOW, then IDT Standard mode will be selected. This mode uses the Empty Flag ($\overline{EF}$) to indicate whether or not there are any words present in the FIFO. It also uses the Full Flag function ($\overline{FF}$) to indicate whether or not the FIFO has any free space for writing. In IDT Standard mode, every word read from the FIFO, including the first, must be requested using the Read Enable ($\overline{REN}$) and RCLK.

If, at the time of Master Reset, FWFT/SI is HIGH, then FWFT mode will be selected. This mode uses Output Ready ($\overline{OR}$) to indicate whether or not there is valid data at the data outputs (Q_n). It also uses Input Ready ($\overline{IR}$) to indicate whether or not the FIFO has any free space for writing. In the FWFT mode, the first word written to an empty FIFO goes directly to Q_n after three RCLK rising edges, $\overline{REN}$ = LOW is not necessary. Subsequent words must be accessed using the Read Enable ($\overline{REN}$) and RCLK.

Various signals, both input and output signals operate differently depending on which timing mode is in effect.

IDT STANDARD MODE

In this mode, the status flags, $\overline{FF}$, $\overline{PAF}$, $\overline{HF}$, $\overline{PAE}$, and $\overline{EF}$ operate in the manner outlined in Table 3. To write data into to the FIFO, Write Enable ($\overline{WEN}$) must be LOW. Data presented to the DATA IN lines will be clocked into the FIFO on subsequent transitions of the Write Clock (WCLK). After the first write is performed, the Empty Flag ($\overline{EF}$) will go HIGH. Subsequent writes will continue to fill up the FIFO. The Programmable Almost-Empty flag ($\overline{PAE}$) will go HIGH after n + 1 words have been loaded into the FIFO, where n is the empty offset value. The default setting for these values are stated in the footnote of Table 2. This parameter is also user programmable. See section on Programmable Flag Offset Loading.

If one continued to write data into the FIFO, and we assumed no read operations were taking place, the Half-Full flag ($\overline{HF}$) would toggle to LOW once the 513rd word for IDT72V3640, 1,025th word for IDT72V3650, 2,049th word for IDT72V3660, 4,097th word for IDT72V3670, 8,193th word for the IDT72V3680 and 16,385th word for the IDT72V3690, respectively was written into the FIFO. Continuing to write data into the FIFO will cause the Programmable Almost-Full flag ($\overline{PAF}$) to go LOW. Again, if no reads are performed, the $\overline{PAF}$ will go LOW after (1,024-m) writes for the IDT72V3640, (2,048-m) writes for the IDT72V3650, (4,096-m) writes for the IDT72V3660, (8,192-m) writes for the IDT72V3670, (16,384-m) writes for the IDT72V3680 and (32,768-m) writes for the IDT72V3690. The offset "m" is the full offset value. The default setting for these values are stated in the footnote of Table 2. This parameter is also user programmable. See section on Programmable Flag Offset Loading.

When the FIFO is full, the Full Flag ($\overline{FF}$) will go LOW, inhibiting further write operations. If no reads are performed after a reset, $\overline{FF}$ will go LOW after D writes to the FIFO. D = 1,024 writes for the IDT72V3640, 2,048 writes for the IDT72V3650, 4,096 writes for the IDT72V3660, 8,192 writes for the IDT72V3670, 16,384 writes for the IDT72V3680 and 32,768 writes for the IDT72V3690, respectively.

If the FIFO is full, the first read operation will cause $\overline{FF}$ to go HIGH. Subsequent read operations will cause $\overline{PAF}$ and $\overline{HF}$ to go HIGH at the conditions described in Table 3. If further read operations occur, without write operations, $\overline{PAE}$ will go LOW when there are n words in the FIFO, where n is the empty offset value. Continuing read operations will cause the FIFO to become empty. When the last word has been read from the FIFO, the $\overline{EF}$ will go LOW inhibiting further read operations. $\overline{REN}$ is ignored when the FIFO is empty.

When configured in IDT Standard mode, the $\overline{EF}$ and $\overline{FF}$ outputs are double register-buffered outputs.

Relevant timing diagrams for IDT Standard mode can be found in Figure 7,8,11 and 13.

FIRST WORD FALL THROUGH MODE (FWFT)

In this mode, the status flags, $\overline{IR}$, $\overline{PAF}$, $\overline{HF}$, $\overline{PAE}$, and $\overline{OR}$ operate in the manner outlined in Table 4. To write data into to the FIFO, $\overline{WEN}$ must be LOW. Data presented to the DATA IN lines will be clocked into the FIFO on subsequent transitions of WCLK. After the first write is performed, the Output Ready ($\overline{OR}$) flag will go LOW. Subsequent writes will continue to fill up the FIFO. $\overline{PAE}$ will go HIGH after n + 2 words have been loaded into the FIFO, where n is the empty offset value. The default setting for these values are stated in the footnote of Table 2. This parameter is also user programmable. See section on Programmable Flag Offset Loading.

If one continued to write data into the FIFO, and we assumed no read operations were taking place, the $\overline{HF}$ would toggle to LOW once the 514th word for the IDT72V3640, 1,026th word for the IDT72V3650, 2,050th word for the IDT72V3660, 4,098th word for the IDT72V3670, 8,194th word for the IDT72V3680, 16,386th word for the IDT72V3690, respectively was written into the FIFO. Continuing to write data into the FIFO will cause the $\overline{PAF}$ to go LOW. Again, if no reads are performed, the $\overline{PAF}$ will go LOW after (1,025-m) writes for the IDT72V3640, (2,049-m) writes for the IDT72V3650, (4,097-m) writes for the IDT72V3660 and (8,193-m) writes for the IDT72V3670, (16,385-m) writes for the IDT72V3680 and (32,769-m) writes for the IDT72V3690, where m is the full offset value. The default setting for these values are stated in the footnote of Table 2.

When the FIFO is full, the Input Ready ($\overline{IR}$) flag will go HIGH, inhibiting further write operations. If no reads are performed after a reset, $\overline{IR}$ will go HIGH after D writes to the FIFO. D = 1,025 writes for the IDT72V3640, 2,049 writes for the IDT72V3650, 4,097 writes for the IDT72V3660 and 8,193 writes for the IDT72V3670,16,385 writes for the IDT72V3680 and 32,769 writes for the IDT72V3690, respectively. Note that the additional word in FWFT mode is due to the capacity of the memory plus output register.

If the FIFO is full, the first read operation will cause the $\overline{IR}$ flag to go LOW. Subsequent read operations will cause the $\overline{PAF}$ and $\overline{HF}$ to go HIGH at the conditions described in Table 4. If further read operations occur, without write operations, the $\overline{PAE}$ will go LOW when there are n + 1 words in the FIFO, where n is the empty offset value. Continuing read operations will cause the FIFO to become empty. When the last word has been read from the FIFO, $\overline{OR}$ will go HIGH inhibiting further read operations. $\overline{REN}$ is ignored when the FIFO is empty.

When configured in FWFT mode, the $\overline{OR}$ flag output is triple register-buffered, and the $\overline{IR}$ flag output is double register-buffered.

Relevant timing diagrams for FWFT mode can be found in Figure 9, 10, 12, and 14.

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TABLE 2 — DEFAULT PROGRAMMABLE FLAG OFFSETS

IDT72V3640, 72V3650			
$\overline{LD}$	FSEL1	FSEL0	Offsets n,m
L	H	L	511
L	L	H	255
L	L	L	127
L	H	H	63
H	L	L	31
H	H	L	15
H	L	H	7
H	H	H	3
$\overline{LD}$	FSEL1	FSEL0	Program Mode
H	X	X	Serial(3)
L	X	X	Parallel(4)
IDT72V3660, 72V3670, 72V3680, 72V3690			
$\overline{LD}$	FSEL1	FSEL0	Offsets n,m
H	L	L	1,023
L	H	L	511
L	L	H	255
L	L	L	127
L	H	H	63
H	H	L	31
H	L	H	15
H	H	H	7
$\overline{LD}$	FSEL1	FSEL0	Program Mode
H	X	X	Serial(3)
L	X	X	Parallel(4)

NOTES:
1. n = empty offset for $\overline{PAE}$.
2. m = full offset for $\overline{PAF}$.
3. As well as selecting serial programming mode, one of the default values will also be loaded depending on the state of FSEL0 & FSEL1.
4. As well as selecting parallel programming mode, one of the default values will also be loaded depending on the state of FSEL0 & FSEL1.

PROGRAMMING FLAG OFFSETS

Full and Empty Flag offset values are user programmable. The IDT72V3640/72V3650/72V3660/72V3670/72V3680/72V3690 have internal registers for these offsets. There are eight default offset values selectable during Master Reset. These offset values are shown in Table 2. Offset values can also be programmed into the FIFO in one of two ways; serial or parallel loading method. The selection of the loading method is done using the $\overline{LD}$ (Load) pin. During Master Reset, the state of the $\overline{LD}$ input determines whether serial or parallel flag offset programming is enabled. A HIGH on $\overline{LD}$ during Master Reset selects serial loading of offset values. A LOW on $\overline{LD}$ during Master Reset selects parallel loading of offset values.

In addition to loading offset values into the FIFO, it is also possible to read the current offset values. Offset values can be read via the parallel output port Q_0-Qn, regardless of the programming mode selected (serial or parallel). It is not possible to read the offset values in serial fashion.

Figure 3, Programmable Flag Offset Programming Sequence, summaries the control pins and sequence for both serial and parallel programming modes. For a more detailed description, see discussion that follows.

The offset registers may be programmed (and reprogrammed) any time after Master Reset, regardless of whether serial or parallel programming has been selected. Valid programming ranges are from 0 to D-1.

SYNCHRONOUS vs ASYNCHRONOUS PROGRAMMABLE FLAG TIMING SELECTION

The IDT72V3640/72V3650/72V3660/72V3670/72V3680/72V3690 can be configured during the Master Reset cycle with either synchronous or asynchronous timing for $\overline{PAF}$ and $\overline{PAE}$ flags by use of the PFM pin.

If synchronous $\overline{PAF}$/$\overline{PAE}$ configuration is selected (PFM, HIGH during $\overline{MRS}$), the PAF is asserted and updated on the rising edge of WCLK only and not RCLK. Similarly, $\overline{PAE}$ is asserted and updated on the rising edge of RCLK only and not WCLK. For detail timing diagrams, see Figure 17 for synchronous $\overline{PAF}$ timing and Figure 18 for synchronous $\overline{PAE}$ timing.

If asynchronous $\overline{PAF}$/$\overline{PAE}$ configuration is selected (PFM, LOW during $\overline{MRS}$), the PAF is asserted LOW on the LOW-to-HIGH transition of WCLK and $\overline{PAF}$ is reset to HIGH on the LOW-to-HIGH transition of RCLK. Similarly, $\overline{PAE}$ is asserted LOW on the LOW-to-HIGH transition of RCLK. $\overline{PAE}$ is reset to HIGH on the LOW-to-HIGH transition of WCLK. For detail timing diagrams, see Figure 19 for asynchronous $\overline{PAF}$ timing and Figure 20 for asynchronous $\overline{PAE}$ timing.

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TABLE 3 — STATUS FLAGS FOR IDT STANDARD MODE

	IDT72V3640	IDT72V3650	IDT72V3660	$\overline{FF}$	$\overline{PAF}$	$\overline{HF}$	$\overline{PAE}$	$\overline{EF}$
Number of Words in FIFO	0	0	0	H	H	H	L	L
	1 to n[1]	1 to n[1]	1 to n[1]	H	H	H	L	H
	(n+1) to 512	(n+1) to 1,024	(n+1) to 2,048	H	H	H	H	H
	513 to (1,024-(m+1))	1,025 to (2,048-(m+1))	2,049 to (4,096-(m+1))	H	H	L	H	H
	(1,024-m) to 1,023	(2,048-m) to 2,047	(4,096m) to 4,095	H	L	L	H	H
	1,024	2,048	4,096	L	L	L	H	H

	IDT72V3670	IDT72V3680	IDT72V3690	$\overline{FF}$	$\overline{PAF}$	$\overline{HF}$	$\overline{PAE}$	$\overline{EF}$
Number of Words in FIFO	0	0	0	H	H	H	L	L
	1 to n[1]	1 to n[1]	1 to n[1]	H	H	H	L	H
	(n+1) to 4,096	(n+1) to 8,192	(n+1) to 16,384	H	H	H	H	H
	4,097 to (8,192-(m+1))	8,193 to (16,384-(m+1))	16,385 to (32,768-(m+1))	H	H	L	H	H
	(8,192-m) to 8,191	(16,384-m) to 16,383	(32,768-m) to 32,767	H	L	L	H	H
	8,192	16,384	32,768	L	L	L	H	H

NOTE:
1. See table 2 for values for n, m.

TABLE 4 — STATUS FLAGS FOR FWFT MODE

	IDT72V3640	IDT72V3650	IDT72V3660	$\overline{IR}$	$\overline{PAF}$	$\overline{HF}$	$\overline{PAE}$	$\overline{OR}$
Number of Words in FIFO	0	0	0	L	H	H	L	H
	1 to n+1	1 to n+1	1 to n+1	L	H	H	L	L
	(n+2) to 513	(n+2) to 1,025	(n+2) to 2,049	L	H	H	H	L
	514 to (1,025-(m+1))	1,026 to (2,049-(m+1))	2,050 to (4,097-(m+1))	L	H	L	H	L
	(1,025-m) to 1,024	(2,049-m) to 2,048	(4,097m) to 4,096	L	L	L	H	L
	1,025	2,049	4,097	H	L	L	H	L

	IDT72V3670	IDT72V3680	IDT72V3690	$\overline{IR}$	$\overline{PAF}$	$\overline{HF}$	$\overline{PAE}$	$\overline{OR}$
Number of Words in FIFO	0	0	0	L	H	H	L	H
	1 to n+1	1 to n+1	1 to n+1	L	H	H	L	L
	(n+2) to 4,097	(n+2) to 8,193	(n+2) to 16,385	L	H	H	H	L
	4,098 to (8,193(m+1))	8,194 to (16,385-(m+1))	16,386 to (32,769-(m+1))	L	H	L	H	L
	(8,194-m) to 8,192	(16,385-m) to 16,384	(32,769-m) to 32,768	L	L	L	H	L
	8,193	16,385	32,769	H	L	L	H	L

NOTE:
1. See table 2 for values for n, m.

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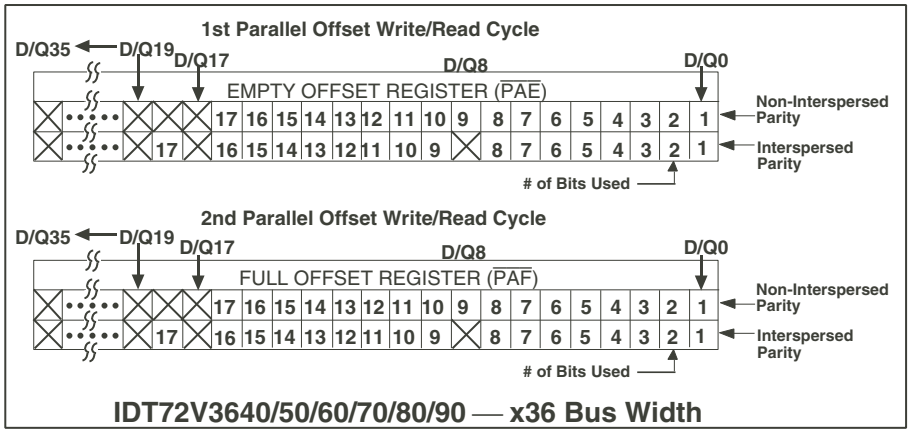
$\overline{LD}$	$\overline{WEN}$	$\overline{REN}$	$\overline{SEN}$	WCLK	RCLK	**IDT72V3640 IDT72V3650 IDT72V3660 IDT72V3670 IDT72V3680 IDT72V3690**
0	0	1	1	↑	X	Parallel write to registers: Empty Offset (LSB) Empty Offset (MSB) Full Offset (LSB) Full Offset (MSB)
0	1	0	1	X	↑	Parallel read from registers: Empty Offset (LSB) Empty Offset (MSB) Full Offset (LSB) Full Offset (MSB)
0	1	1	0	↑	X	Serial shift into registers: 20 bits for the 72V3640 22 bits for the 72V3650 24 bits for the 72V3660 26 bits for the 72V3670 28 bits for the 72V3680 30 bits for the 72V3690 1 bit for each rising WCLK edge Starting with Empty Offset (LSB) Ending with Full Offset (MSB)
X	1	1	1	X	X	No Operation
1	0	X	X	↑	X	Write Memory
1	X	0	X	X	↑	Read Memory
1	1	1	X	X	X	No Operation

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NOTES:
1. The programming method can only be selected at Master Reset.
2. Parallel reading of the offset registers is always permitted regardless of which programming method has been selected.
3. The programming sequence applies to both IDT Standard and FWFT modes.

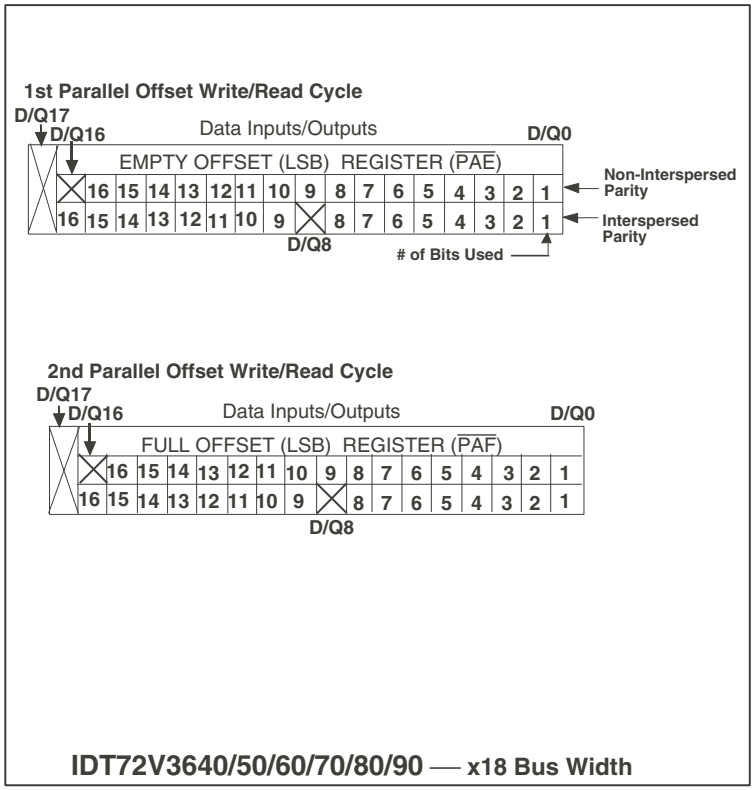
Figure 3. Programmable Flag Offset Programming Sequence

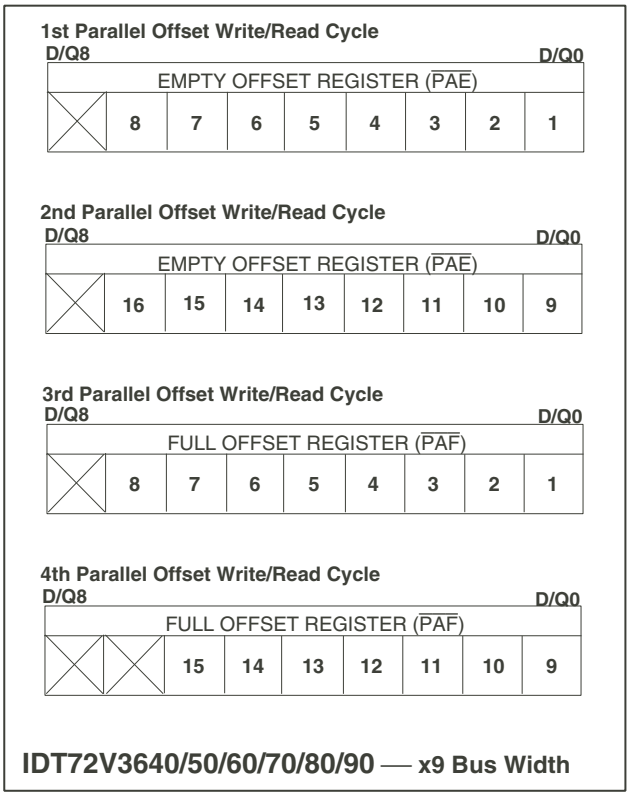
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# of Bits Used:
10 bits for the IDT72V3640
11 bits for the IDT72V3650
12 bits for the IDT72V3660
13 bits for the IDT72V3670
14 bits for the IDT72V3680
15 bits for the IDT72V3690

Note: All unused bits of the LSB & MSB are don't care





4667 drw07

Figure 3. Programmable Flag Offset Programming Sequence (Continued)

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SERIAL PROGRAMMING MODE

If Serial Programming mode has been selected, as described above, then programming of $\overline{PAE}$ and $\overline{PAF}$ values can be achieved by using a combination of the $\overline{LD}$, $\overline{SEN}$, WCLK and SI input pins. Programming $\overline{PAE}$ and $\overline{PAF}$ proceeds as follows: when $\overline{LD}$ and $\overline{SEN}$ are set LOW, data on the SI input are written, one bit for each WCLK rising edge, starting with the Empty Offset LSB and ending with the Full Offset MSB. A total of 20 bits for the IDT72V3640, 22 bits for the IDT72V3650, 24 bits for the IDT72V3660, 26 bits for the IDT72V3670, 28 bits for the IDT72V3680 and 30 bits for the IDT72V3690. See Figure 15, *Serial Loading of Programmable Flag Registers*, for the timing diagram for this mode.

Using the serial method, individual registers cannot be programmed selectively. $\overline{PAE}$ and $\overline{PAF}$ can show a valid status only after the complete set of bits (for all offset registers) has been entered. The registers can be reprogrammed as long as the complete set of new offset bits is entered. When $\overline{LD}$ is LOW and $\overline{SEN}$ is HIGH, no serial write to the registers can occur.

Write operations to the FIFO are allowed before and during the serial programming sequence. In this case, the programming of all offset bits does not have to occur at once. A select number of bits can be written to the SI input and then, by bringing $\overline{LD}$ and $\overline{SEN}$ HIGH, data can be written to FIFO memory via D_n by toggling $\overline{WEN}$. When $\overline{WEN}$ is brought HIGH with $\overline{LD}$ and $\overline{SEN}$ restored to a LOW, the next offset bit in sequence is written to the registers via SI. If an interruption of serial programming is desired, it is sufficient either to set $\overline{LD}$ LOW and deactivate $\overline{SEN}$ or to set $\overline{SEN}$ LOW and deactivate $\overline{LD}$. Once $\overline{LD}$ and $\overline{SEN}$ are both restored to a LOW level, serial offset programming continues.

From the time serial programming has begun, neither programmable flag will be valid until the full set of bits required to fill all the offset registers has been written. Measuring from the rising WCLK edge that achieves the above criteria; $\overline{PAF}$ will be valid after two more rising WCLK edges plus t_{PAF}, $\overline{PAE}$ will be valid after the next two rising RCLK edges plus t_{PAE} plus t_{SKEW2}.

It is only possible to read the flag offset values via the parallel output port Qn.

PARALLEL MODE

If Parallel Programming mode has been selected, as described above, then programming of $\overline{PAE}$ and $\overline{PAF}$ values can be achieved by using a combination of the $\overline{LD}$, WCLK , $\overline{WEN}$ and D_n input pins. Programming $\overline{PAE}$ and $\overline{PAF}$ proceeds as follows: $\overline{LD}$ and $\overline{WEN}$ must be set LOW. For x36 bit input bus width, data on the inputs D_n are written into the Empty Offset Register on the first LOW-to-HIGH transition of WCLK. Upon the second LOW-to-HIGH transition of WCLK, data are written into the Full Offset Register. The third transition of WCLK writes, once again, to the Empty Offset Register. For x18 bit input bus width, data on the inputs Dn are written into the Empty Offset Register LSB on the first LOW-to-HIGH transition of WCLK. Upon the 2nd LOW-to-HIGH transition of WCLK data are written into the Empty Offset Register MSB. The third transition of WCLK writes to the Full Offset Register LSB, the fourth transition of WCLK then writes to the Full Offset Register MSB. The fifth transition of WCLK writes once again to the Empty Offset Register LSB. A total of four writes to the offset registers is required to load values using a x18 input bus width. For an input bus width of x9 bits, a total of six write cycles to the offset registers is required to load values. See Figure 3, *Programmable Flag Offset Programming Sequence*. See Figure 16, *Parallel Loading of Programmable Flag Registers*, for the timing diagram for this mode.

The act of writing offsets in parallel employs a dedicated write offset register pointer. The act of reading offsets employs a dedicated read offset register pointer. The two pointers operate independently; however, a read and a write should not be performed simultaneously to the offset registers. A Master Reset initializes both pointers to the Empty Offset (LSB) register. A Partial Reset has no effect on the position of these pointers.

Write operations to the FIFO are allowed before and during the parallel programming sequence. In this case, the programming of all offset registers does not have to occur at one time. One, two or more offset registers can be written and then by bringing $\overline{LD}$ HIGH, write operations can be redirected to the FIFO memory. When $\overline{LD}$ is set LOW again, and $\overline{WEN}$ is LOW, the next offset register in sequence is written to. As an alternative to holding $\overline{WEN}$ LOW and toggling $\overline{LD}$, parallel programming can also be interrupted by setting $\overline{LD}$ LOW and toggling $\overline{WEN}$.

Note that the status of a programmable flag ($\overline{PAE}$ or $\overline{PAF}$) output is invalid during the programming process. From the time parallel programming has begun, a programmable flag output will not be valid until the appropriate offset word has been written to the register(s) pertaining to that flag. Measuring from the rising WCLK edge that achieves the above criteria; $\overline{PAF}$ will be valid after two more rising WCLK edges plus t_{PAF}, $\overline{PAE}$ will be valid after the next two rising RCLK edges plus t_{PAE} plus t_{SKEW2}.

The act of reading the offset registers employs a dedicated read offset register pointer. The contents of the offset registers can be read on the Q_0-Q_n pins when $\overline{LD}$ is set LOW and $\overline{REN}$ is set LOW. For x36 output bus width, data are read via Q_n from the Empty Offset Register on the first LOW-to-HIGH transition of RCLK. Upon the second LOW-to-HIGH transition of RCLK, data are read from the Full Offset Register. The third transition of RCLK reads, once again, from the Empty Offset Register. For x18 output bus width, a total of four read cycles are required to obtain the values of the offset registers. Starting with the Empty Offset Register LSB and finishing with the Full Offset Register MSB. For x9 output bus width, a total of six read cycles must be performed on the offset registers. See Figure 3, *Programmable Flag Offset Programming Sequence*. See Figure 17, *Parallel Read of Programmable Flag Registers*, for the timing diagram for this mode.

It is permissible to interrupt the offset register read sequence with reads or writes to the FIFO. The interruption is accomplished by deasserting $\overline{REN}$, $\overline{LD}$, or both together. When $\overline{REN}$ and $\overline{LD}$ are restored to a LOW level, reading of the offset registers continues where it left off. It should be noted, and care should be taken from the fact that when a parallel read of the flag offsets is performed, the data word that was present on the output lines Qn will be overwritten.

Parallel reading of the offset registers is always permitted regardless of which timing mode (IDT Standard or FWFT modes) has been selected.

RETRANSMIT OPERATION

The Retransmit operation allows data that has already been read to be accessed again. There are 2 modes of Retransmit operation, normal latency and zero latency. There are two stages to Retransmit: first, a setup procedure that resets the read pointer to the first location of memory, then the actual retransmit, which consists of reading out the memory contents, starting at the beginning of memory.

Retransmit setup is initiated by holding $\overline{RT}$ LOW during a rising RCLK edge. $\overline{REN}$ and $\overline{WEN}$ must be HIGH before bringing $\overline{RT}$ LOW. When zero latency is utilized, $\overline{REN}$ does not need to be HIGH before bringing $\overline{RT}$ LOW. At least two words, but no more than D - 2 words should have been written into the FIFO, and read from the FIFO, between Reset (Master or Partial) and the time of Retransmit setup. D = 1,024 for the IDT72V3640, 2,048 for the IDT72V3650, 4,096 for the IDT72V3660, 8,192 for the IDT72V3670, 16,384 for the IDT72V3680 and 32,768 for the IDT72V3690. In FWFT mode, D = 1,025 for the IDT72V2640, 2,049 for the IDT72V3650, 4,097 for the IDT72V3660, 8,193 for the IDT72V3670, 16,385 for the IDT72V3680 and 32,769 for the IDT72V3690.

If IDT Standard mode is selected, the FIFO will mark the beginning of the Retransmit setup by setting $\overline{EF}$ LOW. The change in level will only be noticeable

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if $\overline{EF}$ was HIGH before setup. During this period, the internal read pointer is initialized to the first location of the RAM array.

When $\overline{EF}$ goes HIGH, Retransmit setup is complete and read operations may begin starting with the first location in memory. Since IDT Standard mode is selected, every word read including the first word following Retransmit setup requires a LOW on $\overline{REN}$ to enable the rising edge of RCLK. See Figure 11, *Retransmit Timing (IDT Standard Mode)*, for the relevant timing diagram.

If FWFT mode is selected, the FIFO will mark the beginning of the Retransmit setup by setting $\overline{OR}$ HIGH. During this period, the internal read pointer is set to the first location of the RAM array.

When $\overline{OR}$ goes LOW, Retransmit setup is complete; at the same time, the contents of the first location appear on the outputs. Since FWFT mode is selected, the first word appears on the outputs, no LOW on $\overline{REN}$ is necessary. Reading all subsequent words requires a LOW on $\overline{REN}$ to enable the rising edge of RCLK. See Figure 12, *Retransmit Timing (FWFT Mode)*, for the relevant timing diagram.

For either IDT Standard mode or FWFT mode, updating of the $\overline{PAE}$, $\overline{HF}$ and $\overline{PAF}$ flags begin with the rising edge of RCLK that $\overline{RT}$ is setup. $\overline{PAE}$ is synchronized to RCLK, thus on the second rising edge of RCLK after $\overline{RT}$ is setup, the $\overline{PAE}$ flag will be updated. $\overline{HF}$ is asynchronous, thus the rising edge of RCLK that $\overline{RT}$ is setup will update $\overline{HF}$. $\overline{PAF}$ is synchronized to WCLK, thus the second rising edge of WCLK that occurs t_{SKEW} after the rising edge of RCLK that $\overline{RT}$ is setup will update $\overline{PAF}$. $\overline{RT}$ is synchronized to RCLK.

The Retransmit function has the option of two modes of operation, either “normal latency” or “zero latency”. Figure 11 and Figure 12 mentioned previously, relate to “normal latency”. Figure 13 and Figure 14 show “zero latency” retransmit operation. Zero latency basically means that the first data word to be retransmitted, is placed onto the output register with respect to the RCLK pulse that initiated the retransmit.

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SIGNAL DESCRIPTION

INPUTS:

DATA IN (D_0 - D_n)

Data inputs for 36-bit wide data (D_0 - D_{35}), data inputs for 18-bit wide data (D_0 - D_{17}) or data inputs for 9-bit wide data (D_0 - D_8).

CONTROLS:

MASTER RESET ($\overline{MRS}$)

A Master Reset is accomplished whenever the $\overline{MRS}$ input is taken to a LOW state. This operation sets the internal read and write pointers to the first location of the RAM array. $\overline{PAE}$ will go LOW, $\overline{PAF}$ will go HIGH, and $\overline{HF}$ will go HIGH.

If FWFT/SI is LOW during Master Reset then the IDT Standard mode, along with $\overline{EF}$ and $\overline{FF}$ are selected. $\overline{EF}$ will go LOW and $\overline{FF}$ will go HIGH. If FWFT/SI is HIGH, then the First Word Fall Through mode (FWFT), along with $\overline{IR}$ and $\overline{OR}$, are selected. $\overline{OR}$ will go HIGH and $\overline{IR}$ will go LOW.

All control settings such as OW, IW, BM, $\overline{BE}$, RM, PFM and IP are defined during the Master Reset cycle.

During a Master Reset, the output register is initialized to all zeroes. A Master Reset is required after power up, before a write operation can take place. $\overline{MRS}$ is asynchronous.

See Figure 5, *Master Reset Timing*, for the relevant timing diagram.

PARTIAL RESET ($\overline{PRS}$)

A Partial Reset is accomplished whenever the $\overline{PRS}$ input is taken to a LOW state. As in the case of the Master Reset, the internal read and write pointers are set to the first location of the RAM array, $\overline{PAE}$ goes LOW, $\overline{PAF}$ goes HIGH, and $\overline{HF}$ goes HIGH.

Whichever mode is active at the time of Partial Reset, IDT Standard mode or First Word Fall Through, that mode will remain selected. If the IDT Standard mode is active, then $\overline{FF}$ will go HIGH and $\overline{EF}$ will go LOW. If the First Word Fall Through mode is active, then $\overline{OR}$ will go HIGH, and $\overline{IR}$ will go LOW.

Following Partial Reset, all values held in the offset registers remain unchanged. The programming method (parallel or serial) currently active at the time of Partial Reset is also retained. The output register is initialized to all zeroes. $\overline{PRS}$ is asynchronous.

A Partial Reset is useful for resetting the device during the course of operation, when reprogramming programmable flag offset settings may not be convenient.

See Figure 6, *Partial Reset Timing*, for the relevant timing diagram.

ASYNCHRONOUS WRITE ($\overline{ASYW}$)

The write port can be configured for either Synchronous or Asynchronous mode of operation. If during Master Reset the $\overline{ASYW}$ input is LOW, then Asynchronous operation of the write port will be selected. During Asynchronous operation of the write port the WCLK input becomes WR input, this is the Asynchronous write strobe input. A rising edge on WR will write data present on the Dn inputs into the FIFO. ($\overline{WEN}$ must be tied LOW when using the write port in Asynchronous mode).

When the write port is configured for Asynchronous operation the full flag ($\overline{FF}$) operates in an asynchronous manner, that is, the full flag will be updated based in both a write operation and read operation. Note, if Asynchronous mode is selected, FWFT is not permissable. Refer to Figures 23, 24, 27 and 28 for relevant timing and operational waveforms.

ASYNCHRONOUS READ ($\overline{ASYR}$)

The read port can be configured for either Synchronous or Asynchronous mode of operation. If during a Master Reset the $\overline{ASYR}$ input is LOW, then Asynchronous operation of the read port will be selected. During Asynchronous operation of the read port the RCLK input becomes RD input, this is the Asynchronous read strobe input. A rising edge on RD will read data from the FIFO via the output register and Qn port. ($\overline{REN}$ must be tied LOW during Asynchronous operation of the read port).

The $\overline{OE}$ input provides three-state control of the Qn output bus, in an asynchronous manner.

When the read port is configured for Asynchronous operation the device must be operating on IDT standard mode, FWFT mode is not permissible if the read port is Asynchronous. The Empty Flag ($\overline{EF}$) operates in an Asynchronous manner, that is, the empty flag will be updated based on both a read operation and a write operation. Refer to figures 25, 26, 27 and 28 for relevant timing and operational waveforms.

RETRANSMIT ($\overline{RT}$)

The Retransmit operation allows data that has already been read to be accessed again. There are 2 modes of Retransmit operation, normal latency and zero latency. There are two stages to Retransmit: first, a setup procedure that resets the read pointer to the first location of memory, then the actual retransmit, which consists of reading out the memory contents, starting at the beginning of the memory.

Retransmit setup is initiated by holding $\overline{RT}$ LOW during a rising RCLK edge. $\overline{REN}$ and $\overline{WEN}$ must be HIGH before bringing $\overline{RT}$ LOW. When zero latency is utilized, $\overline{REN}$ does not need to be HIGH before bringing $\overline{RT}$ LOW.

If IDT Standard mode is selected, the FIFO will mark the beginning of the Retransmit setup by setting $\overline{EF}$ LOW. The change in level will only be noticeable if $\overline{EF}$ was HIGH before setup. During this period, the internal read pointer is initialized to the first location of the RAM array.

When $\overline{EF}$ goes HIGH, Retransmit setup is complete and read operations may begin starting with the first location in memory. Since IDT Standard mode is selected, every word read including the first word following Retransmit setup requires a LOW on $\overline{REN}$ to enable the rising edge of RCLK. See Figure 11, *Retransmit Timing (IDT Standard Mode)*, for the relevant timing diagram.

If FWFT mode is selected, the FIFO will mark the beginning of the Retransmit setup by setting $\overline{OR}$ HIGH. During this period, the internal read pointer is set to the first location of the RAM array.

When $\overline{OR}$ goes LOW, Retransmit setup is complete; at the same time, the contents of the first location appear on the outputs. Since FWFT mode is selected, the first word appears on the outputs, no LOW on $\overline{REN}$ is necessary. Reading all subsequent words requires a LOW on $\overline{REN}$ to enable the rising edge of RCLK. See Figure 12, *Retransmit Timing (FWFT Mode)*, for the relevant timing diagram.

In Retransmit operation, zero latency mode can be selected using the Retransmit Mode (RM) pin during a Master Reset. This can be applied to both IDT Standard mode and FWFT mode.

FIRST WORD FALL THROUGH/SERIAL IN (FWFT/SI)

This is a dual purpose pin. During Master Reset, the state of the FWFT/SI input determines whether the device will operate in IDT Standard mode or First Word Fall Through (FWFT) mode.

If, at the time of Master Reset, FWFT/SI is LOW, then IDT Standard mode will be selected. This mode uses the Empty Flag ($\overline{EF}$) to indicate whether or

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not there are any words present in the FIFO memory. It also uses the Full Flag function ($\overline{FF}$) to indicate whether or not the FIFO memory has any free space for writing. In IDT Standard mode, every word read from the FIFO, including the first, must be requested using the Read Enable ($\overline{REN}$) and RCLK.

If, at the time of Master Reset, FWFT/SI is HIGH, then FWFT mode will be selected. This mode uses Output Ready ($\overline{OR}$) to indicate whether or not there is valid data at the data outputs (Q_n). It also uses Input Ready ($\overline{IR}$) to indicate whether or not the FIFO memory has any free space for writing. In the FWFT mode, the first word written to an empty FIFO goes directly to Q_n after three RCLK rising edges, $\overline{REN}$ = LOW is not necessary. Subsequent words must be accessed using the Read Enable ($\overline{REN}$) and RCLK.

After Master Reset, FWFT/SI acts as a serial input for loading $\overline{PAE}$ and $\overline{PAF}$ offsets into the programmable registers. The serial input function can only be used when the serial loading method has been selected during Master Reset. Serial programming using the FWFT/SI pin functions the same way in both IDT Standard and FWFT modes.

WRITE STROBE & WRITE CLOCK (WR/WCLK)

If Synchronous operation of the write port has been selected via $\overline{ASYW}$, this input behaves as WCLK.

A write cycle is initiated on the rising edge of the WCLK input. Data setup and hold times must be met with respect to the LOW-to-HIGH transition of the WCLK. It is permissible to stop the WCLK. Note that while WCLK is idle, the $\overline{FF}$/$\overline{IR}$, $\overline{PAF}$ and $\overline{HF}$ flags will not be updated. (Note that WCLK is only capable of updating $\overline{HF}$ flag to LOW). The Write and Read Clocks can either be independent or coincident.

If Asynchronous operation has been selected this input is WR (write strobe). Data is Asynchronously written into the FIFO via the Dn inputs whenever there is a rising edge on WR. In this mode the WEN input must be tied LOW.

WRITE ENABLE ($\overline{WEN}$)

When the $\overline{WEN}$ input is LOW, data may be loaded into the FIFO RAM array on the rising edge of every WCLK cycle if the device is not full. Data is stored in the RAM array sequentially and independently of any ongoing read operation.

When $\overline{WEN}$ is HIGH, no new data is written in the RAM array on each WCLK cycle.

To prevent data overflow in the IDT Standard mode, $\overline{FF}$ will go LOW, inhibiting further write operations. Upon the completion of a valid read cycle, $\overline{FF}$ will go HIGH allowing a write to occur. The $\overline{FF}$ is updated by two WCLK cycles + t_{SKEW} after the RCLK cycle.

To prevent data overflow in the FWFT mode, $\overline{IR}$ will go HIGH, inhibiting further write operations. Upon the completion of a valid read cycle, $\overline{IR}$ will go LOW allowing a write to occur. The $\overline{IR}$ flag is updated by two WCLK cycles + t_{SKEW} after the valid RCLK cycle.

$\overline{WEN}$ is ignored when the FIFO is full in either FWFT or IDT Standard mode.

If Asynchronous operation of the write port has been selected, then $\overline{WEN}$ must be held active, (tied LOW).

READ STROBE & READ CLOCK (RD/RCLK)

If Synchronous operation of the read port has been selected via $\overline{ASYR}$, this input behaves as RCLK. A read cycle is initiated on the rising edge of the RCLK input. Data can be read on the outputs, on the rising edge of the RCLK input. It is permissible to stop the RCLK. Note that while RCLK is idle, the $\overline{EF}$/$\overline{OR}$, $\overline{PAE}$ and $\overline{HF}$ flags will not be updated. (Note that RCLK is only capable of updating the $\overline{HF}$ flag to HIGH). The Write and Read Clocks can be independent or coincident.

If Asynchronous operation has been selected this input is RD (Read Strobe) . Data is Asynchronously read from the FIFO via the output register whenever there is a rising edge on RD. In this mode the $\overline{REN}$ input must be tied LOW. The $\overline{OE}$ input is used to provide Asynchronous control of the three-state Qn outputs.

READ ENABLE ($\overline{REN}$)

When Read Enable is LOW, data is loaded from the RAM array into the output register on the rising edge of every RCLK cycle if the device is not empty.

When the $\overline{REN}$ input is HIGH, the output register holds the previous data and no new data is loaded into the output register. The data outputs Q_0-Q_n maintain the previous data value.

In the IDT Standard mode, every word accessed at Q_n, including the first word written to an empty FIFO, must be requested using $\overline{REN}$. When the last word has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go LOW, inhibiting further read operations. $\overline{REN}$ is ignored when the FIFO is empty. Once a write is performed, $\overline{EF}$ will go HIGH allowing a read to occur. The $\overline{EF}$ flag is updated by two RCLK cycles + t_{SKEW} after the valid WCLK cycle.

In the FWFT mode, the first word written to an empty FIFO automatically goes to the outputs Q_n, on the third valid LOW-to-HIGH transition of RCLK + t_{SKEW} after the first write. $\overline{REN}$ does not need to be asserted LOW. In order to access all other words, a read must be executed using $\overline{REN}$. The RCLK LOW-to-HIGH transition after the last word has been read from the FIFO, Output Ready ($\overline{OR}$) will go HIGH with a true read (RCLK with $\overline{REN}$ = LOW), inhibiting further read operations. $\overline{REN}$ is ignored when the FIFO is empty.

If Asynchronous operation of the Read port has been selected, then $\overline{REN}$ must be held active, (tied LOW).

SERIAL ENABLE ($\overline{SEN}$)

The $\overline{SEN}$ input is an enable used only for serial programming of the offset registers. The serial programming method must be selected during Master Reset. $\overline{SEN}$ is always used in conjunction with $\overline{LD}$. When these lines are both LOW, data at the SI input can be loaded into the program register one bit for each LOW-to-HIGH transition of WCLK.

When $\overline{SEN}$ is HIGH, the programmable registers retains the previous settings and no offsets are loaded. $\overline{SEN}$ functions the same way in both IDT Standard and FWFT modes.

OUTPUT ENABLE ($\overline{OE}$)

When Output Enable is enabled (LOW), the parallel output buffers receive data from the output register. When $\overline{OE}$ is HIGH, the output data bus (Q_n) goes into a high impedance state.

LOAD ($\overline{LD}$)

This is a dual purpose pin. During Master Reset, the state of the $\overline{LD}$ input, along with FSEL0 and FSEL1, determines one of eight default offset values for the $\overline{PAE}$ and $\overline{PAF}$ flags, along with the method by which these offset registers can be programmed, parallel or serial (see Table 2). After Master Reset, $\overline{LD}$ enables write operations to and read operations from the offset registers. Only the offset loading method currently selected can be used to write to the registers. Offset registers can be read only in parallel.

After Master Reset, the $\overline{LD}$ pin is used to activate the programming process of the flag offset values $\overline{PAE}$ and $\overline{PAF}$. Pulling $\overline{LD}$ LOW will begin a serial loading or parallel load or read of these offset values.

BUS-MATCHING (BM, IW, OW)

The pins BM, IW and OW are used to define the input and output bus widths. During Master Reset, the state of these pins is used to configure the device bus sizes. See Table 1 for control settings. All flags will operate on the word/byte size boundary as defined by the selection of bus width. See Figure 4 for *Bus-Matching Byte Arrangement*.

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BIG-ENDIAN/LITTLE-ENDIAN ($\overline{BE}$)

During Master Reset, a LOW on $\overline{BE}$ will select Big-Endian operation. A HIGH on $\overline{BE}$ during Master Reset will select Little-Endian format. This function is useful when the following input to output bus widths are implemented: x36 to x18, x36 to x9, x18 to x36 and x9 to x36. If Big-Endian mode is selected, then the most significant byte (word) of the long word written into the FIFO will be read out of the FIFO first, followed by the least significant byte. If Little-Endian format is selected, then the least significant byte of the long word written into the FIFO will be read out first, followed by the most significant byte. The mode desired is configured during master reset by the state of the Big-Endian ($\overline{BE}$) pin. See Figure 4 for *Bus-Matching Byte Arrangement*.

PROGRAMMABLE FLAG MODE (PFM)

During Master Reset, a LOW on PFM will select Asynchronous Programmable flag timing mode. A HIGH on PFM will select Synchronous Programmable flag timing mode. If asynchronous $\overline{PAF}$/$\overline{PAE}$ configuration is selected (PFM, LOW during $\overline{MRS}$), the $\overline{PAE}$ is asserted LOW on the LOW-to-HIGH transition of RCLK. $\overline{PAE}$ is reset to HIGH on the LOW-to-HIGH transition of WCLK. Similarly, the $\overline{PAF}$ is asserted LOW on the LOW-to-HIGH transition of WCLK and $\overline{PAF}$ is reset to HIGH on the LOW-to-HIGH transition of RCLK.

If synchronous $\overline{PAE}$/$\overline{PAF}$ configuration is selected (PFM, HIGH during MRS) , the $\overline{PAE}$ is asserted and updated on the rising edge of RCLK only and not WCLK. Similarly, $\overline{PAF}$ is asserted and updated on the rising edge of WCLK only and not RCLK. The mode desired is configured during master reset by the state of the Programmable Flag Mode (PFM) pin.

INTERSPERSED PARITY (IP)

During Master Reset, a LOW on IP will select Non-Interspersed Parity mode. A HIGH will select Interspersed Parity mode. The IP bit function allows the user to select the parity bit in the word loaded into the parallel port (D_0-Dn) when programming the flag offsets. If Interspersed Parity mode is selected, then the FIFO will assume that the parity bits are located in bit position D_8, D_{17}, D_{26} and D_{35} during the parallel programming of the flag offsets. If Non-Interspersed Parity mode is selected, then D_8, D_{17} and D_{28} are is assumed to be valid bits and D_{32}, D_{33}, D_{34} and D_{35} are ignored. IP mode is selected during Master Reset by the state of the IP input pin. Interspersed Parity control only has an effect during parallel programming of the offset registers. It does not effect the data written to and read from the FIFO.

OUTPUTS:

FULL FLAG ($\overline{FF}$/$\overline{IR}$)

This is a dual purpose pin. In IDT Standard mode, the Full Flag ($\overline{FF}$) function is selected. When the FIFO is full, $\overline{FF}$ will go LOW, inhibiting further write operations. When $\overline{FF}$ is HIGH, the FIFO is not full. If no reads are performed after a reset (either $\overline{MRS}$ or $\overline{PRS}$), $\overline{FF}$ will go LOW after D writes to the FIFO (D = 1,024 for the IDT72V3640, 2,048 for the IDT72V3650, 4,096 for the IDT72V3660, 8,192 for the IDT72V3670, 16,384 for the IDT72V3680 and 32,768 for the IDT72V3690. See Figure 7, *Write Cycle and Full Flag Timing (IDT Standard Mode)*, for the relevant timing information.

In FWFT mode, the Input Ready ($\overline{IR}$) function is selected. $\overline{IR}$ goes LOW when memory space is available for writing in data. When there is no longer any free space left, $\overline{IR}$ goes HIGH, inhibiting further write operations. If no reads are performed after a reset (either $\overline{MRS}$ or $\overline{PRS}$), $\overline{IR}$ will go HIGH after D writes to the FIFO (D = 1,025 for the IDT72V3640, 2,049 for the IDT72V3650, 4,097 for the IDT72V3660, 8,193 for the IDT72V3670, 16,385 for the IDT72V3680 and 32,769 for the IDT72V3690. See Figure 9, *Write Timing (FWFT Mode)*, for the relevant timing information.

The $\overline{IR}$ status not only measures the contents of the FIFO memory, but also counts the presence of a word in the output register. Thus, in FWFT mode, the total number of writes necessary to deassert $\overline{IR}$ is one greater than needed to assert $\overline{FF}$ in IDT Standard mode.

$\overline{FF}$/$\overline{IR}$ is synchronous and updated on the rising edge of WCLK. $\overline{FF}$/$\overline{IR}$ are double register-buffered outputs.

EMPTY FLAG ($\overline{EF}$/$\overline{OR}$)

This is a dual purpose pin. In the IDT Standard mode, the Empty Flag ($\overline{EF}$) function is selected. When the FIFO is empty, $\overline{EF}$ will go LOW, inhibiting further read operations. When $\overline{EF}$ is HIGH, the FIFO is not empty. See Figure 8, *Read Cycle, Empty Flag and First Word Latency Timing (IDT Standard Mode)*, for the relevant timing information.

In FWFT mode, the Output Ready ($\overline{OR}$) function is selected. $\overline{OR}$ goes LOW at the same time that the first word written to an empty FIFO appears valid on the outputs. $\overline{OR}$ stays LOW after the RCLK LOW to HIGH transition that shifts the last word from the FIFO memory to the outputs. $\overline{OR}$ goes HIGH only with a true read (RCLK with $\overline{REN}$ = LOW). The previous data stays at the outputs, indicating the last word was read. Further data reads are inhibited until $\overline{OR}$ goes LOW again. See Figure 10, *Read Timing (FWFT Mode)*, for the relevant timing information.

$\overline{EF}$/$\overline{OR}$ is synchronous and updated on the rising edge of RCLK.

In IDT Standard mode, $\overline{EF}$ is a double register-buffered output. In FWFT mode, $\overline{OR}$ is a triple register-buffered output.

PROGRAMMABLE ALMOST-FULL FLAG ($\overline{PAF}$)

The Programmable Almost-Full flag ($\overline{PAF}$) will go LOW when the FIFO reaches the almost-full condition. In IDT Standard mode, if no reads are performed after reset ($\overline{MRS}$), $\overline{PAF}$ will go LOW after (D - m) words are written to the FIFO. The $\overline{PAF}$ will go LOW after (1,024-m) writes for the IDT72V3640, (2,048-m) writes for the IDT72V3650, (4,096-m) writes for the IDT72V3660, (8,192-m) writes for the IDT72V3670, (16,384-m) writes for the IDT72V3680 and (32,768-m) writes for the IDT72V3690. The offset "m" is the full offset value. The default setting for this value is stated in the footnote of Table 1.

In FWFT mode, the $\overline{PAF}$ will go LOW after (1,025-m) writes for the IDT72V3640, (2,049-m) writes for the IDT72V3650, (4,097-m) writes for the IDT72V3660 and (8,193-m) writes for the IDT72V3670, (16,385-m) writes for the IDT72V3680 and (32,769-m) writes for the IDT72V3690, where m is the full offset value. The default setting for this value is stated in Table 2.

See Figure 18, *Synchronous Programmable Almost-Full Flag Timing (IDT Standard and FWFT Mode)*, for the relevant timing information.

If asynchronous $\overline{PAF}$ configuration is selected, the $\overline{PAF}$ is asserted LOW on the LOW-to-HIGH transition of the Write Clock (WCLK). $\overline{PAF}$ is reset to HIGH on the LOW-to-HIGH transition of the Read Clock (RCLK). If synchronous $\overline{PAF}$ configuration is selected, the $\overline{PAF}$ is updated on the rising edge of WCLK. See Figure 20, *Asynchronous Almost-Full Flag Timing (IDT Standard and FWFT Mode)*.

PROGRAMMABLE ALMOST-EMPTY FLAG ($\overline{PAE}$)

The Programmable Almost-Empty flag ($\overline{PAE}$) will go LOW when the FIFO reaches the almost-empty condition. In IDT Standard mode, $\overline{PAE}$ will go LOW when there are n words or less in the FIFO. The offset "n" is the empty offset value. The default setting for this value is stated in the footnote of Table 1.

In FWFT mode, the $\overline{PAE}$ will go LOW when there are n+1 words or less in the FIFO. The default setting for this value is stated in Table 2.

See Figure 19, *Synchronous Programmable Almost-Empty Flag Timing (IDT Standard and FWFT Mode)*, for the relevant timing information.

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If asynchronous $\overline{PAE}$ configuration is selected, the $\overline{PAE}$ is asserted LOW on the LOW-to-HIGH transition of the Read Clock (RCLK). $\overline{PAE}$ is reset to HIGH on the LOW-to-HIGH transition of the Write Clock (WCLK). If synchronous $\overline{PAE}$ configuration is selected, the $\overline{PAE}$ is updated on the rising edge of RCLK. See Figure 21, *Asynchronous Programmable Almost-Empty Flag Timing (IDT Standard and FWFT Mode)*.

HALF-FULL FLAG ($\overline{HF}$)

This output indicates a half-full FIFO. The rising WCLK edge that fills the FIFO beyond half-full sets $\overline{HF}$ LOW. The flag remains LOW until the difference between the write and read pointers becomes less than or equal to half of the total depth of the device; the rising RCLK edge that accomplishes this condition sets $\overline{HF}$ HIGH.

In IDT Standard mode, if no reads are performed after reset ($\overline{MRS}$ or $\overline{PRS}$), $\overline{HF}$ will go LOW after (D/2 + 1) writes to the FIFO, where D = 1,024 for the IDT72V3640, 2,048 for the IDT72V3650, 4,096 for the IDT72V3660, 8,192 for the IDT72V3670, 16,384 for the IDT72V3680 and 32,768 for the IDT72V3690.

In FWFT mode, if no reads are performed after reset ($\overline{MRS}$ or $\overline{PRS}$), $\overline{HF}$ will go LOW after (D-1/2 + 2) writes to the FIFO, where D = 1,025 for the IDT72V3640, 2,049 for the IDT72V3650, 4,097 for the IDT72V3660, 8,193 for the IDT72V3670, 16,385 for the IDT72V3680 and 32,769 for the IDT72V3690.

See Figure 22, *Half-Full Flag Timing (IDT Standard and FWFT Modes)*, for the relevant timing information. Because $\overline{HF}$ is updated by both RCLK and WCLK, it is considered asynchronous.

DATA OUTPUTS (Q_0-Q_n)

(Q_0-Q_{35}) are data outputs for 36-bit wide data, (Q_0 - Q_{17}) are data outputs for 18-bit wide data or (Q_0-Q_8) are data outputs for 9-bit wide data.

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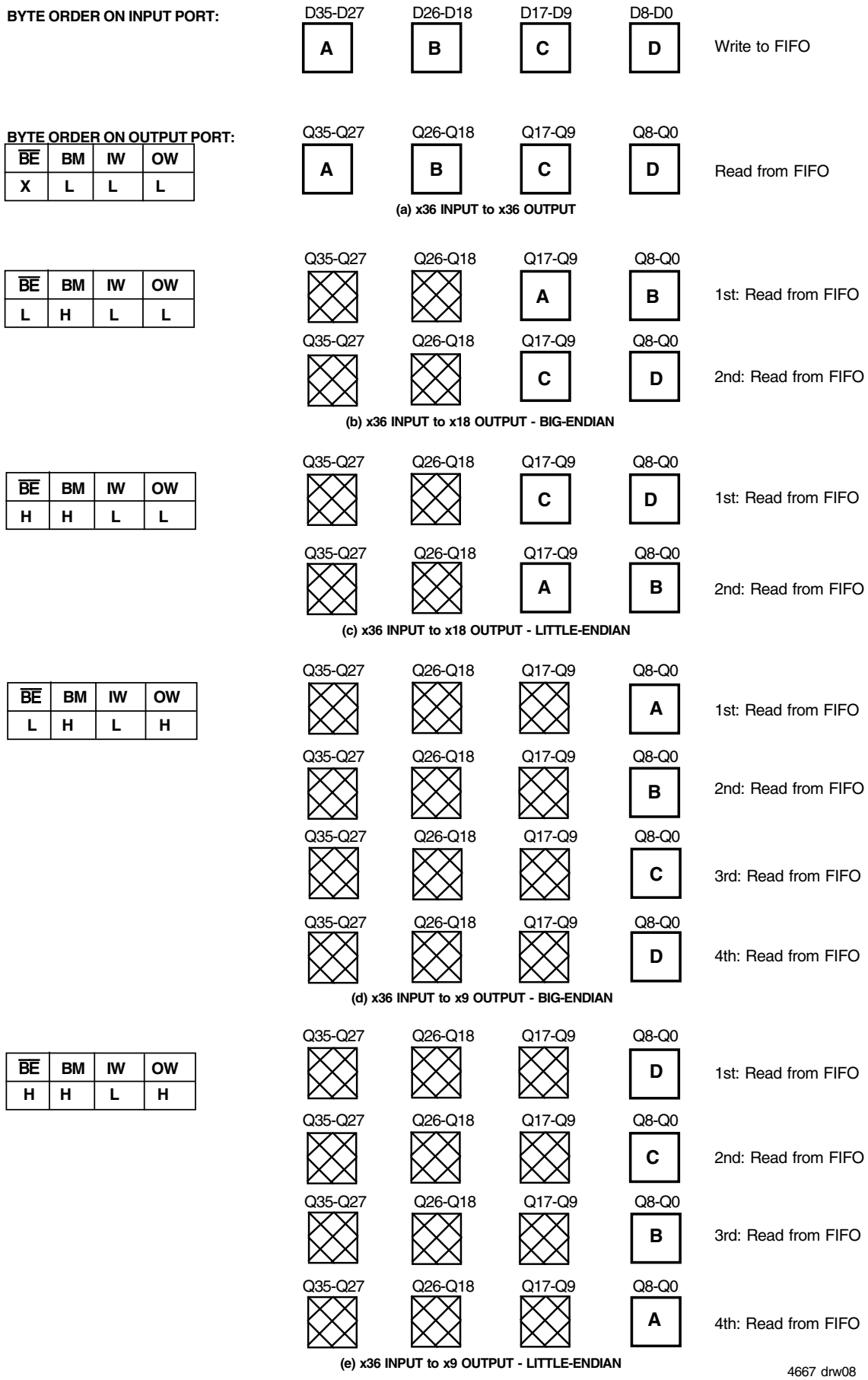


Figure 4. Bus-Matching Byte Arrangement

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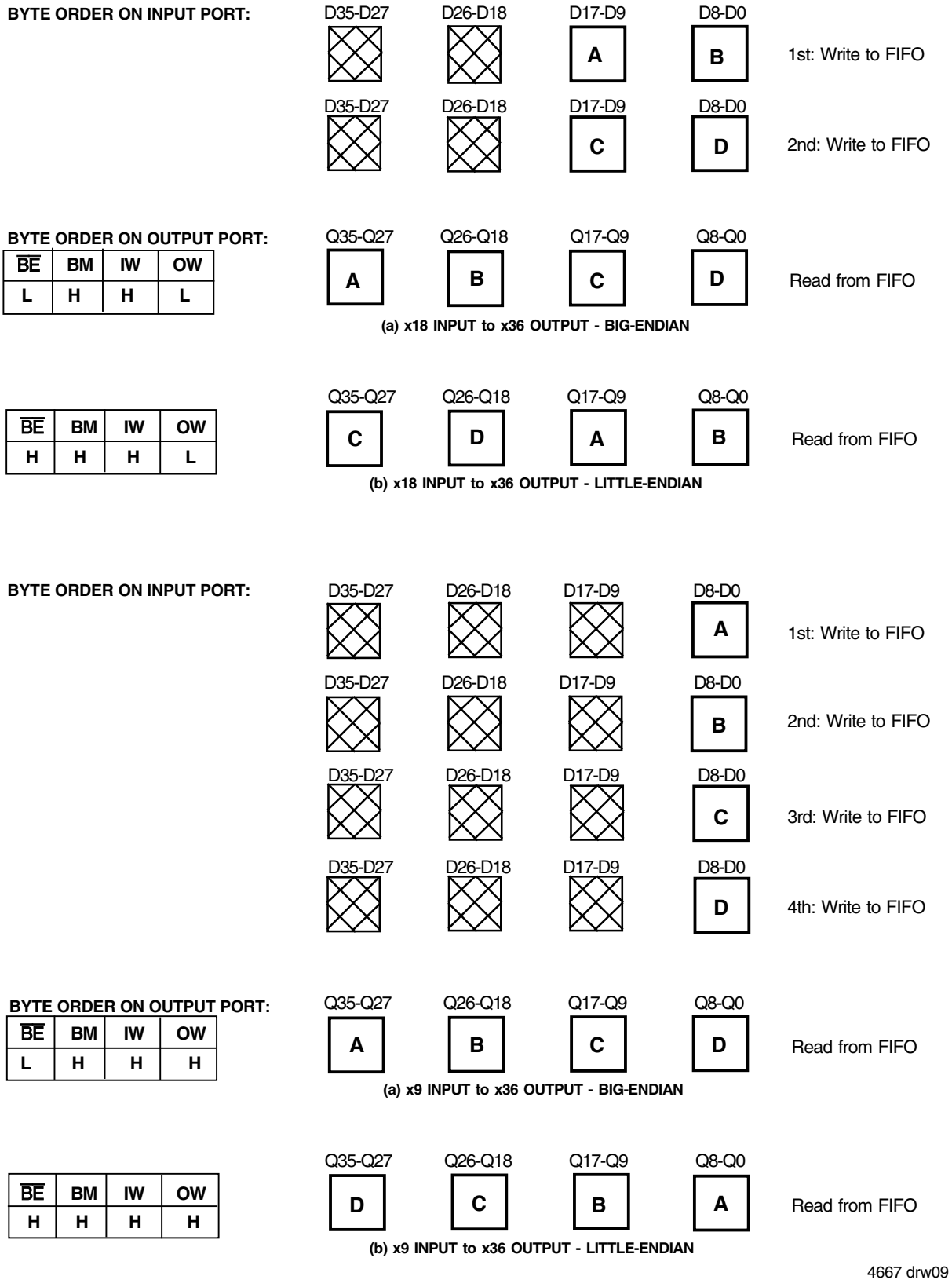


Figure 4. Bus-Matching Byte Arrangement (Continued)

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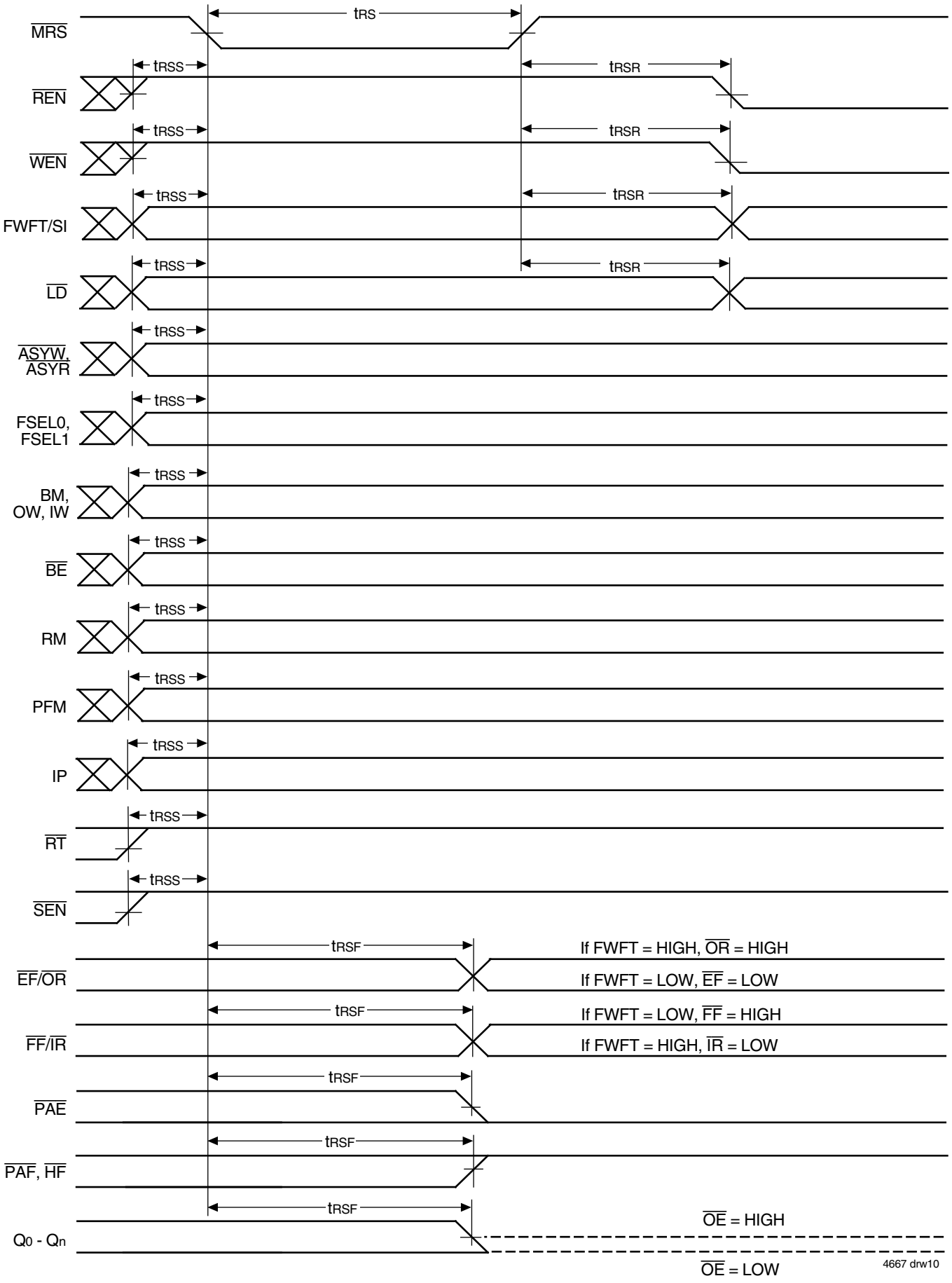


Figure 5. Master Reset Timing

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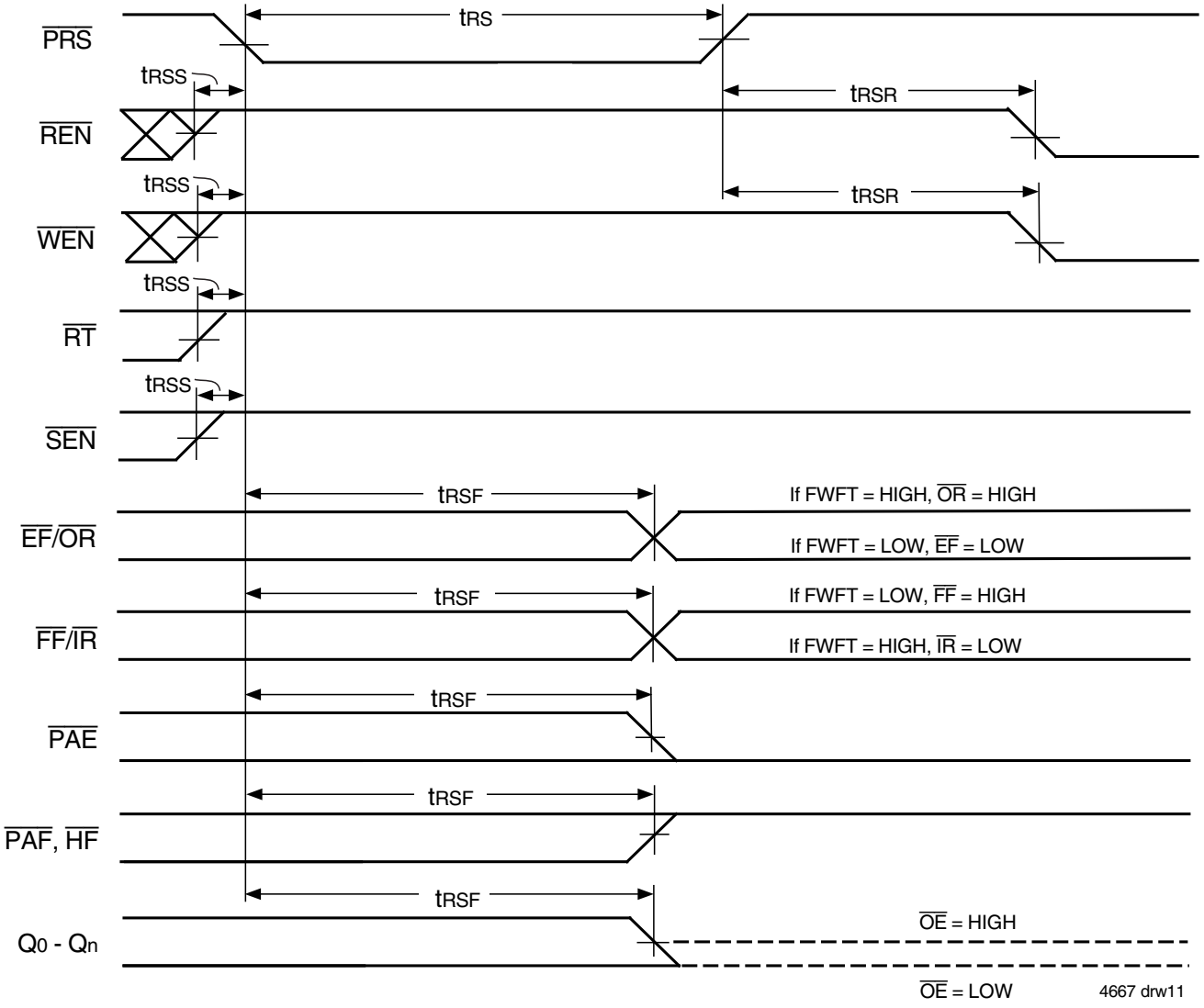
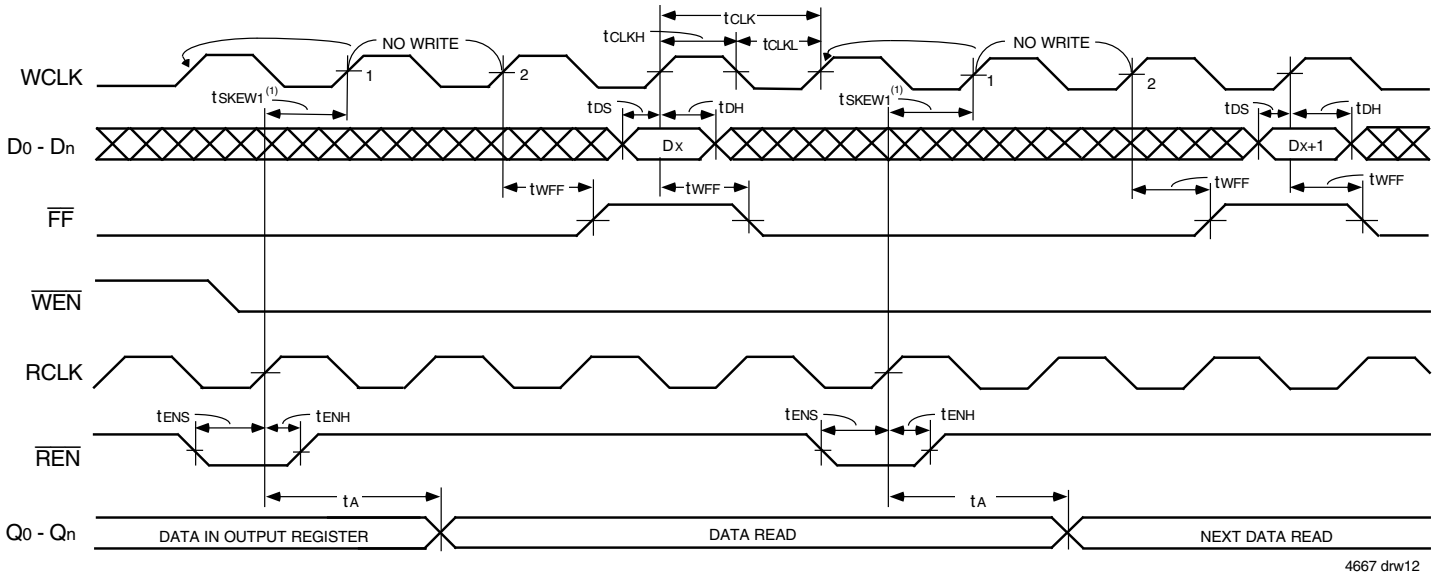


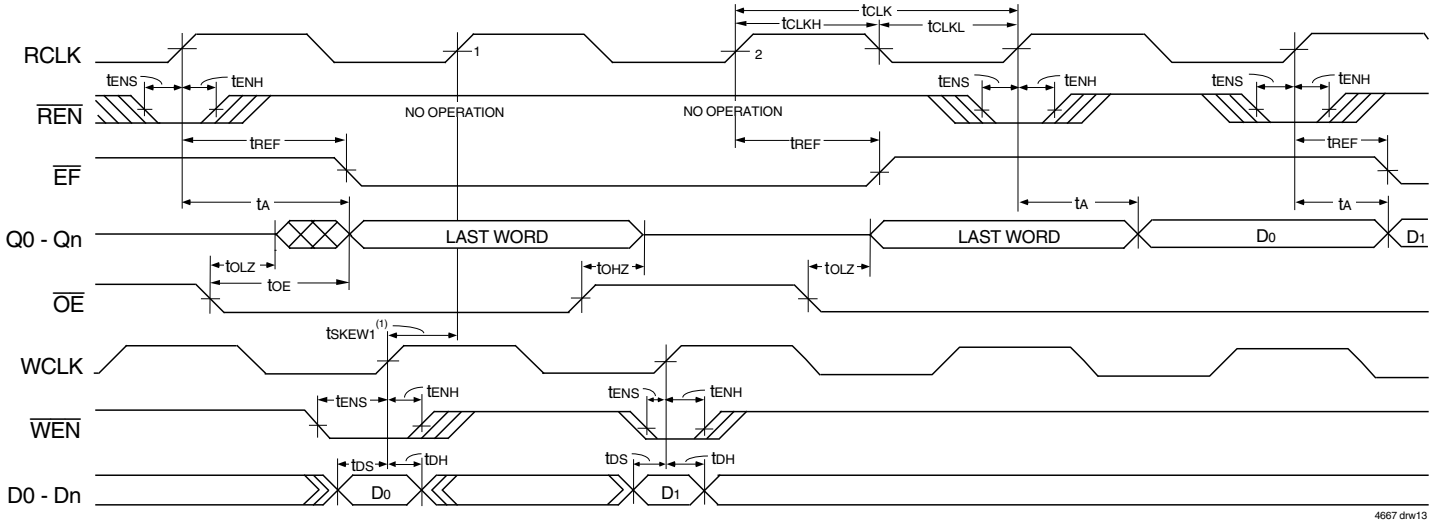
Figure 6. Partial Reset Timing

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NOTES:
1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{FF}$ will go HIGH (after one WCLK cycle pus t_{WFF}). If the time between the rising edge of the RCLK and the rising edge of the WCLK is less than t_{SKEW1}, then the $\overline{FF}$ deassertion may be delayed one extra WCLK cycle.
2. $\overline{LD}$ = HIGH, $\overline{OE}$ = LOW, $\overline{EF}$ = HIGH

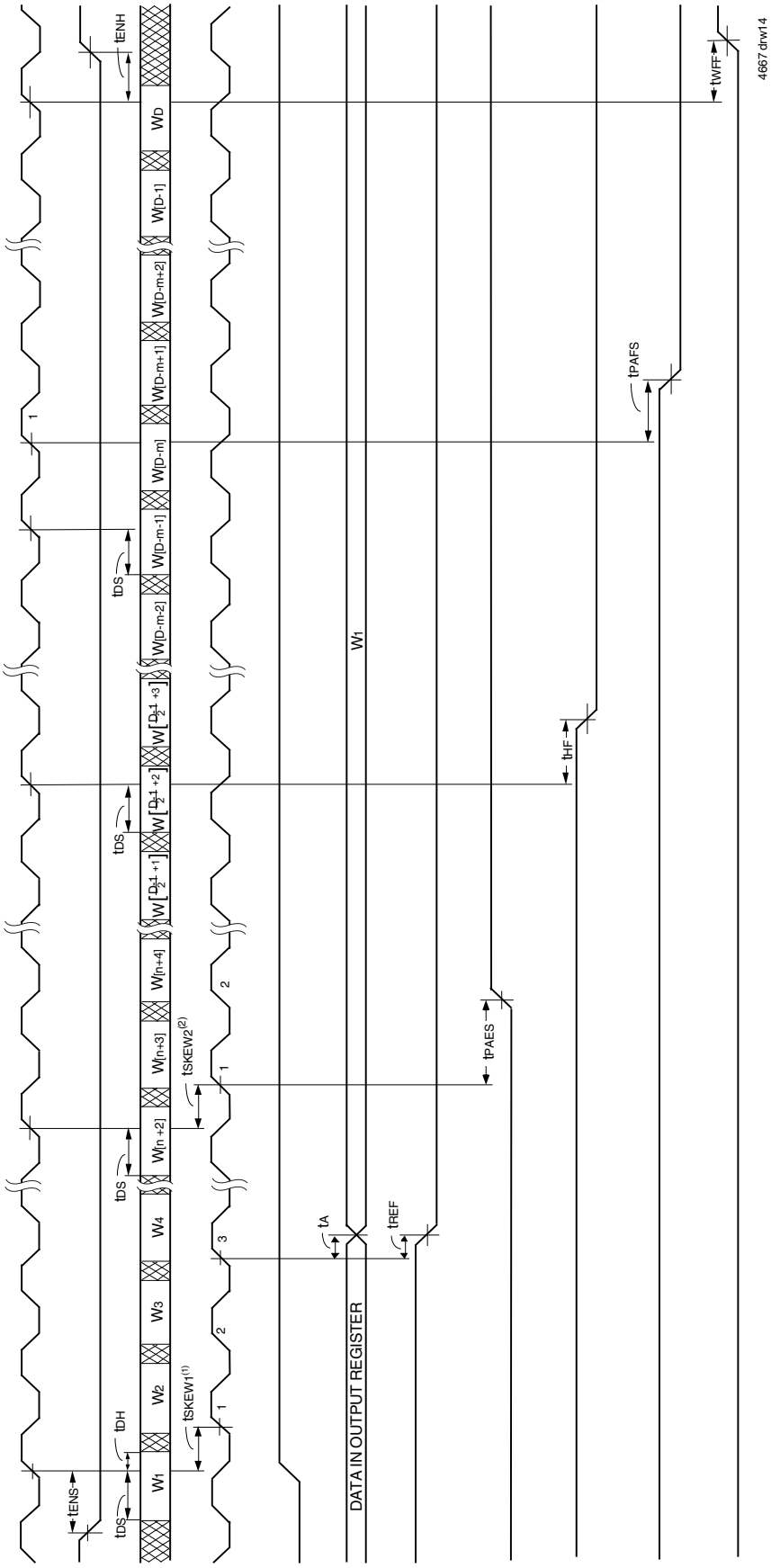
Figure 7. Write Cycle and Full Flag Timing (IDT Standard Mode)



NOTES:
1. t_{SKEW1} is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that $\overline{EF}$ will go HIGH (after one RCLK cycle plus t_{REF}). If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW1}, then $\overline{EF}$ deassertion may be delayed one extra RCLK cycle.
2. $\overline{LD}$ = HIGH.
3. First data word latency = t_{SKEW1} + 1*T_{RCLK} + t_{REF}.

Figure 8. Read Cycle, Empty Flag and First Data Word Latency Timing (IDT Standard Mode)

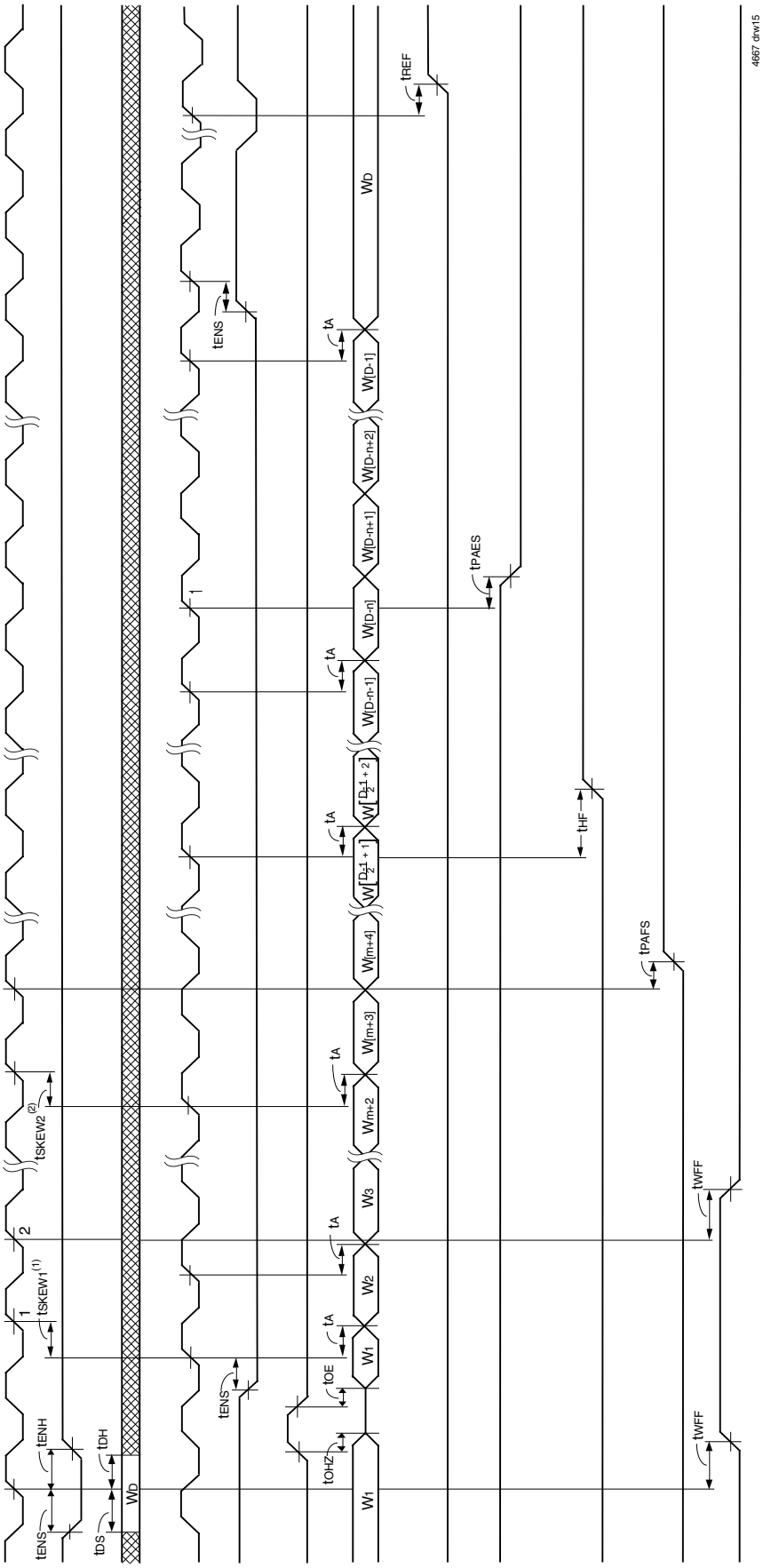
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NOTES:
1. tSKEW1 is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that $\overline{OR}$ will go LOW after two RCLK cycles plus tREF. If the time between the rising edge of WCLK and the rising edge of RCLK is less than tSKEW1, then $\overline{OR}$ assertion may be delayed one extra RCLK cycle.
2. tSKEW2 is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that $\overline{PAE}$ will go HIGH after one RCLK cycle plus tPAES. If the time between the rising edge of WCLK and the rising edge of RCLK is less than tSKEW2, then the $\overline{PAE}$ deassertion may be delayed one extra RCLK cycle.
3. $\overline{LD}$ = HIGH, $\overline{OE}$ = LOW
4. n = $\overline{PAE}$ offset, m = $\overline{PAF}$ offset and D = maximum FIFO depth.
5. D = 1,025 for IDT72V3640, 2,049 for IDT72V3650, 4,097 for IDT72V3660, 8,193 for IDT72V3670, 16,385 for the IDT72V3680 and 32,769 for the IDT72V3690.
6. First data word latency = tSKEW1 + 2*TRCLK + tREF.

Figure 9. Write Timing (First Word Fall Through Mode)

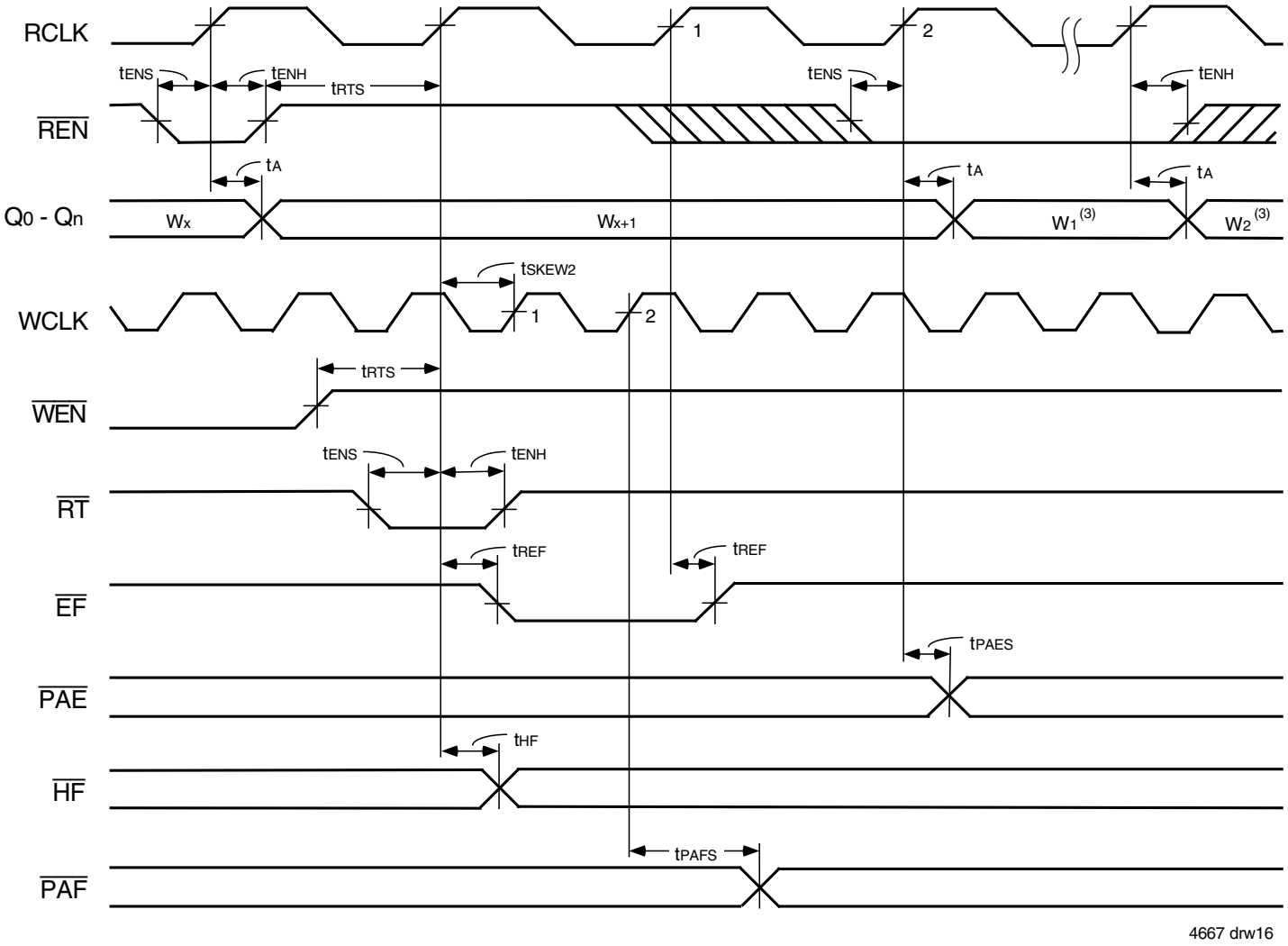
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NOTES:
1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{IR}$ will go LOW after one WCLK cycle plus t_{WFF}. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then the $\overline{IR}$ assertion may be delayed one extra WCLK cycle.
2. t_{SKEW2} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{PAF}$ will go HIGH after one WCLK cycle plus t_{PAFS}. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW2}, then the $\overline{PAF}$ deassertion may be delayed one extra WCLK cycle.
3. $\overline{LD}$ = HIGH
4. n = $\overline{PAE}$ Offset, m = $\overline{PAF}$ offset and D = maximum FIFO depth.
5. D = 1,025 for IDT72V3640, 2,049 for IDT72V3650, 4,097 for IDT72V3660, 8,193 for IDT72V3670, 16,385 for the IDT72V3680 and 32,769 for the IDT72V3690.

Figure 10. Read Timing (First Word Fall Through Mode)

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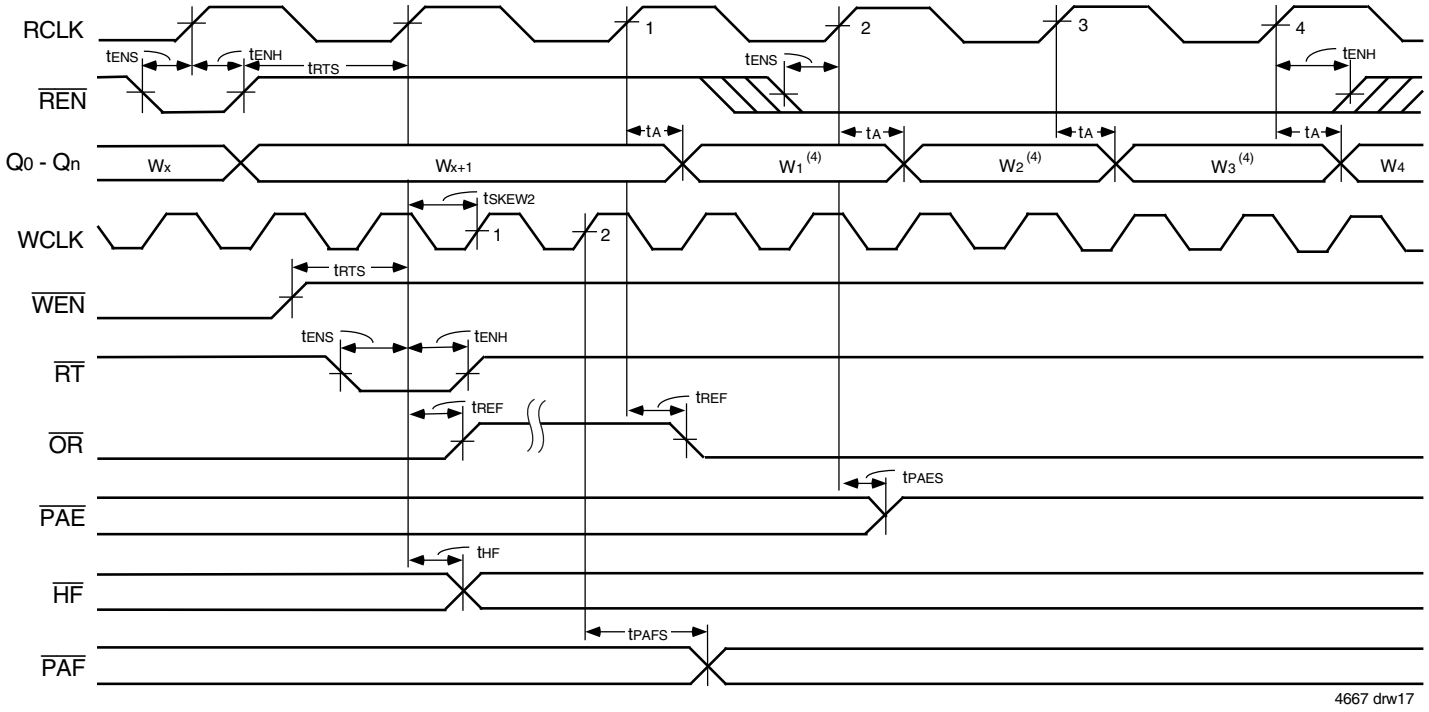


NOTES:

1. Retransmit setup is complete after $\overline{EF}$ returns HIGH, only then can a read operation begin.
2. $\overline{OE}$ = LOW.
3. W_1 = first word written to the FIFO after Master Reset, W_2 = second word written to the FIFO after Master Reset.
4. No more than D - 2 may be written to the FIFO between Reset (Master or Partial) and Retransmit setup. Therefore, $\overline{FF}$ will be HIGH throughout the Retransmit setup procedure. D = 1,024 for IDT72V3640, 2,048 for IDT72V3650, 4,096 for IDT72V3660, 8,192 for IDT72V3670, 16,384 for the IDT72V3680 and 32,768 for the IDT72V3690.
5. There must be at least two words written to the FIFO before a Retransmit operation can be invoked.
6. RM is set HIGH during MRS.

Figure 11. Retransmit Timing (IDT Standard Mode)

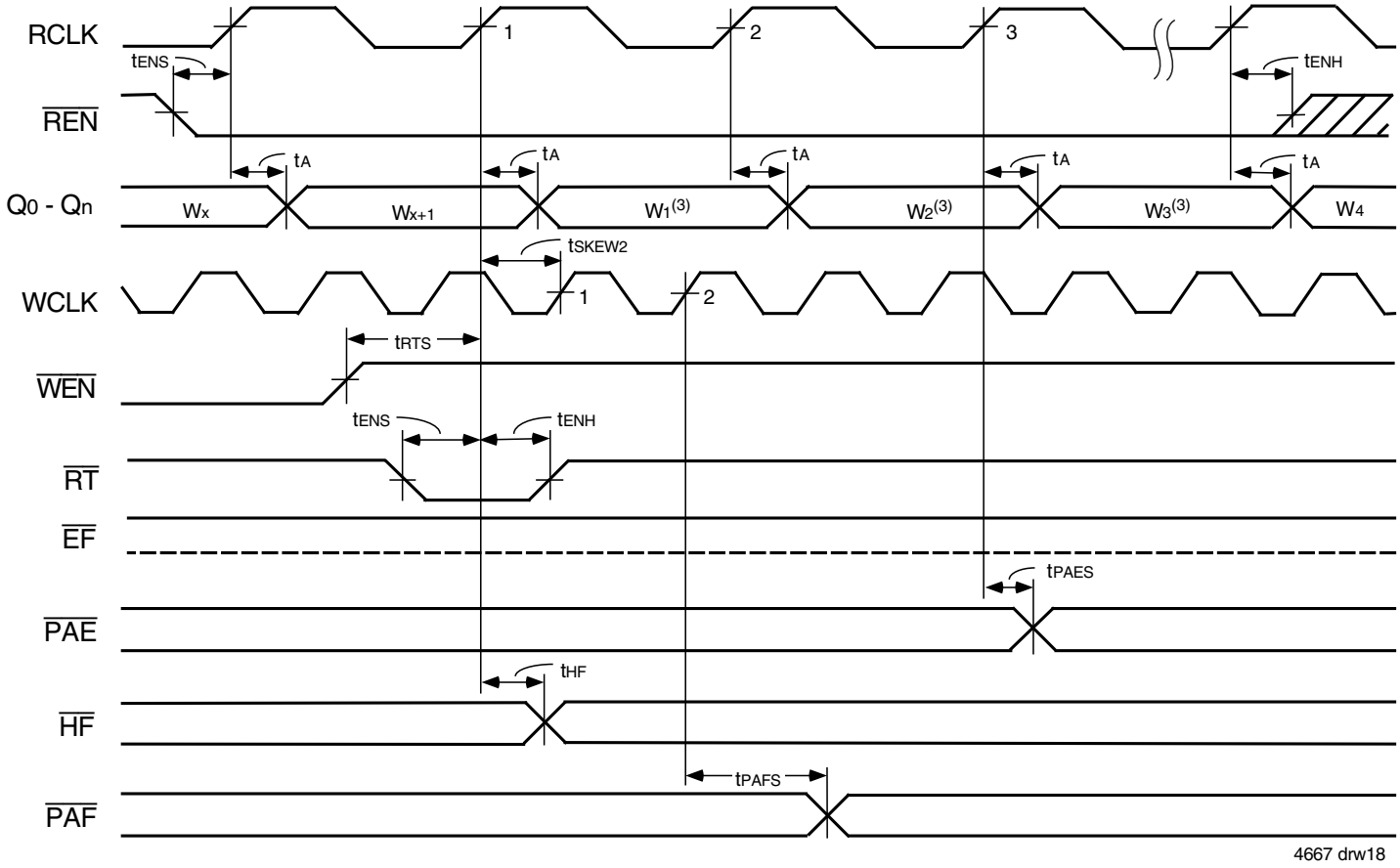
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NOTES:
1. Retransmit setup is complete after $\overline{OR}$ returns LOW.
2. No more than D - 2 words may be written to the FIFO between Reset (Master or Partial) and Retransmit setup. Therefore, $\overline{IR}$ will be LOW throughout the Retransmit setup procedure. D = 1,025 for the IDT72V3640, 2,049 for the IDT72V3650, 4,097 for the IDT72V3660, 8,193 for the IDT72V3670, 16,385 for the IDT72V3680 and 32,769 for the IDT72V3690.
3. $\overline{OE}$ = LOW.
4. W_1, W_2, W_3 = first, second and third words written to the FIFO after Master Reset.
5. There must be at least two words written to the FIFO before a Retransmit operation can be invoked.
6. RM is set HIGH during MRS.

Figure 12. Retransmit Timing (FWFT Mode)

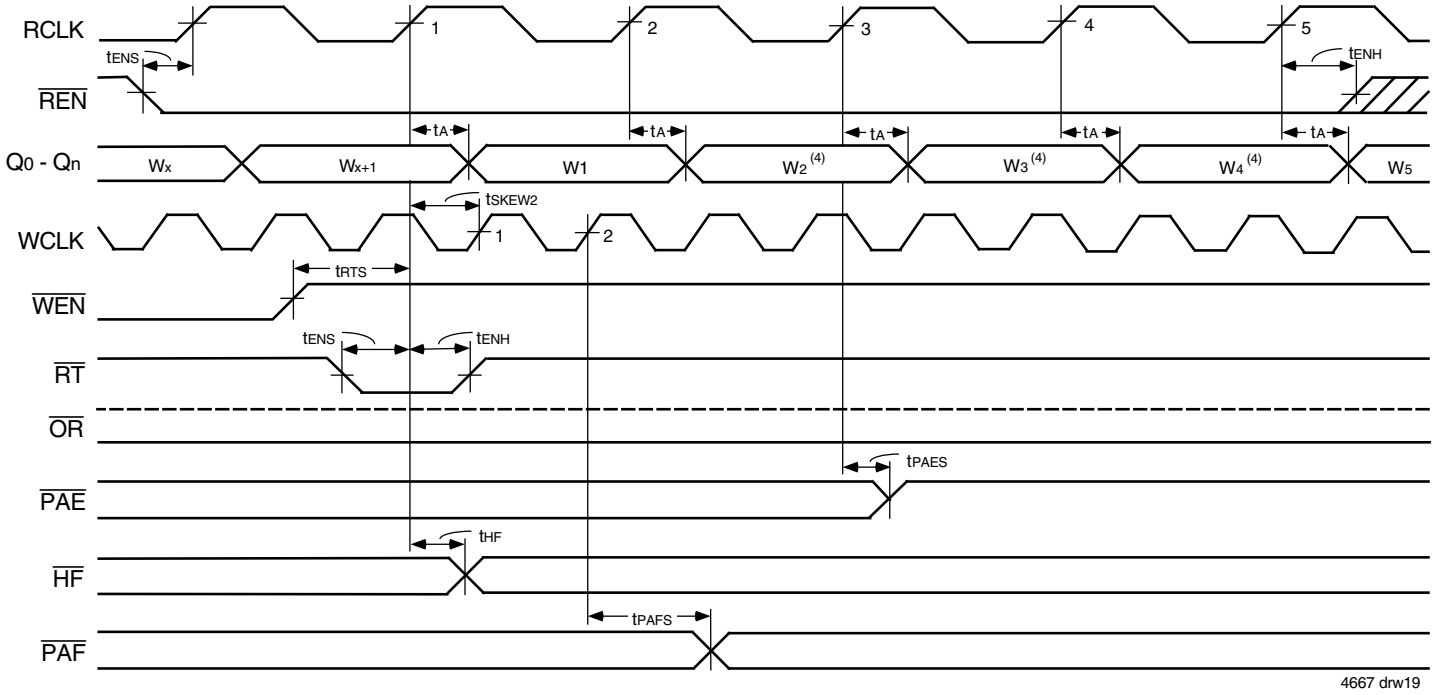
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NOTES:
1. If the part is empty at the point of Retransmit, the empty flag ($\overline{EF}$) will be updated based on RCLK (Retransmit clock cycle), valid data will also appear on the output.
2. $\overline{OE}$ = LOW.
3. W_1 = first word written to the FIFO after Master Reset, W_2 = second word written to the FIFO after Master Reset.
4. No more than D - 2 may be written to the FIFO between Reset (Master or Partial) and Retransmit setup. Therefore, $\overline{FF}$ will be HIGH throughout the Retransmit setup procedure. D = 1,024 for IDT72V3640, 2,048 for IDT72V3650, 4,096 for IDT72V3660, 8,192 for IDT72V3670, 16,384 for the IDT72V3680 and 32,768 for the IDT72V3690.
5. There must be at least two words written to the FIFO before a Retransmit operation can be invoked.
6. RM is set LOW during MRS.

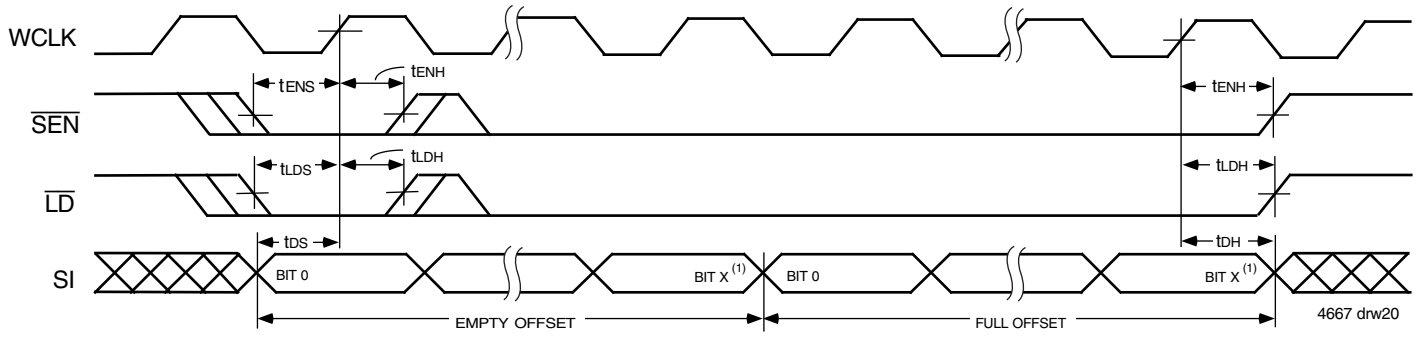
Figure 13. Zero Latency Retransmit Timing (IDT Standard Mode)

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NOTES:
1. If the part is empty at the point of Retransmit, the output ready flag ($\overline{OR}$) will be updated based on RCLK (Retransmit clock cycle), valid data will also appear on the output.
2. No more than D - 2 words may be written to the FIFO between Reset (Master or Partial) and Retransmit setup. Therefore, $\overline{IR}$ will be LOW throughout the Retransmit setup procedure. D = 1,025 for the IDT72V3640, 2,049 for the IDT72V3650, 4,097 for the IDT72V3660, 8,193 for the IDT72V3670, 16,385 for the IDT72V3680 and 32,769 for the IDT72V3690.
3. $\overline{OE}$ = LOW.
4. W_1, W_2, W_3 = first, second and third words written to the FIFO after Master Reset.
5. There must be at least two words written to the FIFO before a Retransmit operation can be invoked.
6. RM is set LOW during MRS.

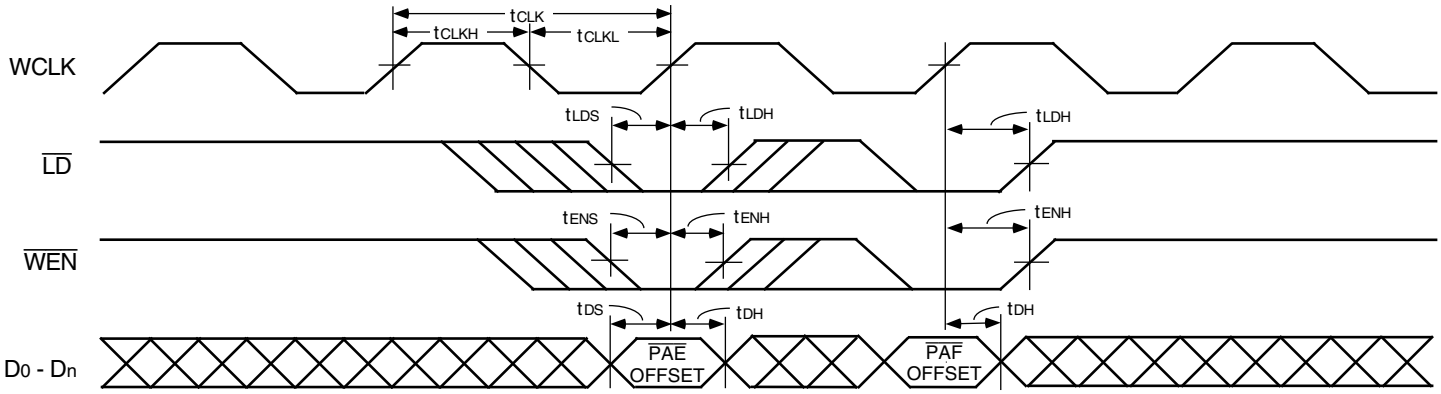
Figure 14. Zero Latency Retransmit Timing (FWFT Mode)



NOTE:
1. X = 9 for the IDT72V3640, X = 10 for the IDT72V3650, X = 11 for the IDT72V3660, X = 12 for the IDT72V3670, X = 13 for the IDT72V3680 and X = 14 for the IDT72V3690.

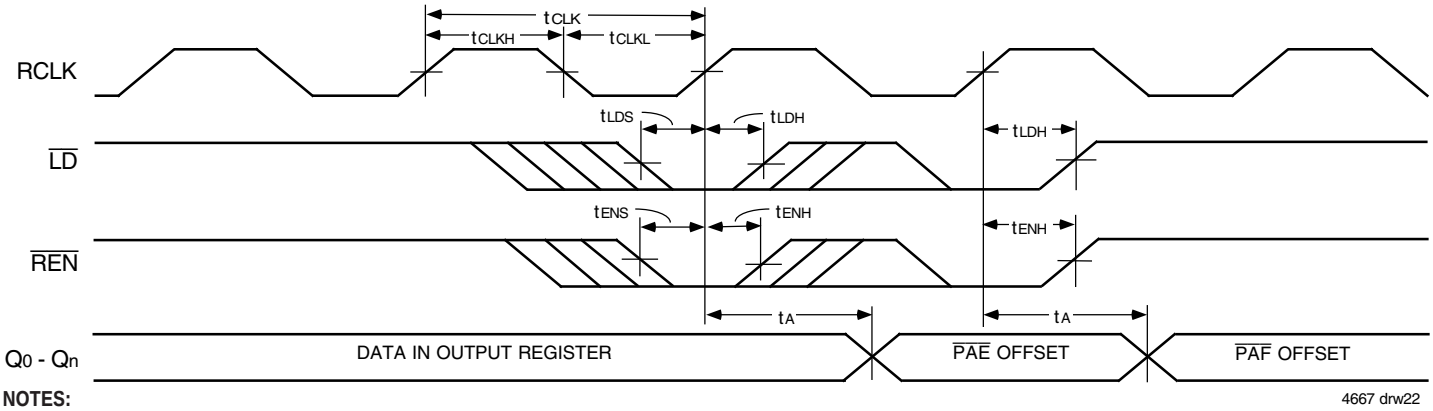
Figure 15. Serial Loading of Programmable Flag Registers (IDT Standard and FWFT Modes)

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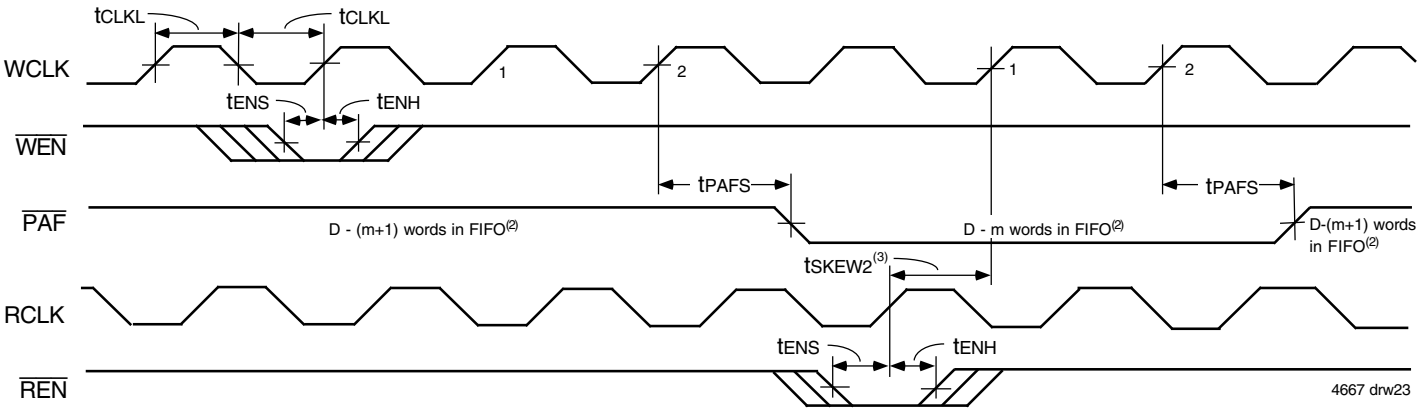
NOTE:
1. This timing diagram illustrates programming with an input bus width of 36 bits.

Figure 16. Parallel Loading of Programmable Flag Registers (IDT Standard and FWFT Modes)



NOTES:
1. OE = LOW.
2. The timing diagram illustrates reading of offset registers with an output bus width of 36 bits.

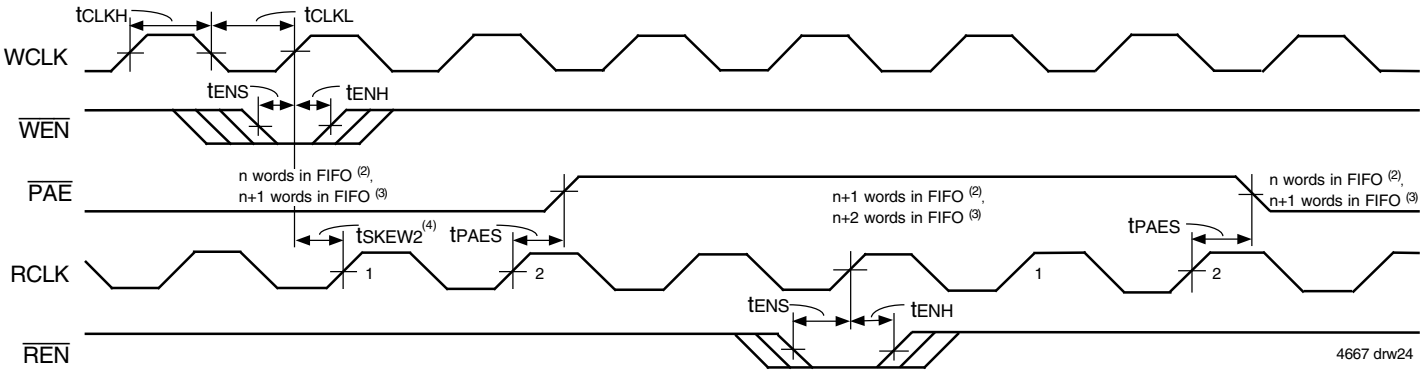
Figure 17. Parallel Read of Programmable Flag Registers (IDT Standard and FWFT Modes)



NOTES:
1. m = $\overline{PAF}$ offset.
2. D = maximum FIFO depth.
   In IDT Standard mode: D = 1,024 for the IDT72V3640, 2,048 for the IDT72V3650, 4,096 for the IDT72V3660 and 8,192 for the IDT72V3670, 16,384 for the IDT72V3680 and 32,768 for the IDT72V3690.
   In FWFT mode: D = 1,025 for the IDT72V3640, 2,049 for the IDT72V3650, 4,097 for the IDT72V3660, 8,193 for the IDT72V3670, 16,385 for the IDT72V3680 and 32,769 for the IDT72V3690.
3. t_{SKEW2} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{PAF}$ will go HIGH (after one WCLK cycle plus t_{PAFS}). If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW2}, then the $\overline{PAF}$ deassertion time may be delayed one extra WCLK cycle.
4. $\overline{PAF}$ is asserted and updated on the rising edge of WCLK only.
5. Select this mode by setting PFM HIGH during Master Reset.

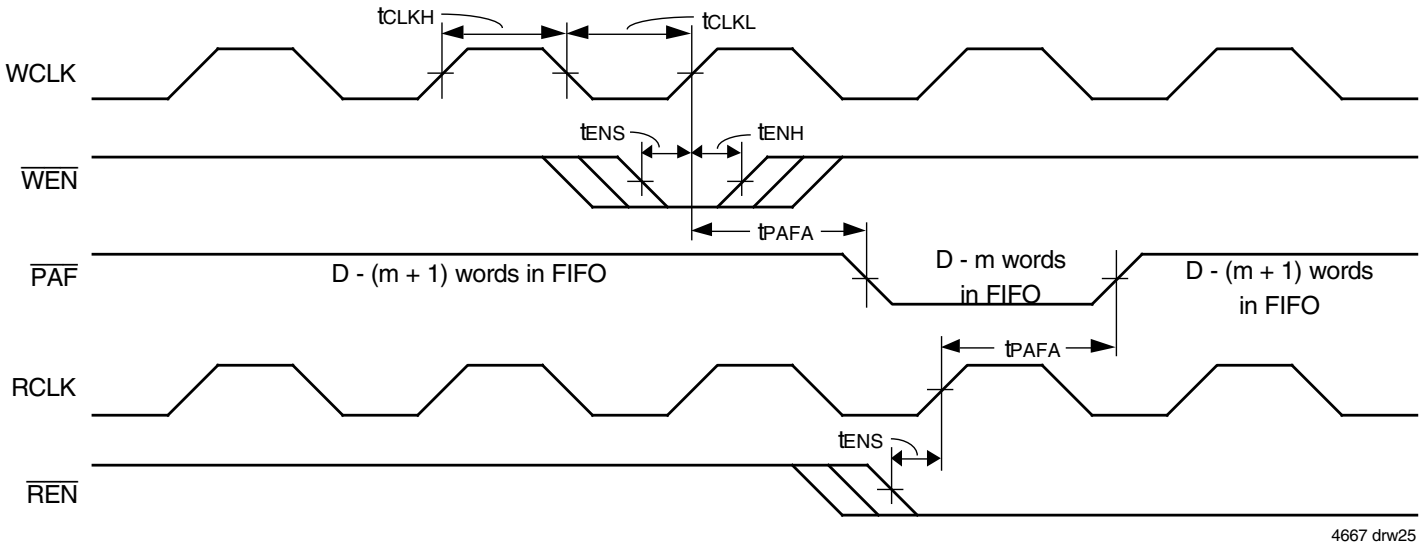
Figure 18. Synchronous Programmable Almost-Full Flag Timing (IDT Standard and FWFT Modes)

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NOTES:
1. n = $\overline{PAE}$ offset.
2. For IDT Standard mode
3. For FWFT mode.
4. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that $\overline{PAE}$ will go HIGH (after one RCLK cycle plus t_{PAES}). If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, then the $\overline{PAE}$ deassertion may be delayed one extra RCLK cycle.
5. $\overline{PAE}$ is asserted and updated on the rising edge of WCLK only.
6. Select this mode by setting PFM HIGH during Master Reset.

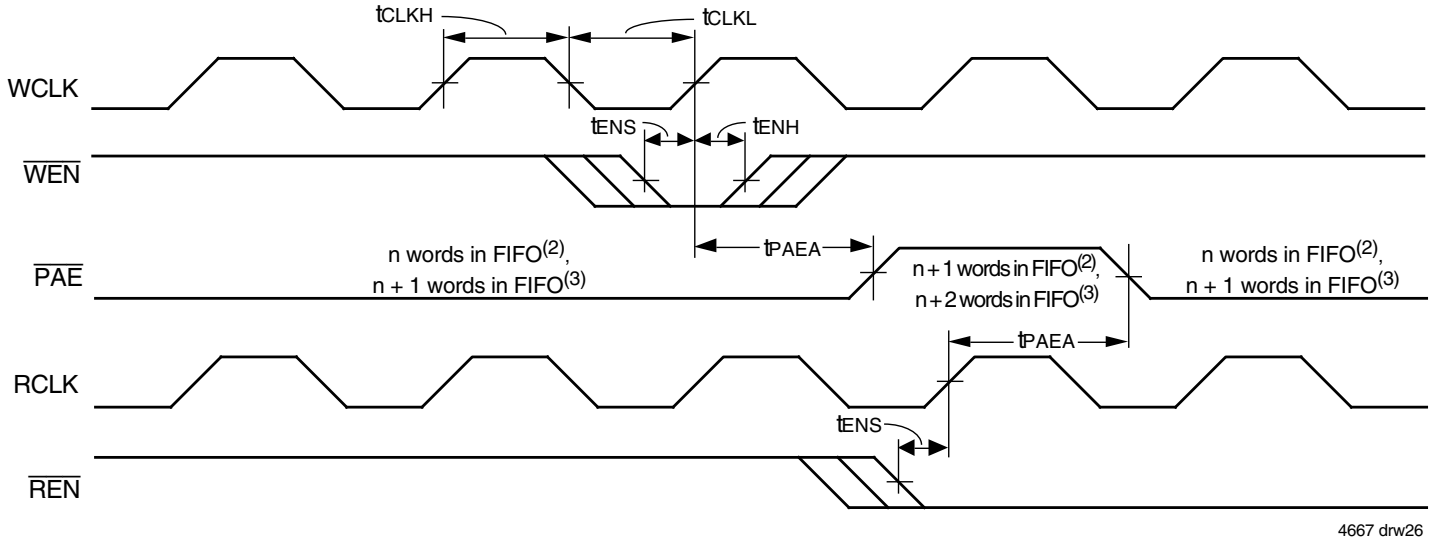
Figure 19. Synchronous Programmable Almost-Empty Flag Timing (IDT Standard and FWFT Modes)



NOTES:
1. m = $\overline{PAF}$ offset.
2. D = maximum FIFO Depth.
   In IDT Standard Mode: D = 1,024 for the IDT72V3640, 2,048 for the IDT72V3650, 4,096 for the IDT72V3660, 8,192 for the IDT72V3670, 16,384 for the IDT72V3680 and 32,768 for the IDT72V3690.
   In FWFT Mode: D = 1,025 for the IDT72V3640, 2,049 for the IDT72V3650, 4,097 for the IDT72V3660, 8,193 for the IDT72V3670, 16,385 for the IDT72V3680 and 32,769 for the IDT72V3690.
3. $\overline{PAF}$ is asserted to LOW on WCLK transition and reset to HIGH on RCLK transition.
4. Select this mode by setting PFM LOW during Master Reset.

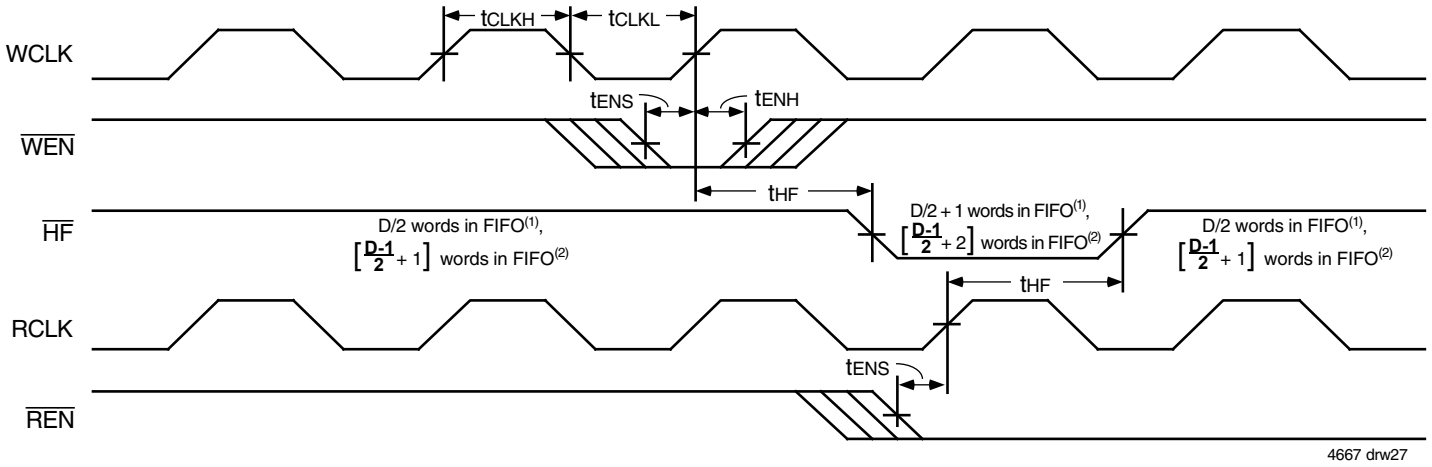
Figure 20. Asynchronous Programmable Almost-Full Flag Timing (IDT Standard and FWFT Modes)

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NOTES:
1. n = $\overline{PAE}$ offset.
2. For IDT Standard Mode.
3. For FWFT Mode.
4. $\overline{PAE}$ is asserted LOW on RCLK transition and reset to HIGH on WCLK transition.
5. Select this mode by setting PFM LOW during Master Reset.

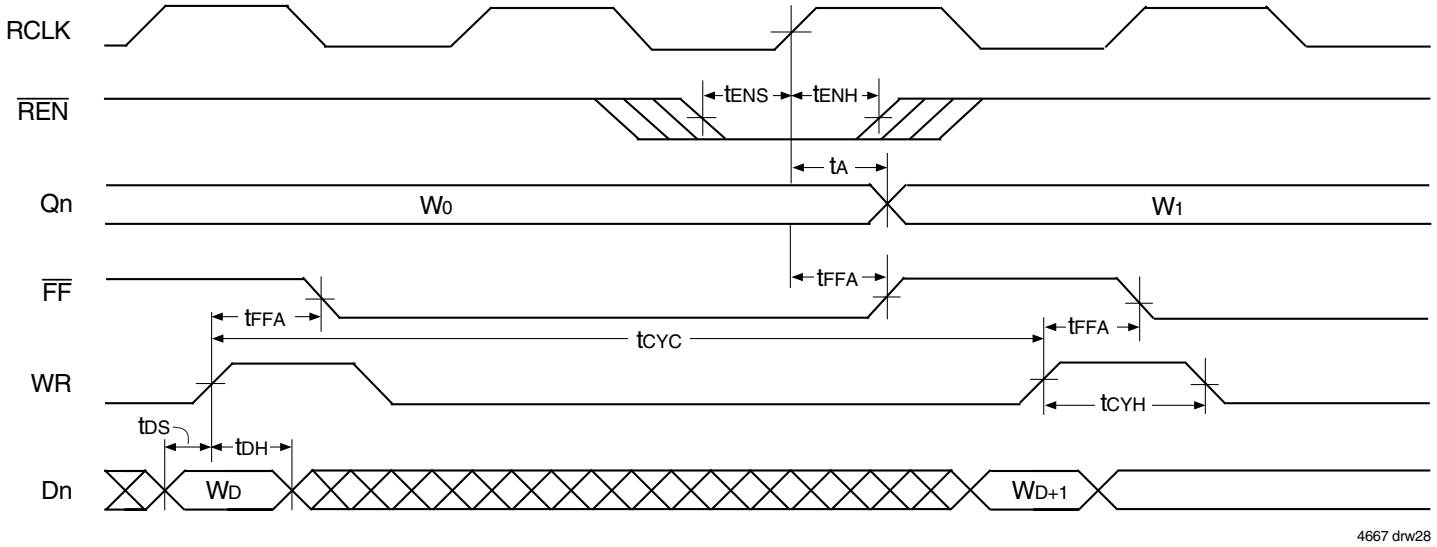
Figure 21. Asynchronous Programmable Almost-Empty Flag Timing (IDT Standard and FWFT Modes)



NOTES:
1. In IDT Standard mode: D = maximum FIFO depth. D = 1,024 for the IDT72V3640, 2,048 for the IDT72V3650, 4,096 for the IDT72V3660, 8,192 for the IDT72V3670, 16,384 for the IDT72V3680 and 32,768 for the IDT72V3690.
2. In FWFT mode: D = maximum FIFO depth. D = 1,025 for the IDT72V3640, 2,049 for the IDT72V3650, 4,097 for the IDT72V3660, 8,193 for the IDT72V3670, 16,385 for the IDT72V3680 and 32,769 for the IDT72V3690.

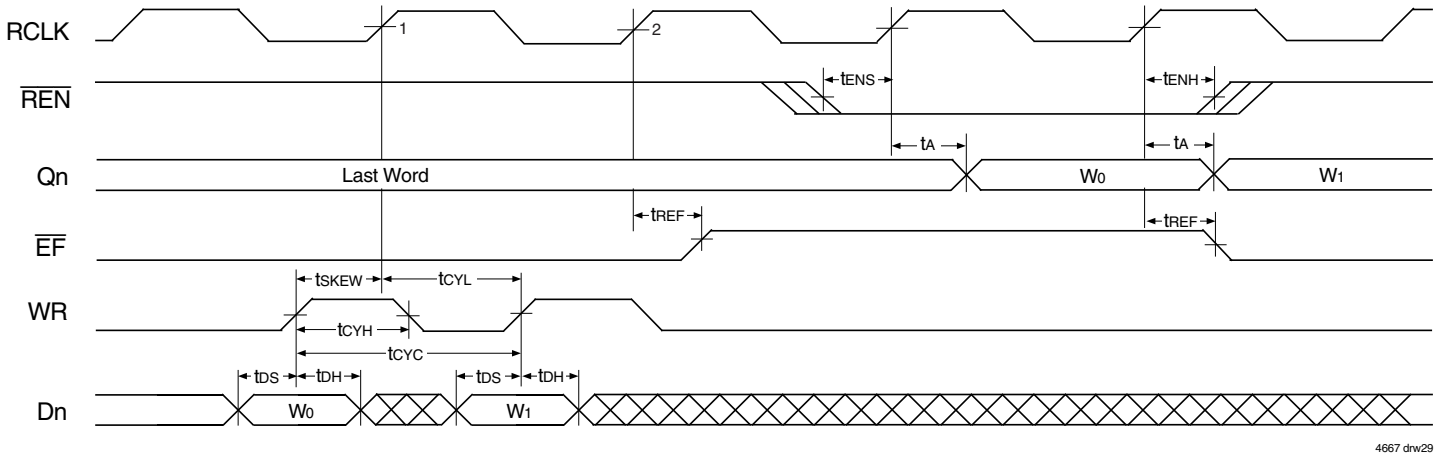
Figure 22. Half-Full Flag Timing (IDT Standard and FWFT Modes)

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NOTE:
1. $\overline{OE}$ = LOW and $\overline{WEN}$ = LOW.

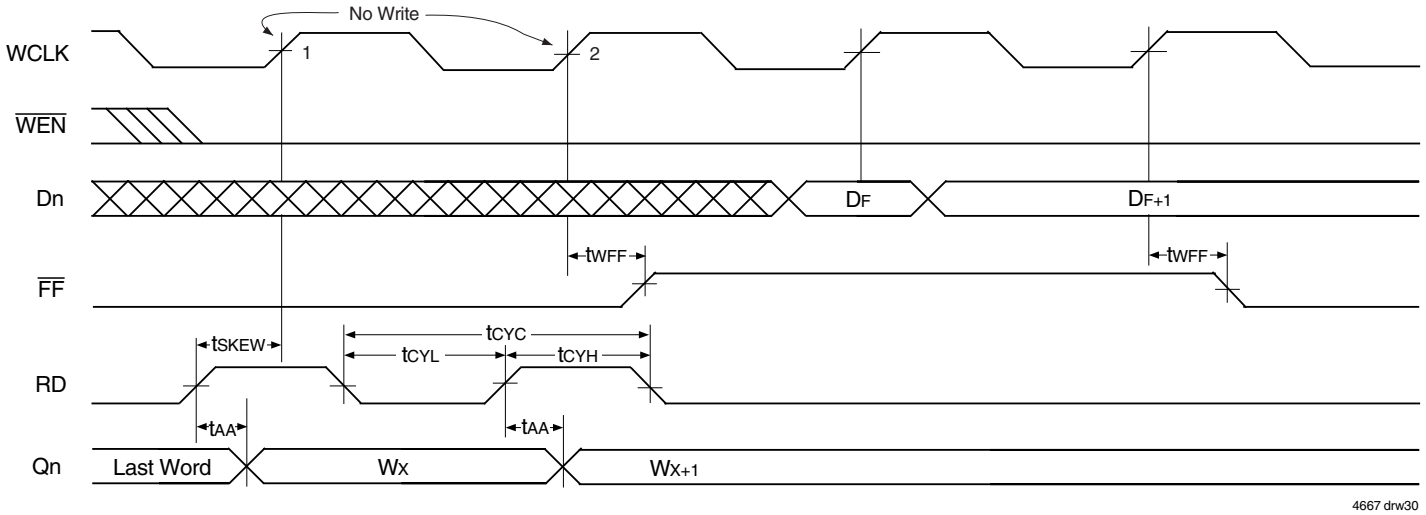
Figure 23. Asynchronous Write, Synchronous Read, Full Flag Operation (IDT Standard Mode)



NOTE:
1. $\overline{OE}$ = LOW and $\overline{WEN}$ = LOW.

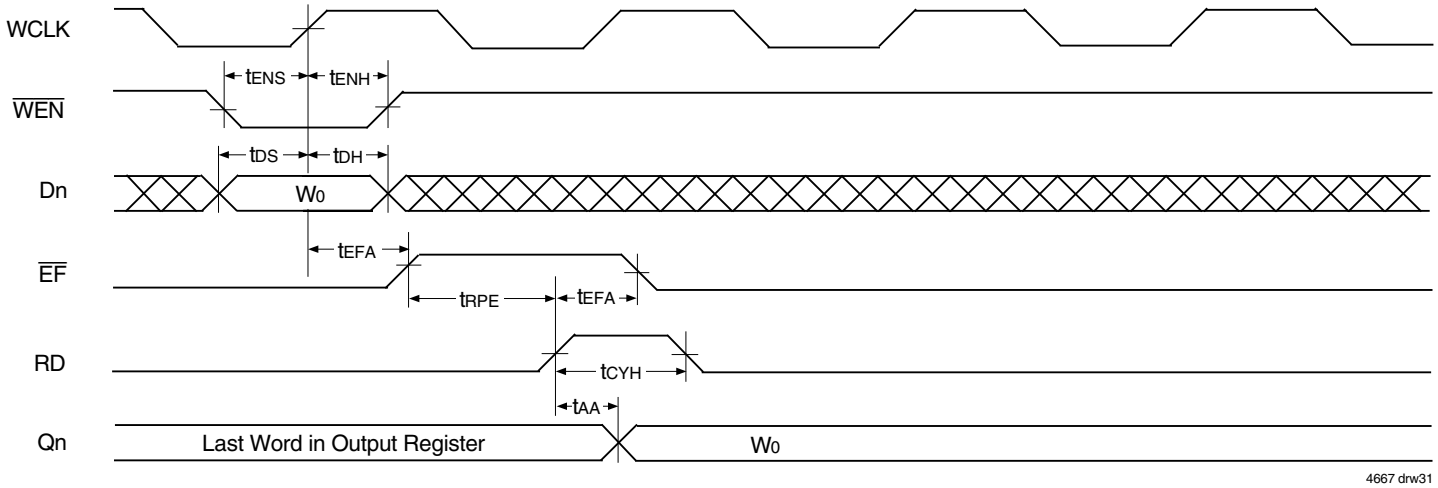
Figure 24. Asynchronous Write, Synchronous Read, Empty Flag Operation (IDT Standard Mode)

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NOTE:
1. $\overline{OE}$ = LOW and $\overline{REN}$ = LOW.
2. Asynchronous Read is available in IDT Standard Mode only.

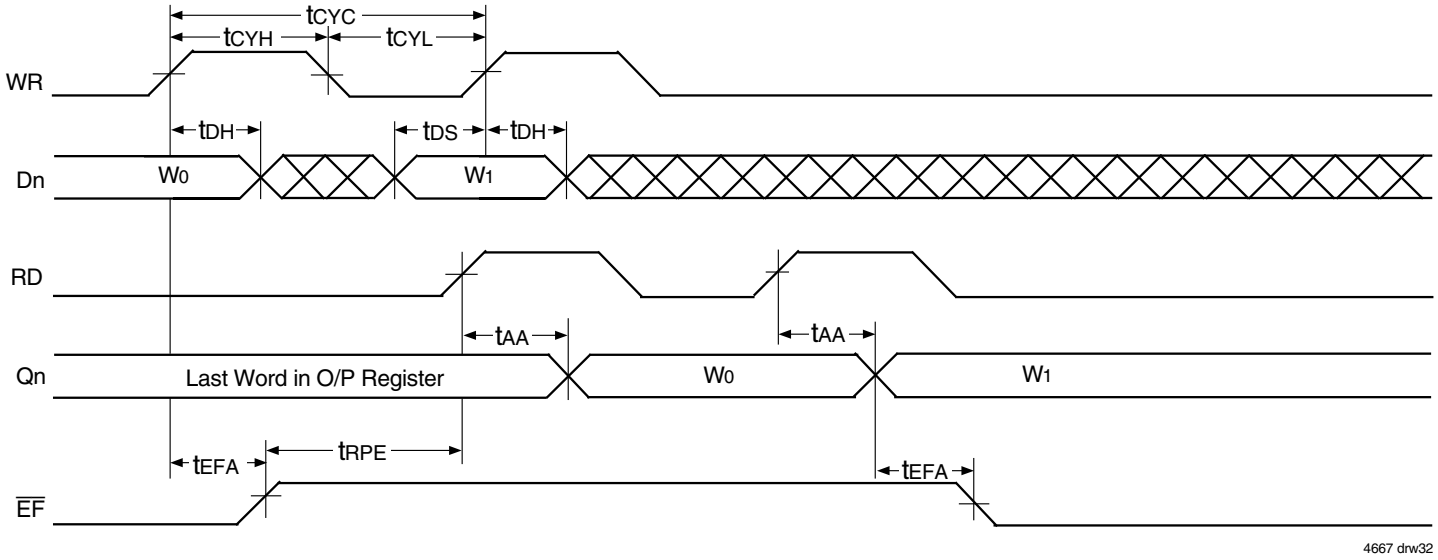
Figure 25. Synchronous Write, Asynchronous Read, Full Flag Operation (IDT Standard Mode)



NOTE:
1. $\overline{OE}$ = LOW and $\overline{REN}$ = LOW.
2. Asynchronous Read is available in IDT Standard Mode only.

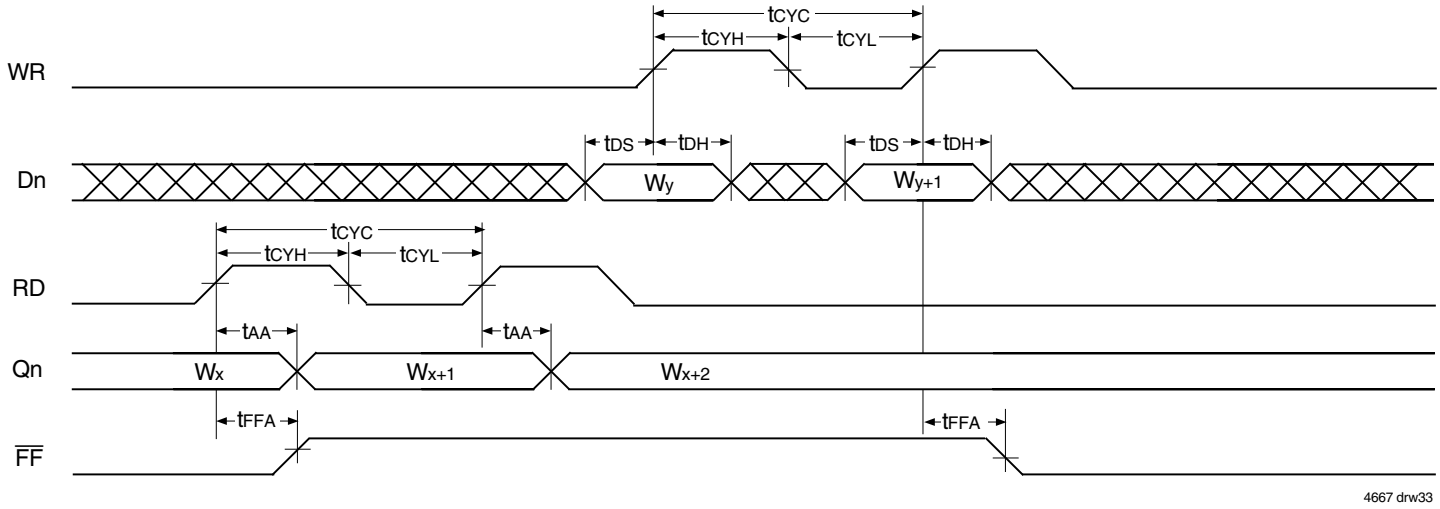
Figure 26. Synchronous Write, Asynchronous Read, Empty Flag Operation (IDT Standard Mode)

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NOTES:
1. $\overline{OE}$ = LOW, $\overline{WEN}$ = LOW, and $\overline{REN}$ = LOW.
2. Asynchronous Read is available in IDT Standard Mode only.

Figure 27. Asynchronous Write, Asynchronous Read, Empty Flag Operation (IDT Standard Mode)



NOTES:
1. $\overline{OE}$ = LOW, $\overline{WEN}$ = LOW, and $\overline{REN}$ = LOW.
2. Asynchronous Read is available in IDT Standard Mode only.

Figure 28. Asynchronous Write, Asynchronous Read, Full Flag Operation (IDT Standard Mode)

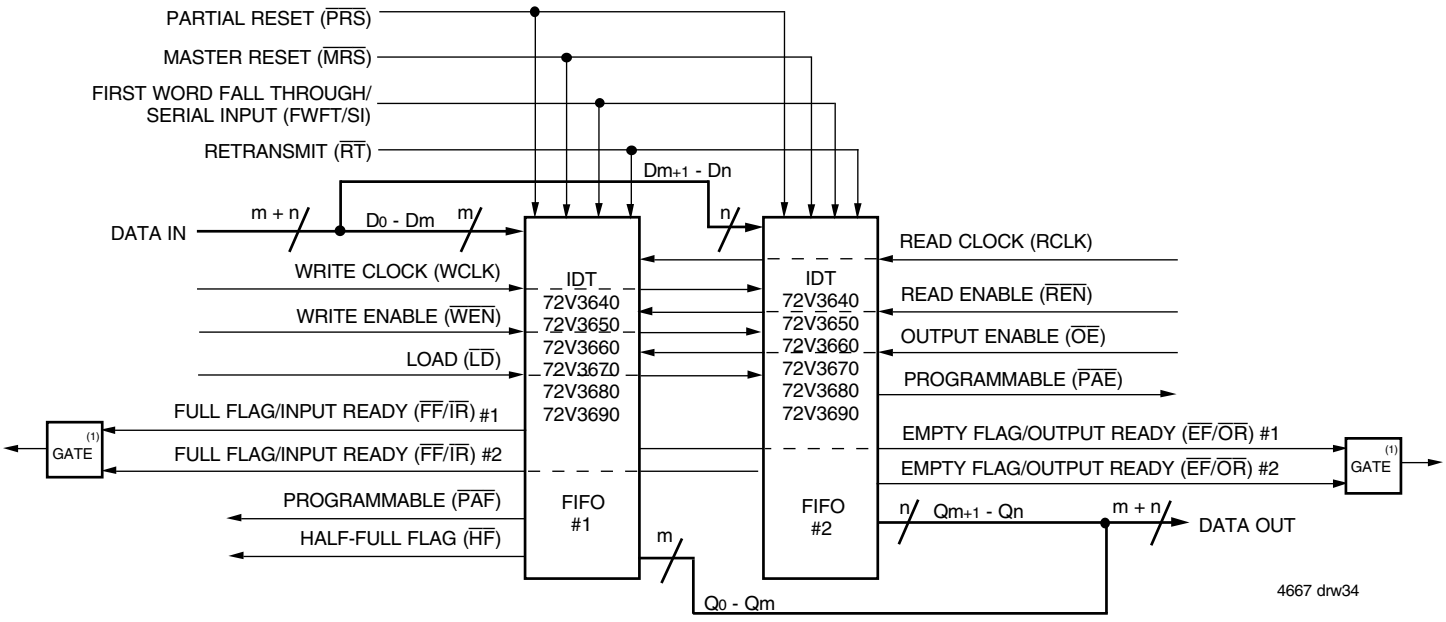
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OPTIONAL CONFIGURATIONS

WIDTH EXPANSION CONFIGURATION

Word width may be increased simply by connecting together the control signals of multiple devices. Status flags can be detected from any one device. The exceptions are the $\overline{EF}$ and $\overline{FF}$ functions in IDT Standard mode and the $\overline{IR}$ and $\overline{OR}$ functions in FWFT mode. Because of variations in skew between RCLK and WCLK, it is possible for $\overline{EF}$/$\overline{FF}$ deassertion and $\overline{IR}$/$\overline{OR}$ assertion to vary by one cycle between FIFOs. In IDT Standard mode, such problems can be avoided by creating composite flags, that is, ANDing $\overline{EF}$ of every FIFO, and separately ANDing $\overline{FF}$ of every FIFO. In FWFT mode, composite flags can be created by ORing $\overline{OR}$ of every FIFO, and separately ORing $\overline{IR}$ of every FIFO.

Figure 29 demonstrates a width expansion using two IDT72V3640/72V3650/72V3660/72V3670/72V3680/72V3690 devices. D_0 - D_{35} from each device form a 72-bit wide input bus and Q_0-Q_{35} from each device form a 72-bit wide output bus. Any word width can be attained by adding additional IDT72V3640/72V3650/72V3660/72V3670/72V3680/72V3690 devices.



NOTES:
1. Use an AND gate in IDT Standard mode, an OR gate in FWFT mode.
2. Do not connect any output control signals directly together.
3. FIFO #1 and FIFO #2 must be the same depth, but may be different word widths.

Figure 29. Block Diagram of 1,024 x 72, 2,048 x 72, 4,096 x 72, 8,192 x 72, 16,384 x 72 and 32,768 x 72 Width Expansion

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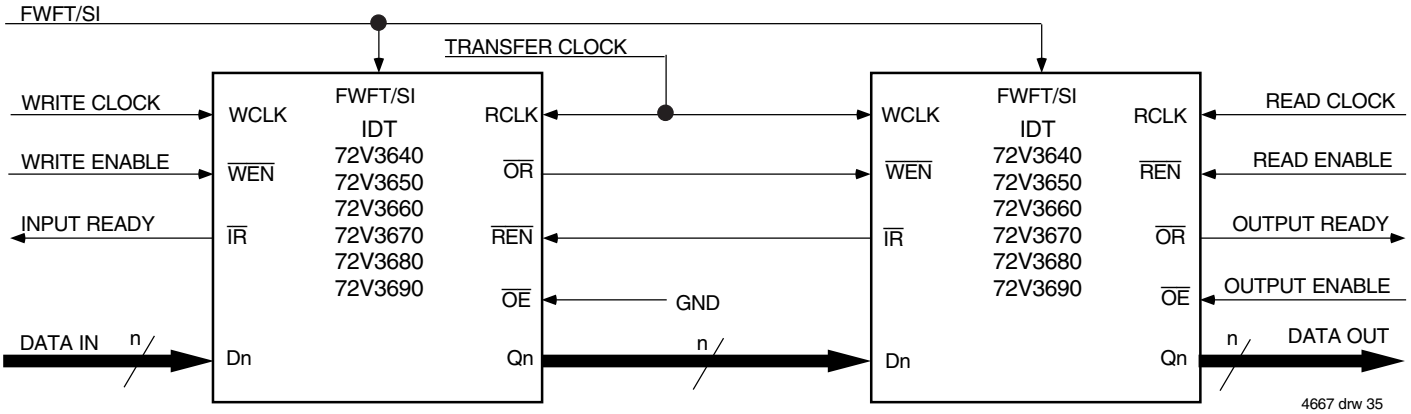


Figure 30. Block Diagram of 2,048 x 36, 4,096 x 36, 8,192 x 36, 16,384 x 36, 32,768 x 36 and 65,536 x 36 Depth Expansion

DEPTH EXPANSION CONFIGURATION (FWFT MODE ONLY)

The IDT72V3640 can easily be adapted to applications requiring depths greater than 1,024, 2,048 for the IDT72V3650, 4,096 for the IDT72V3660, 8,192 for the IDT72V3670, 16,384 for the IDT72V3680 and 32,768 for the IDT72V3690 with an 36-bit bus width. In FWFT mode, the FIFOs can be connected in series (the data outputs of one FIFO connected to the data inputs of the next) with no external logic necessary. The resulting configuration provides a total depth equivalent to the sum of the depths associated with each single FIFO. Figure 30 shows a depth expansion using two IDT72V3640/72V3650/72V3660/72V3670/72V3680/72V3690 devices.

Care should be taken to select FWFT mode during Master Reset for all FIFOs in the depth expansion configuration. The first word written to an empty configuration will pass from one FIFO to the next ("ripple down") until it finally appears at the outputs of the last FIFO in the chain – no read operation is necessary but the RCLK of each FIFO must be free-running. Each time the data word appears at the outputs of one FIFO, that device's $\overline{OR}$ line goes LOW, enabling a write to the next FIFO in line.

For an empty expansion configuration, the amount of time it takes for $\overline{OR}$ of the last FIFO in the chain to go LOW (i.e. valid data to appear on the last FIFO's outputs) after a word has been written to the first FIFO is the sum of the delays for each individual FIFO:

$$(N - 1)*(4*\text{transfer clock}) + 3*T_{RCLK}$$

where N is the number of FIFOs in the expansion and T_{RCLK} is the RCLK period. Note that extra cycles should be added for the possibility that the t_{SKEW1} specification is not met between WCLK and transfer clock, or RCLK and transfer clock, for the $\overline{OR}$ flag.

The "ripple down" delay is only noticeable for the first word written to an empty depth expansion configuration. There will be no delay evident for subsequent words written to the configuration.

The first free location created by reading from a full depth expansion configuration will "bubble up" from the last FIFO to the previous one until it finally moves into the first FIFO of the chain. Each time a free location is created in one FIFO of the chain, that FIFO's $\overline{IR}$ line goes LOW, enabling the preceding FIFO to write a word to fill it.

For a full expansion configuration, the amount of time it takes for $\overline{IR}$ of the first FIFO in the chain to go LOW after a word has been read from the last FIFO is the sum of the delays for each individual FIFO:

$$(N - 1)*(3*\text{transfer clock}) + 2\ T_{WCLK}$$

where N is the number of FIFOs in the expansion and T_{WCLK} is the WCLK period. Note that extra cycles should be added for the possibility that the t_{SKEW1} specification is not met between RCLK and transfer clock, or WCLK and transfer clock, for the $\overline{IR}$ flag.

The Transfer Clock line should be tied to either WCLK or RCLK, whichever is faster. Both these actions result in data moving, as quickly as possible, to the end of the chain and free locations to the beginning of the chain.

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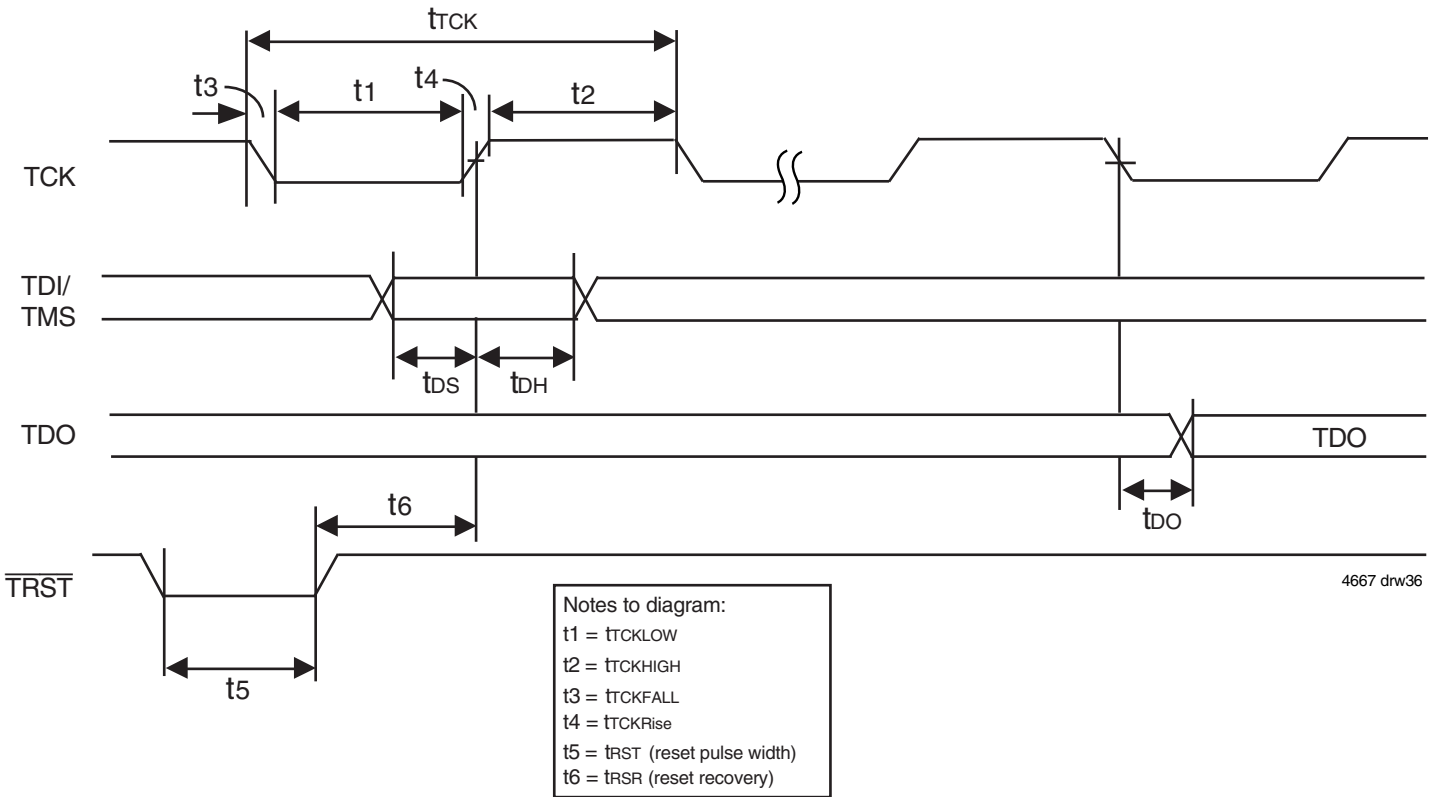


Figure 31. Standard JTAG Timing

SYSTEM INTERFACE PARAMETERS

Parameter	Symbol	Test Conditions	IDT72V3640 IDT72V3650 IDT72V3660 IDT72V3670 IDT72V3680 IDT72V3690		
			Min.	Max.	Units
Data Output	t_{DO} = Max		-	20	ns
Data Output Hold	t_{DOH}(1)		0	-	ns
Data Input	t_{DS}	trise=3ns	10	-	ns
	t_{DH}	tfall=3ns	10	-	

NOTE:
1. 50pf loading on external output signals.

JTAG AC ELECTRICAL CHARACTERISTICS

(Vcc = 3.3V ± 5%; Tcase = 0°C to +85°C)

Parameter	Symbol	Test Conditions			
			Min.	Max.	Units
JTAG Clock Input Period	tTCK	-	100	-	ns
JTAG Clock HIGH	tTCKHIGH	-	40	-	ns
JTAG Clock Low	tTCKLOW	-	40	-	ns
JTAG Clock Rise Time	tTCKRise	-	-	5(1)	ns
JTAG Clock Fall Time	tTCKFall	-	-	5(1)	ns
JTAG Reset	tRST	-	50	-	ns
JTAG Reset Recovery	tRSR	-	50	-	ns

NOTE:
1. Guaranteed by design.

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JTAG INTERFACE

Five additional pins (TDI, TDO, TMS, TCK and $\overline{TRST}$) are provided to support the JTAG boundary scan interface. The IDT72V3640/72V3650/72V3660/72V3670/72V3680/72V3690 incorporates the necessary tap controller and modified pad cells to implement the JTAG facility.

Note that IDT provides appropriate Boundary Scan Description Language program files for these devices.

The Standard JTAG interface consists of four basic elements:

- *Test Access Port (TAP)*
- *TAP controller*
- *Instruction Register (IR)*
- *Data Register Port (DR)*

The following sections provide a brief description of each element. For a complete description refer to the IEEE Standard Test Access Port Specification (IEEE Std. 1149.1-1990).

The Figure below shows the standard Boundary-Scan Architecture

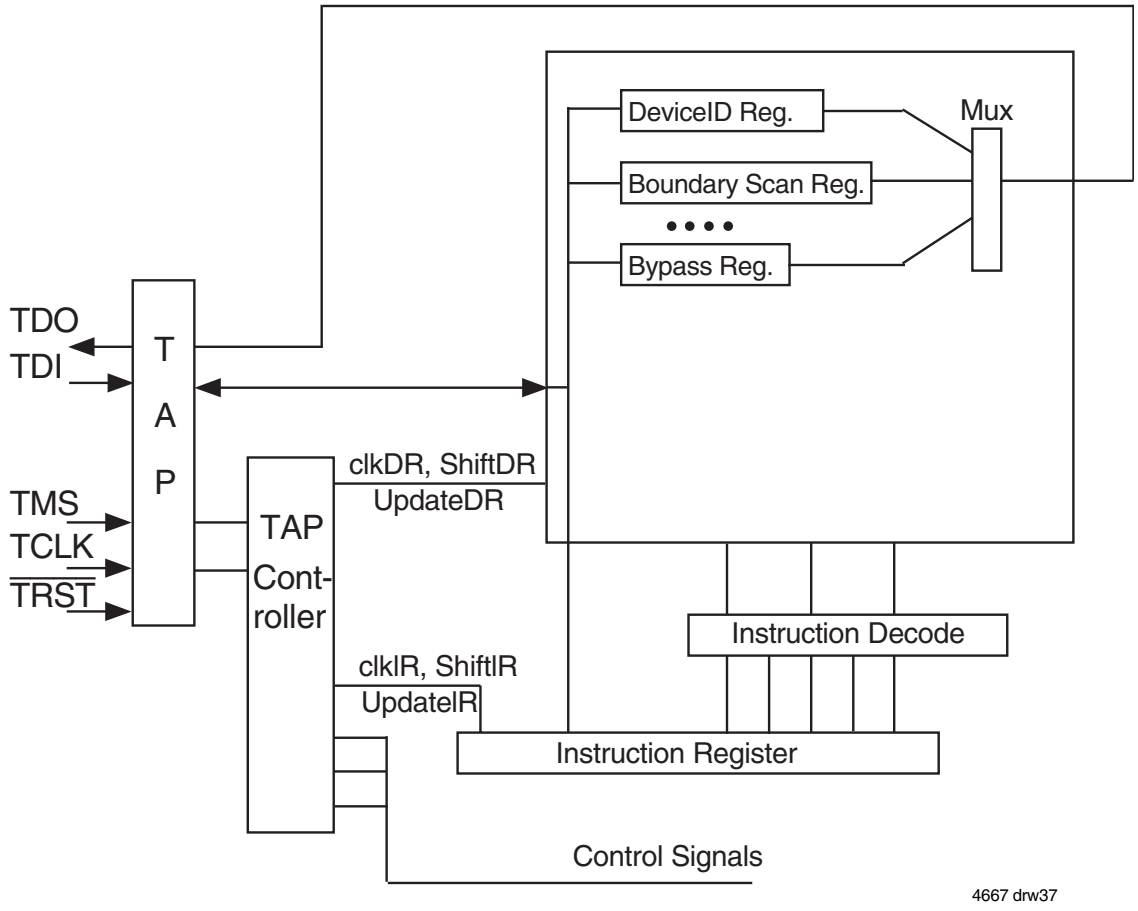


Figure 32. Boundary Scan Architecture

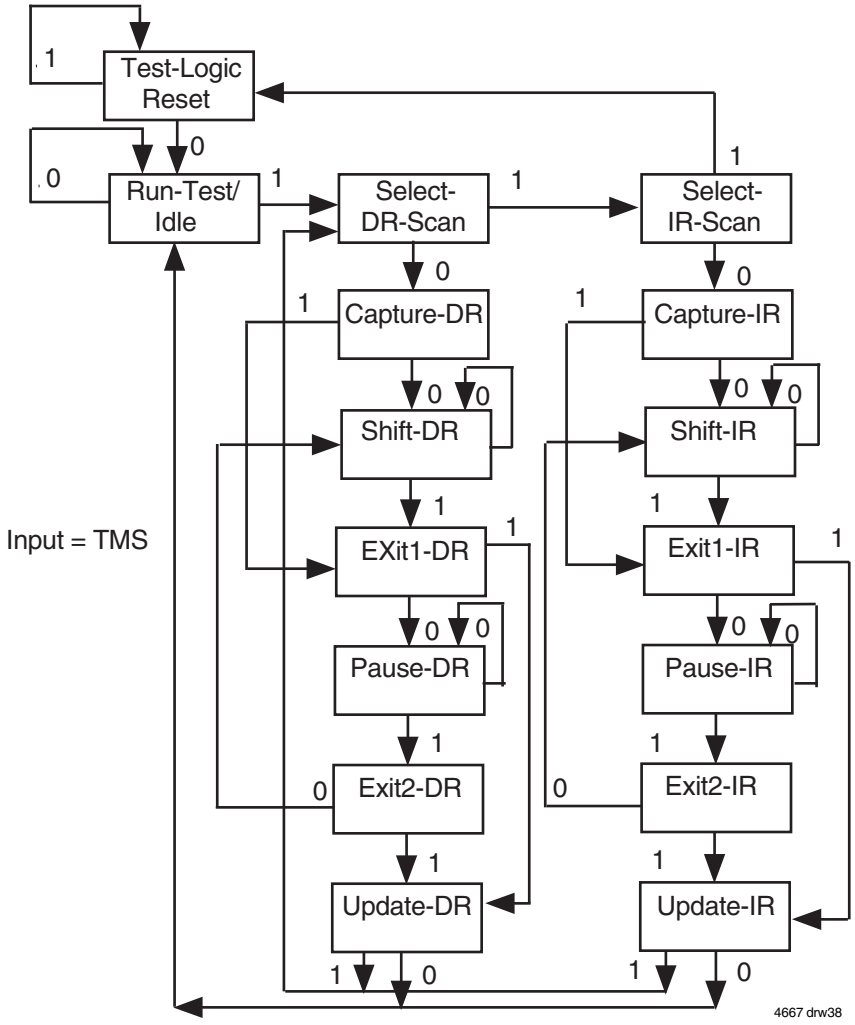
TEST ACCESS PORT (TAP)

The Tap interface is a general-purpose port that provides access to the internal of the processor. It consists of four input ports (TCLK, TMS, TDI, $\overline{TRST}$) and one output port (TDO).

THE TAP CONTROLLER

The Tap controller is a synchronous finite state machine that responds to TMS and TCLK signals to generate clock and control signals to the Instruction and Data Registers for capture and update of data.

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NOTES:
1. Five consecutive TCK cycles with TMS = 1 will reset the TAP.
2. TAP controller does not automatically reset upon power-up. The user must provide a reset to the TAP controller (either by $\overline{TRST}$ or TMS).
3. TAP controller must be reset before normal FIFO operations can begin.

Figure 33. TAP Controller State Diagram

Refer to the IEEE Standard Test Access Port Specification (IEEE Std. 1149.1) for the full state diagram

All state transitions within the TAP controller occur at the rising edge of the TCLK pulse. The TMS signal level (0 or 1) determines the state progression that occurs on each TCLK rising edge. The TAP controller takes precedence over the FIFO memory and must be reset after power up of the device. See $\overline{TRST}$ description for more details on TAP controller reset.

CAPTURE-DR

Data is loaded from the parallel input pins or core outputs into the Data Register.

SHIFT-DR

The previously captured data is shifted in serially, LSB first at the rising edge of TCLK in the TDI/TDO path and shifted out serially, LSB first at the falling edge of TCLK towards the output.

UPDATE-DR

The shifting process has been completed. The data is latched into their parallel outputs in this state to be accessed through the internal bus.

EXIT1-DR / EXIT2-DR

This is a temporary controller state. If TMS is held high, a rising edge applied to TCK while in this state causes the controller to enter the Update-DR state. This terminates the scanning process. All test data registers selected by the current instruction retain their previous state unchanged.

PAUSE-DR

This controller state allows shifting of the test data register in the serial path between TDI and TDO to be temporarily halted. All test data registers selected by the current instruction retain their previous state unchanged.

Capture-IR, Shift-IR and Update-IR, Exit-IR and Pause-IR are similar to Data registers. These instructions operate on the instruction registers.

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THE INSTRUCTION REGISTER

The Instruction register allows an instruction to be shifted in serially into the processor at the rising edge of TCLK.

The Instruction is used to select the test to be performed, or the test data register to be accessed, or both. The instruction shifted into the register is latched at the completion of the shifting process when the TAP controller is at Update-IR state.

The instruction register must contain 4 bit instruction register-based cells which can hold instruction data. These mandatory cells are located nearest the serial outputs they are the least significant bits.

TEST DATA REGISTER

The Test Data register contains three test data registers: the Bypass, the Boundary Scan register and Device ID register.

These registers are connected in parallel between a common serial input and a common serial data output.

The following sections provide a brief description of each element. For a complete description, refer to the IEEE Standard Test Access Port Specification (IEEE Std. 1149.1-1990).

TEST BYPASS REGISTER

The register is used to allow test data to flow through the device from TDI to TDO. It contains a single stage shift register for a minimum length in serial path. When the bypass register is selected by an instruction, the shift register stage is set to a logic zero on the rising edge of TCLK when the TAP controller is in the Capture-DR state.

The operation of the bypass register should not have any effect on the operation of the device in response to the BYPASS instruction.

THE BOUNDARY-SCAN REGISTER

The Boundary Scan Register allows serial data TDI be loaded in to or read out of the processor input/output ports. The Boundary Scan Register is a part of the IEEE 1149.1-1990 Standard JTAG Implementation.

THE DEVICE IDENTIFICATION REGISTER

The Device Identification Register is a Read Only 32-bit register used to specify the manufacturer, part number and version of the processor to be determined through the TAP in response to the IDCODE instruction.

IDT JEDEC ID number is 0xB3. This translates to 0x33 when the parity is dropped in the 11-bit Manufacturer ID field.

For the IDT72V3640/72V3650/72V3660/72V3670/72V3680/72V3690, the Part Number field contains the following values:

Device	Part# Field
IDT72V3640	04E5
IDT72V3650	04E4
IDT72V3660	04E3
IDT72V3670	04E2
IDT72V3680	04E1
IDT72V3690	04E0

31(MSB) 28	27 12	11 1	0(LSB)
Version (4 bits) 0X0	Part Number (16-bit)	Manufacturer ID (11-bit) 0X33	1

IDT72V3640/50/60/70/80/90 JTAG Device Identification Register

JTAG INSTRUCTION REGISTER

The Instruction register allows instruction to be serially input into the device when the TAP controller is in the Shift-IR state. The instruction is decoded to perform the following:

- Select test data registers that may operate while the instruction is current. The other test data registers should not interfere with chip operation and the selected data register.
- Define the serial test data register path that is used to shift data between TDI and TDO during data register scanning.

The Instruction Register is a 4 bit field (i.e.IR3, IR2, IR1, IR0) to decode 16 different possible instructions. Instructions are decoded as follows.

Hex Value	Instruction	Function
0x00	EXTEST	Select Boundary Scan Register
0x02	IDCODE	Select Chip Identification data register
0x01	SAMPLE/PRELOAD	Select Boundary Scan Register
0x03	HI-Z	JTAG
0x0F	BYPASS	Select Bypass Register

Table 6. JTAG Instruction Register Decoding

The following sections provide a brief description of each instruction. For a complete description refer to the IEEE Standard Test Access Port Specification (IEEE Std. 1149.1-1990).

EXTEST

The mandatory EXTEST instruction is provided for external circuity and board level interconnection check.

IDCODE

This instruction is provided to select Device Identification Register to read out manufacture's identity, part number and version number.

SAMPLE/PRELOAD

The mandatory SAMPLE/PRELOAD instruction allows data values to be loaded onto the latched parallel outputs of the boundary-scan shift register prior to selection of the boundary-scan test instruction. The SAMPLE instruction allows a snapshot of data flowing from the system pins to the on-chip logic or vice versa.

HIGH-Z

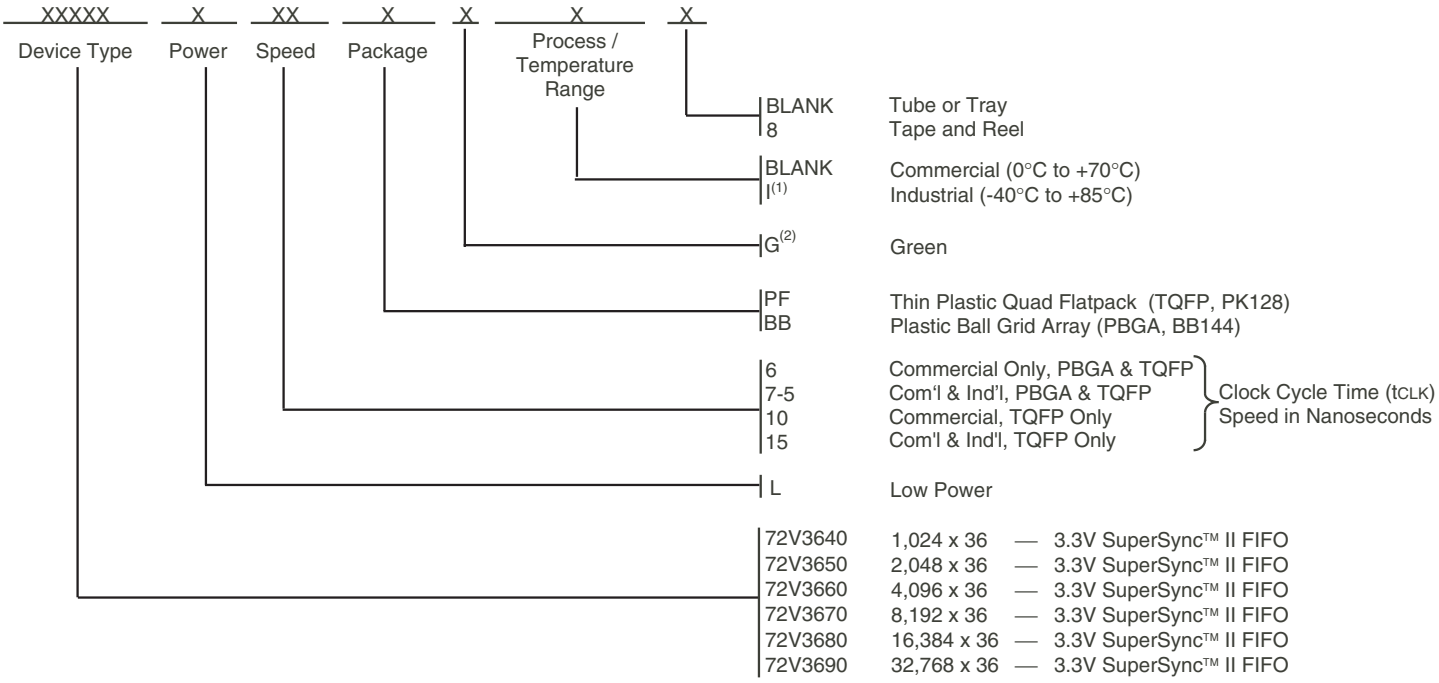
This instruction places all the output pins on the device into a high impedance state.

BYPASS

The Bypass instruction contains a single shift-register stage and is set to provide a minimum-length serial path between the TDI and the TDO pins of the device when no test operation of the device is required.

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ORDERING INFORMATION



4667 drw 39

NOTES:

1. Industrial temperature range product for 7-5ns and 15ns are available as standard device. All other speed grades are available by special order.
2. Green parts are available. For specific speeds and packages contact your sales office.
   LEAD FINISH (SnPb) parts are in EOL process. Product Discontinuation Notice - PDN# SP-17-02

DATASHEET DOCUMENT HISTORY

05/25/2000	pgs. 1, 6, 7, 8, 34, and 35.
07/28/2000	pgs. 13, 14, and 34.
12/14/2000	pgs. 6, 7, and 8.
03/27/2001	pg. 7.
04/06/2001	pgs. 4, 5, and 18.
12/14/2001	pgs. 1-46.
12/20/2001	pg. 9.
03/25/2002	pg. 42.
04/19/2002	pg. 3.
05/24/2002	pgs. 3, and 11.
01/20/2003	pgs. 1, 7, 9, 10, and 16.
02/11/2003	pgs. 7, and 44.
07/15/2003	pgs. 3, 19, and 37-39.
09/29/2003	pg. 8.
11/02/2005	pgs. 1, 8-10, and 46.
04/06/2006	pg. 4.
10/22/2008	pg. 46.
10/31/2014	pg. 1-3 and 46.
03/19/2018	Product Discontinuation Notice - PDN# SP-17-02 Last time buy expires June 15, 2018.
08/06/2018	pg. 3.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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