A1357

Two-Wire High Precision Linear Hall-Effect Sensor IC With Pulse Width Modulated Output Current

Discontinued Product

This device is no longer in production. The device should not be purchased for new design applications. Samples are no longer available.

Date of status change: September 29, 2023

Recommended Substitutions:

For existing customer transition, and for new customers or new applications, contact Allegro Sales.

NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

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Two-Wire High Precision Linear Hall-Effect Sensor IC With Pulse Width Modulated Output Current

FEATURES AND BENEFITS

- Two-wire output enables reduced wiring costs in long wire systems
- Simultaneous programming of PWM carrier frequency, quiescent duty cycle (QDC), and sensitivity for system optimization
- Fully differential signal path increases EMC immunity and reduces output offset drifts
- Factory-programmed sensitivity temperature coefficient and quiescent duty cycle drift
- Programmability at end-of-line
- Pulse width modulated (PWM) current output provides increased noise and EMC immunity compared to an analog output
- Precise recoverability after temperature cycling
- Duty cycle clamps provide short circuit diagnostic capabilities
- Optional 50% duty cycle calibration test mode at device power up
- Wide ambient temperature range: –40°C to 150°C
- Resistant to mechanical stress

PACKAGE:

3-pin SIP (suffix KB)

Not to scale



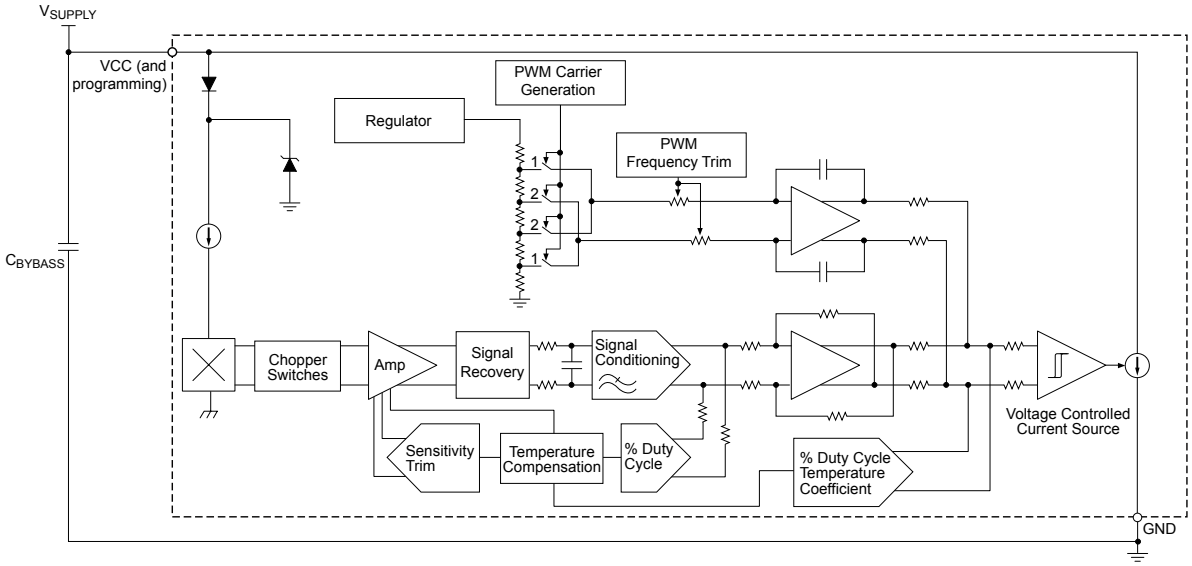
DESCRIPTION

The A1357 device is a high precision, programmable two-wire Hall-effect linear sensor IC with a pulse width modulated (PWM) current. The A1357 device converts an analog signal from its internal Hall sensor element to a digitally encoded PWM signal. The coupled noise immunity of the digitally encoded PWM is far superior to the noise immunity of an analog output signal.

The BiCMOS, monolithic circuit inside of the A1357 integrates a Hall element, precision temperature-compensating circuitry to reduce the intrinsic sensitivity and offset drift of the Hall element, a small-signal high-gain amplifier, proprietary dynamic offset cancellation circuits, and PWM conversion circuitry. The dynamic offset cancellation circuits reduce the residual offset voltage of the Hall element that is normally caused by device overmolding, temperature dependencies, and thermal stress. The high frequency offset cancellation (chopping) clock allows for a greater sampling rate, which increases the accuracy of the output current signal and results in faster signal processing capability.

The A1357 sensor is provided in a lead (Pb) free 3-pin single inline package (KB suffix), with 100% matte tin leadframe plating.

Functional Block Diagram



SELECTION GUIDE

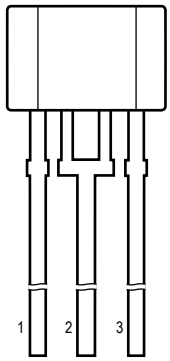
Part Number	Packing*
A1357LKB-T	500 pieces per bag
A1357LKBTN-T	4000 pieces per 13-in. reel

*Contact Allegro™ for additional packing options

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{CC}		28	V
Reverse Supply Voltage	V_{RCC}		–18	V
Forward Supply Current	I_{CC}		50	mA
Reverse Supply Current	I_{RCC}		–50	mA
Operating Ambient Temperature	T_A	L temperature range	–40 to 150	°C
Maximum Junction Temperature	T_J(max)		165	°C
Storage Temperature	T_{stg}	V_{CC} = 0 V	–65 to 170	°C

Pinout Diagram



Terminal List Table

Number	Name	Function
1	VCC	Input power supply; use bypass capacitor to connect to ground; also used for programming
2	GND	Ground
3	NC	No connect

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OPERATING CHARACTERISTICS: Valid over full operating temperature range, T_A, V_{CC} = 4.5 to 18 V, C_{BYPASS} = 0.1 µF, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit [1]
ELECTRICAL CHARACTERISTICS						
Supply Voltage [2]	V_{CC}		4.5	–	18	V
Supply Current	I_{CC_LOW}		–	6	8	mA
	I_{CC_HIGH}		12	–	16.5	mA
Supply Current Ratio			2	–	–	–
Supply Zener Clamp Voltage	$V_{Zsupply}$	I_{CC} = 18 mA, T_A = 25°C	28	–	–	V
Power-On Time [3][4]	t_{PO}	f_{pwm} = 1 kHz	–	–	5	ms
Internal Bandwidth	BW_i	Small signal –3 dB, 100 $G_{(P-P)}$ magnetic input signal, T_A = 25 C°	–	400	–	Hz
Chopping Frequency [5]	f_C	T_A = 25°C	–	200	–	kHz
OUTPUT CURRENT CHARACTERISTICS						
PWM_{OUT} Rise Time [3][4]	t_r	VCC pin, No C_{BYPASS} or R_{SENSE}, T_A = 25°C	–	6.5	–	mA/µs
PWM_{OUT} Fall Time [3][4]	t_f	VCC pin, No C_{BYPASS} or R_{SENSE}, T_A = 25°C	–	6.5	–	mA/µs
Maximum Propagation Delay [3][4]	t_{PROP}	T_A = 25 C°	–	2	3	ms
Response Time [3][4]	$t_{RESPONSE}$	Impulse magnetic field of 300 G, f_{pwm} = 1 kHz, slew rate < 120 G/ms, T_A = 25°C	–	2	3.125	ms
Duty Cycle Jitter [3][4][6]	$Jitter_{PWM}$	Measured over 1000 output PWM clock periods, 3 sigma values, Sens = 60 m% / G, T_A = 25°C	–	–	±0.090	% D
Clamp Duty Cycle	$D_{CLP(HIGH)}$		90	–	95	% D
	$D_{CLP(LOW)}$		5	–	10	% D
PRE-PROGRAMMING TARGET [7]						
Pre-Programming Quiescent Current Duty Cycle	$D_{(Q)PRE}$	B = 0 G, T_A = 25°C	–	50	–	% D
Pre-Programming Sensitivity	$Sens_{PRE}$	T_A = 25°C	–	25	–	(m% D)/G
Pre-Programming PWM_{OUT} Carrier Frequency	f_{PWMPRE}	T_A = 25°C	–	1.5	–	kHz
QUIESCENT CURRENT DUTY CYCLE PROGRAMMING						
Initial Quiescent Current Duty Cycle	$D_{(Q)init}$	B = 0 G, T_A = 25°C	–	$D_{(Q)PRE}$	–	% D
Guaranteed Quiescent Current Duty Cycle Output Range [8]	$D_{(Q)}$	B = 0 G, T_A = 25°C	40	–	60	% D
Quiescent Current Duty Cycle Programming Bits			–	9	–	bit
Average Quiescent Current Duty Cycle Step Size [9][10]	$Step_{D(Q)}$	T_A = 25°C	0.091	0.103	0.115	% D
Quiescent Current Duty Cycle Programming Resolution [11]	$Err_{PGD(Q)}$	T_A = 25°C	–	$Step_{D(Q)}$ × ±0. 5	–	% D

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OPERATING CHARACTERISTICS (continued): Valid over full operating temperature range, T_A, V_{CC} = 4.5 to 18 V, C_{BYPASS} = 0.1 µF, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SENSITIVITY PROGRAMMING						
Initial Sensitivity	$Sens_{init}$	T_A = 25°C	–	$Sens_{PRE}$	–	(% D)/G
Sensitivity Programming Bits	Range_ Selection	T_A = 25°C	–	1	–	bit
	Fine	T_A = 25°C	–	8	–	bit
Guaranteed Sensitivity Range	$Sens_{Range1}$	T_A = 25°C	35	–	70	(m% D)/G
	$Sens_{Range2}$	T_A = 25°C	70	–	145	(m% D)/G
Average Sensitivity Step Size [9][10]	$Step_{SENS1}$	T_A = 25°C	215	300	375	(µ% D)/G
	$Step_{SENS2}$	T_A = 25°C	430	600	750	(µ% D)/G
Sensitivity Programming Resolution [11]	Err_{PGSENS}	T_A = 25°C	–	$Step_{SENS}$ × ±0. 5	–	(µ% D)/G
CARRIER FREQUENCY PROGRAMMING						
Initial Carrier Frequency	$f_{PWMinit}$	T_A = 25°C	–	f_{PWMPRE}	–	Hz
Carrier Frequency Programming Range	f_{PWM}	T_A = 25°C	0.9	1	1.1	kHz
Carrier Frequency Programming Bits			–	4	–	bit
Average Carrier Frequency Step Size [9][10]	$Step_{fPWM}$	T_A = 25°C	38	54	70	Hz
Carrier Frequency Programming Resolution [11]	Err_{PGfPWM}	T_A = 25°C	–	$Step_{fPWM}$ × ±0. 5	–	Hz
CALIBRATION TEST MODE						
Calibration Test Mode Selection Bit			–	1	–	bit
Calibration Test Mode Duration [4]	t_{CAL}	f_{PWM} = 1 kHz	45	50	55	ms
Output Duty Cycle During Calibration Mode [4]	D_{CAL}		49	50	51	% D
LOCK BIT PROGRAMMING						
Overall Programming Lock Bit	LOCK		–	1	–	bit
FACTORY-PROGRAMMED SENSITIVITY TEMPERATURE COEFFICIENT AND DRIFT CHARACTERISTICS						
Sensitivity Temperature Coefficient [12]	$Sens_{TC_NdFeB}$	T_A = 150°C	–	0.11	–	%/°C
Sensitivity Drift Through Temperature Range [13]	$\Delta Sens_{TC}$	T_A = 150°C	–	< ±3	–	%
Sensitivity Drift Due to Package Hysteresis [3]	$\Delta Sens_{PKG}$	T_A = 150°C, after temperature cycling	–	< ±1	–	%

Continued on the next page…

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OPERATING CHARACTERISTICS (continued): Valid over full operating temperature range, T_A, V_{CC} = 4.5 to 18 V, C_{BYPASS} = 0.1 µF, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
FACTORY-PROGRAMMED QUIESCENT CURRENT DUTY CYCLE DRIFT						
Quiescent Current Duty Cycle Temperature Coefficient [12]	$D_{TC(Q)}$	T_A = 150°C	–	0	–	(% D)/°C
Quiescent Current Duty Cycle Drift Through Temperature Range [14]	$\Delta D_{(Q)}$	Sens = $Sens_{PRE}$, T_A = 150°C	–	< ±0.35	–	% D
ERROR COMPONENTS						
Linearity Sensitivity Error	Lin_{ERR}		–	< ±1.5	–	%
Symmetry Sensitivity Error	Sym_{ERR}		–	< ±1.5	–	%

[1] 1 G (gauss) = 0.1 mT (millitesla).
[2] Supply Voltage is the voltage drop between device supply and ground pins. It does not include a drop through a sense resistor.
[3] See Characteristic Definitions section.
[4] Guaranteed by design only. Characterized but not tested in production.
[5] f_C varies up to approximately ±20% through the full operating ambient temperature range, T_A, and process.
[6] Jitter is dependent on the sensitivity of the device.
[7] Raw device characteristic values before any programming.
[8] $D_{(Q)}$(max) is the value available with all programming fuses blown (maximum programming code set). The $D_{(Q)}$ range is the total range from $D_{(Q)}$ (min) up to and including $D_{(Q)}$(max). See Characteristic Definitions section.
[9] Step size is larger than required, in order to provide for manufacturing spread. See Characteristic Definitions section.
[10] Non-ideal behavior in the programming DAC can cause the step size at each significant bit rollover code to be greater than twice the maximum specified value of $Step_{D(Q)}$, $Step_{SENS}$, or $Step_{fPWM}$.
[11] Overall programming value accuracy. See Characteristic Definitions section.
[12] Programmed at 150°C and calculated relative to 25°C.
[13] Sensitivity drift from expected value at T_A after programming $SENS_{TC}$. See Characteristic Definitions section.
[14] $D_{(Q)}$ drift from expected value at T_A after programming $D_{TC(Q)}$.

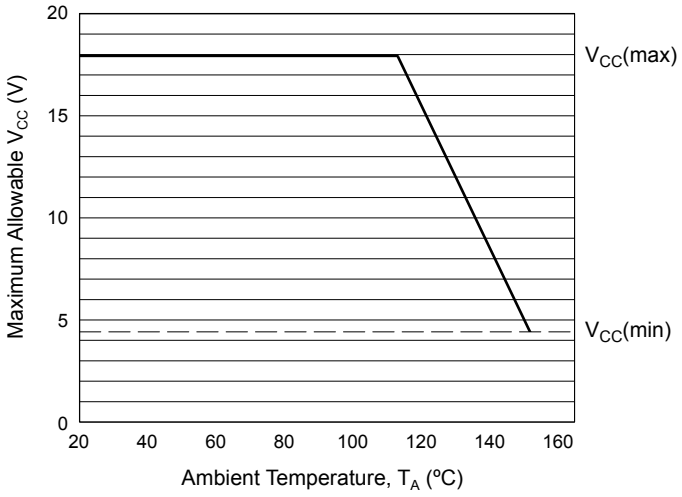
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THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

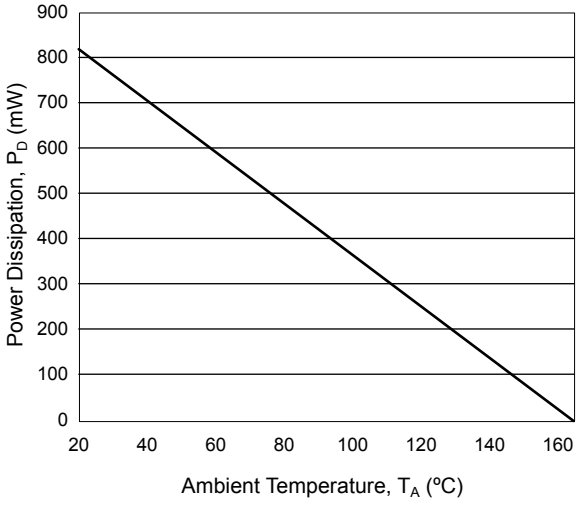
Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	1-layer PCB with copper limited to solder pads	177	°C/W

*Additional thermal data available on the Allegro website.

Power Derating Curve



Power Dissipation versus Ambient Temperature



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CHARACTERISTIC DEFINITIONS

Power-On Time. When the supply is ramped to its operating voltage, the device requires a finite time to power its internal components before supplying a valid PWM output duty-cycle. Power-On Time, t_{PO}, is defined as the time it takes for the output voltage to settle within ±10% of its steady state value after the power supply has reached its minimum specified operating voltage, V_{CC}(min). (See figure 1.)

Propagation Delay. Traveling time of signal from input Hall plate to output stage of device. (See figure 2.)

Response Time. The time interval, $t_{RESPONSE}$, between a) when the applied magnetic field reaches 90% of its final value, and b) when the sensor IC reaches 90% of its output corresponding to the applied magnetic field. (See figure 2.)

PWM_{OUT} Rise Time. The time, t_r, elapsed between 10% and 90% of the rising signal value when output current switches from low to high states.

PWM_{OUT} Fall Time. The time, t_f, elapsed between 90% and 10% of the falling signal value when output current switches from high to low states.

Quiescent Current Duty Cycle. In the quiescent state (no significant magnetic field: B = 0 G), the Quiescent Current Duty Cycle, $D_{(Q)}$, equals a specific programmed duty cycle throughout the entire operating ranges of V_{CC} and ambient temperature, T_A.

Guaranteed Quiescent Current Duty Cycle Range. The Quiescent Current Duty Cycle, $D_{(Q)}$, can be programmed around its nominal value of 50% D, within the Guaranteed Quiescent Duty Cycle Range limits: $D_{(Q)}$(min) and $D_{(Q)}$(max). The available guaranteed programming range for $D_{(Q)}$ falls within the distributions of the minimum and the maximum programming code for setting $D_{(Q)}$. (See figure 3.)

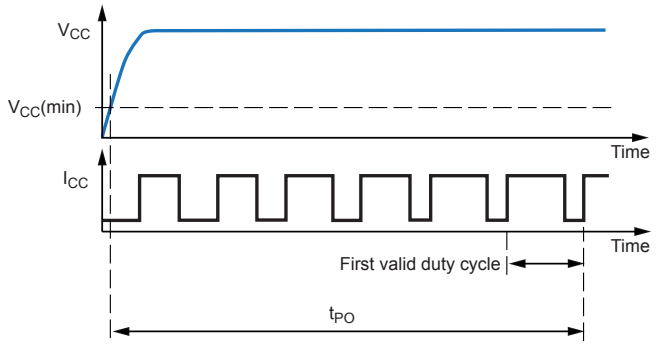


Figure 1. Definition of Power-On Time

Average Quiescent Current Duty Cycle Step Size. The Average Quiescent Current Duty Cycle Step Size, $Step_{D(Q)}$, for a single device is determined using the following calculation:

$$Step_{D(Q)} = \frac{D_{(Q)}(max) - D_{(Q)}(min)}{2^n - 1} \quad , \qquad (1)$$

where:

n is the number of available programming bits in the trim range,

$2^n - 1$ is the value of programming steps in the range,

$D_{(Q)}$(max) is the maximum reached quiescent duty cycle, and

$D_{(Q)}$(min) is minimum reached quiescent duty cycle.

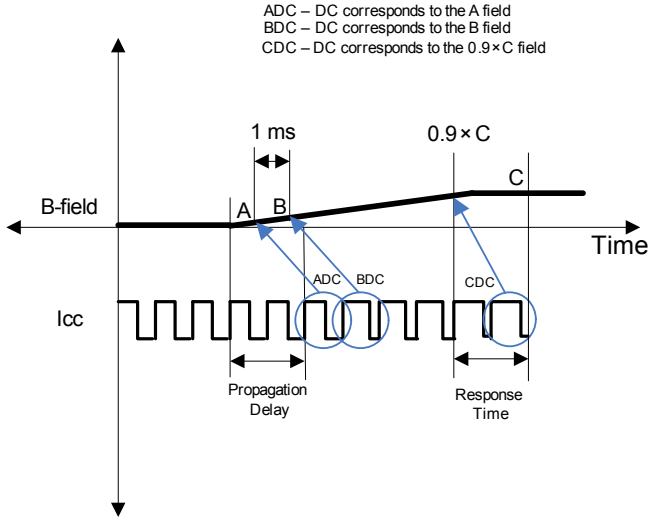


Figure 2. Definitions of Propagation Delay and Response Time

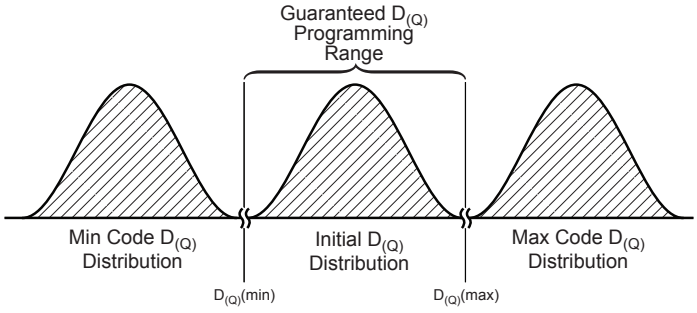


Figure 3. Definition of Guaranteed Quiescent Voltage Output Range

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Quiescent Current Duty Cycle Output Programming Resolution. The programming resolution for any device is half of its programming step size. Therefore, the typical programming resolution will be:

$$Err_{PGD(Q)}(typ) = 0.5 \times Step_{D(Q)}(typ) \quad . \qquad (2)$$

Quiescent Duty Cycle Output Drift through Temperature Range. Due to internal component tolerances and thermal considerations, the Quiescent Duty Cycle Temperature Coefficient, $D_{TC(Q)}$, may drift from its nominal value over the operating ambient temperature, T_A. For purposes of specification, the Quiescent Duty Cycle Output Drift Through Temperature Range, $\Delta D_{(Q)}$ (% D), is defined as:

$$\Delta D_{(Q)} = D_{(Q)(TA)} - D_{(Q)(25°C)} \quad , \qquad (3)$$

where $D_{(Q)(TA)}$ is the quiescent duty cycle measured at T_A and $D_{(Q)(25°C)}$ is the quiescent duty cycle measured at 25°C.

Sensitivity. The presence of a south polarity magnetic field, perpendicular to the branded surface of the package face, increases the current duty cycle from its quiescent value toward the maximum duty cycle limit. The amount of the current duty cycle increase is proportional to the magnitude of the magnetic field applied. Conversely, the application of a north polarity field decreases the current duty cycle from its quiescent value. This proportionality is specified as the magnetic Sensitivity, Sens ((% D)/G), of the device, and it is defined for bipolar devices as:

$$Sens = \frac{D_{(BPOS)} - D_{(BNEG)}}{BPOS - BNEG} \quad , \qquad (4)$$

and for unipolar devices as:

$$Sens = \frac{D_{(BPOS)} - D_{(Q)}}{BPOS} \quad , \qquad (5)$$

where BPOS and BNEG are two magnetic fields with opposite polarities.

Guaranteed Sensitivity Range. The magnetic Sensitivity can be programmed from its initial value, $Sens_{init}$, to a value within the Guaranteed Sensitivity Range limits: $Sens_{Range}(min)$ and $Sens_{Range}(max)$.

Average Sensitivity Step Size. Refer to the Average Quiescent Current Duty Cycle Step Size section for a conceptual explanation.

Sensitivity Programming Resolution. Refer to the Quiescent Current Duty Cycle Programming Resolution section for a conceptual explanation.

Carrier Frequency Target. The PWM_{OUT} signal Carrier Frequency Programming Range, f_{PWM}, can be programmed to its typical value of 1 kHz.

Average Carrier Frequency Step Size. Refer to the Average Quiescent Current Duty Cycle Step Size section for a conceptual explanation.

Carrier Frequency Programming Resolution. Refer to the Quiescent Durrent Duty Cycle Programming Resolution section for a conceptual explanation.

Sensitivity Temperature Coefficient. Device sensitivity changes as temperature changes, with respect to its programmed Sensitivity Temperature Coefficient, $Sens_{TC}$. $Sens_{TC}$ is programmed at 150°C, and calculated relative to the nominal sensitivity programming temperature of 25°C. $Sens_{TC}$ (%/°C) is defined as:

$$Sens_{TC} = \left(\frac{Sens_{T2} - Sens_{T1}}{Sens_{T1}} \times 100\%\right)\left(\frac{1}{T2 - T1}\right) \quad , \qquad (6)$$

where T1 is the nominal Sens programming temperature of 25°C, and T2 is the programming temperature of 150°C. The expected value of Sens through the full ambient temperature range, $Sens_{EXPECTED(TA)}$, is defined as:

$$Sens_{EXPECTED(TA)} = \frac{Sens_{T1} \times [100\% + Sens_{TC}(T_A - T1)]}{100\ \%} \quad . \qquad (7)$$

$Sens_{EXPECTED\ (TA)}$ should be calculated using the actual measured values of $Sens_{T1}$ and $Sens_{TC}$ rather than programming target values.

Sensitivity Drift Through Temperature Range. Second order Sensitivity Temperature Coefficient effects cause the magnetic Sensitivity, Sens, to drift from its expected value through the operating ambient temperature range, T_A. For purposes of specification, the Sensitivity Drift Through Temperature Range, $\Delta Sens_{TC}$, is defined as:

$$\Delta Sens_{TC} = \frac{Sens_{TA} - Sens_{EXPECTED(TA)}}{Sens_{EXPECTED(TA)}} \times 100\% \quad . \qquad (8)$$

Sensitivity Drift Due to Package Hysteresis. Package stress and relaxation can cause the device Sensitivity at T_A = 25°C to change during and after temperature cycling.

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For purposes of specification, the Sensitivity Drift Due to Package Hysteresis, $\Delta Sens_{PKG}$, is defined as:

$$\Delta Sens_{PKG} = \frac{Sens_{(25°C)2} - Sens_{(25°C)1}}{Sens_{(25°C)1}} \times 100\% \quad , \tag{9}$$

where $Sens_{(25°C)1}$ is the programmed value of sensitivity at T_A = 25°C, and $Sens_{(25°C)2}$ is the value of sensitivity at T_A = 25°C, after temperature cycling T_A up to 150°C, down to –40°C, and back to up 25°C.

Linearity Sensitivity Error. The A1357 is designed to provide a linear current output in response to a ramping applied magnetic field. Consider two magnetic fields, B1 and B2. Ideally, the sensitivity of a device is the same for both fields, for a given supply voltage and temperature. Linearity error is present when there is a difference between the sensitivities measured at B1 and B2.

Linearity Sensitivity Error is calculated separately for the positive (Lin_{ERRPOS}) and negative (Lin_{ERRNEG}) applied magnetic fields. Linearity error (%) is measured and defined as:

$$Lin_{ERRPOS} = \left(1 - \frac{Sens_{BPOS2}}{Sens_{BPOS1}}\right) \times 100\% \quad ,$$

$$Lin_{ERRNEG} = \left(1 - \frac{Sens_{BNEG2}}{Sens_{BNEG1}}\right) \times 100\% \quad , \tag{10}$$

where:

$$Sens_{Bx} = \frac{|D_{(Bx)} - D_{(Q)}|}{B_x} \quad . \tag{11}$$

and B_{POSx} and B_{NEGx} are positive and negative magnetic fields, with respect to the quiescent current duty cycle such that B_{POS2} = 2 × B_{POS1} and B_{NEG2} = 2 × B_{NEG1}.

Then:

$$Lin_{ERR} = \max(Lin_{ERRPOS}, Lin_{ERRNEG}) \quad . \tag{12}$$

Note that unipolar devices only have positive linearity error (Lin_{ERRPOS}).

Symmetry Sensitivity Error. The magnetic sensitivity of the A1357 device is constant for any two applied magnetic fields of equal magnitude and opposite polarities. Symmetry Sensitivity Error, Sym_{ERR} (%), is measured and defined as:

$$Sym_{ERR} = \left(1 - \frac{Sens_{BPOS}}{Sens_{BNEG}}\right) \times 100\% \quad , \tag{13}$$

where $Sens_{Bx}$ is as defined in equation 11, and BPOS and BNEG are positive and negative magnetic fields such that |BPOS| = |BNEG|. Note that the Symmetry Sensitivity Error specification is valid only for bipolar devices.

Duty Cycle Jitter. The duty cycle of the PWM_{OUT} output may vary slightly over time despite the presence of a constant applied magnetic field and a constant Carrier Frequency, f_{PWM}, for the PWM_{OUT} signal. This phenomenon is known as jitter, and is defined as:

$$Jitter_{PWM} = \left(\frac{1}{n}\sum_{i=1}^{n} D_{Bi}\right) \pm 3\,\sigma \quad , \tag{14}$$

where $D_{B1}, \ldots, D_{Bn}$ are the sampled duty cycles in a constant applied magnetic field, B, measured over 1000 PWM clock periods, and $Jitter_{PWM}$ is given in % D.

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TYPICAL APPLICATION CIRCUIT

The current switching performed by the Hall sensor IC can be observed as voltage switching. To do so, place a sense resistor, R_{SENSE}, between the supply and the A1357 VCC pin (see figure 4), or between the A1357 GND pin and ground (figure 5). There is an advantage to putting the sense resistor between the supply and the A1357 VCC pin, because the resistor can then provide additional device protection from supply transients.

When specifying value of the R_{SENSE} and the applied supply voltage in the application, the following equation must be applied, in order to provide enough voltage to allow the A1357 to power-up:

$$V_{SUPPLY} > R_{SENSE} \times I_{CC_HIGH}(max) + V_{CC}(min) \ , \quad (15)$$

where $I_{CC}(max)$ is the maximum A1357 supply current and $V_{CC}(min)$ is the A1357 minimum supply voltage.

Substituting into equation 15:

$$12 \text{ V} > R_{SENSE} \times 16.5 \text{ mA} + 4.5 \text{ V} \ ,$$

therefore:

$$R_{SENSE} \leq (12 - 4.5) \text{ V} / 16.5 \text{ mA}$$
$$\leq 454 \ \Omega \ .$$

It can be seen that R_{SENSE} is proportional to V_{SUPPLY}. The higher the value of R_{SENSE}, the higher the application supply voltage required.

The recommended minimum C_{BYPASS} value is 0.01 µF.

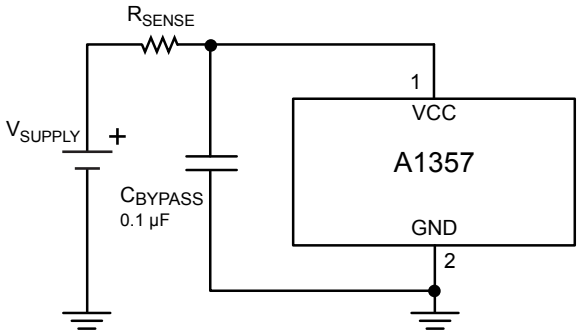


Figure 4. High-side PWM voltage sensing configuration

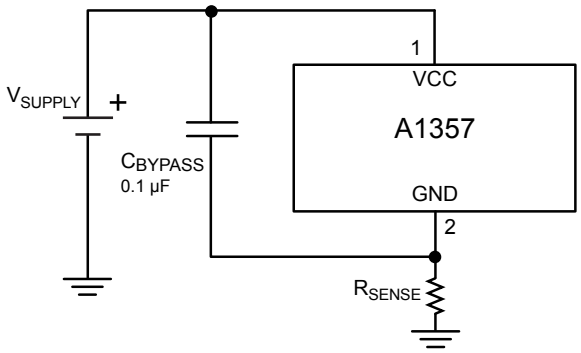


Figure 5. Low-side PWM voltage sensing configuration

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PROGRAMMING GUIDELINES

Overview

Programming is accomplished by sending a series of input voltage pulses serially through the VCC pin of the device. A unique combination of different voltage level pulses controls the internal programming logic of the device to select a programmable parameter and change its value. There are three voltage levels that must be taken into account when programming. These levels are referred to as *high*, $V_{P(HIGH)}$, *mid*, $V_{P(MID)}$, and *low*, $V_{P(LOW)}$.

The A1357 features Try mode, Blow mode and Lock mode:

- In Try mode, the value of multiple programmable parameters may be set and measured simultaneously. The parameter values are stored temporarily and reset after cycling the supply voltage.
- In Blow mode, the value of a single programmable parameter may be set and measured, and then permanently set by blowing solid-state fuses internal to the device. Additional parameters may be blown sequentially. This mode also is used for blowing the device-level fuse (when Lock mode is enabled), which permanently blocks the further programming of all parameters.
- Lock mode prevents all future programming of the device. This is accomplished by blowing a special fuse using Blow mode.

The programming sequence is designed to help prevent the device from being programmed accidentally; for example, as a result of noise on the supply line. Although any programmable variable power supply can be used to generate the pulse waveforms, Allegro highly recommends using the Allegro Sensor Evaluation Kit.

Definition of Terms

Register. The section of the programming logic that controls the choice of programmable modes and parameters.

Bit Field. The internal fuses unique to each register, represented as a binary number. Changing the bit field settings of a particular register causes its programmable parameter to change, based on the internal programming logic.

Key. A series of mid-level voltage pulses used to select a register, with a value expressed as the decimal equivalent of the binary value. The LSB of a register is denoted as key 1, or bit 0.

Code. The number used to identify the combination of fuses activated in a bit field, expressed as the decimal equivalent of the binary value. The LSB of a bit field is denoted as code 1, or bit 0.

Addressing. Increasing the bit field code of a selected register by serially applying a pulse train through the VCC pin of the device. Each parameter can be measured during the addressing process, but the internal fuses must be blown before the programming code (and parameter value) becomes permanent.

Fuse Blowing. Applying a high voltage pulse of sufficient duration to permanently set an addressed bit by blowing a fuse internal to the device. After a bit (fuse) has been blown, it cannot be reset.

Blow Pulse. A high voltage pulse of sufficient duration to blow the addressed fuse.

Cycling the Supply. Powering-down, and then powering-up the supply voltage. Cycling the supply is used to clear the programming settings in Try mode.

Programming Pulse Requirements, Protocol at T_A = 25 °C

Characteristic	Symbol	Notes	Min.	Typ.	Max.	Unit
Programming Voltage	$V_{P(LOW)}$	Measured at the VCC pin.	4.5	5	5.5	V
	$V_{P(MID)}$		13	15	16	V
	$V_{P(HIGH)}$		26	27	28	V
Programming Current	I_P	Minimum supply current required to ensure proper fuse blowing. In addition, a minimum capacitance, C_{BLOW} = 0.1 µF, must be connected between the supply and GND pins during programming to provide the current necessary for fuse blowing. The blowing capacitor should be removed, and the load capacitance used for properly programming duty cycle measurements.	300	–	–	mA
Pulse Width	t_{LOW}	Duration of $V_{P(LOW)}$ for separating $V_{P(MID)}$ and $V_{P(HIGH)}$ pulses.	40	–	–	µs
	t_{ACTIVE}	Duration of $V_{P(MID)}$ and $V_{P(HIGH)}$ pulses for register selection or bit field addressing.	40	–	–	µs
	t_{BLOW}	Duration of $V_{P(HIGH)}$ pulses for fuse blowing.	40	–	–	µs
Pulse Rise Time	t_{Pr}	Rise time required for transitions from $V_{P(LOW)}$ to either $V_{P(MID)}$ or $V_{P(HIGH)}$.	5	–	100	µs
Pulse Fall Time	t_{Pf}	Fall time required for transitions from $V_{P(HIGH)}$ to either $V_{P(MID)}$ or $V_{P(LOW)}$.	5	–	100	µs

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PROGRAMMING PROCEDURES

Mode and Parameter Selection

Each programmable mode and parameter can be accessed through specific registers. To select a register, a sequence of voltage pulses consisting of a $V_{P(HIGH)}$ pulse, a series of $V_{P(MID)}$ pulses, and a $V_{P(HIGH)}$ pulse (with no VCC supply interruptions) must be applied serially to the supply pin. The quantity of $V_{P(MID)}$ pulses is called the key, and uniquely identifies each register. The pulse train used for selection of the first register, key 1, is shown in figure 6.

The A1357 has two registers that select among the three programmable modes:

- Register Mode 1:

  Blow and Lock modes

- Register Mode 2:

  Try mode

And there are four registers that select among the four programmable parameters:

- Register 1:

  Sensitivity, Sens

- Register 2:

  Quiescent Current Duty Cycle, $D_{(Q)}$

- Register 3:

  Pulse width modulated carrier frequency, f_{PWM}

- Register 6:

  Lock (device locking)

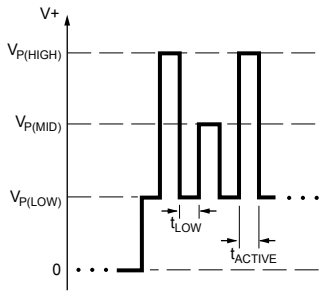


Figure 6. Parameter selection pulse train. This shows the sequence for selecting the register corresponding to key 1, indicated by a single $V_{P(MID)}$ pulse.

Bit Field Addressing

After a programmable parameter has been selected, a $V_{P(HIGH)}$ pulse transitions the programming logic into the bit field addressing state. Applying a series of $V_{P(MID)}$ pulses to the VCC pin of the device, as shown in figure 7, increases by one the bit field of the selected parameter.

When addressing the bit field, the quantity of $V_{P(MID)}$ pulses is represented by a decimal number called a *code*. Addressing activates the corresponding fuse locations in the given bit field by increasing the binary value of an internal DAC. The value of the bit field (and code) increases by one with the falling edge of each $V_{P(MID)}$ pulse, up to the maximum possible code (see the Programming Logic table). As the value of the bit field code increases, the value of the programmable parameter changes. Measurements can be taken after each pulse to determine if the required result for the programmable parameter has been reached. Cycling the supply voltage resets all the locations in the bit field that have unblown fuses to their initial states.

Fuse Blowing

After the required code is found for a given parameter, its value can be set permanently by blowing individual fuses in the appropriate register bit field. Blowing is accomplished by applying a $V_{P(HIGH)}$ pulse, called a *blow* pulse, of sufficient duration at the $V_{P(HIGH)}$ level to permanently set an addressed bit by blowing a fuse internal to the device. Due to power requirements, the fuse for each bit in the bit field must be blown individually. To accomplish this, the code representing the required parameter value must be translated to a binary number. For example, as shown in figure 8, decimal code 5 is equivalent to the binary number 101. Therefore bit 2 (code 4) must be addressed and blown, the device power supply cycled, and then bit 0 (code 1) addressed

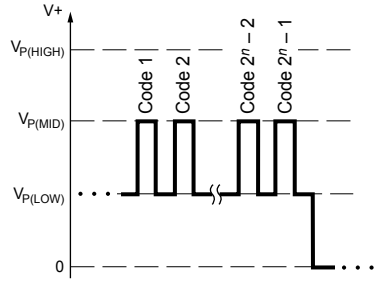


Figure 7. Bit field addressing pulse train. Addressing the bit field by increasing the code causes the programmable parameter value to change. The number of bits available for a given programming code, *n*, varies among parameters; for example, the bit field for $D_{(Q)}$ has 8 bits available, which allows 255 separate codes to be used.

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and blown. An appropriate sequence for blowing code 5 is shown in figure 9. The order of blowing bits, however, is not important. Blowing bit 0 first, and then bit 2 is acceptable.

Note: After blowing, the programming is not reversible, even after cycling the supply power. Although a register bit field fuse cannot be reset after it is blown, additional bits within the same register can be blown at any time until the device is locked. For example, if bit 1 (binary 10) has been blown, it is still possible to blow bit 0. The end result would be binary 11 (decimal code 3).

Locking the Device

After the required code for each parameter is programmed, the device can be locked to prevent further programming of any parameters.

Additional Guidelines

The additional guidelines presented in this section should be followed to ensure the proper behavior of these devices:

- A 0.1 µF blowing capacitor, C_{BLOW}, must be mounted between the VCC pin and the GND pin during programming, to ensure enough current is available to blow fuses.

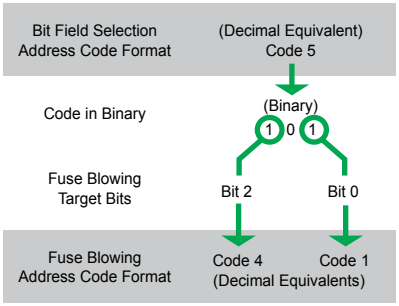


Figure 8. Example of code 5 broken into its binary components, which are code 4 and code 1.

- The application load capacitance, C_L, should be used when measuring the duty cycle during programming. The blowing capacitor, C_{BLOW}, should be removed during measurement and should only be applied when blowing fuses.
- The blowing capacitor, C_{BLOW}, must be replaced in the final application with the load capacitance, C_L, for proper operation.
- The power supply used for programming must be capable of delivering at least 26 V and 300 mA.
- Be careful to observe the t_{LOW} delay time before powering down the device after blowing each bit.
- The following programming order is recommended:

  1. f_{PWM}
  2. Sens
  3. $D_{(Q)}$
  4. Lock the device (only after all other parameters have been programmed and validated, because this prevents any further programming of the device)

Programming Modes

Try Mode. Try mode allows multiple programmable parameters to be tested simultaneously without permanently setting any values. In this mode, each $V_{P(HIGH)}$ pulse will indefinitely loop the programming logic through the mode, register, and bit field selection states. There must be no interruptions in the V_{CC} supply.

After powering the V_{CC} supply, select mode key 2, followed by the parameter register, and then address its bit field. When addressing the bit field, each $V_{P(MID)}$ pulse increases the value of the parameter register by one, up to the maximum possible code (see Programming Logic section). The addressed parameter value is stored in the device even after the programming drive voltage is removed from the VCC pin, allowing its value to be measured. To test an additional programmable parameter in

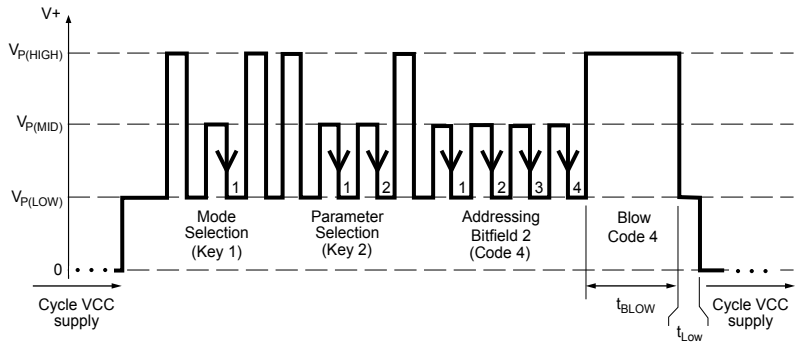


Figure 9. Example of Blow Mode programming pulses applied to the VCC pin. In this example, $D_{(Q)}$ (Parameter Key 2) is addressed to code 4 (i.e bit 2) and its value is permanently blown.

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conjunction with the original, enter an additional $V_{P(HIGH)}$ pulse on the VCC pin to reenter the parameter selection field. Select a different parameter register, and address its bit field, without any supply interruptions. Both parameter values will be stored and can be measured after removing the programming drive voltage. Multiple programming combinations can be tested to achieve optimal application accuracy. See figure 10 for an example of the Try mode pulse train.

Registers can be addressed and re-addressed an indefinite number of times in any order. After the required code is found for each register, cycle the supply and blow the bit field using Blow mode.

Blow Mode. After the required value of the programmable parameter is found using Try mode, the corresponding code should be blown to make the value permanent. To do this, first select Blow mode as key 1, then the required parameter register, and address and blow each required bit separately (as described in the Fuse Blowing section). The supply must be cycled between blowing each bit of a given code. After a bit is blown, cycling the supply will not reset its value.

Single parameters can be still addressed in the Blow mode before fuse blowing. Simultaneous addressing of multiple parameters, as in Try mode, is not possible. After powering the V_{CC} supply, select the desired parameter register and address its bit field. When addressing the bit field, each $V_{P(MID)}$ pulse increases the value of the parameter register by one, up to the maximum possible code (see Programming Logic table). The addressed parameter value is stored in the device even after the programming drive voltage is removed from the VCC pin, allowing its value to be measured. It is not possible to decrease the value of the register without resetting the parameter bit field. To reset the bit field, and thus the value of the programmable parameter, cycle the supply, V_{CC}, voltage.

It is possible to switch between Try and Blow modes in that, after individual programmable parameters have been blown in Blow mode, other parameters can be still tested in Try mode.

Lock Mode. To lock the device, first select Lock mode, then address the Lock bit and apply a blow pulse with C_{BLOW} in place. After locking the device, no future programming of any parameter is possible.

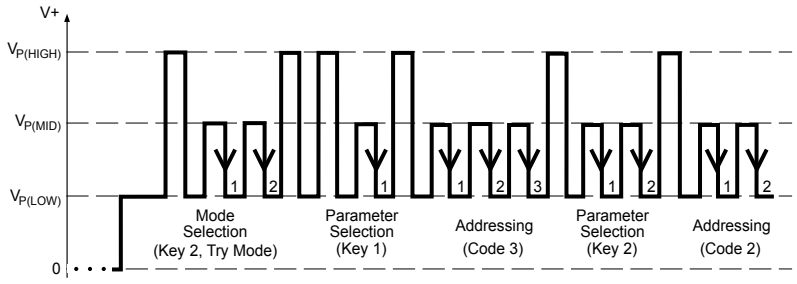
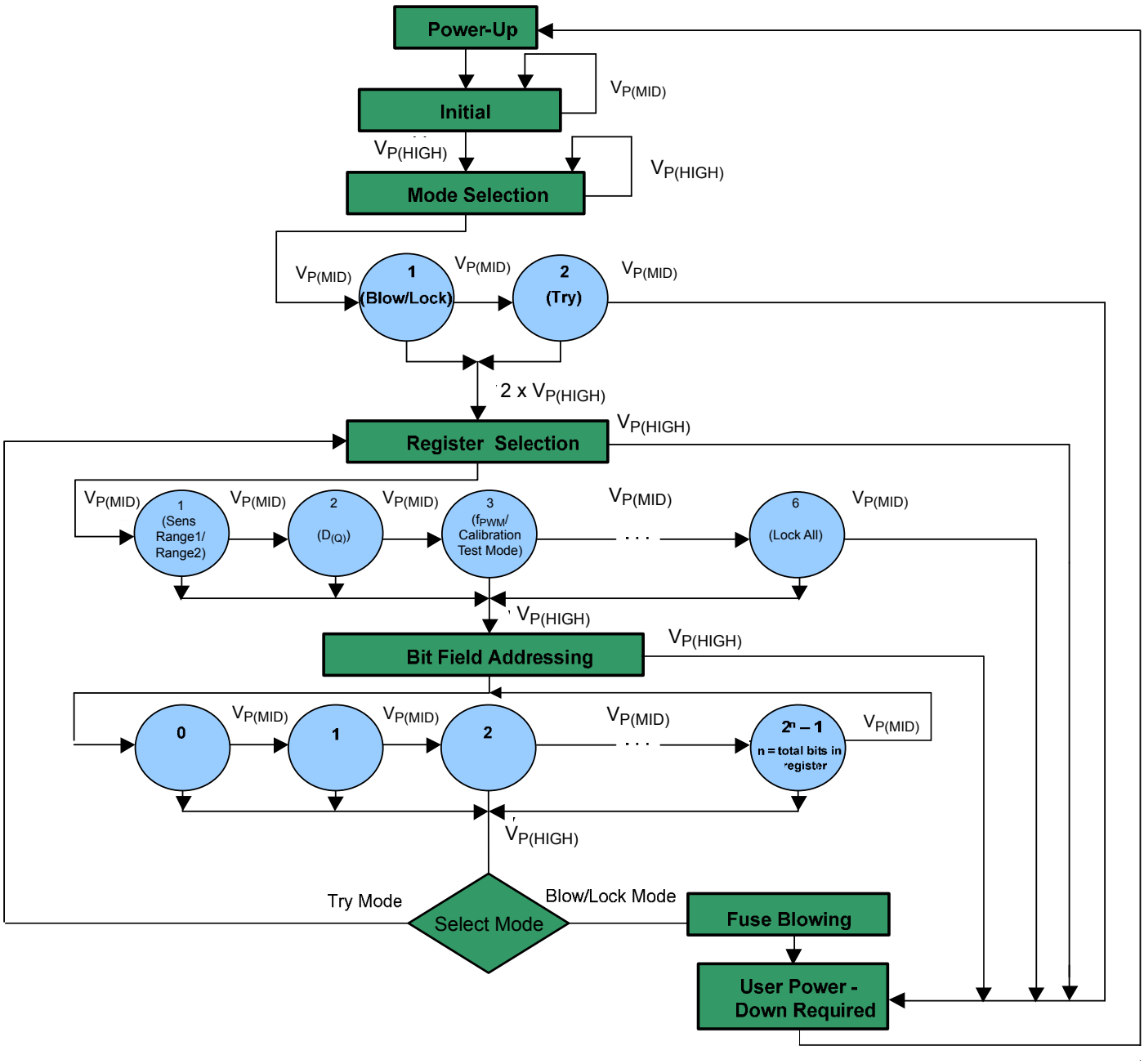


Figure 10. Example of Try mode programming pulses applied to the VCC pin. In this example, Sensitivity (parameter key 1) is addressed to code 3, and $D_{(Q)}$ (parameter key 2) is addressed to code 2. The values set in the Sensitivity and $D_{(Q)}$ registers will be held in the device until the supply is cycled. Permanent fuse blowing cannot be accomplished in Try mode.

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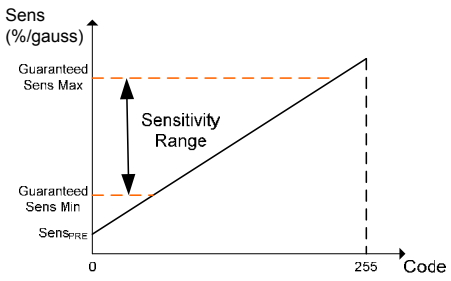
PROGRAMMING STATE MACHINE

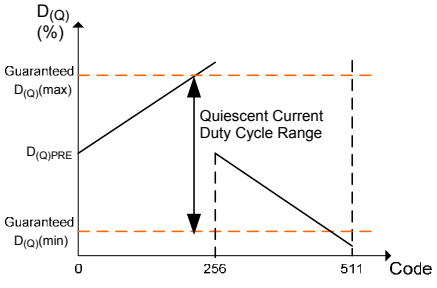


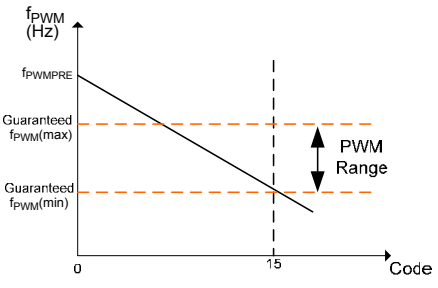
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PROGRAMMING LOGIC TABLE

Mode or Parameter Name (Register Key)	Bit Field Address		Description
	Binary Format [MSB → LSB]	Decimal Equivalent Code	
Programmable Mode			
Lock, Blow (1)	01	1	Entry to Lock or Blow mode
Try (2)	10	2	Entry to Try mode
Programmable Parameter			
Sens (Range1/Range2) (1)	0 0000 0000	0	Minimum Sens value in $Sens_{Range1}$, Sens = $Sens_{PRE}$
	0 1111 1111	255	Maximum Sens value in $Sens_{Range1}$
	1 0000 0000	256	Minimum Sens value in $Sens_{Range2}$
	1 1111 1111	511	Maximum Sens value in $Sens_{Range2}$
$D_{(Q)}$ (2)	0 0000 0000	0	Initial value, $D_{(Q)} = D_{(Q)PRE}$
	0 1111 1111	255	Maximum quiescent current duty cycle in range
	1 0000 0000	256	Switch from programming increasing $D_{(Q)}$ to programming decreasing $D_{(Q)}$
	1 1111 1111	511	Minimum quiescent current duty cycle in range
f_{PWM}/ Calibration Test Mode (3)	0 0000 0000	0	Initial value; $f_{PWM} = f_{PWMPRE}$
	0 0000 1111	15	Minimum PWM frequency in range
	0 0001 0000	16	Enable 50% Duty Cycle Calibration Test Mode
Lock All (6)	10 0000 0000	512	Enable blowing Lock fuse to lock device







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50% DUTY CYCLE CALIBRATION TEST MODE

The calibration mode is provided so that the user can compensate for differences in the ground potential between the A1357 and any interface circuitry used to measure the pulse width of the A1357 current. The test mode is optional and must be enabled by blowing programming bits. After the bit for the test mode has been blown, the device enters 50% Duty Cycle Calibration Test mode every time the device is powered-up. The bit enabling test mode is key 3, bit 4.

In customer applications, the PWM interface circuitry (shown as the system controller in figure 11) and the A1357 may be powered via different power and ground circuits. As a result, the ground reference for the A1357 may differ from the ground reference of the system controller. In some customer applications, this ground difference can be as large as ±0.5 V.

Differences in the ground reference for the A1357 and the system controller can result in variations in the threshold voltage used to measure the duty cycle of the A1357. If the PWM conversion threshold voltage varies, then the duty cycle will vary because there is a finite rise time, t_r, and fall time, t_f, in the PWM waveform. This problem is shown in figure 12.

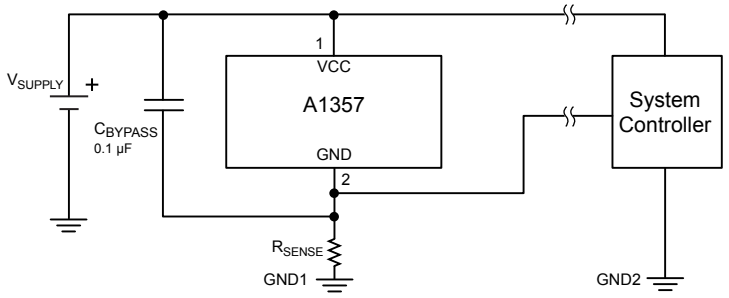


Figure 11. In many applications the A1357 may be powered using a different ground reference than the system controller. This may cause the ground reference for the A1357 (GND1) to differ from the ground reference of the system controller (GND2) by as much as to ± 0.5 V.

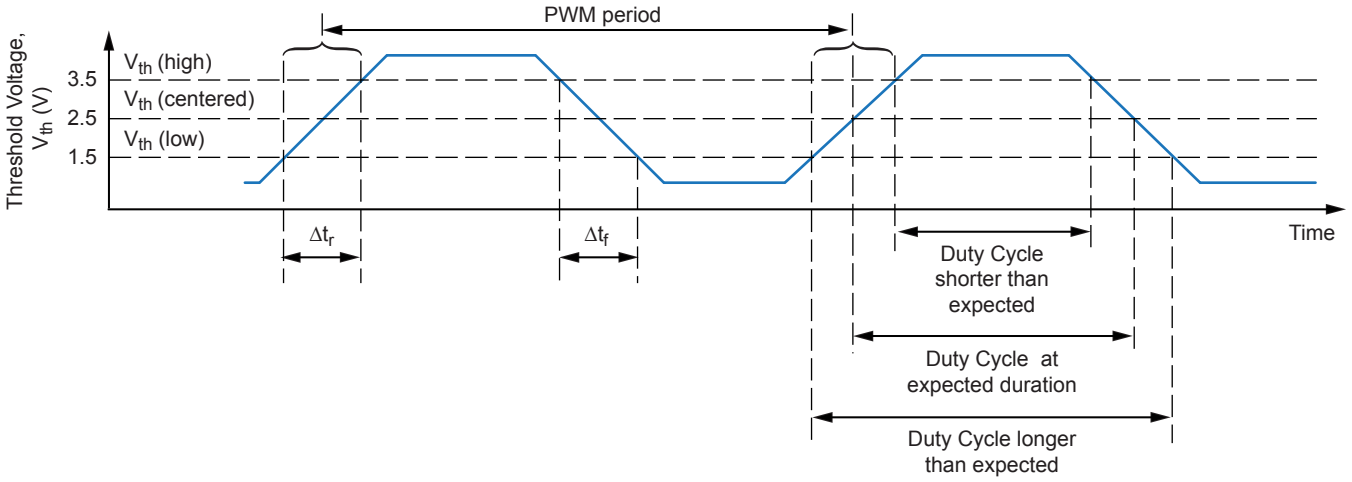


Figure 12. When the threshold voltage, V_{th}, is correctly centered between V_{th} (high) and V_{th} (low), the current duty cycle accurately coincides with the applied magnetic field. If the threshold voltage is raised, the current duty cycle appears shorter than expected. Conversely, if the threshold voltage is lowered, the current duty cycle is longer than expected.

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The 50% Duty Cycle Calibration Test mode allows end users to compensate for any threshold errors that result from a difference in system ground potentials. When calibration mode has been enabled, at power-up the device operates initially in calibration mode for t_{CAL}, 50 ms, during which the device current waveform has a fixed 50% duty cycle (the programmed quiescent duty cycle, $D_{(Q)}$, value) regardless of the applied external magnetic field (see figure 13). This allows the system controller to compare the measured quiescent duty cycle with an ideal 50% duty cycle. After t_{CAL} has elapsed, the duty cycle will correspond to an applied magnetic field as expected. The calibration test time (t_{CAL}) corresponds with a target PWM frequency of 1 kHz. If the PWM frequency is programmed away from its target of 1 kHz, the duration of the calibration test time will scale inversely with the change in PWM frequency.

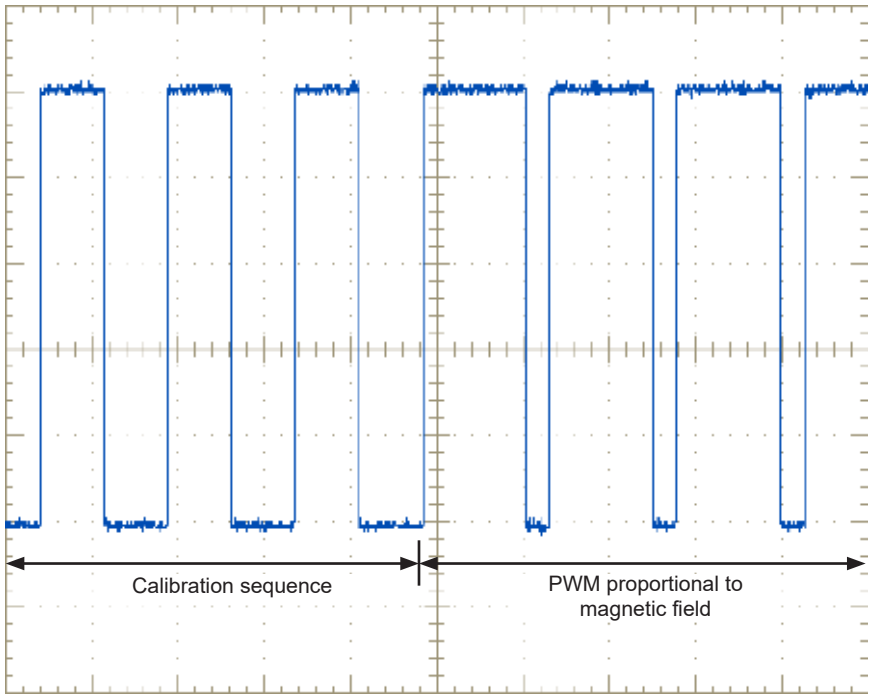
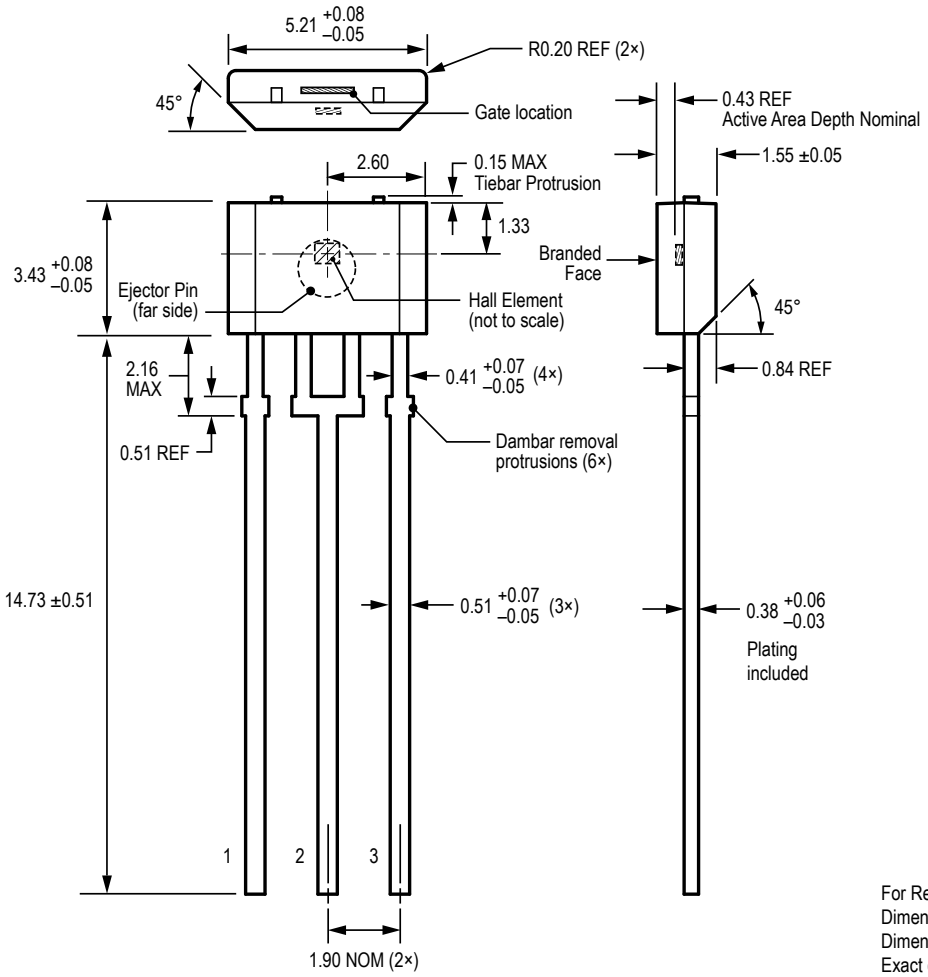
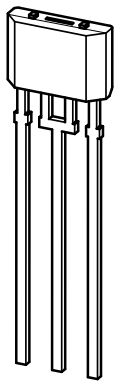


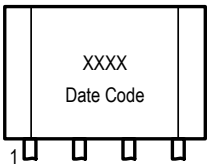
Figure 13. With calibration mode in effect, after powering-on the A1357 outputs a 50% duty cycle for the first 50 ms, t_{CAL}, regardless of the applied magnetic field. After t_{CAL} has elapsed, the output responds to a magnetic field as expected. The example in this figure assumes that a large +B field is applied to the device after t_{CAL} has elapsed.

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Package KB, 3-Pin SIP







Standard Branding Reference View

Lines 1, 2 = 4 characters.

Line 1: Part Number
Line 2: 4-digit Date Code

Branding scale and appearance at supplier discretion

For Reference Only; not for tooling use (reference Allegro DWG-0000225)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

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Revision History

Number	Date	Description
–	April 23, 2013	Initial release
1	February 19, 2019	Minor editorial updates
2	March 27, 2020	Minor editorial updates
3	March 18, 2022	Updated package drawing (page 19)
4	June 22, 2022	Updated product status to Not for New Design
5	September 28, 2023	Updated product status to Discontinued

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