SEMTECH INTERNATIONAL AG

EClamp2454P
ESD/EMI Protection for Color LCD Interfaces

PROTECTION PRODUCTS - EMIClamp™

Description

The EClamp™2454P is a (L-C) low pass filter array with integrated TVS diodes. It is designed to suppress unwanted EMI/RFI signals and provide electrostatic discharge (ESD) protection in portable electronic equipment. This state-of-the-art device utilizes solid-state silicon-avalanche technology for superior clamping performance and DC electrical characteristics. They have been optimized for **protection of color LCD and camera lines** in cellular phones and other portable electronics.

The device consists of four identical circuits comprised of TVS diodes for ESD protection, and a 5-pole inductor - capacitor network for EMI/RFI filtering. A typical inductor value of 28nH and a capacitor value of 12pF are used to achieve 40dB minimum attenuation at 800MHz. The TVS diodes provide effective suppression of ESD voltages in excess of ±15kV (air discharge) and ±8kV (contact discharge) per IEC 61000-4-2, level 4.

The EClamp2454P is in a 8-pin, RoHS/WEEE compliant, SLP2116P8 package. It measures 2.1 x 1.6 x 0.58mm. The leads are spaced at a pitch of 0.5mm and are finished with lead-free NiPd. The small package makes it ideal for use in portable electronics such as cell phones, digital still cameras, and PDAs.

Features

- Bidirectional EMI/RFI filter with integrated TVS for ESD protection
- ESD protection to **IEC 61000-4-2 (ESD) Level 4, ±15kV (air), ±8kV (contact)**
- Filter performance: 40dB minimum attenuation at 800MHz to 2.7GHz
- TVS working voltage: 5V
- Inductor: 28nH (Typical)
- Capacitors: 12pF (Typical at VR = 2.5V)
- Protection and filtering for four lines
- Solid-state technology

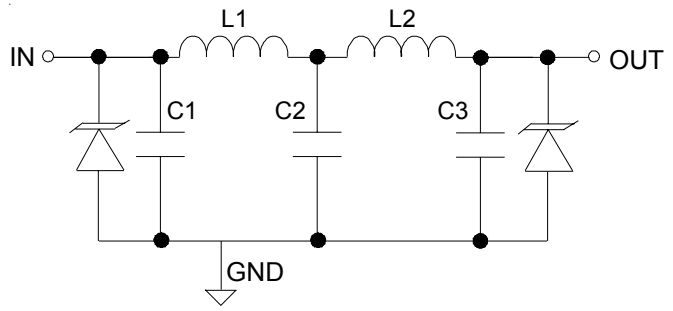
Mechanical Characteristics

- SLP2116P8 8-pin package
- RoHS/WEEE Compliant
- Nominal Dimensions: 2.1 x 1.6 x 0.58 mm
- Lead Pitch: 0.5mm
- Lead finish: NiPd
- Marking: Marking Code
- Packaging: Tape and Reel per EIA 481

Applications

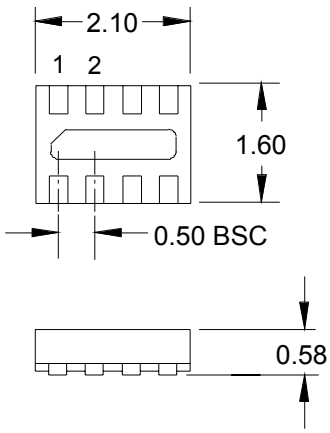
- Color LCD Protection
- Cell Phone CCD Camera Lines
- Clamshell Cell Phones

Circuit Diagram (Each Line)



Device Schematic (4X)

Package Configuration



8 Pin SLP package (Bottom Side View)
Nominal Dimensions in mm

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Maximum Ratings

Rating	Symbol	Value	Units
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	+/- 20 +/- 15	kV
Junction Temperature	T_J	125	°C
Operating Temperature	T_{op}	-40 to +85	°C
Storage Temperature	T_{STG}	-55 to +150	°C

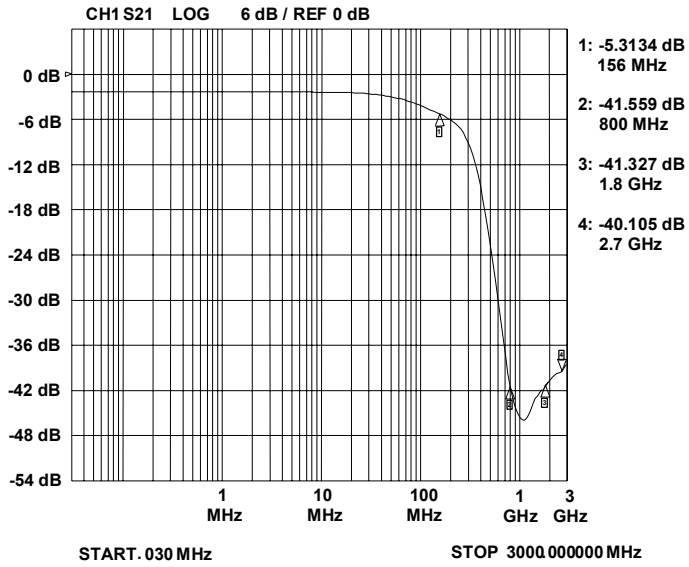
Electrical Characteristics (T=25°C)

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
TVS Reverse Stand-Off Voltage	V_{RWM}				5	V
TVS Reverse Breakdown Voltage	V_{BR}	I_t = 1mA	6	8	10	V
TVS Reverse Leakage Current	I_R	V_{RWM} = 3.3V			0.1	µA
DC Resistance	R_{DC}			33		Ohms
Filter Cut-Off Frequency	fc	Z_{Source} = Z_{Load} = 50 Ohms		155		MHz
Inductance	L			28		nH
Total Series Inductance	$L_1 + L_2$	Each Line		56		nH
Capacitance	C_1 , C_2 , C_3	V_R = 2.5V, f = 1MHz	10	12	15	pF
Total Capacitance	$C_1 + C_2 + C_3$	Input to Gnd, Each Line V_R = 2.5V, f = 1MHz	30	36	45	pF

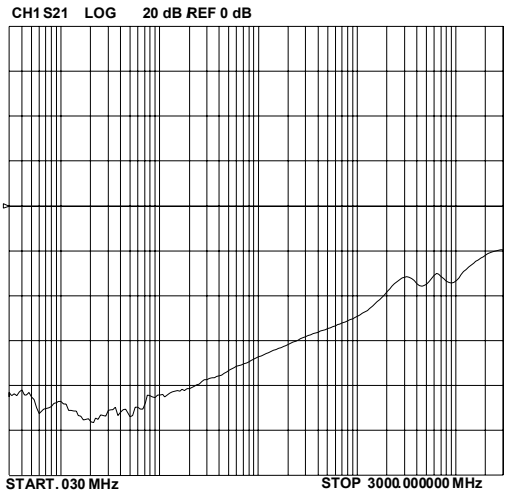
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Typical Characteristics

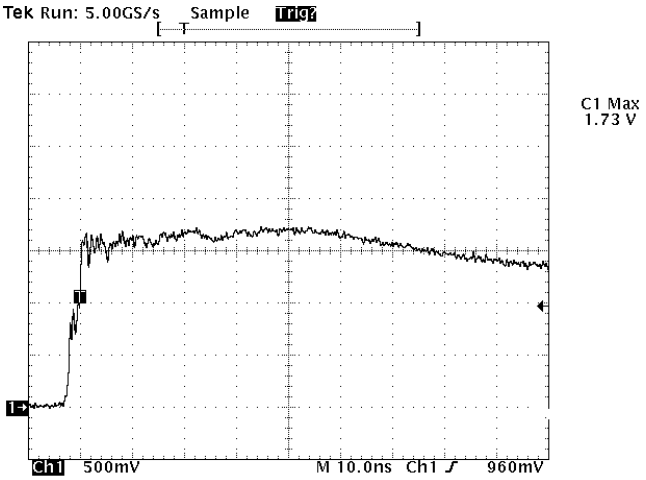
Typical Insertion Loss S21 (Each Line)



Analog Crosstalk (Each Line)

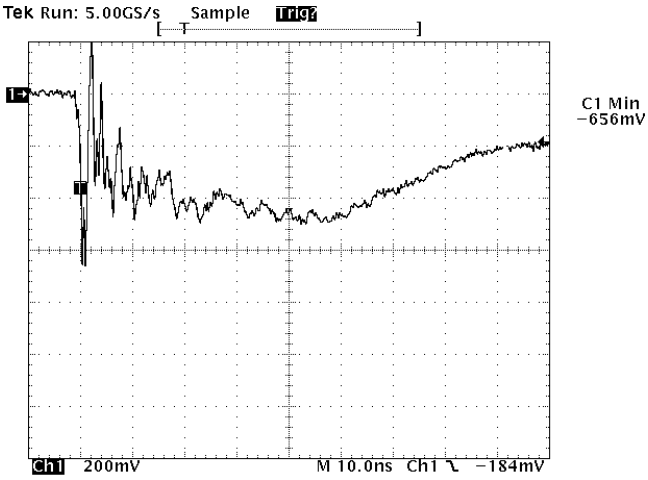


ESD Clamping (+8kV Contact)



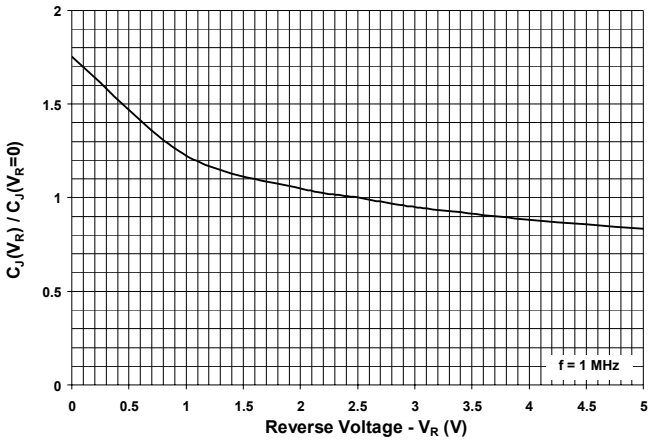
Note: Data is taken with a 10x attenuator

ESD Clamping (-8kV Contact)



Note: Data is taken with a 10x attenuator

Capacitance vs. Reverse Voltage (Normalized to 2.5 volts)



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Device Connection

The EClamp2454P is comprised of four identical circuits each consisting of a low pass filter for EMI/RFI suppression and dual TVS diodes for ESD protection. The device is in a 8-pin SLP package. Electrical connection is made to the 8 pins located at the bottom of the device. A center tab serves as the ground connection. The device has a flow through design for easy layout. Pin connections are noted in Figure 1. All path lengths should be kept as short as possible to minimize the effects of parasitic inductance in the board traces. Recommendations for the ground connection are given below.

Ground Connection Recommendation

Parasitic inductance present in the board layout will affect the filtering performance of the device. As frequency increases, the effect of the inductance becomes more dominant. This effect is given by Equation 1.

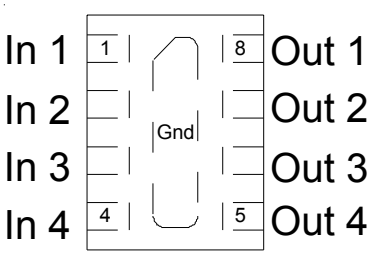
Equation 1: The Impedance of an Inductor at Frequency XLF

$$XLF(L,f) = 2*\pi*f*L$$

Where:
L= Inductance (H)
f = Frequency (Hz)

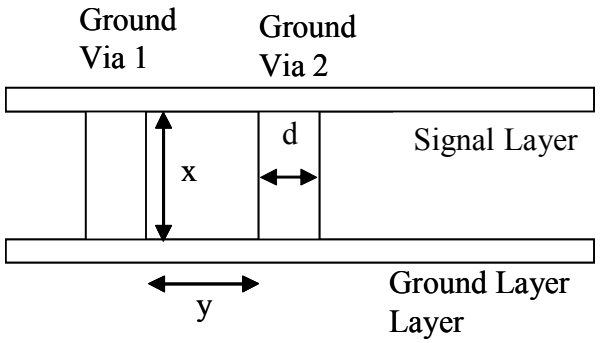
Via connections to the ground plane form rectangular wire loops or ground loop inductance as shown in Figure 2. Ground loop inductance can be reduced by using multiple vias to make the connection to the ground plane. Bringing the ground plane closer to the signal layer (preferably the next layer) also reduces ground loop inductance. Multiple vias in the device ground pad will result in a lower inductive ground loop over two exterior vias. Vias with a diameter d are separated by a distance y run between layers separated by a distance x. The inductance of the loop path is given by Equation 2. Thus, decreasing distance x and y will reduce the loop inductance and result in better high frequency filter characteristics.

Figure 1 - Pin Identification and Configuration (Top Side View)



Pin	Identification
1 - 4	Input Lines
5 - 8	Output Lines
Center Tab	Ground

Figure 2 - Inductance of Rectangular Wire Loops



Equation 2: Inductance of Rectangular Wire Loop

$$LRECT(d,x,y) = 10.16*10^{-9}*\left[x*\ln\left[\frac{2*y}{d}\right]+y*\ln\left[\frac{2*x}{d}\right]\right]$$

Where:
d = Diameter of the wire (in)
x = Length of wire loop (in)
y = Breath of wire loop (in)

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Applications Information

Figure 3 shows the recommended device layout. The ground pad vias have a diameter of 0.008 inches (0.20 mm) while the two external vias have a diameter of 0.010 inches (0.250mm). The internal vias are spaced approximately evenly from the center of the pad. The designer may choose to use more vias with a smaller diameter (such as 0.005 inches or 0.125mm) since changing the diameter of the via will result in little change in inductance (i.e. the log function in Equation 2 in highly insensitive to parameter d) . Figure 4 shows a typical insertion loss (S21) plot for the device using Semtech's filter evaluation board with 50 Ohm traces and the recommended via configuration.

Figure 3 - Recommended Layout Using Ground Vias

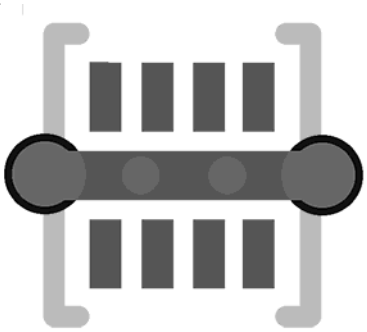
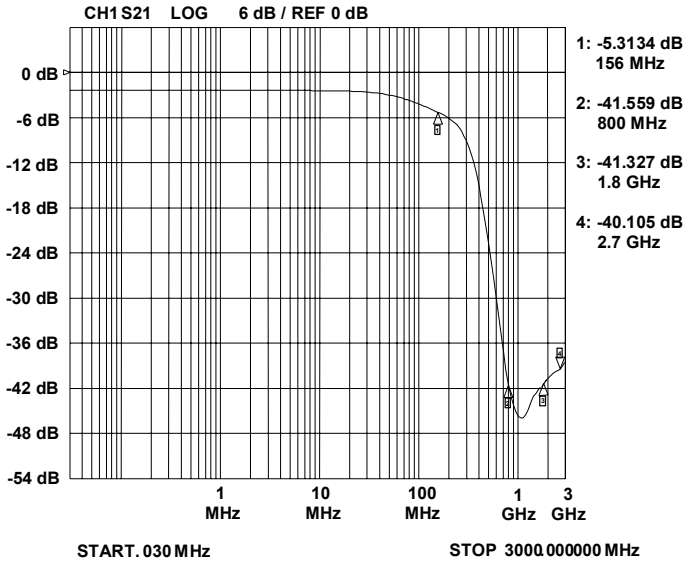


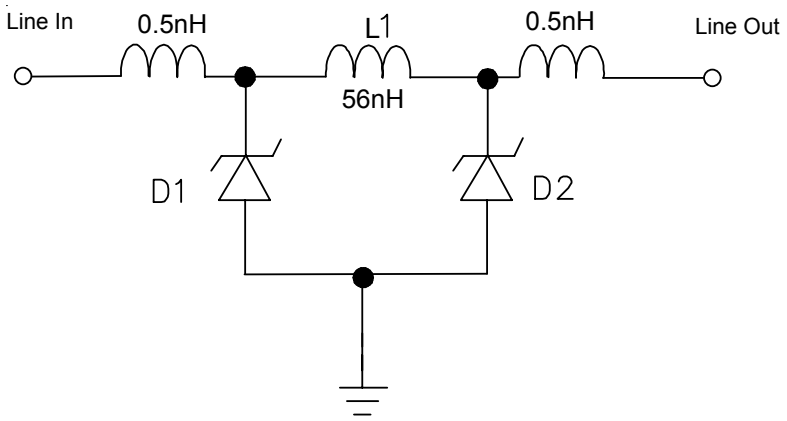
Figure 4 - Filter Characteristics Using Recommended Layout with Internal Vias



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Applications Information - Spice Model

EClamp2454P Spice Model & Parameters



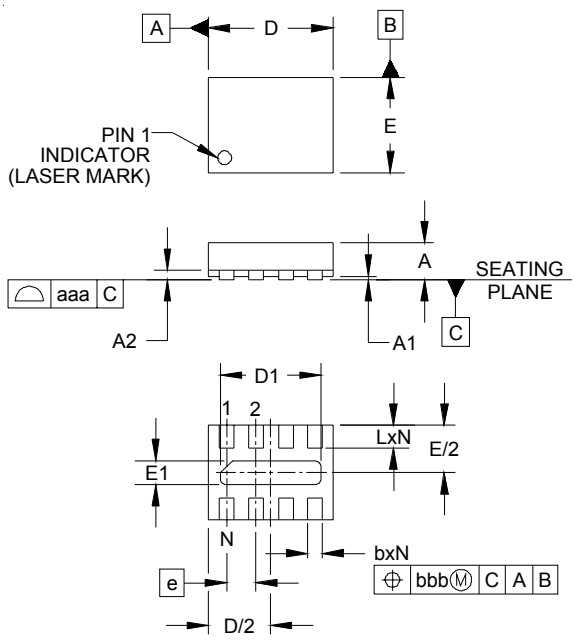
EClamp2454P Spice Model

Table 1 - EClamp2454P Spice Parameters

Parameter	Unit	D1 (TVS)	D2 (TVS)
IS	Amp	4.09E-15	4.09E-15
BV	Volt	7.44	7.44
VJ	Volt	0.744	0.744
RS	Ohm	0.584	0.584
IBV	Amp	1E-3	1E-3
CJO	Farad	31E-12	31E-12
TT	sec	2.541E-9	2.541E-9
M	--	0.23	0.23
N	--	1.1	1.1
EG	eV	1.11	1.11

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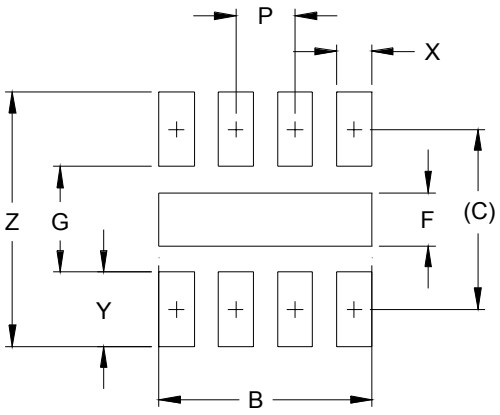
Outline Drawing - SLP2116P8



DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.020	.023	.026	0.50	0.58	0.65
A1	-	.001	.002	0.00	.003	0.05
A2		(.006)			(0.15)	
b	.007	.010	.012	0.20	0.25	0.30
D	.079	.083	.087	2.00	2.10	2.20
D1	.061	.067	.071	1.55	1.70	1.80
E	.059	.063	.067	1.50	1.60	1.70
E1	.010	.016	.020	0.25	0.40	0.50
e	.020 BSC			0.50 BSC		
L	.011	.013	.015	0.28	0.33	0.38
N	6			6		
aaa	.003			0.08		
bbb	.004			0.10		

NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

Land Pattern - SLP2116P8

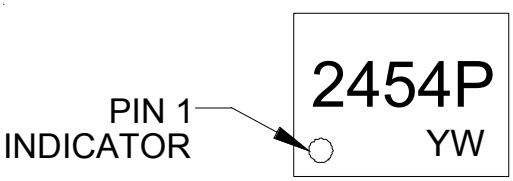


DIMENSIONS		
DIM	INCHES	MILLIMETERS
B	.071	1.80
C	.060	1.52
F	.018	0.45
G	.035	0.89
P	.020	0.50
X	.012	0.30
Y	.025	0.63
Z	.085	2.15

NOTES:
1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

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Marking



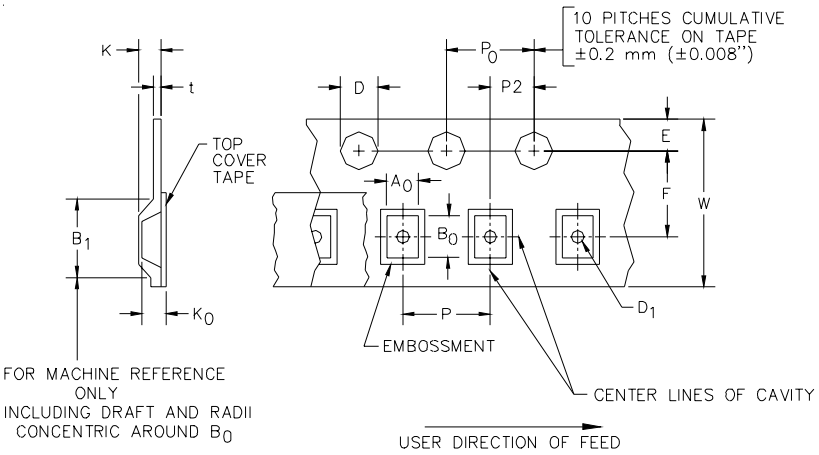
YW = Date Code (Y=Year, W=Week)

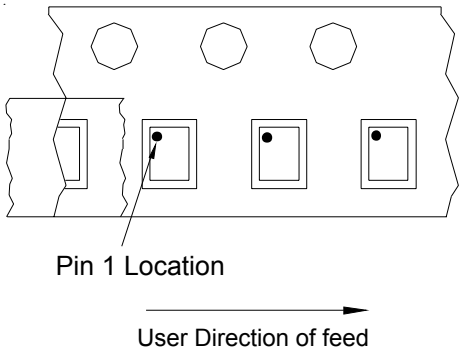
Ordering Information

Part Number	Qty per Reel	Reel Size
EClamp2454P.TCT	3000	7 Inch

This is a lead-free RoHS/WEEE Compliant Device
EMIClamp and EClamp are marks of Semtech Corporation

Tape and Reel Specification





A0	B0	K0
1.96 +/-0.05 mm	2.31 +/-0.05 mm	0.74 +/-0.05 mm

Device Orientation in Tape

Tape Width	B, (Max)	D	D1	E	F	K (MAX)	P	P0	P2	T(MAX)	W
8 mm	4.2 mm (.165)	1.5 + 0.1 mm - 0.0 mm (0.59 +.005 - .000)	0.8 mm ±0.05 (.031)	1.750±.10 mm (.069±.004)	3.5±0.05 mm (.138±.002)	2.4 mm (.094)	4.0±0.1 mm (.157±.00-4)	4.0±0.1 mm (.157±.00-4)	2.0±0.05m-m (.079±.002)	0.4 mm (.016)	8.0 mm + 0.3 mm - 0.1 mm (.312±.012)

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