SC4150
Negative Voltage Hot Swap Controller

Description

The SC4150 is a negative voltage hotswap controller that allows the insertion of line cards into a live backplane.

The inrush current is programmable and closed loop operation limits the maximum current even under short circuit conditions. A built in timing circuit prevents false shutdown. The signal from the drain voltage is fed to the timer, providing safety for the MOSFET when in linear mode. The SC4150 latches off under abnormal condition and attempts to restart after a time out period.

The device comes in two options, PWRGD (SC4150H) and $\overline{\text{PWRGD}}$ (SC4150L). These signals can be directly used to enable power modules.

Features

- Programmable slew of the inrush current when used for hot insertion in the negative 24V and 48V backplane
- Closed loop operation limits the maximum current even in short circuit condition
- Built in timer prevents false shutdown, when the closed loop operation limits the current.
- Sensing the drain voltage allows for immediate shutdown in short circuit condition, where current spikes and noise is ignored.
- Power good signal
- Input UVLO and OVLO sensing
- SO-8 package

Applications

- Central office switching
- -48V Distributed power systems
- Power supply hotswap & inrush control

Typical Application Circuit

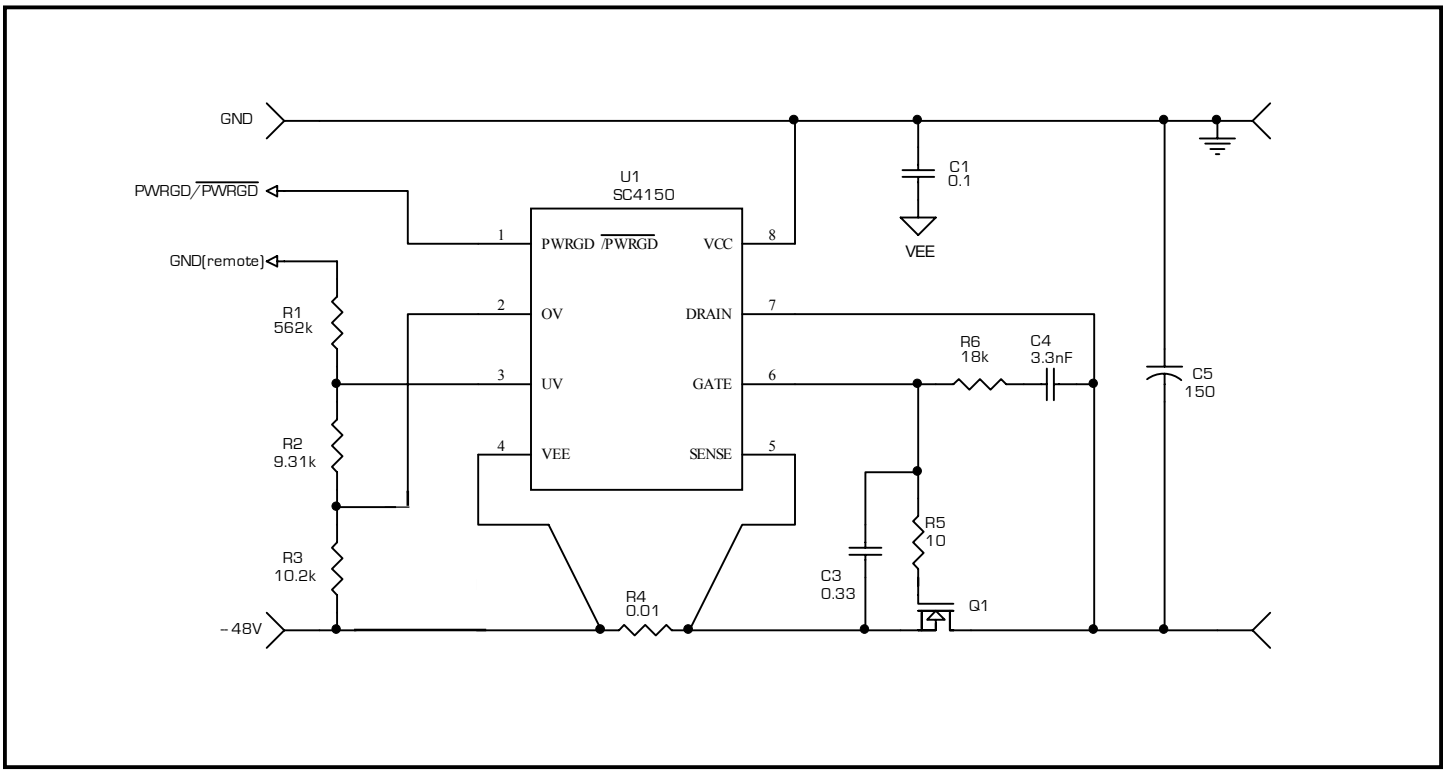


Figure 1

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Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Maximum	Units
Supply Voltage	V_{CC}	-0.3 to 100	V
DRAIN, $\overline{PWRGD}$/ PWRGD		-0.3 to 100	V
SENSE, GATE		-0.3 to 20	V
UV, OV		-0.3 to 60	V
Thermal Resistance Junction to Ambient	θ_{JA}	163	°C
Thermal Resistance Junction to Case	θ_{JC}	38.8	°C
Operating Junction Temperature Range	T_J	-40 to 125	°C
Storage Temperature Range	T_{STG}	-65 to 150	°C
Lead Temperature (Soldering) 10 sec	T_{LEAD}	300	°C

Electrical Characteristics

Unless specified: T_A = 25°C, V_{CC} = 48V, V_{EE} = 0V.
Values in **bold** apply over full operating temperature range.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
DC Characteristics						
Supply Operating Range	V_{CC}		**10**		**80**	V
Supply Current	I_{CC}	UV = 3V, 0V = V_{EE}, SENSE = V_{EE}		**4**	**7**	mA
Circuit Breaker Trip Voltage	V_{CB}	V_{CB} = (V_{SENSE} - V_{EE})	**50**	**60**	**70**	mV
Gate Pin Pull-up Current	I_{PU}	Gate drive ON, V_{GATE} = V_{EE}		-50		µA
Gate Pin Pull-down Current	I_{PD}	Any fault condition		40		mA
Sense Pin Current	I_{SENSE}	V_{SENSE} = 50mV		-0.05		µA
External Gate Drive	ΔV_{GATE}	(V_{GATE} -V_{EE}), 20V < V_{DD} ≤ 80V	**9**	**13**	**16**	V
		(V_{GATE} -V_{EE}), 10V ≤ V_{DD} ≤ 20V		**8**		
UV Pin High Threshold Voltage	V_{UVH}	UV Low to High transition	**1.241**	**1.273**	**1.305**	V
UV Pin Low Threshold Voltage	V_{UVL}	UV High to Low transition	**1.192**	**1.223**	**1.253**	V
UV Pin Hystersis	V_{UVHY}			**50**		mV
UV Pin Input Current	I_{INUV}	V_{UV} = V_{EE}		-0.1		µA
OV Pin High Threshold Voltage	V_{OVH}	OV Low to High transition	**1.192**	**1.223**	**1.253**	V
OV Pin Low Threshold Voltage	V_{OVL}	OV High to Low transition	**1.153**	**1.188**	**1.223**	V
OV Pin Hystersis	V_{OVHY}			35		mV
OV Pin Input Current	I_{INOV}	V_{OV} ≥ 1.5V		-0.05		µA

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Electrical Characteristics (Cont.)

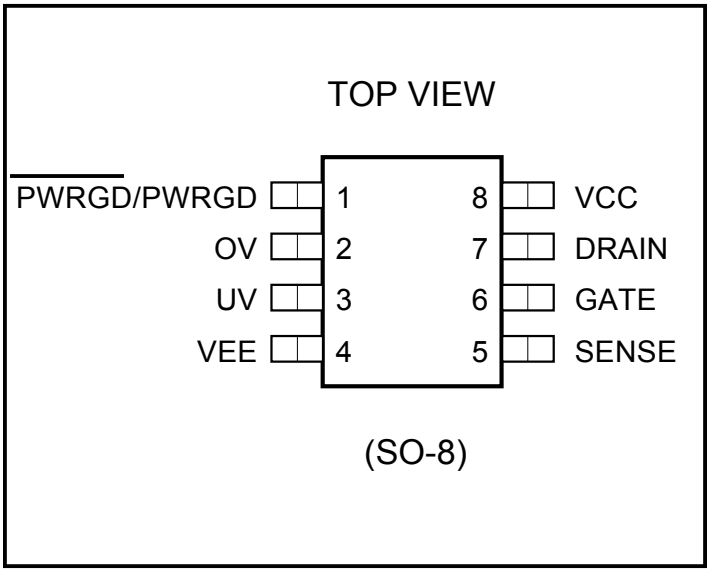
Unless specified: T_A = 25°C, V_{CC} = 48V, V_{EE} = 0V.
Values in **bold** apply over full operating temperature range.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Power Good Threshold	V_{PG}	V_{DRAIN} - V_{EE}, High to Low transition	1.5	1.75	2.0	V
Power Good Threshold Hysteresis	V_{PGHY}			0.4		V
Drain Input Bias Current	I_{DRAIN}	V_{DRAIN} = 48V		**15**	**50**	µA
Output Low Voltage	V_{OL}	SC4150H, V_{OL} = PWRGD - V_{DRAIN} @ V_{DRAIN} = 5V, I_O = 1mA		1		V
		SC4150L, V_{OL} = PWRGD - V_{EE} @ V_{DRAIN} = 1V, I_O = 1mA		1		V
Output Leakage	I_{OH}	SC4150H, V_{DRAIN} -V_{EE} = 1V, V_{PWRGD} = 80V		**1.0**	**10**	µA
		SC4150L, V_{DRAIN} -V_{EE} = 5V		**1.0**	**10**	µA
AC Characteristics						
OV High to Gate Low	t_{PHLOV}			1.7		µs
UV Low to Gate Low	t_{PHLUV}			1.5		µs
OV Low to Gate High	t_{PLHOV}			5.5		µs
UV Low to Gate High	t_{PLHUV}			6.5		µs
SENSE High to Gate Low	$t_{PHLSENSE}$			3		µs
DRAIN Low to $\overline{\text{PWRGD}}$ Low DRAIN Low to (PWRGD - DRAIN) High	t_{PHLPG}			0.5		µs
DRAIN High to $\overline{\text{PWRGD}}$ High DRAIN High to (PWRGD - DRAIN) Low	t_{PLHPG}			0.5		µs
Gate ON Time - Time Delay	t_{ON_1}	V_{DRAIN} > 8V, after short circuit		5		µs
Gate ON Time - Time Delay	t_{ON_2}	V_{DRAIN} < 7V, after short circuit		250		µs
Gate OFF Time	t_{OFF}	SC4150, After short, prior to retry		100		ms
		SC4150-4, After short, prior to retry		400		

Note:
(1) This device is ESD sensitive. Use of standard ESD handling precaution is required.

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Pin Configuration



Ordering Information

Part Number(1)(2)(3)	Package
SC4150HISTRT	SO-8
SC4150LISTRT	
SC4150HIS-4TRT	
SC4150LIS-4TRT	

Notes:

(1) Only available in tape and reel packaging. A reel contains 2500 devices.

(2) Device marking:
SC4150H, SC4150L - 100ms
4150H-4, 4150L-4 - 400ms

(3) Lead free product.

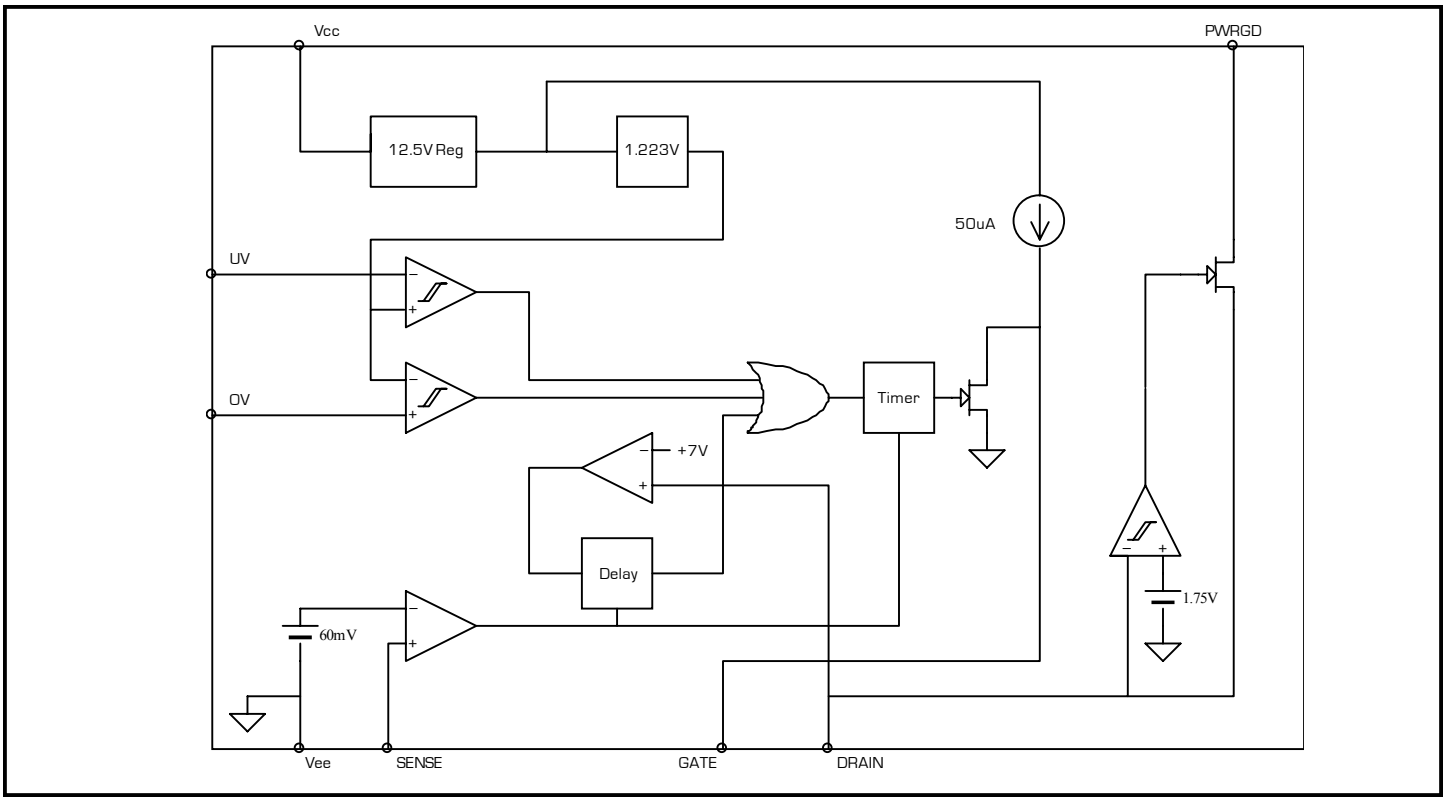
Pin Descriptions

Pin	Pin Name	Pin Function
1	$\overline{\text{PWRGD}}$/PWRGD	Power Good output pin. This pin will toggle when V_{DRAIN} is within V_{PG} of V_{EE}. This pin can be connected directly to the enable pin of a power module, 0.1µF to VEE is optional.
2	OV	Analog Overvoltage input. When OV is pulled above 1.223V threshold, an overvoltage condition is detected and the GATE pin will be immediately pulled low. The GATE pin will remain low until OV drops below the 1.188V high to low threshold.
3	UV	Analog Undervoltage input. When UV is pulled below the 1.223V threshold, an undervoltage condition is detected and the GATE pin will be immediately pulled low. The GATE pin will remain low until UV rises above the 1.273 threshold.
4	VEE	Negative supply voltage input. Connect to the lower potential of the power supply.
5	SENSE	Circuit breaker sense pin. With a sense resistor placed in the supply path between V_{EE} and SENSE, the circuit breaker will trip when the voltage across the resistor exceeds 60mV. Noise spikes of less than 2µs are filtered out and will not trip the circuit breaker. If the circuit breaker trip current is set to twice the normal operating current, only 25mV is dropped across the sense resistor during normal operation. To disable the circuit breaker, V_{EE} and SENSE can be shorted together.
6	GATE	Gate drive output for external n-channel. The GATE pin will go high when the following start-up conditions are met: the UV pin is high, t he OV pin is low and (V_{SENSE} - V_{EE}) < 60mV. The GATE pin is pulled high by a 50µA current source and pulled low with a 40mA current source.
7	DRAIN	Analog Drain sense input. Connect this pin to the drain of the external N-channel FET and the V(-) pin of the power module. When the DRAIN pin is below V_{PG}, the $\overline{\text{PWRGD}}$ or PWRGD pin will toggle.
8	VCC	Positive supply voltage input. Connect this pin to the higher potential of the power supply input and the V(+) pin of the power module.

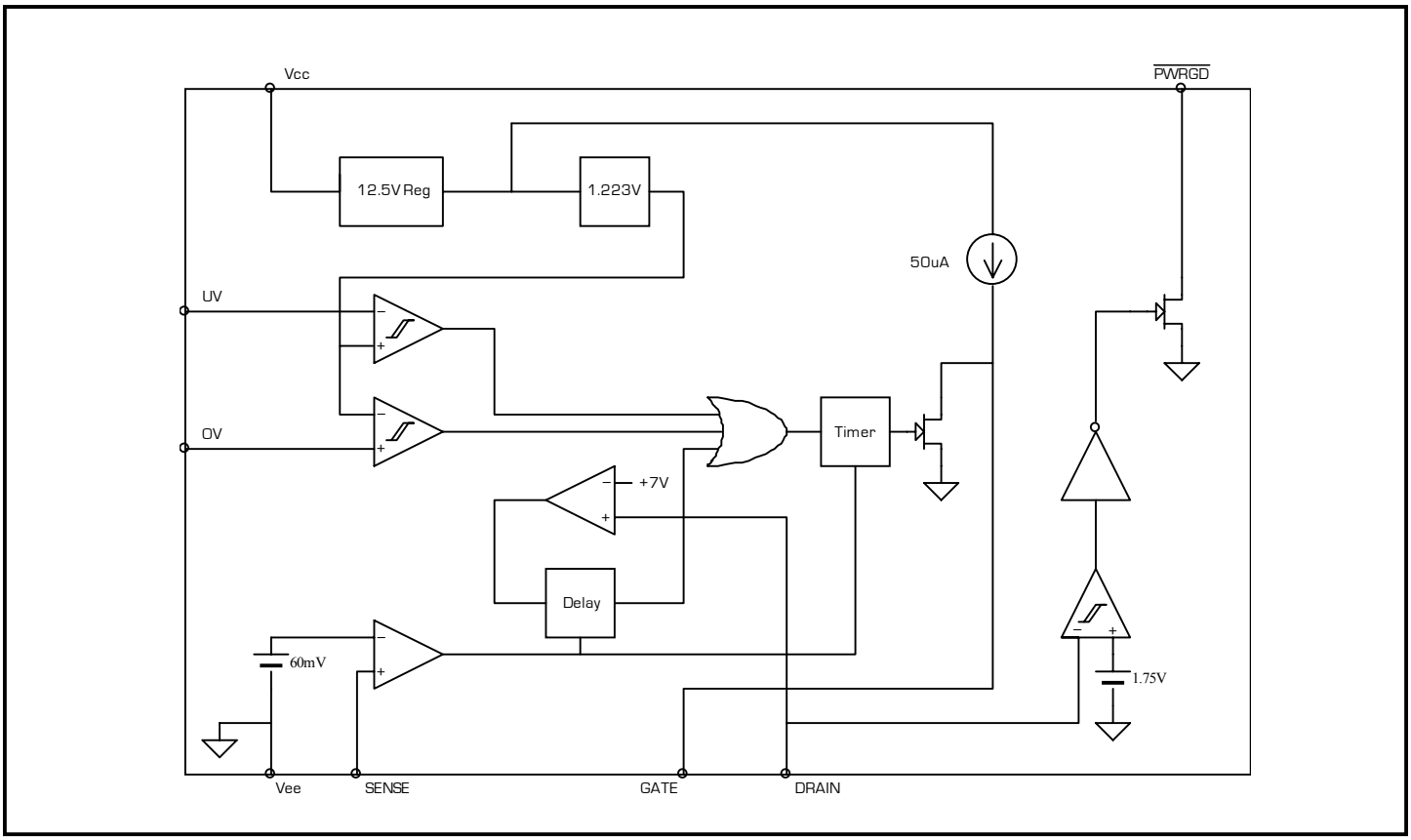
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Block Diagram

Active High PWRGD



Active Low $\overline{\text{PWRGD}}$



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Applications Information

Insertion of a power circuit board into a live backplane would draw enormous inrush currents. This is mostly due to the charging of the bulk electrolytic capacitors at the input of the power module being plugged in.

The transient currents would send glitches all over the power system and could cause corruption of the signals and even a power down if the source isn't able to handle these high surges.

This section describes the components selection needed for a typical application utilizing the SC4150. Let's assume the following requirements for a representative system:

Input voltage range: 36V to 72V

Nominal current: 2A typ.

Over-current condition: 5A

Bulk capacitance: Cload = 150µF

The schematic in Figure 2 combines internal function blocks along with the external components of the application circuit.

Resistors R1, R2 and R3 make up a voltage divider to set the Under-Voltage (UV) and Over-Voltage (OV) trip points.

When the input power supply ramps up the UV trips at 1.273V and OV trips at 1.223V; during the ramp down transition the UV trips at 1.223V and OV trips at 1.198V.

The 50mV hysteresis for UV and 25mV hysteresis for OV provide the necessary guard-bands to prevent false tripping during power up and power down conditions.

As an additional noise killing and stabilizing measure, the **capacitor C1** should be placed at the OV terminal with the value in range from 1,000 to 10,000pF.

For the UV=38V and OV=70V the values of the resistor can be calculated as follows:

$$Vuv = 1.273V \cdot (R1+R2+R3) \div (R2+R3)$$

$$Vov = 1.223V \cdot (R1+R2+R3) \div R3$$

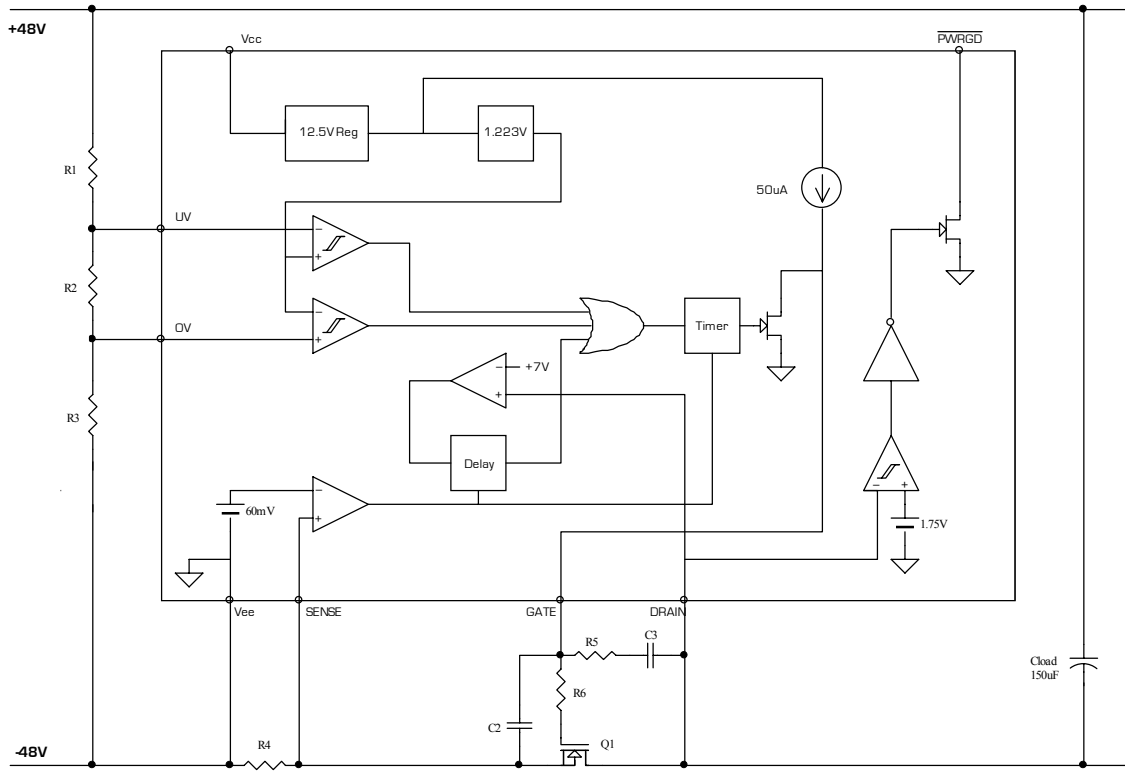


Figure 2

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Applications Information (Cont.)

With the input bias current of the UV and OV comparators in the range of 20-30nA, let's choose the R1 to be 562kΩ. This yields the values of R2=9.31kΩ and R3 = 10.2kΩ. With these values the accuracy is about 1% which is quite acceptable for those functions.
Resistor R4 sets the over-current trip. To choose R4, the user must determine the level of the current where it should trip. As a rule of thumb, the over-current is set to be 200-300% of the nominal value. In our case, we assumed this value to be 5A.

Considering the minimum trip voltage is 50mV the value of R4 is 50mV ÷ 5A = 10 mΩ.

The tolerance of this resistor is usually price driven and 5% is an adequate range of accuracy.

The actual position and layout of the circuitry around the sense resistor R4 is critical to avoid a false over-current tripping. The trace routing between R4 and SC4150 should be as short as possible and wide enough to handle the maximum current with zero current in the sense lines – ideally "Kelvin" like.
Additionally, there is a short delay circuit at the comparator to filter out unwanted noise and otherwise induced transients.

Inrush Current is being controlled by the **R5C3** network and swamping capacitor **C2**.

When a board is plugged into a live backplane, the input bulk capacitance of the board's power supply produces large current transients due to the rush of the currents charging those capacitors. The main feature of the SC4150 is to provide an orderly and well-controlled inrush current.

Since the minimum trip voltage is 50mV, let's choose the inrush current to be 3A.

$Imax = Cload \cdot \Delta Vmax / dt$

$dt = Cload \cdot \Delta Vmax / Imax = 150\mu F \cdot 70V / 3A = 3.5ms$

This would be the minimum time for the gate voltage plateau during which the Vdd linearly decreases maintaining 3A charge current of the Cload.

The inrush can be calculated using the following equation:
$I_{MAX} = (50\mu A \bullet C_{LOAD}) / C3$

With the values shown in the schematic the actual inruch current will be about 2A, which is within the limits we have chosen.

Resistor **R5** will produce a time constant which prevents Q1 from turning on when power is initially applied and the circuit is not ready to actively pull the gate low. It's value is not critical and 18k ensures the adequate delay.

The value of **C2** is chosen to prevent false turn-on of the FET due to the current flowing via C3 into the gate of the FET when the circuit initially connects to the power source. Capacitors C2 and C3 form a divider from Vin to GND. C2 must keep the initial voltage at the gate below Vth minimum.

For the typical FET, this threshold is around 1V to 2V, therefore C2 = 100 • C3 will keep gate voltage at 0.7V, even at the "worst" case of Vin = 70V.
The choice of the **Q1** is quite straightforward and is guided mostly by thermal considerations due to the power dissipation in the steady state.

For instance, in our case, the nominal current is 2A, the power dissipation due to the conducting losses will be

$Pdis = Inom^2 \bullet Rds_on.$

The MOSFET should be able to withstand Vdss ≥ 100V with continuous drain current Id ≥ 6A. Device SUD06N10 or similar fits this application. It has an Rds_on = 0.2Ω, and will dissipate

$Pdis = 2^2 \bullet 0.2 = 0.8W$, which can be handled by this DPAK device.

If there is a consideration of reducing the temperature of the MOSFET then the lower Rds_on device should be chosen or a different style (D2PAK) which has lower Junction-to-Ambient thermal characteristics.

The **R6** has a function of dumping high frequency oscillations. The value of it is not critical and can be in the range of 5Ω to 20Ω.

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Typical Characteristics

Below are the snap-shots taken at start-up with different loading conditions and during the application of the over-current at the output of the circuit.

For all figures, Ch1: V_{DRAIN}; Ch2: V_{GATE}; Ch3: PWRGD; Ch4: V_{R4} (Input current)

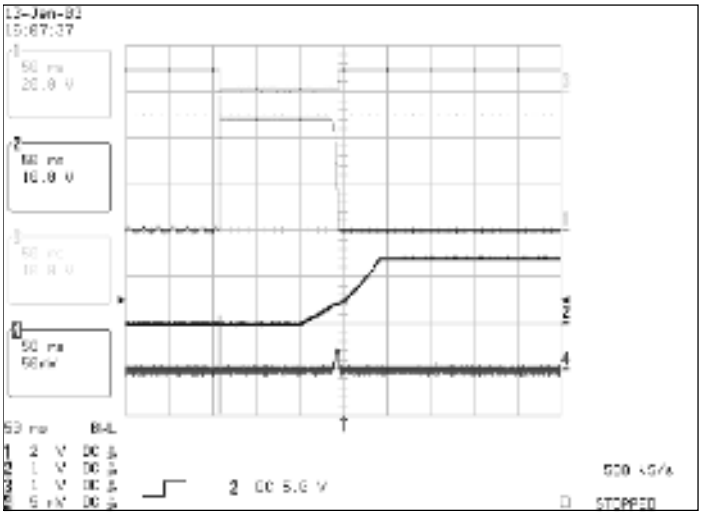


Figure 3. Start-up with no load.

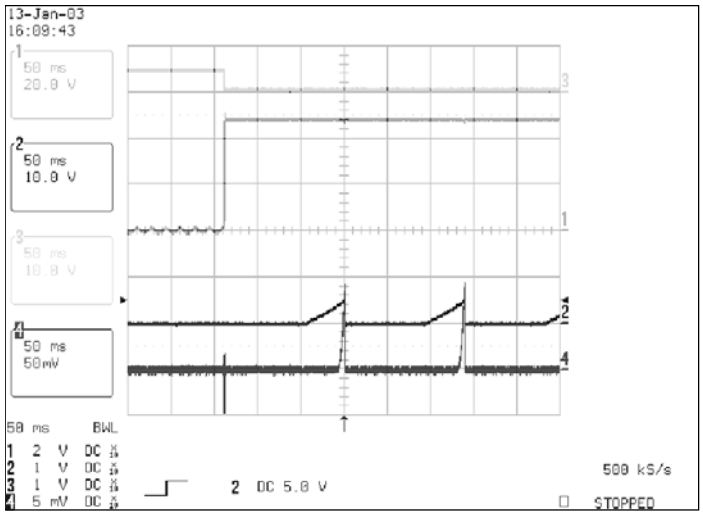


Figure 4. Start-up in over load.

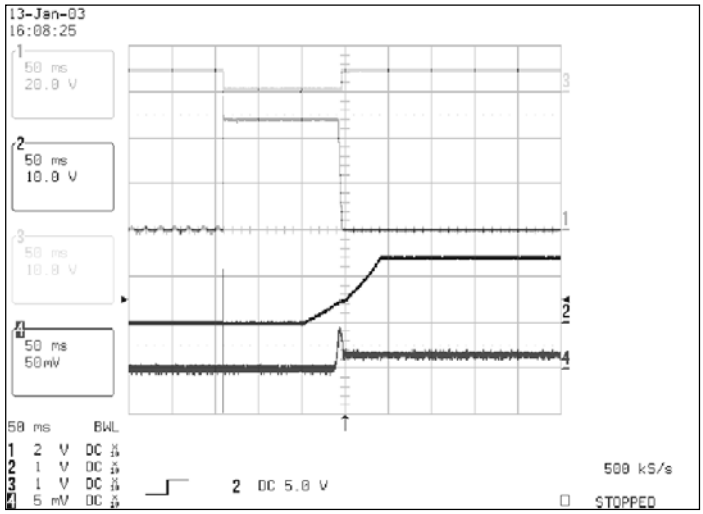


Figure 5. Start-up with 1Amp load.

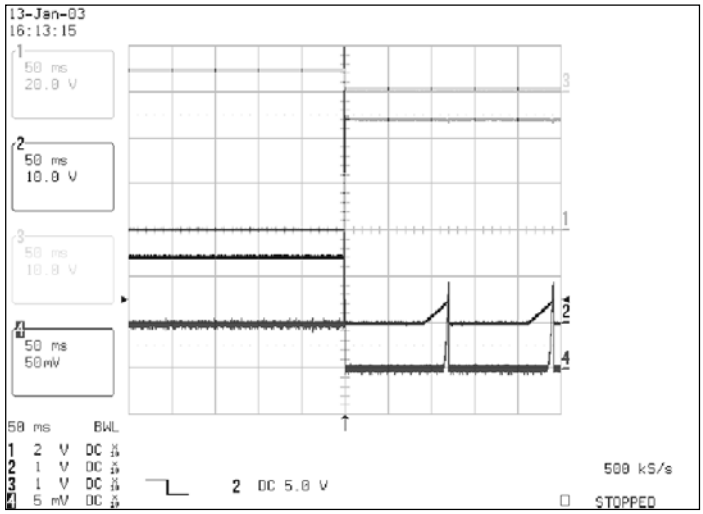


Figure 6. From 3A load into “short circuit”.

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Typical Characteristics (Cont.)

The following set of snapshots demonstrates effectiveness of SC4250 circuit in the case where connection to the live back plane is very “bouncy”, which is usually the situation with manual replacements of the power cards.

For all figures, Ch1: V_{DRAIN}; Ch2: V_{GATE}; Ch3: PWRGD (referenced to V_{DRAIN}); Ch4: V_{R4} (Input current)

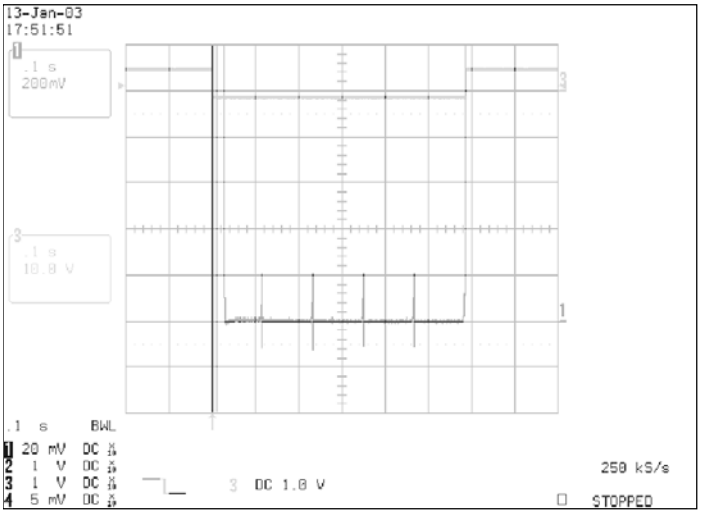


Figure 7. Short circuit hiccup.

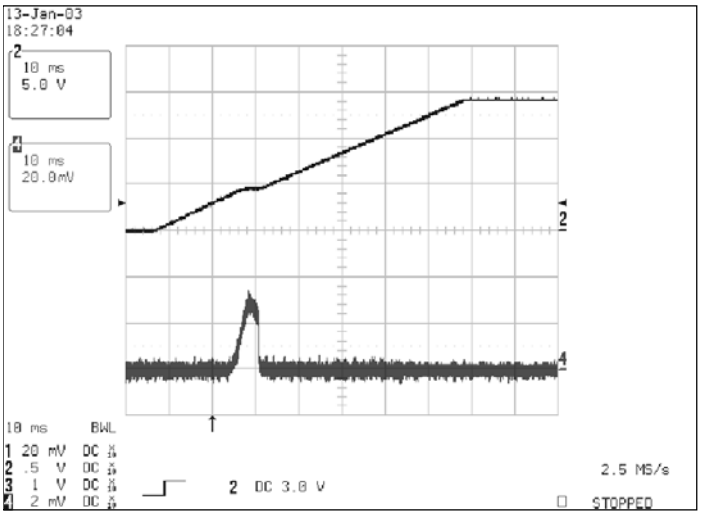


Figure 8. Inrush limit.

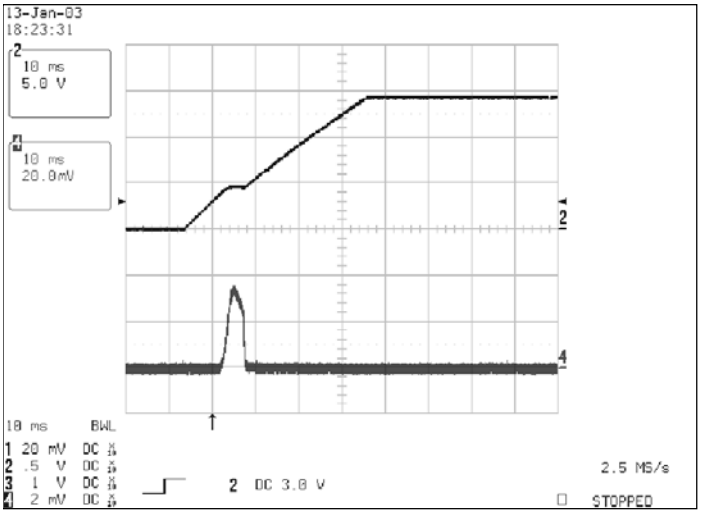


Figure 9. Inrush limit.

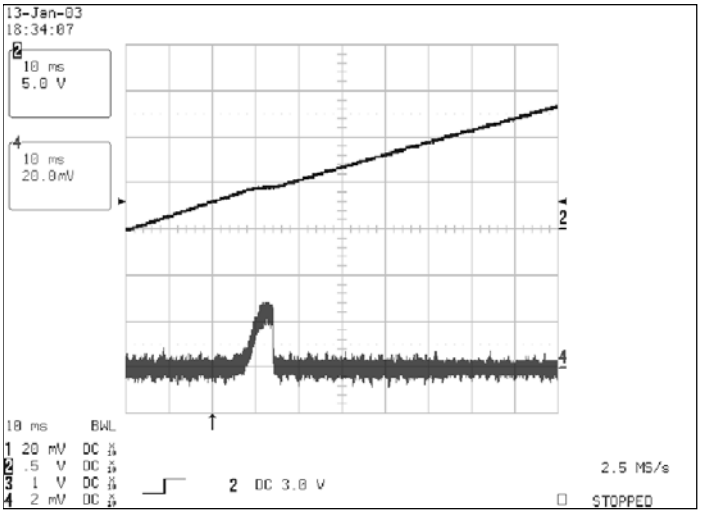
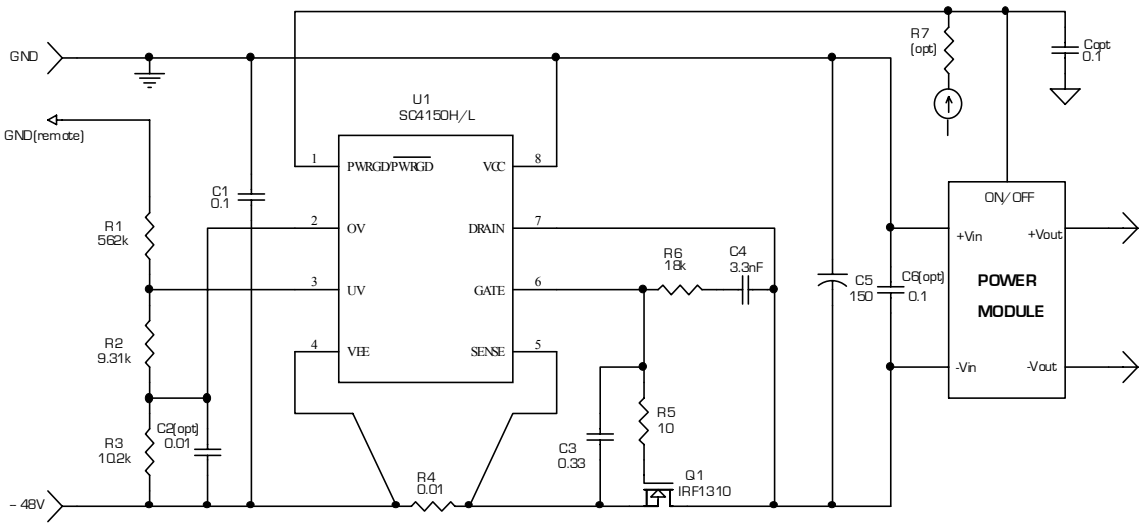


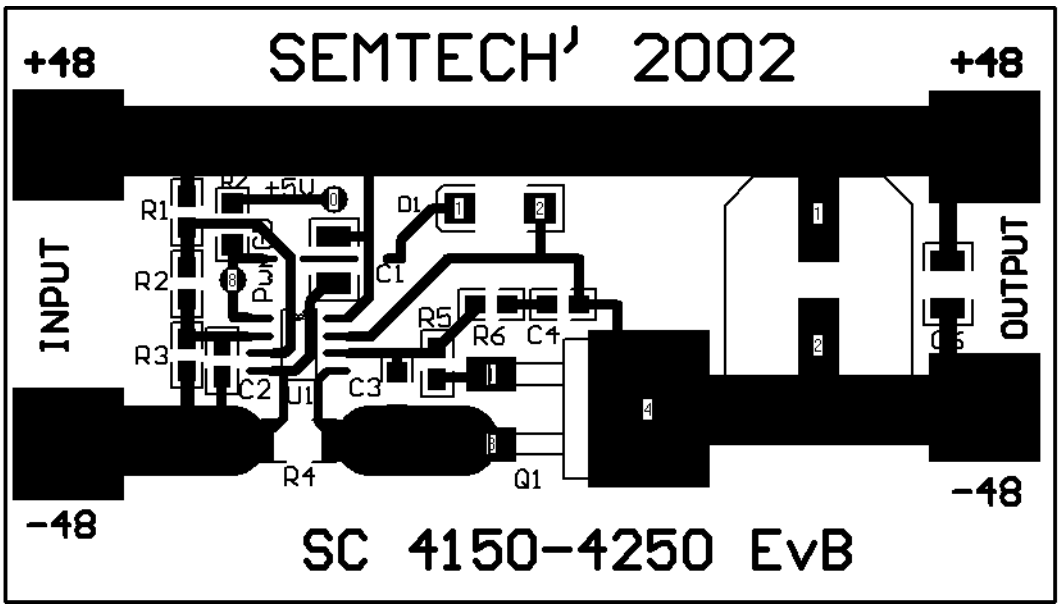
Figure 10. Inrush limit.

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Evaluation Board Schematic



Evaluation Board



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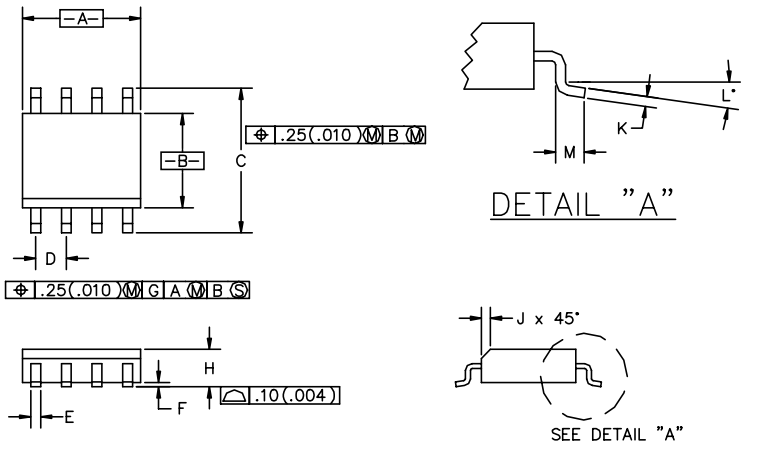
Evaluation Board - Bill of Materials

Ref	Qty	Designator	Value	Description	Footprint
1	1	C1	0.1/100V	Ceramic cap	1210
2	1	C2 (opt.)	0.01	Ceramic cap	0805
3	1	C3	0.33	Ceramic cap	1206S
4	1	C4	0.0033/100V	Ceramic cap	0805
5	1	C5	150/80V	Aluminum cap	CAP-AL-H
6	1	C6 (opt.)	0.1/100V	Ceramic cap	1210
7	1	Q1	IRF1310	MOSFET	D2PAK
8	1	R1	562k	Resistor	0805
9	1	R2	9.31k	Resistor	0805
10	1	R3	10.2k	Resistor	0805
11	1	R4	0.01	Resistor	2010CS
12	1	R5	10	Resistor	0805
13	1	R6	18k	Resistor	0805
14	1	R7	5.1k	Resistor	1206S
15	1	U1	SC4150	Semtech IC	SO-8

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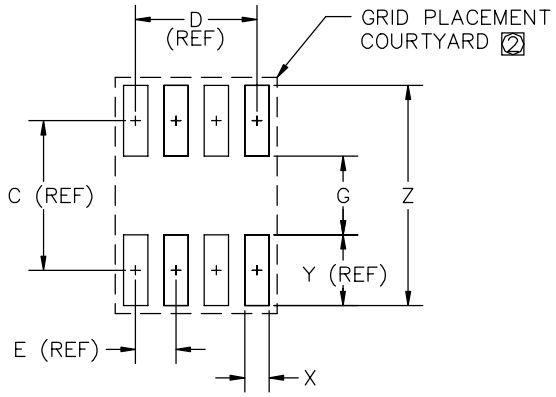
Outline Drawing - SO-8

JEDEC REF: MS-012AA



DIMENSIONS					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.188	.197	4.80	5.00	
B	.149	.158	3.80	4.00	
C	.228	.244	5.80	6.20	
D	.050 BSC		1.27 BSC		
E	.013	.020	0.33	0.51	
F	.004	.010	0.10	0.25	
H	.053	.069	1.35	1.75	
J	.011	.019	0.28	0.48	
K	.007	.010	.19	.25	
L	0°	8°	0°	8°	
M	.016	.050	0.40	1.27	

Minimum Land Pattern - SO-8



DIMENSIONS (1)					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
C	–	.19	–	5.00	–
D	–	.15	–	3.81	–
E	–	.05	–	1.27	–
G	.10	.11	2.60	2.80	–
X	.02	.03	.60	.80	–
Y	–	.09	–	2.40	–
Z	–	.29	7.20	7.40	–

(2) GRID PLACEMENT COURTYARD IS 12x16 ELEMENTS (6 mm X 8mm) IN ACCORDANCE WITH THE INTERNATIONAL GRID DETAILED IN IEC PUBLICATION 97.

(1) CONTROLLING DIMENSION: MILLIMETERS

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