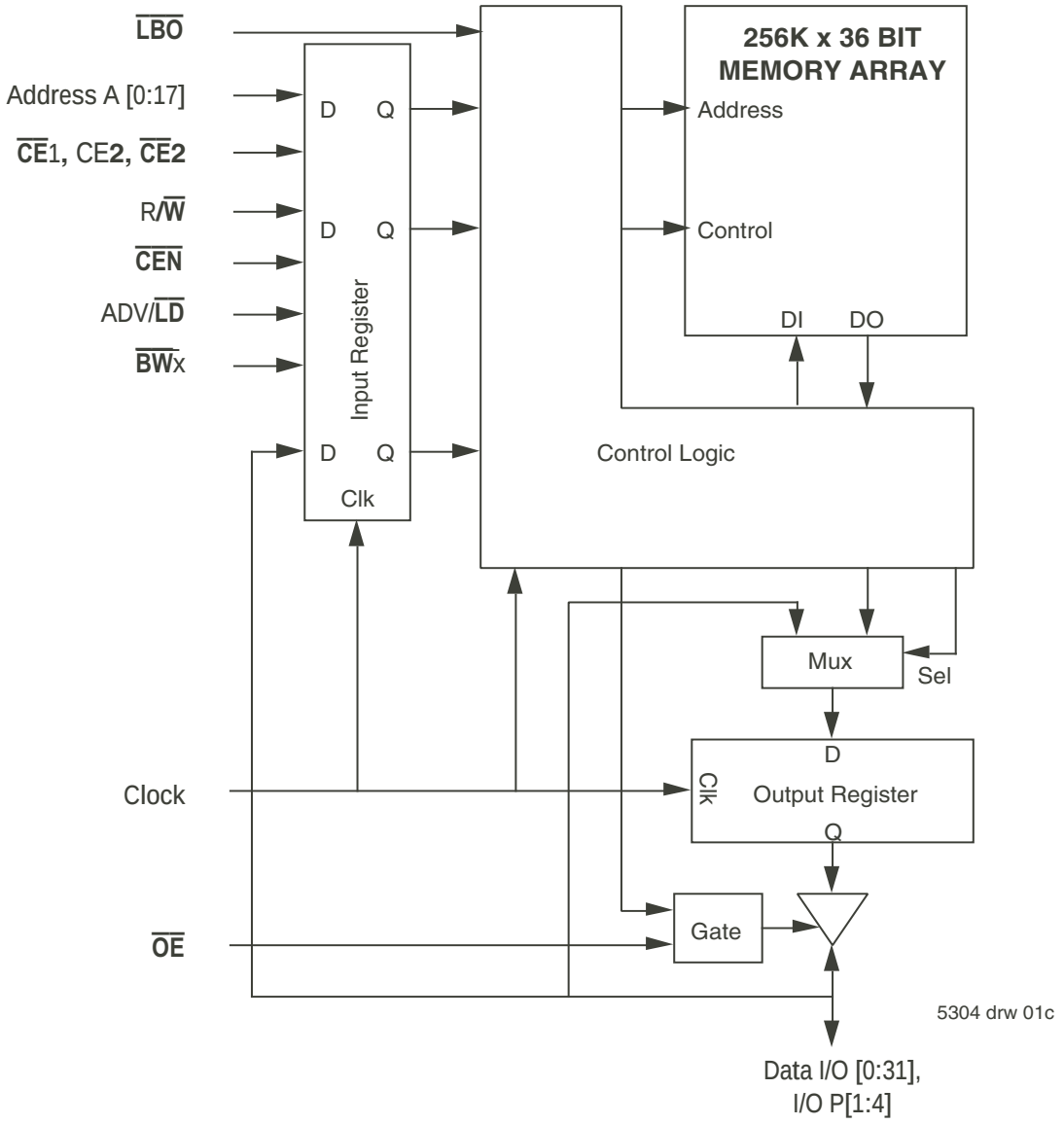
256K x 36, 512K x 18
3.3V Synchronous ZBT™ SRAMs
ZBT™ Feature
3.3V I/O, Burst Counter
Pipelined Outputs

71V65603
71V65803

Features

- 256K x 36, 512K x 18 memory configurations
- Supports high performance system speed - 150MHz (3.8ns Clock-to-Data Access)
- ZBT™ Feature - No dead cycles between write and read cycles
- Internally synchronized output buffer enable eliminates the need to control $\overline{OE}$
- Single R/$\overline{W}$ (READ/WRITE) control pin
- Positive clock-edge triggered address, data, and control signal registers for fully pipelined applications
- 4-word burst capability (interleaved or linear)
- Individual byte write ($\overline{BW}_1$ - $\overline{BW}_4$) control (May tie active)
- Three chip enables for simple depth expansion
- 3.3V power supply (±5%)
- 3.3V I/O Supply (V_{DDQ})
- Power down controlled by ZZ input
- Packaged in a JEDEC standard 100-pin plastic thin quad flatpack (TQFP), 119 ball grid array (BGA) and 165 fine pitch ball grid array(fBGA)
- Industrial temperature range (–40°C to +85°C) is available for selected speeds
- Green parts available, see ordering information

Functional Block Diagram — 256K x 36



ZBT and Zero Bus Turnaround are trademarks of Renesas Electronics Corporation and the architecture is supported by Micron Technology and Motorola, Inc.

Description

The IDT71V65603/5803 are 3.3V high-speed 9,437,184-bit (9 Megabit) synchronous SRAMS. They are designed to eliminate dead bus cycles when turning the bus around between reads and writes, or writes and reads. Thus, they have been given the name ZBT™, or Zero Bus Turn-around.

Address and control signals are applied to the SRAM during one clock cycle, and two cycles later the associated data cycle occurs, be it read or write.

The IDT71V65603/5803 contain data I/O, address and control signal registers. Output enable is the only asynchronous signal and can be used to disable the outputs at any given time.

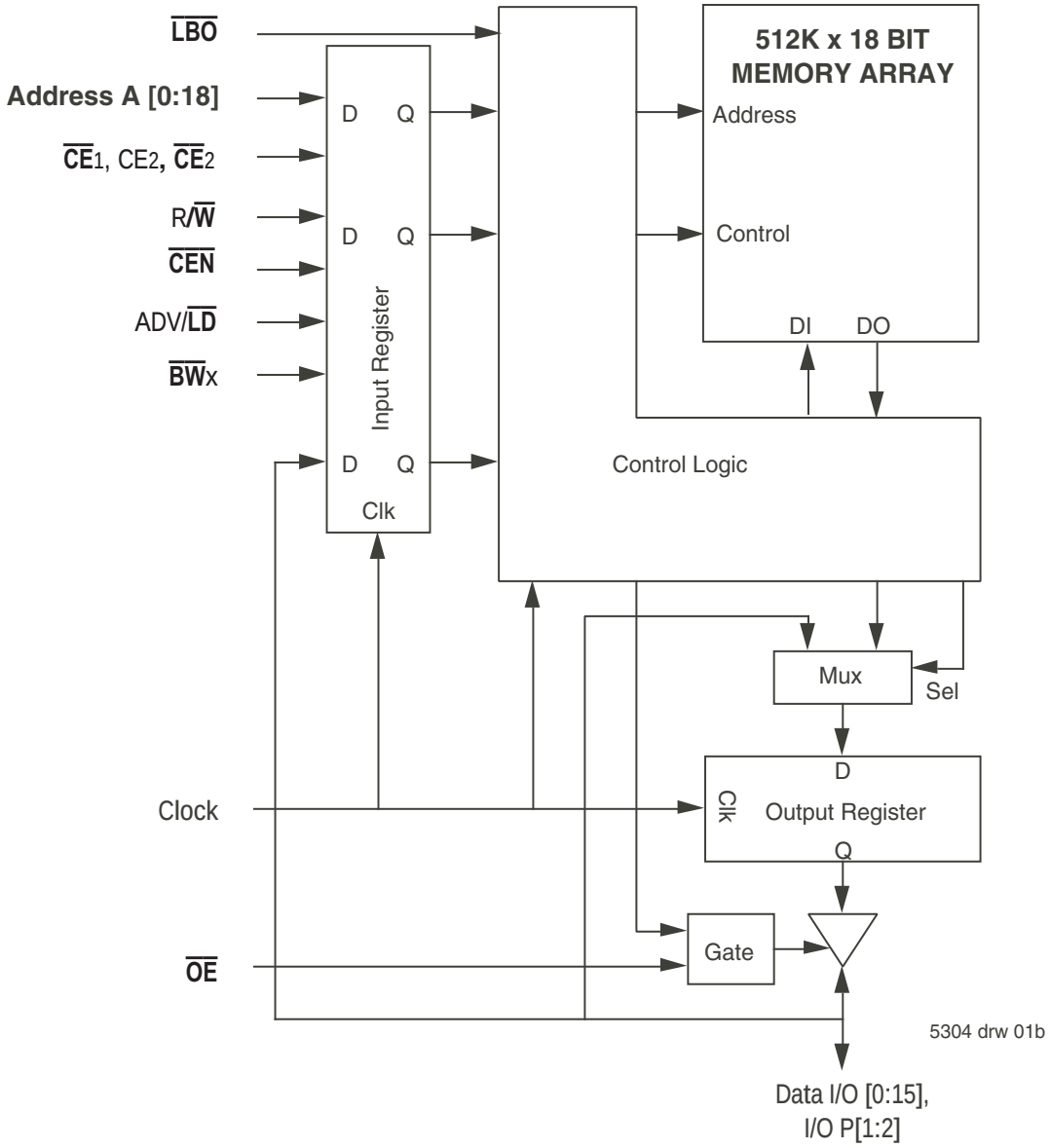
A Clock Enable ($\overline{CEN}$) pin allows operation of the IDT71V65603/5803 to be suspended as long as necessary. All synchronous inputs are ignored when ($\overline{CEN}$) is high and the internal device registers will hold their previous values.

There are three chip enable pins ($\overline{CE}1$, CE2, $\overline{CE}2$) that allow the user to deselect the device when desired. If any one of these three are not asserted when ADV/$\overline{LD}$ is low, no new memory operation can be initiated. However, any pending data transfers (reads or writes) will be completed. The data bus will tri-state two cycles after chip is deselected or a write is initiated.

The IDT71V65603/5803 have an on-chip burst counter. In the burst mode, the IDT71V65603/5803 can provide four cycles of data for a single address presented to the SRAM. The order of the burst sequence is defined by the $\overline{LBO}$ input pin. The $\overline{LBO}$ pin selects between linear and interleaved burst sequence. The ADV/$\overline{LD}$ signal is used to load a new external address (ADV/$\overline{LD}$ = LOW) or increment the internal burst counter (ADV/$\overline{LD}$ = HIGH).

The IDT71V65603/5803 SRAMs utilize a high-performance CMOS process, and are packaged in a JEDEC Standard 14mm x 20mm 100-pin thin plastic quad flatpack (TQFP) as well as a 119 ball grid array (BGA) and 165 fine pitch ball grid array (fBGA) .

Functional Block Diagram — 512K x 18



Pin Description Summary

A_0-A_{18}	Address Inputs	Input	Synchronous
$\overline{CE}_1$, CE_2, $\overline{CE}_2$	Chip Enables	Input	Synchronous
$\overline{OE}$	Output Enable	Input	Asynchronous
R/$\overline{W}$	Read/Write Signal	Input	Synchronous
$\overline{CEN}$	Clock Enable	Input	Synchronous
$\overline{BW}_1$, $\overline{BW}_2$, $\overline{BW}_3$, $\overline{BW}_4$	Individual Byte Write Selects	Input	Synchronous
CLK	Clock	Input	N/A
ADV/$\overline{LD}$	Advance burst address / Load new address	Input	Synchronous
$\overline{LBO}$	Linear / Interleaved Burst Order	Input	Static
ZZ	Sleep Mode	Input	Asynchronous
I/O_0-I/O_{31}, I/O_{P1}-I/O_{P4}	Data Input / Output	I/O	Synchronous
V_{DD}, V_{DDQ}	Core Power, I/O Power	Supply	Static
V_{SS}	Ground	Supply	Static

5304 tbl 01

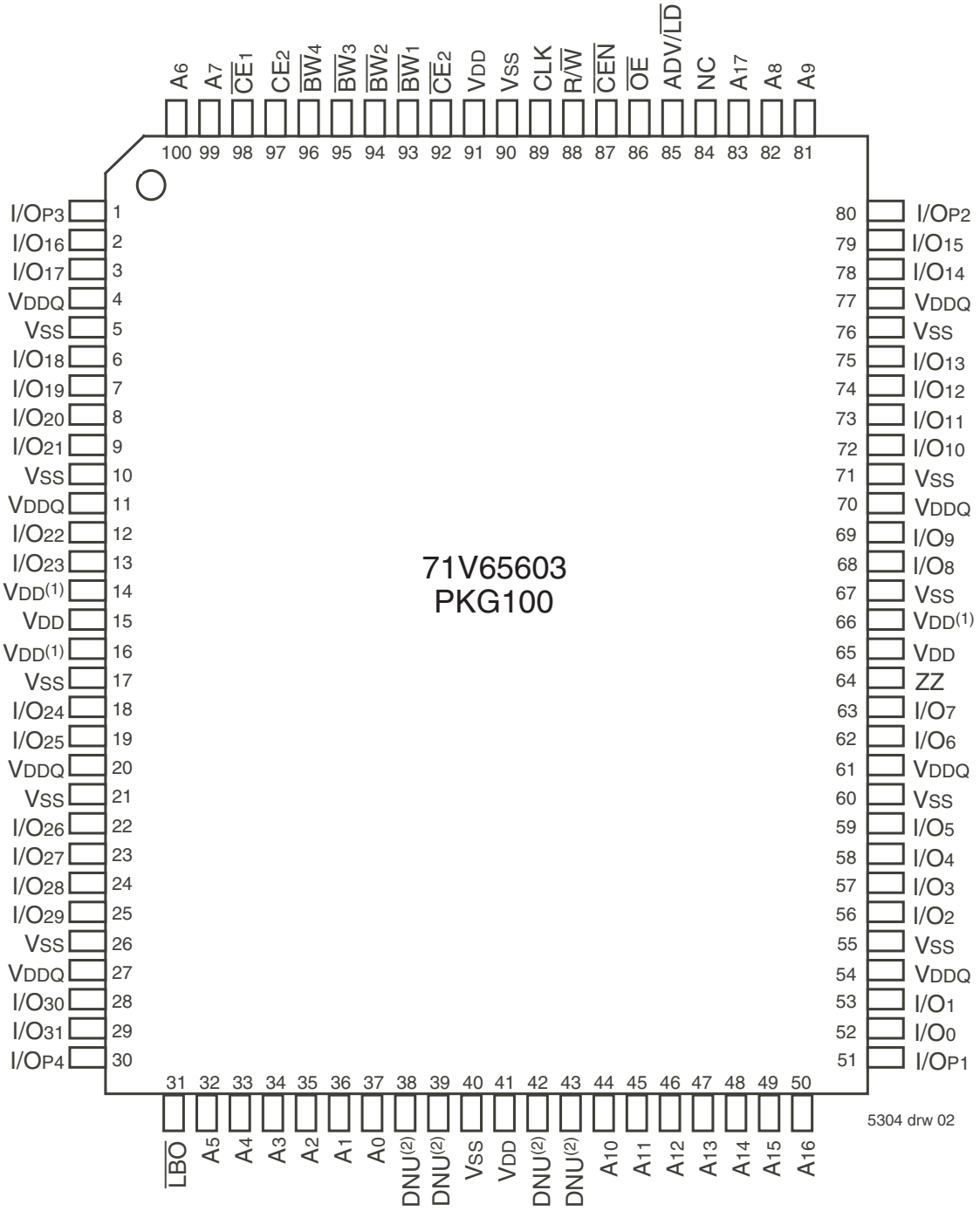
Pin Definitions(1)

Symbol	Pin Function	I/O	Active	Description
A_0-A_{18}	Address Inputs	I	N/A	Synchronous Address inputs. The address register is triggered by a combination of the rising edge of CLK, ADV/$\overline{LD}$ low, $\overline{CEN}$ low, and true chip enables.
ADV/$\overline{LD}$	Advance / Load	I	N/A	ADV/$\overline{LD}$ is a synchronous input that is used to load the internal registers with new address and control when it is sampled low at the rising edge of clock with the chip selected. When ADV/$\overline{LD}$ is low with the chip deselected, any burst in progress is terminated. When ADV/$\overline{LD}$ is sampled high then the internal burst counter is advanced for any burst that was in progress. The external addresses are ignored when ADV/$\overline{LD}$ is sampled high.
R/$\overline{W}$	Read / Write	I	N/A	R/$\overline{W}$ signal is a synchronous input that identifies whether the current load cycle initiated is a Read or Write access to the memory array. The data bus activity for the current cycle takes place two clock cycles later.
$\overline{CEN}$	Clock Enable	I	LOW	Synchronous Clock Enable Input. When $\overline{CEN}$ is sampled high, all other synchronous inputs, including clock are ignored and outputs remain unchanged. The effect of $\overline{CEN}$ sampled high on the device outputs is as if the low to high clock transition did not occur. For normal operation, $\overline{CEN}$ must be sampled low at rising edge of clock.
$\overline{BW_1}$-$\overline{BW_4}$	Individual Byte Write Enables	I	LOW	Synchronous byte write enables. Each 9-bit byte has its own active low byte write enable. On load write cycles (When R/$\overline{W}$ and ADV/$\overline{LD}$ are sampled low) the appropriate byte write signal ($\overline{BW_1}$-$\overline{BW_4}$) must be valid. The byte write signal must also be valid on each cycle of a burst write. Byte Write signals are ignored when R/$\overline{W}$ is sampled high. The appropriate byte(s) of data are written into the device two cycles later. $\overline{BW_1}$-$\overline{BW_4}$ can all be tied low if always doing write to the entire 36-bit word.
$\overline{CE_1}$, $\overline{CE_2}$	Chip Enables	I	LOW	Synchronous active low chip enable. $\overline{CE_1}$ and $\overline{CE_2}$ are used with CE_2 to enable the IDT71V65603/5803. ($\overline{CE_1}$ or $\overline{CE_2}$ sampled high or CE_2 sampled low) and ADV/$\overline{LD}$ low at the rising edge of clock, initiates a deselect cycle. The ZBT™ has a two cycle deselect, i.e., the data bus will tri-state two clock cycles after deselect is initiated.
CE_2	Chip Enable	I	HIGH	Synchronous active high chip enable. CE_2 is used with $\overline{CE_1}$ and $\overline{CE_2}$ to enable the chip. CE_2 has inverted polarity but otherwise identical to $\overline{CE_1}$ and $\overline{CE_2}$.
CLK	Clock	I	N/A	This is the clock input to the IDT71V65603/5803. Except for $\overline{OE}$, all timing references for the device are made with respect to the rising edge of CLK.
I/O_0-I/O_{31} I/O_{P1}-I/O_{P4}	Data Input/Output	I/O	N/A	Synchronous data input/output (I/O) pins. Both the data input path and data output path are registered and triggered by the rising edge of CLK.
$\overline{LBO}$	Linear Burst Order	I	LOW	Burst order selection input. When $\overline{LBO}$ is high the Interleaved burst sequence is selected. When $\overline{LBO}$ is low the Linear burst sequence is selected. $\overline{LBO}$ is a static input and it must not change during device operation.
$\overline{OE}$	Output Enable	I	LOW	Asynchronous output enable. $\overline{OE}$ must be low to read data from the 71V65603/5803. When $\overline{OE}$ is high the I/O pins are in a high-impedance state. $\overline{OE}$ does not need to be actively controlled for read and write cycles. In normal operation, $\overline{OE}$ can be tied low.
ZZ	Sleep Mode	I	N/A	Asynchronous sleep mode input. ZZ HIGH will gate the CLK internally and power down the 71V65603/5803 to its lowest power consumption level. Data retention is guaranteed in Sleep Mode.
V_{DD}	Power Supply	N/A	N/A	3.3V core power supply.
V_{DDQ}	Power Supply	N/A	N/A	3.3V I/O Supply.
V_{SS}	Ground	N/A	N/A	Ground.

5304tbl 02

NOTE:
1. All synchronous inputs must meet specified setup and hold times with respect to CLK.

Pin Configuration - 256K x 36, PKG100(3)

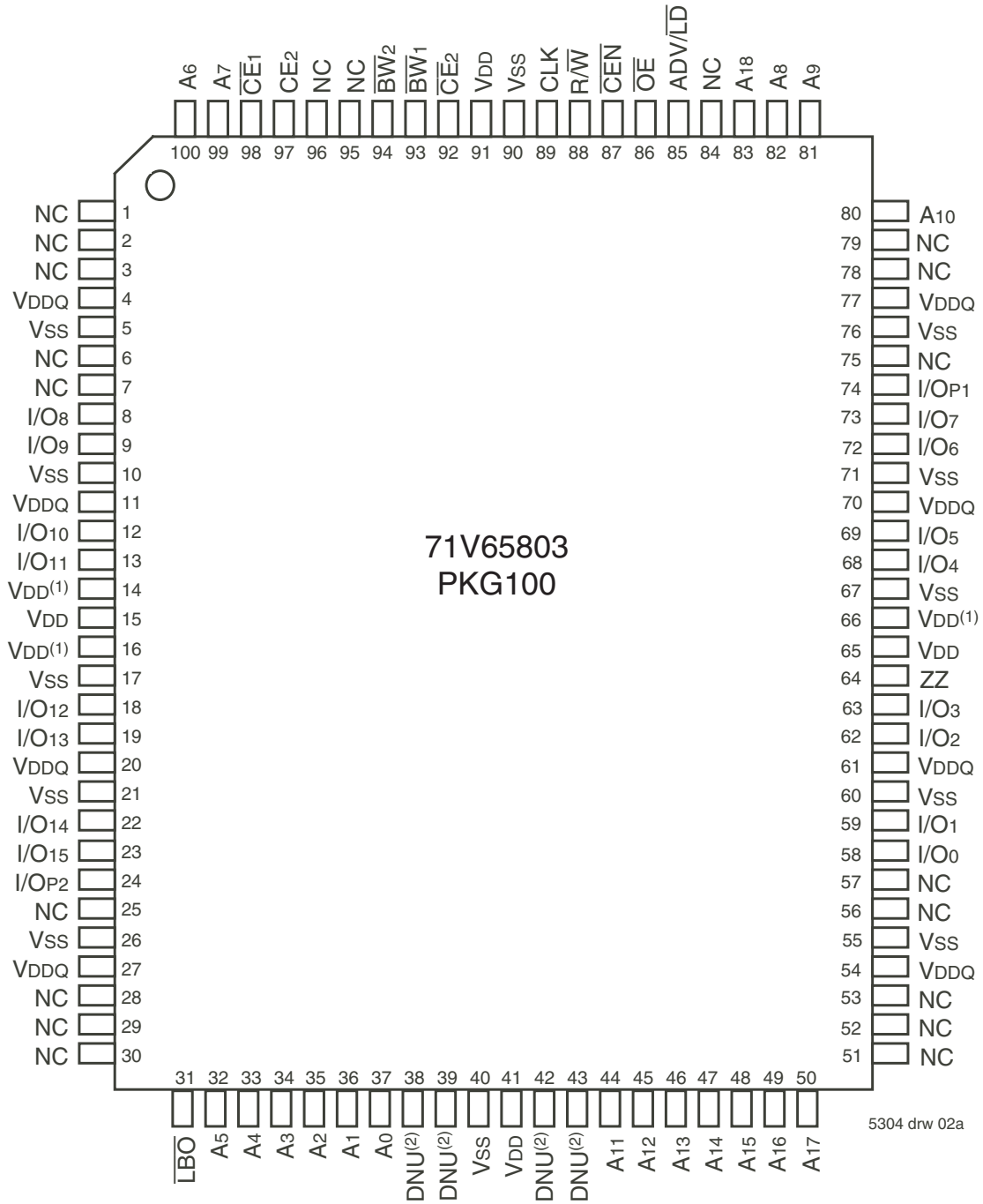


Top View
100 TQFP

NOTES:

1. Pins 14, 16 and 66 do not have to be connected directly to V_{DD} as long as the input voltage is ≥ V_{IH}.
2. DNU=Do not use. The current die revision allows these pins to be left unconnected, tied LOW (V_{SS}), or tied HIGH (V_{DD}).
3. This text does not indicate orientation of actual part-marking.

Pin Configuration - 512K x 18, PKG100(3)



Top View
100 TQFP

NOTES:
1. Pins 14, 16 and 66 do not have to be connected directly to V_{DD} as long as the input voltage is ≥ V_{IH}.
2. DNU=Do not use. The current die revision allows these pins to be left unconnected, tied LOW (V_{SS}), or tied HIGH (V_{DD}).
3. This text does not indicate orientation of actual part-marking.

Pin Configuration - 256K X 36, BG119, BGG119(3)

	1	2	3	4	5	6	7
A	VDDQ	A6	A4	NC	A8	A16	VDDQ
B	NC	CE2	A3	ADV/$\overline{LD}$	A9	$\overline{CE_2}$	NC
C	NC	A7	A2	VDD	A12	A15	NC
D	I/O16	I/OP3	VSS	NC	VSS	I/OP2	I/O15
E	I/O17	I/O18	VSS	$\overline{CE_1}$	VSS	I/O13	I/O14
F	VDDQ	I/O19	VSS	$\overline{OE}$	VSS	I/O12	VDDQ
G	I/O20	I/O21	$\overline{BW_3}$	A17	$\overline{BW_2}$	I/O11	I/O10
H	I/O22	I/O23	VSS	R/$\overline{W}$	VSS	I/O9	I/O8
J	VDDQ	VDD	VDD(1)	VDD	VDD(1)	VDD	VDDQ
K	I/O24	I/O26	VSS	CLK	VSS	I/O6	I/O7
L	I/O25	I/O27	$\overline{BW_4}$	NC	$\overline{BW_1}$	I/O4	I/O5
M	VDDQ	I/O28	VSS	$\overline{CEN}$	VSS	I/O3	VDDQ
N	I/O29	I/O30	VSS	A1	VSS	I/O2	I/O1
P	I/O31	I/OP4	VSS	A0	VSS	I/OP1	I/O0
R	NC	A5	$\overline{LBO}$	VDD	VDD(1)	A13	NC
T	NC	NC	A10	A11	A14	NC	ZZ
U	VDDQ	DNU(2)	DNU(2)	DNU(2)	DNU(2)	DNU(2)	VDDQ

5304 drw 13a

Top View

Pin Configuration - 512K X 18, BG119, BGG119(3)

	1	2	3	4	5	6	7
A	VDDQ	A6	A4	NC	A8	A16	VDDQ
B	NC	CE2	A3	ADV/$\overline{LD}$	A9	$\overline{CE_2}$	NC
C	NC	A7	A2	VDD	A13	A17	NC
D	I/O8	NC	VSS	NC	VSS	I/OP1	NC
E	NC	I/O9	VSS	$\overline{CE_1}$	VSS	NC	I/O7
F	VDDQ	NC	VSS	$\overline{OE}$	VSS	I/O6	VDDQ
G	NC	I/O10	$\overline{BW_2}$	A18	VSS	NC	I/O5
H	I/O11	NC	VSS	R/$\overline{W}$	VSS	I/O4	NC
J	VDDQ	VDD	VDD(1)	VDD	VDD(1)	VDD	VDDQ
K	NC	I/O12	VSS	CLK	VSS	NC	I/O3
L	I/O13	NC	VSS	NC	$\overline{BW_1}$	I/O2	NC
M	VDDQ	I/O14	VSS	$\overline{CEN}$	VSS	NC	VDDQ
N	I/O15	NC	VSS	A1	VSS	I/O 1	NC
P	NC	I/OP2	VSS	A0	VSS	NC	I/O 0
R	NC	A5	$\overline{LBO}$	VDD	VDD(1)	A12	NC
T	NC	A10	A15	NC	A14	A11	ZZ
U	VDDQ	DNU(2)	DNU(2)	DNU(2)	DNU(2)	DNU(2)	VDDQ

5304 drw 13b

Top View

NOTES:

1. J3, J5, and R5 do not have to be directly connected to V_{DD} as long as the input voltage is $\geq V_{IH}$.
2. DNU = Do not use. The current die revision allows these pins to be left unconnected, tied LOW (V_{SS}), or tied HIGH (V_{DD}).
3. This text does not indicate orientation of actual part-marking.

Pin Configuration - 256K X 36, BQ165, BQG165(3)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A7	$\overline{CE}_1$	$\overline{BW}_3$	$\overline{BW}_2$	$\overline{CE}_2$	$\overline{CEN}$	ADV/$\overline{LD}$	A17	A8	NC
B	NC	A6	CE2	$\overline{BW}_4$	$\overline{BW}_1$	CLK	R/$\overline{W}$	$\overline{OE}$	NC	A9	NC
C	I/OP3	NC	VDDQ	VSS	VSS	VSS	VSS	VSS	VDDQ	NC	I/OP2
D	I/O17	I/O16	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O15	I/O14
E	I/O19	I/O18	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O13	I/O12
F	I/O21	I/O20	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O11	I/O10
G	I/O_{23}	I/O22	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O9	I/O8
H	VDD(1)	VDD(1)	NC	VDD	VSS	VSS	VSS	VDD	NC	NC	ZZ
J	I/O25	I/O24	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O7	I/O6
K	I/O27	I/O26	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O5	I/O4
L	I/O29	I/O28	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O3	I/O2
M	I/O31	I/O30	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O1	I/O0
N	I/OP4	NC	VDDQ	VSS	DNU(2)	NC	VDD(1)	VSS	VDDQ	NC	I/OP1
P	NC	NC	A5	A2	DNU(2)	A1	DNU(2)	A10	A13	A14	NC
R	$\overline{LBO}$	NC	A4	A3	DNU(2)	A0	DNU(2)	A11	A12	A15	A16

5304 tbl 25a

Pin Configuration - 512K X 18, BQ165, BQG165(3)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A7	$\overline{CE}_1$	$\overline{BW}_2$	NC	$\overline{CE}_2$	$\overline{CEN}$	ADV/$\overline{LD}$	A18	A8	A10
B	NC	A6	CE2	NC	$\overline{BW}_1$	CLK	R/$\overline{W}$	$\overline{OE}$	NC	A9	NC
C	NC	NC	VDDQ	VSS	VSS	VSS	VSS	VSS	VDDQ	NC	I/OP1
D	NC	I/O8	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	I/O7
E	NC	I/O9	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	I/O6
F	NC	I/O10	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	I/O5
G	NC	I/O11	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	I/O4
H	VDD(1)	VDD(1)	NC	VDD	VSS	VSS	VSS	VDD	NC	NC	ZZ
J	I/O12	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O3	NC
K	I/O13	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O2	NC
L	I/O14	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O1	NC
M	I/O15	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O0	NC
N	I/OP2	NC	VDDQ	VSS	DNU(2)	NC	VDD(1)	VSS	VDDQ	NC	NC
P	NC	NC	A5	A2	DNU(2)	A1	DNU(2)	A11	A14	A15	NC
R	$\overline{LBO}$	NC	A4	A3	DNU(2)	A0	DNU(2)	A12	A13	A16	A17

5304 tbl25b

NOTES:

1. H1, H2, and N7 do not have to be directly connected to VDD as long as the input voltage is ≥ VIH.
2. DNU=Do not use. The current die revision allows these pins to be left unconnected, tied LOW (VSS), or tied HIGH (VDD).
3 This text does not indicate orientation of actual part-marking.

Absolute Maximum Ratings(1)

Symbol	Rating	Commercial & Industrial	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
V_{TERM}(3,6)	Terminal Voltage with Respect to GND	-0.5 to V_{DD}	V
V_{TERM}(4,6)	Terminal Voltage with Respect to GND	-0.5 to V_{DD} +0.5	V
V_{TERM}(5,6)	Terminal Voltage with Respect to GND	-0.5 to V_{DDQ} +0.5	V
T_A(7)	**Commercial** Operating Temperature	-0 to +70	°C
	Industrial Operating Temperature	-40 to +85	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-55 to +125	°C
P_T	Power Dissipation	2.0	W
I_{OUT}	DC Output Current	50	mA

5304 tbl 06

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{DD} terminals only.
3. V_{DDQ} terminals only.
4. Input terminals only.
5. I/O terminals only.
6. This is a steady-state DC parameter that applies after the power supply has reached its nominal operating value. Power sequencing is not necessary; however, the voltage on any input or I/O pin cannot exceed V_{DDQ} during power supply ramp up.
7. During production testing, the case temperature equals T_A.

Recommended Operating Temperature and Supply Voltage

Grade	Ambient Temperature(1)	V_{SS}	V_{DD}	V_{DDQ}
Commercial	0° C to +70° C	0V	3.3V±5%	3.3V±5%
Industrial	-40°C to +85°C	0V	3.3V±5%	3.3V±5%

5304 tbl 05

NOTE:
1. During production testing, the case temperature equals the ambient temperature.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Core Supply Voltage	3.135	3.3	3.465	V
V_{DDQ}	I/O Supply Voltage	3.135	3.3	3.465	V
V_{SS}	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage - Inputs	2.0	—	V_{DD}+0.3	V
V_{IH}	Input High Voltage - I/O	2.0	—	V_{DDQ}+0.3	V
V_{IL}	Input Low Voltage	-0.3(1)	—	0.8	V

5304 tbl 04

NOTE:
1. V_{IL} (min.) = –1.0V for pulse width less than $t_{CYC}/2$, once per cycle.

165 fBGA Capacitance(1)

(T_A = +25° C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	TBD	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	TBD	pF

5304 tbl 07b

100 TQFP Capacitance(1)

(T_A = +25° C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	5	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	7	pF

5304 tbl 07

119 BGA Capacitance(1)

(T_A = +25° C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	7	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	7	pF

5304 tbl 07a

NOTE:
1. This parameter is guaranteed by device characterization, but not production tested.

Synchronous Truth Table(1)

$\overline{CEN}$	R/$\overline{W}$	Chip(5) Enable	ADV/$\overline{LD}$	$\overline{BW}$x	ADDRESS USED	PREVIOUS CYCLE	CURRENT CYCLE	I/O (2 cycles later)
L	L	Select	L	Valid	External	X	LOAD WRITE	D(7)
L	H	Select	L	X	External	X	LOAD READ	Q(7)
L	X	X	H	Valid	Internal	LOAD WRITE / BURST WRITE	BURST WRITE (Advance burst counter)(2)	D(7)
L	X	X	H	X	Internal	LOAD READ / BURST READ	BURST READ (Advance burst counter)(2)	Q(7)
L	X	Deselect	L	X	X	X	DESELECT or STOP(3)	HiZ
L	X	X	H	X	X	DESELECT / NOOP	NOOP	HiZ
H	X	X	X	X	X	X	SUSPEND(4)	Previous Value

5304 tbl 08

NOTES:
1. L = V_{IL}, H = V_{IH}, X = Don't Care.
2. When ADV/$\overline{LD}$ signal is sampled high, the internal burst counter is incremented. The R/$\overline{W}$ signal is ignored when the counter is advanced. Therefore the nature of the burst cycle (Read or Write) is determined by the status of the R/$\overline{W}$ signal when the first address is loaded at the beginning of the burst cycle.
3. Deselect cycle is initiated when either ($\overline{CE}_1$, or $\overline{CE}_2$ is sampled high or CE_2 is sampled low) and ADV/$\overline{LD}$ is sampled low at rising edge of clock. The data bus will tri-state two cycles after deselect is initiated.
4. When $\overline{CEN}$ is sampled high at the rising edge of clock, that clock edge is blocked from propagating through the part. The state of all the internal registers and the I/Os remains unchanged.
5. To select the chip requires $\overline{CE}_1$ = L, $\overline{CE}_2$ = L, CE_2 = H on these chip enables. Chip is deselected if any one of the chip enables is false.
6. Device Outputs are ensured to be in High-Z after the first rising edge of clock upon power-up.
7. Q - Data read from the device, D - data written to the device.

Partial Truth Table for Writes(1)

OPERATION	R/$\overline{W}$	$\overline{BW}_1$	$\overline{BW}_2$	$\overline{BW}_3$(3)	$\overline{BW}_4$(3)
READ	H	X	X	X	X
WRITE ALL BYTES	L	L	L	L	L
WRITE BYTE 1 (I/O[0:7], I/O_{P1})(2)	L	L	H	H	H
WRITE BYTE 2 (I/O[8:15], I/O_{P2})(2)	L	H	L	H	H
WRITE BYTE 3 (I/O[16:23], I/O_{P3})(2,3)	L	H	H	L	H
WRITE BYTE 4 (I/O[24:31], I/O_{P4})(2,3)	L	H	H	H	L
NO WRITE	L	H	H	H	H

5304 tbl 09

NOTES:
1. L = V_{IL}, H = V_{IH}, X = Don't Care.
2. Multiple bytes may be selected during the same cycle.
3. N/A for X18 configuration.

Interleaved Burst Sequence Table ($\overline{LBO}$=VDD)

	Sequence 1		Sequence 2		Sequence 3		Sequence 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
Second Address	0	1	0	0	1	1	1	0
Third Address	1	0	1	1	0	0	0	1
Fourth Address(1)	1	1	1	0	0	1	0	0

5304 tbl 10

NOTE:
1. Upon completion of the Burst sequence the counter wraps around to its initial state and continues counting.

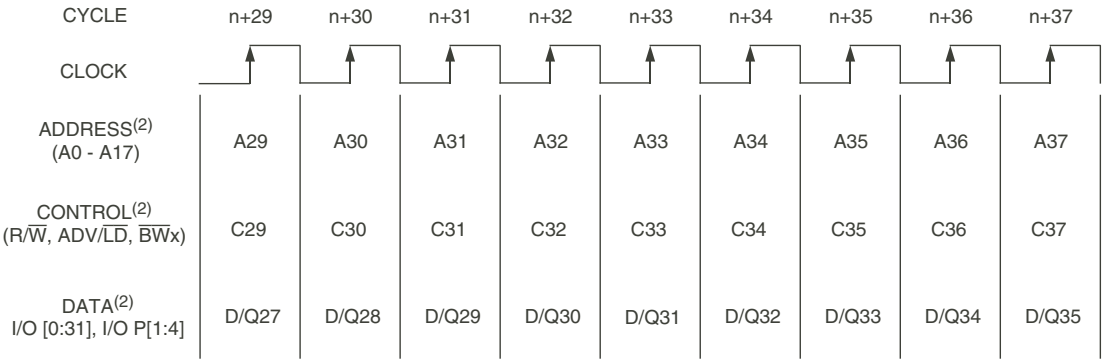
Linear Burst Sequence Table ($\overline{LBO}$=Vss)

	Sequence 1		Sequence 2		Sequence 3		Sequence 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
Second Address	0	1	1	0	1	1	0	0
Third Address	1	0	1	1	0	0	0	1
Fourth Address(1)	1	1	0	0	0	1	1	0

5304 tbl 11

NOTE:
1. Upon completion of the Burst sequence the counter wraps around to its initial state and continues counting.

Functional Timing Diagram(1)



5304 drw 03

NOTES:
1. This assumes $\overline{CEN}$, $\overline{CE}_1$, CE_2, $\overline{CE}_2$ are all true.
2. All Address, Control and Data_In are only required to meet set-up and hold time with respect to the rising edge of clock. Data_Out is valid after a clock-to-data delay from the rising edge of clock.

Device Operation - Showing Mixed Load, Burst, Deselect and NOOP Cycles(2)

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}$(1)	$\overline{CEN}$	$\overline{BW}$x	$\overline{OE}$	I/O	Comments
n	A_0	H	L	L	L	X	X	X	Load read
n+1	X	X	H	X	L	X	X	X	Burst read
n+2	A_1	H	L	L	L	X	L	Q_0	Load read
n+3	X	X	L	H	L	X	L	Q_{0+1}	Deselect or STOP
n+4	X	X	H	X	L	X	L	Q_1	NOOP
n+5	A_2	H	L	L	L	X	X	Z	Load read
n+6	X	X	H	X	L	X	X	Z	Burst read
n+7	X	X	L	H	L	X	L	Q_2	Deselect or STOP
n+8	A_3	L	L	L	L	L	L	Q_{2+1}	Load write
n+9	X	X	H	X	L	L	X	Z	Burst write
n+10	A_4	L	L	L	L	L	X	D_3	Load write
n+11	X	X	L	H	L	X	X	D_{3+1}	Deselect or STOP
n+12	X	X	H	X	L	X	X	D_4	NOOP
n+13	A_5	L	L	L	L	L	X	Z	Load write
n+14	A_6	H	L	L	L	X	X	Z	Load read
n+15	A_7	L	L	L	L	L	X	D_5	Load write
n+16	X	X	H	X	L	L	L	Q_6	Burst write
n+17	A_8	H	L	L	L	X	X	D_7	Load read
n+18	X	X	H	X	L	X	X	D_{7+1}	Burst read
n+19	A_9	L	L	L	L	L	L	Q_8	Load write

5304tbl 12

NOTES:
1. $\overline{CE}$ = L is defined as $\overline{CE}_1$ = L, $\overline{CE}_2$ = L and CE_2 = H. $\overline{CE}$ = H is defined as $\overline{CE}_1$ = H, $\overline{CE}_2$ = H or CE_2 = L.
2. H = High; L = Low; X = Don't Care; Z = High Impedance.

Read Operation(1)

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}$(2)	$\overline{CEN}$	$\overline{BW}$x	$\overline{OE}$	I/O	Comments
n	A_0	H	L	L	L	X	X	X	Address and Control meet setup
n+1	X	X	X	X	L	X	X	X	Clock Setup Valid
n+2	X	X	X	X	X	X	L	Q_0	Contents of Address A_0 Read Out

5304 tbl 13

NOTES:
1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\overline{CE}$ = L is defined as $\overline{CE}_1$ = L, $\overline{CE}_2$ = L and CE_2 = H. $\overline{CE}$ = H is defined as $\overline{CE}_1$ = H, $\overline{CE}_2$ = H or CE_2 = L.

Burst Read Operation(1)

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}$(2)	$\overline{CEN}$	$\overline{BW}$x	$\overline{OE}$	I/O	Comments
n	A_0	H	L	L	L	X	X	X	Address and Control meet setup
n+1	X	X	H	X	L	X	X	X	Clock Setup Valid, Advance Counter
n+2	X	X	H	X	L	X	L	Q_0	Address A_0 Read Out, Inc. Count
n+3	X	X	H	X	L	X	L	Q_{0+1}	Address A_{0+1} Read Out, Inc. Count
n+4	X	X	H	X	L	X	L	Q_{0+2}	Address A_{0+2} Read Out, Inc. Count
n+5	A_1	H	L	L	L	X	L	Q_{0+3}	Address A_{0+3} Read Out, Load A_1
n+6	X	X	H	X	L	X	L	Q_0	Address A_0 Read Out, Inc. Count
n+7	X	X	H	X	L	X	L	Q_1	Address A_1 Read Out, Inc. Count
n+8	A_2	H	L	L	L	X	L	Q_{1+1}	Address A_{1+1} Read Out, Load A_2

5304 tbl 14

NOTES:
1. H = High; L = Low; X = Don't Care; Z = High Impedance..
2. $\overline{CE}$ = L is defined as $\overline{CE}_1$ = L, $\overline{CE}_2$ = L and CE_2 = H. $\overline{CE}$ = H is defined as $\overline{CE}_1$ = H, $\overline{CE}_2$ = H or CE_2 = L.

Write Operation(1)

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}$(2)	$\overline{CEN}$	$\overline{BW}$x	$\overline{OE}$	I/O	Comments
n	A_0	L	L	L	L	L	X	X	Address and Control meet setup
n+1	X	X	X	X	L	X	X	X	Clock Setup Valid
n+2	X	X	X	X	L	X	X	D_0	Write to Address A_0

5304 tbl 15

NOTES:
1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\overline{CE}$ = L is defined as $\overline{CE}_1$ = L, $\overline{CE}_2$ = L and CE_2 = H. $\overline{CE}$ = H is defined as $\overline{CE}_1$ = H, $\overline{CE}_2$ = H or CE_2 = L.

Burst Write Operation(1)

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}$(2)	$\overline{CEN}$	$\overline{BW}$x	$\overline{OE}$	I/O	Comments
n	A_0	L	L	L	L	L	X	X	Address and Control meet setup
n+1	X	X	H	X	L	L	X	X	Clock Setup Valid, Inc. Count
n+2	X	X	H	X	L	L	X	D_0	Address A_0 Write, Inc. Count
n+3	X	X	H	X	L	L	X	D_{0+1}	Address A_{0+1} Write, Inc. Count
n+4	X	X	H	X	L	L	X	D_{0+2}	Address A_{0+2} Write, Inc. Count
n+5	A_1	L	L	L	L	L	X	D_{0+3}	Address A_{0+3} Write, Load A_1
n+6	X	X	H	X	L	L	X	D_0	Address A_0 Write, Inc. Count
n+7	X	X	H	X	L	L	X	D_1	Address A_1 Write, Inc. Count
n+8	A_2	L	L	L	L	L	X	D_{1+1}	Address A_{1+1} Write, Load A_2

5304 tbl 16

NOTES:
1. H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance.
2. $\overline{CE}$ = L is defined as $\overline{CE}_1$ = L, $\overline{CE}_2$ = L and CE_2 = H. $\overline{CE}$ = H is defined as $\overline{CE}_1$ = H, $\overline{CE}_2$ = H or CE_2 = L.

Read Operation with Clock Enable Used(1)

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}$(2)	$\overline{CEN}$	$\overline{BW}$x	$\overline{OE}$	I/O	Comments
n	A_0	H	L	L	L	X	X	X	Address and Control meet setup
n+1	X	X	X	X	H	X	X	X	Clock n+1 Ignored
n+2	A_1	H	L	L	L	X	X	X	Clock Valid
n+3	X	X	X	X	H	X	L	Q_0	Clock Ignored, Data Q_0 is on the bus.
n+4	X	X	X	X	H	X	L	Q_0	Clock Ignored, Data Q_0 is on the bus.
n+5	A_2	H	L	L	L	X	L	Q_0	Address A_0 Read out (bus trans.)
n+6	A_3	H	L	L	L	X	L	Q_1	Address A_1 Read out (bus trans.)
n+7	A_4	H	L	L	L	X	L	Q_2	Address A2 Read out (bus trans.)

5304 tbl 17

NOTES:
1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\overline{CE}$ = L is defined as $\overline{CE}_1$ = L, $\overline{CE}_2$ = L and CE_2 = H. $\overline{CE}$ = H is defined as $\overline{CE}_1$ = H, $\overline{CE}_2$ = H or CE_2 = L.

Write Operation with Clock Enable Used(1)

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}$(2)	$\overline{CEN}$	$\overline{BW}$x	$\overline{OE}$	I/O	Comments
n	A_0	L	L	L	L	L	X	X	Address and Control meet setup.
n+1	X	X	X	X	H	X	X	X	Clock n+1 Ignored.
n+2	A_1	L	L	L	L	L	X	X	Clock Valid.
n+3	X	X	X	X	H	X	X	X	Clock Ignored.
n+4	X	X	X	X	H	X	X	X	Clock Ignored.
n+5	A_2	L	L	L	L	L	X	D_0	Write Data D_0
n+6	A_3	L	L	L	L	L	X	D_1	Write Data D_1
n+7	A_4	L	L	L	L	L	X	D_2	Write Data D_2

5304 tbl 18

NOTES:
1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\overline{CE}$ = L is defined as $\overline{CE}_1$ = L, $\overline{CE}_2$ = L and CE_2 = H. $\overline{CE}$ = H is defined as $\overline{CE}_1$ = H, $\overline{CE}_2$ = H or CE_2 = L.

Read Operation with Chip Enable Used(1)

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}$(2)	$\overline{CEN}$	$\overline{BW}$x	$\overline{OE}$	I/O(3)	Comments
n	X	X	L	H	L	X	X	?	Deselected.
n+1	X	X	L	H	L	X	X	?	Deselected.
n+2	A_0	H	L	L	L	X	X	Z	Address and Control meet setup
n+3	X	X	L	H	L	X	X	Z	Deselected or STOP.
n+4	A_1	H	L	L	L	X	L	Q_0	Address A_0 Read out. Load A_1.
n+5	X	X	L	H	L	X	X	Z	Deselected or STOP.
n+6	X	X	L	H	L	X	L	Q_1	Address A_1 Read out. Deselected.
n+7	A_2	H	L	L	L	X	X	Z	Address and control meet setup.
n+8	X	X	L	H	L	X	X	Z	Deselected or STOP.
n+9	X	X	L	H	L	X	L	Q_2	Address A_2 Read out. Deselected.

5304 tbl 19

NOTES:
1. H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance.
2. $\overline{CE}$ = L is defined as $\overline{CE}_1$ = L, $\overline{CE}_2$ = L and CE_2 = H. $\overline{CE}$ = H is defined as $\overline{CE}_1$ = H, $\overline{CE}_2$ = H or CE_2 = L.
3. Device Outputs are ensured to be in High-Z after the first rising edge of clock upon power-up.

Write Operation with Chip Enable Used(1)

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}$(2)	$\overline{CEN}$	$\overline{BW}$x	$\overline{OE}$	I/O(3)	Comments
n	X	X	L	H	L	X	X	?	Deselected.
n+1	X	X	L	H	L	X	X	?	Deselected.
n+2	A_0	L	L	L	L	L	X	Z	Address and Control meet setup
n+3	X	X	L	H	L	X	X	Z	Deselected or STOP.
n+4	A_1	L	L	L	L	L	X	D_0	Address D_0 Write in. Load A_1.
n+5	X	X	L	H	L	X	X	Z	Deselected or STOP.
n+6	X	X	L	H	L	X	X	D_1	Address D_1 Write in. Deselected.
n+7	A_2	L	L	L	L	L	X	Z	Address and control meet setup.
n+8	X	X	L	H	L	X	X	Z	Deselected or STOP.
n+9	X	X	L	H	L	X	X	D_2	Address D_2 Write in. Deselected.

5304 tbl 20

NOTES:
1. H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance.
2. $\overline{CE}$ = L is defined as $\overline{CE}_1$ = L, $\overline{CE}_2$ = L and CE_2 = H. $\overline{CE}$ = H is defined as $\overline{CE}_1$ = H, $\overline{CE}_2$ = H or CE_2 = L.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{DD} = 3.3V +/-5%)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{DD} = Max., V_{IN} = 0V to V_{DD}	—	5	µA
$\|I_{LI}\|$	$\overline{LBO}$ Input Leakage Current[1]	V_{DD} = Max., V_{IN} = 0V to V_{DD}	—	30	µA
$\|I_{LO}\|$	Output Leakage Current	V_{OUT} = 0V to V_{DDQ}, Device Deselected	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = +8mA, V_{DD} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -8mA, V_{DD} = Min.	2.4	—	V

NOTE:
5304 tbl 21

1. The $\overline{LBO}$ pin will be internally pulled to V_{DD} if it is not actively driven in the application and the ZZ pin will be internally pulled to Vss if not actively driven.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range[1] (V_{DD} = 3.3V +/-5%)

Symbol	Parameter	Test Conditions	150MHz		133MHz		100MHz		Unit
			Com'l	Ind	Com'l	Ind	Com'l	Ind	
I_{DD}	Operating Power Supply Current	Device Selected, Outputs Open, ADV/$\overline{LD}$ = X, V_{DD} = Max., $V_{IN} \geq V_{IH}$ or $\leq V_{IL}$, f = f_{MAX}[2]	325	345	300	320	250	270	mA
I_{SB1}	CMOS Standby Power Supply Current	Device Deselected, Outputs Open, V_{DD} = Max., $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, f = 0[2,3]	40	60	40	60	40	60	mA
I_{SB2}	Clock Running Power Supply Current	Device Deselected, Outputs Open, V_{DD} = Max., $V_{IN} \geq V_{HD}$ or < V_{LD}, f = f_{MAX}[2,3]	120	140	110	130	100	120	mA
I_{SB3}	Idle Power Supply Current	Device Selected, Outputs Open, $\overline{CEN} \geq V_{IH}$, V_{DD} = Max., $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, f = f_{MAX}[2,3]	40	60	40	60	40	60	mA
I_{ZZ}	Full Sleep Mode Supply Current	Device Selected, Outputs Open $\overline{CEN} \leq V_{IL}$, V_{DD} = Max., ZZ $\geq V_{HD}$ $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, f = fMax[2,3]	40	60	40	60	40	60	mA

NOTES:
5304 tbl 22

1. All values are maximum guaranteed values.
2. At f = f_{MAX}, inputs are cycling at the maximum frequency of read cycles of 1/t_{CYC}; f=0 means no input lines are changing.
3. For I/Os V_{HD} = V_{DDQ} – 0.2V, V_{LD} = 0.2V. For other inputs V_{HD} = V_{DD} – 0.2V, V_{LD} = 0.2V.

AC Test Load

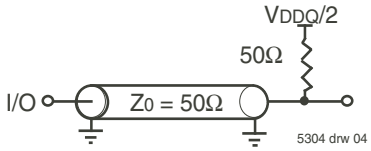


Figure 1. AC Test Load

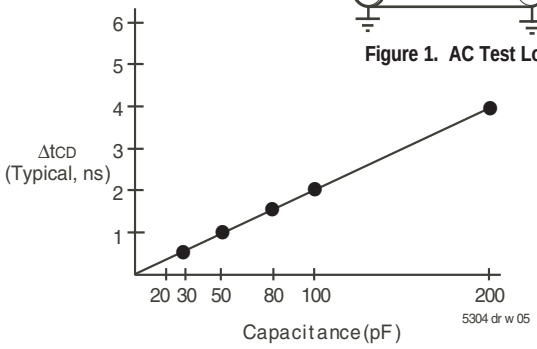


Figure 2. Lumped Capacitive Load, Typical Derating

AC Test Conditions (V_{DDQ} = 3.3V)

Input Pulse Levels	0 to 3V
Input Rise/Fall Times	2ns
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
AC Test Load	See Figure 1

5304 tbl 23

AC Electrical Characteristics

(VDD = 3.3V +/-5%, Commercial and Industrial Temperature Ranges)

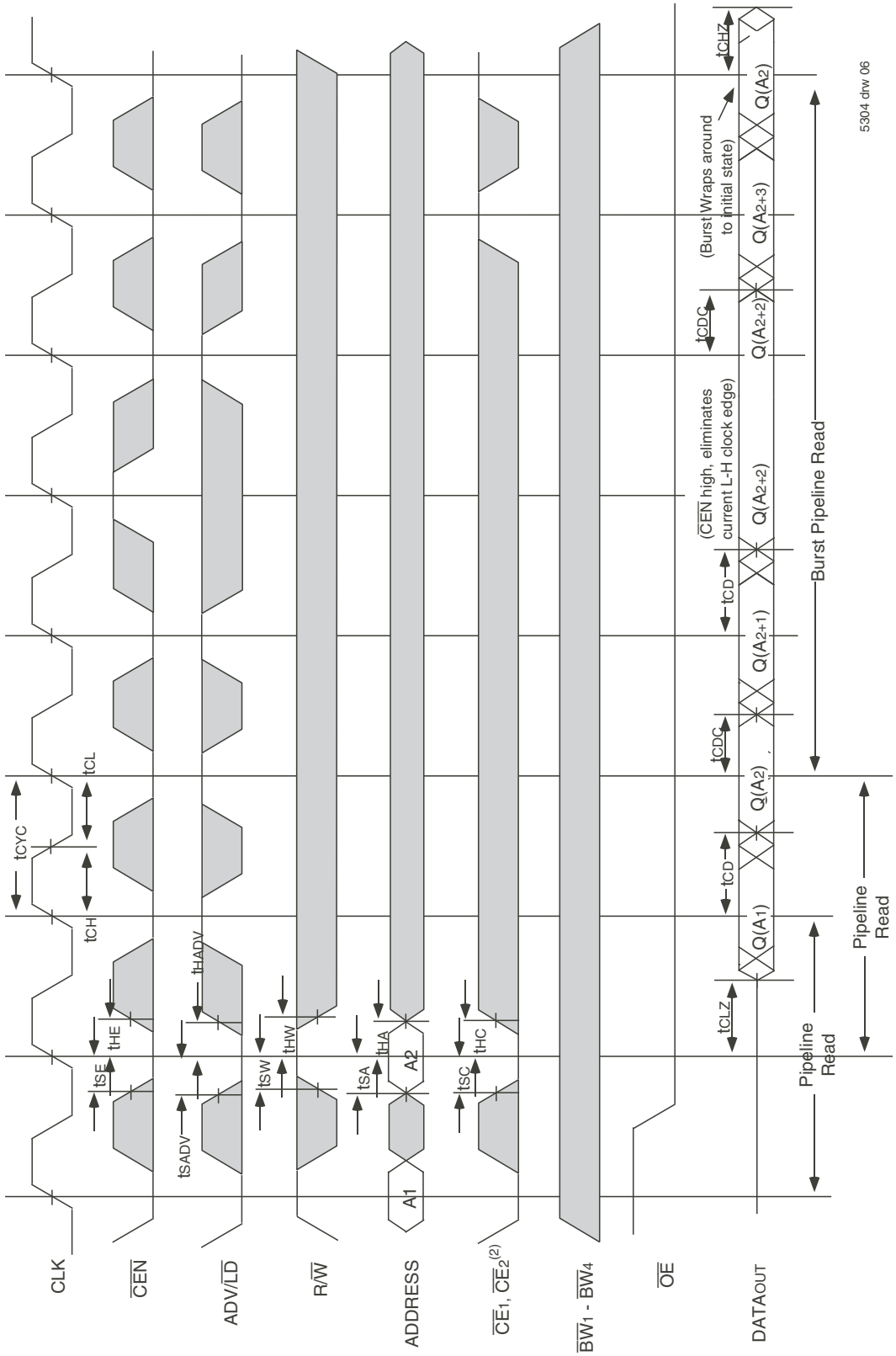
Symbol	Parameter	150MHz(6)		133MHz		100MHz		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC}	Clock Cycle Time	6.7	—	7.5	—	10	—	ns
t_F(1)	Clock Frequency	—	150	—	133	—	100	MHz
t_{CH}(2)	Clock High Pulse Width	2.0	—	2.2	—	3.2	—	ns
t_{CL}(2)	Clock Low Pulse Width	2.0	—	2.2	—	3.2	—	ns
Output Parameters								
t_{CD}	Clock High to Valid Data	—	3.8.	—	4.2	—	5	ns
t_{CDC}	Clock High to Data Change	1.5	—	1.5	—	1.5	—	ns
t_{CLZ}(3,4,5)	Clock High to Output Active	1.5	—	1.5	—	1.5	—	ns
t_{CHZ}(3,4,5)	Clock High to Data High-Z	1.5	3	1.5	3	1.5	3.3	ns
t_{OE}	Output Enable Access Time	—	3.8	—	4.2	—	5	ns
t_{OLZ}(3,4)	Output Enable Low to Data Active	0	—	0	—	0	—	ns
t_{OHZ}(3,4)	Output Enable High to Data High-Z	—	3.8	—	4.2	—	5	ns
Set Up Times								
t_{SE}	Clock Enable Setup Time	1.5	—	1.7	—	2.0	—	ns
t_{SA}	Address Setup Time	1.5	—	1.7	—	2.0	—	ns
t_{SD}	Data In Setup Time	1.5	—	1.7	—	2.0	—	ns
t_{SW}	Read/Write (R/$\overline{W}$) Setup Time	1.5	—	1.7	—	2.0	—	ns
t_{SADV}	Advance/Load (ADV/$\overline{LD}$) Setup Time	1.5	—	1.7	—	2.0	—	ns
t_{SC}	Chip Enable/Select Setup Time	1.5	—	1.7	—	2.0	—	ns
t_{SB}	Byte Write Enable ($\overline{BW}$x) Setup Time	1.5	—	1.7	—	2.0	—	ns
Hold Times								
t_{HE}	Clock Enable Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{HA}	Address Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{HD}	Data In Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{HW}	Read/Write (R/$\overline{W}$) Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{HADV}	Advance/Load (ADV/$\overline{LD}$) Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{HC}	Chip Enable/Select Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{HB}	Byte Write Enable ($\overline{BW}$x) Hold Time	0.5	—	0.5	—	0.5	—	ns

5304 tbl 24

NOTES:

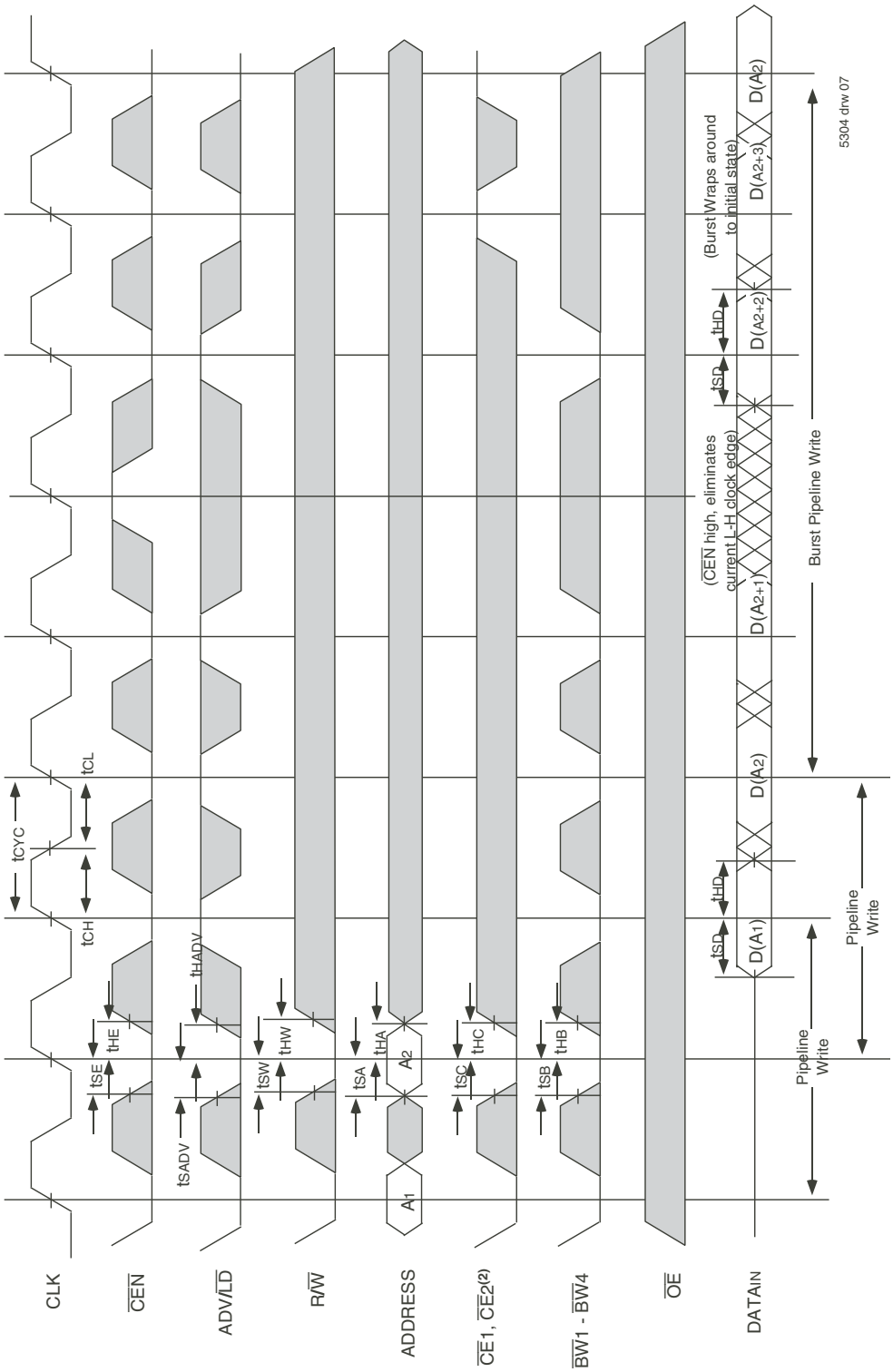
1. $t_F = 1/t_{CYC}$.
2. Measured as HIGH above 0.6V_{DDQ} and LOW below 0.4V_{DDQ}.
3. Transition is measured ±200mV from steady-state.
4. These parameters are guaranteed with the AC load (Figure 1) by device characterization. They are not production tested.
5. To avoid bus contention, the output buffers are designed such that t_{CHZ} (device turn-off) is about 1ns faster than t_{CLZ} (device turn-on) at a given temperature and voltage. The specs as shown do not imply bus contention because t_{CLZ} is a Min. parameter that is worse case at totally different test conditions (0 deg. C, 3.465V) than t_{CHZ}, which is a Max. parameter (worse case at 70 deg. C, 3.135V).
6. Commercial temperature range only.

Timing Waveform of Read Cycle(1,2,3,4)



NOTES:
1. Q (A1) represents the first output from the external address A1. Q (A2) represents the first output from the external address A2; Q (A2+1) represents the next output data in the burst sequence of the base address A2, etc. where address bits A0 and A1 are advancing for the four word burst in the sequence defined by the state of the $\overline{LBO}$ input.
2. CE_2 timing transitions are identical but inverted to the $\overline{CE}_1$ and $\overline{CE}_2$ signals. For example, when $\overline{CE}_1$ and $\overline{CE}_2$ are LOW on this waveform, CE_2 is HIGH.
3. Burst ends when new address and control are loaded into the SRAM by sampling ADV/$\overline{LD}$ LOW.
4. R/$\overline{W}$ is don't care when the SRAM is bursting (ADV/$\overline{LD}$ sampled HIGH). The nature of the burst access (Read or Write) is fixed by the state of the R/$\overline{W}$ signal when new address and control are loaded into the SRAM.

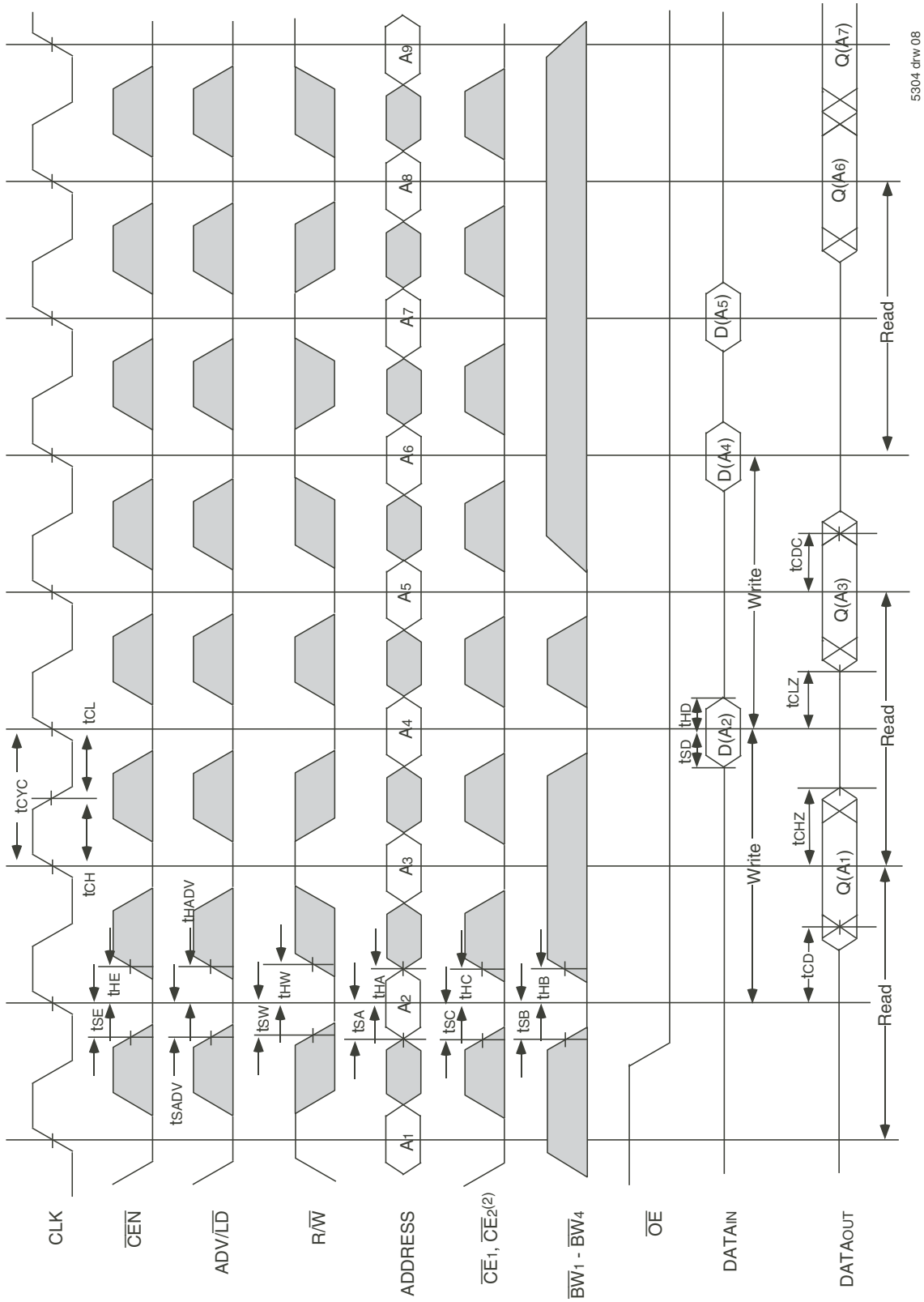
Timing Waveform of Write Cycles(1,2,3,4,5)



NOTES:

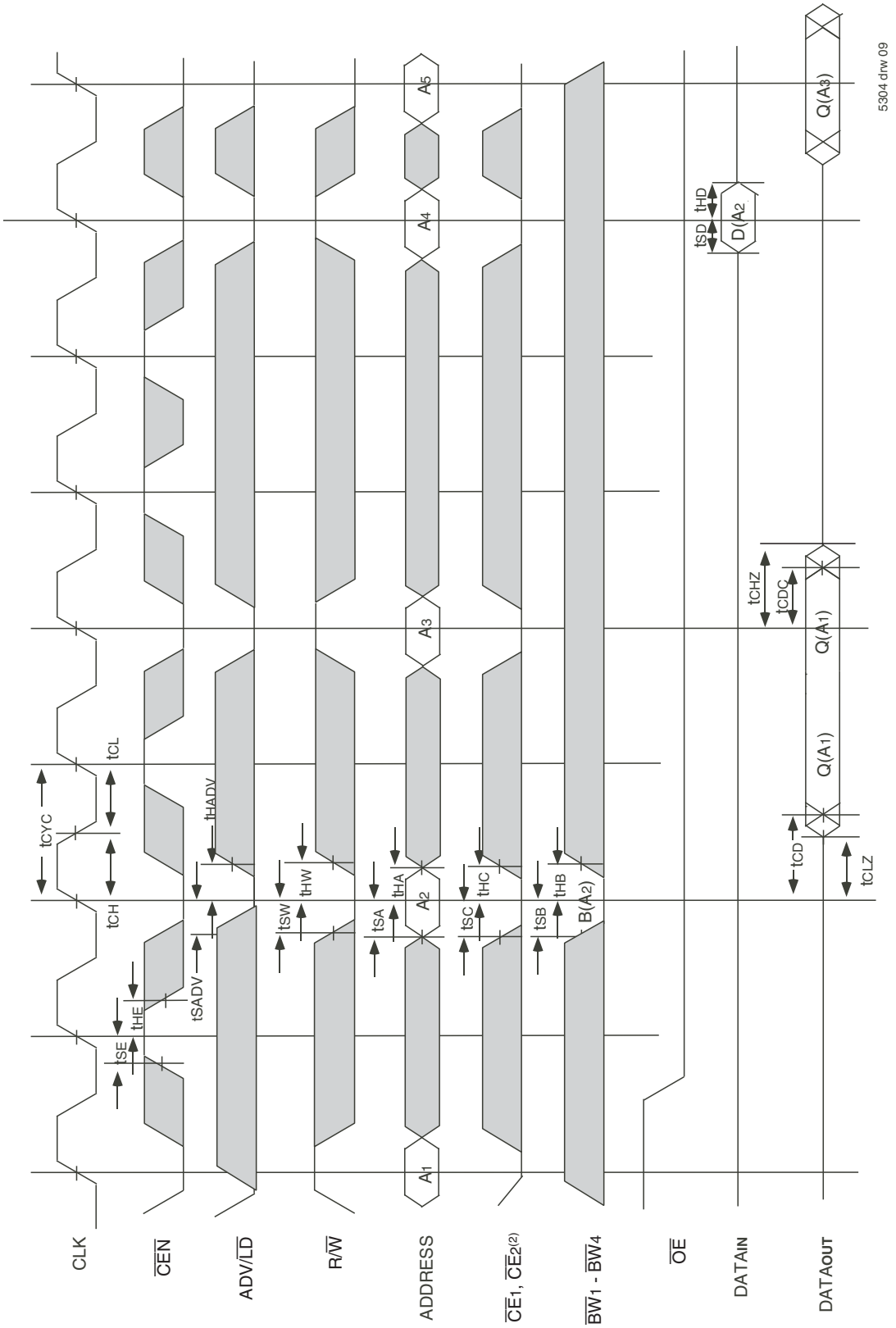
1. D (A1) represents the first input to the external address A1. D (A2) represents the first input to the external address A2; D (A2+1) represents the next input data in the burst sequence of the base address A2, etc. where address bits A0 and A1 are advancing for the four word burst in the sequence defined by the state of the $\overline{LBO}$ input.
2. CE2 timing transitions are identical but inverted to the $\overline{CE}_1$ and $\overline{CE}_2$ signals. For example, when $\overline{CE}_1$ and $\overline{CE}_2$ are LOW on this waveform, CE2 is HIGH.
3. Burst ends when new address and control are loaded into the SRAM by sampling ADV/$\overline{LD}$ LOW.
4. R/$\overline{W}$ is don't care when the SRAM is bursting (ADV/$\overline{LD}$ sampled HIGH). The nature of the burst access (Read or Write) is fixed by the state of the R/$\overline{W}$ signal when new address and control are loaded into the SRAM.
5. Individual Byte Write signals ($\overline{BW}$x) must be valid on all write and burst-write cycles. A write cycle is initiated when R/$\overline{W}$ signal is sampled LOW. The byte write information comes in two cycles before the actual data is presented to the SRAM.

Timing Waveform of Combined Read and Write Cycles(1,2,3)



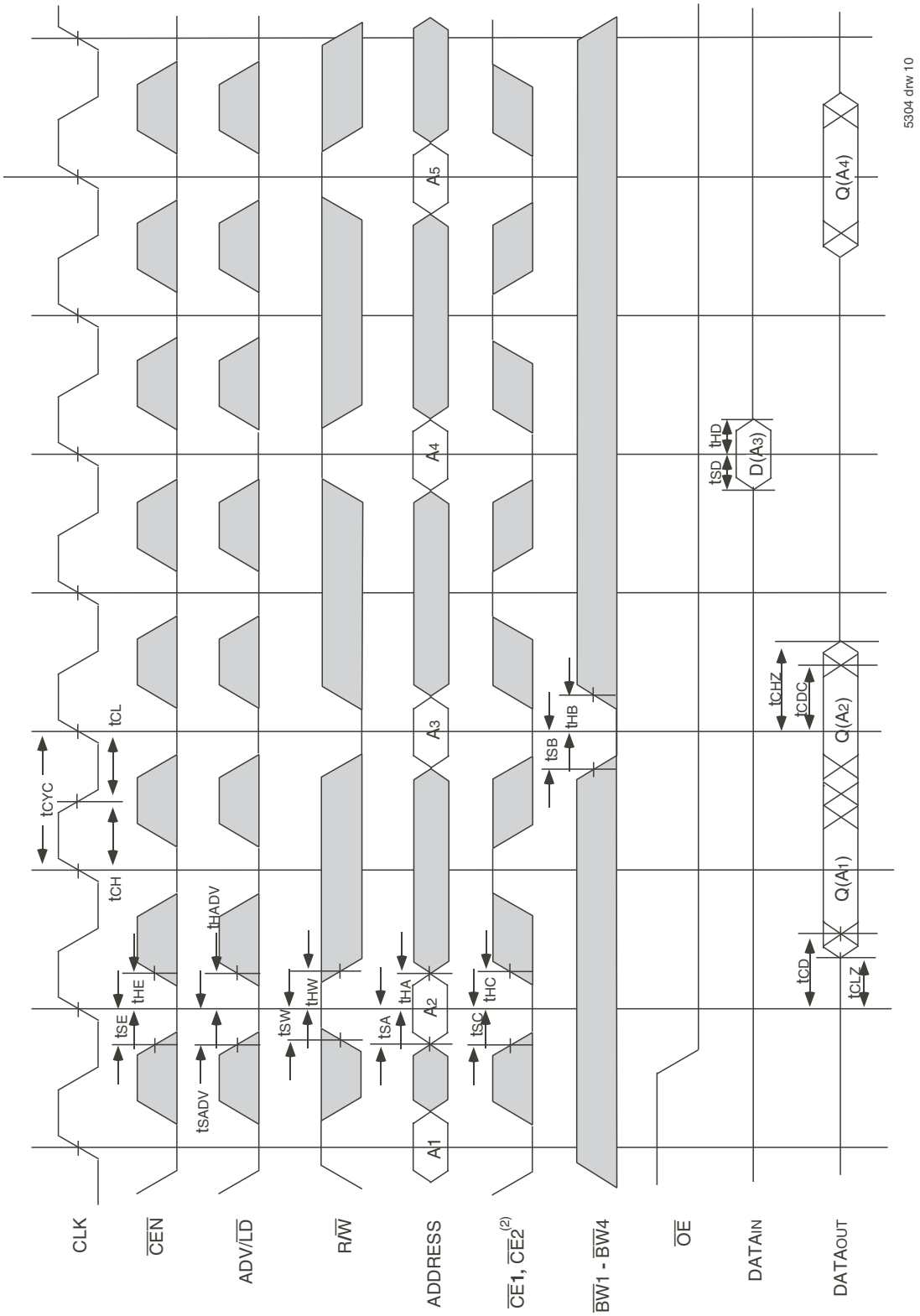
NOTES:
1. Q (A1) represents the first output from the external address A1. D (A2) represents the input data to the SRAM corresponding to address A2.
2. CE2 timing transitions are identical but inverted to the $\overline{CE}_1$ and $\overline{CE}_2$ signals. For example, when $\overline{CE}_1$ and $\overline{CE}_2$ are LOW on this waveform, CE2 is HIGH.
3. Individual Byte Write signals ($\overline{BW}x$) must be valid on all write and burst-write cycles. A write cycle is initiated when R/$\overline{W}$ signal is sampled LOW. The byte write information comes in two cycles before the actual data is presented to the SRAM.

Timing Waveform of $\overline{CEN}$ Operation(1,2,3,4)



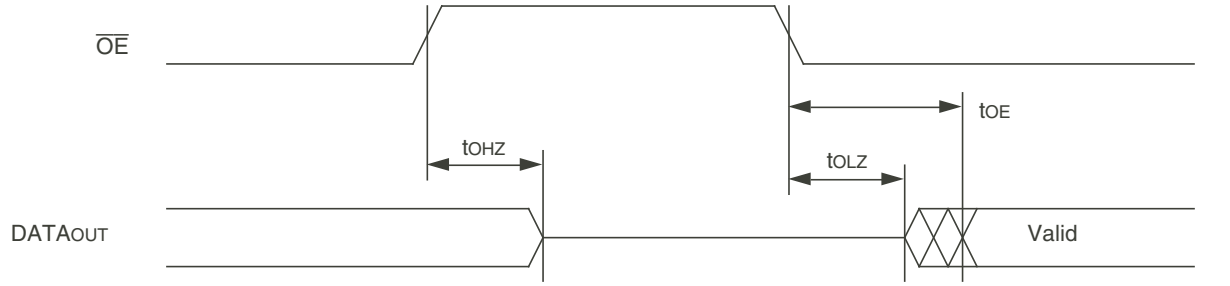
NOTES:
1. Q (A1) represents the first output from the external address A1. D (A2) represents the input data to the SRAM corresponding to address A2.
2. CE2 timing transitions are identical but inverted to the $\overline{CE}_1$ and $\overline{CE}_2$ signals. For example, when $\overline{CE}_1$ and $\overline{CE}_2$ are LOW on this waveform, CE2 is HIGH.
3. $\overline{CEN}$ when sampled high on the rising edge of clock will block that L-H transition of the clock from propagating into the SRAM. The part will behave as if the L-H clock transition did not occur. All internal registers in the SRAM will retain their previous state.
4. Individual Byte Write signals ($\overline{BW}$x) must be valid on all write and burst-write cycles. A write cycle is initiated when R/$\overline{W}$ signal is sampled LOW. The byte write information comes in two cycles before the actual data is presented to the SRAM.

Timing Waveform of $\overline{CS}$ Operation(1,2,3,4)



NOTES:
1. Q (A1) represents the first output from the external address A1. D (A3) represents the input data to the SRAM corresponding to address A3.
2. CE2 timing transitions are identical but inverted to the $\overline{CE}_1$ and $\overline{CE}_2$ signals. For example, when $\overline{CE}_1$ and $\overline{CE}_2$ are LOW on this waveform, CE2 is HIGH.
3. $\overline{CEN}$ when sampled high on the rising edge of clock will block that L-H transition of the clock from propagating into the SRAM. The part will behave as if the L-H clock transition did not occur. All internal registers in the SRAM will retain their previous state.
4. Individual Byte Write signals ($\overline{BW}x$) must be valid on all write and burst-write cycles. A write cycle is initiated when R/$\overline{W}$ signal is sampled LOW. The byte write information comes in two cycles before the actual data is presented to the SRAM.

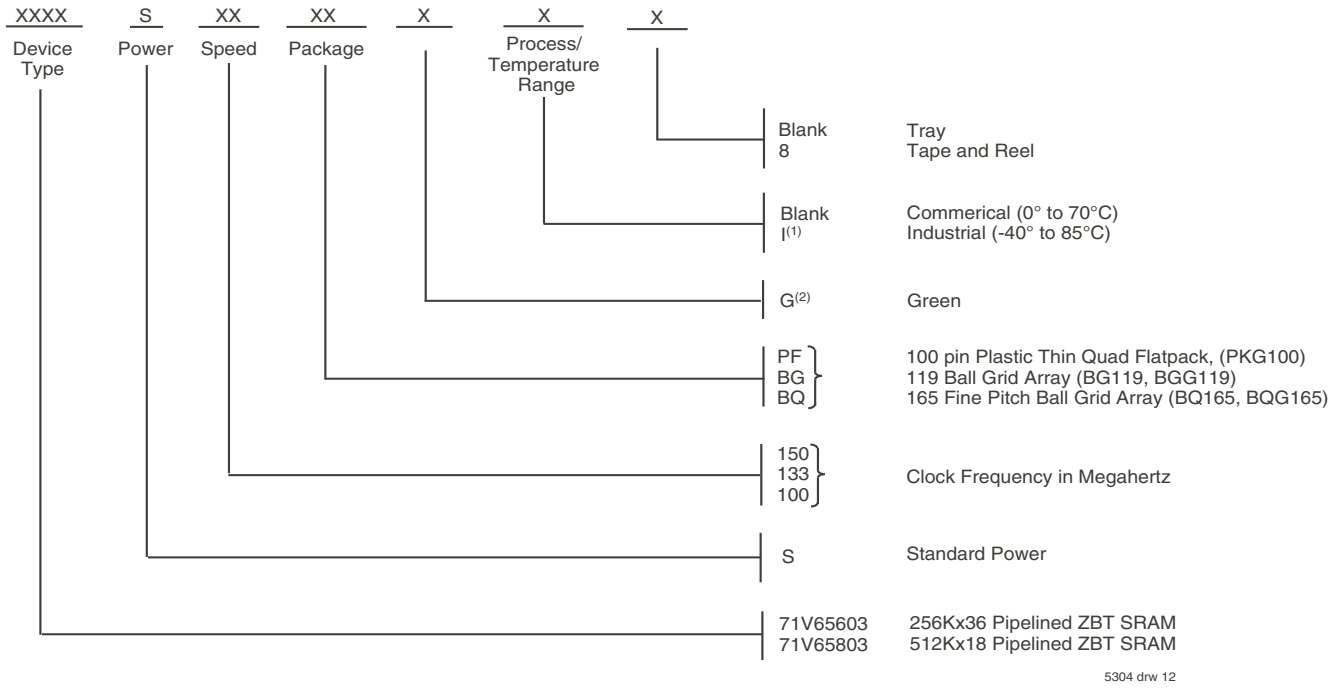
Timing Waveform of $\overline{OE}$ Operation(1)



5304 drw 11

NOTE:
1. A read operation is assumed to be in progress.

Ordering Information



5304 drw 12

NOTES:
1. Contact your local sales office for Industrial temp range for other speeds, packages and powers.
2. Green parts available. For specific speeds, packages and powers contact your local sales office.

Orderable Part Information

Speed (MHz)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
100	71V65603S100BG	BG119	PBGA	C
	71V65603S100BG8	BG119	PBGA	C
	71V65603S100BGI	BG119	PBGA	I
	71V65603S100BGI8	BG119	PBGA	I
	71V65603S100BQ	BQ165	CABGA	C
	71V65603S100BQG	BQG165	CABGA	C
	71V65603S100BQG8	BQG165	CABGA	C
	71V65603S100BQGI	BQG165	CABGA	I
	71V65603S100BQGI8	BQG165	CABGA	I
	71V65603S100BQI	BQ165	CABGA	I
	71V65603S100PFG	PKG100	TQFP	C
	71V65603S100PFG8	PKG100	TQFP	C
	71V65603S100PFGI	PKG100	TQFP	I
	71V65603S100PFGI8	PKG100	TQFP	I
133	71V65603S133BG	BG119	PBGA	C
	71V65603S133BG8	BG119	PBGA	C
	71V65603S133BGG	BGG119	PBGA	C
	71V65603S133BGG8	BGG119	PBGA	C
	71V65603S133BGGI	BGG119	PBGA	I
	71V65603S133BGGI8	BGG119	PBGA	I
	71V65603S133BGI	BG119	PBGA	I
	71V65603S133BGI8	BG119	PBGA	I
	71V65603S133BQ	BQ165	CABGA	C
	71V65603S133BQG	BQG165	CABGA	C
	71V65603S133BQG8	BQG165	CABGA	C
	71V65603S133BQGI	BQG165	CABGA	I
	71V65603S133BQGI8	BQG165	CABGA	I
	71V65603S133BQI	BQ165	CABGA	I
	71V65603S133PFG	PKG100	TQFP	C
	71V65603S133PFG8	PKG100	TQFP	C
	71V65603S133PFGI	PKG100	TQFP	I
	71V65603S133PFGI8	PKG100	TQFP	I

Speed (MHz)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
150	71V65603S150BG	BG119	PBGA	C
	71V65603S150BG8	BG119	PBGA	C
	71V65603S150BGG	BGG119	PBGA	C
	71V65603S150BGG8	BGG119	PBGA	C
	71V65603S150BGGI	BGG119	PBGA	I
	71V65603S150BGGI8	BGG119	PBGA	I
	71V65603S150BQ	BQ165	CABGA	C
	71V65603S150BQ8	BQ165	CABGA	C
	71V65603S150BQG	BQG165	CABGA	C
	71V65603S150BQG8	BQG165	CABGA	C
	71V65603S150BQGI	BQG165	CABGA	I
	71V65603S150BQGI8	BQG165	CABGA	I
	71V65603S150BQI	BQ165	CABGA	I
	71V65603S150BQI8	BQ165	CABGA	I
	71V65603S150PFG	PKG100	TQFP	C
	71V65603S150PFG8	PKG100	TQFP	C
	71V65603S150PFGI	PKG100	TQFP	I
	71V65603S150PFGI8	PKG100	TQFP	I

Orderable Part Information(con't)

Speed (MHz)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
100	71V65803S100BG	BG119	PBGA	C
	71V65803S100BG8	BG119	PBGA	C
	71V65803S100BGG	BGG119	PBGA	C
	71V65803S100BGG8	BGG119	PBGA	C
	71V65803S100BGGI	BGG119	PBGA	I
	71V65803S100BGGI8	BGG119	PBGA	I
	71V65803S100BGI	BG119	PBGA	I
	71V65803S100BGI8	BG119	PBGA	I
	71V65803S100BQ	BQ165	CABGA	C
	71V65803S100BQG	BQG165	CABGA	C
	71V65803S100BQG8	BQG165	CABGA	C
	71V65803S100BQI	BQ165	CABGA	I
	71V65803S100PFG	PKG100	TQFP	C
	71V65803S100PFG8	PKG100	TQFP	C
	71V65803S100PFGI	PKG100	TQFP	I
	71V65803S100PFGI8	PKG100	TQFP	I
133	71V65803S133BG	BG119	PBGA	C
	71V65803S133BG8	BG119	PBGA	C
	71V65803S133BGG	BGG119	PBGA	C
	71V65803S133BGG8	BGG119	PBGA	C
	71V65803S133BGGI	BGG119	PBGA	I
	71V65803S133BGGI8	BGG119	PBGA	I
	71V65803S133BGI	BG119	PBGA	I
	71V65803S133BGI8	BG119	PBGA	I
	71V65803S133BQ	BQ165	CABGA	C
	71V65803S133BQG	BQG165	CABGA	C
	71V65803S133BQG8	BQG165	CABGA	C
	71V65803S133BQI	BQ165	CABGA	I
	71V65803S133BQI8	BQ165	CABGA	I
	71V65803S133PFG	PKG100	TQFP	C
	71V65803S133PFG8	PKG100	TQFP	C
	71V65803S133PFGI	PKG100	TQFP	I
	71V65803S133PFGI8	PKG100	TQFP	I

Speed (MHz)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
150	71V65803S150BG	BG119	PBGA	C
	71V65803S150BG8	BG119	PBGA	C
	71V65803S150BGI	BG119	PBGA	I
	71V65803S150BGI8	BG119	PBGA	I
	71V65803S150BQ	BQ165	CABGA	C
	71V65803S150BQG	BQG165	CABGA	C
	71V65803S150BQG8	BQG165	CABGA	C
	71V65803S150BQI	BQ165	CABGA	I
	71V65803S150BQI8	BQ165	CABGA	I
	71V65803S150PFG	PKG100	TQFP	C
	71V65803S150PFG8	PKG100	TQFP	C
	71V65803S150PFGI	PKG100	TQFP	I
	71V65803S150PFGI8	PKG100	TQFP	I

Datasheet Document History

12/31/99		Created new datasheet from obsolete devices IDT71V656 and IDT71V658
03/04/00	Pg. 1,14,15	Removed 166MHz speed grade offering; Added 150MHz speed grade offering
04/20/00	Pg. 5,6	Added JTAG test pins to TQFP pin configuration; removed footnote
	Pg. 5,6	Add clarification note to Recommended Operating temperature and Absolute Max Ratings tables
	Pg. 7	Add note to BGA pin Configuration; correct typo within pinout
	Pg. 21	Insert TQFP Package Diagram Outline
05/23/00		Add new package offering, 13 x 15mm 165 fBGA
	Pg. 23	Correction in BG 119 Package Diagram Outline
07/28/00		Add industrial temperature
	Pg. 2	Correction V_{DDQ} 3.3V I/O supply
	Pg. 5-8	Remove JTAG offerings, refer to IDT71V656xx and IDT71V658xx device errata sheet
	Pg. 7	Correct pin B2
	Pg. 8	Change pin B1 to NC
	Pg. 23	Update BG119 Package Diagram Outline
11/04/00	Pg. 8	Add note to pin N5 on BQ165 pinout, reserved for JTAG $\overline{TRST}$
	Pg. 15	Add Izz parameter to DC Electrical Characteristics
10/16/01	Pg. 16	Changed sub-header to include Commercial and Industrial Temperature Ranges. Corrected the TCH from 22ns to 2.2ns and TSADV from 20ns to 2.0ns.
12/04/02	Pg. 1-25	Changed datasheet from Preliminary to final release.
	Pg. 15	Added I temp to 150MHz.
	Pg. 16	Corrected typo from 22 to 2.2.
12/19/02	Pg. 1,2,5,6, 7,8	Removed JTAG functionality for current die revision.
	Pg. 7	Corrected pin configuration on the x36, 119BGA. Switched pins I/O0 and I/OP1.
09/30/04	Pg. 5,6	Updated temperature T_A note.
	Pg. 7	Updated pin configuration for the 119BGA-reordered I/O signals on P7,N6,L6, K7,H6, G7, F6, E7, D6 (512K x18).
	Pg. 25	Added "restricted hazardous substance device" to ordering information.
02/21/07	Pg. 25	Added Z generation die step to data sheet ordering information.
10/16/08	Pg. 25	Updated the ordering information by removing the "IDT" notation.
11/12/21	Pg. 1 - 27	Source file updated to reflect previous Corporate Marketing rebranding
	Pg. 1 & 23	Removed Z stepping information
	Pg. 1 & 23	Updated Industrial temp range, green availability and package codes
	Pg. 23	Added Tape & Reel and green to ordering information
	Pg. 5 - 8	Updated package codes
	Pg. 22 - 24	Deleted all Package Diagram Outlines
	Pg. 24 - 25	Added Orderable Part Information tables

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