RX71M Group
Renesas MCUs

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240-MHz 32-bit RX MCU, on-chip FPU, 480 DMIPS, up to 4-MB flash memory, 512-KB SRAM, various communications interfaces including IEEE 1588-compliant Ethernet MAC, high-speed USB 2.0 with battery charging, SD host interface (optional), quad SPI, and CAN, 12-bit A/D converter, RTC, encryption (optional), serial interface for audio, CMOS camera interface

Features

■ 32-bit RXv2 CPU core
- Max. operating frequency: 240 MHz
  Capable of 480 DMIPS in operation at 240 MHz
- Single precision 32-bit IEEE-754 floating point
- Two types of multiply-and-accumulation unit (between memories and between registers)
- 32-bit multiplier (fastest instruction execution takes one CPU clock cycle)
- Divider (fastest instruction execution takes two CPU clock cycles)
- Fast interrupt
- CISC Harvard architecture with 5-stage pipeline
- Variable-length instructions: Ultra-compact code
- Supports the memory protection unit (MPU)
- JTAG and FINE (one-line) debugging interfaces

■ Low-power design and architecture
- Single voltage supply: 2.7 to 3.6 V
- Low power consumption: A product that supports all peripheral functions draws only 0.2mA/MHz (Typ.).
- RTC is capable of operation from a dedicated power supply.
- Four low-power modes

■ On-chip code flash memory
- Up to 4 Mbyte
- No wait states at up to 120 MHz or when the AFU is hit, one wait state at above 120 MHz and when the AFU is missed
- User code is programmable by on-board or off-board programming.
- Background programming/erasing (BGO:Background operation)

■ On-chip data flash memory
- 64 Kbytes, reprogrammable up to 100,000 times
- Background programming/erasing (BGO:Background operation)

■ On-chip SRAM
- 512 Kbytes of SRAM (no wait states except in the 256 Kbytes from 0004 0000h to 0007 FFFFh when ICLK is set to 120 MHz or faster)
- 32 Kbytes of RAM with ECC (single-error correction and double error detection)
- 8 Kbytes of standby RAM (backup on deep software standby)

■ Data transfer
- DMAC: 8 channels
- DTC
- EXDMAC: 2 channels
- DMAC for the Ethernet controller: 3 channels for 176- and 177-pin products; 2 channels for 100-, 144-, and 145-pin products

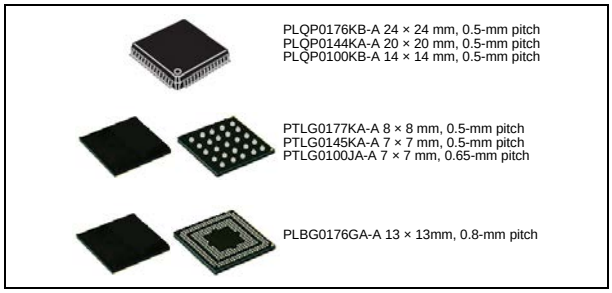
■ Reset and supply management
- Power-on reset (POR)
- Low voltage detection (LVD) with voltage settings

■ Clock functions
- External crystal resonator or internal PLL for operation at 8 to 24 MHz
- Internal 240-kHz LOCO and HOCO selectable from 16, 18, and 20 MHz
- 120-kHz clock for the IWDTa

■ Real-time clock
- Adjustment functions (30 seconds, leap year, and error)
- Real-time clock counting and binary counting modes are selectable
- Time capture function
  (for capturing times in response to event-signal input)

■ Independent watchdog timer
- 120-kHz (1/2 LOCO frequency) clock operation

■ Useful functions for IEC60730 compliance
- Oscillation-stoppage detection, frequency measurement, CRC, IWDTa, self-diagnostic function for the A/D converter, etc.
- Register write protection function can protect values in important registers against overwriting.



■ Various communications interfaces
- IEEE 1588-compliant Ethernet MAC
  (for 176- and 177-pin products: 2 modules)
- PHY layer for host/function or OTG controller (1) with high-speed USB 2.0 with battery charging transfer (only for 176- and 177-pin products)
- PHY layer (1) for host/function or OTG controller (1) with full-speed USB 2.0 transfer
- CAN (compliant with ISO11898-1), incorporating 32 mailboxes (up to 3 modules)
- SCIg and SCIh with multiple functionalities (up to 9)
  Choose from among asynchronous mode, clock-synchronous mode, smart-card interface mode, simplified SPI, simplified I^2C, and extended serial mode.
- SCIFA with 16-byte transmission and reception FIFOs (up to 4 interfaces)
- I^2C bus interface for transfer at up to 1 Mbps (up to 2 interfaces)
- Four-wire QSPI (1 interface) in addition to RSPIa (2 interfaces)
- Parallel data capture unit (PDC) for the CMOS camera interface (not in 100-pin products)
- SD host interface (optional: 1 interface) with a 1- or 4-bit SD bus for use with SD memory or SDIO
- MMCIF with 1-, 4-, or 8-bit transfer bus width

■ External address space
- Buses for full-speed data transfer (max. operating frequency of 60 MHz)
- 8 CS areas
- 8-, 16-, or 32-bit bus space is selectable per area
- Independent SDRAM area (128 Mbytes)

■ Up to 29 extended-function timers
- 16-bit TPUa, MTU3a, and GPTA: input capture, output compare, PWM waveform output
- 8-bit TMRa (4 channels), 16-bit CMT (4 channels), 32-bit CMTW (2 channels)

■ 12-bit A/D converter
- Two 12-bit units (8 channels for unit 0; 21 channels for unit 1)
- Self diagnosis
- Detection of analog input disconnection

■ 12-bit D/A converter: 2 channels
- On-chip operational amplifier output or direct input selectable

■ Temperature sensor for measuring temperature within the chip

■ Encryption (optional)
- AES (key lengths: 128, 192, and 256 bits)
- DES (key lengths: 56 bits (DES); 3 × 56 bits (T-DES))
- SHA (SHA-1 (128), SHA-2 (224 or 256), HMAC (160, 224, or 256))

■ Up to 127 pins for general I/O ports
- 5-V tolerance, open drain, input pull-up, switchable driving ability

■ Operating temp. range
- D-version: –40°C to +85°C
- G-version: –40°C to +105°C

1. Overview

1.1 Outline of Specifications

Table 1.1 lists the specifications in outline, and Table 1.2 gives a comparison of the functions of products in different packages.
Table 1.1 shows the outline of maximum specifications, and the number of peripheral module channels differs depending on the pin number on the package and the code flash memory capacity. For details, see Table 1.2, Comparison of Functions for Different Packages.

Table 1.1 Outline of Specifications (1/9)

Classification	Module/Function	Description
CPU	CPU	• Maximum operating frequency: 240 MHz • 32-bit RX CPU (RXv2) • Minimum instruction execution time: One instruction per state (cycle of the system clock) • Address space: 4-Gbyte linear • Register set of the CPU General purpose: Sixteen 32-bit registers Control: Ten 32-bit registers Accumulator: Two 72-bit registers • Basic instructions: 75 • Floating-point instructions: 11 • DSP instructions: 23 • Addressing modes: 11 • Data arrangement Instructions: Little endian Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits
	FPU	• Single precision (32-bit) floating point • Data types and floating-point exceptions in conformance with the IEEE754 standard
Memory	Code flash memory	• Capacity: 2 Mbytes, 2.5 Mbytes, 3 Mbytes, 4 Mbytes • No-wait access at up to 120 MHz, single wait access at frequencies above 120 MHz • No-wait access to instructions and operands when the AFU is hit in operation at 240 MHz • On-board programming: Four types • Off-board programming (parallel programmer mode) • The trusted memory (TM) function protects against the reading of programs from blocks 8 and 9.
	Data flash memory	• Capacity: 64 Kbytes • Programming/erasing: 100,000 times
	RAM	• Capacity: 512 Kbytes • 0000 0000h to 0003 FFFFh (256 Kbytes): 240 MHz No-wait access 0004 0000h to 0007 FFFFh (256 Kbytes): No-wait access at up to 120 MHz, single wait access at frequencies above 120 MHz • SED (single error detection)
	Unique ID	• 12-byte length ID unique to the device
	RAM with ECC (ECCRAM)	• Capacity: 32 Kbytes • Single wait access at up to 120 MHz, two wait accesses for reading and three wait accesses for writing at frequencies above 120 MHz • SEC-DED (single error correction/double error detection)
	Standby RAM	• Capacity: 8 Kbytes • Operation synchronized with PCLKB: Up to 60 MHz, two-cycle access

Table 1.1 Outline of Specifications (2/9)

Classification	Module/Function	Description
Operating modes		• Operating modes by the mode-setting pins at the time of release from the reset state Single-chip mode Boot mode (for the SCI interface) Boot mode (for the USB interface) User boot mode • Selection of operating mode by register setting Single-chip mode, user boot mode On-chip ROM disabled extended mode On-chip ROM enabled extended mode • Endian selectable
Clock	Clock generation circuit	• Main clock oscillator, sub clock oscillator, low-speed/high-speed on-chip oscillator, PLL frequency synthesizer, and IWDT-dedicated on-chip oscillator • The peripheral module clocks can be set to frequencies above that of the system clock. • Main-clock oscillation stoppage detection • Separate frequency-division and multiplication settings for the system clock (ICLK), peripheral module clocks (PCLKA, PCLKB, PCLKC, PCLKD), flash-IF clock (FCLK) and external bus clock (BCLK) The CPU and other bus masters run in synchronization with the system clock (ICLK): Up to 240 MHz Peripheral modules of MTU3, GPT, RSPI, SCIFA, USBA, ETHERC, EPTPC, EDMAC, and AES run in synchronization with PCLKA, which operates at up to 120 MHz. Other peripheral modules run in synchronization with PCLKB: Up to 60 MHz ADCLK in the S12AD (unit 0) runs in synchronization with PCLKC: Up to 60 MHz ADCLK in the S12AD (unit 1) runs in synchronization with PCLKD: Up to 60 MHz Flash IF run in synchronization with the flash-IF clock (FCLK): Up to 60 MHz Devices connected to the external bus run in synchronization with the external bus clock (BCLK): Up to 60 MHz • Multiplication is possible with using the high-speed on-chip oscillator (HOCO) as a reference clock of the PLL circuit
Reset		Nine types of reset • RES# pin reset: Generated when the RES# pin is driven low. • Power-on reset: Generated when the RES# pin is driven high and VCC = AVCC0 = AVCC1 rises. • Voltage-monitoring 0 reset: Generated when VCC = AVCC0 = AVCC1 falls. • Voltage-monitoring 1 reset: Generated when VCC = AVCC0 = AVCC1 falls. • Voltage-monitoring 2 reset: Generated when VCC = AVCC0 = AVCC1 falls. • Deep software standby reset: Generated in response to an interrupt to trigger release from deep software standby. • Independent watchdog timer reset: Generated when the independent watchdog timer underflows, or a refresh error occurs. • Watchdog timer reset: Generated when the watchdog timer underflows, or a refresh error occurs. • Software reset: Generated by register setting.
Power-on reset		If the RES# pin is at the high level when power is supplied, an internal reset is generated. After VCC = AVCC0 = AVCC1 has exceeded the voltage detection level and the specified period has elapsed, the reset is cancelled.
Voltage detection circuit (LVDA)		Monitors the voltage being input to the VCC = AVCC0 = AVCC1 pins and generates an internal reset or internal interrupt. • Voltage detection circuit 0 Capable of generating an internal reset The option-setting memory can be used to select enabling or disabling of the reset. Voltage detection level: Selectable from three different levels (2.94 V, 2.87 V, and 2.80 V) • Voltage detection circuits 1 and 2 Voltage detection level: Selectable from three different levels (2.99 V, 2.92 V, and 2.85 V) Digital filtering (1/2, 1/4, 1/8, and 1/16 LOCO frequency) Capable of generating an internal reset • Two types of timing are selectable for release from reset An internal interrupt can be requested. • Detection of voltage rising above and falling below thresholds is selectable. • Maskable or non-maskable interrupt is selectable Voltage detection monitoring Event linking

Table 1.1 Outline of Specifications (3/9)

Classification	Module/Function	Description
Low power consumption	Low power consumption facilities	• Module stop function • Four low power consumption modes Sleep mode, all-module clock stop mode, software standby mode, and deep software standby mode
	Battery backup function	• When the voltage on the VCC pin drops, battery power from the VBATT pin is supplied to keep the real-time clock (RTC) operating.
Interrupt	Interrupt controller (ICUA)	• Peripheral function interrupts: 298 sources • External interrupts: 16 (pins IRQ0 to IRQ15) • Software interrupts: 2 sources • Non-maskable interrupts: 7 sources • Sixteen levels specifiable for the order of priority • Method of interrupt source selection: The interrupt vectors consist of 256 vectors (128 sources are fixed. The remaining 128 vectors are selected from among the other 157 sources.)
External bus extension		• The external address space can be divided into eight areas (CS0 to CS7), each with independent control of access settings. Capacity of each area: 16 Mbytes (CS0 to CS7) A chip-select signal (CS0# to CS7#) can be output for each area. Each area is specifiable as an 8-, 16-, or 32-bit bus space. The data arrangement in each area is selectable as little or big endian (only for data). • SDRAM interface connectable • Bus format: Separate bus, multiplex bus • Wait control • Write buffer facility
DMA	DMA controller (DMACAa)	• 8 channels • Three transfer modes: Normal transfer, repeat transfer, and block transfer • Request sources: Software trigger, external interrupts, and interrupt requests from peripheral functions
	EXDMA controller (EXDMACa)	• 2 channels Four transfer modes: Normal transfer, repeat transfer, block transfer, and cluster transfer • Single-address transfer enabled with the EDACKn signal • Request sources: Software trigger, external DMA requests (EDREQn), and interrupt requests from peripheral functions
	Data transfer controller (DTCa)	• Three transfer modes: Normal transfer, repeat transfer, and block transfer • Request sources: External interrupts and interrupt requests from peripheral functions
I/O ports	Programmable I/O ports	• I/O ports for the 177-pin TFLGA, 176-pin LFBGA, and 176-pin LFQFP I/O pins: 127 Input pin: 1 Pull-up resistors: 127 Open-drain outputs: 127 5-V tolerance: 19 • I/O ports for the 145-pin TFLGA and 144-pin LFQFP I/O pins: 111 Input pin: 1 Pull-up resistors: 111 Open-drain outputs: 111 5-V tolerance: 18 • I/O ports for the 100-pin TFLGA and 100-pin LFQFP I/O pins: 78 Input pin: 1 Pull-up resistors: 78 Open-drain outputs: 78 5-V tolerance: 17

Table 1.1 Outline of Specifications (4/9)

Classification	Module/Function	Description
Event link controller (ELC)		• Event signals such as interrupt request signals can be interlinked with the operation of functions such as timer counting, eliminating the need for intervention by the CPU to control the functions. • 119 internal event signals can be freely combined for interlinked operation with connected functions. • Event signals from peripheral modules can be used to change the states of output pins (of ports B and E). • Changes in the states of pins (of ports B and E) being used as inputs can be interlinked with the operation of peripheral modules.
Timers	16-bit timer pulse unit (TPUa)	• (16 bits × 6 channels) × 1 unit • Maximum of 16 pulse-input/output possible • Select from among seven or eight counter-input clock signals for each channel • Input capture/output compare function • Output of PWM waveforms in up to 15 phases in PWM mode • Support for buffered operation, phase-counting mode (two phase encoder input) and cascade-connected operation (32 bits × 2 channels) depending on the channel. • PPG output trigger can be generated • Capable of generating conversion start triggers for the A/D converters • Digital filtering of signals from the input capture pins • Event linking by the ELC
	Multifunction timer pulse unit (MTU3a)	• 9 channels (16 bits × 8 channels, 32 bits × 1 channel) • Maximum of 28 pulse-input/output and 3 pulse-input possible • Select from among 14 counter-input clock signals for each channel (PCLKA/1, PCLKA/2, PCLKA/4, PCLKA/8, PCLKA/16, PCLKA/32, PCLKA/64, PCLKA/256, PCLKA/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD, MTIOC1A) 14 of the signals are available for channel 0, 12 are available for channel 2, 11 are available for channels 1, 3, 4, 6 to 8, and 10 are available for channel 5. • Input capture function • 39 output compare/input capture registers • Counter clear operation (synchronous clearing by compare match/input capture) • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous register input/output by synchronous counter operation • Buffered operation • Support for cascade-connected operation • 43 interrupt sources • Automatic transfer of register data • Pulse output mode Toggle/PWM/complementary PWM/reset-synchronized PWM • Complementary PWM output mode Outputs non-overlapping waveforms for controlling 3-phase inverters Automatic specification of dead times PWM duty cycle: Selectable as any value from 0% to 100% Delay can be applied to requests for A/D conversion. Non-generation of interrupt requests at peak or trough values of counters can be selected. Double buffer configuration • Reset synchronous PWM mode Three phases of positive and negative PWM waveforms can be output with desired duty cycles. • Phase-counting mode: 16-bit mode (channels 1 and 2); 32-bit mode (channels 1 and 2) • Counter functionality for dead-time compensation • Generation of triggers for A/D converter conversion • A/D converter start triggers can be skipped • Digital filter function for signals on the input capture and external counter clock pins • PPG output trigger can be generated • Event linking by the ELC
	Port output enable 3 (POE3a)	• Control of the high-impedance state of the MTU3/GPT's waveform output pins • 5 pins for input from signal sources: POE0, POE4, POE8, POE10, POE11 • Initiation on detection of short-circuited outputs (detection of simultaneous PWM output to the active level) • Initiation by oscillation-stoppage detection or software • The conditions for control can be set for the target pins subject to output control.

Table 1.1 Outline of Specifications (5/9)

Classification	Module/Function	Description
Timers	General PWM timer (GPTA)	• 16 bits × 4 channels • Counting up or down (saw-wave), counting up and down (triangle-wave) selectable for all channels • Four clock sources independently selectable for all channels (PCLKA/1, PCLKA/4, PCLKA/8, PCLKA/16) • 2 input/output pins per channel • 2 output compare/input capture registers per channel • For the 2 output compare/input capture registers of each channel, 4 registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use. • In output compare operation, buffer switching can be at peaks or troughs, enabling the generation of laterally asymmetrically PWM waveforms. • Registers for setting up frame intervals on each channel (with capability for generating interrupts on overflow or underflow) • Synchronizable operation of the several counters • Modes of synchronized operation (synchronized, or displaced by desired times for phase shifting) • Generation of dead times in PWM operation • Through combination of three counters, generation of automatic three-phase PWM waveforms incorporating dead times • Starting, clearing, and stopping counters in response to external or internal triggers • Internal trigger sources: output of the internal comparator detection, software, and compare-match • Digital filter function for signals on the input capture and external trigger pins • Event linking by the ELC
	Programmable pulse generator (PPG)	• (4 bits × 4 groups) × 2 units • Pulse output with the MTU or TPU output as a trigger • Maximum of 32 pulse-output possible
	8-bit timers (TMRb)	• (8 bits × 2 channels) × 2 units • Select from among seven internal clock signals (PCLKB/1, PCLKB/2, PCLKB/8, PCLKB/32, PCLKB/64, PCLKB/1024, PCLKB/8192) and one external clock signal • Capable of output of pulse trains with desired duty cycles or of PWM signals • The 2 channels of each unit can be cascaded to create a 16-bit timer • Generation of triggers for A/D converter conversion • Capable of generating the internal operating clock signals for SCI5, SCI6, or SCI12 • Event linking by the ELC
	Compare match timer (CMT)	• (16 bits × 2 channels) × 2 units • Select from among four internal clock signals (PCLKB/8, PCLKB/32, PCLKB/128, PCLKB/512) • Event linking by the ELC
	Compare match timer W (CMTW)	• (32 bits × 1 channel) × 2 units • Compare-match, input-capture input, and output-comparison output are available. • Select from among four internal clock signals (PCLKB/8, PCLKB/32, PCLKB/128, PCLKB/512) • Interrupt requests can be output in response to compare-match, input-capture, and output-comparison events. • Event linking by the ELC
	Realtime clock (RTCd)	• Clock sources: Main clock, sub clock • Selection of the 32-bit binary count in time count/second unit possible • Clock and calendar functions • Interrupt sources: Alarm interrupt, periodic interrupt, and carry interrupt • Battery backup operation • Time-capture facility for three values • Event linking by the ELC
	Watchdog timer (WDTA)	• 14 bits × 1 channel • Select from among 6 counter-input clock signals (PCLKB/4, PCLKB/64, PCLKB/128, PCLKB/512, PCLKB/2048, PCLKB/8192)

Table 1.1 Outline of Specifications (6/9)

Classification	Module/Function	Description
Timers	Independent watchdog timer (IWDTa)	• 14 bits × 1 channel • Counter-input clock: IWDT-dedicated on-chip oscillator • Dedicated clock/1, dedicated clock/16, dedicated clock/32, dedicated clock/64, dedicated clock/128, dedicated clock/256 • Window function: The positions where the window starts and ends are specifiable (the window defines the timing with which refreshing is enabled and disabled). • Event linking by the ELC
Communication function	Ethernet controller (ETHERC)	• 2 channels • Input and output of Ethernet/IEEE 802.3 frames • Transfer at 10 or 100 Mbps • Full- and half-duplex modes • MII (Media Independent Interface) or RMII (Reduced Media Independent Interface) as defined in IEEE 802.3u • Detection of Magic Packets™*1 or output of a “wake-on-LAN” signal (WOL) • Compliance with flow control as defined in IEEE 802.3x standards • Filtering of multicast frames • Direct transfer of frames between two channels by cut-through
	PTP controller for Ethernet controller (EPTPCa)	• A block compatible with the IEEE 1588 standard is connected to the Ethernet controller (ETHERC). • Matching with a time stamp can start counting by MTU3 and the GPT.
	DMA controller for Ethernet controller (EDMACa)	• 3 channels (the round-robin method determines the priority of the channels) 2 channels for ETHERC; 1 channel for EPTPC • Alleviation of CPU load by the descriptor control method • Transmission FIFO: 2 Kbytes; Reception FIFO: 4 Kbytes
	USB 2.0 FS host/ function module (USBb)	• Includes a UDC (USB Device Controller) and transceiver for USB 2.0 FS • One port • Compliance with the USB 2.0 specification • Transfer rate: Full speed (12 Mbps), low speed (1.5 Mbps) (host only) • Both self-power mode and bus power are supported • OTG (On the Go) operation is possible (low-speed is not supported) • Incorporates 2 Kbytes of RAM as a transfer buffer • External pull-up and pull-down resistors are not required
	USB 2.0 HS host/ function module with battery charging (USBAa)	• Includes a UDC (USB Device Controller) and transceiver for USB 2.0 HS • One port (only in 177-/176-pin devices) • Compliance with the USB 2.0 specification • Transfer rate: High speed (480 Mbps), full speed (12 Mbps), low speed (1.5 Mbps) (host only) • Both self-power mode and bus power are supported • OTG (On the Go) operation is possible (low-speed is not supported) • Incorporates 8.5 Kbytes of RAM as a transfer buffer • External pull-up and pull-down resistors are not required
	Serial communications interfaces (SCIg, SCIh)	• 9 channels (SCIg: 8 channels + SCIh: 1 channel) • SCIg Serial communications modes: Asynchronous, clock synchronous, and smart-card interface Multi-processor function On-chip baud rate generator allows selection of the desired bit rate Choice of LSB-first or MSB-first transfer Average transfer rate clock can be input from TMR timers for SCI5, SCI6, and SCI12 Start-bit detection: Level or edge detection is selectable. Simple I^2C Simple SPI 9-bit transfer mode Bit rate modulation Double-speed mode Event linking by the ELC (supported by SCI5 only) • SCIh (The following functions are added to SCIg) Supports the serial communications protocol, which contains the start frame and information frame Supports the LIN format

Table 1.1 Outline of Specifications (7/9)

Classification	Module/Function	Description
Communication function	Serial communications interface with FIFO (SCIFA)	• 4 channels • Methods of transfer: Asynchronous and clock synchronous • Desired bit rates can be selected from the internal baud rate generators. • LSB or MSB first is selectable. • Both the transmission and reception sections are equipped with 16-byte FIFO buffers, allowing continuous transmission and reception. • Bit rate modulation • Double-speed mode
	I^2C bus interface (RIICa)	• 2 channels (only channel 0 can be used in fast-mode plus) Communication formats I^2C bus format/SMBus format Supports the multi-master Max. transfer rate: 1 Mbps (channel 0) • Event linking by the ELC
	CAN module (CAN)	• 3 channels • Compliance with the ISO11898-1 specification (standard frame and extended frame) • 32 mailboxes per channel
	Serial peripheral interface (RSPIa)	• 2 channels • RSPI transfer facility Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPCK (RSPI clock) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) Capable of handling serial transfer as a master or slave • Data formats Switching between MSB first and LSB first The number of bits in each transfer can be changed to any number of bits from 8 to 16, or to 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) • Buffered structure Double buffers for both transmission and reception • RSPCK can be stopped with the receive buffer full for master reception. • Event linking by the ELC
	Quad serial peripheral interface (QSPI)	• 1 channel • Connectable with serial flash memory equipped with multiple input and output lines (i.e. for single, dual, or quad operation) • Selectable bit length, polarity, and phase of the clock signal • Sequential execution of transfer • LSB or MSB first is selectable.
Serial sound interface (SSI)		• 2 channels • Full-duplex transfer is possible (only on channel 0). • Support for multiple audio formats • Support for master or slave operation • Bit clock frequency is selectable from four different types (16 fs, 32 fs, 48 fs, and 64 fs). • Support for 8-/16-/18-/20-/22-/24 bit data formats • Internal 8-stage FIFO for transmission and reception • Stopping SSIWS when data transfer is stopped is selectable.
Sampling rate converter (SRC)		• 1 channel • Data formats: 32-bit stereo (16 bits for the left, 16 bits for the right) and 16-bit monaural. • Input sampling rates: 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48 kHz • Output sampling rates: 32, 44.1, 48, 8*2 or 16 kHz*2
SD host interface (SDHI)*4		• 1 channel • Transfer speed: Supports high-speed mode (15 MB/s) and default speed mode (10 MB/s) • One interface for SD memory and I/O cards (supporting 1- and 4-bit SD buses) • SD specifications Part 1: Physical Layer Specification Ver. 3.01 compliant (DDR not supported) Part E1: SDIO Specification Ver. 3.00 • Error checking: CRC7 for commands and CRC16 for data • Interrupt requests: Card access interrupt, SDIO access interrupt, card detection interrupt • DMA transfer requests: SD_BUF write and SD_BUF read • Support for card detection and write protection

Table 1.1 Outline of Specifications (8/9)

Classification	Module/Function	Description
MMC host interface (MMCIF)		• 1 channel • Transfer speed: Supports high-speed mode (30 MB/s) and Backward-compatible mode (25 MB/s) • Compliant with JEDEC STANDARD JESD84-A441 (DDR is not supported) • Interface for Multimedia Cards (MMCs) • Device buses: Support for 1-, 4-, and 8-bit MMC buses • Interrupt requests: Card detection interrupt, error/timeout interrupt, normal operation interrupt • DMA transfer requests: CE_DATA write and CE_DATA read • Support for card detection, boot operation, high priority interrupt (HPI)
Parallel data capture unit (PDC)		• 1 channel • Acquisition of synchronization through external 8-bit horizontal and vertical synchronization signals • Setting of the image size when clipping of the output for a one-frame image is required
12-bit A/D converter (S12ADC)		• 12 bits × 2 units (unit 0: 8 channels; unit 1: 21 channels) • 12-bit resolution (switchable between 8, 10, and 12 bits) • Conversion time 0.48 µs per channel (for 12-bit conversion) 0.45 µs per channel (for 10-bit conversion) 0.42 µs per channel (for 8-bit conversion) • Operating mode Scan mode (single scan mode, continuous scan mode, or group scan mode) Group A priority control (only for group scan mode) • Sample-and-hold function Common sample-and-hold circuit included In addition, channel-dedicated sample-and-hold function (3ch: in unit 0 only) included • Sampling variable Sampling time can be set up for each channel. • Digital comparison Method: Comparison to detect voltages above or below thresholds and window comparison Measurement: Comparison of two results of conversion or comparison of a value in the comparison register and a result of conversion • Self-diagnostic function The self-diagnostic function internally generates three analog input voltages (unit 0: VREFL0, VREFH0 × 1/2, VREFH0; unit 1: AVSS1, AVCC1 × 1/2, AVCC1) • Double trigger mode (A/D conversion data duplicated) • Detection of analog input disconnection • Three ways to start A/D conversion Software trigger, timer (MTU3, GPT, TMR, TPU) trigger, external trigger • Event linking by the ELC
12-bit D/A converter (R12DA)		• 2 channels • 12-bit resolution • Output voltage: 0.2 V to AVCC1 – 0.2 V (amplifier output), 0 V to AVCC1 (direct output) • Output via an amplifier or direct output can be selected. • Event linking by the ELC
Temperature sensor		• 1 channel • Relative precision: ±1°C • The voltage of the temperature is converted into a digital value by the 12-bit A/D converter (unit 1).
Safety	Memory protection unit (MPU)	• Protection area: Eight areas (max.) can be specified in the range from 0000 0000h to FFFF FFFFh. • Minimum protection unit: 16 bytes • Reading from, writing to, and enabling the execution access can be specified for each area. • An address exception occurs when the detected access is not in the permitted area.
	Trusted Memory (TM) Function	• Protects against the reading of programs from blocks 8 and 9 of the code flash memory • Instruction fetching by the CPU is the only form of access to these areas when the TM function is enabled.
	Register write protection function	• Protects important registers from being overwritten for in case a program runs out of control.

Table 1.1 Outline of Specifications (9/9)

Classification	Module/Function	Description
Safety	CRC calculator (CRC)	• CRC code generation for arbitrary amounts of data in 8-bit units • Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$ • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable
	Oscillation stop detection function for the main clock	• Main clock oscillation stop detection: Available
	Clock frequency accuracy measurement circuit (CAC)	• Monitors the clock output from the main clock oscillator, sub-clock oscillator, low- and high-speed on-chip oscillators, the PLL frequency synthesizer, IWDT-dedicated on-chip oscillator, and PCLKB, and generates interrupts when the setting range is exceeded.
	Data operation circuit (DOC)	• The function to compare, add, or subtract 16-bit data
Encryption function	AESa*3	• Key lengths: 128, 192, and 256 bits • Support for CBC, ECB, CFB, OFB, CTR, and CMAC operating modes • Speed of calculations: 128-bit key length in 22 cycles 192-bit key length in 26 cycles 256-bit key length in 30 cycles • Compliant with FIPS PUB 197
	DES*3	• Key lengths: 56 bits (DES)/3 × 56 bits (T-DES) • Support for DES and triple DES • Support for ECB and CBC operating modes • Speed of calculations: 6 clock cycles in single DES mode 14 clock cycles in triple DES mode • Compliant with FIPS PUB 46-3 • Compliant with FIPS PUB 81
	SHAa*3	• Support for SHA-1 (128), SHA-2 (224 or 256), and HMAC (160, 224, or 256) • Speed of calculations: 50 clock cycles in SHA-1 mode 42 clock cycles in SHA-224 mode 42 clock cycles in SHA-256 mode • Compliant with SHA as defined in FIPS PUB 180-1 and -2 • Compliant with HMAC as defined in FIPS PUB 198
	True random number generator (RNG)*3	• Length of random numbers: 16 bits • Generation of random-number-generated interrupts after a number is generated • Random number generation time: 3.6 ms (typ)
Operating frequency		Up to 240 MHz
Power supply voltage		VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0, VCC_USBA = AVCC_USBA = 2.7 to 3.6 V, V_{BATT} = 2.0 to 3.6 V
Operating temperature		D-version: –40 to +85°C G-version: –40 to +105°C*5
Package		177-pin TFLGA (PTLG0177KA-A) 176-pin LFBGA (PLBG0176GA-A) 176-pin LFQFP (PLQP0176KB-A) 145-pin TFLGA (PTLG0145KA-A) 144-pin LFQFP (PLQP0144KA-A) 100-pin TFLGA (PTLG0100JA-A) 100-pin LFQFP (PLQP0100KB-A)
On-chip debugging system		• E1 emulator (JTAG and FINE interfaces) • E20 emulator (JTAG interface)

Note 1. Magic Packet™ is a registered trademark of Advanced Micro Devices, Inc.
Note 2. Setting is only possible when the input sampling rate 44.1 kHz is selected.
Note 3. The product part number differs according to whether or not it supports encryption.
Note 4. The product part number differs according to whether or not it includes an SDHI (SD host interface).
Note 5. Please contact us if you are using a G-version product.

Table 1.2 Comparison of Functions for Different Packages (1/2)

Functions		RX71M Group		
Package		**177 Pins, 176 Pins**	**145 Pins, 144 Pins**	**100 Pins**
External bus	External bus width	32 bits	16 bits	
	SDRAM area controller	Available		Not supported
DMA	DMA controller	Ch. 0 to 7		
	Data transfer controller	Available		
	EXDMA controller	Ch. 0 and 1		
Timers	16-bit timer pulse unit	Ch. 0 to 5		
	Multi-function timer pulse unit 3	Ch. 0 to 8		
	General-purpose PWM timer	Ch. 0 to 3		
	Port output enable 3	Available		
	Programmable pulse generator	Ch. 0 and 1		
	8-bit timers	Ch. 0 to 3		
	Compare match timer	Ch. 0 to 3		
	Compare match timer W	Ch. 0 and 1		
	Realtime clock	Available		
	Watchdog timer	Available		
	Independent watchdog timer	Available		
Communication function	Ethernet controller	Ch. 0 and 1	Ch. 0	
	PTP controller for ethernet controller	Available		
	DMAC controller for ethernet	Ch. 0 and 1 (ETHERC) Ch. 2 (EPTPC)	Ch. 0 (ETHERC) and 2 (EPTPC)	
	USB 2.0 FS host/function module	Ch. 0		
	USB 2.0 HS host/function module with battery charging	Available	Not supported	
	Serial communications interfaces (SCIg)	Ch. 0 to 7		Ch. 0 to 3, 5 and 6
	Serial communications interfaces (SCIh)	Ch. 12		
	Serial communications interfaces with FIFO	Ch. 8 to 11		Ch. 8 and 9
	I^2C bus interfaces	Ch. 0 and 2		
	Serial peripheral interface	Ch. 0 and 1		
	CAN module	Ch. 0 to 2		Ch. 0 and 1
	Quad serial peripheral interface	Ch. 0		
	Serial sound interfaces	Ch. 0 and 1		
	Sampling rate converter	Available		
	SD host interface	Ch. 0		
	MMC host interface	Ch. 0		
	Parallel data capture unit	Available		Not supported
12-bit A/D converter		AN000 to 007 (unit 0: 8 channels) AN100 to 120 (unit 1: 21 channels)		AN000 to 007 (unit 0: 8 channels) AN100 to 113 (unit 1: 14 channels)
12-bit D/A converter		Ch. 0 and 1		Ch. 1
Temperature sensor		Available		
CRC calculator		Available		
Data operation circuit		Available		
Clock frequency accuracy measurement circuit		Available		
AES		Available		

Table 1.2 Comparison of Functions for Different Packages (2/2)

Functions	RX71M Group		
Package	**177 Pins, 176 Pins**	**145 Pins, 144 Pins**	**100 Pins**
DES	Available		
SHA	Available		
RNG	Available		
Event link controller	Available		

1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part no.

Table 1.3 List of Products (1/4)

Group	Part No.	Package	Code Flash Memory Capacity	RAM Capacity	Data Flash Memory Capacity	Operating Frequency (Max.)	Encryption Module	SDHI
RX71M (D-version)	R5F571MLCDFC	PLQP0176KB-A	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MLDDFC	PLQP0176KB-A	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MLGDFC	PLQP0176KB-A	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MLHDFC	PLQP0176KB-A	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MJCDFC	PLQP0176KB-A	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MJDDFC	PLQP0176KB-A	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MJGDFC	PLQP0176KB-A	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MJHDFC	PLQP0176KB-A	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MGCDFC	PLQP0176KB-A	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MGDDFC	PLQP0176KB-A	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MGGDFC	PLQP0176KB-A	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MGHDFC	PLQP0176KB-A	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MFCDFC	PLQP0176KB-A	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MFDDFC	PLQP0176KB-A	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MFGDFC	PLQP0176KB-A	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MFHDFC	PLQP0176KB-A	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MLCDFB	PLQP0144KA-A	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MLDDFB	PLQP0144KA-A	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MLGDFB	PLQP0144KA-A	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MLHDFB	PLQP0144KA-A	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MJCDFB	PLQP0144KA-A	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MJDDFB	PLQP0144KA-A	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MJGDFB	PLQP0144KA-A	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MJHDFB	PLQP0144KA-A	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MGCDFB	PLQP0144KA-A	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MGDDFB	PLQP0144KA-A	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MGGDFB	PLQP0144KA-A	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MGHDFB	PLQP0144KA-A	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MFCDFB	PLQP0144KA-A	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MFDDFB	PLQP0144KA-A	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MFGDFB	PLQP0144KA-A	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MFHDFB	PLQP0144KA-A	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MLCDFP	PLQP0100KB-A	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MLDDFP	PLQP0100KB-A	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MLGDFP	PLQP0100KB-A	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MLHDFP	PLQP0100KB-A	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MJCDFP	PLQP0100KB-A	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MJDDFP	PLQP0100KB-A	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MJGDFP	PLQP0100KB-A	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MJHDFP	PLQP0100KB-A	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MGCDFP	PLQP0100KB-A	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MGDDFP	PLQP0100KB-A	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MGGDFP	PLQP0100KB-A	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MGHDFP	PLQP0100KB-A	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available

Table 1.3 List of Products (2/4)

Group	Part No.	Package	Code Flash Memory Capacity	RAM Capacity	Data Flash Memory Capacity	Operating Frequency (Max.)	Encryption Module	SDHI
RX71M (D-version)	R5F571MFCDFP	PLQP0100KB-A	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MFDDFP	PLQP0100KB-A	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MFGDFP	PLQP0100KB-A	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MFHDFP	PLQP0100KB-A	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MLCDBG	PLBG0176GA-A	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MLDDBG	PLBG0176GA-A	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MLGDBG	PLBG0176GA-A	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MLHDBG	PLBG0176GA-A	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MJCDBG	PLBG0176GA-A	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MJDDBG	PLBG0176GA-A	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MJGDBG	PLBG0176GA-A	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MJHDBG	PLBG0176GA-A	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MGCDBG	PLBG0176GA-A	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MGDDBG	PLBG0176GA-A	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MGGDBG	PLBG0176GA-A	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MGHDBG	PLBG0176GA-A	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MFCDBG	PLBG0176GA-A	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MFDDBG	PLBG0176GA-A	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MFGDBG	PLBG0176GA-A	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MFHDBG	PLBG0176GA-A	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MLCDLC	PTLG0177KA-A	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MLDDLC	PTLG0177KA-A	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MLGDLC	PTLG0177KA-A	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MLHDLC	PTLG0177KA-A	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MJCDLC	PTLG0177KA-A	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MJDDLC	PTLG0177KA-A	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MJGDLC	PTLG0177KA-A	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MJHDLC	PTLG0177KA-A	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MGCDLC	PTLG0177KA-A	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MGDDLC	PTLG0177KA-A	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MGGDLC	PTLG0177KA-A	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MGHDLC	PTLG0177KA-A	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MFCDLC	PTLG0177KA-A	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MFDDLC	PTLG0177KA-A	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MFGDLC	PTLG0177KA-A	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MFHDLC	PTLG0177KA-A	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MLCDLK	PTLG0145KA-A	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MLDDLK	PTLG0145KA-A	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MLGDLK	PTLG0145KA-A	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MLHDLK	PTLG0145KA-A	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MJCDLK	PTLG0145KA-A	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MJDDLK	PTLG0145KA-A	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MJGDLK	PTLG0145KA-A	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MJHDLK	PTLG0145KA-A	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MGCDLK	PTLG0145KA-A	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MGDDLK	PTLG0145KA-A	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MGGDLK	PTLG0145KA-A	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MGHDLK	PTLG0145KA-A	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available

Table 1.3 List of Products (3/4)

Group	Part No.	Package	Code Flash Memory Capacity	RAM Capacity	Data Flash Memory Capacity	Operating Frequency (Max.)	Encryption Module	SDHI
RX71M (D-version)	R5F571MFCDLK	PTLG0145KA-A	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MFDDLK	PTLG0145KA-A	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MFGDLK	PTLG0145KA-A	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MFHDLK	PTLG0145KA-A	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MLCDLJ	PTLG0100JA-A	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MLDDLJ	PTLG0100JA-A	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MLGDLJ	PTLG0100JA-A	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MLHDLJ	PTLG0100JA-A	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MJCDLJ	PTLG0100JA-A	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MJDDLJ	PTLG0100JA-A	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MJGDLJ	PTLG0100JA-A	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MJHDLJ	PTLG0100JA-A	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MGCDLJ	PTLG0100JA-A	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MGDDLJ	PTLG0100JA-A	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MGGDLJ	PTLG0100JA-A	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MGHDLJ	PTLG0100JA-A	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MFCDLJ	PTLG0100JA-A	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MFDDLJ	PTLG0100JA-A	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MFGDLJ	PTLG0100JA-A	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MFHDLJ	PTLG0100JA-A	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available

Table 1.3 List of Products (4/4)

Group	Part No.	Package	Code Flash Memory Capacity	RAM Capacity	Data Flash Memory Capacity	Operating Frequency (Max.)	Encryption Module	SDHI
RX71M (G-version)	R5F571MLCGFC	PLQP0176KB-A	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MLDGFC	PLQP0176KB-A	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MLGGFC	PLQP0176KB-A	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MLHGFC	PLQP0176KB-A	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MJCGFC	PLQP0176KB-A	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MJDGFC	PLQP0176KB-A	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MJGGFC	PLQP0176KB-A	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MJHGFC	PLQP0176KB-A	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MGCGFC	PLQP0176KB-A	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MGDGFC	PLQP0176KB-A	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MGGGFC	PLQP0176KB-A	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MGHGFC	PLQP0176KB-A	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MFCGFC	PLQP0176KB-A	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MFDGFC	PLQP0176KB-A	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MFGGFC	PLQP0176KB-A	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MFHGFC	PLQP0176KB-A	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MLCGFB	PLQP0144KA-A	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MLDGFB	PLQP0144KA-A	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MLGGFB	PLQP0144KA-A	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MLHGFB	PLQP0144KA-A	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MJCGFB	PLQP0144KA-A	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MJDGFB	PLQP0144KA-A	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MJGGFB	PLQP0144KA-A	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MJHGFB	PLQP0144KA-A	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MGCGFB	PLQP0144KA-A	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MGDGFB	PLQP0144KA-A	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MGGGFB	PLQP0144KA-A	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MGHGFB	PLQP0144KA-A	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MFCGFB	PLQP0144KA-A	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MFDGFB	PLQP0144KA-A	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MFGGFB	PLQP0144KA-A	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MFHGFB	PLQP0144KA-A	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MLCGFP	PLQP0100KB-A	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MLDGFP	PLQP0100KB-A	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MLGGFP	PLQP0100KB-A	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MLHGFP	PLQP0100KB-A	4 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MJCGFP	PLQP0100KB-A	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MJDGFP	PLQP0100KB-A	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MJGGFP	PLQP0100KB-A	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MJHGFP	PLQP0100KB-A	3 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MGCGFP	PLQP0100KB-A	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MGDGFP	PLQP0100KB-A	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MGGGFP	PLQP0100KB-A	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MGHGFP	PLQP0100KB-A	2.5 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available
	R5F571MFCGFP	PLQP0100KB-A	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Not supported
	R5F571MFDGFP	PLQP0100KB-A	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Not supported	Available
	R5F571MFGGFP	PLQP0100KB-A	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Not supported
	R5F571MFHGFP	PLQP0100KB-A	2 Mbytes	512 Kbytes	64 Kbytes	240 MHz	Available	Available

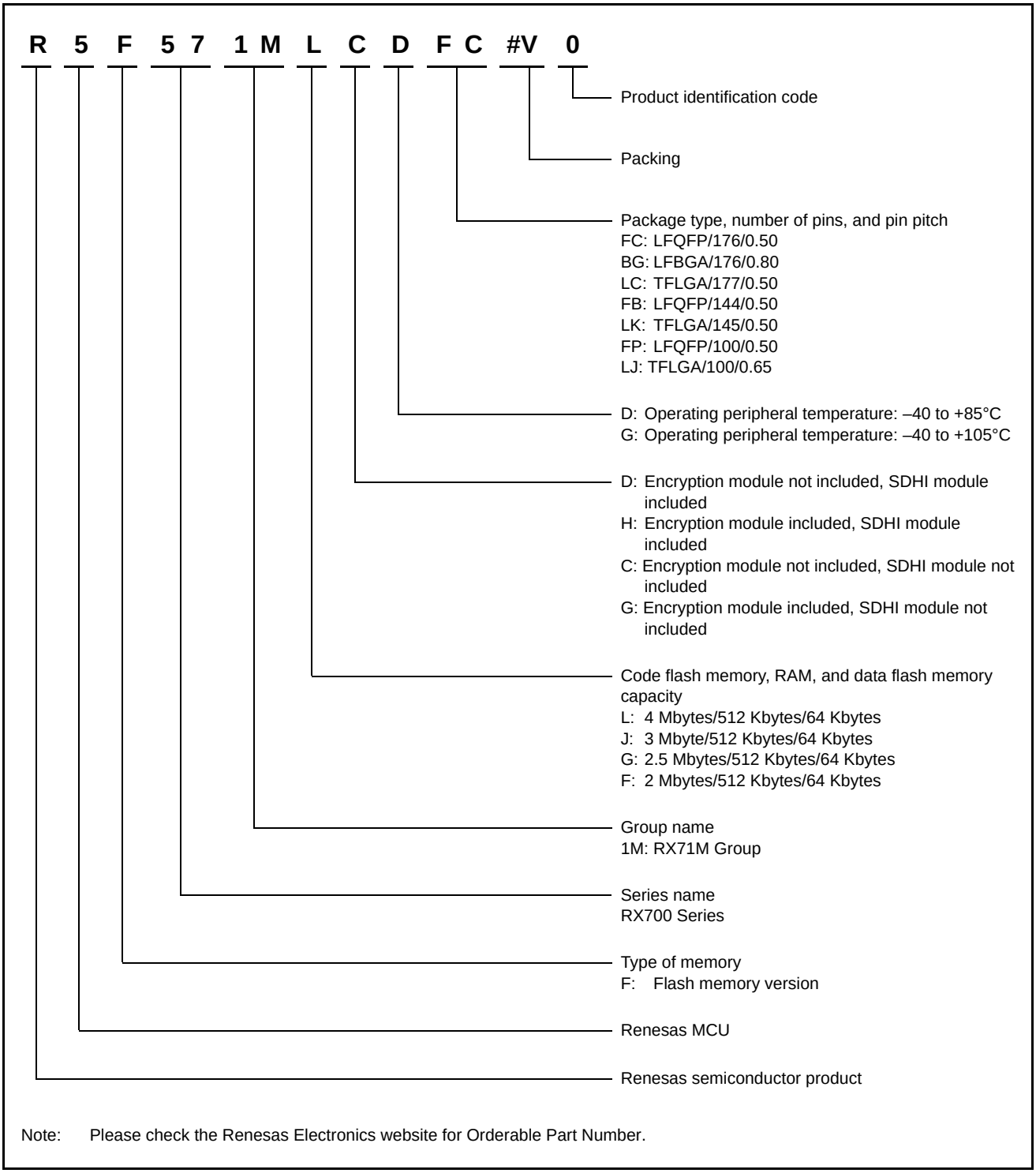
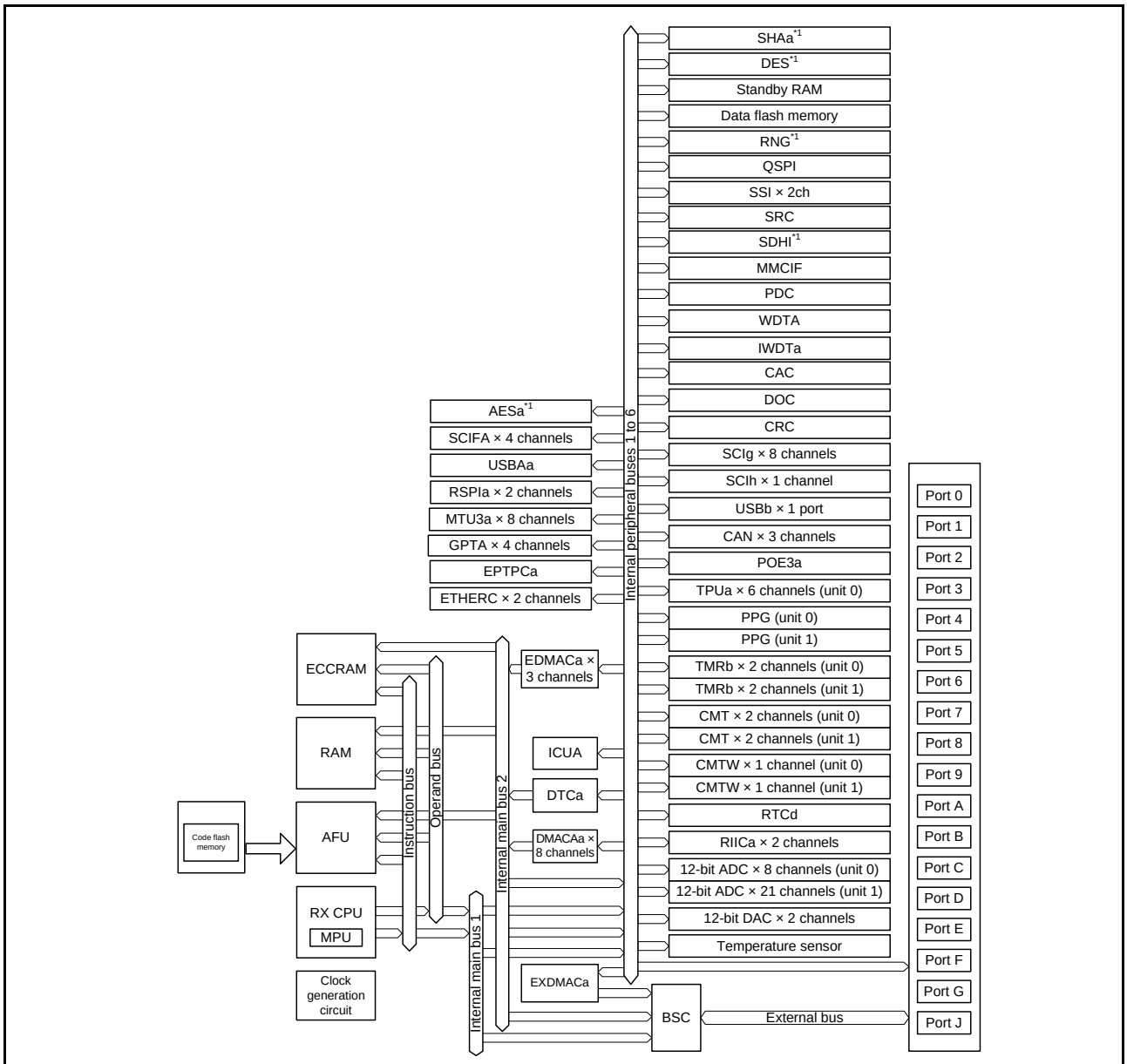


Figure 1.1 How to Read the Product Part Number

1.3 Block Diagram

Figure 1.2 shows a block diagram.



ETHERC: Ethernet controller
EPTPCa: PTP controller for ethernet controller
EDMAC: DMA controller for ethernet controller
ICUA: Interrupt controller
DTCa: Data transfer controller
DMACAa: DMA controller
EXDMACa: EXDMA controller
BSC: Bus controller
WDTA: Watchdog timer
IWDTa: Independent watchdog timer
CRC: CRC (cyclic redundancy check) calculator
SCI: Serial communications interface
SCIFA: Serial communications interface with FIFO
USBb: USB2.0 FS host/function module
USBAa: USB2.0 HS host/function module with battery charging
RSPIa: Serial peripheral interface
MPU: Memory protection unit
QSPI: Quad serial peripheral interface
SDHI: SD host interface*1
MMCIF: MMC host interface

PDC: Parallel data capture unit
CAN: CAN module
MTU3a: Multi-function timer pulse unit 3
POE3a: Port output enable 3
GPTA: General-purpose PWM timer
TPUa: 16-bit timer pulse unit
PPG: Programmable pulse generator
TMRb: 8-bit timer
CMT: Compare match timer
CMTW: Compare match timer W
RTCd: Realtime clock
RIICa: I^2C bus interface
DOC: Data operation circuit
CAC: Clock frequency accuracy measurement circuit
AESa: AES*1
DES: DES*1
SHAa: SHA-256*1
RNG: True random number generator*1
SSI: Serial sound interface
SRC: Sampling rate converter
AFU: Advanced fetching unit

Note 1. Optional

Figure 1.2 Block Diagram

1.4 Pin Functions

Table 1.4 lists the pin functions.

Table 1.4 Pin Functions (1/8)

Classifications	Pin Name	I/O	Description
Digital power supply	VCC	Input	Power supply pin. Connect this pin to the system power supply. Connect the pin to VSS via a 0.1-µF multilayer ceramic capacitor. The capacitor should be placed close to the pin.
	VCL	Input	Connect this pin to VSS via a 0.22-µF multilayer ceramic capacitor. The capacitor should be placed close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
	VBATT	Input	Backup power pin
Clock	XTAL	Output	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	BCLK	Output	Outputs the external bus clock for external devices.
	SDCLK	Output	Outputs the SDRAM-dedicated clock.
	XCOUT	Output	Input/output pins for the sub clock oscillator. Connect a crystal resonator between XCOUT and XCIN.
	XCIN	Input	
Clock frequency accuracy measurement	CACREF	Input	Reference clock input pin for the clock frequency accuracy measurement circuit
Operating mode control	MD	Input	Pins for setting the operating mode. The signal levels on these pins must not be changed during operation.
	UB	Input	USB boot mode or user boot mode enable pin
	UPSEL	Input	Selects the power supply method in USB boot mode. The low level selects self-power mode and the high level selects bus power mode.
System control	RES#	Input	Reset signal input pin. This LSI enters the reset state when this signal goes low.
	EMLE	Input	Input pin for the on-chip emulator enable signal. When the on-chip emulator is used, this pin should be driven high. When not used, it should be driven low.
	BSCANP	Input	Boundary scan enable pin. Boundary scan is enabled when this pin goes high. When not used, it should be driven low.
On-chip emulator	FINED	I/O	Fine interface pin
	TRST#	Input	On-chip emulator or boundary scan pins. When the EMLE pin is driven high, these pins are dedicated for the on-chip emulator.
	TMS	Input	
	TDI	Input	
	TCK	Input	
	TDO	Output	
	TRCLK	Output	This pin outputs the clock for synchronization with the trace data.
	TRSYNC	Output	This pin indicates that output from the TRDATA0 to TRDATA3 pins is valid.
	TRDATA0 to TRDATA3	Output	These pins output the trace information.
Address bus	A0 to A23	Output	Output pins for the address
Data bus	D0 to D31	I/O	Input and output pins for the bidirectional data bus
Multiplexed bus	A0/D0 to A15/D15	I/O	Address/data multiplexed bus

Table 1.4 Pin Functions (2/8)

Classifications	Pin Name	I/O	Description
Bus control	RD#	Output	Strobe signal which indicates that reading from the external bus interface space is in progress
	WR#	Output	Strobe signal which indicates that writing to the external bus interface space is in progress, in 1-write strobe mode
	WR0# to WR3#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0, D15 to D8, D23 to D16 and D31 to D24) is valid in writing to the external bus interface space, in byte strobe mode
	BC0# to BC3#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0, D15 to D8, D23 to D16 and D31 to D24) is valid in access to the external bus interface space, in 1-write strobe mode
	ALE	Output	Address latch signal when address/data multiplexed bus is selected
	WAIT#	Input	Input pin for wait request signals in access to the external space
	CS0# to CS7#	Output	Select signals for CS areas
	CKE	Output	SDRAM clock enable signal
	SDCS#	Output	SDRAM chip select signal
	RAS#	Output	SDRAM row address strobe signal
	CAS#	Output	SDRAM column address strove signal
	WE#	Output	SDRAM write enable pin
	DQM0 to DQM3	Output	SDRAM I/O data mask enable signals
EXDMA controller	EDREQ0, EDREQ1	Input	External DMA transfer request pins
	EDACK0, EDACK1	Output	Single address transfer acknowledge signals
Interrupt	NMI	Input	Non-maskable interrupt request pin
	IRQ0 to IRQ15	Input	Maskable interrupt request pins
Multi-function timer pulse unit 3	MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D	I/O	The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins
	MTIOC1A, MTIOC1B	I/O	The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins
	MTIOC2A, MTIOC2B	I/O	The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins
	MTIOC3A, MTIOC3B, MTIOC3C, MTIOC3D	I/O	The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins
	MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D	I/O	The TGRA4 to TGRD4 input capture input/output compare output/PWM output pins
	MTIC5U, MTIC5V, MTIC5W	Input	The TGRU5, TGRV5, and TGRW5 input capture input/dead time compensation input pins
	MTIOC6A, MTIOC6B, MTIOC6C, MTIOC6D	I/O	The TGRA6 to TGRD6 input capture input/output compare output/PWM output pins
	MTIOC7A, MTIOC7B, MTIOC7C, MTIOC7D	I/O	The TGRA7 to TGRD7 input capture input/output compare output/PWM output pins
	MTIOC8A, MTIOC8B, MTIOC8C, MTIOC8D	I/O	The TGRA8 to TGRD8 input capture input/output compare output/PWM output pins
	MTCLKA, MTCLKB, MTCLKC, MTCLKD	Input	Input pins for external clock signals or for phase counting mode clock signals
Port output enable 3	POE0#, POE4#, POE8#, POE10#, POE11#	Input	Input pins for request signals to place the MTU or GPT in the high impedance state

Table 1.4 Pin Functions (3/8)

Classifications	Pin Name	I/O	Description
General-purpose PWM timer	GTIOC0A-A/GTIOC0A-B/ GTIOC0A-C/GTIOC0A-D/ GTIOC0A-E, GTIOC0B-A/GTIOC0B-B/ GTIOC0B-C/GTIOC0B-D/ GTIOC0B-E	I/O	GPT0.GTGRA and GPT0.GTGRB input capture input/output compare output/PWM output pins
	GTIOC1A-A/GTIOC1A-B/ GTIOC1A-C/GTIOC1A-D/ GTIOC1A-E, GTIOC1B-A/GTIOC1B-B/ GTIOC1B-C/GTIOC1B-D/ GTIOC1B-E	I/O	GPT1.GTGRA and GPT1.GTGRB input capture input/output compare output/PWM output pins
	GTIOC2A-A/GTIOC2A-B/ GTIOC2A-C/GTIOC2A-D/ GTIOC2A-E, GTIOC2B-A/GTIOC2B-B/ GTIOC2B-C/GTIOC2B-D/ GTIOC2B-E	I/O	GPT2.GTGRA and GPT2.GTGRB input capture input/output compare output/PWM output pins
	GTIOC3A-D/GTIOC3A-E, GTIOC3B-D/GTIOC3B-E	I/O	GPT3.GTGRA and GPT3.GTGRB input capture input/output compare output/PWM output pins
	GTETRG-B/GTETRG-C/ GTETRG-D	Input	External trigger input pin for GPT0 to GPT3
16-bit timer pulse unit	TIOCA0, TIOCB0, TIOCC0, TIOCD0	I/O	The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins
	TIOCA1, TIOCB1	I/O	The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins
	TIOCA2, TIOCB2	I/O	The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins
	TIOCA3, TIOCB3, TIOCC3, TIOCD3	I/O	The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins
	TIOCA4, TIOCB4	I/O	The TGRA4 and TGRB4 input capture input/output compare output/PWM output pins
	TIOCA5, TIOCB5	I/O	The TGRA5 and TGRB5 input capture input/output compare output/PWM output pins
	TCLKA, TCLKB, TCLKC, TCLKD	Input	Input pins for external clock signals or for phase counting mode clock signals
Programmable pulse generator	PO0 to PO31	Output	Output pins for the pulse signals
8-bit timer	TMO0 to TMO3	Output	Compare match output pins
	TMCI0 to TMCI3	Input	Input pins for external clocks to be input to the counter
	TMRI0 to TMRI3	Input	Input pins for the counter reset
Compare match timer W	TIC0 to TIC3	Input	Input pins for CMTW
	TOC0 to TOC3	Output	Output pins for CMTW

Table 1.4 Pin Functions (4/8)

Classifications	Pin Name	I/O	Description
Serial communications interface (SCIg)	• Asynchronous mode/clock synchronous mode		
	SCK0 to SCK7	I/O	Input/output pins for the clock
	RXD0 to RXD7	Input	Input pins for received data
	TXD0 to TXD7	Output	Output pins for transmitted data
	CTS0# to CTS7#	Input	Input pins for controlling the start of transmission and reception
	RTS0# to RTS7#	Output	Output pins for controlling the start of transmission and reception
	• Simple I^2C mode		
	SSCL0 to SSCL7	I/O	Input/output pins for the I^2C clock
	SSDA0 to SSDA7	I/O	Input/output pins for the I^2C data
	• Simple SPI mode		
	SCK0 to SCK7	I/O	Input/output pins for the clock
	SMISO0 to SMISO7	I/O	Input/output pins for slave transmission of data
	SMOSI0 to SMOSI7	I/O	Input/output pins for master transmission of data
	SS0# to SS7#	Input	Chip-select input pins
Serial communications interface (SCIh)	• Asynchronous mode/clock synchronous mode		
	SCK12	I/O	Input/output pin for the clock
	RXD12	Input	Input pin for received data
	TXD12	Output	Output pin for transmitted data
	CTS12#	Input	Input pin for controlling the start of transmission and reception
	RTS12#	Output	Output pin for controlling the start of transmission and reception
	• Simple I^2C mode		
	SSCL12	I/O	Input/output pin for the I^2C clock
	SSDA12	I/O	Input/output pin for the I^2C data
	• Simple SPI mode		
	SCK12	I/O	Input/output pin for the clock
	SMISO12	I/O	Input/output pin for slave transmission of data
	SMOSI12	I/O	Input/output pin for master transmission of data
	SS12#	Input	Chip-select input pin
	• Extended serial mode		
	RXDX12	Input	Input pin for received data
	TXDX12	Output	Output pin for transmitted data
	SIOX12	I/O	Input/output pin for received or transmitted data
Serial communications interface with FIFO (SCIFA)	SCK8 to SCK11	I/O	Input/output pins for the clock
	RXD8 to RXD11	Input	Input pins for received data
	TXD8 to TXD11	Output	Output pins for transmitted data
	CTS8# to CTS11#	Input	Input pins for controlling the start of transmission and reception
	RTS8# to RTS11#	Output	Output pins for controlling the start of transmission and reception
I^2C bus interface	SCL0[FM+], SCL2	I/O	Input/output pins for clocks. Bus can be directly driven by the N-channel open drain
	SDA0[FM+], SDA2	I/O	Input/output pins for data. Bus can be directly driven by the N-channel open drain

Table 1.4 Pin Functions (5/8)

Classifications	Pin Name	I/O	Description
Ethernet controller	REF50CK0, REF50CK1	Input	50-MHz reference clocks. These pins input reference signals for transmission/reception timings in RMII mode.
	RMII0_CRS_DV, RMII1_CRS_DV	Input	Indicate that there are carrier detection signals and valid receive data on RMII_RXD1 and RMII_RXD0 in RMII mode.
	RMII0_TXD0, RMII0_TXD1, RMII1_TXD0, RMII1_TXD1	Output	2-bit transmit data in RMII mode
	RMII0_RXD0, RMII0_RXD1, RMII1_RXD0, RMII1_RXD1	Input	2-bit receive data in RMII mode
	RMII0_TXD_EN, RMII1_TXD_EN	Output	Output pins for data transmit enable signals in RMII mode
	RMII0_RX_ER, RMII1_RX_ER	Input	Indicate an error has occurred during reception of data in RMII mode.
	ET0_CRS, ET1_CRS	Input	Carrier detection/data reception enable pins
	ET0_RX_DV, ET1_RX_DV	Input	Indicate that there are valid receive data on ET_ERXD3 to ET_ERXD0.
	ET0_EXOUT, ET1_EXOUT	Output	General-purpose external output pins
	ET0_LINKSTA, ET1_LINKSTA	Input	Input link status from the PHY-LSI.
	ET0_ETXD0 to ET0_ETXD3, ET1_ETXD0 to ET1_ETXD3	Output	4 bits of MII transmit data
	ET0_ERXD0 to ET0_ERXD3, ET1_ERXD0 to ET1_ERXD3	Input	4 bits of MII receive data
	ET0_TX_EN, ET1_TX_EN	Output	Transmit enable pins. Function as signals indicating that transmit data is ready on ET_ETXD3 to ET_ETXD0.
	ET0_TX_ER, ET1_TX_ER	Output	Transmit error pins. Function as signals notifying the PHY-LSI of an error during transmission.
	ET0_RX_ER, ET1_RX_ER	Input	Receive error pins. Function as signals to recognize an error during reception.
	ET0_TX_CLK, ET1_TX_CLK	Input	Transmit clock pins. These pins input reference signals for output timings from ET_TX_EN, ET_ETXD3 to ET_ETXD0, and ET_TX_ER.
	ET0_RX_CLK, ET1_RX_CLK	Input	Receive clock pins. These pins input reference signals for input timings to ET_RX_DV, ET_ERXD3 to ET_ERXD0, and ET_RX_ER.
	ET0_COL, ET1_COL	Input	Input collision detection signals.
	ET0_WOL, ET1_WOL	Output	Receive Magic packets.
	ET0_MDC, ET1_MDC	Output	Output reference clock signals for information transfer via ET_MDIO.
	ET0_MDIO, ET1_MDIO	I/O	Input or output bidirectional signals for exchange of management information between this MCU and the PHY-LSI.

Table 1.4 Pin Functions (6/8)

Classifications	Pin Name	I/O	Description
USB 2.0 host/function module	VCC_USB, VCC_USBA	Input	Power supply pins
	VSS_USB, VSS1_USBA, VSS2_USBA	Input	Ground pins
	AVCC_USBA	Input	USBA analog power supply pin
	AVSS_USBA	Input	USBA analog ground pin. Short this pin with the PVSS_USBA pin.
	PVSS_USBA	Input	USBA PLL circuit ground pin. Short this pin with the AVSS_USBA pin.
	USBA_RREF	I/O	USBA reference current supply pin. Connect 2.2 kΩ (±1%) to the AVSS_USBA pin.
	USB0_DP, USBA_DP	I/O	Input or output USB transceiver D+ data.
	USB0_DM, USBA_DM	I/O	Input or output USB transceiver D- data.
	USB0_EXICEN, USBA_EXICEN	Output	Connect to the OTG power IC.
	USB0_ID, USBA_ID	Input	Connect to the OTG power IC.
	USB0_VBUSEN, USBA_VBUSEN	Output	USB VBUS power enable pins
	USB0_OVRCURA/ USB0_OVRCURB, USBA_OVRCURA/ USBA_OVRCURB	Input	USB overcurrent pins
	USB0_VBUS, USBA_VBUS	Input	USB cable connection/disconnection detection input pins
CAN module	CRX0, CRX1-DS, CRX2	Input	Input pins
	CTX0 to CTX2	Output	Output pins
Serial peripheral interface	RSPCKA-A/RSPCKA-B/ RSPCKB-A/RSPCKB-B	I/O	Clock input/output pin
	MOSIA-A/MOSIA-B/ MOSIB-A/MOSIB-B	I/O	Inputs or outputs data output from the master
	MISOA-A/MISOA-B/ MISOB-A/MISOB-B	I/O	Inputs or outputs data output from the slave
	SSLA0-A/SSLA0-B/ SSLB0-A/SSLB0-B	I/O	Input or output pin for slave selection
	SSLA1-A/SSLA1-B/ SSLB1-A/SSLB1-B to SSLA3-A/SSLA3-B/ SSLB3-A/SSLB3-B	Output	Output pin for slave selection
Quad serial peripheral interface	QSPCLK-A/-B	Output	QSPI clock output pin
	QSSL-A/-B	Output	QSPI slave output pin
	QMO-A/-B, QIO0-A/-B	I/O	Master transmit data/data 0
	QMI-A/-B, QIO1-A/-B	I/O	Master input data/data 1
	QIO2-A/-B, QIO3-A/-B	I/O	Data 2, data 3
Serial sound interface	SSISCK0, SSISCK1	I/O	SSI serial bit clock pins
	SSIWS0, SSIWS1	I/O	Word select pins
	SSITXD0	Output	Serial data output pins
	SSIRXD0	Input	Serial data input pins
	SSIDATA1	I/O	Serial data input/output pins
	AUDIO_MCLK	Input	Master clock pin for audio

Table 1.4 Pin Functions (7/8)

Classifications	Pin Name	I/O	Description
MMC host interface	MMC_CLK-A/ MMC_CLK-B	Output	MMC clock pin
	MMC_CMD-A/ MMC_CMD-B	I/O	Command/response pin
	MMC_D7-A/MMC_D7-B to MMC_D0-A/MMC_D0-B	I/O	Transmit data/receive data
	MMC_CD-A/MMC_CD-B	Input	Card detection pin
	MMC_RES#-A/MMC_RES#-B	Output	MMC reset output pin
SD host interface	SDHI_CLK-A/SDHI_CLK-B	Output	SD clock output pin
	SDHI_CMD-A/SDHI_CMD-B	I/O	SD command output, response input signal pin
	SDHI_D3-A/SDHI_D3-B to SDHI_D0-A/SDHI_D0-B	I/O	SD data bus pins
	SDHI_CD-A/SDHI_CD-B	Input	SD card detection pin
	SDHI_WP-A/SDHI_WP-B	Input	SD write-protect signal
Parallel data capture unit	PIXCLK	Input	Image transfer clock pin
	VSYNC	Input	Vertical synchronization signal pin
	HSYNC	Input	Horizontal synchronization signal pin
	PIXD0 to PIXD7	Input	8-bit image data pins
	PCKO	Output	Output pin for dot clock
Realtime clock	RTCOUT	Output	Output pin for 1-Hz/64-Hz clock
	RTCIC0 to RTCIC2	Input	Time capture event input pins
12-bit A/D converter	AN000 to AN007, AN100 to AN120	Input	Input pins for the analog signals to be processed by the A/D converter
	ADTRG0#, ADTRG1#	Input	Input pins for the external trigger signals that start the A/D conversion
	ANEX0	Output	Extended analog output pin
	ANEX1	Input	Extended analog input pin
12-bit D/A converter	DA0, DA1	Output	Output pins for the analog signals to be processed by the D/A converter
Analog power supply	AVCC0	Input	Analog voltage supply pin for the 12-bit A/D converter (unit 0). Connect this pin to a branch from the VCC power supply.
	AVSS0	Input	Analog ground pin for the 12-bit A/D converter (unit 0). Connect this pin to a branch from the VSS ground power supply.
	VREFH0	Input	Analog reference voltage supply pin for the 12-bit A/D converter (unit 0). Connect this pin to VCC if the 12-bit A/D converter is not to be used.
	VREFL0	Input	Analog reference ground pin for the 12-bit A/D converter (unit 0). Connect this pin to VSS if the 12-bit A/D converter is not to be used.
	AVCC1	Input	Analog voltage supply and reference voltage supply pin for the 12-bit A/D converter (unit 1) and D/A converter. This pin also supplies the analog voltage to the temperature sensor. Connect this pin to a branch from the VCC power supply.
	AVSS1	Input	Analog voltage supply and reference voltage supply pin for the 12-bit A/D converter (unit 1) and D/A converter. This pin also supplies the analog ground voltage to the temperature sensor. Connect this pin to a branch from the VSS ground power supply.

Table 1.4 Pin Functions (8/8)

Classifications	Pin Name	I/O	Description
I/O ports	P00 to P03, P05, P07	I/O	6-bit input/output pins
	P10 to P17	I/O	8-bit input/output pins
	P20 to P27	I/O	8-bit input/output pins
	P30 to P37	I/O	8-bit input/output pins (P35: input pin)
	P40 to P47	I/O	8-bit input/output pins
	P50 to P56	I/O	7-bit input/output pins (176-pin devices have only P50 to P53)
	P60 to P67	I/O	8-bit input/output pins
	P70 to P77	I/O	8-bit input/output pins
	P80 to P83, P86, P87	I/O	6-bit input/output pins
	P90 to P97	I/O	8-bit input/output pins
	PA0 to PA7	I/O	8-bit input/output pins
	PB0 to PB7	I/O	8-bit input/output pins
	PC0 to PC7	I/O	8-bit input/output pins
	PD0 to PD7	I/O	8-bit input/output pins
	PE0 to PE7	I/O	8-bit input/output pins
	PF0 to PF5	I/O	6-bit input/output pins
	PG0 to PG7	I/O	8-bit input/output pins
	PJ3, PJ5	I/O	2-bit input/output pins

Note: Note the following regarding pin names. For details, see section 1.5, Pin Assignments.

- We recommend that pins suffixed with the same letter such as -A and -B, indicating grouping of the pins, should be used as a set. The AC characteristics of the RSPI, QSPI, SDHI, and MMC are measured using the pins from the same group.
- When the pin functions have “-DS” appended to their names, they can also be used as triggers for release from deep software standby.
- RIIC pin functions that have [FM+] appended to their names support fast-mode plus.

1.5 Pin Assignments

1.5.1 177-Pin TFLGA

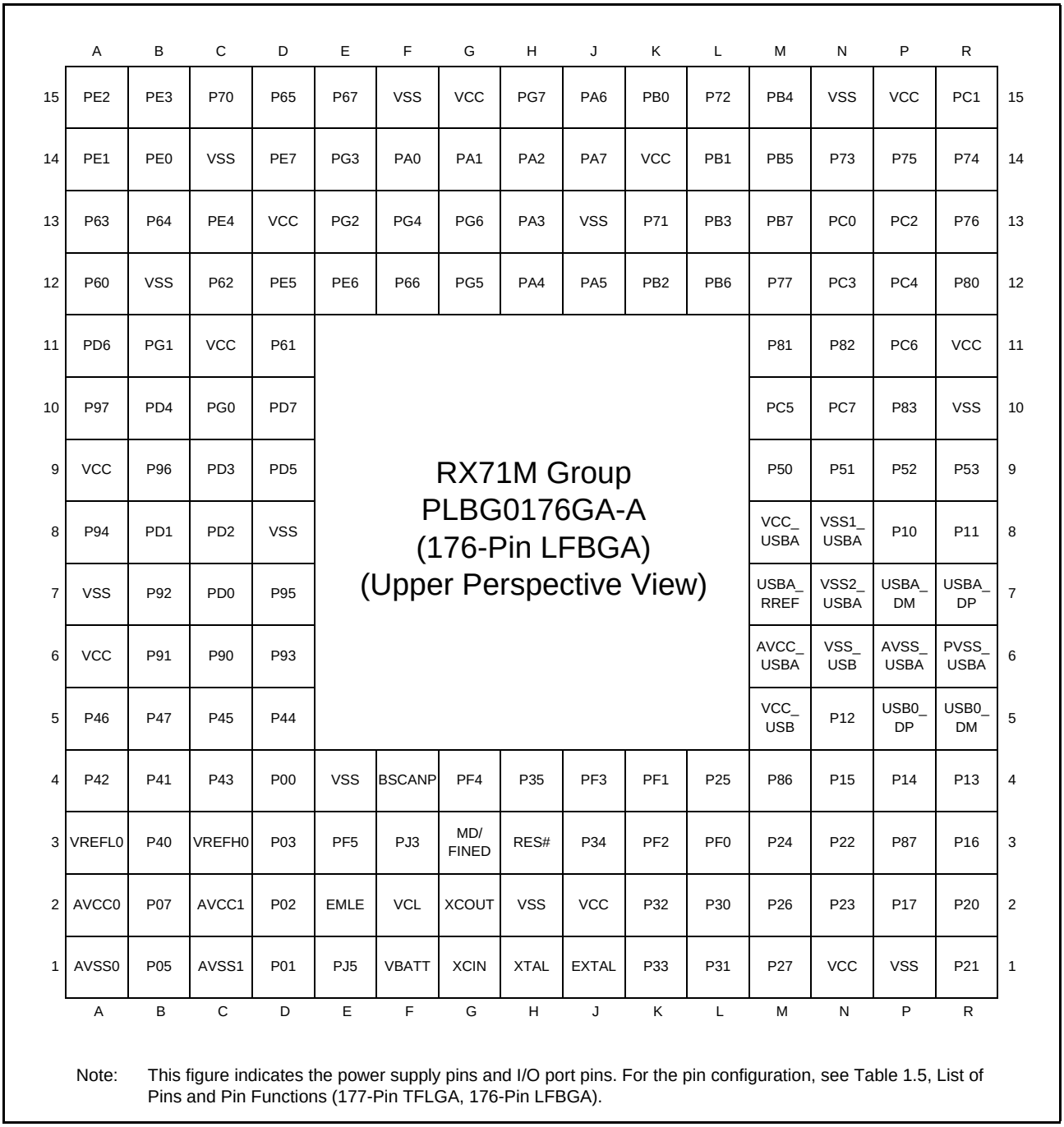
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	
15	PE2	PE3	P70	P65	P67	VSS	VCC	PG7	PA6	PB0	P72	PB4	VSS	VCC	PC1	15
14	PE1	PE0	VSS	PE7	PG3	PA0	PA1	PA2	PA7	VCC	PB1	PB5	P73	P75	P74	14
13	P63	P64	PE4	VCC	PG2	PG4	PG6	PA3	VSS	P71	PB3	PB7	PC0	PC2	P76	13
12	P60	VSS	P62	PE5	PE6	P66	PG5	PA4	PA5	PB2	PB6	P77	PC3	PC4	P80	12
11	PD6	PG1	VCC	P61								P81	P82	PC6	VCC	11
10	P97	PD4	PG0	PD7								PC5	PC7	P83	VSS	10
9	VCC	P96	PD3	PD5								P50	P51	P52	P53	9
8	P94	PD1	PD2	VSS								VCC_ USBA	VSS1_ USBA	P10	P11	8
7	VSS	P92	PD0	P95								USBA_ RREF	VSS2_ USBA	USBA_ DM	USBA_ DP	7
6	VCC	P91	P90	P93								AVCC_ USBA	VSS_ USB	AVSS_ USBA	PVSS_ USBA	6
5	P46	P47	P45	P44	NC							VCC_ USB	P12	USB0_ DP	USB0_ DM	5
4	P42	P41	P43	P00	VSS	BSCANP	PF4	P35	PF3	PF1	P25	P86	P15	P14	P13	4
3	VREFL0	P40	VREFH0	P03	PF5	PJ3	MD/ FINED	RES#	P34	PF2	PF0	P24	P22	P87	P16	3
2	AVCC0	P07	AVCC1	P02	EMLE	VCL	XCOUT	VSS	VCC	P32	P30	P26	P23	P17	P20	2
1	AVSS0	P05	AVSS1	P01	PJ5	VBATT	XCIN	XTAL	EXTAL	P33	P31	P27	VCC	VSS	P21	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	

RX71M Group
PTLG0177KA-A
(177-Pin TFLGA)
(Upper Perspective View)

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.5, List of Pins and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA).

Figure 1.3 Pin Assignment (177-Pin TFLGA)

1.5.2 176-Pin LFBGA

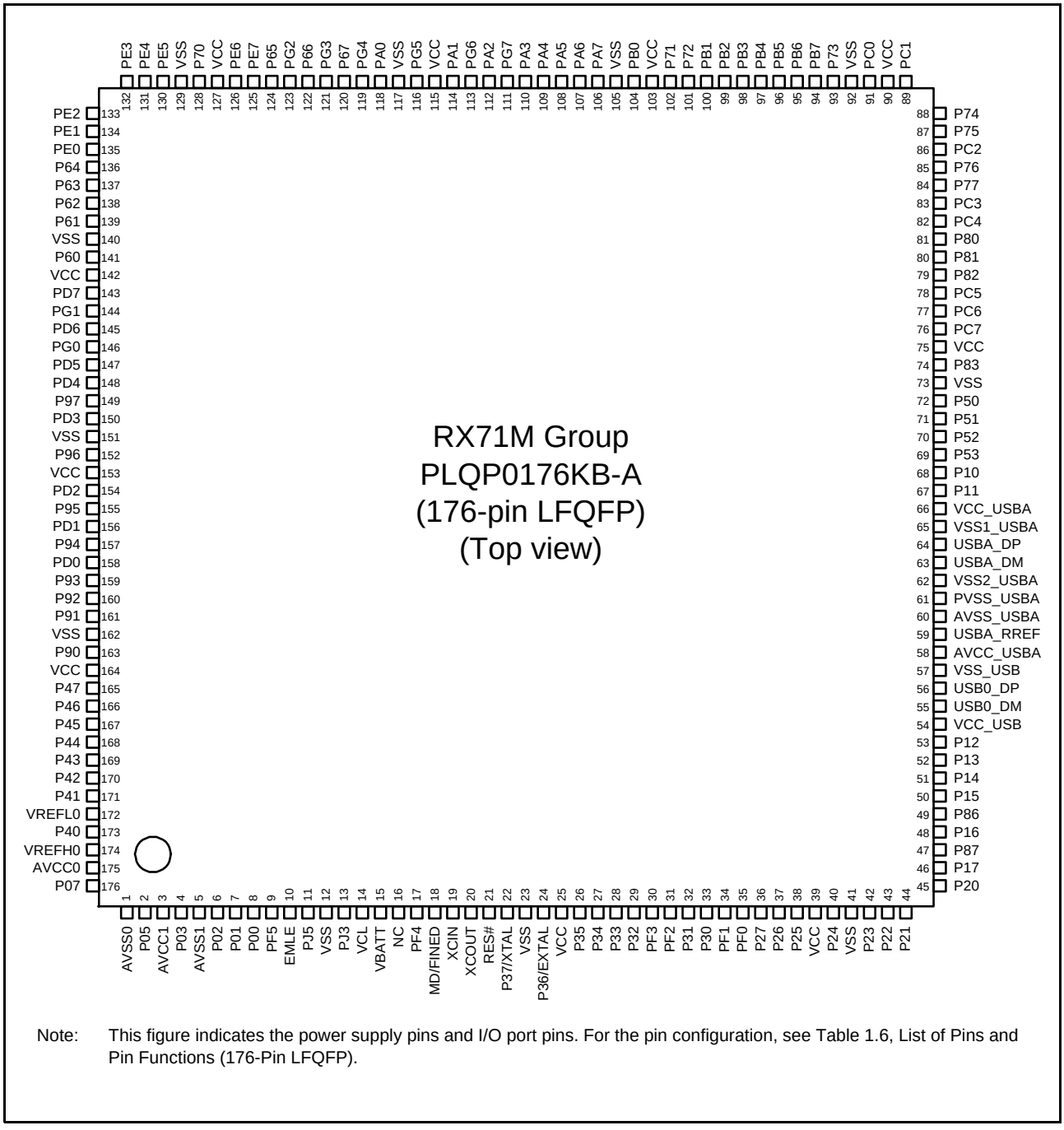


	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	
15	PE2	PE3	P70	P65	P67	VSS	VCC	PG7	PA6	PB0	P72	PB4	VSS	VCC	PC1	15
14	PE1	PE0	VSS	PE7	PG3	PA0	PA1	PA2	PA7	VCC	PB1	PB5	P73	P75	P74	14
13	P63	P64	PE4	VCC	PG2	PG4	PG6	PA3	VSS	P71	PB3	PB7	PC0	PC2	P76	13
12	P60	VSS	P62	PE5	PE6	P66	PG5	PA4	PA5	PB2	PB6	P77	PC3	PC4	P80	12
11	PD6	PG1	VCC	P61								P81	P82	PC6	VCC	11
10	P97	PD4	PG0	PD7								PC5	PC7	P83	VSS	10
9	VCC	P96	PD3	PD5								P50	P51	P52	P53	9
8	P94	PD1	PD2	VSS								VCC_ USBA	VSS1_ USBA	P10	P11	8
7	VSS	P92	PD0	P95								USBA_ RREF	VSS2_ USBA	USBA_ DM	USBA_ DP	7
6	VCC	P91	P90	P93								AVCC_ USBA	VSS_ USB	AVSS_ USBA	PVSS_ USBA	6
5	P46	P47	P45	P44								VCC_ USB	P12	USB0_ DP	USB0_ DM	5
4	P42	P41	P43	P00	VSS	BSCANP	PF4	P35	PF3	PF1	P25	P86	P15	P14	P13	4
3	VREFL0	P40	VREFH0	P03	PF5	PJ3	MD/ FINED	RES#	P34	PF2	PF0	P24	P22	P87	P16	3
2	AVCC0	P07	AVCC1	P02	EMLE	VCL	XCOUT	VSS	VCC	P32	P30	P26	P23	P17	P20	2
1	AVSS0	P05	AVSS1	P01	PJ5	VBATT	XCIN	XTAL	EXTAL	P33	P31	P27	VCC	VSS	P21	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.5, List of Pins and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA).

Figure 1.4 Pin Assignment (176-Pin LFBGA)

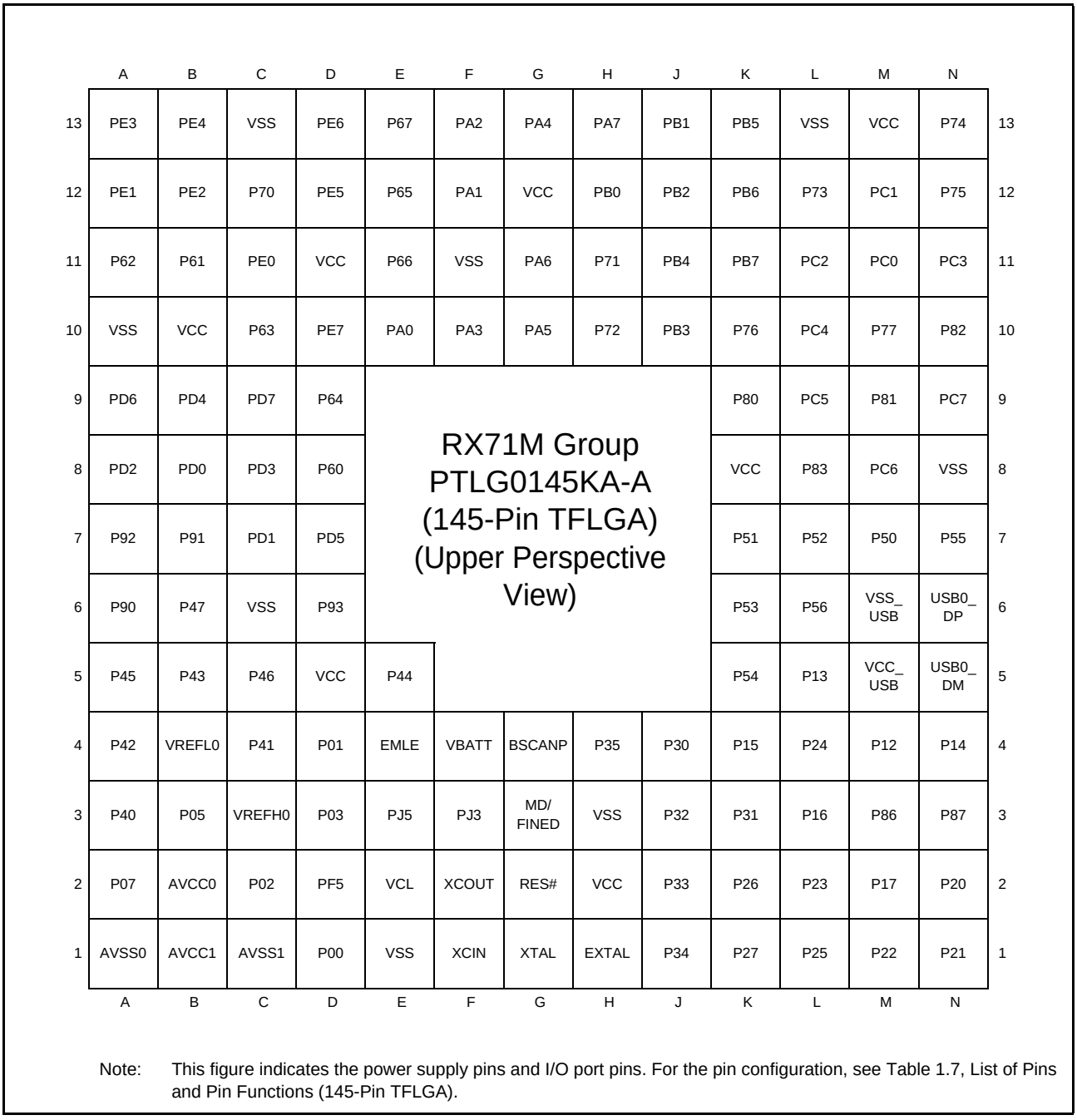
1.5.3 176-pin LFQFP



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.6, List of Pins and Pin Functions (176-Pin LFQFP).

Figure 1.5 Pin Assignment (176-Pin LFQFP)

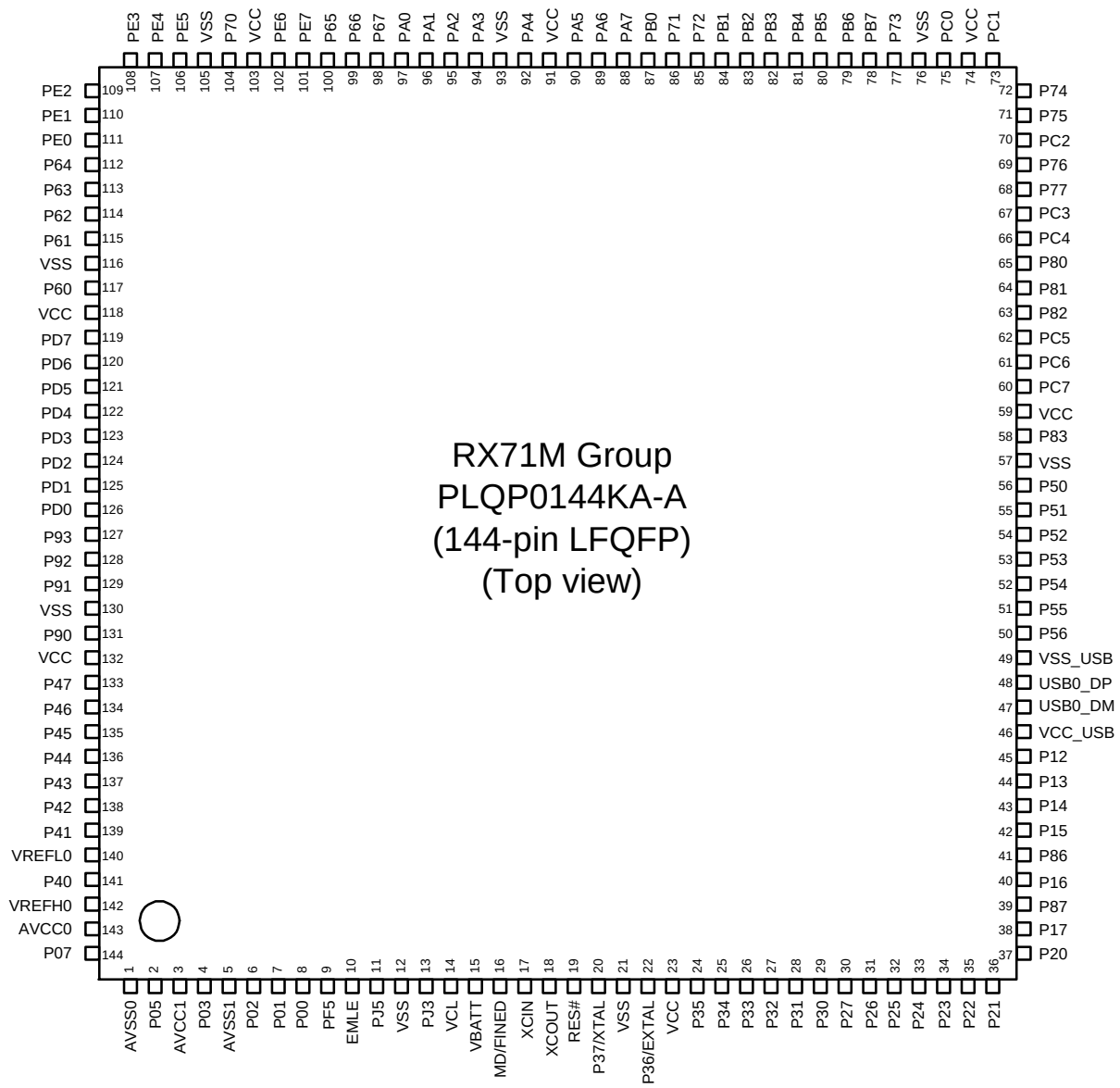
1.5.4 145-Pin TFLGA



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.7, List of Pins and Pin Functions (145-Pin TFLGA).

Figure 1.6 Pin Assignment (145-Pin TFLGA)

1.5.5 144-pin LFQFP



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.8, List of Pins and Pin Functions (144-Pin LFQFP).

Figure 1.7 Pin Assignment (144-Pin LFQFP)

1.5.6 100-Pin TFLGA

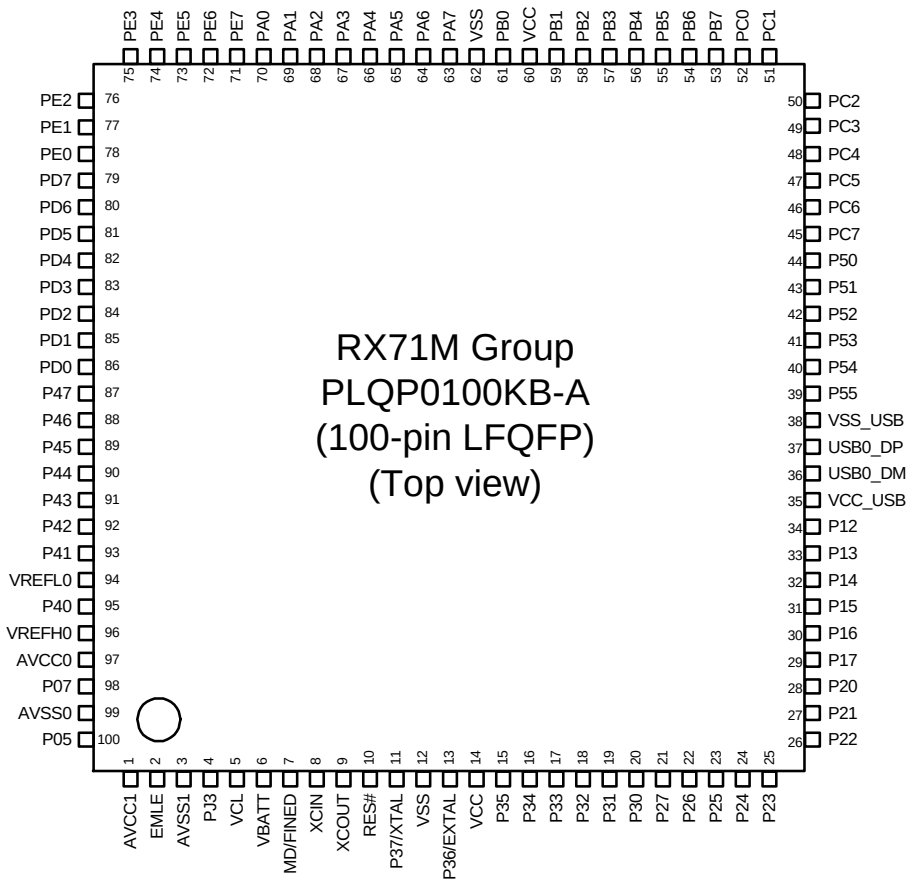
RX71M Group
PTLG0100JA-A (100-Pin TFLGA)
(Upper Perspective View)

	A	B	C	D	E	F	G	H	J	K	
10	PE2	PE3	PE4	PA0	PA3	VSS	VCC	PB7	PC1	PC2	10
9	PE1	PD7	PE5	PA1	PA5	PA7	PB1	PB6	PC0	PC3	9
8	PE0	PD6	PD5	PE7	PA4	PB0	PB4	PC6	PC4	PC5	8
7	PD4	PD3	PD2	PE6	PA6	PB2	PB5	PC7	P50	P51	7
6	PD0	PD1	P47	P46	PA2	PB3	P52	P54	VCC_ USB	USB0_ DP	6
5	P43	P44	P42	P45	P41	P12	P53	P55	VSS_ USB	USB0_ DM	5
4	VREFL0	P40	VREFH0	VBATT	P34	P32	P27	P15	P13	P14	4
3	P07	AVCC0	PJ3	MD/ FINED	RES#	P35	P30	P16	P17	P20	3
2	AVCC1	AVSS0	AVSS1	XCOUT	VSS	VCC	P31	P25	P21	P22	2
1	P05	EMLE	VCL	XCIN	XTAL	EXTAL	P33	P26	P24	P23	1
	A	B	C	D	E	F	G	H	J	K	

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.9, List of Pins and Pin Functions (100-Pin TFLGA).

Figure 1.8 Pin Assignment (100-Pin TFLGA)

1.5.7 100-pin LFQFP



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.10, List of Pins and Pin Functions (100-Pin LFQFP).

Figure 1.9 Pin Assignment (100-Pin LFQFP)

1.6 List of Pins and Pin Functions

1.6.1 177-Pin TFLGA and 176-Pin LFBGA

Table 1.5 List of Pins and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (1/7)

Pin Number 177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
A1	AVSS0							
A2	AVCC0							
A3	VREFL0							
A4		P42					IRQ10-DS	AN002
A5		P46					IRQ14-DS	AN006
A6	VCC							
A7	VSS							
A8		P94	A20/D20		ET1_ERXD0/ RMII1_RXD0			
A9	VCC							
A10		P97	A23/D23		ET1_ERXD3			
A11		PD6	D6[A6/D6]	MTIC5V/MTIOC8A/ POE4#		MMC_D0-B/ SDHI_D0-B/ QIO0-B/ QMO-B	IRQ6	AN106
A12		P60	CS0#		ET1_TX_EN/ RMII1_TXD_EN			
A13		P63	CS3#/CAS#					
A14		PE1	D9[A9/D9]	MTIOC4C/MTIOC3B/ GTIOC1B-A/PO18	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/SSLB2-B	MMC_D5-B		ANEX1
A15		PE2	D10[A10/D10]	MTIOC4A/ GTIOC0B-A/PO23/ TIC3	RXD12/SMISO12/ SSCL12/RXDX12/ SSLB3-B	MMC_D6-B	IRQ7-DS	AN100
B1		P05					IRQ13	DA1
B2		P07					IRQ15	ADTRG0#
B3		P40					IRQ8-DS	AN000
B4		P41					IRQ9-DS	AN001
B5		P47					IRQ15-DS	AN007
B6		P91	A17/D17		ET1_COL/SCK7			AN115
B7		P92	A18/D18	POE4#	ET1_CRS/ RMII1_CRS_DV/ RXD7/SMISO7/SSCL7			AN116
B8		PD1	D1[A1/D1]	MTIOC4B/ GTIOC1A-E/POE0#	CTX0		IRQ1	AN109
B9		P96	A22/D22		ET1_ERXD2			
B10		PD4	D4[A4/D4]	MTIOC8B/POE11#		MMC_CMD-B/ SDHI_CMD-B/ QSSL-B	IRQ4	AN112
B11		PG1	D25		ET1_RX_ER/ RMII1_RX_ER			
B12	VSS							
B13		P64	CS4#/WE#					
B14		PE0	D8[A8/D8]	MTIOC3D/ GTIOC2B-A	SCK12/SSLB1-B	MMC_D4-B		ANEX0

Table 1.5 List of Pins and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (2/7)

Pin Number 177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
B15		PE3	D11[A11/D11]	MTIOC4B/ GTIOC2A-A/PO26/ POE8#/TOC3	CTS12#/RTS12#/ SS12#/ ET0_ERXD3	MMC_D7-B		AN101
C1	AVSS1							
C2	AVCC1							
C3	VREFH0							
C4		P43					IRQ11-DS	AN003
C5		P45					IRQ13-DS	AN005
C6		P90	A16/D16		ET1_RX_DV/ TXD7/SMOSI7/SSDA7			AN114
C7		PD0	D0[A0/D0]	GTIOC1B-E/POE4#			IRQ0	AN108
C8		PD2	D2[A2/D2]	MTIOC4D/ GTIOC0B-E/TIC2	CRX0	MMC_D2-B/ SDHI_D2-B/ QIO2-B	IRQ2	AN110
C9		PD3	D3[A3/D3]	MTIOC8D/ GTIOC0A-E/POE8#/ TOC2		MMC_D3-B/ SDHI_D3-B/ QIO3-B	IRQ3	AN111
C10		PG0	D24		ET1_RX_CLK/ REF50CK1			
C11	VCC							
C12		P62	CS2#/RAS#					
C13		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A/ GTIOC1A-A/PO28	ET0_ERXD2/SSLB0-B			AN102
C14	VSS							
C15		P70	SDCLK					
D1		P01		TMCI0	RXD6/SMISO6/ SSCL6		IRQ9	AN119
D2		P02		TMCI1	SCK6		IRQ10	AN120
D3		P03					IRQ11	DA0
D4		P00		TMRI0	TXD6/SMOSI6/ SSDA6		IRQ8	AN118
D5		P44					IRQ12-DS	AN004
D6		P93	A19/D19	POE0#	ET1_LINKSTA/CTS7#/ RTS7#/SS7#			AN117
D7		P95	A21/D21		ET1_ERXD1/ RMII1_RXD1			
D8	VSS							
D9		PD5	D5[A5/D5]	MTIC5W/MTIOC8C/ POE10#		MMC_CLK-B/ SDHI_CLK-B/ QSPCLK-B	IRQ5	AN113
D10		PD7	D7[A7/D7]	MTIC5U/POE0#		MMC_D1-B/ SDHI_D1-B/ QIO1-B/QMI-B	IRQ7	AN107
D11		P61	CS1#/SDCS#					
D12		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B/ GTIOC0A-A	ET0_RX_CLK/ REF50CK0/ RSPCKB-B		IRQ5	AN103
D13	VCC							
D14		PE7	D15[A15/D15]	MTIOC6A/ GTIOC3A-E/TOC1	MISOB-B	MMC_RES#-B/ SDHI_WP-B	IRQ7	AN105
D15		P65	CS5#/CKE					
E1		PJ5		POE8#	CTS2#/RTS2#/SS2#			
E2	EMLE							

Table 1.5 List of Pins and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (3/7)

Pin Number 177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
E3		PF5					IRQ4	
E4	VSS							
E5*1								
E12		PE6	D14[A14/D14]	MTIOC6C/ GTIOC3B-E/TIC1	MOSIB-B	MMC_CD-B/ SDHI_CD-B	IRQ6	AN104
E13	TRDATA0	PG2	D26		ET1_TX_CLK			
E14	TRDATA1	PG3	D27		ET1_ETXD0/ RMII1_TXD0			
E15		P67	CS7#/DQM1	MTIOC7C/ GTIOC1B-C	CRX2		IRQ15	
F1	VBATT							
F2	VCL							
F3		PJ3	EDACK1	MTIOC3C	ET0_EXOUT/ CTS6#/RTS6#/ CTS0#/RTS0#/ SS6#/SS0#			
F4	BSCANP							
F12		P66	CS6#/DQM0	MTIOC7D/ GTIOC2B-C	CTX2			
F13	TRSYNC	PG4	D28		ET1_ETXD1/ RMII1_TXD1			
F14		PA0	A0/BC0#/ DQM2	MTIOC4A/MTIOC6D/ GTIOC0B-C/TIOCA0/ CACREF/PO16	SSLA1-B/ ET0_TX_EN/ RMII0_TXD_EN			
F15	VSS							
G1	XCIN							
G2	XCOUT							
G3	MD/FINED							
G4	TRST#	PF4						
G12	TRCLK	PG5	D29		ET1_ETXD2			
G13	TRDATA2	PG6	D30		ET1_ETXD3			
G14		PA1	A1/DQM3	MTIOC0B/MTCLKC/ MTIOC7B/ GTIOC2A-C/TIOCB0/ PO17	SCK5/SSLA2-B/ ET0_WOL		IRQ11	
G15	VCC							
H1	XTAL	P37						
H2	VSS							
H3	RES#							
H4	UPSEL	P35					NMI	
H12		PA4	A4	MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20	TXD5/SMOSI5/ SSDA5/SSLA0-B/ ET0_MDC		IRQ5-DS	
H13		PA3	A3	MTIOC0D/MTCLKD/ TIOCD0/TCLKB/PO19	RXD5/SMISO5/ SSCL5/ ET0_MDIO		IRQ6-DS	
H14		PA2	A2	MTIOC7A/ GTIOC1A-C/PO18	RXD5/SMISO5/ SSCL5/SSLA3-B			
H15	TRDATA3	PG7	D31		ET1_TX_ER			
J1	EXTAL	P36						
J2	VCC							
J3		P34		MTIOC0A/TMCI3/ PO12/POE10#	SCK6/SCK0/ ET0_LINKSTA		IRQ4	

Table 1.5 List of Pins and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (4/7)

Pin Number 177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
J4	TMS	PF3						
J12		PA5	A5	MTIOC6B/ GTIOC0A-C/TIOCB1/ PO21	RSPCKA-B/ ET0_LINKSTA			
J13	VSS							
J14		PA7	A7	TIOCB2/PO23	MISOA-B/ ET0_WOL			
J15		PA6	A6	MTIC5V/MTCLKB/ GTETRG-C/TIOCA2/ TMCI3/PO22/POE10#	CTS5#/RTS5#/SS5#/ MOSIA-B/ ET0_EXOUT			
K1		P33	EDREQ1	MTIOC0D/TIOCD0/ TMRI3/PO11/POE4#/ POE11#	RXD6/RXD0/ SMISO6/ SMISO0/SSCL6/ SSCL0/CRX0	PCKO	IRQ3-DS	
K2		P32		MTIOC0C/TIOCC0/ TMO3/PO10/ RTCOUT/RTCIC2/ POE0#/POE10#	TXD6/TXD0/ SMOSI6/SMOSI0/ SSDA6/SSDA0/ CTX0/ USB0_VBUSEN	VSYNC	IRQ2-DS	
K3	TDI	PF2			RXD1/SMISO1/ SSCL1			
K4	TCK	PF1			SCK1			
K12		PB2	A10	TIOCC3/TCLKC/ PO26	CTS4#/RTS4#/CTS6#/ RTS6#/SS4#/SS6#/ ET0_RX_CLK/ REF50CK0			
K13		P71	A18/CS1#		ET0_MDIO			
K14	VCC							
K15		PB0	A8	MTIC5W/TIOCA3/ PO24	RXD4/RXD6/SMISO4/ SMISO6/SSCL4/ SSCL6/ET0_ERXD1/ RMII0_RXD1		IRQ12	
L1		P31		MTIOC4D/TMCI2/ PO9/RTCIC1	CTS1#/RTS1#/ SS1#/ET1_MDC/ SSLB0-A		IRQ1-DS	
L2		P30		MTIOC4B/TMRI3/ PO8/RTCIC0/POE8#	RXD1/SMISO1/ SSCL1/ET1_MDIO/ MISOB-A		IRQ0-DS	
L3	TDO	PF0			TXD1/SMOSI1/ SSDA1			
L4		P25	CS5#/ EDACK1	MTIOC4C/MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/ SSCL3/ SSIDATA1	HSYNC		ADTRG0#
L12		PB6	A14	MTIOC3D/TIOCA5/ PO30	RXD9/ET0_ETXD1/ RMII0_TXD1			
L13		PB3	A11	MTIOC0A/MTIOC4A/ TIOCD3/TCLKD/ TMO0/PO27/POE11#	SCK4/SCK6/ ET0_RX_ER/ RMII0_RX_ER			
L14		PB1	A9	MTIOC0C/MTIOC4C/ TIOCB3/TMCI0/PO25	TXD4/TXD6/SMOSI4/ SMOSI6/SSDA4/ SSDA6/ET0_ERXD0/ RMII0_RXD0		IRQ4-DS	
L15		P72	A19/CS2#		ET0_MDC			
M1		P27	CS7#	MTIOC2B/TMCI3/PO7	SCK1/ET1_WOL/ RSPCKB-A			
M2		P26	CS6#	MTIOC2A/TMO1/PO6	TXD1/CTS3#/ RTS3#/SMOSI1/ SS3#/SSDA1/ ET1_EXOUT/ MOSIB-A			

Table 1.5 List of Pins and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (5/7)

Pin Number 177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
M3		P24	CS4#/ EDREQ1	MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4	SCK3/ USB0_VBUSEN/ SSISCK1	PIXCLK		
M4		P86		MTIOC4D/ GTIOC2B-B/TIOCA0	RXD10	PIXD1		
M5	VCC_USB							
M6	AVCC_USBA							
M7	USBA_RREF							
M8	VCC_USBA							
M9		P50	WR0#/WR#		TXD2/SMOSI2/ SSDA2/SSLB1-A			
M10		PC5	A21/CS2#/ WAIT#	MTIOC3B/MTCLKD/ GTIOC1A-D/TMRI2/ PO29	SCK8/RSPCKA-A/ RTS8#/ET0_ETXD2	MMC_D5-A		
M11		P81	EDACK0	MTIOC3D/ GTIOC0B-D/PO27	RXD10/ET0_ETXD0/ RMII0_TXD0	MMC_D3-A/ SDHI_CD-A/ QIO3-A		
M12		P77	CS7#	PO23	TXD11/ET0_RX_ER/ RMII0_RX_ER	MMC_CLK-A/ SDHI_CLK-A/ QSPCLK-A		
M13		PB7	A15	MTIOC3B/TIOCB5/ PO31	TXD9/ET0_CRS/ RMII0_CRS_DV			
M14		PB5	A13	MTIOC2A/MTIOC1B/ TIOCB4/TMRI1/PO29/ POE4#	SCK9/RTS9#/ ET0_ETXD0/ RMII0_TXD0			
M15		PB4	A12	TIOCA4/PO28	CTS9#/ET0_TX_EN/ RMII0_TXD_EN			
N1	VCC							
N2		P23	EDACK0	MTIOC3D/MTCLKD/ GTIOC0A-B/TIOCD3/ PO3	TXD3/CTS0#/RTS0#/ SMOSI3/SS0#/ SSDA3/SSISCK0	PIXD7		
N3		P22	EDREQ0	MTIOC3B/MTCLKC/ GTIOC1A-B/TIOCC3/ TMO0/PO2	SCK0/ USB0_OVRCURB/ USBA_OVRCURB/ AUDIO_MCLK	PIXD6		
N4		P15		MTIOC0B/MTCLKB/ GTETRG-B/TIOCB2/ TCLKB/TMCI2/PO13	RXD1/SCK3/SMISO1/ SSCL1/CRX1-DS/ USBA_VBUSEN/ SSIWS1	PIXD0	IRQ5	
N5		P12	WR3#/BC3#	MTIC5U/TMCI1	RXD2/SMISO2/ SSCL2/ SCL0[FM+]		IRQ2	
N6	VSS_USB							
N7	VSS2_USBA							
N8	VSS1_USBA							
N9		P51	WR1#/BC1#/ WAIT#		SCK2/SSLB2-A			
N10	UB	PC7	A23/CS0#	MTIOC3A/MTCLKB/ GTIOC3A-D/TMO2/ TOC0/PO31/CACREF	TXD8/MISOA-A/ ET0_COL	MMC_D7-A	IRQ14	
N11		P82	EDREQ1	MTIOC4A/ GTIOC2A-D/PO28	TXD10/ET0_ETXD1/ RMII0_TXD1	MMC_D4-A		
N12		PC3	A19	MTIOC4D/ GTIOC1B-D/TCLKB/ PO24	TXD5/SMOSI5/ SSDA5/ET0_TX_ER	MMC_D0-A/ SDHI_D0-A/ QIO0-A/ QMO-A		
N13		PC0	A16	MTIOC3C/TCLKC/ PO17	CTS5#/RTS5#/SS5#/ SSLA1-A/ET0_ERXD3		IRQ14	
N14		P73	CS3#	PO16	ET0_WOL			

Table 1.5 List of Pins and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (6/7)

Pin Number 177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
N15	VSS							
P1	VSS							
P2		P17		MTIOC3A/MTIOC3B/ MTIOC4B/ GTIOC0B-B/TIOCB0/ TCLKD/TMO1/PO15/ POE8#	SCK1/TXD3/ SMOSI3/SSDA3/ SDA2-DS/ SSITXD0	PIXD3	IRQ7	ADTRG1#
P3		P87		MTIOC4C/ GTIOC1B-B/TIOCA2	TXD10	PIXD2		
P4		P14		MTIOC3A/MTCLKA/ TIOCB5/TCLKA/ TMRI2/PO15	CTS1#/RTS1#/ SS1#/CTX1/ USB0_OVRCURA		IRQ4	
P5					USB0_DP			
P6	AVSS_USBA							
P7					USBA_DM			
P8		P10	ALE	MTIC5W/TMRI3	USBA_OVRCURA		IRQ0	
P9		P52	RD#		RXD2/SMISO2/ SSCL2/SSLB3-A			
P10		P83	EDACK1	MTIOC4C/ GTIOC0A-D	CTS10#/ET0_CRS/ RMII0_CRS_DV/ SCK10			
P11		PC6	A22/CS1#	MTIOC3C/MTCLKA/ GTIOC3B-D/TMCI2/ TIC0/PO30	RXD8/MOSIA-A/ ET0_ETXD3	MMC_D6-A	IRQ13	
P12		PC4	A20/CS3#	MTIOC3D/MTCLKC/ GTETRG-D/TMCI1/ PO25/POE0#	SCK5/CTS8#/ SSLA0-A/ ET0_TX_CLK	MMC_D1-A/ SDHI_D1-A/ QIO1-A/QMI-A		
P13		PC2	A18	MTIOC4B/ GTIOC2B-D/TCLKA/ PO21	RXD5/SMISO5/ SSCL5/SSLA3-A/ ET0_RX_DV	MMC_CD-A/ SDHI_D3-A		
P14		P75	CS5#	PO20	SCK11/RTS11#/ ET0_ERXD0/ RMII0_RXD0	MMC_RES#-A/ SDHI_D2-A		
P15	VCC							
R1		P21		MTIOC1B/MTIOC4A/ GTIOC2A-B/TIOCA3/ TMCI0/PO1	RXD0/SMISO0/ SSCL0/ USB0_EXICEN/ USBA_EXICEN/ SSIWS0	PIXD5	IRQ9	
R2		P20		MTIOC1A/TIOCB3/ TMRI0/PO0	TXD0/SMOSI0/ SSDA0/USB0_ID/ USBA_ID/ SSIRXD0	PIXD4	IRQ8	
R3		P16		MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/ TMO2/PO14/ RTCOUT	TXD1/RXD3/ SMOSI1/SMISO3/ SSDA1/SSCL3/SCL2-DS/USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB		IRQ6	ADTRG0#
R4		P13	WR2#/BC2#	MTIOC0B/TIOCA5/ TMO3/PO13	TXD2/SMOSI2/ SSDA2/ SDA0[FM+]		IRQ3	ADTRG1#
R5					USB0_DM			
R6	PVSS_USBA							
R7					USBA_DP			
R8		P11		MTIC5V/TMCI3	SCK2/ USBA_VBUS/ USBA_VBUSEN		IRQ1	
R9		P53*2	BCLK					

Table 1.5 List of Pins and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (7/7)

Pin Number 177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
R10	VSS							
R11	VCC							
R12		P80	EDREQ0	MTIOC3B/PO26	SCK10/RTS10#/ ET0_TX_EN/ RMII0_TXD_EN	MMC_D2-A/ SDHI_WP-A/ QIO2-A		
R13		P76	CS6#	PO22	RXD11/ET0_RX_CLK/ REF50CK0	MMC_CMD-A/ SDHI_CMD-A/ QSSL-A		
R14		P74	A20/CS4#	PO19	CTS11#/ET0_ERXD1/ RMII0_RXD1			
R15		PC1	A17	MTIOC3A/TCLKD/ PO18	SCK5/SSLA2-A/ ET0_ERXD2		IRQ12	

Note 1. The 176-pin LFBGA does not include the E5 pin.
Note 2. The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.

1.6.2 176-Pin LFQFP

Table 1.6 List of Pins and Pin Functions (176-Pin LFQFP) (1/7)

Pin Number 176-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
1	AVSS0							
2		P05					IRQ13	DA1
3	AVCC1							
4		P03					IRQ11	DA0
5	AVSS1							
6		P02		TMCI1	SCK6		IRQ10	AN120
7		P01		TMCI0	RXD6/SMISO6/ SSCL6		IRQ9	AN119
8		P00		TMRI0	TXD6/SMOSI6/ SSDA6		IRQ8	AN118
9		PF5					IRQ4	
10	EMLE							
11		PJ5		POE8#	CTS2#/RTS2#/SS2#			
12	VSS							
13		PJ3	EDACK1	MTIOC3C	ET0_EXOUT/ CTS6#/RTS6#/ CTS0#/RTS0#/ SS6#/SS0#			
14	VCL							
15	VBATT							
16	NC							
17	TRST#	PF4						
18	MD/FINED							
19	XCIN							
20	XCOUT							
21	RES#							
22	XTAL	P37						
23	VSS							
24	EXTAL	P36						
25	VCC							
26	UPSEL	P35					NMI	
27		P34		MTIOC0A/TMCI3/ PO12/POE10#	SCK6/SCK0/ ET0_LINKSTA		IRQ4	
28		P33	EDREQ1	MTIOC0D/TIOCD0/ TMRI3/PO11/POE4#/ POE11#	RXD6/RXD0/ SMISO6/ SMISO0/SSCL6/ SSCL0/CRX0	PCKO	IRQ3-DS	
29		P32		MTIOC0C/TIOCC0/ TMO3/PO10/ RTCOUT/RTCIC2/ POE0#/POE10#	TXD6/TXD0/ SMOSI6/SMOSI0/ SSDA6/SSDA0/ CTX0/ USB0_VBUSEN	VSYNC	IRQ2-DS	
30	TMS	PF3						
31	TDI	PF2			RXD1/SMISO1/ SSCL1			
32		P31		MTIOC4D/TMCI2/ PO9/RTCIC1	CTS1#/RTS1#/ SS1#/ET1_MDC/ SSLB0-A		IRQ1-DS	
33		P30		MTIOC4B/TMRI3/ PO8/RTCIC0/POE8#	RXD1/SMISO1/ SSCL1/ET1_MDIO/ MISOB-A		IRQ0-DS	

Table 1.6 List of Pins and Pin Functions (176-Pin LFQFP) (2/7)

Pin Number 176-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
34	TCK	PF1			SCK1			
35	TDO	PF0			TXD1/SMOSI1/SSDA1			
36		P27	CS7#	MTIOC2B/TMCI3/PO7	SCK1/ET1_WOL/ RSPCKB-A			
37		P26	CS6#	MTIOC2A/TMO1/PO6	TXD1/CTS3#/ RTS3#/SMOSI1/ SS3#/SSDA1/ ET1_EXOUT/ MOSIB-A			
38		P25	CS5#/ EDACK1	MTIOC4C/MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/ SSCL3/ SSIDATA1	HSYNC		ADTRG0#
39	VCC							
40		P24	CS4#/ EDREQ1	MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4	SCK3/ USB0_VBUSEN/ SSISCK1	PIXCLK		
41	VSS							
42		P23	EDACK0	MTIOC3D/MTCLKD/ GTIOC0A-B/TIOCD3/ PO3	TXD3/CTS0#/ RTS0#/SMOSI3/ SS0#/SSDA3/ SSISCK0	PIXD7		
43		P22	EDREQ0	MTIOC3B/MTCLKC/ GTIOC1A-B/TIOCC3/ TMO0/PO2	SCK0/ USB0_OVRCURB/ USBA_OVRCURB/ AUDIO_MCLK	PIXD6		
44		P21		MTIOC1B/MTIOC4A/ GTIOC2A-B/TIOCA3/ TMCI0/PO1	RXD0/SMISO0/ SSCL0/ USB0_EXICEN/ USBA_EXICEN/ SSIWS0	PIXD5	IRQ9	
45		P20		MTIOC1A/TIOCB3/ TMRI0/PO0	TXD0/SMOSI0/ SSDA0/USB0_ID/ USBA_ID/ SSIRXD0	PIXD4	IRQ8	
46		P17		MTIOC3A/MTIOC3B/ MTIOC4B/ GTIOC0B-B/TIOCB0/ TCLKD/TMO1/PO15/ POE8#	SCK1/TXD3/ SMOSI3/SSDA3/ SDA2-DS/ SSITXD0	PIXD3	IRQ7	ADTRG1#
47		P87		MTIOC4C/ GTIOC1B-B/TIOCA2	TXD10	PIXD2		
48		P16		MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/ TMO2/PO14/ RTCOUT	TXD1/RXD3/ SMOSI1/SMISO3/ SSDA1/SSCL3/ SCL2-DS/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB		IRQ6	ADTRG0#
49		P86		MTIOC4D/ GTIOC2B-B/TIOCA0	RXD10	PIXD1		
50		P15		MTIOC0B/MTCLKB/ GTETRG-B/TIOCB2/ TCLKB/TMCI2/PO13	RXD1/SCK3/ SMISO1/SSCL1/ CRX1-DS/ USBA_VBUSEN/ SSIWS1	PIXD0	IRQ5	
51		P14		MTIOC3A/MTCLKA/ TIOCB5/TCLKA/ TMRI2/PO15	CTS1#/RTS1#/ SS1#/CTX1/ USB0_OVRCURA		IRQ4	
52		P13	WR2#/BC2#	MTIOC0B/TIOCA5/ TMO3/PO13	TXD2/SMOSI2/ SSDA2/ SDA0[FM+]		IRQ3	ADTRG1#
53		P12	WR3#/BC3#	MTIC5U/TMCI1	RXD2/SMISO2/ SSCL2/ SCL0[FM+]		IRQ2	

Table 1.6 List of Pins and Pin Functions (176-Pin LFQFP) (3/7)

Pin Number 176-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
54	VCC_USB							
55					USB0_DM			
56					USB0_DP			
57	VSS_USB							
58	AVCC_ USBA							
59	USBA_ RREF							
60	AVSS_ USBA							
61	PVSS_ USBA							
62	VSS2_ USBA							
63					USBA_DM			
64					USBA_DP			
65	VSS1_ USBA							
66	VCC_ USBA							
67		P11		MTIC5V/TMCI3	SCK2/USBA_VBUS/ USBA_VBUSEN		IRQ1	
68		P10	ALE	MTIC5W/TMRI3	USBA_OVRCURA		IRQ0	
69		P53*1	BCLK					
70		P52	RD#		RXD2/SMISO2/ SSCL2/SSLB3-A			
71		P51	WR1#/BC1#/ WAIT#		SCK2/SSLB2-A			
72		P50	WR0#/WR#		TXD2/SMOSI2/ SSDA2/SSLB1-A			
73	VSS							
74		P83	EDACK1	MTIOC4C/ GTIOC0A-D	CTS10#/ET0_CRS/ RMII0_CRS_DV/ SCK10			
75	VCC							
76	UB	PC7	A23/CS0#	MTIOC3A/MTCLKB/ GTIOC3A-D/TMO2/ TOC0/PO31/CACREF	TXD8/MISOA-A/ ET0_COL	MMC_D7-A	IRQ14	
77		PC6	A22/CS1#	MTIOC3C/MTCLKA/ GTIOC3B-D/TMCI2/ TIC0/PO30	RXD8/MOSIA-A/ ET0_ETXD3	MMC_D6-A	IRQ13	
78		PC5	A21/CS2#/ WAIT#	MTIOC3B/MTCLKD/ GTIOC1A-D/TMRI2/ PO29	SCK8/RSPCKA-A/ RTS8#/ET0_ETXD2	MMC_D5-A		
79		P82	EDREQ1	MTIOC4A/ GTIOC2A-D/PO28	TXD10/ET0_ETXD1/ RMII0_TXD1	MMC_D4-A		
80		P81	EDACK0	MTIOC3D/ GTIOC0B-D/PO27	RXD10/ET0_ETXD0/ RMII0_TXD0	MMC_D3-A/ SDHI_CD-A/ QIO3-A		
81		P80	EDREQ0	MTIOC3B/PO26	SCK10/RTS10#/ ET0_TX_EN/ RMII0_TXD_EN	MMC_D2-A/ SDHI_WP-A/ QIO2-A		
82		PC4	A20/CS3#	MTIOC3D/MTCLKC/ GTETRG-D/TMCI1/ PO25/POE0#	SCK5/CTS8#/SSLA0-A/ET0_TX_CLK	MMC_D1-A/ SDHI_D1-A/ QIO1-A/QMI-A		

Table 1.6 List of Pins and Pin Functions (176-Pin LFQFP) (4/7)

Pin Number 176-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
83		PC3	A19	MTIOC4D/ GTIOC1B-D/TCLKB/ PO24	TXD5/SMOSI5/ SSDA5/ ET0_TX_ER	MMC_D0-A/ SDHI_D0-A/ QIO0-A/ QMO-A		
84		P77	CS7#	PO23	TXD11/ET0_RX_ER/ RMII0_RX_ER	MMC_CLK-A/ SDHI_CLK-A/ QSPCLK-A		
85		P76	CS6#	PO22	RXD11/ET0_RX_CLK/ REF50CK0	MMC_CMD-A/ SDHI_CMD-A/ QSSL-A		
86		PC2	A18	MTIOC4B/ GTIOC2B-D/TCLKA/ PO21	RXD5/SMISO5/ SSCL5/SSLA3-A/ ET0_RX_DV	MMC_CD-A/ SDHI_D3-A		
87		P75	CS5#	PO20	SCK11/RTS11#/ ET0_ERXD0/ RMII0_RXD0	MMC_RES#-A/ SDHI_D2-A		
88		P74	A20/CS4#	PO19	CTS11#/ET0_ERXD1/ RMII0_RXD1			
89		PC1	A17	MTIOC3A/TCLKD/ PO18	SCK5/SSLA2-A/ ET0_ERXD2		IRQ12	
90	VCC							
91		PC0	A16	MTIOC3C/TCLKC/ PO17	CTS5#/RTS5#/SS5#/ SSLA1-A/ET0_ERXD3		IRQ14	
92	VSS							
93		P73	CS3#	PO16	ET0_WOL			
94		PB7	A15	MTIOC3B/TIOCB5/ PO31	TXD9/ET0_CRS/ RMII0_CRS_DV			
95		PB6	A14	MTIOC3D/TIOCA5/ PO30	RXD9/ET0_ETXD1/ RMII0_TXD1			
96		PB5	A13	MTIOC2A/MTIOC1B/ TIOCB4/TMRI1/PO29/ POE4#	SCK9/RTS9#/ ET0_ETXD0/ RMII0_TXD0			
97		PB4	A12	TIOCA4/PO28	CTS9#/ET0_TX_EN/ RMII0_TXD_EN			
98		PB3	A11	MTIOC0A/MTIOC4A/ TIOCD3/TCLKD/ TMO0/PO27/POE11#	SCK4/SCK6/ ET0_RX_ER/ RMII0_RX_ER			
99		PB2	A10	TIOCC3/TCLKC/ PO26	CTS4#/RTS4#/CTS6#/ RTS6#/SS4#/SS6#/ ET0_RX_CLK/ REF50CK0			
100		PB1	A9	MTIOC0C/MTIOC4C/ TIOCB3/TMCI0/PO25	TXD4/TXD6/SMOSI4/ SMOSI6/SSDA4/ SSDA6/ET0_ERXD0/ RMII0_RXD0		IRQ4-DS	
101		P72	A19/CS2#		ET0_MDC			
102		P71	A18/CS1#		ET0_MDIO			
103	VCC							
104		PB0	A8	MTIC5W/TIOCA3/ PO24	RXD4/RXD6/SMISO4/ SMISO6/SSCL4/ SSCL6/ET0_ERXD1/ RMII0_RXD1		IRQ12	
105	VSS							
106		PA7	A7	TIOCB2/PO23	MISOA-B/ ET0_WOL			
107		PA6	A6	MTIC5V/MTCLKB/ GTETRG-C/TIOCA2/ TMCI3/PO22/POE10#	CTS5#/RTS5#/SS5#/ MOSIA-B/ ET0_EXOUT			

Table 1.6 List of Pins and Pin Functions (176-Pin LFQFP) (5/7)

Pin Number 176-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
108		PA5	A5	MTIOC6B/ GTIOC0A-C/TIOCB1/ PO21	RSPCKA-B/ ET0_LINKSTA			
109		PA4	A4	MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20	TXD5/SMOSI5/ SSDA5/SSLA0-B/ ET0_MDC		IRQ5-DS	
110		PA3	A3	MTIOC0D/MTCLKD/ TIOCD0/TCLKB/PO19	RXD5/SMISO5/ SSCL5/ ET0_MDIO		IRQ6-DS	
111	TRDATA3	PG7	D31		ET1_TX_ER			
112		PA2	A2	MTIOC7A/ GTIOC1A-C/PO18	RXD5/SMISO5/ SSCL5/SSLA3-B			
113	TRDATA2	PG6	D30		ET1_ETXD3			
114		PA1	A1/DQM3	MTIOC0B/MTCLKC/ MTIOC7B/ GTIOC2A-C/TIOCB0/ PO17	SCK5/SSLA2-B/ ET0_WOL		IRQ11	
115	VCC							
116	TRCLK	PG5	D29		ET1_ETXD2			
117	VSS							
118		PA0	A0/BC0#/ DQM2	MTIOC4A/MTIOC6D/ GTIOC0B-C/TIOCA0/ CACREF/PO16	SSLA1-B/ ET0_TX_EN/ RMII0_TXD_EN			
119	TRSYNC	PG4	D28		ET1_ETXD1/ RMII1_TXD1			
120		P67	CS7#/DQM1	MTIOC7C/ GTIOC1B-C	CRX2		IRQ15	
121	TRDATA1	PG3	D27		ET1_ETXD0/ RMII1_TXD0			
122		P66	CS6#/DQM0	MTIOC7D/ GTIOC2B-C	CTX2			
123	TRDATA0	PG2	D26		ET1_TX_CLK			
124		P65	CS5#/CKE					
125		PE7	D15[A15/D15]	MTIOC6A/ GTIOC3A-E/TOC1	MISOB-B	MMC_RES#-B/ SDHI_WP-B	IRQ7	AN105
126		PE6	D14[A14/D14]	MTIOC6C/ GTIOC3B-E/TIC1	MOSIB-B	MMC_CD-B/ SDHI_CD-B	IRQ6	AN104
127	VCC							
128		P70	SDCLK					
129	VSS							
130		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B/ GTIOC0A-A	ET0_RX_CLK/ REF50CK0/ RSPCKB-B		IRQ5	AN103
131		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A/ GTIOC1A-A/PO28	ET0_ERXD2/SSLB0-B			AN102
132		PE3	D11[A11/D11]	MTIOC4B/ GTIOC2A-A/PO26/ POE8#/TOC3	CTS12#/RTS12#/ SS12#/ ET0_ERXD3	MMC_D7-B		AN101
133		PE2	D10[A10/D10]	MTIOC4A/ GTIOC0B-A/PO23/ TIC3	RXD12/SMISO12/ SSCL12/RXDX12/ SSLB3-B	MMC_D6-B	IRQ7-DS	AN100
134		PE1	D9[A9/D9]	MTIOC4C/MTIOC3B/ GTIOC1B-A/PO18	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/SSLB2-B	MMC_D5-B		ANEX1
135		PE0	D8[A8/D8]	MTIOC3D/ GTIOC2B-A	SCK12/SSLB1-B	MMC_D4-B		ANEX0
136		P64	CS4#/WE#					
137		P63	CS3#/CAS#					

Table 1.6 List of Pins and Pin Functions (176-Pin LFQFP) (6/7)

Pin Number 176-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
138		P62	CS2#/RAS#					
139		P61	CS1#/SDCS#					
140	VSS							
141		P60	CS0#		ET1_TX_EN/ RMII1_TXD_EN			
142	VCC							
143		PD7	D7[A7/D7]	MTIC5U/POE0#		MMC_D1-B/ SDHI_D1-B/ QIO1-B/QMI-B	IRQ7	AN107
144		PG1	D25		ET1_RX_ER/ RMII1_RX_ER			
145		PD6	D6[A6/D6]	MTIC5V/MTIOC8A/ POE4#		MMC_D0-B/ SDHI_D0-B/ QIO0-B/ QMO-B	IRQ6	AN106
146		PG0	D24		ET1_RX_CLK/ REF50CK1			
147		PD5	D5[A5/D5]	MTIC5W/MTIOC8C/ POE10#		MMC_CLK-B/ SDHI_CLK-B/ QSPCLK-B	IRQ5	AN113
148		PD4	D4[A4/D4]	MTIOC8B/POE11#		MMC_CMD-B/ SDHI_CMD-B/ QSSL-B	IRQ4	AN112
149		P97	A23/D23		ET1_ERXD3			
150		PD3	D3[A3/D3]	MTIOC8D/ GTIOC0A-E/POE8#/ TOC2		MMC_D3-B/ SDHI_D3-B/ QIO3-B	IRQ3	AN111
151	VSS							
152		P96	A22/D22		ET1_ERXD2			
153	VCC							
154		PD2	D2[A2/D2]	MTIOC4D/ GTIOC0B-E/TIC2	CRX0	MMC_D2-B/ SDHI_D2-B/ QIO2-B	IRQ2	AN110
155		P95	A21/D21		ET1_ERXD1/ RMII1_RXD1			
156		PD1	D1[A1/D1]	MTIOC4B/ GTIOC1A-E/POE0#	CTX0		IRQ1	AN109
157		P94	A20/D20		ET1_ERXD0/ RMII1_RXD0			
158		PD0	D0[A0/D0]	GTIOC1B-E/POE4#			IRQ0	AN108
159		P93	A19/D19	POE0#	ET1_LINKSTA/CTS7#/ RTS7#/SS7#			AN117
160		P92	A18/D18	POE4#	ET1_CRS/ RMII1_CRS_DV/ RXD7/SMISO7/SSCL7			AN116
161		P91	A17/D17		ET1_COL/SCK7			AN115
162	VSS							
163		P90	A16/D16		ET1_RX_DV/ TXD7/SMOSI7/SSDA7			AN114
164	VCC							
165		P47					IRQ15-DS	AN007
166		P46					IRQ14-DS	AN006
167		P45					IRQ13-DS	AN005

Table 1.6 List of Pins and Pin Functions (176-Pin LFQFP) (7/7)

Pin Number 176-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
168		P44					IRQ12-DS	AN004
169		P43					IRQ11-DS	AN003
170		P42					IRQ10-DS	AN002
171		P41					IRQ9-DS	AN001
172	VREFL0							
173		P40					IRQ8-DS	AN000
174	VREFH0							
175	AVCC0							
176		P07					IRQ15	ADTRG0#

Note 1. The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.

1.6.3 145-Pin TFLGA

Table 1.7 List of Pins and Pin Functions (145-Pin TFLGA) (1/5)

Pin Number 145-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
A1	AVSS0							
A2		P07					IRQ15	ADTRG0#
A3		P40					IRQ8-DS	AN000
A4		P42					IRQ10-DS	AN002
A5		P45					IRQ13-DS	AN005
A6		P90	A16		TXD7/SMOSI7/SSDA7			AN114
A7		P92	A18	POE4#	RXD7/SMISO7/SSCL7			AN116
A8		PD2	D2[A2/D2]	MTIOC4D/ GTIOC0B-E/TIC2	CRX0	MMC_D2-B/ SDHI_D2-B/ QIO2-B	IRQ2	AN110
A9		PD6	D6[A6/D6]	MTIC5V/MTIOC8A/ POE4#		MMC_D0-B/ SDHI_D0-B/ QIO0-B/ QMO-B	IRQ6	AN106
A10	VSS							
A11		P62	CS2#/RAS#					
A12		PE1	D9[A9/D9]	MTIOC4C/MTIOC3B/ GTIOC1B-A/PO18	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/SSLB2-B	MMC_D5-B		ANEX1
A13		PE3	D11[A11/D11]	MTIOC4B/ GTIOC2A-A/PO26/ POE8#/TOC3	CTS12#/RTS12#/ SS12#/ET0_ERXD3	MMC_D7-B		AN101
B1	AVCC1							
B2	AVCC0							
B3		P05					IRQ13	DA1
B4	VREFL0							
B5		P43					IRQ11-DS	AN003
B6		P47					IRQ15-DS	AN007
B7		P91	A17		SCK7			AN115
B8		PD0	D0[A0/D0]	GTIOC1B-E/POE4#			IRQ0	AN108
B9		PD4	D4[A4/D4]	MTIOC8B/POE11#		MMC_CMD-B/ SDHI_CMD-B/ QSSL-B	IRQ4	AN112
B10	VCC							
B11		P61	CS1#/SDCS#					
B12		PE2	D10[A10/D10]	MTIOC4A/ GTIOC0B-A/PO23/ TIC3	RXD12/SMISO12/ SSCL12/RXDX12/ SSLB3-B	MMC_D6-B	IRQ7-DS	AN100
B13		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A/ GTIOC1A-A/PO28	ET0_ERXD2/SSLB0-B			AN102
C1	AVSS1							
C2		P02		TMCI1	SCK6		IRQ10	AN120
C3	VREFH0							
C4		P41					IRQ9-DS	AN001
C5		P46					IRQ14-DS	AN006
C6	VSS							

Table 1.7 List of Pins and Pin Functions (145-Pin TFLGA) (2/5)

Pin Number 145-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
C7		PD1	D1[A1/D1]	MTIOC4B/ GTIOC1A-E/POE0#	CTX0		IRQ1	AN109
C8		PD3	D3[A3/D3]	MTIOC8D/ GTIOC0A-E/POE8#/ TOC2		MMC_D3-B/ SDHI_D3-B/ QIO3-B	IRQ3	AN111
C9		PD7	D7[A7/D7]	MTIC5U/POE0#		MMC_D1-B/ SDHI_D1-B/ QIO1-B/QMI-B	IRQ7	AN107
C10		P63	CS3#/CAS#					
C11		PE0	D8[A8/D8]	MTIOC3D/ GTIOC2B-A	SCK12/SSLB1-B	MMC_D4-B		ANEX0
C12		P70	SDCLK					
C13	VSS							
D1		P00		TMRI0	TXD6/SMOSI6/SSDA6		IRQ8	AN118
D2		PF5					IRQ4	
D3		P03					IRQ11	DA0
D4		P01		TMCI0	RXD6/SMISO6/SSCL6		IRQ9	AN119
D5	VCC							
D6		P93	A19	POE0#	CTS7#/RTS7#/SS7#			AN117
D7		PD5	D5[A5/D5]	MTIC5W/MTIOC8C/ POE10#		MMC_CLK-B/ SDHI_CLK-B/ QSPCLK-B	IRQ5	AN113
D8		P60	CS0#					
D9		P64	CS4#/WE#					
D10		PE7	D15[A15/D15]	MTIOC6A/ GTIOC3A-E/TOC1	MISOB-B	MMC_RES#-B/ SDHI_WP-B	IRQ7	AN105
D11	VCC							
D12		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B/ GTIOC0A-A	ET0_RX_CLK/ REF50CK0/ RSPCKB-B		IRQ5	AN103
D13		PE6	D14[A14/D14]	MTIOC6C/GTIOC3B-E/TIC1	MOSIB-B	MMC_CD-B/ SDHI_CD-B	IRQ6	AN104
E1	VSS							
E2	VCL							
E3		PJ5		POE8#	CTS2#/RTS2#/SS2#			
E4	EMLE							
E5		P44					IRQ12-DS	AN004
E10		PA0	A0/BC0#	MTIOC4A/MTIOC6D/ GTIOC0B-C/TIOCA0/ CACREF/PO16	SSLA1-B/ ET0_TX_EN/ RMII0_TXD_EN			
E11		P66	CS6#/DQM0	MTIOC7D/ GTIOC2B-C	CTX2			
E12		P65	CS5#/CKE					
E13		P67	CS7#/DQM1	MTIOC7C/ GTIOC1B-C	CRX2		IRQ15	
F1	XCIN							
F2	XCOUT							
F3		PJ3	EDACK1	MTIOC3C	ET0_EXOUT/CTS6#/ RTS6#/CTS0#/RTS0#/ SS6#/SS0#			
F4	VBATT							
F10		PA3	A3	MTIOC0D/MTCLKD/ TIOCD0/TCLKB/PO19	RXD5/SMISO5/ SSCL5/ET0_MDIO		IRQ6-DS	

Table 1.7 List of Pins and Pin Functions (145-Pin TFLGA) (3/5)

Pin Number 145-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
F11	VSS							
F12		PA1	A1	MTIOC0B/MTCLKC/ MTIOC7B/ GTIOC2A-C/TIOCB0/ PO17	SCK5/SSLA2-B/ ET0_WOL		IRQ11	
F13		PA2	A2	MTIOC7A/ GTIOC1A-C/PO18	RXD5/SMISO5/ SSCL5/SSLA3-B			
G1	XTAL	P37						
G2	RES							
G3	MD/FINED							
G4	BSCANP							
G10		PA5	A5	MTIOC6B/TIOCB1/ GTIOC0A-C/PO21	RSPCKA-B/ ET0_LINKSTA			
G11		PA6	A6	MTIC5V/MTCLKB/ GTETRG-C/TIOCA2/ TMCI3/PO22/POE10#	CTS5#/RTS5#/SS5#/ MOSIA-B/ ET0_EXOUT			
G12	VCC							
G13		PA4	A4	MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20	TXD5/SMOSI5/ SSDA5/SSLA0-B/ ET0_MDC		IRQ5-DS	
H1	EXTAL	P36						
H2	VCC							
H3	VSS							
H4	UPSEL	P35					NMI	
H10		P72	A19/CS2#		ET0_MDC			
H11		P71	A18/CS1#		ET0_MDIO			
H12		PB0	A8	MTIC5W/TIOCA3/ PO24	RXD4/RXD6/SMISO4/ SMISO6/SSCL4/ SSCL6/ET0_ERXD1/ RMII0_RXD1		IRQ12	
H13		PA7	A7	TIOCB2/PO23	MISOA-B/ET0_WOL			
J1	TRST#	P34		MTIOC0A/TMCI3/ PO12/POE10#	SCK6/SCK0/ ET0_LINKSTA		IRQ4	
J2		P33	EDREQ1	MTIOC0D/TIOCD0/ TMRI3/PO11/POE4#/ POE11#	RXD6/RXD0/SMISO6/ SMISO0/SSCL6/ SSCL0/CRX0	PCKO	IRQ3-DS	
J3		P32		MTIOC0C/TIOCC0/ TMO3/PO10/ RTCOUT/RTCIC2/ POE0#/POE10#	TXD6/TXD0/SMOSI6/ SMOSI0/SSDA6/ SSDA0/CTX0/ USB0_VBUSEN	VSYNC	IRQ2-DS	
J4	TDI	P30		MTIOC4B/TMRI3/ PO8/RTCIC0/POE8#	RXD1/SMISO1/ SSCL1/MISOB-A		IRQ0-DS	
J10		PB3	A11	MTIOC0A/MTIOC4A/ TIOCD3/TCLKD/ TMO0/PO27/POE11#	SCK4/SCK6/ ET0_RX_ER/ RMII0_RX_ER			
J11		PB4	A12	TIOCA4/PO28	CTS9#/ET0_TX_EN/ RMII0_TXD_EN			
J12		PB2	A10	TIOCC3/TCLKC/ PO26	CTS4#/RTS4#/CTS6#/ RTS6#/SS4#/SS6#/ ET0_RX_CLK/ REF50CK0			
J13		PB1	A9	MTIOC0C/MTIOC4C/ TIOCB3/TMCI0/PO25	TXD4/TXD6/SMOSI4/ SMOSI6/SSDA4/ SSDA6/ET0_ERXD0/ RMII0_RXD0		IRQ4-DS	
K1	TCK	P27	CS7#	MTIOC2B/TMCI3/PO7	SCK1/RSPCKB-A			

Table 1.7 List of Pins and Pin Functions (145-Pin TFLGA) (4/5)

Pin Number 145-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
K2	TDO	P26	CS6#	MTIOC2A/TMO1/PO6	TXD1/CTS3#/RTS3#/ SMOSI1/SS3#/ SSDA1/MOSIB-A			
K3	TMS	P31		MTIOC4D/TMCI2/ PO9/RTCIC1	CTS1#/RTS1#/SS1#/ SSLB0-A		IRQ1-DS	
K4		P15		MTIOC0B/MTCLKB/ GTETRG-B/TIOCB2/ TCLKB/TMCI2/PO13	RXD1/SCK3/SMISO1/ SSCL1/CRX1-DS/ SSIWS1	PIXD0	IRQ5	
K5	TRDATA2	P54	ALE/EDACK0	MTIOC4B/TMCI1	CTS2#/RTS2#/SS2#/ CTX1/ET0_LINKSTA			
K6		P53*1	BCLK					
K7		P51	WR1#/BC1#/ WAIT#		SCK2/SSLB2-A			
K8	VCC							
K9	TRDATA0	P80	EDREQ0	MTIOC3B/PO26	SCK10/RTS10#/ ET0_TX_EN/ RMII0_TXD_EN	MMC_D2-A/ SDHI_WP-A/ QIO2-A		
K10		P76	CS6#	PO22	RXD11/ET0_RX_CLK/ REF50CK0	MMC_CMD-A/ SDHI_CMD-A/ QSSL-A		
K11		PB7	A15	MTIOC3B/TIOCB5/ PO31	TXD9/ET0_CRS/ RMII0_CRS_DV			
K12		PB6	A14	MTIOC3D/TIOCA5/ PO30	RXD9/ET0_ETXD1/ RMII0_TXD1			
K13		PB5	A13	MTIOC2A/MTIOC1B/ TIOCB4/TMRI1/PO29/ POE4#	SCK9/RTS9#/ ET0_ETXD0/ RMII0_TXD0			
L1		P25	CS5#/ EDACK1	MTIOC4C/MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/ SSCL3/SSIDATA1	HSYNC		ADTRG0#
L2		P23	EDACK0	MTIOC3D/MTCLKD/ GTIOC0A-B/TIOCD3/ PO3	TXD3/CTS0#/RTS0#/ SMOSI3/SS0#/ SSDA3/SSISCK0	PIXD7		
L3		P16		MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/ TMO2/PO14/ RTCOUT	TXD1/RXD3/SMOSI1/ SMISO3/SSDA1/ SSCL3/SCL2-DS/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB		IRQ6	ADTRG0#
L4		P24	CS4#/ EDREQ1	MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4	SCK3/ USB0_VBUSEN/ SSISCK1	PIXCLK		
L5		P13		MTIOC0B/TIOCA5/ TMO3/PO13	TXD2/SMOSI2/ SSDA2/SDA0[FM+]		IRQ3	ADTRG1#
L6		P56	EDACK1	MTIOC3C/TIOCA1				
L7		P52	RD#		RXD2/SMISO2/ SSCL2/SSLB3-A			
L8	TRCLK	P83	EDACK1	MTIOC4C/ GTIOC0A-D	CTS10#/ET0_CRS/ RMII0_CRS_DV/ SCK10			
L9		PC5	A21/CS2#/ WAIT#	MTIOC3B/MTCLKD/ GTIOC1A-D/TMRI2/ PO29	SCK8/RSPCKA-A/ RTS8#/ET0_ETXD2	MMC_D5-A		
L10		PC4	A20/CS3#	MTIOC3D/MTCLKC/ GTETRG-D/TMCI1/ PO25/POE0#	SCK5/CTS8#/ SSLA0-A/ ET0_TX_CLK	MMC_D1-A/ SDHI_D1-A/ QIO1-A/QMI-A		
L11		PC2	A18	MTIOC4B/ GTIOC2B-D/TCLKA/ PO21	RXD5/SMISO5/ SSCL5/SSLA3-A/ ET0_RX_DV	MMC_CD-A/ SDHI_D3-A		
L12		P73	CS3#	PO16	ET0_WOL			
L13	VSS							

Table 1.7 List of Pins and Pin Functions (145-Pin TFLGA) (5/5)

Pin Number 145-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
M1		P22	EDREQ0	MTIOC3B/MTCLKC/ GTIOC1A-B/TIOCC3/ TMO0/PO2	SCK0/ USB0_OVRCURB/ AUDIO_MCLK	PIXD6		
M2		P17		MTIOC3A/MTIOC3B/ MTIOC4B/ GTIOC0B-B/TIOCB0/ TCLKD/TMO1/PO15/ POE8#	SCK1/TXD3/SMOSI3/ SSDA3/SDA2-DS/ SSITXD0	PIXD3	IRQ7	ADTRG1#
M3		P86		MTIOC4D/ GTIOC2B-B/TIOCA0	RXD10	PIXD1		
M4		P12		TMCI1	RXD2/SMISO2/ SSCL2/SCL0[FM+]		IRQ2	
M5	VCC_USB							
M6	VSS_USB							
M7		P50	WR0#/WR#		TXD2/SMOSI2/ SSDA2/SSLB1-A			
M8		PC6	A22/CS1#	MTIOC3C/MTCLKA/ GTIOC3B-D/TMCI2/ TIC0/PO30	RXD8/MOSIA-A/ ET0_ETXD3	MMC_D6-A	IRQ13	
M9	TRDATA1	P81	EDACK0	MTIOC3D/ GTIOC0B-D/PO27	RXD10/ET0_ETXD0/ RMII0_TXD0	MMC_D3-A/ SDHI_CD-A/ QIO3-A		
M10		P77	CS7#	PO23	TXD11/ET0_RX_ER/ RMII0_RX_ER	MMC_CLK-A/ SDHI_CLK-A/ QSPCLK-A		
M11		PC0	A16	MTIOC3C/TCLKC/ PO17	CTS5#/RTS5#/SS5#/ SSLA1-A/ET0_ERXD3		IRQ14	
M12		PC1	A17	MTIOC3A/TCLKD/ PO18	SCK5/SSLA2-A/ ET0_ERXD2		IRQ12	
M13	VCC							
N1		P21		MTIOC1B/MTIOC4A/ GTIOC2A-B/TIOCA3/ TMCI0/PO1	RXD0/SMISO0/SSCL0/ USB0_EXICEN/ SSIWS0	PIXD5	IRQ9	
N2		P20		MTIOC1A/TIOCB3/ TMRI0/PO0	TXD0/SMOSI0/ SSDA0/USB0_ID/ SSIRXD0	PIXD4	IRQ8	
N3		P87		MTIOC4C/ GTIOC1B-B/TIOCA2	TXD10	PIXD2		
N4		P14		MTIOC3A/MTCLKA/ TIOCB5/TCLKA/ TMRI2/PO15	CTS1#/RTS1#/SS1#/ CTX1/ USB0_OVRCURA		IRQ4	
N5					USB0_DM			
N6					USB0_DP			
N7	TRDATA3	P55	WAIT#/ EDREQ0	MTIOC4D/TMO3	CRX1/ET0_EXOUT		IRQ10	
N8	VSS							
N9	UB	PC7	A23/CS0#	MTIOC3A/MTCLKB/ GTIOC3A-D/TMO2/ TOC0/PO31/CACREF	TXD8/MISOA-A/ ET0_COL	MMC_D7-A	IRQ14	
N10	TRSYNC	P82	EDREQ1	MTIOC4A/ GTIOC2A-D/PO28	TXD10/ET0_ETXD1/ RMII0_TXD1	MMC_D4-A		
N11		PC3	A19	MTIOC4D/ GTIOC1B-D/TCLKB/ PO24	TXD5/SMOSI5/ SSDA5/ET0_TX_ER	MMC_D0-A/ SDHI_D0-A/ QIO0-A/ QMO-A		
N12		P75	CS5#	PO20	SCK11/RTS11#/ ET0_ERXD0/ RMII0_RXD0	MMC_RES#-A/ SDHI_D2-A		
N13		P74	A20/CS4#	PO19	CTS11#/ET0_ERXD1/ RMII0_RXD1			

Note 1. The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.

1.6.4 144-Pin LFQFP

Table 1.8 List of Pins and Pin Functions (144-Pin LFQFP) (1/5)

Pin Number 144-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
1	AVSS0							
2		P05					IRQ13	DA1
3	AVCC1							
4		P03					IRQ11	DA0
5	AVSS1							
6		P02		TMCI1	SCK6		IRQ10	AN120
7		P01		TMCI0	RXD6/SMISO6/SSCL6		IRQ9	AN119
8		P00		TMRI0	TXD6/SMOSI6/SSDA6		IRQ8	AN118
9		PF5					IRQ4	
10	EMLE							
11		PJ5		POE8#	CTS2#/RTS2#/SS2#			
12	VSS							
13		PJ3	EDACK1	MTIOC3C	ET0_EXOUT/CTS6#/ RTS6#/CTS0#/RTS0#/ SS6#/SS0#			
14	VCL							
15	VBATT							
16	MD/FINED							
17	XCIN							
18	XCOUT							
19	RES							
20	XTAL	P37						
21	VSS							
22	EXTAL	P36						
23	VCC							
24	UPSEL	P35					NMI	
25	TRST#	P34		MTIOC0A/TMCI3/ PO12/POE10#	SCK6/SCK0/ ET0_LINKSTA		IRQ4	
26		P33	EDREQ1	MTIOC0D/TIOCD0/ TMRI3/PO11/POE4#/ POE11#	RXD6/RXD0/SMISO6/ SMISO0/SSCL6/ SSCL0/CRX0	PCKO	IRQ3-DS	
27		P32		MTIOC0C/TIOCC0/ TMO3/PO10/ RTCOUT/RTCIC2/ POE0#/POE10#	TXD6/TXD0/SMOSI6/ SMOSI0/SSDA6/ SSDA0/CTX0/ USB0_VBUSEN	VSYNC	IRQ2-DS	
28	TMS	P31		MTIOC4D/TMCI2/ PO9/RTCIC1	CTS1#/RTS1#/SS1#/ SSLB0-A		IRQ1-DS	
29	TDI	P30		MTIOC4B/TMRI3/ PO8/RTCIC0/POE8#	RXD1/SMISO1/ SSCL1/MISOB-A		IRQ0-DS	
30	TCK	P27	CS7#	MTIOC2B/TMCI3/PO7	SCK1/RSPCKB-A			
31	TDO	P26	CS6#	MTIOC2A/TMO1/PO6	TXD1/CTS3#/RTS3#/ SMOSI1/SS3#/ SSDA1/MOSIB-A			
32		P25	CS5#/ EDACK1	MTIOC4C/MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/ SSCL3/SSIDATA1	HSYNC		ADTRG0#
33		P24	CS4#/ EDREQ1	MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4	SCK3/ USB0_VBUSEN/ SSISCK1	PIXCLK		
34		P23	EDACK0	MTIOC3D/MTCLKD/ GTIOC0A-B/TIOCD3/ PO3	TXD3/CTS0#/RTS0#/ SMOSI3/SS0#/ SSDA3/SSISCK0	PIXD7		

Table 1.8 List of Pins and Pin Functions (144-Pin LFQFP) (2/5)

Pin Number 144-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
35		P22	EDREQ0	MTIOC3B/MTCLKC/ GTIOC1A-B/TIOCC3/ TMO0/PO2	SCK0/ USB0_OVRCURB/ AUDIO_MCLK	PIXD6		
36		P21		MTIOC1B/MTIOC4A/ GTIOC2A-B/TIOCA3/ TMCI0/PO1	RXD0/SMISO0/ SSCL0/ USB0_EXICEN/ SSIWS0	PIXD5	IRQ9	
37		P20		MTIOC1A/TIOCB3/ TMRI0/PO0	TXD0/SMOSI0/ SSDA0/USB0_ID/ SSIRXD0	PIXD4	IRQ8	
38		P17		MTIOC3A/MTIOC3B/ MTIOC4B/ GTIOC0B-B/TIOCB0/ TCLKD/TMO1/PO15/ POE8#	SCK1/TXD3/SMOSI3/ SSDA3/SDA2-DS/ SSITXD0	PIXD3	IRQ7	ADTRG1#
39		P87		MTIOC4C/ GTIOC1B-B/TIOCA2	TXD10	PIXD2		
40		P16		MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/ TMO2/PO14/ RTCOUT	TXD1/RXD3/SMOSI1/ SMISO3/SSDA1/ SSCL3/SCL2-DS/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB		IRQ6	ADTRG0#
41		P86		MTIOC4D/ GTIOC2B-B/TIOCA0	RXD10	PIXD1		
42		P15		MTIOC0B/MTCLKB/ GTETRG-B/TIOCB2/ TCLKB/TMCI2/PO13	RXD1/SCK3/SMISO1/ SSCL1/CRX1-DS/ SSIWS1	PIXD0	IRQ5	
43		P14		MTIOC3A/MTCLKA/ TIOCB5/TCLKA/ TMRI2/PO15	CTS1#/RTS1#/SS1#/ CTX1/ USB0_OVRCURA		IRQ4	
44		P13		MTIOC0B/TIOCA5/ TMO3/PO13	TXD2/SMOSI2/ SSDA2/SDA0[FM+]		IRQ3	ADTRG1#
45		P12		TMCI1	RXD2/SMISO2/ SSCL2/SCL0[FM+]		IRQ2	
46	VCC_USB							
47					USB0_DM			
48					USB0_DP			
49	VSS_USB							
50		P56	EDACK1	MTIOC3C/TIOCA1				
51	TRDATA3	P55	WAIT#/ EDREQ0	MTIOC4D/TMO3	CRX1/ET0_EXOUT		IRQ10	
52	TRDATA2	P54	ALE/EDACK0	MTIOC4B/TMCI1	CTS2#/RTS2#/SS2#/ CTX1/ET0_LINKSTA			
53		P53*1	BCLK					
54		P52	RD#		RXD2/SMISO2/ SSCL2/SSLB3-A			
55		P51	WR1#/BC1#/ WAIT#		SCK2/SSLB2-A			
56		P50	WR0#/WR#		TXD2/SMOSI2/ SSDA2/SSLB1-A			
57	VSS							
58	TRCLK	P83	EDACK1	MTIOC4C/ GTIOC0A-D	CTS10#/ET0_CRS/ RMII0_CRS_DV/ SCK10			
59	VCC							
60	UB	PC7	A23/CS0#	MTIOC3A/MTCLKB/ GTIOC3A-D/TMO2/ TOC0/PO31/CACREF	TXD8/MISOA-A/ ET0_COL	MMC_D7-A	IRQ14	

Table 1.8 List of Pins and Pin Functions (144-Pin LFQFP) (3/5)

Pin Number 144-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
61		PC6	A22/CS1#	MTIOC3C/MTCLKA/ GTIOC3B-D/TMCI2/ TIC0/PO30	RXD8/MOSIA-A/ ET0_ETXD3	MMC_D6-A	IRQ13	
62		PC5	A21/CS2#/ WAIT#	MTIOC3B/MTCLKD/ GTIOC1A-D/TMRI2/ PO29	SCK8/RSPCKA-A/ RTS8#/ET0_ETXD2	MMC_D5-A		
63	TRSYNC	P82	EDREQ1	MTIOC4A/ GTIOC2A-D/PO28	TXD10/ET0_ETXD1/ RMII0_TXD1	MMC_D4-A		
64	TRDATA1	P81	EDACK0	MTIOC3D/ GTIOC0B-D/PO27	RXD10/ET0_ETXD0/ RMII0_TXD0	MMC_D3-A/ SDHI_CD-A/ QIO3-A		
65	TRDATA0	P80	EDREQ0	MTIOC3B/PO26	SCK10/RTS10#/ ET0_TX_EN/ RMII0_TXD_EN	MMC_D2-A/ SDHI_WP-A/ QIO2-A		
66		PC4	A20/CS3#	MTIOC3D/MTCLKC/ GTETRG-D/TMCI1/ PO25/POE0#	SCK5/CTS8#/ SSLA0-A/ ET0_TX_CLK	MMC_D1-A/ SDHI_D1-A/ QIO1-A/QMI-A		
67		PC3	A19	MTIOC4D/ GTIOC1B-D/TCLKB/ PO24	TXD5/SMOSI5/ SSDA5/ET0_TX_ER	MMC_D0-A/ SDHI_D0-A/ QIO0-A/ QMO-A		
68		P77	CS7#	PO23	TXD11/ET0_RX_ER/ RMII0_RX_ER	MMC_CLK-A/ SDHI_CLK-A/ QSPCLK-A		
69		P76	CS6#	PO22	RXD11/ET0_RX_CLK/ REF50CK0	MMC_CMD-A/ SDHI_CMD-A/ QSSL-A		
70		PC2	A18	MTIOC4B/ GTIOC2B-D/TCLKA/ PO21	RXD5/SMISO5/ SSCL5/SSLA3-A/ ET0_RX_DV	MMC_CD-A/ SDHI_D3-A		
71		P75	CS5#	PO20	SCK11/RTS11#/ ET0_ERXD0/ RMII0_RXD0	MMC_RES#-A/ SDHI_D2-A		
72		P74	A20/CS4#	PO19	CTS11#/ET0_ERXD1/ RMII0_RXD1			
73		PC1	A17	MTIOC3A/TCLKD/ PO18	SCK5/SSLA2-A/ ET0_ERXD2		IRQ12	
74	VCC							
75		PC0	A16	MTIOC3C/TCLKC/ PO17	CTS5#/RTS5#/SS5#/ SSLA1-A/ET0_ERXD3		IRQ14	
76	VSS							
77		P73	CS3#	PO16	ET0_WOL			
78		PB7	A15	MTIOC3B/TIOCB5/ PO31	TXD9/ET0_CRS/ RMII0_CRS_DV			
79		PB6	A14	MTIOC3D/TIOCA5/ PO30	RXD9/ET0_ETXD1/ RMII0_TXD1			
80		PB5	A13	MTIOC2A/MTIOC1B/ TIOCB4/TMRI1/PO29/ POE4#	SCK9/RTS9#/ ET0_ETXD0/ RMII0_TXD0			
81		PB4	A12	TIOCA4/PO28	CTS9#/ET0_TX_EN/ RMII0_TXD_EN			
82		PB3	A11	MTIOC0A/MTIOC4A/ TIOCD3/TCLKD/ TMO0/PO27/POE11#	SCK4/SCK6/ ET0_RX_ER/ RMII0_RX_ER			
83		PB2	A10	TIOCC3/TCLKC/ PO26	CTS4#/RTS4#/CTS6#/ RTS6#/SS4#/SS6#/ ET0_RX_CLK/ REF50CK0			
84		PB1	A9	MTIOC0C/MTIOC4C/ TIOCB3/TMCI0/PO25	TXD4/TXD6/SMOSI4/ SMOSI6/SSDA4/ SSDA6/ET0_ERXD0/ RMII0_RXD0		IRQ4-DS	

Table 1.8 List of Pins and Pin Functions (144-Pin LFQFP) (4/5)

Pin Number 144-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
85		P72	A19/CS2#		ET0_MDC			
86		P71	A18/CS1#		ET0_MDIO			
87		PB0	A8	MTIC5W/TIOCA3/ PO24	RXD4/RXD6/SMISO4/ SMISO6/SSCL4/ SSCL6/ET0_ERXD1/ RMII0_RXD1		IRQ12	
88		PA7	A7	TIOCB2/PO23	MISOA-B/ET0_WOL			
89		PA6	A6	MTIC5V/MTCLKB/ GTETRG-C/TIOCA2/ TMCI3/PO22/POE10#	CTS5#/RTS5#/SS5#/ MOSIA-B/ ET0_EXOUT			
90		PA5	A5	MTIOC6B/TIOCB1/ GTIOC0A-C/PO21	RSPCKA-B/ ET0_LINKSTA			
91	VCC							
92		PA4	A4	MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20	TXD5/SMOSI5/ SSDA5/SSLA0-B/ ET0_MDC		IRQ5-DS	
93	VSS							
94		PA3	A3	MTIOC0D/MTCLKD/ TIOCD0/TCLKB/PO19	RXD5/SMISO5/ SSCL5/ET0_MDIO		IRQ6-DS	
95		PA2	A2	MTIOC7A/ GTIOC1A-C/PO18	RXD5/SMISO5/ SSCL5/SSLA3-B			
96		PA1	A1	MTIOC0B/MTCLKC/ MTIOC7B/ GTIOC2A-C/TIOCB0/ PO17	SCK5/SSLA2-B/ ET0_WOL		IRQ11	
97		PA0	A0/BC0#	MTIOC4A/MTIOC6D/ GTIOC0B-C/TIOCA0/ CACREF/PO16	SSLA1-B/ ET0_TX_EN/ RMII0_TXD_EN			
98		P67	CS7#/DQM1	MTIOC7C/ GTIOC1B-C	CRX2		IRQ15	
99		P66	CS6#/DQM0	MTIOC7D/ GTIOC2B-C	CTX2			
100		P65	CS5#/CKE					
101		PE7	D15[A15/D15]	MTIOC6A/ GTIOC3A-E/TOC1	MISOB-B	MMC_RES#-B/ SDHI_WP-B	IRQ7	AN105
102		PE6	D14[A14/D14]	MTIOC6C/GTIOC3B-E/TIC1	MOSIB-B	MMC_CD-B/ SDHI_CD-B	IRQ6	AN104
103	VCC							
104		P70	SDCLK					
105	VSS							
106		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B/ GTIOC0A-A	ET0_RX_CLK/ REF50CK0/ RSPCKB-B		IRQ5	AN103
107		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A/ GTIOC1A-A/PO28	ET0_ERXD2/SSLB0-B			AN102
108		PE3	D11[A11/D11]	MTIOC4B/ GTIOC2A-A/PO26/ POE8#/TOC3	CTS12#/RTS12#/ SS12#/ET0_ERXD3	MMC_D7-B		AN101
109		PE2	D10[A10/D10]	MTIOC4A/ GTIOC0B-A/PO23/ TIC3	RXD12/SMISO12/ SSCL12/RXDX12/ SSLB3-B	MMC_D6-B	IRQ7-DS	AN100
110		PE1	D9[A9/D9]	MTIOC4C/MTIOC3B/ GTIOC1B-A/PO18	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/SSLB2-B	MMC_D5-B		ANEX1
111		PE0	D8[A8/D8]	MTIOC3D/ GTIOC2B-A	SCK12/SSLB1-B	MMC_D4-B		ANEX0
112		P64	CS4#/WE#					
113		P63	CS3#/CAS#					

Table 1.8 List of Pins and Pin Functions (144-Pin LFQFP) (5/5)

Pin Number 144-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
114		P62	CS2#/RAS#					
115		P61	CS1#/SDCS#					
116	VSS							
117		P60	CS0#					
118	VCC							
119		PD7	D7[A7/D7]	MTIC5U/POE0#		MMC_D1-B/ SDHI_D1-B/ QIO1-B/QMI-B	IRQ7	AN107
120		PD6	D6[A6/D6]	MTIC5V/MTIOC8A/ POE4#		MMC_D0-B/ SDHI_D0-B/ QIO0-B/QMO-B	IRQ6	AN106
121		PD5	D5[A5/D5]	MTIC5W/MTIOC8C/ POE10#		MMC_CLK-B/ SDHI_CLK-B/ QSPCLK-B	IRQ5	AN113
122		PD4	D4[A4/D4]	MTIOC8B/POE11#		MMC_CMD-B/ SDHI_CMD-B/ QSSL-B	IRQ4	AN112
123		PD3	D3[A3/D3]	MTIOC8D/ GTIOC0A-E/POE8#/ TOC2		MMC_D3-B/ SDHI_D3-B/ QIO3-B	IRQ3	AN111
124		PD2	D2[A2/D2]	MTIOC4D/ GTIOC0B-E/TIC2	CRX0	MMC_D2-B/ SDHI_D2-B/ QIO2-B	IRQ2	AN110
125		PD1	D1[A1/D1]	MTIOC4B/ GTIOC1A-E/POE0#	CTX0		IRQ1	AN109
126		PD0	D0[A0/D0]	GTIOC1B-E/POE4#			IRQ0	AN108
127		P93	A19	POE0#	CTS7#/RTS7#/SS7#			AN117
128		P92	A18	POE4#	RXD7/SMISO7/SSCL7			AN116
129		P91	A17		SCK7			AN115
130	VSS							
131		P90	A16		TXD7/SMOSI7/SSDA7			AN114
132	VCC							
133		P47					IRQ15-DS	AN007
134		P46					IRQ14-DS	AN006
135		P45					IRQ13-DS	AN005
136		P44					IRQ12-DS	AN004
137		P43					IRQ11-DS	AN003
138		P42					IRQ10-DS	AN002
139		P41					IRQ9-DS	AN001
140	VREFL0							
141		P40					IRQ8-DS	AN000
142	VREFH0							
143	AVCC0							
144		P07					IRQ15	ADTRG0#

Note 1. The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.

1.6.5 100-Pin TFLGA

Table 1.9 List of Pins and Pin Functions (100-Pin TFLGA) (1/4)

Pin Number 100-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF)	Interrupt	S12ADC, R12DA
A1	P05						IRQ13	DA1
A2	AVCC1							
A3		P07					IRQ15	ADTRG0#
A4	VREFL0							
A5		P43					IRQ11-DS	AN003
A6		PD0	D0[A0/D0]	GTIOC1B-E/POE4#			IRQ0	AN108
A7		PD4	D4[A4/D4]	MTIOC8B/POE11#		MMC_CMD-B/ SDHI_CMD-B/ QSSL-B	IRQ4	AN112
A8		PE0	D8[A8/D8]	MTIOC3D/GTIOC2B-A	SCK12/SSLB1-B	MMC_D4-B		ANEX0
A9		PE1	D9[A9/D9]	MTIOC4C/MTIOC3B/ GTIOC1B-A/PO18	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/SSLB2-B	MMC_D5-B		ANEX1
A10		PE2	D10[A10/ D10]	MTIOC4A/GTIOC0B-A/PO23/TIC3	RXD12/SMISO12/ SSCL12/RXDX12/ SSLB3-B	MMC_D6-B	IRQ7-DS	AN100
B1	EMLE							
B2	AVSS0							
B3	AVCC0							
B4		P40					IRQ8-DS	AN000
B5		P44					IRQ12-DS	AN004
B6		PD1	D1[A1/D1]	MTIOC4B/GTIOC1A-E/POE0#	CTX0		IRQ1	AN109
B7		PD3	D3[A3/D3]	MTIOC8D/GTIOC0A-E/POE8#/TOC2		MMC_D3-B/ SDHI_D3-B/ QIO3-B	IRQ3	AN111
B8		PD6	D6[A6/D6]	MTIC5V/MTIOC8A/ POE4#		MMC_D0-B/ SDHI_D0-B/ QIO0-B/QMO-B	IRQ6	AN106
B9		PD7	D7[A7/D7]	MTIC5U/POE0#		MMC_D1-B/ SDHI_D1-B/ QIO1/QMI-B	IRQ7	AN107
B10		PE3	D11[A11/ D11]	MTIOC4B/GTIOC2A-A/PO26/POE8#/TOC3	CTS12#/RTS12#/ SS12#/ET0_ERXD3	MMC_D7-B		AN101
C1	VCL							
C2	AVSS1							
C3		PJ3	EDACK1	MTIOC3C	ET0_EXOUT/CTS6#/ RTS6#/CTS0#/RTS0#/ SS6#/SS0#			
C4	VREFH0							
C5		P42					IRQ10-DS	AN002
C6		P47					IRQ15-DS	AN007
C7		PD2	D2[A2/D2]	MTIOC4D/GTIOC0B-E/TIC2	CRX0	MMC_D2-B/ SDHI_D2-B/ QIO2-B	IRQ2	AN110
C8		PD5	D5[A5/D5]	MTIC5W/MTIOC8C/ POE10#		MMC_CLK-B/ SDHI_CLK-B/ QSPCLK-B	IRQ5	AN113

Table 1.9 List of Pins and Pin Functions (100-Pin TFLGA) (2/4)

Pin Number 100-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF)	Interrupt	S12ADC, R12DA
C9		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B/GTIOC0A-A	ET0_RX_CLK/REF50CK0/RSPCKB-B		IRQ5	AN103
C10		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A/GTIOC1A-A/PO28	ET0_ERXD2/SSLB0-B			AN102
D1	XCIN							
D2	XCOUT							
D3	MD/FINED							
D4	VBATT							
D5		P45					IRQ13-DS	AN005
D6		P46					IRQ14-DS	AN006
D7		PE6	D14[A14/D14]	MTIOC6C/GTIOC3B-E/TIC1	MOSIB-B	MMC_CD-B/SDHI_CD-B	IRQ6	AN104
D8		PE7	D15[A15/D15]	MTIOC6A/GTIOC3A-E/TOC1	MISOB-B	MMC_RES#-B/SDHI_WP-B	IRQ7	AN105
D9		PA1	A1	MTIOC0B/MTCLKC/MTIOC7B/GTIOC2A-C/TIOCB0/PO17	SCK5/SSLA2-B/ET0_WOL		IRQ11	
D10		PA0	A0/BC0#	MTIOC4A/MTIOC6D/GTIOC0B-C/TIOCA0/CACREF/PO16	SSLA1-B/ET0_TX_EN/RMII0_TXD_EN			
E1	XTAL	P37						
E2	VSS							
E3	RES#							
E4	TRST#	P34		MTIOC0A/TMCI3/PO12/POE10#	SCK6/SCK0/ET0_LINKSTA		IRQ4	
E5		P41					IRQ9-DS	AN001
E6		PA2	A2	MTIOC7A/GTIOC1A-C/PO18	RXD5/SMISO5/SSCL5/SSLA3-B			
E7		PA6	A6	MTIC5V/MTCLKB/GTETRG-C/TIOCA2/TMCI3/PO22/POE10#	CTS5#/RTS5#/SS5#/MOSIA-B/ET0_EXOUT			
E8		PA4	A4	MTIC5U/MTCLKA/TIOCA1/TMRI0/PO20	TXD5/SMOSI5/SSDA5/SSLA0-B/ET0_MDC		IRQ5-DS	
E9		PA5	A5	MTIOC6B/TIOCB1/GTIOC0A-C/PO21	RSPCKA-B/ET0_LINKSTA			
E10		PA3	A3	MTIOC0D/MTCLKD/TIOCD0/TCLKB/PO19	RXD5/SMISO5/SSCL5/ET0_MDIO		IRQ6-DS	
F1	EXTAL	P36						
F2	VCC							
F3	UPSEL	P35					NMI	
F4		P32		MTIOC0C/TIOCC0/TMO3/PO10/RTCOUT/RTCIC2/POE0#/POE10#	TXD6/TXD0/SMOSI6/SMOSI0/SSDA6/SSDA0/CTX0/USB0_VBUSEN		IRQ2-DS	
F5		P12		TMCI1	RXD2/SMISO2/SSCL2/SCL0[FM+]		IRQ2	
F6		PB3	A11	MTIOC0A/MTIOC4A/TIOCD3/TCLKD/TMO0/PO27/POE11#	SCK6/ET0_RX_ER/RMII0_RX_ER			
F7		PB2	A10	TIOCC3/TCLKC/PO26	CTS6#/RTS6#/SS6#/ET0_RX_CLK/REF50CK0			

Table 1.9 List of Pins and Pin Functions (100-Pin TFLGA) (3/4)

Pin Number 100-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF)	Interrupt	S12ADC, R12DA
F8		PB0	A8	MTIC5W/TIOCA3/ PO24	RXD6/SMISO6/ SSCL6/ET0_ERXD1/ RMII0_RXD1		IRQ12	
F9		PA7	A7	TIOCB2/PO23	MISOA-B/ET0_WOL			
F10	VSS							
G1		P33	EDREQ1	MTIOC0D/TIOCD0/ TMRI3/PO11/POE4#/ POE11#	RXD6/RXD0/SMISO6/ SMISO0/SSCL6/ SSCL0/CRX0		IRQ3-DS	
G2	TMS	P31		MTIOC4D/TMCI2/ PO9/RTCIC1	CTS1#/RTS1#/SS1#/ SSLB0-A		IRQ1-DS	
G3	TDI	P30		MTIOC4B/TMRI3/ PO8/RTCIC0/POE8#	RXD1/SMISO1/ SSCL1/MISOB-A		IRQ0-DS	
G4	TCK	P27	CS7#	MTIOC2B/TMCI3/PO7	SCK1/RSPCKB-A			
G5		P53*1	BCLK					
G6		P52	RD#		RXD2/SMISO2/ SSCL2/SSLB3-A			
G7		PB5	A13	MTIOC2A/MTIOC1B/ TIOCB4/TMRI1/PO29/ POE4#	SCK9/RTS9#/ ET0_ETXD0/ RMII0_TXD0			
G8		PB4	A12	TIOCA4/PO28	CTS9#/ET0_TX_EN/ RMII0_TXD_EN			
G9		PB1	A9	MTIOC0C/MTIOC4C/ TIOCB3/TMCI0/PO25	TXD6/SMOSI6/ SSDA6/ET0_ERXD0/ RMII0_RXD0		IRQ4-DS	
G10	VCC							
H1	TDO	P26	CS6#	MTIOC2A/TMO1/PO6	TXD1/CTS3#/RTS3#/ SMOSI1/SS3#/ SSDA1/MOSIB-A			
H2		P25	CS5#/ EDACK1	MTIOC4C/MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/ SSCL3/SSIDATA1			ADTRG0#
H3		P16		MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/ TMO2/PO14/ RTCOUT	TXD1/RXD3/SMOSI1/ SMISO3/SSDA1/ SSCL3/SCL2-DS/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB		IRQ6	ADTRG0#
H4		P15		MTIOC0B/MTCLKB/ GTETRG-B/TIOCB2/ TCLKB/TMCI2/PO13	RXD1/SCK3/SMISO1/ SSCL1/CRX1-DS/ SSIWS1		IRQ5	
H5		P55	WAIT#/ EDREQ0	MTIOC4D/TMO3	CRX1/ET0_EXOUT		IRQ10	
H6		P54	ALE/ EDACK0	MTIOC4B/TMCI1	CTS2#/RTS2#/SS2#/ CTX1/ET0_LINKSTA			
H7	UB	PC7	A23/CS0#	MTIOC3A/MTCLKB/ GTIOC3A-D/TMO2/ TOC0/PO31/CACREF	TXD8/MISOA-A/ ET0_COL		IRQ14	
H8		PC6	A22/CS1#	MTIOC3C/MTCLKA/ GTIOC3B-D/TMCI2/ TIC0/PO30	RXD8/MOSIA-A/ ET0_ETXD3		IRQ13	
H9		PB6	A14	MTIOC3D/TIOCA5/ PO30	RXD9/ET0_ETXD1/ RMII0_TXD1			
H10		PB7	A15	MTIOC3B/TIOCB5/ PO31	TXD9/ET0_CRS/ RMII0_CRS_DV			
J1		P24	CS4#/ EDREQ1	MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4	SCK3/ USB0_VBUSEN/ SSISCK1			
J2		P21		MTIOC1B/MTIOC4A/ GTIOC2A-B/TIOCA3/ TMCI0/PO1	RXD0/SMISO0/ SSCL0/ USB0_EXICEN/ SSIWS0		IRQ9	

Table 1.9 List of Pins and Pin Functions (100-Pin TFLGA) (4/4)

Pin Number 100-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF)	Interrupt	S12ADC, R12DA
J3		P17		MTIOC3A/MTIOC3B/ MTIOC4B/GTIOC0B-B/TIOCB0/TCLKD/ TMO1/PO15/POE8#	SCK1/TXD3/SMOSI3/ SSDA3/SDA2-DS/ SSITXD0		IRQ7	ADTRG1#
J4		P13		MTIOC0B/TIOCA5/ TMO3/PO13	TXD2/SMOSI2/ SSDA2/SDA0[FM+]		IRQ3	ADTRG1#
J5	VSS_USB							
J6	VCC_USB							
J7		P50	WR0#/WR#		TXD2/SMOSI2/ SSDA2/SSLB1-A			
J8		PC4	A20/CS3#	MTIOC3D/MTCLKC/ GTETRG-D/TMCI1/ PO25/POE0#	SCK5/CTS8#/SSLA0-A/ET0_TX_CLK			
J9		PC0	A16	MTIOC3C/TCLKC/ PO17	CTS5#/RTS5#/SS5#/ SSLA1-A/ET0_ERXD3		IRQ14	
J10		PC1	A17	MTIOC3A/TCLKD/ PO18	SCK5/SSLA2-A/ ET0_ERXD2		IRQ12	
K1		P23	EDACK0	MTIOC3D/MTCLKD/ GTIOC0A-B/TIOCD3/ PO3	TXD3/CTS0#/RTS0#/ SMOSI3/SS0#/ SSDA3/SSISCK0			
K2		P22	EDREQ0	MTIOC3B/MTCLKC/ GTIOC1A-B/TIOCC3/ TMO0/PO2	SCK0/ USB0_OVRCURB/ AUDIO_MCLK			
K3		P20		MTIOC1A/TIOCB3/ TMRI0/PO0	TXD0/SMOSI0/ SSDA0/USB0_ID/ SSIRXD0		IRQ8	
K4		P14		MTIOC3A/MTCLKA/ TIOCB5/TCLKA/ TMRI2/PO15	CTS1#/RTS1#/SS1#/ CTX1/ USB0_OVRCURA		IRQ4	
K5					USB0_DM			
K6					USB0_DP			
K7		P51	WR1#/BC1#/ WAIT#		SCK2/SSLB2-A			
K8		PC5	A21/CS2#/ WAIT#	MTIOC3B/MTCLKD/ GTIOC1A-D/TMRI2/ PO29	SCK8/RSPCKA-A/ RTS8#/ET0_ETXD2			
K9		PC3	A19	MTIOC4D/GTIOC1B-D/TCLKB/PO24	TXD5/SMOSI5/ SSDA5/ET0_TX_ER			
K10		PC2	A18	MTIOC4B/GTIOC2B-D/TCLKA/PO21	RXD5/SMISO5/ SSCL5/SSLA3-A/ ET0_RX_DV			

Note 1. The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.

1.6.6 100-Pin LFQFP

Table 1.10 List of Pins and Pin Functions (100-Pin LFQFP) (1/4)

Pin Number 100-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF)	Interrupt	S12ADC, R12DA
1	AVCC1							
2	EMLE							
3	AVSS1							
4		PJ3	EDACK1	MTIOC3C	ET0_EXOUT/ CTS6#/RTS6#/CTS0#/ RTS0#/SS6#/SS0#			
5	VCL							
6	VBATT							
7	MD/FINED							
8	XCIN							
9	XCOUT							
10	RES#							
11	XTAL	P37						
12	VSS							
13	EXTAL	P36						
14	VCC							
15	UPSEL	P35					NMI	
16	TRST#	P34		MTIOC0A/TMCI3/ PO12/POE10#	SCK6/SCK0/ ET0_LINKSTA		IRQ4	
17		P33	EDREQ1	MTIOC0D/TIOCD0/ TMRI3/PO11/POE4#/ POE11#	RXD6/RXD0/SMISO6/ SMISO0/SSCL6/ SSCL0/CRX0		IRQ3-DS	
18		P32		MTIOC0C/TIOCC0/ TMO3/PO10/ RTCOUT/RTCIC2/ POE0#/POE10#	TXD6/TXD0/SMOSI6/ SMOSI0/SSDA6/ SSDA0/CTX0/ USB0_VBUSEN		IRQ2-DS	
19	TMS	P31		MTIOC4D/TMCI2/ PO9/RTCIC1	CTS1#/RTS1#/SS1#/ SSLB0-A		IRQ1-DS	
20	TDI	P30		MTIOC4B/TMRI3/ PO8/RTCIC0/POE8#	RXD1/SMISO1/ SSCL1/MISOB-A		IRQ0-DS	
21	TCK	P27	CS7#	MTIOC2B/TMCI3/PO7	SCK1/RSPCKB-A			
22	TDO	P26	CS6#	MTIOC2A/TMO1/PO6	TXD1/CTS3#/RTS3#/ SMOSI1/SS3#/ SSDA1/MOSIB-A			
23		P25	CS5#/ EDACK1	MTIOC4C/MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/ SSCL3/SSIDATA1			ADTRG0#
24		P24	CS4#/ EDREQ1	MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4	SCK3/ USB0_VBUSEN/ SSISCK1			
25		P23	EDACK0	MTIOC3D/MTCLKD/ GTIOC0A-B/TIOCD3/ PO3	TXD3/CTS0#/RTS0#/ SMOSI3/SS0#/ SSDA3/SSISCK0			
26		P22	EDREQ0	MTIOC3B/MTCLKC/ GTIOC1A-B/TIOCC3/ TMO0/PO2	SCK0/ USB0_OVRCURB/ AUDIO_MCLK			
27		P21		MTIOC1B/MTIOC4A/ GTIOC2A-B/TIOCA3/ TMCI0/PO1	RXD0/SMISO0/ SSCL0/ USB0_EXICEN/ SSIWS0		IRQ9	
28		P20		MTIOC1A/TIOCB3/ TMRI0/PO0	TXD0/SMOSI0/ SSDA0/USB0_ID/ SSIRXD0		IRQ8	

Table 1.10 List of Pins and Pin Functions (100-Pin LFQFP) (2/4)

Pin Number 100-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF)	Interrupt	S12ADC, R12DA
29		P17		MTIOC3A/MTIOC3B/ MTIOC4B/ GTIOC0B-B/TIOCB0/ TCLKD/TMO1/PO15/ POE8#	SCK1/TXD3/SMOSI3/ SSDA3/SDA2-DS/ SSITXD0		IRQ7	ADTRG1#
30		P16		MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/ TMO2/PO14/ RTCOUT	TXD1/RXD3/SMOSI1/ SMISO3/SSDA1/ SSCL3/SCL2-DS/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB		IRQ6	ADTRG0#
31		P15		MTIOC0B/MTCLKB/ GTETRG-B/TIOCB2/ TCLKB/TMCI2/PO13	RXD1/SCK3/SMISO1/ SSCL1/CRX1-DS/ SSIWS1		IRQ5	
32		P14		MTIOC3A/MTCLKA/ TIOCB5/TCLKA/ TMRI2/PO15	CTS1#/RTS1#/SS1#/ CTX1/ USB0_OVRCURA		IRQ4	
33		P13		MTIOC0B/TIOCA5/ TMO3/PO13	TXD2/SMOSI2/ SSDA2/SDA0[FM+]		IRQ3	ADTRG1#
34		P12		TMCI1	RXD2/SMISO2/ SSCL2/SCL0[FM+]		IRQ2	
35	VCC_USB							
36					USB0_DM			
37					USB0_DP			
38	VSS_USB							
39		P55	WAIT#/ EDREQ0	MTIOC4D/TMO3	CRX1/ET0_EXOUT		IRQ10	
40		P54	ALE/EDACK0	MTIOC4B/TMCI1	CTS2#/RTS2#/SS2#/ CTX1/ET0_LINKSTA			
41		P53*1	BCLK					
42		P52	RD#		RXD2/SMISO2/ SSCL2/SSLB3-A			
43		P51	WR1#/BC1#/ WAIT#		SCK2/SSLB2-A			
44		P50	WR0#/WR#		TXD2/SMOSI2/ SSDA2/SSLB1-A			
45	UB	PC7	A23/CS0#	MTIOC3A/MTCLKB/ GTIOC3A-D/TMO2/ TOC0/PO31/CACREF	TXD8/MISOA-A/ ET0_COL		IRQ14	
46		PC6	A22/CS1#	MTIOC3C/MTCLKA/ GTIOC3B-D/TMCI2/ TIC0/PO30	RXD8/MOSIA-A/ ET0_ETXD3		IRQ13	
47		PC5	A21/CS2#/ WAIT#	MTIOC3B/MTCLKD/ GTIOC1A-D/TMRI2/ PO29	SCK8/RSPCKA-A/ RTS8#/ET0_ETXD2			
48		PC4	A20/CS3#	MTIOC3D/MTCLKC/ GTETRG-D/TMCI1/ PO25/POE0#	SCK5/CTS8#/ SSLA0-A/ ET0_TX_CLK			
49		PC3	A19	MTIOC4D/ GTIOC1B-D/TCLKB/ PO24	TXD5/SMOSI5/ SSDA5/ET0_TX_ER			
50		PC2	A18	MTIOC4B/ GTIOC2B-D/TCLKA/ PO21	RXD5/SMISO5/ SSCL5/SSLA3-A/ ET0_RX_DV			
51		PC1	A17	MTIOC3A/TCLKD/ PO18	SCK5/SSLA2-A/ ET0_ERXD2		IRQ12	
52		PC0	A16	MTIOC3C/TCLKC/ PO17	CTS5#/RTS5#/SS5#/ SSLA1-A/ET0_ERXD3		IRQ14	
53		PB7	A15	MTIOC3B/TIOCB5/ PO31	TXD9/ET0_CRS/ RMII0_CRS_DV			

Table 1.10 List of Pins and Pin Functions (100-Pin LFQFP) (3/4)

Pin Number 100-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF)	Interrupt	S12ADC, R12DA
54		PB6	A14	MTIOC3D/TIOCA5/ PO30	RXD9/ET0_ETXD1/ RMII0_TXD1			
55		PB5	A13	MTIOC2A/MTIOC1B/ TIOCB4/TMRI1/PO29/ POE4#	SCK9/RTS9#/ ET0_ETXD0/ RMII0_TXD0			
56		PB4	A12	TIOCA4/PO28	CTS9#/ET0_TX_EN/ RMII0_TXD_EN			
57		PB3	A11	MTIOC0A/MTIOC4A/ TIOCD3/TCLKD/ TMO0/PO27/POE11#	SCK6/ET0_RX_ER/ RMII0_RX_ER			
58		PB2	A10	TIOCC3/TCLKC/ PO26	CTS6#/RTS6#/SS6#/ ET0_RX_CLK/ REF50CK0			
59		PB1	A9	MTIOC0C/MTIOC4C/ TIOCB3/TMCI0/PO25	TXD6/SMOSI6/ SSDA6/ET0_ERXD0/ RMII0_RXD0		IRQ4-DS	
60	VCC							
61		PB0	A8	MTIC5W/TIOCA3/ PO24	RXD6/SMISO6/ SSCL6/ET0_ERXD1/ RMII0_RXD1		IRQ12	
62	VSS							
63		PA7	A7	TIOCB2/PO23	MISOA-B/ET0_WOL			
64		PA6	A6	MTIC5V/MTCLKB/ GTETRG-C/TIOCA2/ TMCI3/PO22/POE10#	CTS5#/RTS5#/SS5#/ MOSIA-B/ ET0_EXOUT			
65		PA5	A5	MTIOC6B/TIOCB1/ GTIOC0A-C/PO21	RSPCKA-B/ ET0_LINKSTA			
66		PA4	A4	MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20	TXD5/SMOSI5/ SSDA5/SSLA0-B/ ET0_MDC		IRQ5-DS	
67		PA3	A3	MTIOC0D/MTCLKD/ TIOCD0/TCLKB/PO19	RXD5/SMISO5/ SSCL5/ET0_MDIO		IRQ6-DS	
68		PA2	A2	MTIOC7A/ GTIOC1A-C/PO18	RXD5/SMISO5/ SSCL5/SSLA3-B			
69		PA1	A1	MTIOC0B/MTCLKC/ MTIOC7B/ GTIOC2A-C/TIOCB0/ PO17	SCK5/SSLA2-B/ ET0_WOL		IRQ11	
70		PA0	A0/BC0#	MTIOC4A/MTIOC6D/ GTIOC0B-C/TIOCA0/ CACREF/PO16	SSLA1-B/ ET0_TX_EN/ RMII0_TXD_EN			
71		PE7	D15[A15/D15]	MTIOC6A/ GTIOC3A-E/TOC1	MISOB-B	MMC_RES#-B/ SDHI_WP-B	IRQ7	AN105
72		PE6	D14[A14/D14]	MTIOC6C/GTIOC3B-E/TIC1	MOSIB-B	MMC_CD-B/ SDHI_CD-B	IRQ6	AN104
73		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B/ GTIOC0A-A	ET0_RX_CLK/ REF50CK0/ RSPCKB-B		IRQ5	AN103
74		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A/ GTIOC1A-A/PO28	ET0_ERXD2/SSLB0-B			AN102
75		PE3	D11[A11/D11]	MTIOC4B/ GTIOC2A-A/PO26/ POE8#/TOC3	CTS12#/RTS12#/ SS12#/ET0_ERXD3	MMC_D7-B		AN101
76		PE2	D10[A10/D10]	MTIOC4A/ GTIOC0B-A/PO23/ TIC3	RXD12/SMISO12/ SSCL12/RXDX12/ SSLB3-B	MMC_D6-B	IRQ7-DS	AN100
77		PE1	D9[A9/D9]	MTIOC4C/MTIOC3B/ GTIOC1B-A/PO18	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/SSLB2-B	MMC_D5-B		ANEX1
78		PE0	D8[A8/D8]	MTIOC3D/ GTIOC2B-A	SCK12/SSLB1-B	MMC_D4-B		ANEX0

Table 1.10 List of Pins and Pin Functions (100-Pin LFQFP) (4/4)

Pin Number 100-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF)	Interrupt	S12ADC, R12DA
79		PD7	D7[A7/D7]	MTIC5U/POE0#		MMC_D1-B/ SDHI_D1-B/ QIO1-B/ QMI-B	IRQ7	AN107
80		PD6	D6[A6/D6]	MTIC5V/MTIOC8A/ POE4#		MMC_D0-B/ SDHI_D0-B/ QIO0-B/QMO-B	IRQ6	AN106
81		PD5	D5[A5/D5]	MTIC5W/MTIOC8C/ POE10#		MMC_CLK-B/ SDHI_CLK-B/ QSPCLK-B	IRQ5	AN113
82		PD4	D4[A4/D4]	MTIOC8B/POE11#		MMC_CMD-B/ SDHI_CMD-B/ QSSL-B	IRQ4	AN112
83		PD3	D3[A3/D3]	MTIOC8D/ GTIOC0A-E/POE8#/ TOC2		MMC_D3-B/ SDHI_D3-B/ QIO3-B	IRQ3	AN111
84		PD2	D2[A2/D2]	MTIOC4D/ GTIOC0B-E/TIC2	CRX0	MMC_D2-B/ SDHI_D2-B/ QIO2-B	IRQ2	AN110
85		PD1	D1[A1/D1]	MTIOC4B/ GTIOC1A-E/POE0#	CTX0		IRQ1	AN109
86		PD0	D0[A0/D0]	GTIOC1B-E/POE4#			IRQ0	AN108
87		P47					IRQ15-DS	AN007
88		P46					IRQ14-DS	AN006
89		P45					IRQ13-DS	AN005
90		P44					IRQ12-DS	AN004
91		P43					IRQ11-DS	AN003
92		P42					IRQ10-DS	AN002
93		P41					IRQ9-DS	AN001
94	VREFL0							
95		P40					IRQ8-DS	AN000
96	VREFH0							
97	AVCC0							
98		P07					IRQ15	ADTRG0#
99	AVSS0							
100	P05						IRQ13	DA1

Note 1. The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2.1 Absolute Maximum Rating

Conditions: VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V

Item		Symbol	Value	Unit
Power supply voltage		VCC, VCC_USB	–0.3 to +4.6	V
V_{BATT} power supply voltage		V_{BATT}	–0.3 to +4.6	V
Input voltage (except for ports for 5 V tolerant*1)		V_{in}	–0.3 to VCC + 0.3	V
Input voltage (ports for 5 V tolerant*1)		V_{in}	–0.3 to VCC + 4.6 (≤ 5.8 max.)	V
Reference power supply voltage		VREFH0	–0.3 to AVCC0 + 0.3	V
Analog power supply voltage		AVCC0, AVCC1*2	–0.3 to +4.6	V
USBA power supply voltage		VCC_USBA*2	–0.3 to +4.6	V
USBA analog power supply voltage		AVCC_USBA*2	–0.3 to +4.6	V
Analog input voltage		V_{AN}	–0.3 to AVCC + 0.3	V
Junction temperature	D version	Tj	–40 to +105	°C
	G version		–40 to +125	
Storage temperature		T_{stg}	–55 to +125	°C

Caution: Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

Note 1. P07, P11 to P17, P20, P21, P30 to P33, P67, and PC0 to PC3 are 5 V tolerant.

Note 2. Connect the AVCC0, AVCC1, and VCC_USB pins to VCC, and the AVSS0, AVSS1, and VSS_USB pins to VSS.
When the A/D converter unit 0 is not to be used, connect the VREFH0 pin to VCC and the VREFL0 pin to VSS, respectively. Do not leave these pins open.
When the USBA is not to be used, connect the VCC_USBA and AVCC_USBA pins to VCC and the VSS1_USBA, VSS2_USBA, PVSS_USBA, and AVSS_USBA pins to VSS, respectively. Do not leave these pins open.

Table 2.2 Recommended Operating Conditions

Item		Symbol	Min.	Typ.	Max.	Unit
Power supply voltage		VCC	2.7	—	3.6	V
		VSS	—	0	—	V
Power supply voltage (only the RTC and subclock oscillator)*1		VCC	2.0	—	3.6	V
V_{BATT} power supply voltage		V_{BATT}	2.0	—	3.6	V
Reference power voltage		VREFH0	2.7	—	AVCC0	V
		VREFL0	—	0	—	V
Analog power supply voltage		AVCC0, AVCC1	—	VCC	—	V
		AVSS0, AVSS1	—	0	—	V
USB power supply voltage		VCC_USB	—	VCC	—	V
		VSS_USB	—	0	—	V
USBA power supply voltage		VCC_USBA	3.0	—	3.6	V
		VSS1_USBA, VSS2_USBA	—	0	—	V
USBA analog power supply voltage		AVCC_USBA	3.0	—	3.6	V
		AVSS_USBA, PVSS_USBA	—	0	—	V
Operating temperature	D version	T_{opr}	–40	—	85	°C
	G version	T_{opr}	–40	—	105	°C

Note 1. The power-supply voltage range of VBATT in which the RTC and subclock oscillator operate

2.2 DC Characteristics

Table 2.3 DC Characteristics (1)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
$T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	IRQ input pin*1 MTU input pin*1 GPT input pin*1 POE3 input pin*1 TPU input pin*1 TMR input pin*1 CMTW input pin*1 RTC input pin*1 SCI input pin*1 ADTRG# input pin*1 QSPI input pin*1 RES#, NMI, TCK	V_{IH}	0.8 × VCC	—	VCC + 0.3	V	
		V_{IL}	–0.3	—	0.2 × VCC		
		ΔV_T	0.06 × VCC	—	—		
	RIIC input pin (except for SMBus)	V_{IH}	0.7 × VCC	—	VCC + 3.6 (≤ 5.8 max.)		
		V_{IL}	–0.3	—	0.3 × VCC		
		ΔV_T	0.05 × VCC	—	—		
	Ports for 5 V tolerant*2	V_{IH}	0.8 × VCC	—	VCC + 3.6 (≤ 5.8 max.)		
		V_{IL}	–0.3	—	0.2 × VCC		
	Other input pins excluding ports for 5 V tolerant*3	V_{IH}	0.8 × VCC	—	VCC + 0.3		
		V_{IL}	–0.3	—	0.2 × VCC		
Input high voltage (except for Schmitt trigger input pin)	MD pin, EMLE	V_{IH}	0.9 × VCC	—	VCC + 0.3	V	
	EXTAL, RSPI input pin, EXDMAC input pin, WAIT#, TCK, SSI input pin, SDHI input pin, MMC input pin, PDC input pin, QSPI input pin		0.8 × VCC	—	VCC + 0.3		
	ETHERC input pin		2.3	—	VCC + 0.3		
	D0 to D31		0.7 × VCC	—	VCC + 0.3		
	RIIC (SMBus)		2.1	—	VCC + 0.3		
Input low voltage (except for Schmitt trigger input pin)	MD pin, EMLE	V_{IL}	–0.3	—	0.1 × VCC	V	
	EXTAL, RSPI input pin, ETHERC input pin, EXDMAC input pin, WAIT#, TCK, SSI input pin, SDHI input pin, MMC input pin, PDC input pin, QSPI input pin		–0.3	—	0.2 × VCC		
	D0 to D31		–0.3	—	0.3 × VCC		
	RIIC (SMBus)		–0.3	—	0.8		

Note 1. This does not include the pins, which are multiplexed as ports for 5 V tolerant.
Note 2. P07, P11 to P17, P20, P21, P30 to P33, P67, and PC0 to PC3 are 5 V tolerant.
Note 3. For P32, P31, and P30, input as follows when the V_{BATT} power supply is selected.
VIH Min. = V_{BATT} × 0.8, VIH Max. = V_{BATT} + 0.3, VIL Min. = –0.3, VIL Max. = V_{BATT} × 0.2 (V_{BATT} = 2.0 to 3.6 V)

Table 2.4 DC Characteristics (2)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
$T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output high voltage	All output pins	V_{OH}	VCC – 0.5	—	—	V	I_{OH} = –1 mA
Output low voltage	All output pins (except for RIIC pins and ETHERC output pin)	V_{OL}	—	—	0.5	V	I_{OL} = 1.0 mA
	RIIC output pin		—	—	0.4		I_{OL} = 3.0 mA
			—	—	0.6		I_{OL} = 6.0 mA
	RIIC output pin (only P12 and P13 in channel 0)	V_{OL}	—	—	0.4	V	I_{OL} = 15.0 mA (ICFER.FMPE = 1)
			—	0.4	—		I_{OL} = 20.0 mA (ICFER.FMPE = 1)
	ETHERC output pin	V_{OL}	—	—	0.4	V	I_{OL} = 1.0 mA
Input leakage current	RES#, MD pin, EMLE*1, BSCANP*1, NMI	$\lvert I_{in} \rvert$	—	—	1.0	µA	V_{in} = 0 V V_{in} = VCC
Three-state leakage current (off state)	Other than ports for 5 V tolerant	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0 V V_{in} = VCC
	Ports for 5 V tolerant		—	—	5.0		V_{in} = 0 V V_{in} = 5.5 V
Pull-up Resistor	Ports 0 to 2, P30 to P34, P36, P37, Ports 4 to G, PJ3, PJ5	R_{PU}	10	—	100	kΩ	VCC = 2.7 to 3.6 V V_{in} = 0 V
Pull-down Resistor	EMLE, BSCANP	R_{PD}	10	—	100	kΩ	V_{in} = VCC
Input capacitance	All input pins (except for P03, P05, P12, P13, P16, P17, EMLE, BSCANP, USB0_DP, USB0_DM, USBA_DP, and USBA_DM)	C_{in}	—	—	8	pF	Vbias = 0 V Vamp = 20 mV f = 1 MHz T_a = 25°C
	P03, P05, P12, P13, P16, P17, EMLE, BSCANP, USB0_DP, USB0_DM, USBA_DP, and USBA_DM		—	—	16		
Output voltage of the VCL pin		V_{CL}	—	1.25	—	V	

Note 1. The input leakage current value at the EMLE and BSCANP pins are only when V_{in} = 0 V.

Table 2.5 DC Characteristics (3)

Conditions: VCC = AVCC0 = AVCC1 = VREFH0 = VCC_USB = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
$T_a = T_{opr}$

Item				Symbol	D-version		G-version		Unit	Test Conditions
					Typ.	Max.	Typ.	Max.		
Supply current*1	High-speed operating mode	Max.*2		I_{CC}*3	—	220	—	250	mA	ICLK = 240 MHz PCLKA = 120 MHz PCLKB = 60 MHz PCLKC = 60 MHz PCLKD = 60 MHz FCLK = 60 MHz BCLK = 120 MHz BCLK pin = 60 MHz
		Normal	Peripheral function clock signal supplied*4		52	—	52	—		
			Peripheral function clock signal stopped*4		28	—	28	—		
		CoreMark	Peripheral function clock signal stopped*4		41	—	41	—		
		Sleep mode: The clock signal to peripheral modules is supplied*4			37	108	37	137		
		All-module-clock-stop mode (reference value)			15	80	15	108		
		Increased by BGO operation *5	Reading from the code flash memory while the data flash memory is being programmed		7	—	7	—		
			Reading from the code flash memory while the code flash memory is being programmed		10	—	10	—		
	Low-speed operating mode 1: Supply of the clock signal to peripheral modules is stopped*4				4.4	—	4.4	—		All clocks 1 MHz
	Low-speed operating mode 2: Supply of the clock signal to peripheral modules is stopped*4				3.0	—	3.0	—		All clocks 32.768 kHz
	Software standby mode				1.9	59	1.9	83		
	Deep software standby mode	Power supplied to standby RAM and USB resume detecting unit (USBb only)			25	75	25	108	µA	
		Power not supplied to standby RAM and USB resume detecting unit (USBb only)	Power-on reset circuit and low-power consumption function disabled*6		12.5	26	12.5	36.4		
			Power-on reset circuit and low-power consumption function enabled*7		3.1	13.5	3.1	20.0		
		Increased by RTC operation	When a crystal resonator for low clock loads is in use		0.6	—	0.6	—		
			When a crystal resonator for standard clock loads is in use		2.0	—	2.0	—		
	RTC operating while VCC is off (with the battery backup function, only the RTC and sub-clock oscillator operate)		RCR3.RTCDV[2:0] set to drive capacity for standard CL		0.9	—	0.9	—		V_{BATT} = 2.0 V, VCC = 0 V
					1.6	—	1.6	—		V_{BATT} = 3.3 V, VCC = 0 V
			RCR3.RTCDV[2:0] set to drive capacity for low CL		1.7	—	1.7	—		V_{BATT} = 2.0 V, VCC = 0 V
					3.3	—	3.3	—		V_{BATT} = 3.3 V, VCC = 0 V

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Supply of the clock signal to peripheral modules is stopped in this state. This does not include operations as BGO (background operations).
Note 3. I_{CC} depends on f (ICLK) as follows. (ICLK:PCLKA:PCLKB/PCLKC/PCLKD:BCLK:BCLK pin = 10:5:2.5:5:2.5 when EXTAL = 24 MHz)
- D-version
  I_{CC} Max. = 0.47 × f + 107 (max. operation in high-speed operating mode)
  I_{CC} Typ. = 0.09 × f + 7 (normal operation in high-speed operating mode)
  I_{CC} Typ. = 0.50 × f + 4 (low-speed operating mode 1)
  I_{CC} Max. = 0.14 × f + 74 (sleep mode)
- G-version
  I_{CC} Max. = 0.47 × f + 137 (max. operation in high-speed operating mode)
  I_{CC} Typ. = 0.09 × f + 7 (normal operation in high-speed operating mode)
  I_{CC} Typ. = 0.40 × f + 4 (low-speed operating mode 1)
  I_{CC} Max. = 0.14 × f + 103 (sleep mode)

Note 4. This does not include operations as BGO (background operations). Whether supply of the clock signal to peripheral modules continues or is stopped only depends on the state determined by the settings of the bits in module stop control registers A to D. The setting for the peripheral module clock stopped state is FCLK = BCLK = PCLKA = PCLKB = PCLKC = PCLKD = BCLK pin = 3.75 MHz (division by 64).
Note 5. This is the increase for programming or erasure of the code flash memory (limitations apply to the combinations of ranges in which writing proceed) or data flash memory during program execution in the code flash memory.
Note 6. The low power consumption function is disabled and DEEPCUT[1:0] = 01b.
Note 7. The low power consumption function is enabled and DEEPCUT[1:0] = 11b.

Table 2.6 DC Characteristics (4)

Conditions: VCC = AVCC0 = AVCC1 = VREFH0 = VCC_USB = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
$T_a = T_{opr}$

Item			Symbol	D-version			G-version			Unit	Test Conditions
				Min.	Typ.	Max.	Min.	Typ.	Max.		
Analog power supply current*1	During 12-bit A/D conversion (unit 0)		AI_{CC}	—	0.7	1.1	—	0.7	1.1	mA	IAVCC0_AD
	During 12-bit A/D conversion (unit 0) with the channel-dedicated sample-and-hold circuits for 3 channels operating			—	2.2	3.3	—	2.2	3.3	mA	IAVCC0_AD+SH
	During 12-bit A/D conversion (unit 1)			—	0.7	1.1	—	0.7	1.1	mA	IAVCC1_AD
	During 12-bit A/D conversion (unit 1) with the temperature sensor operating			—	0.7	2.3	—	0.7	2.3	mA	IAVCC1_AD+TEMP
	During D/A conversion (per unit)	Without AMP output		—	0.24	0.4	—	0.24	0.4	mA	IAVCC1_DA
		With AMP output		—	0.45	0.7	—	0.45	0.7	mA	
	Waiting for A/D, D/A, or temperature sensor conversion (all units)			—	0.9	1.6	—	0.9	1.6	mA	IAVCC0 + IAVCC1
	A/D, D/A converter, temperature sensor in standby mode (all units)			—	1.3	5.0	—	1.3	5.0	µA	IAVCC0 + IAVCC1
Reference power supply current	During 12-bit A/D conversion (unit 0)		AI_{REFH}	—	70	120	—	70	120	µA	IVREFH0
	Waiting for 12-bit A/D conversion (unit 0)			—	0.07	0.5	—	0.07	0.5	µA	IVREFH0
	12-bit A/D converter in standby mode (unit 0)			—	0.07	0.5	—	0.07	0.5	µA	IVREFH0
USB operating current	Low speed	USB	$I_{CCUSBLS}$	—	3.5	6.5	—	3.5	6.5	mA	VCC_USB
		USBA		—	10.5	13.5	—	10.5	13.5	mA	VCC_USBA = AVCC_USBA (PHYSET.HSEB = 0)
		USBA		—	2.8	3.6	—	2.8	3.6	mA	VCC_USBA = AVCC_USBA (PHYSET.HSEB = 1)
	Full speed	USB	$I_{CCUSBFS}$	—	4.0	10.0	—	4.0	10.0	mA	VCC_USB
		USBA		—	14.0	22.0	—	14.0	22.0	mA	VCC_USBA = AVCC_USBA (PHYSET.HSEB = 0)
		USBA		—	6.5	13.0	—	6.5	13.0	mA	VCC_USBA = AVCC_USBA (PHYSET.HSEB = 1)
	High speed	USBA	$I_{CCUSBHS}$	—	50.0	65.0	—	50.0	65.0	mA	VCC_USBA = AVCC_USBA
	Standby mode (direct power down)	USBA	$I_{CCUSBSBY}$	—	0.1	3.0	—	0.1	3.0	µA	VCC_USBA = AVCC_USBA
RAM standby voltage			V_{RAM}	2.7	—	—	2.7	—	—	V	
VCC rising gradient			SrVCC	8.4	—	20000	8.4	—	20000	µs/V	
VCC falling gradient*2			SfVCC	8.4	—	—	8.4	—	—	µs/V	

Note 1. The reference power supply current is included in the power supply current value for 12-bit A/D converter (unit 1) and D/A converter.

Note 2. This applies when V_{BATT} is used.

Table 2.7 Thermal Resistances (Reference)

Item	Package	Symbol	Max.	Unit	Test Conditions
Thermal resistance	PLQP0176KB-A	θ_{ja}	39.1	°C/W	JESD51-2 and JESD51-7 compliant
	PLQP0144KA-A		40.4		
	PLQP0100KB-A		41.3		
	PLBG0176GA-A		28.4		JESD51-2 and JESD51-9 compliant
	PTLG0177KA-A		27.7		
	PTLG0145KA-A		28.2		
	PTLG0100JA-A		20.6		
	PLQP0176KB-A	Ψ_{jt}	0.5	°C/W	JESD51-2 and JESD51-7 compliant
	PLQP0144KA-A		0.5		
	PLQP0100KB-A		0.5		
	PLBG0176GA-A		0.2		JESD51-2 and JESD51-9 compliant
	PTLG0177KA-A		0.2		
	PTLG0145KA-A		0.2		
	PTLG0100JA-A		0.2		

Note: The values are reference values when the 4-layer printed circuit board is used. Thermal resistance depends on the number of layers and size of the board. For details, refer to the JEDEC standards.

Table 2.8 Permissible Output Currents

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
$T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit
Permissible output low current (average value per pin)	All output pins*1	Normal drive	I_{OL}	—	—	2.0	mA
	All output pins*2	High drive	I_{OL}	—	—	3.8	mA
Permissible output low current (max. value per pin)	All output pins*1	Normal drive	I_{OL}	—	—	4.0	mA
	All output pins*2	High drive	I_{OL}	—	—	7.6	mA
Permissible output low current (total)	Total of all output pins		ΣI_{OL}	—	—	80	mA
Permissible output high current (average value per pin)	All output pins*1	Normal drive	I_{OH}	—	—	–2.0	mA
	USB_DPUPE pin*2	High drive	I_{OH}	—	—	–3.8	mA
Permissible output high current (max. value per pin)	All output pins*1	Normal drive	I_{OH}	—	—	–4.0	mA
	All output pins*2	High drive	I_{OH}	—	—	–7.6	mA
Permissible output high current (total)	Total of all output pins		ΣI_{OH}	—	—	–80	mA

Caution: To protect the LSI's reliability, the output current values should not exceed the values in this table.
Note 1. This is the value when normal driving ability is set with a pin for which normal driving ability is selectable.
Note 2. This is the value when high driving ability is set with a pin for which normal driving ability is selectable or the value of the pin to which high driving ability is fixed.

2.3 AC Characteristics

Table 2.9 Operating Frequency (High-Speed Operating Mode)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
$T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit
Operating frequency	System clock (ICLK)		f	—	—	240	MHz
	Peripheral module clock (PCLKA)			—	—	120	
	Peripheral module clock (PCLKB)			—	—	60	
	Peripheral module clock (PCLKC)			—	—	60	
	Peripheral module clock (PCLKD)			—	—	60	
	Flash-IF clock (FCLK)			—*1	—	60	
	External bus clock (BCLK)	Packages with 177 to 144 pins only		—	—	120	
		Package with 100 pins only		—	—	60	
	BCLK pin output	Packages with 177 to 144 pins only		—	—	60	
		Package with 100 pins only		—	—	30	
	SDRAM clock (SDCLK)	Packages with 177 to 144 pins only		—	—	60	
	SDCLK pin output	Packages with 177 to 144 pins only		—	—	60	

Note 1. The FCLK must run at a frequency of at least 4 MHz when changing the flash memory contents.

Table 2.10 Operating Frequency (Low-Speed Operating Mode 1)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
$T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit
Operating frequency	System clock (ICLK)		f	—	—	1	MHz
	Peripheral module clock (PCLKA)			—	—	1	
	Peripheral module clock (PCLKB)			—	—	1	
	Peripheral module clock (PCLKC)*1			—	—	1	
	Peripheral module clock (PCLKD)*1			—	—	1	
	Flash-IF clock (FCLK)			—	—	1	
	External bus clock (BCLK)	Packages with 177 to 144 pins only		—	—	1	
		Package with 100 pins only		—	—	1	
	BCLK pin output	Packages with 177 to 144 pins only		—	—	1	
		Package with 100 pins only		—	—	1	
	SDRAM clock (SDCLK)	Packages with 177 to 144 pins only		—	—	1	
	SDCLK pin output	Packages with 177 to 144 pins only		—	—	1	

Note 1. When the 12-bit A/D converter is used, the frequency must be set to at least 1 MHz.

Table 2.11 Operating Frequency (Low-Speed Operating Mode 2)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
$T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit
Operating frequency	System clock (ICLK)		f	32	—	264	kHz
	Peripheral module clock (PCLKA)			—	—	264	
	Peripheral module clock (PCLKB)			—	—	264	
	Peripheral module clock (PCLKC)*1			—	—	264	
	Peripheral module clock (PCLKD)*1			—	—	264	
	Flash-IF clock (FCLK)			32	—	264	
	External bus clock (BCLK)	Packages with 177 to 144 pins only		—	—	264	
		Package with 100 pins only		—	—	264	
	BCLK pin output	Packages with 177 to 144 pins only		—	—	264	
		Package with 100 pins only		—	—	264	
	SDRAM clock (SDCLK)	Packages with 177 to 144 pins only		—	—	264	
	SDCLK pin output	Packages with 177 to 144 pins only		—	—	264	

Note 1. The 12-bit A/D converter cannot be used.

2.3.1 Reset Timing

Table 2.12 Reset Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
$T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RES# pulse width	Power-on	t_{RESWP}	1	—	—	ms	Figure 2.1
	Deep software standby mode	t_{RESWD}	0.6	—	—	ms	Figure 2.2
	Software standby mode, low-speed operating mode 2	t_{RESWS}	0.3	—	—	ms	
	Programming or erasure of the code flash memory, or programming, erasure or blank checking of the data flash memory	t_{RESWF}	200	—	—	µs	
	Other than above	t_{RESW}	200	—	—	µs	
Waiting time after release from the RES# pin reset		t_{RESWT}	62	—	63	t_{Lcyc}	Figure 2.1
Internal reset time (independent watchdog timer reset, watchdog timer reset, software reset)		t_{RESW2}	108	—	116	t_{Lcyc}	

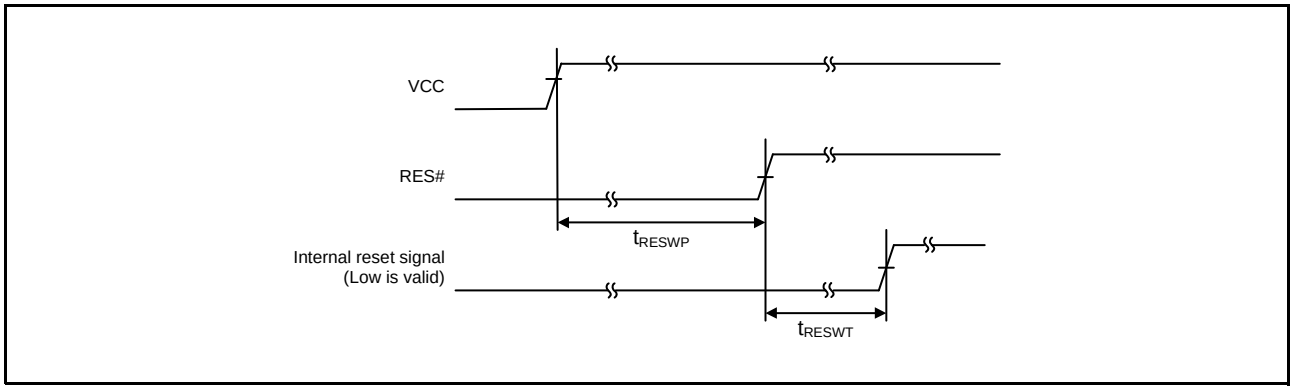


Figure 2.1 Reset Input Timing at Power-On

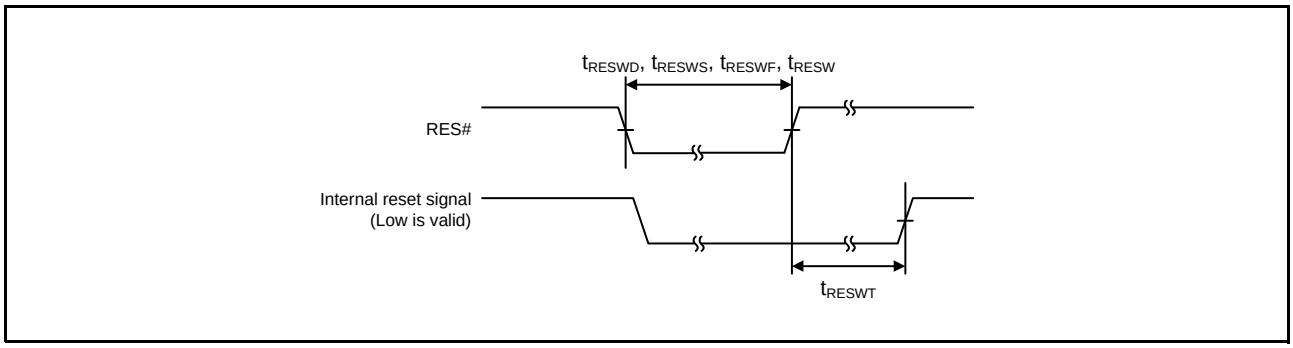


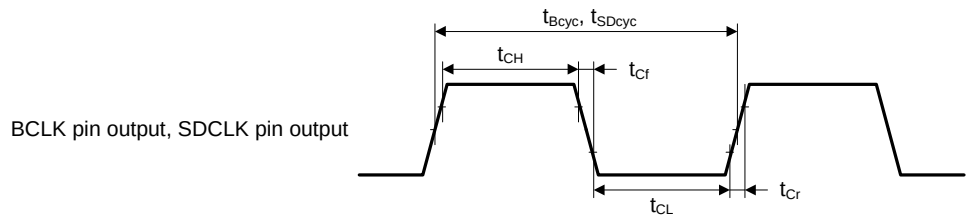
Figure 2.2 Reset Input Timing

2.3.2 Clock Timing

Table 2.13 BCLK Pin Output, SDCLK Pin Output Clock Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
$T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BCLK pin output cycle time	Packages with 177 to 144 pins	t_{Bcyc}	16.6	—	—	ns	Figure 2.3
	Packages with 100 pins or less		33.2	—	—	ns	
BCLK pin output high pulse width		t_{CH}	3.3	—	—	ns	
BCLK pin output low pulse width		t_{CL}	3.3	—	—	ns	
BCLK pin output rising time		t_{Cr}	—	—	5	ns	
BCLK pin output falling time		t_{Cf}	—	—	5	ns	
SDCLK pin output cycle time	Packages with 177 to 144 pins	t_{SDcyc}	16.6	—	—	ns	
SDCLK pin output high pulse width		t_{CH}	3.3	—	—	ns	
SDCLK pin output low pulse width		t_{CL}	3.3	—	—	ns	
SDCLK pin output rising time		t_{Cr}	—	—	5	ns	
SDCLK pin output falling time		t_{Cf}	—	—	5	ns	



Test conditions: V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, C = 30 pF

Figure 2.3 BCLK Pin and SDCLK Pin Output Timing

Table 2.14 EXTAL Clock Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
EXTAL external clock input cycle time	t_{EXcyc}	41.66	—	—	ns	Figure 2.4
EXTAL external clock input high pulse width	t_{EXH}	15.83	—	—	ns	
EXTAL external clock input low pulse width	t_{EXL}	15.83	—	—	ns	
EXTAL external clock rising time	t_{EXr}	—	—	5	ns	
EXTAL external clock falling time	t_{EXf}	—	—	5	ns	

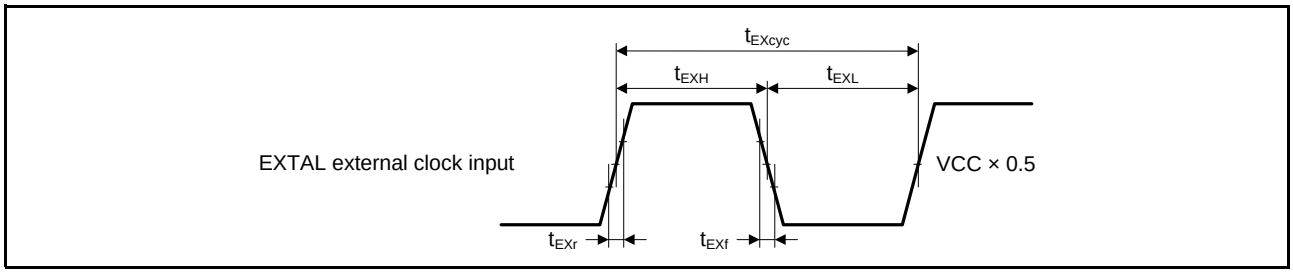


Figure 2.4 EXTAL External Clock Input Timing

Table 2.15 Main Clock Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Main clock oscillation frequency	f_{MAIN}	8	—	24	MHz	
Main clock oscillator stabilization time (crystal)	$t_{MAINOSC}$	—	—	—*1	ms	Figure 2.5
Main clock oscillation stabilization wait time (crystal)	$t_{MAINOSCWT}$	—	—	—*2	ms	

Note 1. When using a main clock, ask the manufacturer of the oscillator to evaluate its oscillation. Refer to the results of evaluation provided by the manufacturer for the oscillation stabilization time.

Note 2. The number of cycles selected by the value of the MOSCWTCR.MSTS[7:0] bits determines the main clock oscillation stabilization wait time in accord with the formula below.
$t_{MAINOSCWT}$ = [(MSTS[7:0] bits × 32) + 10] / f_{LOCO}

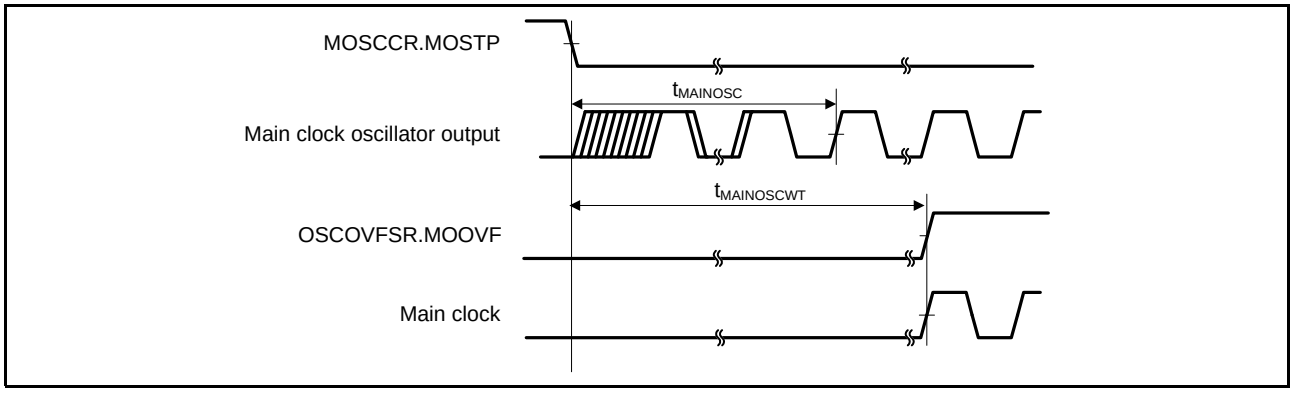


Figure 2.5 Main Clock Oscillation Start Timing

Table 2.16 LOCO and IWDT-Dedicated Low-Speed Clock Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
LOCO clock cycle time	t_{Lcyc}	3.78	4.16	4.63	µs	
LOCO clock oscillation frequency	f_{LOCO}	216	240	264	kHz	
LOCO clock oscillation stabilization wait time	t_{LOCOWT}	—	—	44	µs	Figure 2.6
IWDT-dedicated low-speed clock cycle time	t_{ILcyc}	7.57	8.33	9.26	µs	
IWDT-dedicated low-speed clock oscillation frequency	f_{ILOCO}	108	120	132	kHz	
IWDT-dedicated low-speed clock oscillation stabilization wait time	$t_{ILOCOWT}$	—	142	190	µs	Figure 2.7

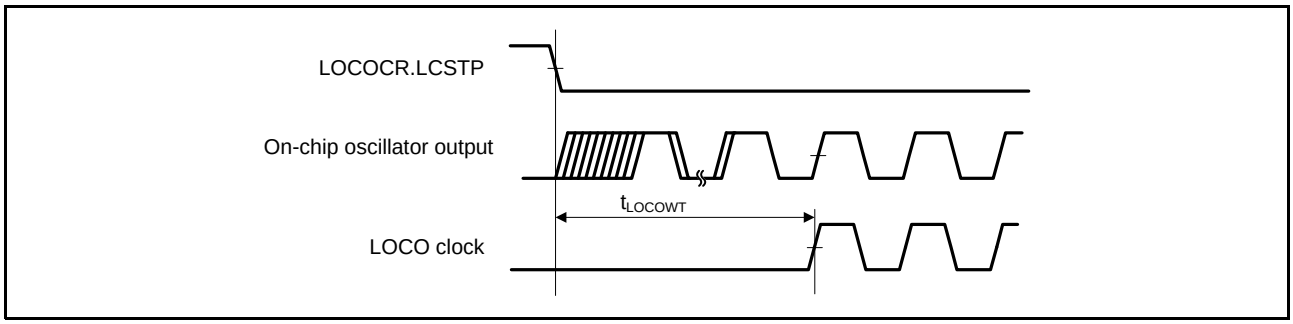


Figure 2.6 LOCO Clock Oscillation Start Timing

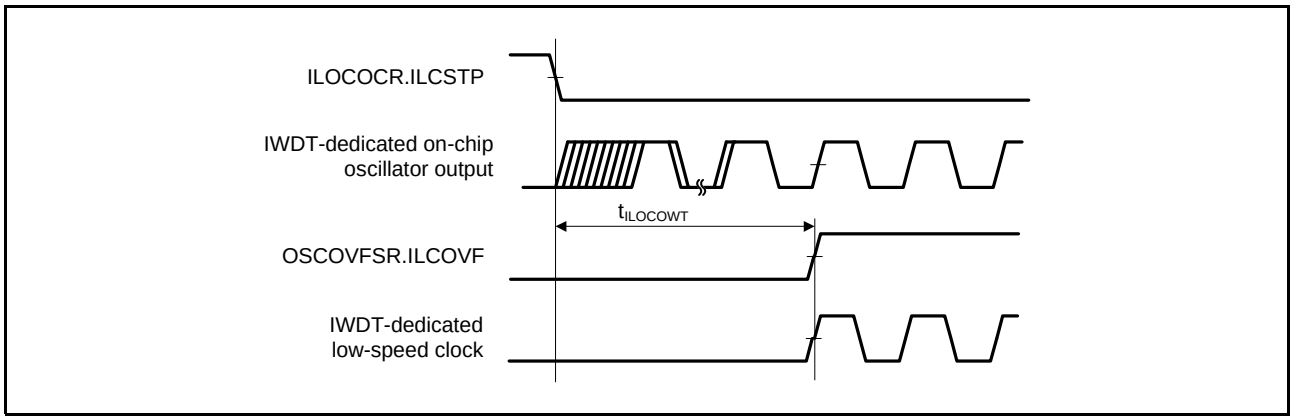


Figure 2.7 IWDT-dedicated Low-Speed Clock Oscillation Start Timing

Table 2.17 HOCO Clock Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
HOCO clock oscillation frequency	f_{HOCO}	15.61	16	16.39	MHz	–20°C ≤ T_a ≤ 85°C
		17.56	18	18.44	MHz	
		19.52	20	20.48	MHz	
		15.52	16	16.48	MHz	–40°C ≤ T_a < –20°C
		17.46	18	18.54	MHz	
		19.40	20	20.60	MHz	
HOCO clock oscillation stabilization wait time	t_{HOCOWT}	—	105	149	µs	Figure 2.8
HOCO clock power supply stabilization time	t_{HOCOP}	—	—	150	µs	Figure 2.9

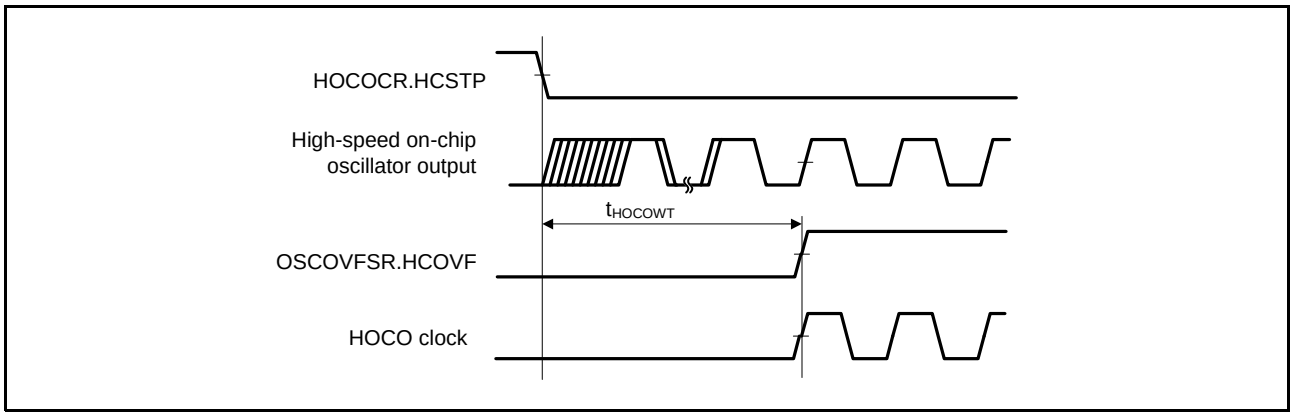


Figure 2.8 HOCO Clock Oscillation Start Timing (Oscillation is Started by Setting the HOCOCR.HCSTP Bit)

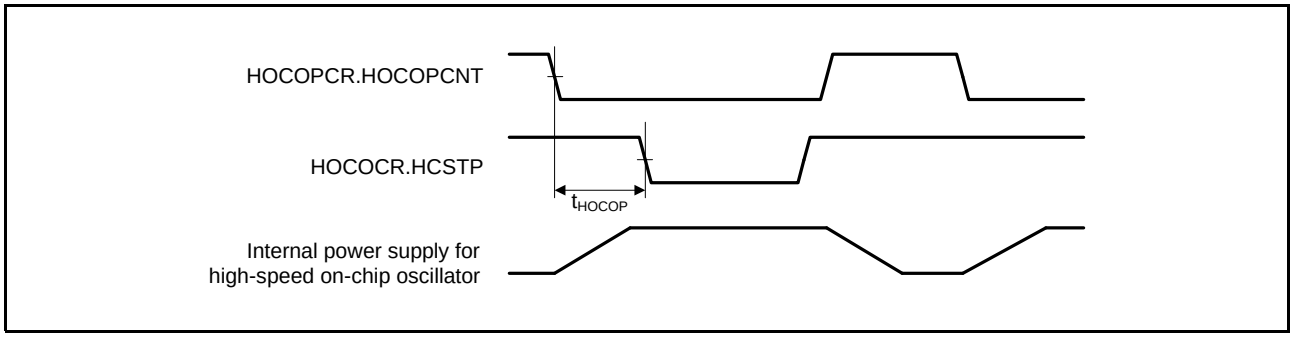


Figure 2.9 High-Speed On-Chip Oscillator Power Supply Control Timing

Table 2.18 PLL Clock Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
PLL clock oscillation frequency	f_{PLL}	120	—	240	MHz	
PLL clock oscillation stabilization wait time	t_{PLLWT}	—	259	320	µs	Figure 2.10

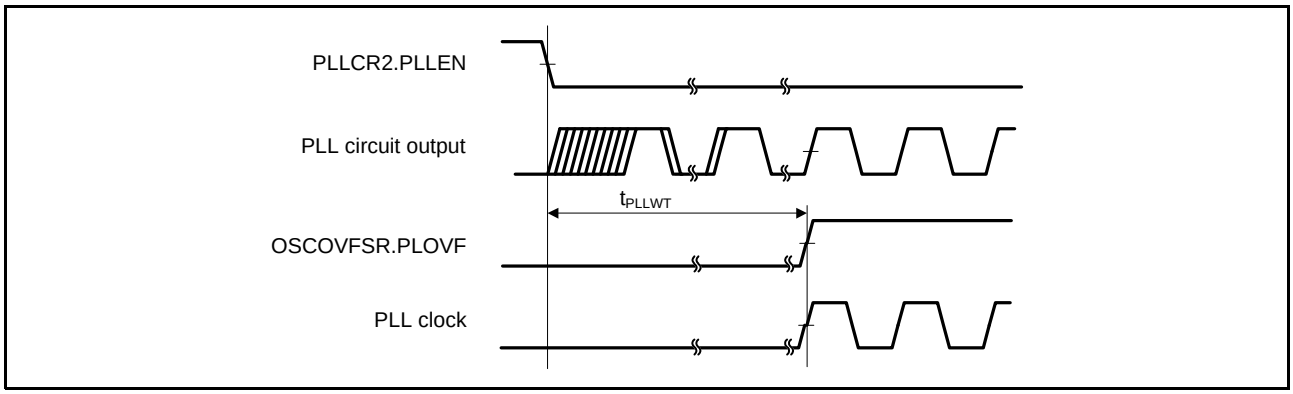


Figure 2.10 PLL Clock Oscillation Start Timing

Table 2.19 Sub-Clock Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
V_{BATT} = 2.0 to 3.6 V, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Sub-clock oscillation frequency	f_{SUB}	—	32.768	—	kHz	
Sub-clock oscillation stabilization time	t_{SUBOSC}	—	—	*1	s	Figure 2.11
Sub-clock oscillation stabilization wait time	$t_{SUBOSCWT}$	—	—	*2	s	

Note 1. When using a sub-clock, ask the manufacturer of the oscillator to evaluate its oscillation. Refer to the results of evaluation provided by the manufacturer for the oscillation stabilization time.

Note 2. The number of cycles selected by the value of the SOSCWTCR.SSTS[7:0] bits determines the sub-clock oscillation stabilization wait time in accord with the formula below.
$t_{SUBOSCWT}$ = [(SSTS[7:0] bits × 16384) + 10] / f_{LOCO}

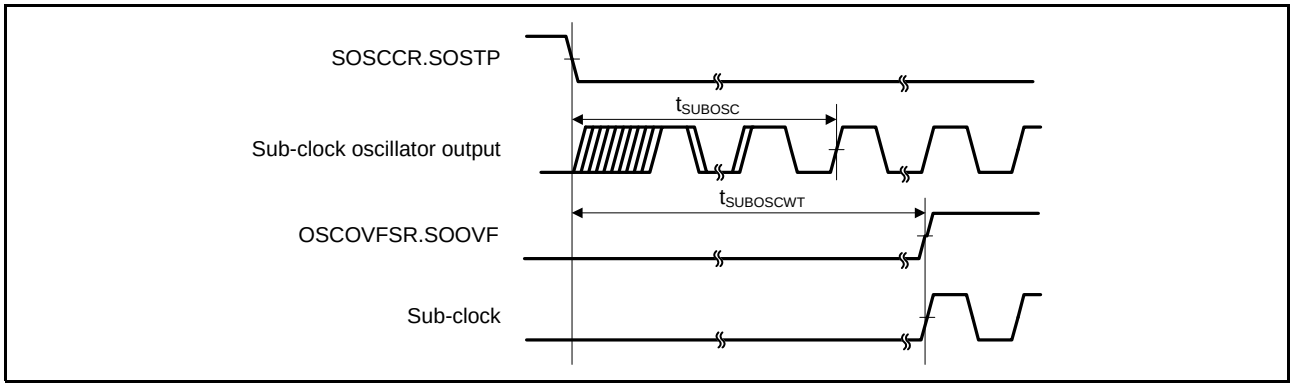


Figure 2.11 Sub-Clock Oscillation Start Timing

2.3.3 Timing of Recovery from Low Power Consumption Modes

Table 2.20 Timing of Recovery from Low Power Consumption Modes (1)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
$T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.		Unit	Test Conditions
						$t_{SBYOSCWT}$*2	t_{SBYSEQ}*3		
Recovery time after cancellation of software standby mode*1	Crystal resonator connected to main clock oscillator	Main clock oscillator operating	t_{SBYMC}	—	—	{(MSTS[7:0] bit × 32) + 76} / 0.216	100 µs + 7/f_{ICLK} + 2n/f_{MAIN}	µs	Figure 2.12
		Main clock oscillator and PLL circuit operating	t_{SBYPC}			{(MSTS[7:0] bit × 32) + 138} / 0.216	100 µs + 7/f_{ICLK} + 2n/f_{PLL}		
	External clock input to main clock oscillator	Main clock oscillator operating	t_{SBYEX}			352	100 µs + 7/f_{ICLK} + 2n/f_{EXMAIN}		
		Main clock oscillator and PLL circuit operating	t_{SBYPE}			639	100 µs + 7/f_{ICLK} + 2n/f_{PLL}		
	Sub-clock oscillator operating		t_{SBYSC}			{(SSTS[7:0] bit × 16384) + 13} / 0.216 + 10/f_{FCLK}	100 µs + 4/f_{ICLK} + 2n/f_{SUB}		
	High-speed on-chip oscillator operating	High-speed on-chip oscillator operating	t_{SBYHO}			454	100 µs + 7/f_{ICLK} + 2n/f_{HOCO}		
		High-speed on-chip oscillator operating and PLL circuit operating	t_{SBYPH}			741	100 µs + 7/f_{ICLK} + 2n/f_{PLL}		
	Low-speed on-chip oscillator operating*4		t_{SBYLO}			338	100 µs + 7/f_{ICLK} + 2n/f_{LOCO}		

Note 1. The time for return after release from software standby is determined by the value obtained by adding the oscillation stabilization waiting time ($t_{SBYOSCWT}$) and the time required for operations by the software standby release sequencer (t_{SBYSEQ}).
Note 2. When several oscillators were running before the transition to software standby, the greatest value of the oscillation stabilization waiting time $t_{SBYOSCWT}$ is selected.
Note 3. For n, the greatest value is selected from among the internal clock division settings.
Note 4. This condition applies when f_{ICLK}:f_{FCLK} = 1:1, 2:1, or 4:1.

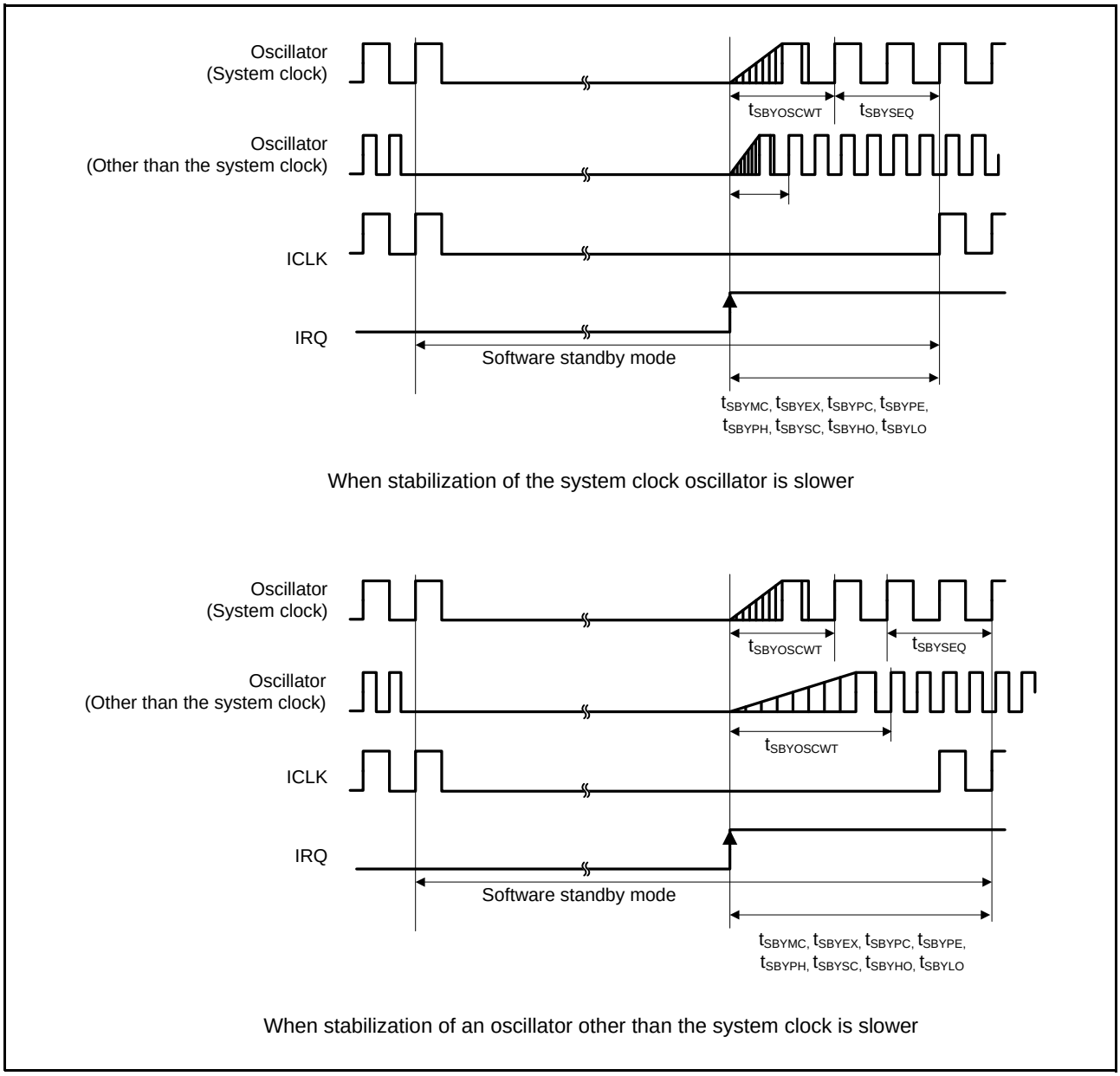


Figure 2.12 Software Standby Mode Cancellation Timing

Table 2.21 Timing of Recovery from Low Power Consumption Modes (2)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
$T_a = T_{opr}$

Item	Symbol	min	typ	max	Unit	Test Conditions
Recovery time after cancellation of deep software standby mode	t_{DSBY}	—	—	0.9	ms	Figure 2.13
Wait time after cancellation of deep software standby mode	t_{DSBYWT}	31	—	32	t_{Lcyc}	

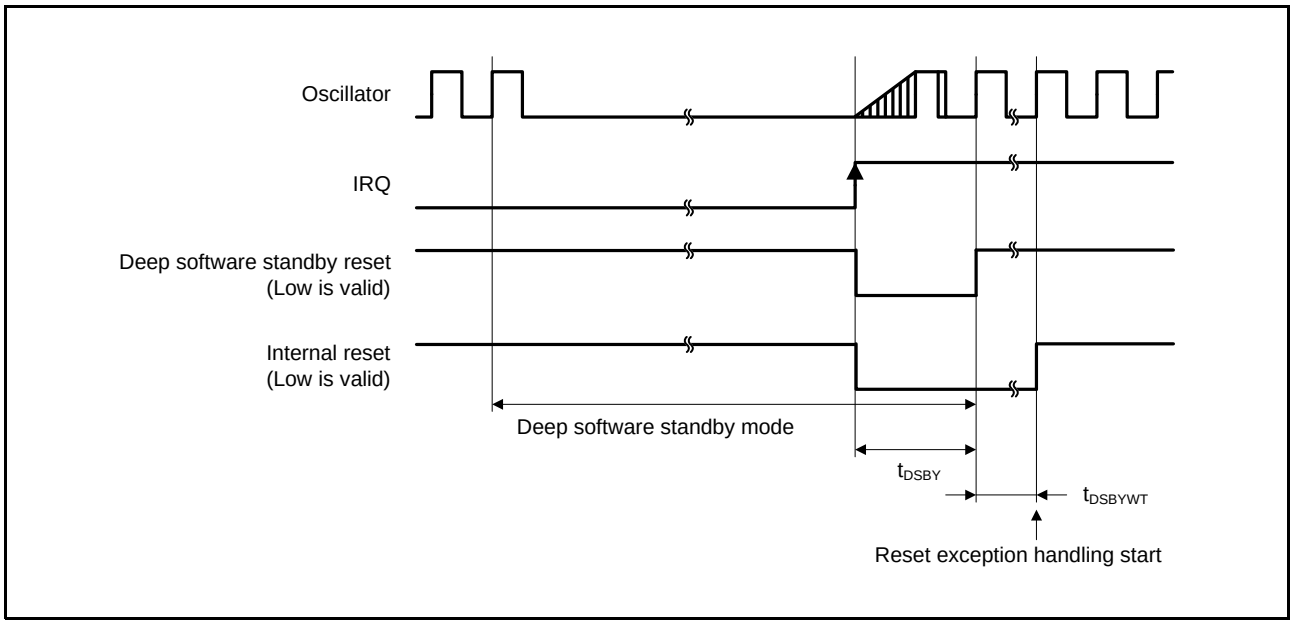


Figure 2.13 Deep Software Standby Mode Cancellation Timing

2.3.4 Control Signal Timing

Table 2.22 Control Signal Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
PLCKB = 8 to 60 MHz, $T_a = T_{opr}$

Item	Symbol	Min.*1	Typ.	Max.	Unit	Test Conditions*1
NMI pulse width	t_{NMIW}	200	—	—	ns	$t_{PBcyc} \times 2 \leq 200$ ns, Figure 2.14
		$t_{PBcyc} \times 2$	—	—	ns	$t_{PBcyc} \times 2 > 200$ ns, Figure 2.14
IRQ pulse width	t_{IRQW}	200	—	—	ns	$t_{PBcyc} \times 2 \leq 200$ ns, Figure 2.15
		$t_{PBcyc} \times 2$	—	—	ns	$t_{PBcyc} \times 2 > 200$ ns, Figure 2.15

Note 1. t_{PBcyc}: PCLKB cycle

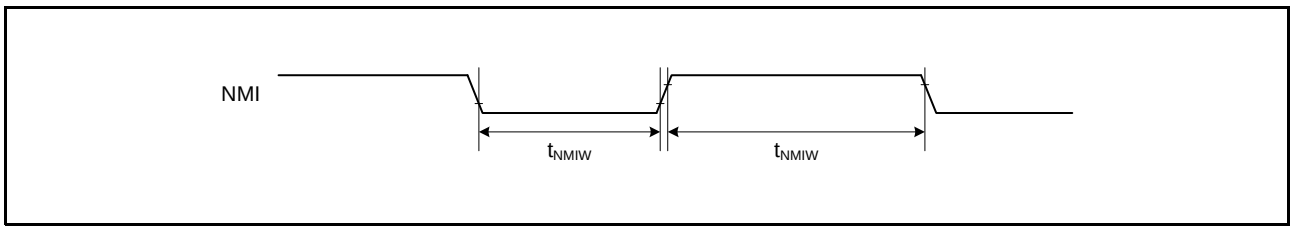


Figure 2.14 NMI Interrupt Input Timing

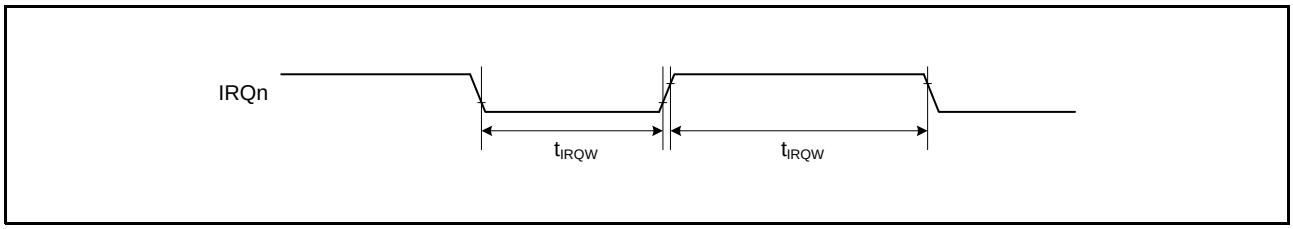


Figure 2.15 IRQ Interrupt Input Timing

2.3.5 Bus Timing

Table 2.23 Bus Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
ICLK = 8 to 240 MHz, PCLKA = 8 to 120 MHz, PCLKB = BCLK = SDCLK = 8 to 60 MHz, $T_a = T_{opr}$
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF
High-drive output is selected by the driving ability control register.

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	12.5	ns	Figure 2.16 to Figure 2.21
Byte control delay time	t_{BCD}	—	12.5	ns	
CS# delay time	t_{CSD}	—	12.5	ns	
ALE delay time	t_{ALED}	—	12.5	ns	
RD# delay time	t_{RSD}	—	12.5	ns	
Read data setup time	t_{RDS}	12.5	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	12.5	ns	
Write data delay time	t_{WDD}	—	12.5	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	12.5	—	ns	Figure 2.22
WAIT# hold time	t_{WTH}	0	—	ns	
Address delay time 2 (SDRAM)	t_{AD2}	1	12.5	ns	Figure 2.23
CS# delay time 2 (SDRAM)	t_{CSD2}	1	12.5	ns	
DQM delay time (SDRAM)	t_{DQMD}	1	12.5	ns	
CKE delay time (SDRAM)	t_{CKED}	1	12.5	ns	
Read data setup time 2 (SDRAM)	t_{RDS2}	10	—	ns	
Read data hold time 2 (SDRAM)	t_{RDH2}	0	—	ns	
Write data delay time 2 (SDRAM)	t_{WDD2}	—	12.5	ns	
Write data hold time 2 (SDRAM)	t_{WDH2}	1	—	ns	
WE# delay time (SDRAM)	t_{WED}	1	12.5	ns	
RAS# delay time (SDRAM)	t_{RASD}	1	12.5	ns	
CAS# delay time (SDRAM)	t_{CASD}	1	12.5	ns	

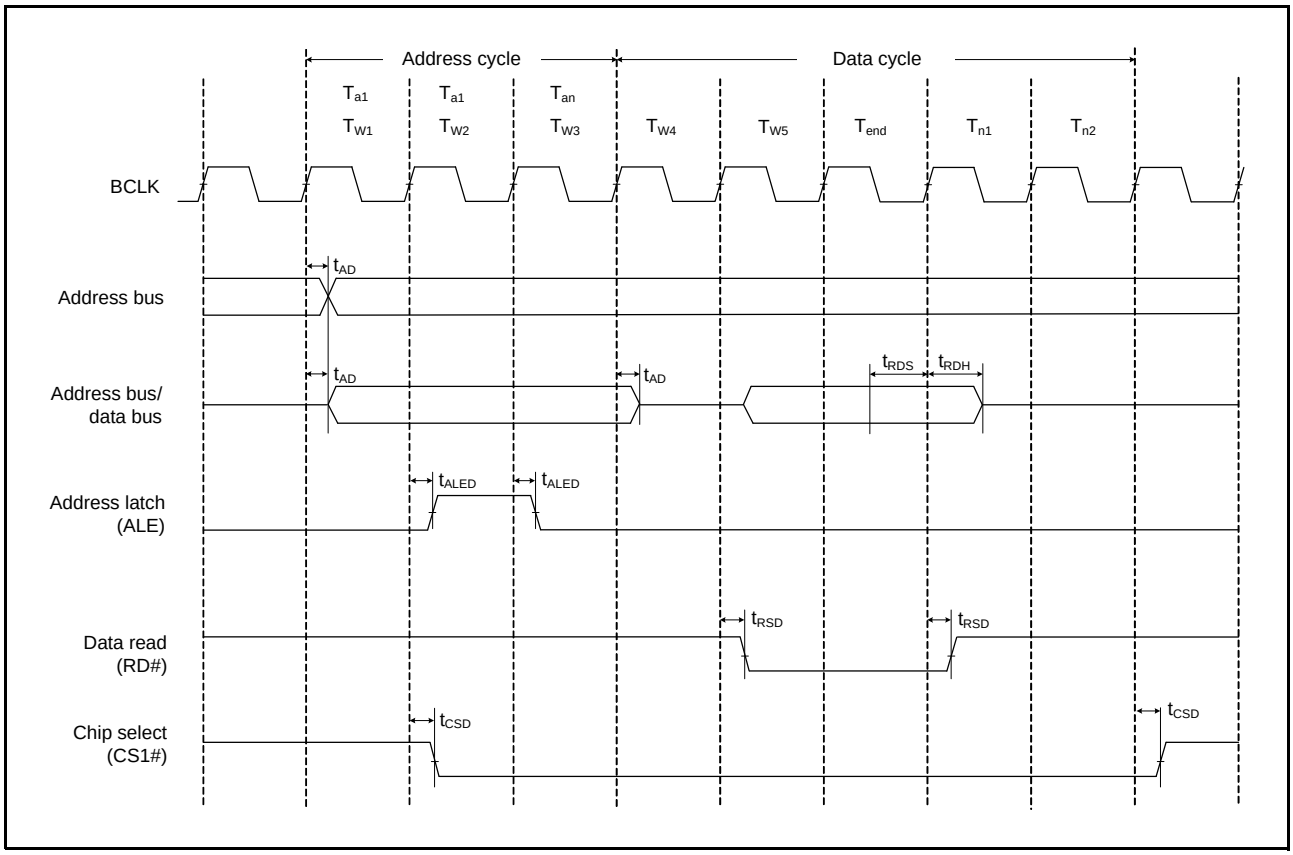


Figure 2.16 Address/Data Multiplexed Bus Read Access Timing

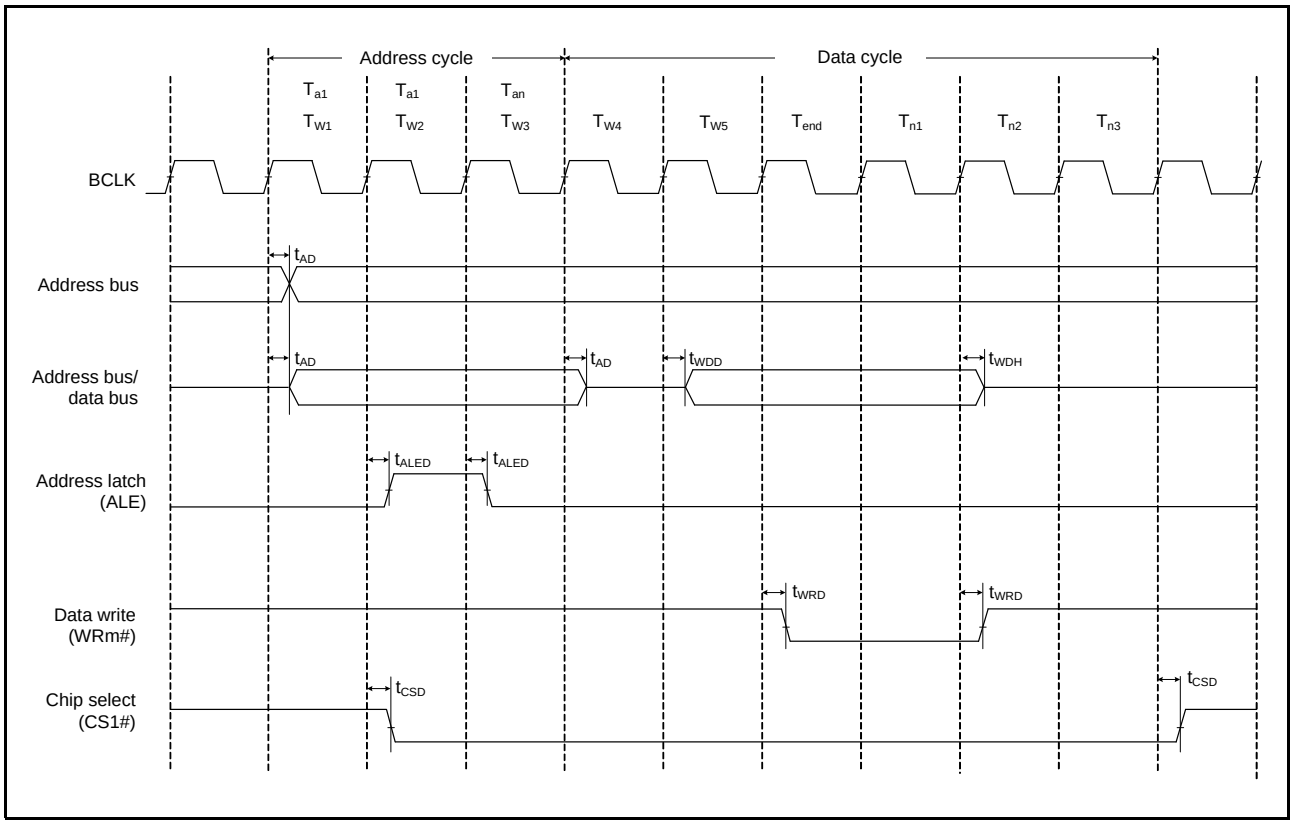


Figure 2.17 Address/Data Multiplexed Bus Write Access Timing

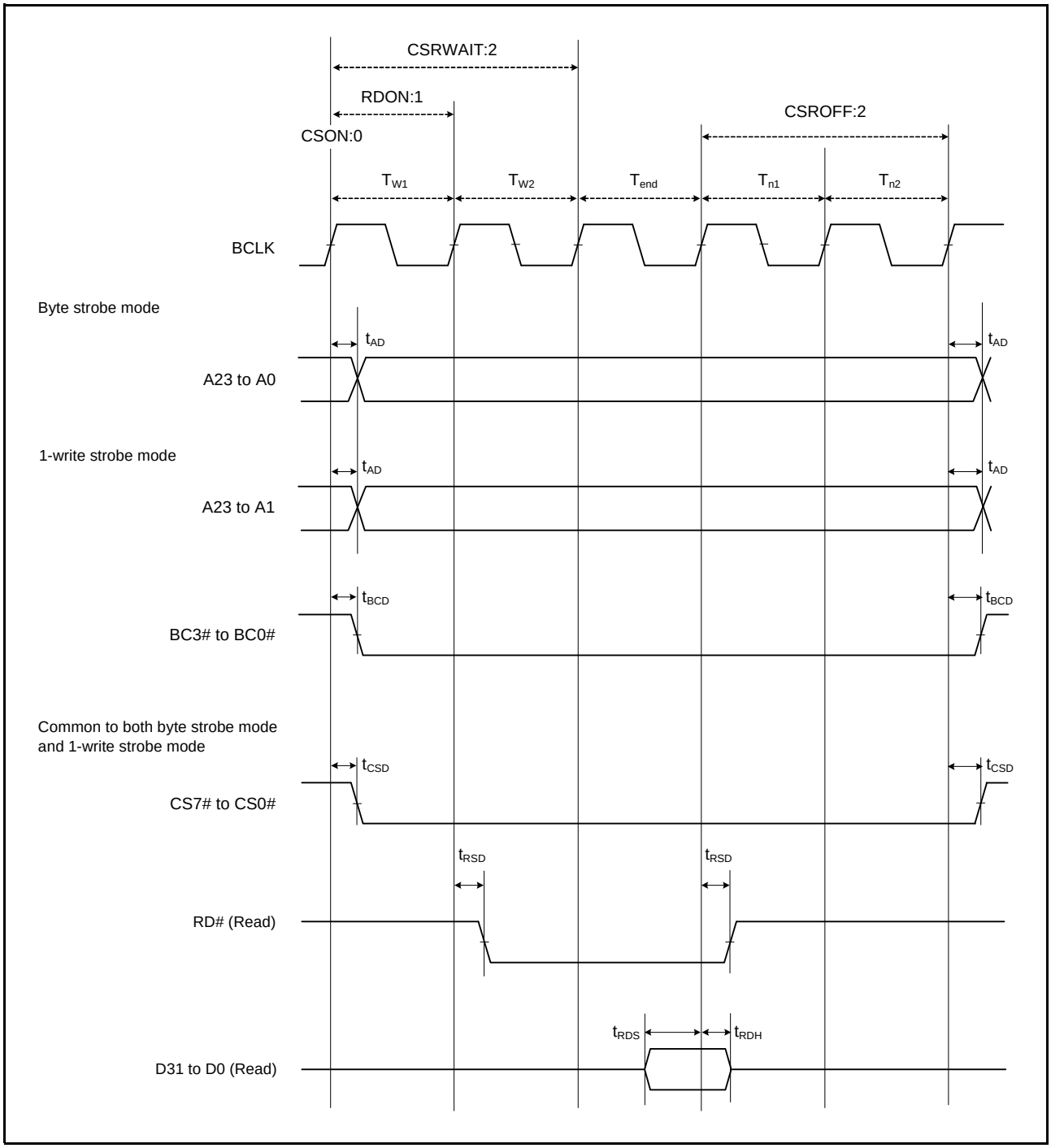
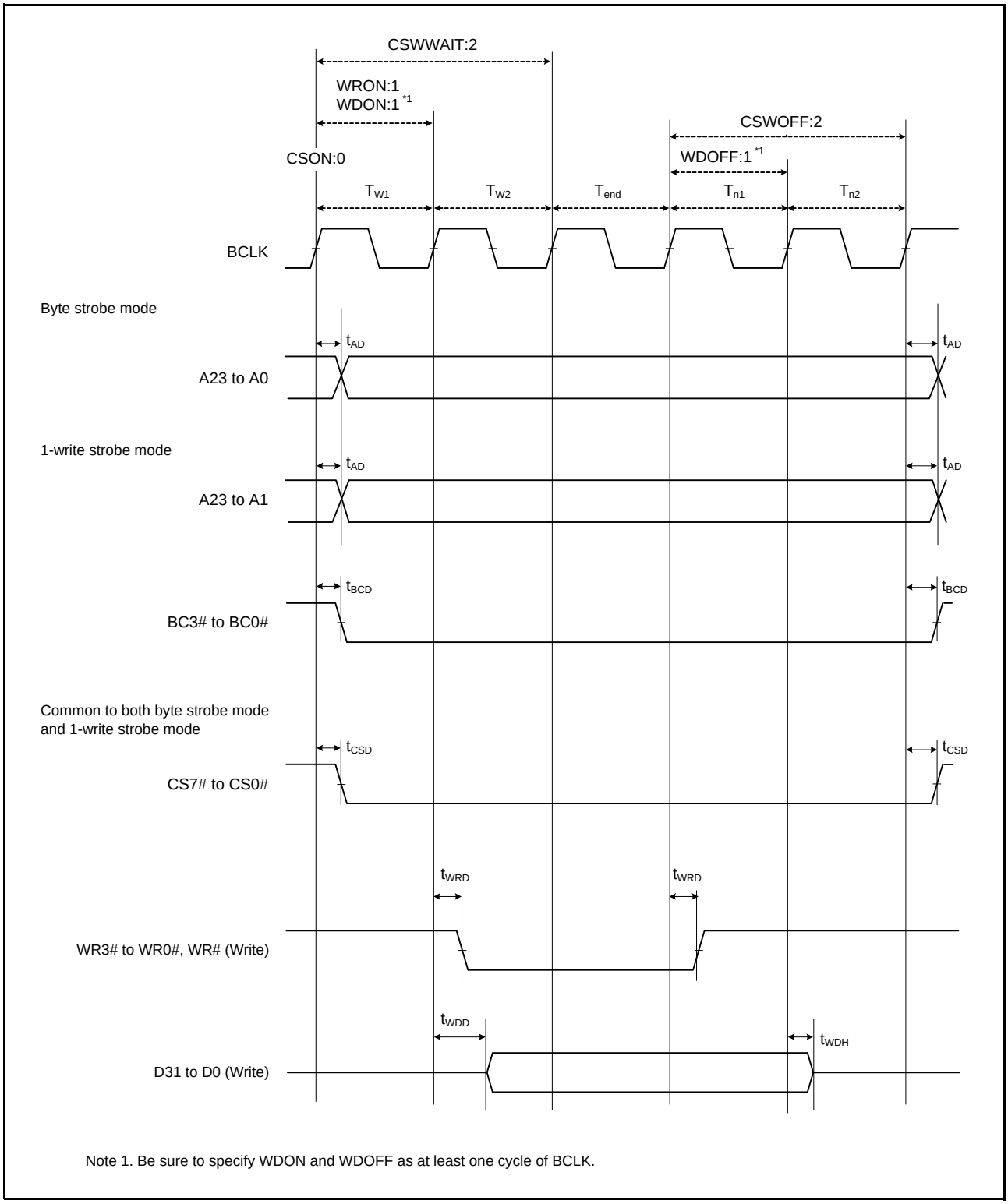


Figure 2.18 External Bus Timing/Normal Read Cycle (Bus Clock Synchronized)



Note 1. Be sure to specify WDON and WDOFF as at least one cycle of BCLK.

Figure 2.19 External Bus Timing/Normal Write Cycle (Bus Clock Synchronized)

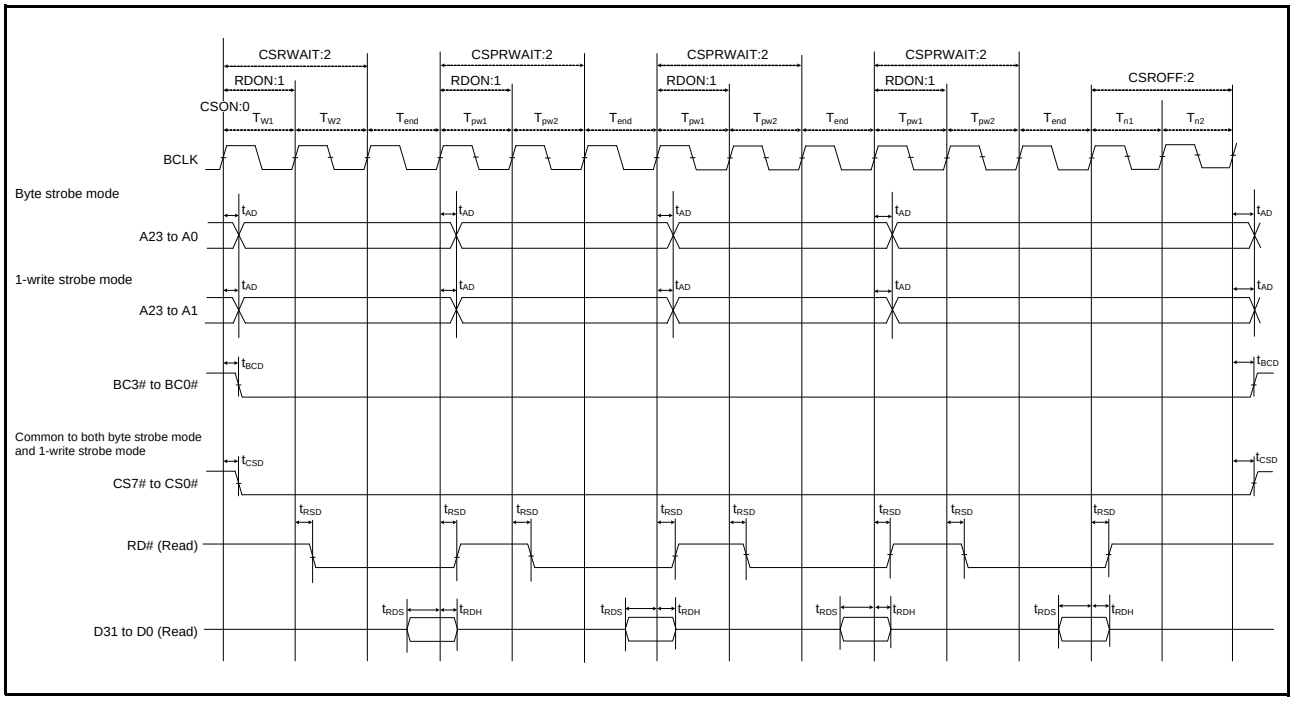
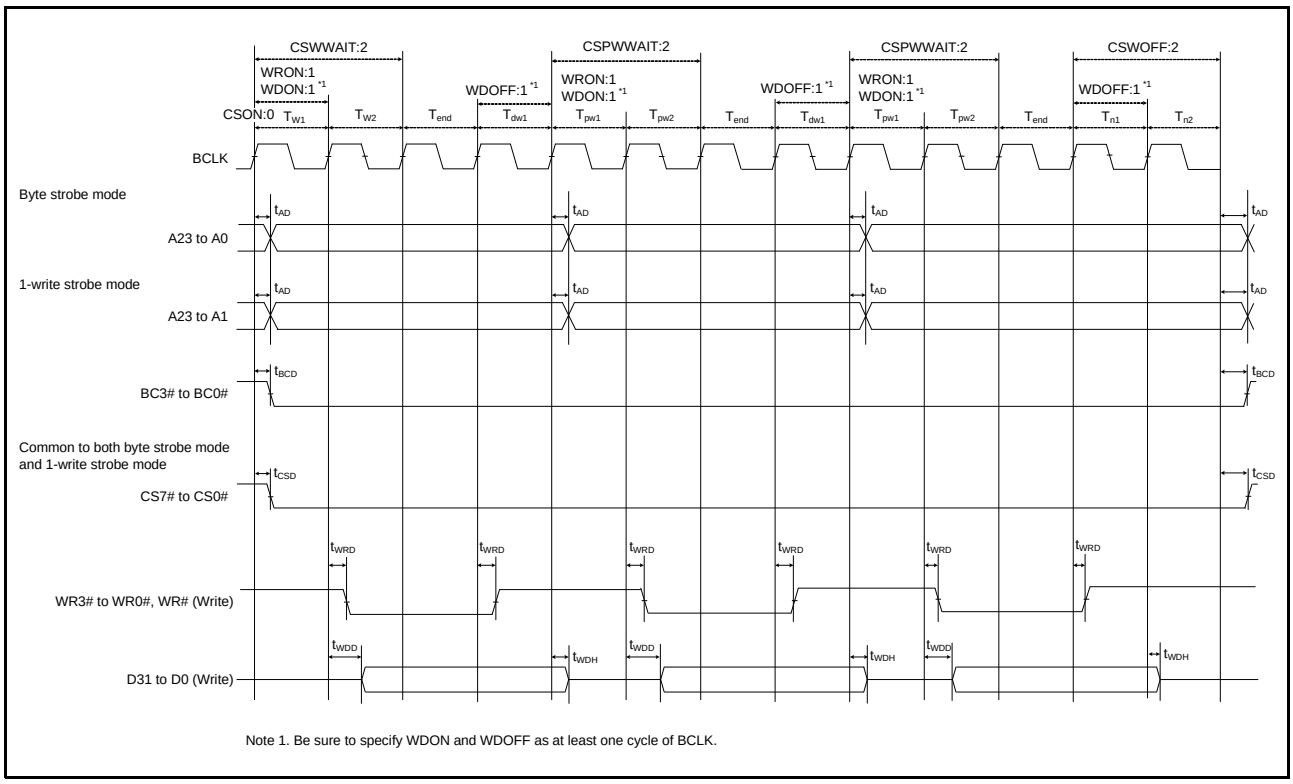


Figure 2.20 External Bus Timing/Page Read Cycle (Bus Clock Synchronized)



Note 1. Be sure to specify WDON and WDOFF as at least one cycle of BCLK.

Figure 2.21 External Bus Timing/Page Write Cycle (Bus Clock Synchronized)

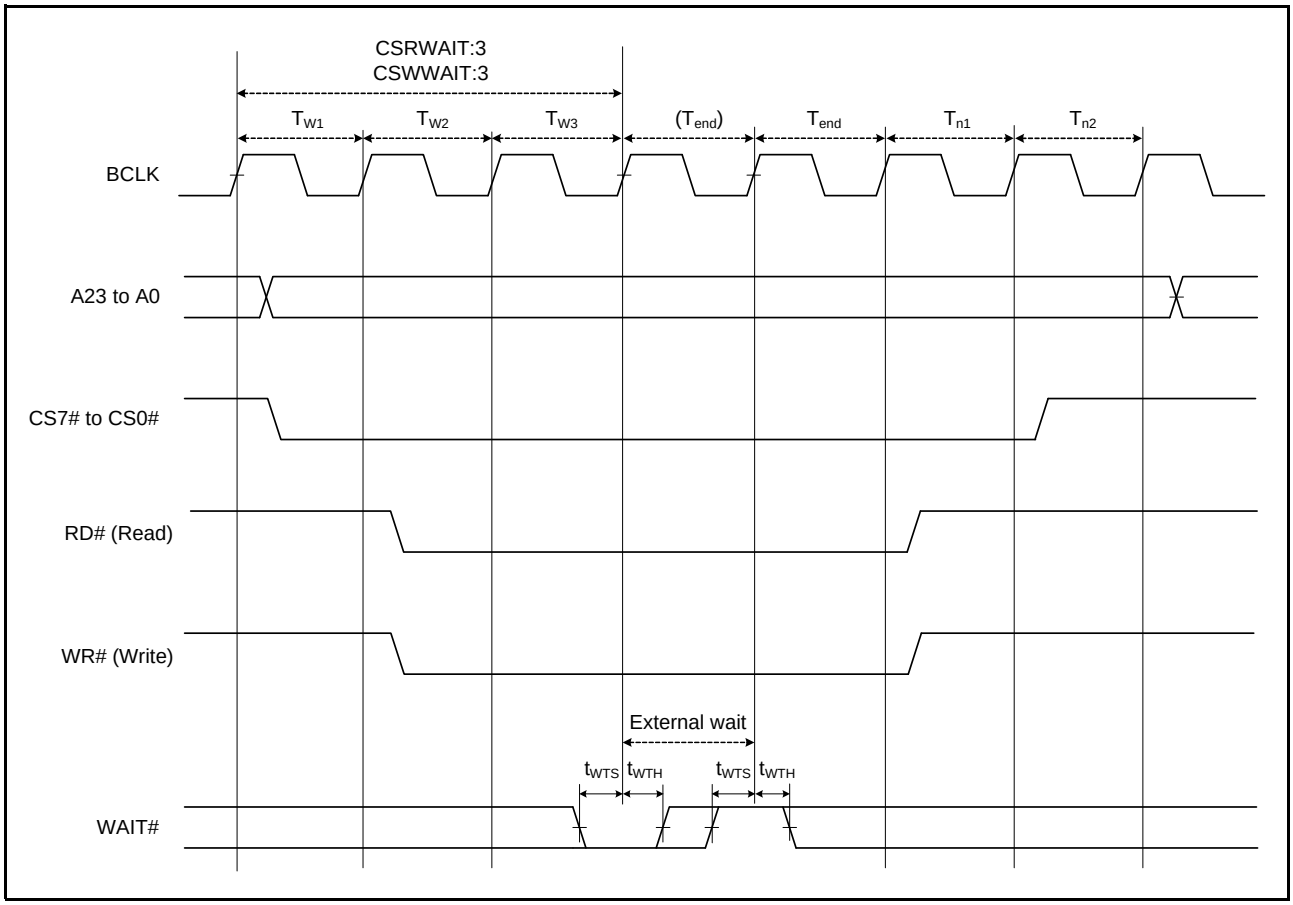
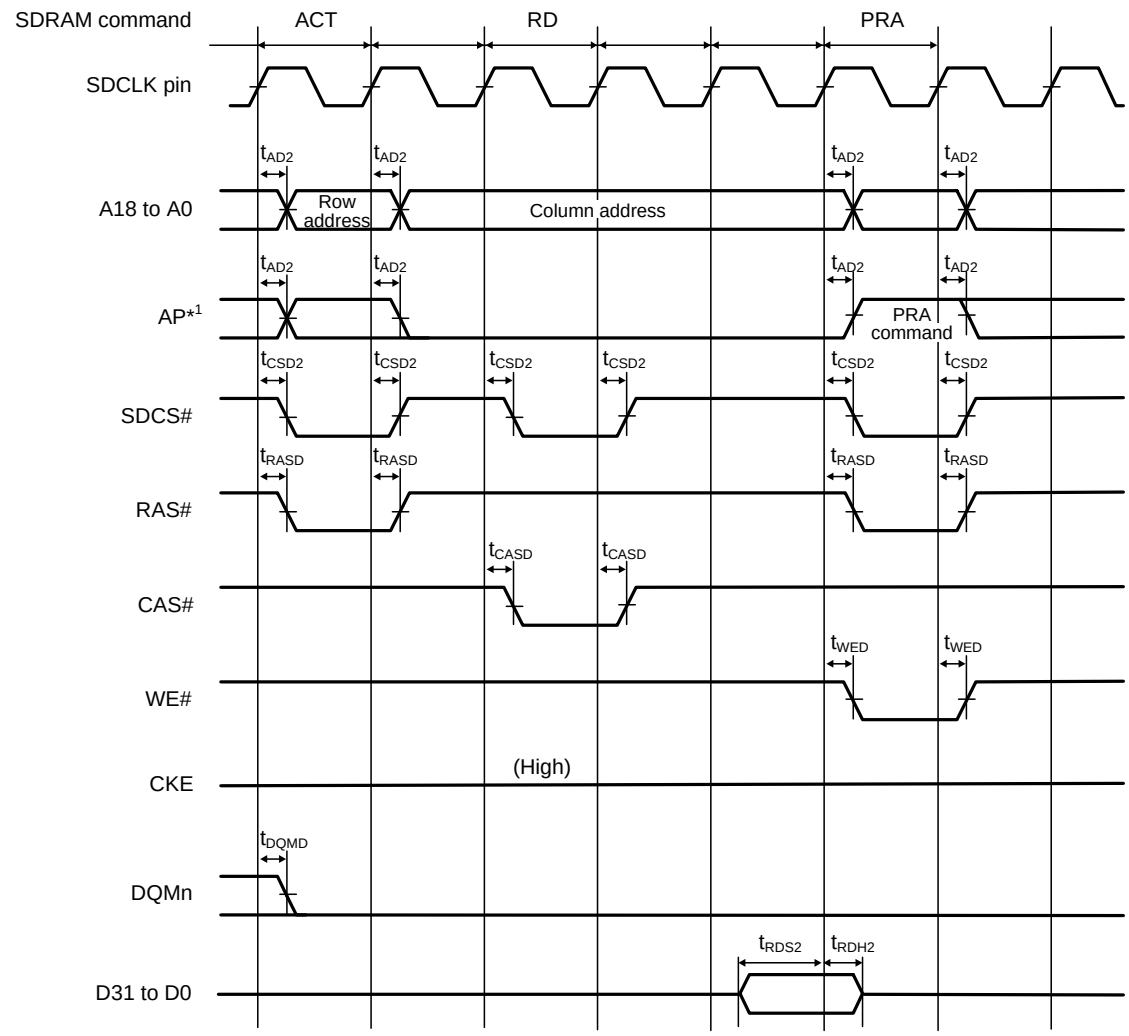
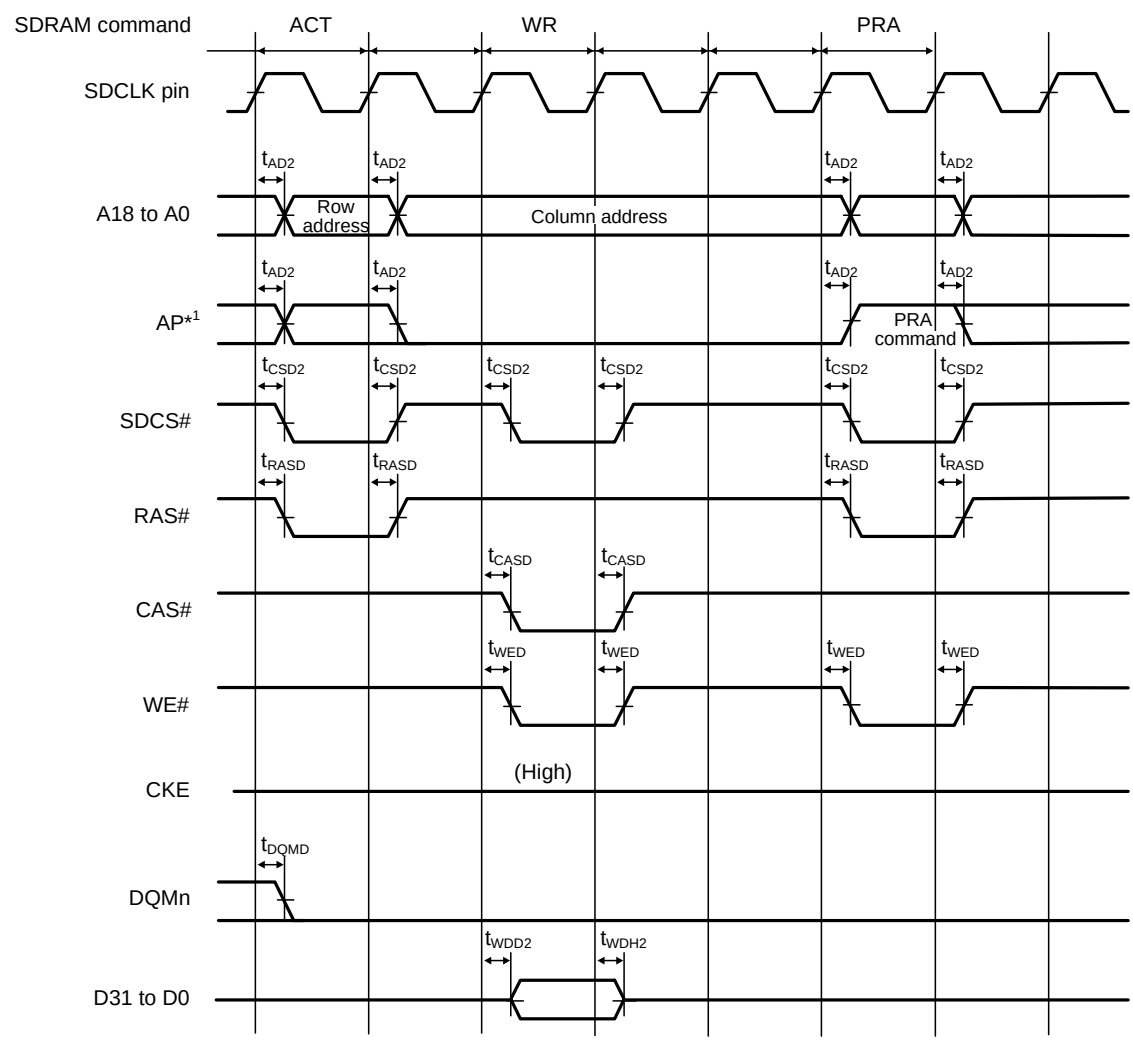


Figure 2.22 External Bus Timing/External Wait Control



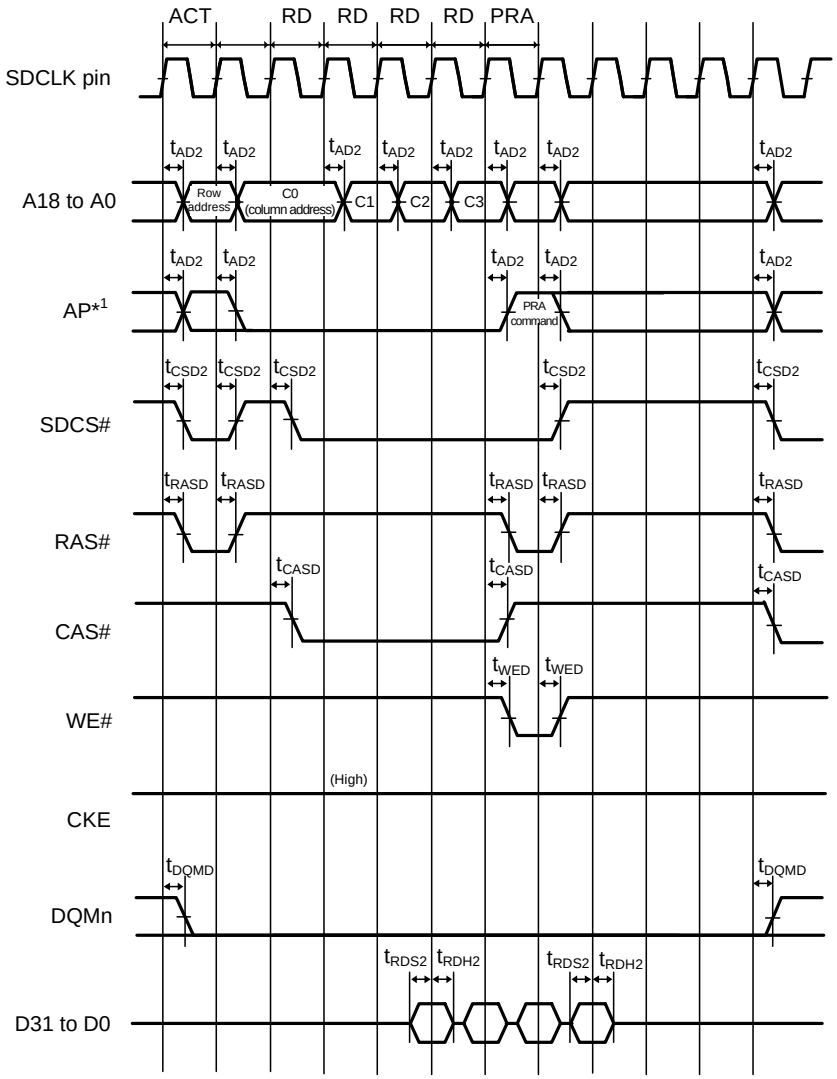
Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 2.23 SDRAM Space Single Read Bus Timing



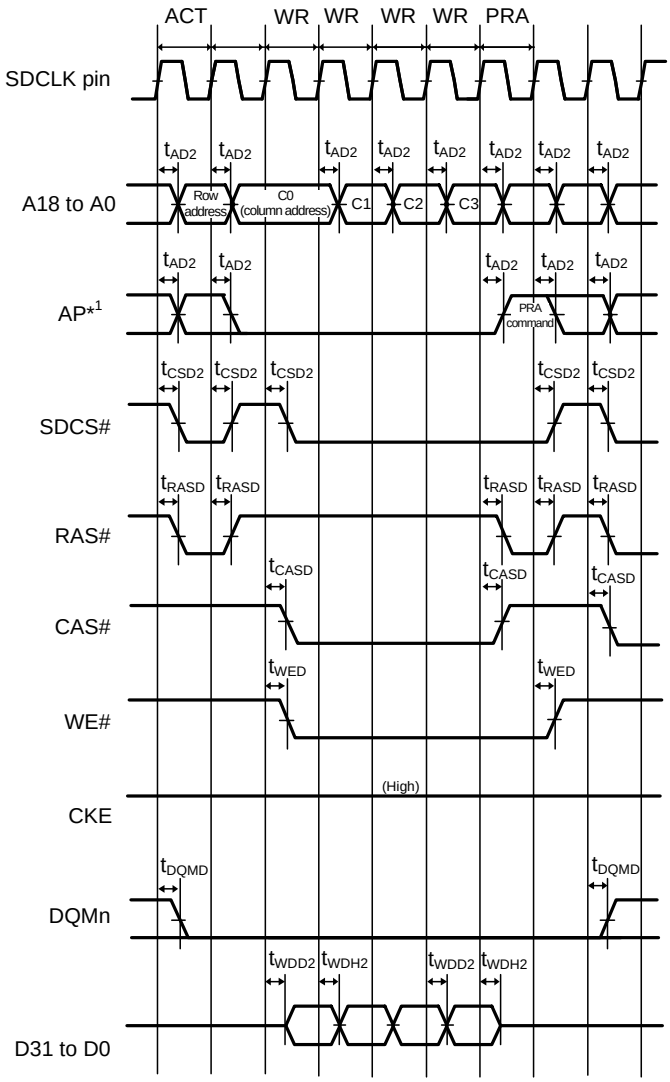
Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 2.24 SDRAM Space Single Write Bus Timing



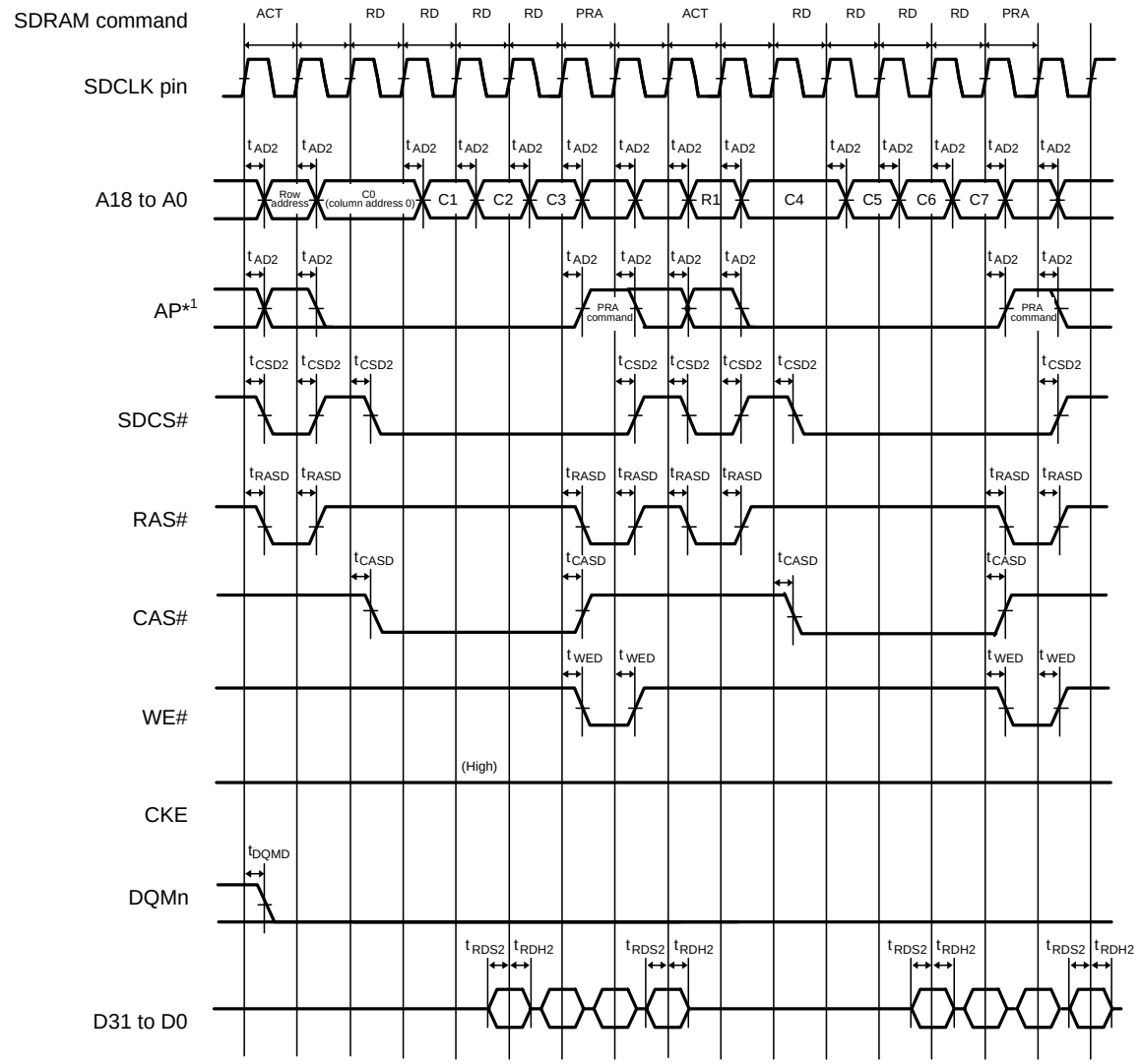
Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 2.25 SDRAM Space Multiple Read Bus Timing



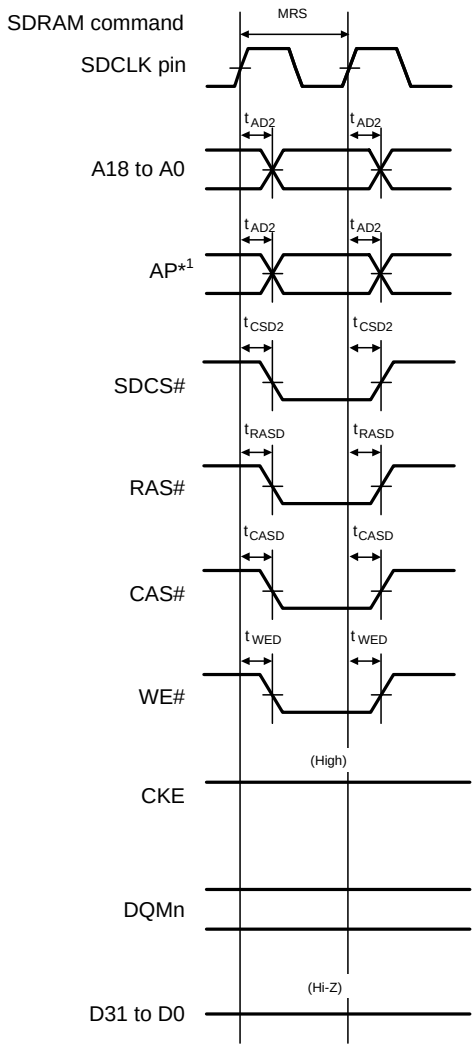
Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 2.26 SDRAM Space Multiple Write Bus Timing



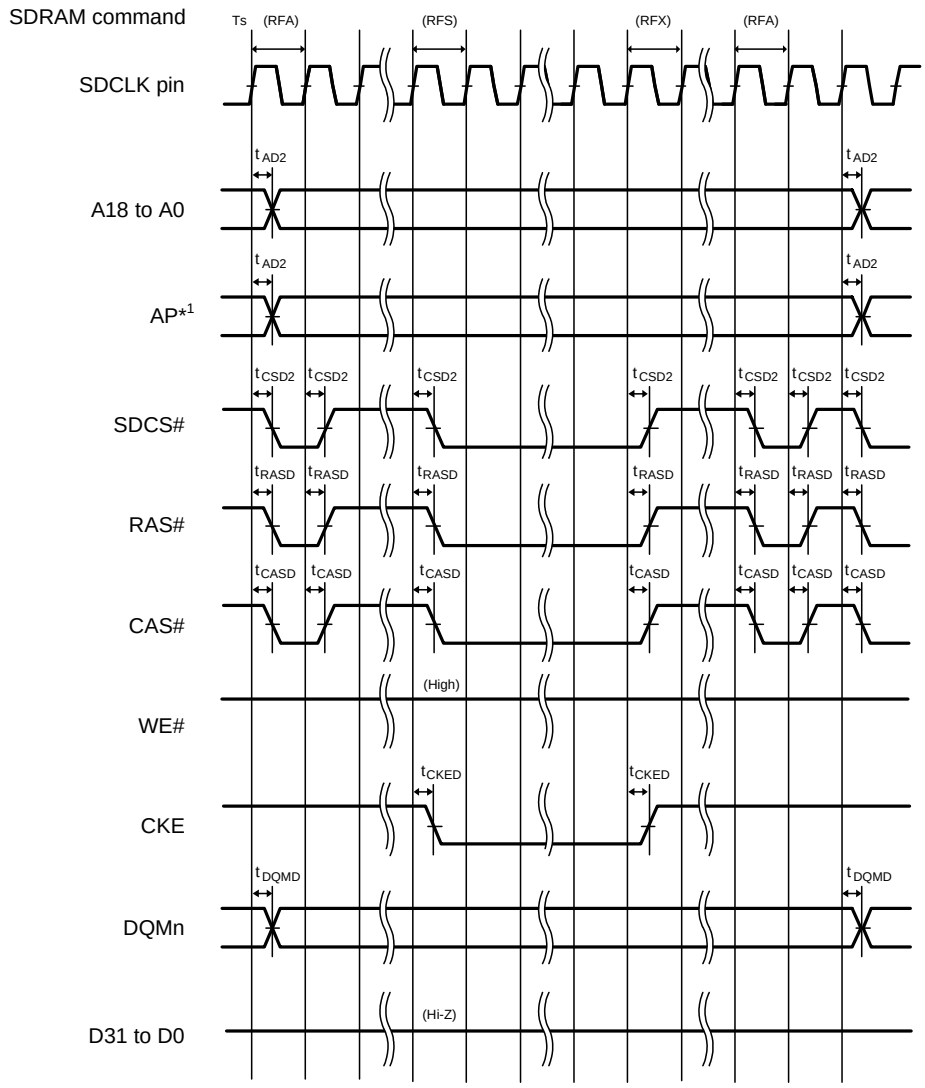
Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 2.27 SDRAM Space Multiple Read Line Stride Bus Timing



Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 2.28 SDRAM Space Mode Register Set Bus Timing



Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 2.29 SDRAM Space Self-Refresh Bus Timing

2.3.6 EXDMAC Timing

Table 2.24 EXDMAC Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
ICLK = 8 to 240 MHz, PCLKA = 8 to 120 MHz, PCLKB = BCLK = SDCLK = 8 to 60 MHz, $T_a = T_{opr}$
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF
High-drive output is selected by the driving ability control register.

Item		Symbol	Min.	Max.	Unit	Test Conditions
EXDMAC	EDREQ setup time	t_{EDRQS}	13	—	ns	Figure 2.30
	EDREQ hold time	t_{EDRQH}	2	—	ns	
	EDACK delay time	t_{EDACD}	—	13	ns	Figure 2.31, Figure 2.32

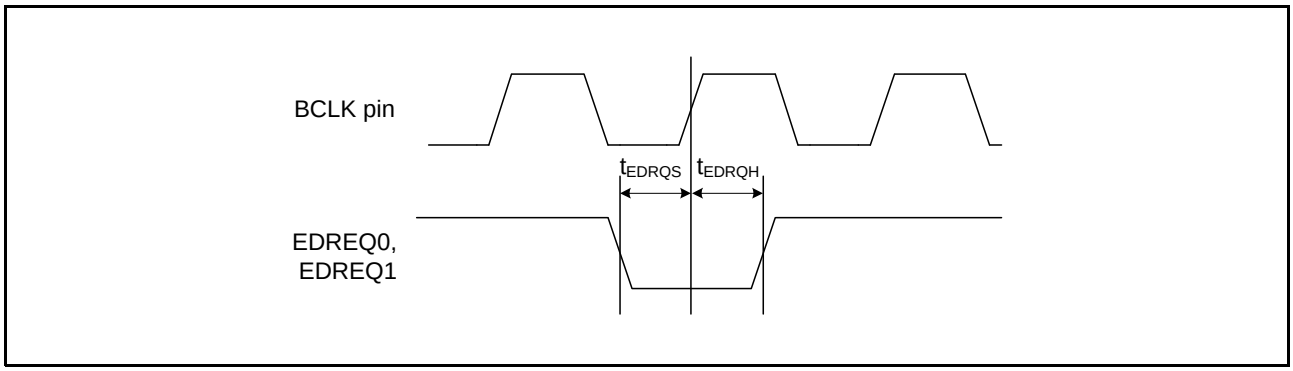


Figure 2.30 EDREQ0 and EDREQ1 Input Timing

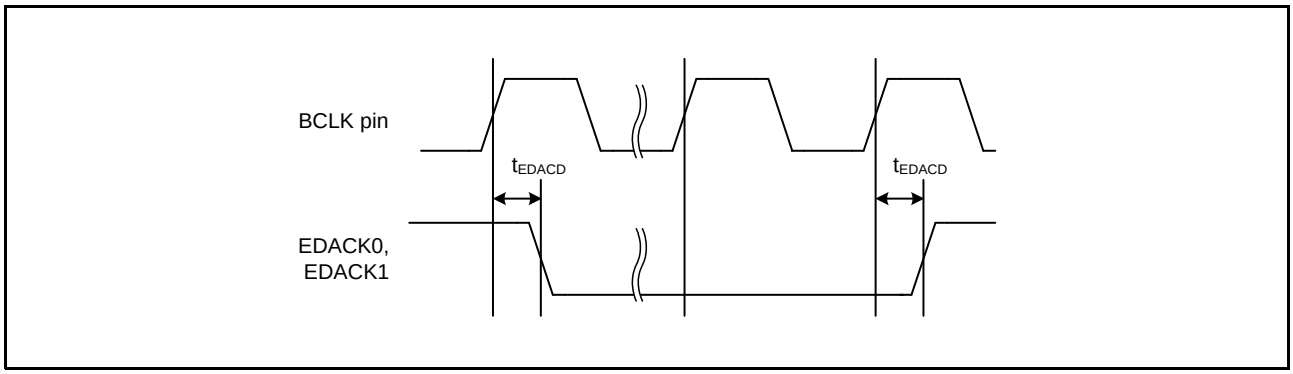


Figure 2.31 EDACK0 and EDACK1 Single-Address Transfer Timing (for a CS Area)

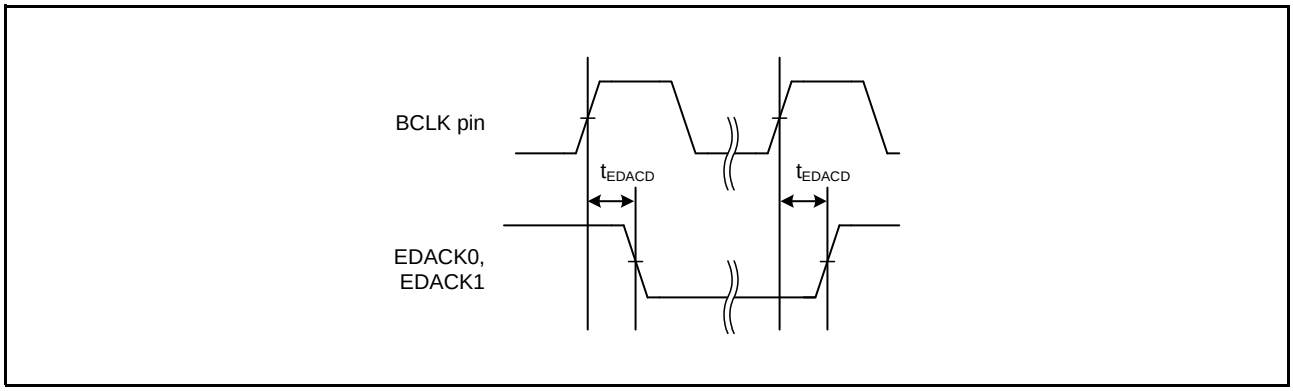


Figure 2.32 EDACK0 and EDACK1 Single-Address Transfer Timing (for SDRAM)

2.3.7 Timing of On-Chip Peripheral Modules

2.3.7.1 I/O Port

Table 2.25 I/O Port Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF
High-drive output is selected by the driving ability control register.

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
I/O ports	Input data pulse width	t_{PRW}	1.5	—	t_{PBcyc}	Figure 2.33

Note 1. t_{PBcyc}: PCLKB cycle

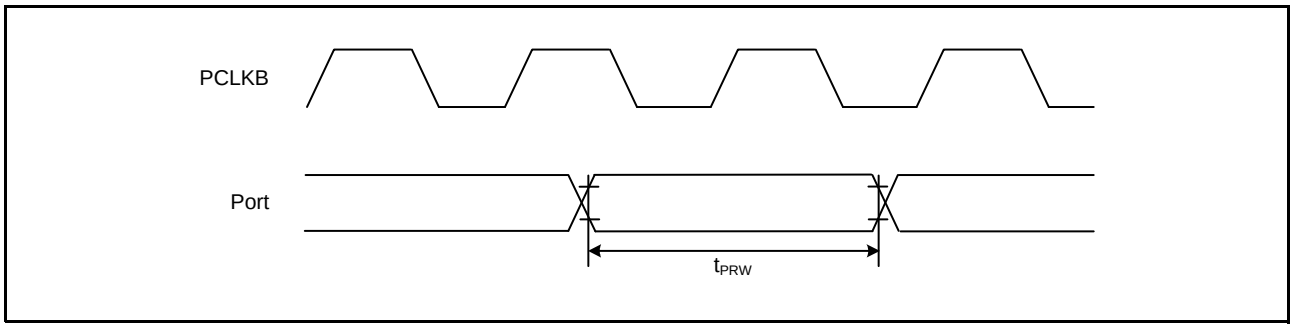


Figure 2.33 I/O Port Input Timing

2.3.7.2 TPU

Table 2.26 TPU Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF
High-drive output is selected by the driving ability control register.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
TPU	Input capture input pulse width	Single-edge setting	t_{TICW}	1.5	—	t_{PBcyc}	Figure 2.34
		Both-edge setting		2.5	—		
	Timer clock pulse width	Single-edge setting	t_{TCKWH}, t_{TCKWL}	1.5	—	t_{PBcyc}	Figure 2.35
		Both-edge setting		2.5	—		
		Phase counting mode		2.5	—		

Note 1. t_{PBcyc}: PCLKB cycle

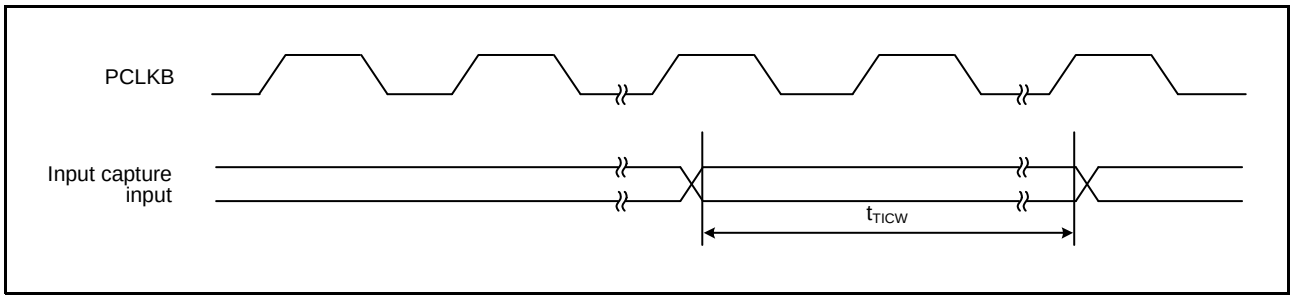


Figure 2.34 TPU Input Capture Input Timing

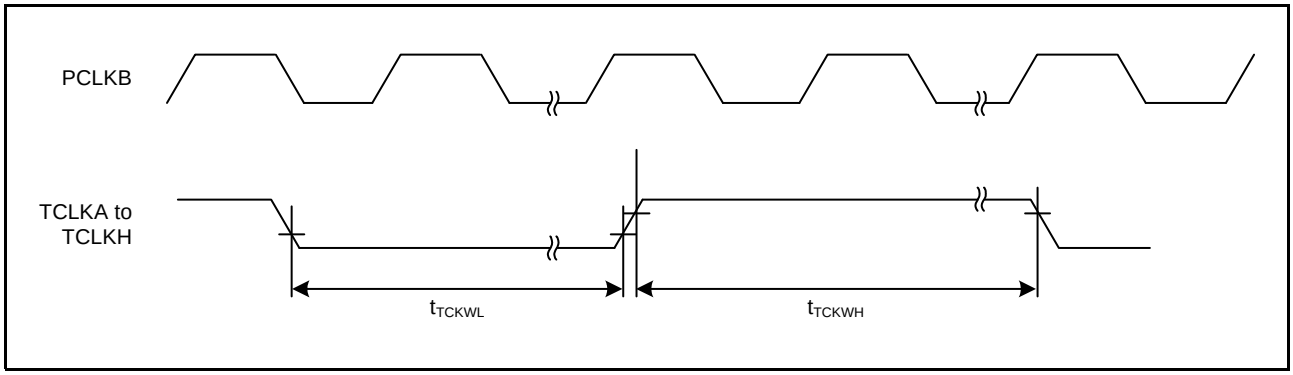


Figure 2.35 TPU Clock Input Timing

2.3.7.3 TMR

Table 2.27 TMR Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF
High-drive output is selected by the driving ability control register.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
TMR	Timer clock pulse width	Single-edge setting	t_{TMCWH}, t_{TMCWL}	1.5	—	t_{PBcyc}	Figure 2.36
		Both-edge setting		2.5	—		

Note 1. t_{PBcyc}: PCLKB cycle

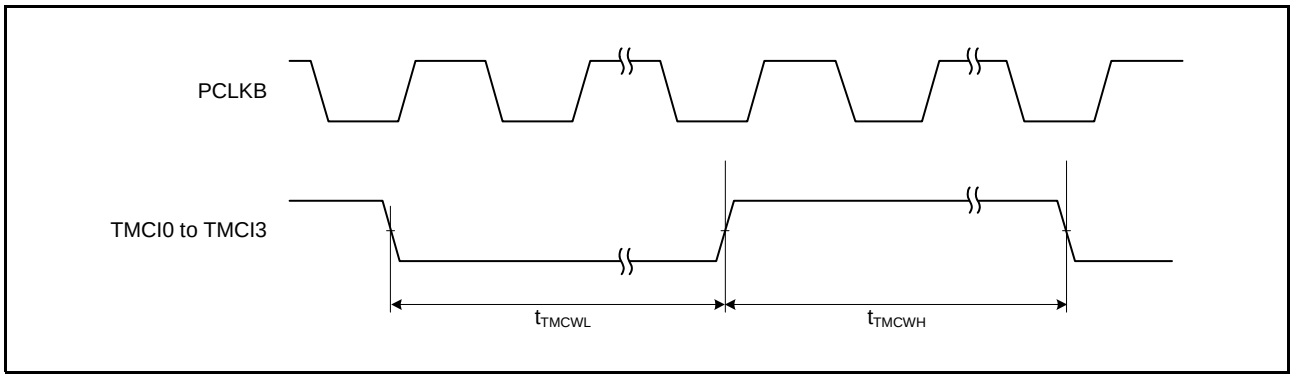


Figure 2.36 TMR Clock Input Timing

2.3.7.4 CMTW

Table 2.28 CMTW Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF
High-drive output is selected by the driving ability control register.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
CMTW	Input capture input pulse width	Single-edge setting	$t_{CMTWTICW}$	1.5	—	t_{PBcyc}	Figure 2.37
		Both-edge setting		2.5	—		

Note 1. t_{PBcyc}: PCLKB cycle

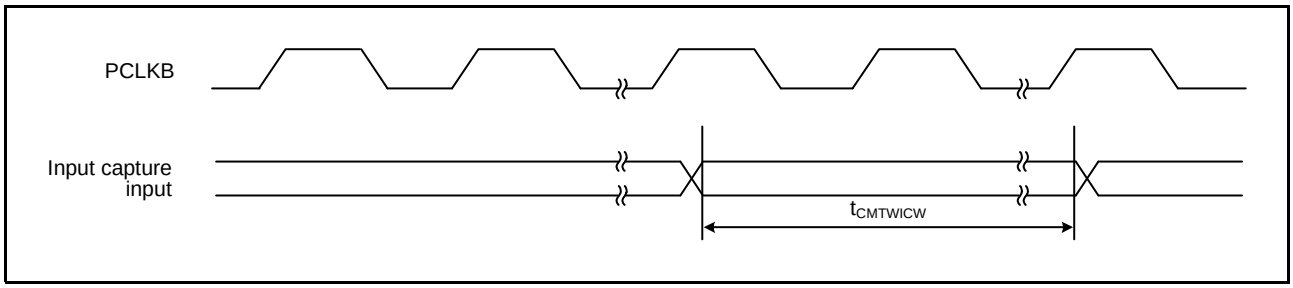


Figure 2.37 CMTW Input Capture Input Timing

2.3.7.5 MTU3

Table 2.29 MTU3 Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF
High-drive output is selected by the driving ability control register.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
MTU3	Input capture input pulse width	Single-edge setting	t_{MTICW}	1.5	—	t_{PAcyc}	Figure 2.38
		Both-edge setting		2.5	—		
	Timer clock pulse width	Single-edge setting	t_{MTCKWH}, t_{MTCKWL}	1.5	—	t_{PAcyc}	Figure 2.39
		Both-edge setting		2.5	—		
		Phase counting mode		2.5	—		

Note 1. t_{PAcyc}: PCLKA cycle

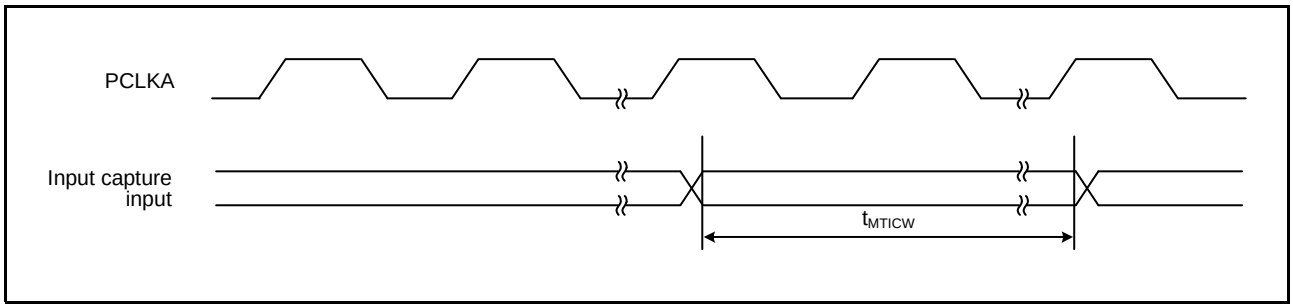


Figure 2.38 MTU3 Input Capture Input Timing

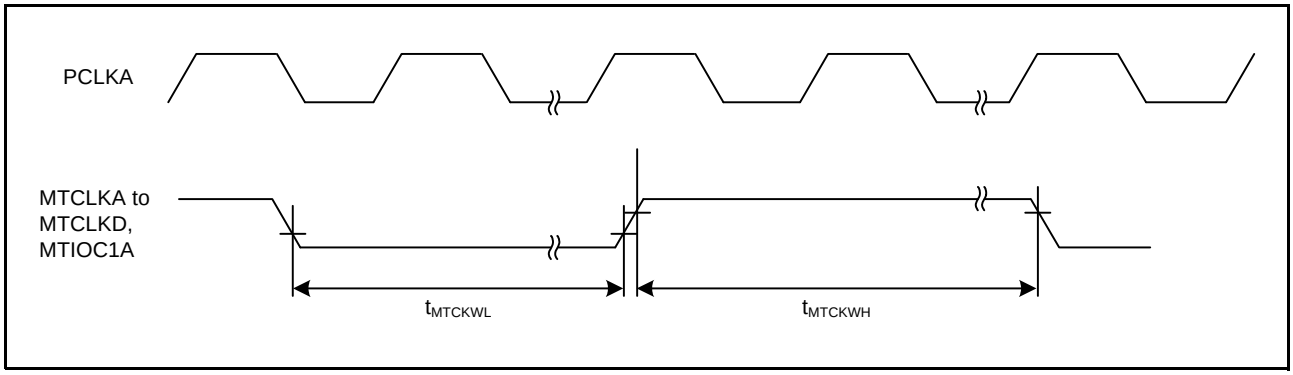


Figure 2.39 MTU3 Clock Input Timing

2.3.7.6 POE3

Table 2.30 POE3 Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF
High-drive output is selected by the driving ability control register.

Item			Symbol	Min.	Typ.	Max.	Unit*1	Test Conditions
POE	POEn# input pulse width		t_{POEW}	1.5	—	—	t_{PBcyc}	Figure 2.40
	Output isable time	Transition of the POEn# signal level	t_{POEDI}	—	—	5 PCLKB + 0.24	µs	Figure 2.41 When detecting falling edges (ICSRm.POEnM[3:0] = 0000b (m = 1 to 5, n = 0, 4, 8, 10, 11))
		Simultaneous conduction of output pins	t_{POEDO}	—	—	3 PCLKB + 0.2	µs	Figure 2.42
		Register setting	t_{POEDS}	—	—	1 PCLKB + 0.2	µs	Figure 2.43 Time for access to the register is not included.
		Oscillation stop detection	t_{POEDOS}	—	—	21	µs	Figure 2.44

Note 1. t_{PBcyc}: PCLKB cycle

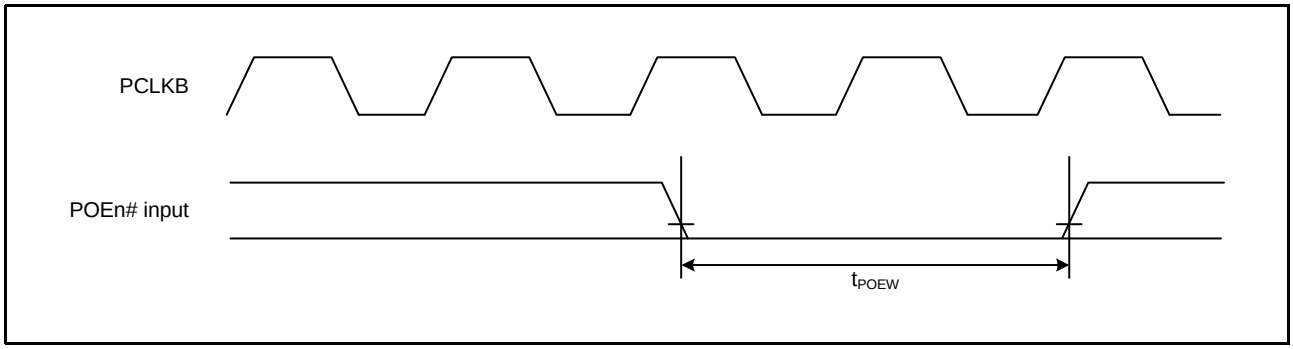


Figure 2.40 POE# Input Timing

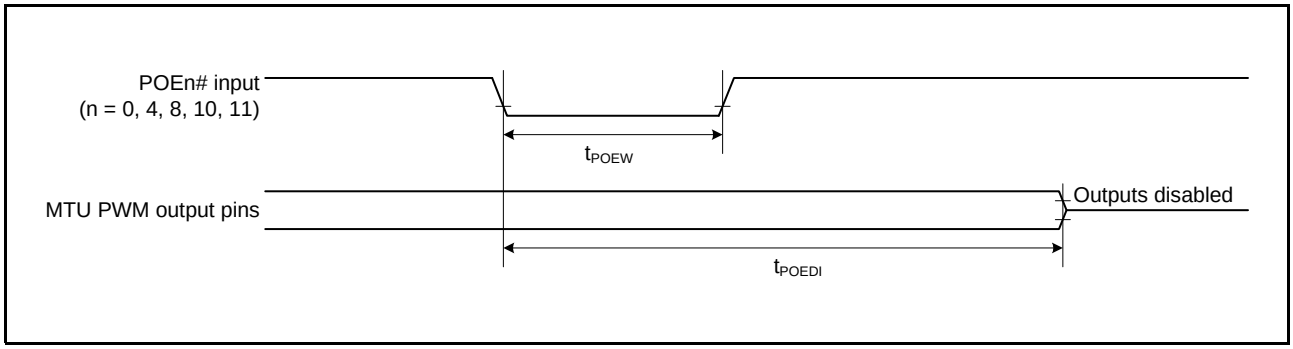
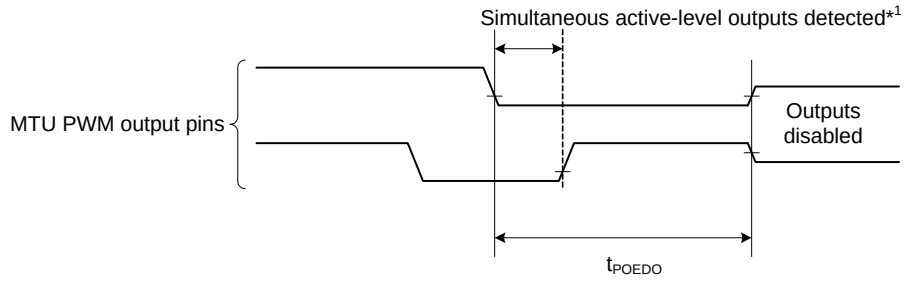


Figure 2.41 Output Disable Time for POE in Response to Transition of the POEn# Signal Level



Note 1. When the active level is set to low.

Figure 2.42 Output Disable Time for POE in Response to the Simultaneous Conduction of Output Pins

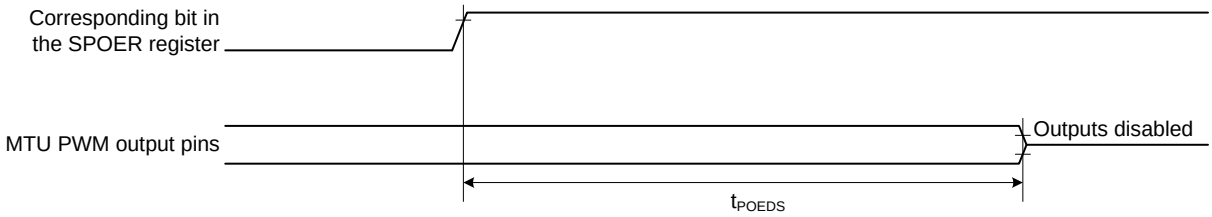


Figure 2.43 Output Disable Time for POE in Response to the Register Setting

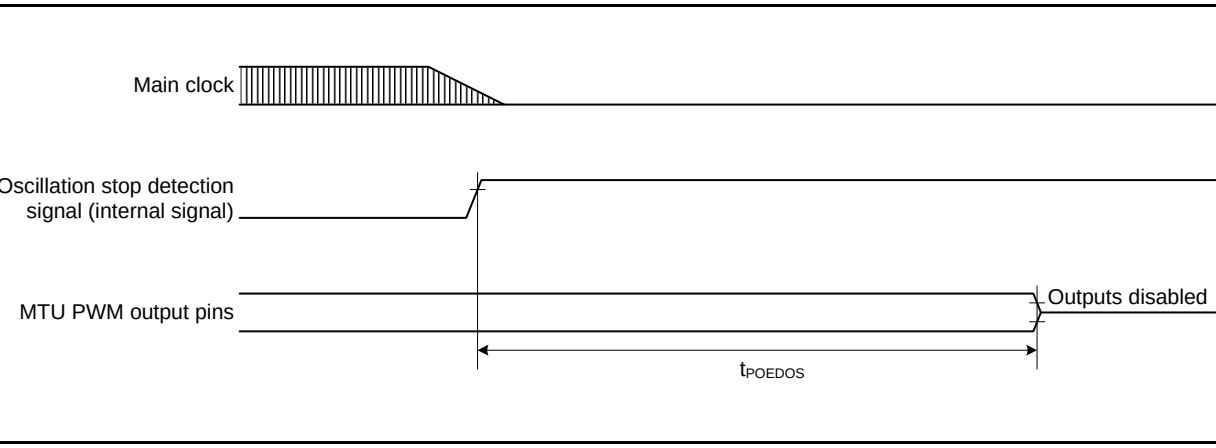


Figure 2.44 Output Disable Time for POE in Response to the Oscillation Stop Detection

2.3.7.7 GPT

Table 2.31 GPT Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF
High-drive output is selected by the driving ability control register.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
GPT	Input capture input pulse width	Single-edge setting	t_{GTICW}	3	—	t_{PAcyc}	Figure 2.45
		Both-edge setting		5	—		
	External trigger input pulse width	Single-edge setting	t_{GTEW}	1.5	—	t_{PAcyc}	Figure 2.46
		Both-edge setting		2.5	—		

Note 1. t_{PAcyc}: PCLKA cycle

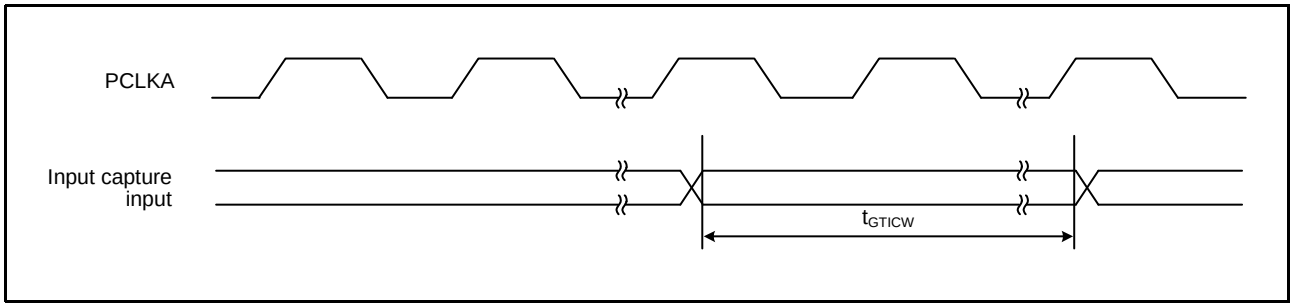


Figure 2.45 GPT Input Capture Input Timing

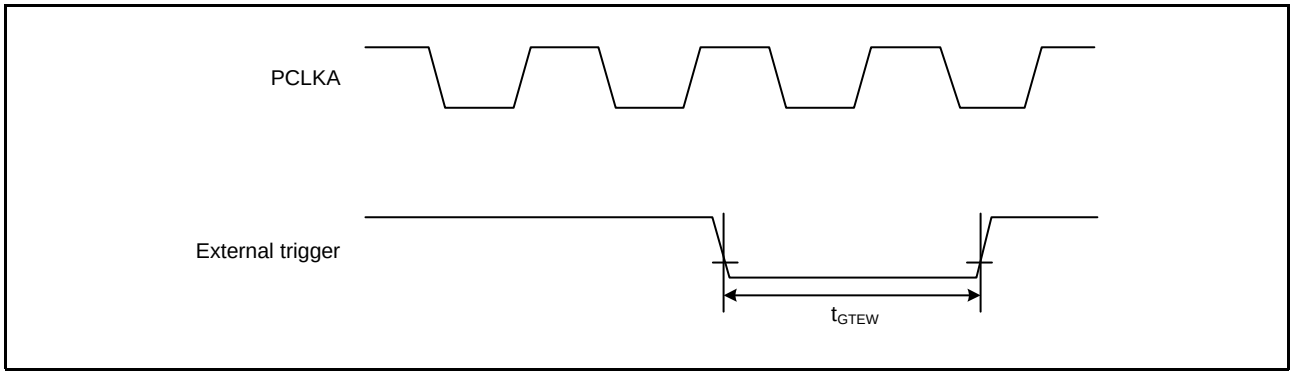


Figure 2.46 GPT External Trigger Input Timing

2.3.7.8 SCI

Table 2.32 SCI and SCIF Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF
High-drive output is selected by the driving ability control register.

Item			Symbol	Min.*1	Max.*1	Unit*1	Test Conditions
SCI	Input clock cycle	Asynchronous	t_{Scyc}	4	—	t_{PBcyc}	Figure 2.47
		Clock synchronous		6	—		
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time		t_{SCKr}	—	5	ns	
	Input clock fall time		t_{SCKf}	—	5	ns	
	Output clock cycle	Asynchronous*2	t_{Scyc}	8	—	t_{PBcyc}	
		Clock synchronous		4	—		
	Output clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time		t_{SCKr}	—	5	ns	
	Output clock fall time		t_{SCKf}	—	5	ns	
	Transmit data delay time	Clock synchronous	t_{TXD}	—	28	ns	Figure 2.48
	Receive data setup time	Clock synchronous	t_{RXS}	15	—	ns	
	Receive data hold time	Clock synchronous	t_{RXH}	5	—	ns	
SCIF	Input clock cycle	Asynchronous	t_{Scyc}	4	—	t_{PAcyc}	Figure 2.47
		Clock synchronous		12	—		
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time		t_{SCKr}	—	5	ns	
	Input clock fall time		t_{SCKf}	—	5	ns	
	Output clock cycle	Asynchronous*3	t_{Scyc}	8	—	t_{PAcyc}	
		Clock synchronous		4	—		
	Output clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time		t_{SCKr}	—	5	ns	
	Output clock fall time		t_{SCKf}	—	5	ns	
	Transmit data delay time	Master	t_{TXD}	—	10	ns	Figure 2.48
		Slave		—	$4 \times t_{PAcyc} + 20$		
	Receive data setup time	Master	t_{RXS}	$3 \times t_{PAcyc} + 20$	—	ns	
		Slave		$t_{PAcyc} + 10$	—		
	Receive data hold time	Master	t_{RXH}	$-3 \times t_{PAcyc} + 5$	—	ns	
		Slave		$2 \times t_{PAcyc} + 10$	—		

Note 1. t_{PBcyc}: PCLKB cycle; t_{PAcyc}: PCLKA cycle
Note 2. When the SEMR.ABCS and SEMR.BGDM bits are set to 1
Note 3. When the SEMR.ABCS0 and SEMR.BGDM bits are set to 1

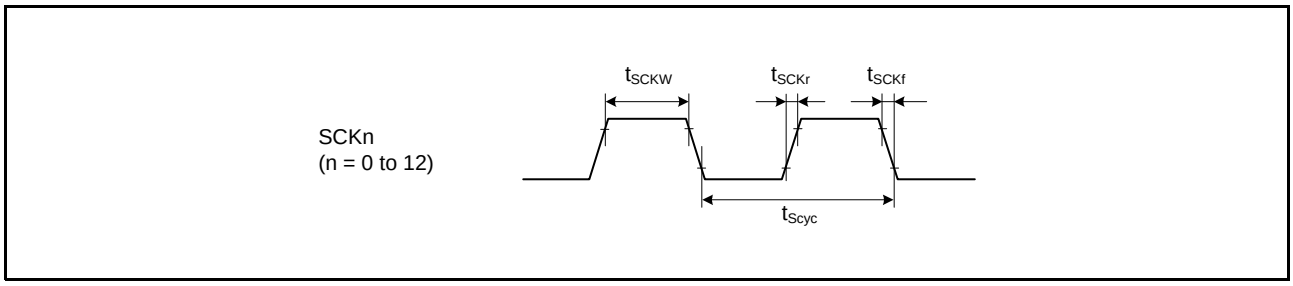


Figure 2.47 SCK Clock Input Timing

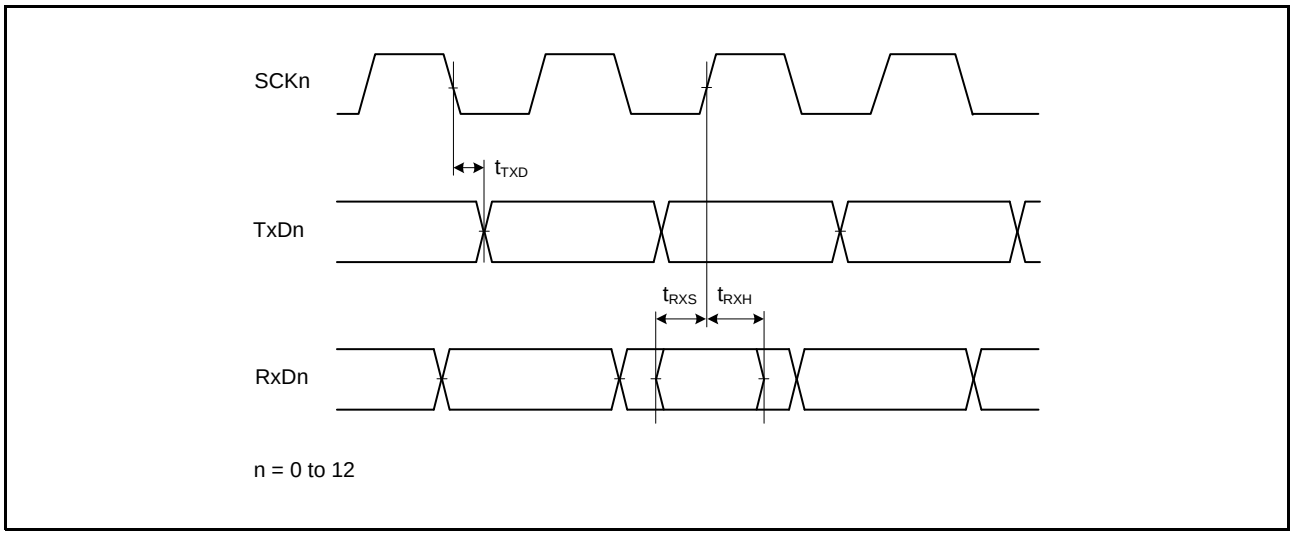


Figure 2.48 SCI Input/Output Timing: Clock Synchronous Mode

Table 2.33 Simple IIC Timing

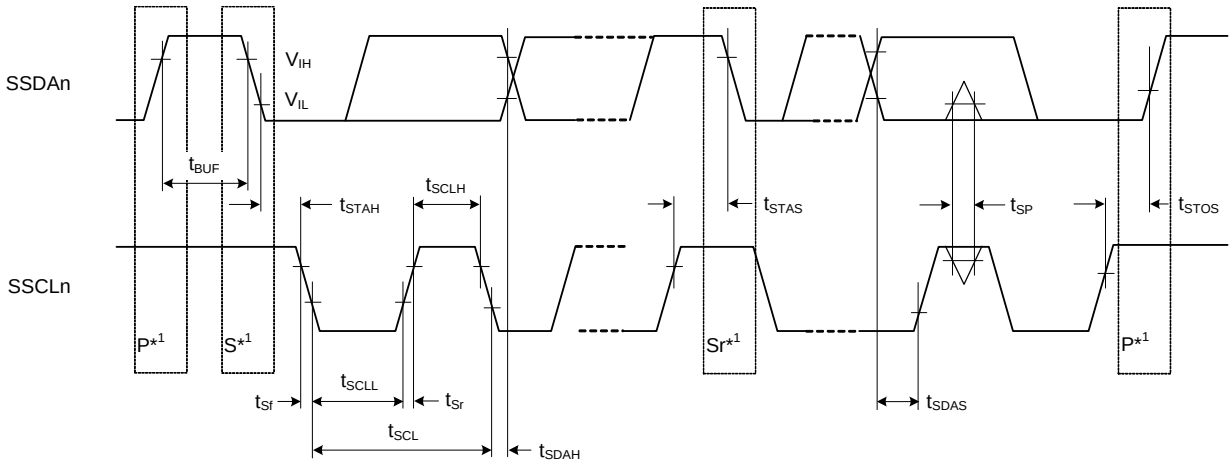
Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$
High-drive output is selected by the driving ability control register.

Item		Symbol	Min.*1, *2	Max.	Unit	Test Conditions
Simple IIC (Standard-mode)	SSDA input rise time	t_{Sr}	—	1000	ns	Figure 2.49
	SSDA input fall time	t_{Sf}	—	300	ns	
	SSDA input spike pulse removal time	t_{SP}	0	4 × t_{PBcyc}	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SSCL, SSDA capacitive load	C_b	—	400	pF	
Simple IIC (Fast-mode)	SSCL, SSDA input rise time	t_{Sr}	—	300	ns	
	SSCL, SSDA input fall time	t_{Sf}	—	300	ns	
	SSCL, SSDA input spike pulse removal time	t_{SP}	0	4 × t_{PBcyc}	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SSCL, SSDA capacitive load	C_b	—	400	pF	

Note: t_{IICcyc}: RIIC internal reference clock (IICφ) cycle
Note 1. The value within parentheses is applicable when the value of the ICMR3.NF[1:0] bits is 11b while the digital filter is enabled by

the setting ICFER.NFE = 1.

Note 2. Cb is the total capacitance of the bus lines.



Note 1. S, P, and Sr indicate the following conditions.
S: Start condition
P: Stop condition
Sr: Restart condition

n = 0 to 7, 12

Test conditions
V_{IH} = 0.7 × VCC, V_{IL} = 0.3 × VCC
V_{OL} = 0.6 V, I_{OL} = 6 mA

Figure 2.49 Simple IIC Bus Interface Input/Output Timing

Table 2.34 Simple SPI Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF
High-drive output is selected by the driving ability control register.

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)	t_{SPcyc}	4	65536	t_{PBcyc}	Figure 2.50
	SCK clock cycle input (slave)		8	65536		
	SCK clock high pulse width	t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width	t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise/fall time	t_{SPCKr}, t_{SPCKf}	—	20	ns	
	Data input setup time	t_{SU}	33.3	—	ns	Figure 2.51 to Figure 2.54
	Data input hold time	t_H	33.3	—	ns	
	SS input setup time	t_{LEAD}	1	—	t_{SPcyc}	
	SS input hold time	t_{LAG}	1	—	t_{SPcyc}	
	Data output delay time	t_{OD}	—	33.3	ns	
	Data output hold time	t_{OH}	–10	—	ns	
	Data rise/fall time	t_{Dr}, t_{Df}	—	16.6	ns	
	SS input rise/fall time	t_{SSLr}, t_{SSLf}	—	16.6	ns	
	Slave access time	t_{SA}	—	5	t_{PBcyc}	Figure 2.53, Figure 2.54
	Slave output release time	t_{REL}	—	5	t_{PBcyc}	

Note 1. t_{PBcyc}: PCLKB cycle

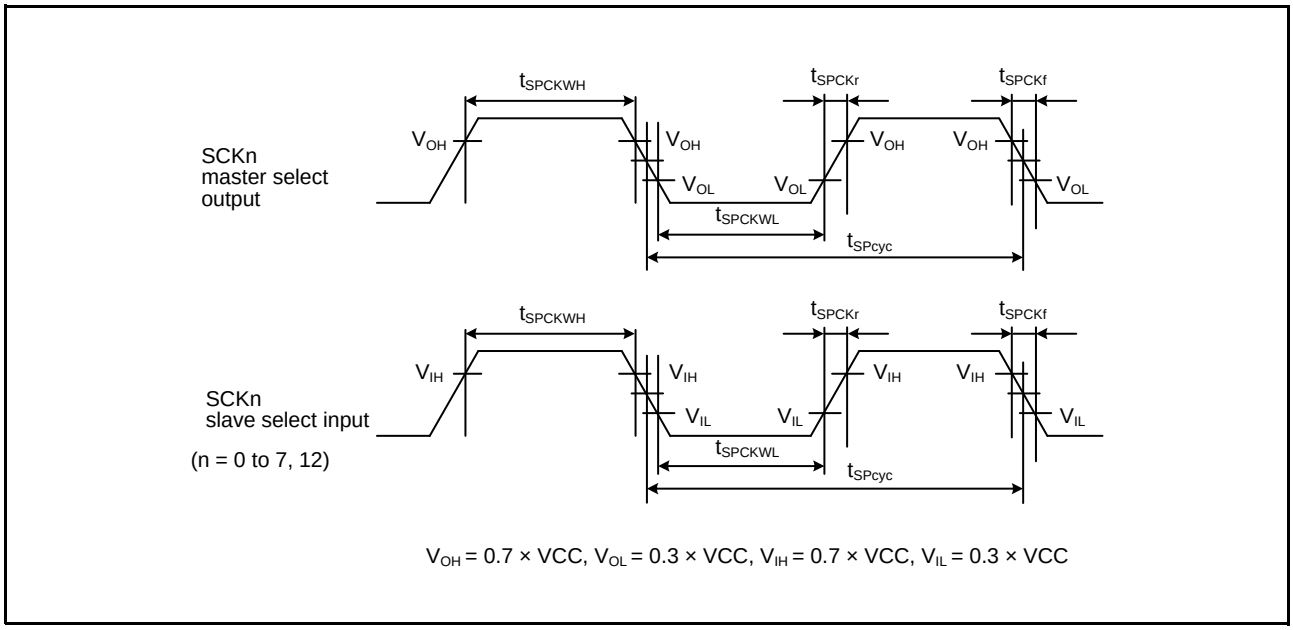


Figure 2.50 Simple SPI Clock Timing

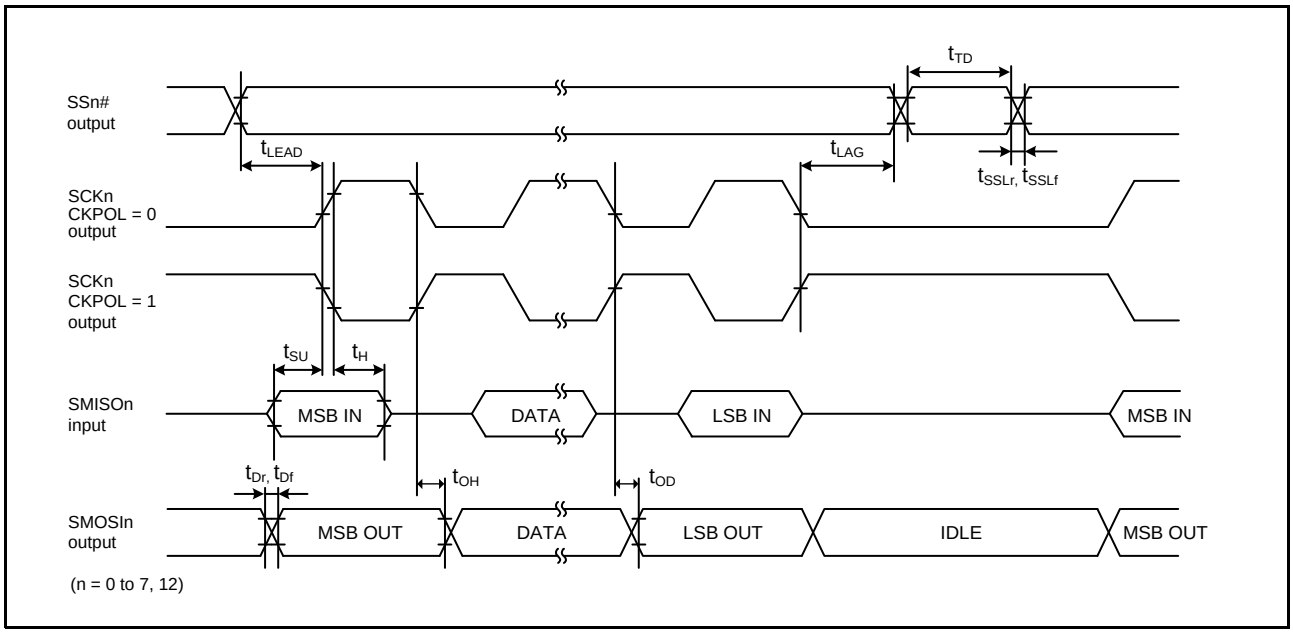


Figure 2.51 Simple SPI Timing (Master, CKPH = 1)

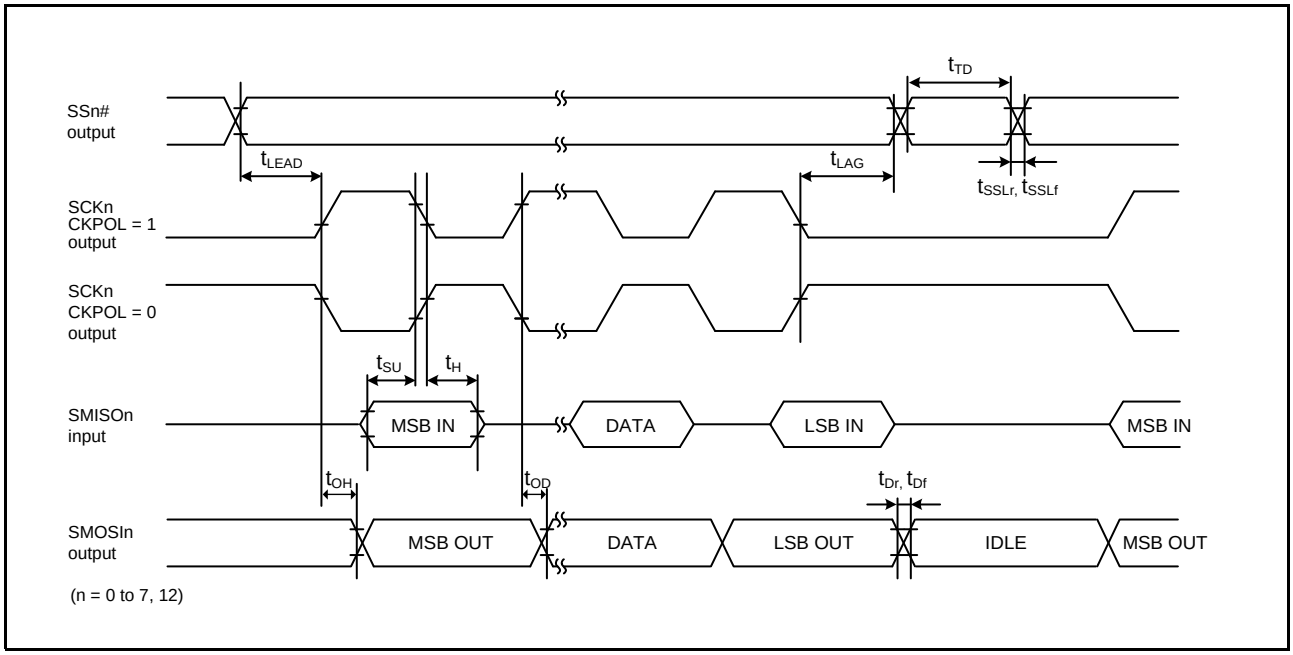


Figure 2.52 Simple SPI Timing (Master, CKPH = 0)

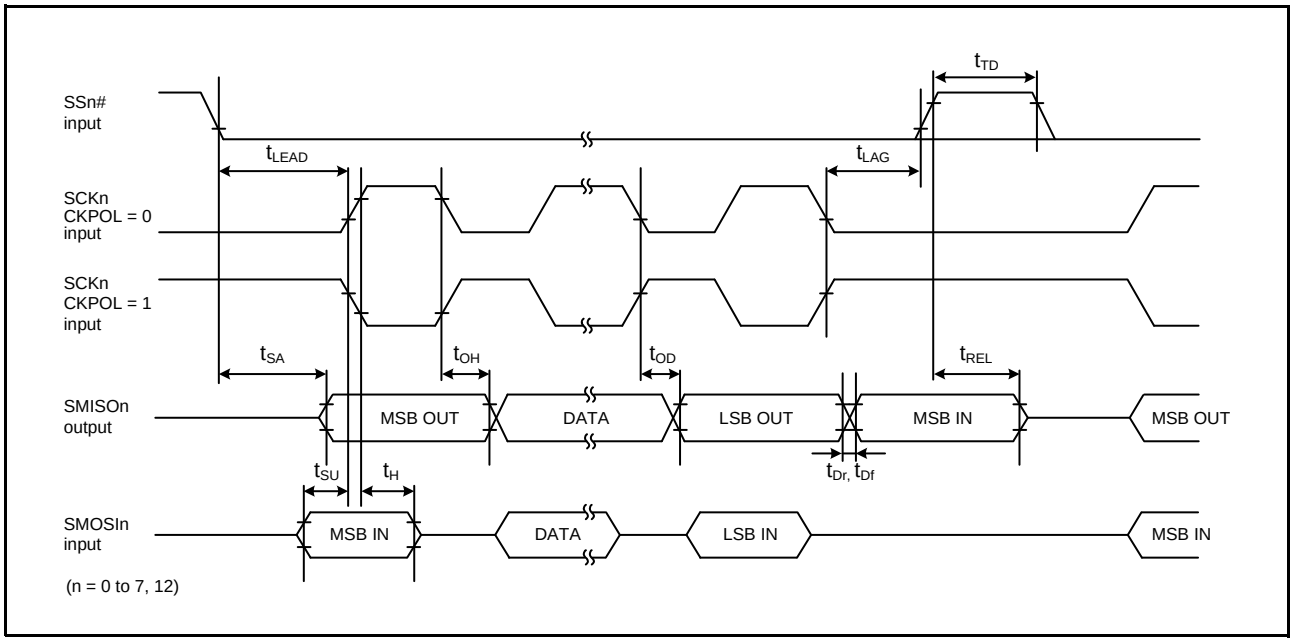


Figure 2.53 Simple SPI Timing (Slave, CKPH = 1)

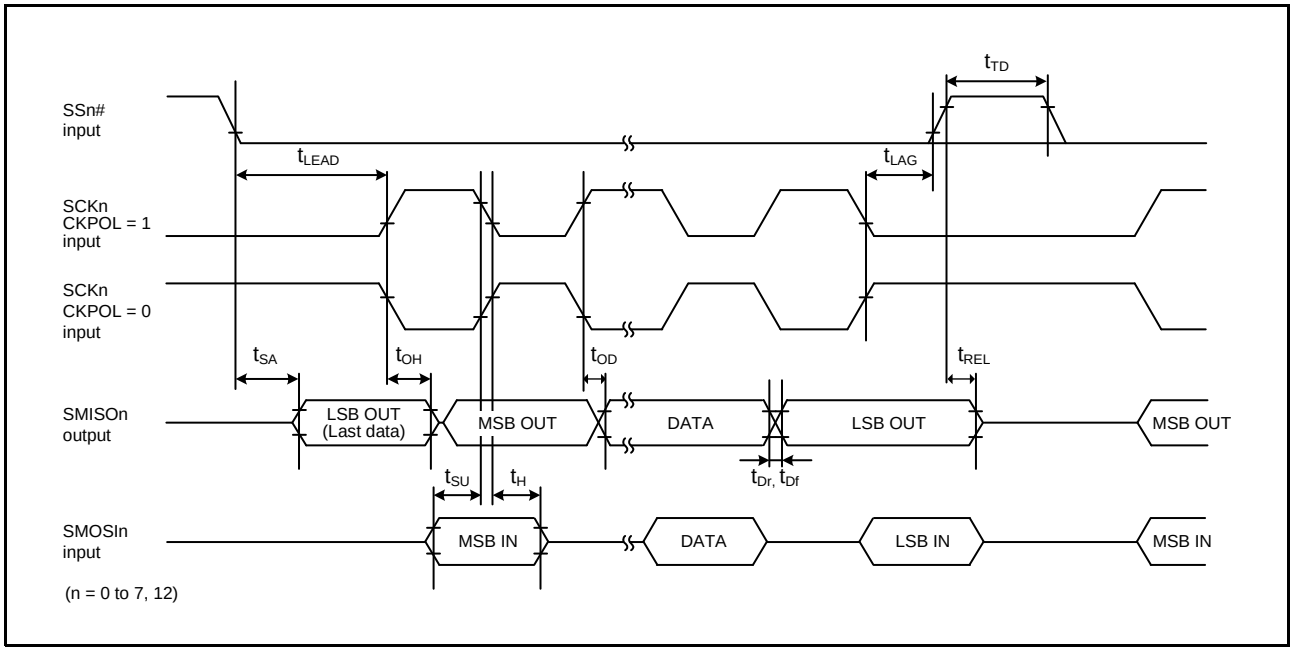


Figure 2.54 Simple SPI Timing (Slave, CKPH = 0)

2.3.7.9 RIIC

Table 2.35 RIIC Timing (1/2)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$
High-drive output is selected by the driving ability control register.

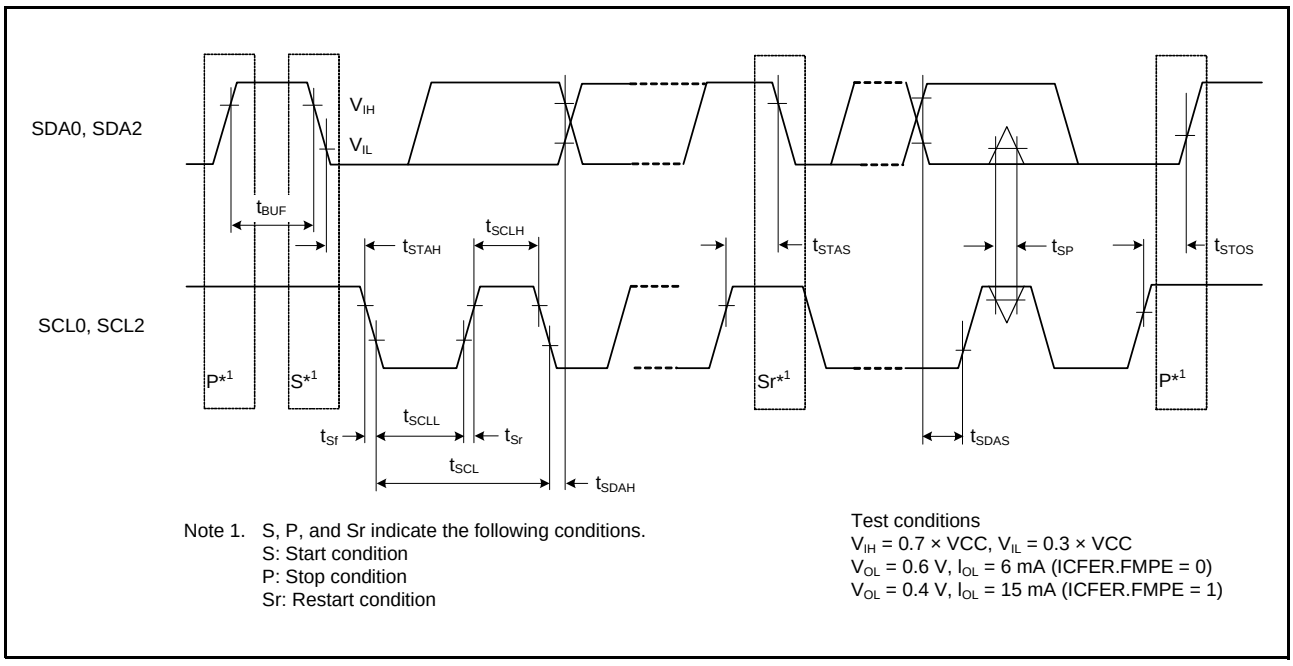
Item		Symbol	Min.*1, *2	Max.	Unit	Test Conditions
RIIC (Standard-mode, SMBus) ICFER.FMPE = 0	SCL input cycle time	t_{SCL}	6(12) × t_{IICcyc} + 1300	—	ns	Figure 2.55
	SCL input high pulse width	t_{SCLH}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rise time	t_{Sr}	—	1000	ns	
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3(6) × t_{IICcyc} + 300	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Restart condition input setup time	t_{STAS}	1000	—	ns	
	Stop condition input setup time	t_{STOS}	1000	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
RIIC (Fast-mode) ICFER.FMPE = 0	SCL input cycle time	t_{SCL}	6(12) × t_{IICcyc} + 600	—	ns	
	SCL input high pulse width	t_{SCLH}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rise time	t_{Sr}	20 × (External pull-up voltage / 5.5 V)	300	ns	
	SCL, SDA input fall time	t_{Sf}	20 × (External pull-up voltage / 5.5 V)	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3(6) × t_{IICcyc} + 300	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Restart condition input setup time	t_{STAS}	300	—	ns	
	Stop condition input setup time	t_{STOS}	300	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Table 2.35 RIIC Timing (2/2)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$
High-drive output is selected by the driving ability control register.

Item		Symbol	Min.*1, *2	Max.	Unit	Test Conditions
RIIC (Fast-mode+) ICFER.FMPE = 1	SCL input cycle time	t_{SCL}	6(12) × t_{IICcyc} + 240	—	ns	Figure 2.55
	SCL input high pulse width	t_{SCLH}	3(6) × t_{IICcyc} + 120	—	ns	
	SCL input low pulse width	t_{SCLL}	3(6) × t_{IICcyc} + 120	—	ns	
	SCL, SDA input rise time	t_{Sr}	—	120	ns	
	SCL, SDA input fall time	t_{Sf}	—	120	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3(6) × t_{IICcyc} + 120	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 120	—	ns	
	Restart condition input setup time	t_{STAS}	120	—	ns	
	Stop condition input setup time	t_{STOS}	120	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 20	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	550	pF	

Note: t_{IICcyc}: RIIC internal reference clock (IICφ) cycle
Note 1. The value within parentheses is applicable when the value of the ICMR3.NF[1:0] bits is 11b while the digital filter is enabled by the setting ICFER.NFE = 1.
Note 2. Cb is the total capacitance of the bus lines.



Note 1. S, P, and Sr indicate the following conditions.
S: Start condition
P: Stop condition
Sr: Restart condition

Test conditions
V_{IH} = 0.7 × VCC, V_{IL} = 0.3 × VCC
V_{OL} = 0.6 V, I_{OL} = 6 mA (ICFER.FMPE = 0)
V_{OL} = 0.4 V, I_{OL} = 15 mA (ICFER.FMPE = 1)

Figure 2.55 RIIC Bus Interface Input/Output Timing

2.3.7.10 RSPI

Table 2.36 RSPI Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF
High-drive output is selected by the driving ability control register.

Item				Symbol	Min.*1	Max.*1	Unit*1	Test Conditions*2
RSPI	RSPCK clock cycle	Master		t_{SPcyc}	2	4096	t_{PAcyc}	Figure 2.56
		Slave			8	—		
	RSPCK clock high pulse width	Master		t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2$	—		
	RSPCK clock low pulse width	Master		t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2$	—		
	RSPCK clock rise/ fall time	Output		t_{SPCKr}, t_{SPCKf}	—	5	ns	
		Input			—	1	µs	
	Data input setup time	Master		t_{SU}	6	—	ns	Figure 2.57 to Figure 2.62
		Slave			$8.3 - t_{PAcyc}$	—		
	Data input hold time	Master	PCLKA division ratio set to 1/2	t_{HF}	0	—	ns	
			PCLKA division ratio set to a value other than 1/2	t_H	t_{PAcyc}	—		
		Slave			$8.3 + 2 \times t_{PAcyc}$	—		
	SSL setup time	Master		t_{LEAD}	1	8	t_{SPcyc}	
		Slave			4	—	t_{PAcyc}	
	SSL hold time	Master		t_{LAG}	1	8	t_{SPcyc}	
		Slave			4	—	t_{PAcyc}	
	Data output delay time	Master		t_{OD}	—	6.3	ns	
		Slave			—	$3 \times t_{PAcyc} + 20$		
	Data output hold time	Master		t_{OH}	0	—	ns	
		Slave			0	—		
	Successive transmission delay time	Master		t_{TD}	$t_{SPcyc} + 2 \times t_{PAcyc}$	$8 \times t_{SPcyc} + 2 \times t_{PAcyc}$	ns	
		Slave			$4 \times t_{PAcyc}$	—		
	MOSI and MISO rise/fall time	Output		t_{Dr}, t_{Df}	—	5	ns	
		Input			—	1	µs	
	SSL rise/fall time	Output		t_{SSLr}, t_{SSLf}	—	5	ns	
		Input			—	1	µs	
	Slave access time			t_{SA}	—	4	t_{PAcyc}	Figure 2.61, Figure 2.62
	Slave output release time			t_{REL}	—	3	t_{PAcyc}	

Note 1. t_{PAcyc}: PCLKA cycle
Note 2. We recommend that pins suffixed with the same letter such as -A and -B, indicating grouping of the pins, should be used as a set. The AC characteristics of the RSPI are measured using the pins from the same group.

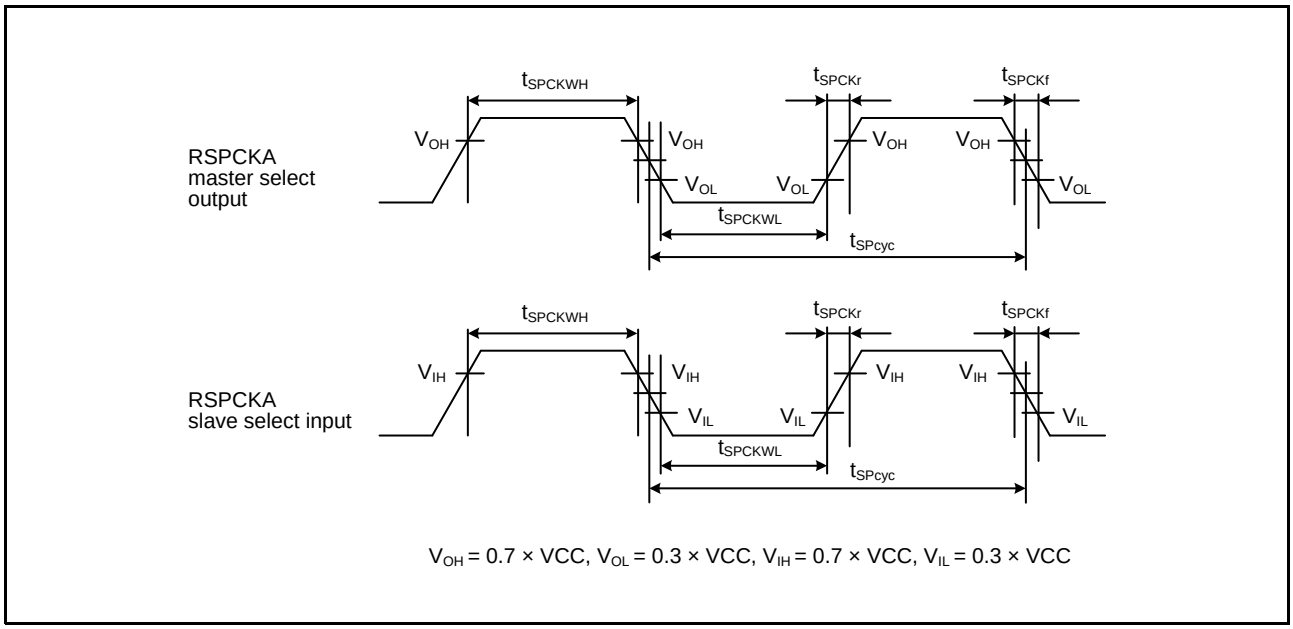


Figure 2.56 RSPI Clock Timing

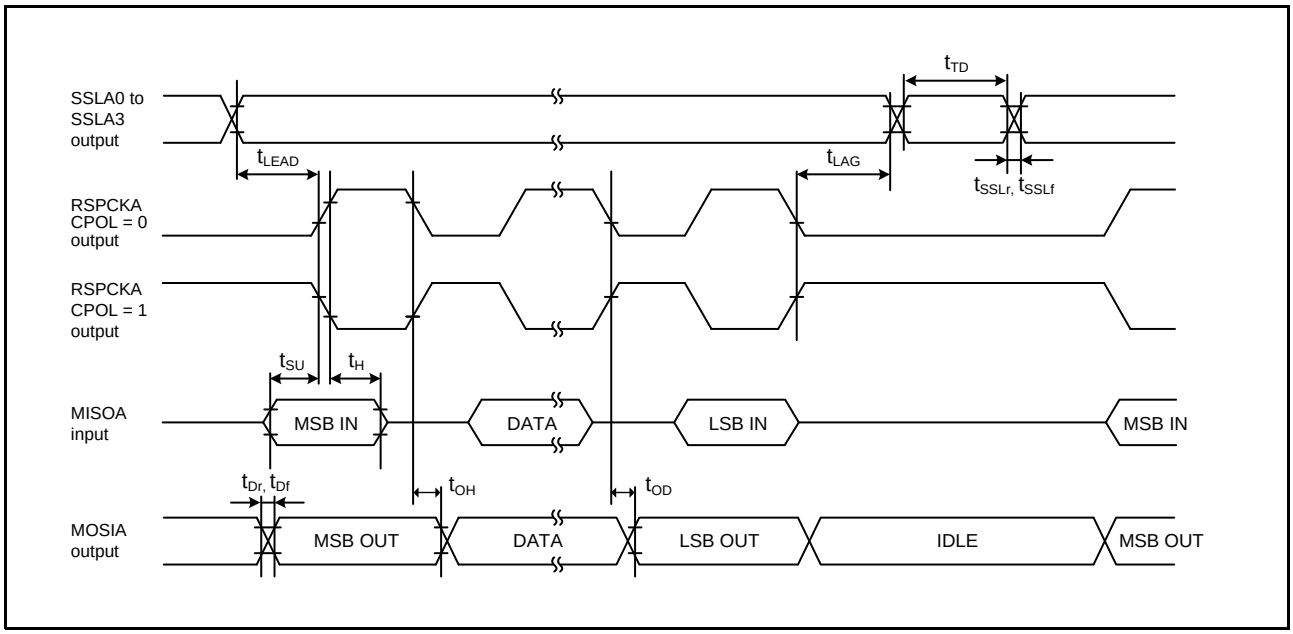


Figure 2.57 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKA Division Ratio Set to a Value Other Than 1/2)

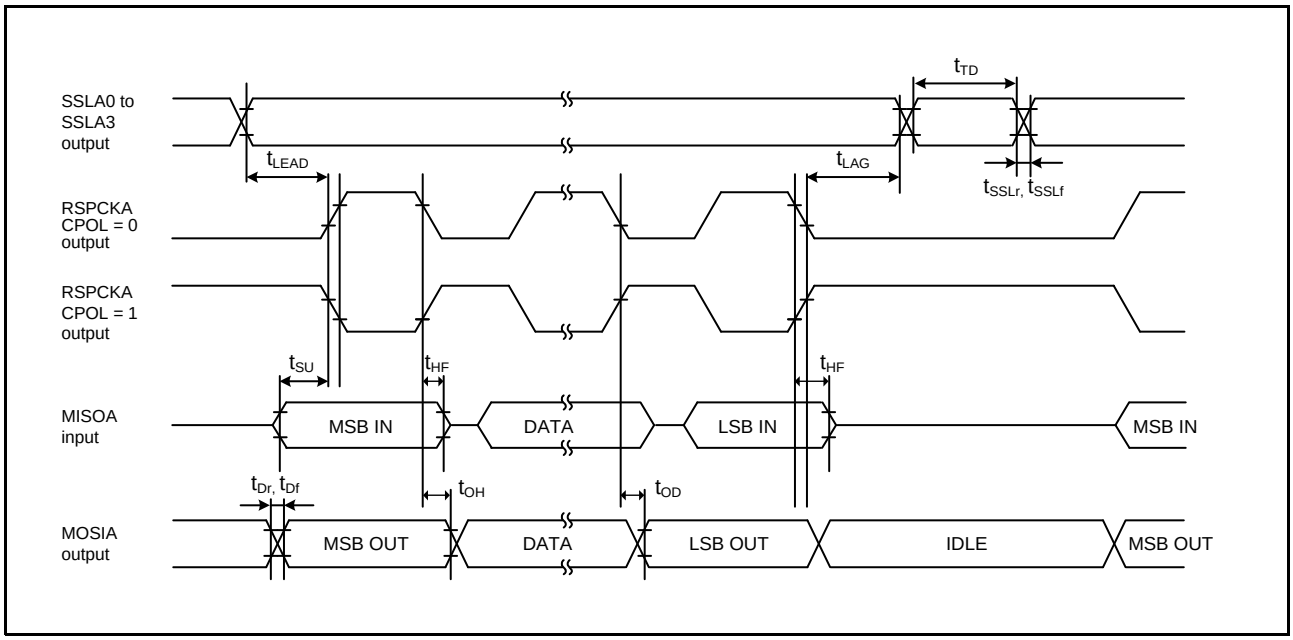


Figure 2.58 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKA Division Ratio Set to 1/2)

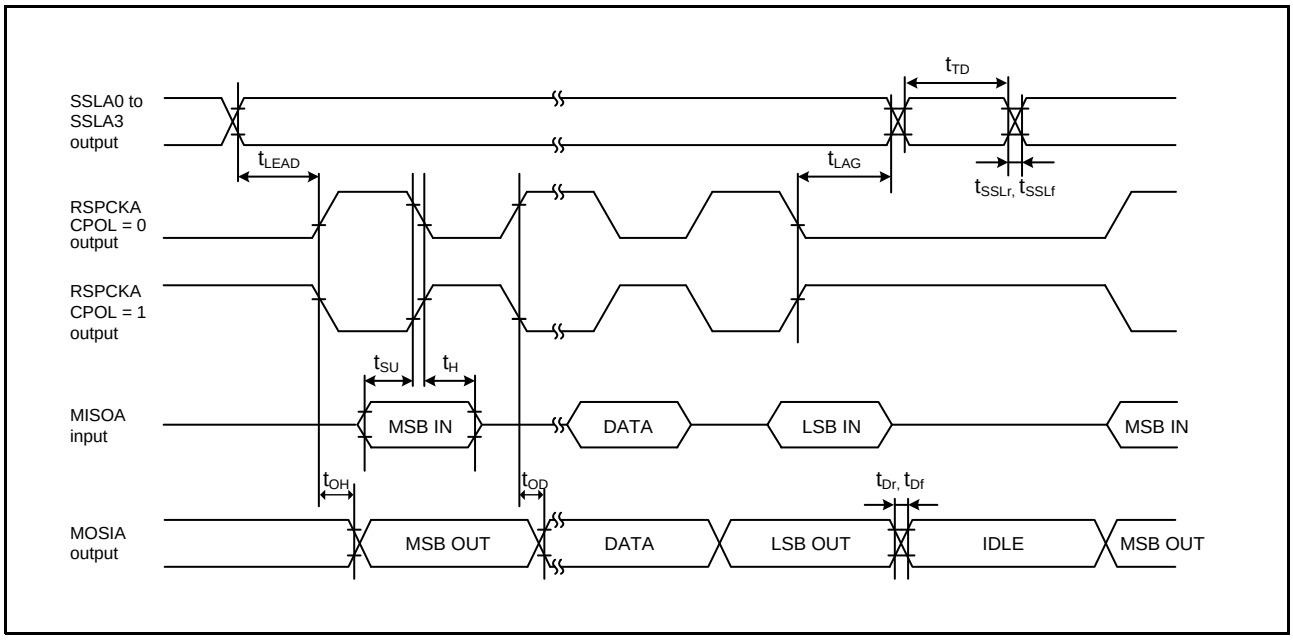


Figure 2.59 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKA Division Ratio Set to a Value Other Than 1/2)

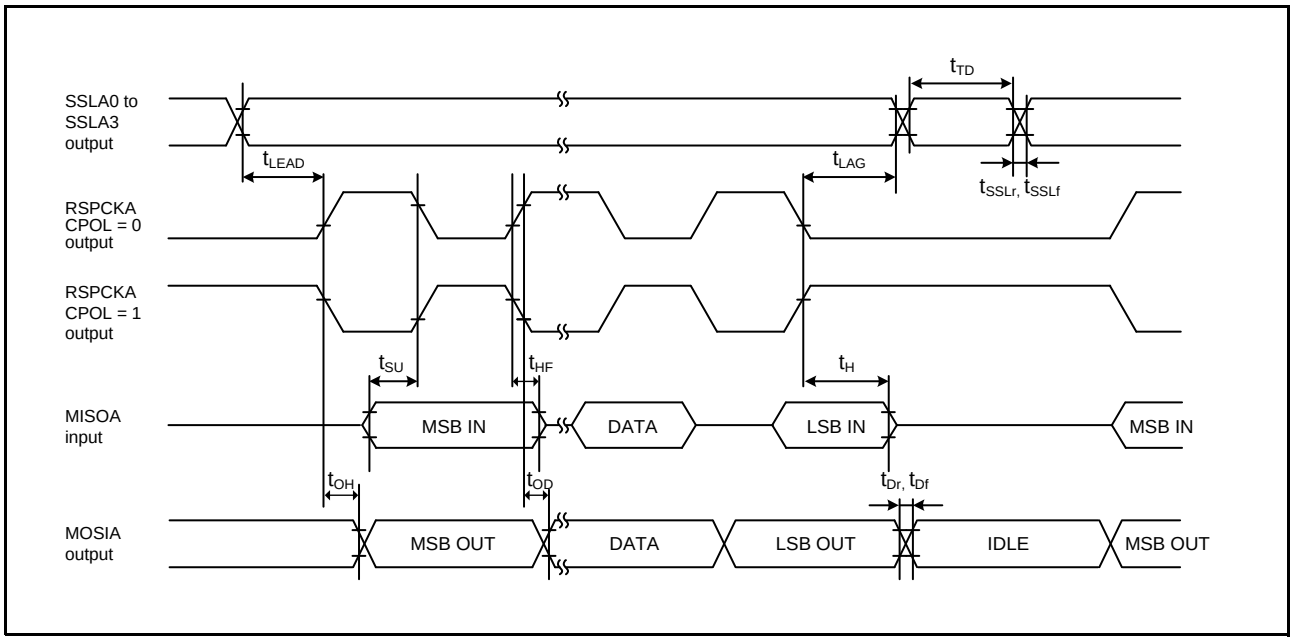


Figure 2.60 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKA Division Ratio Set to 1/2)

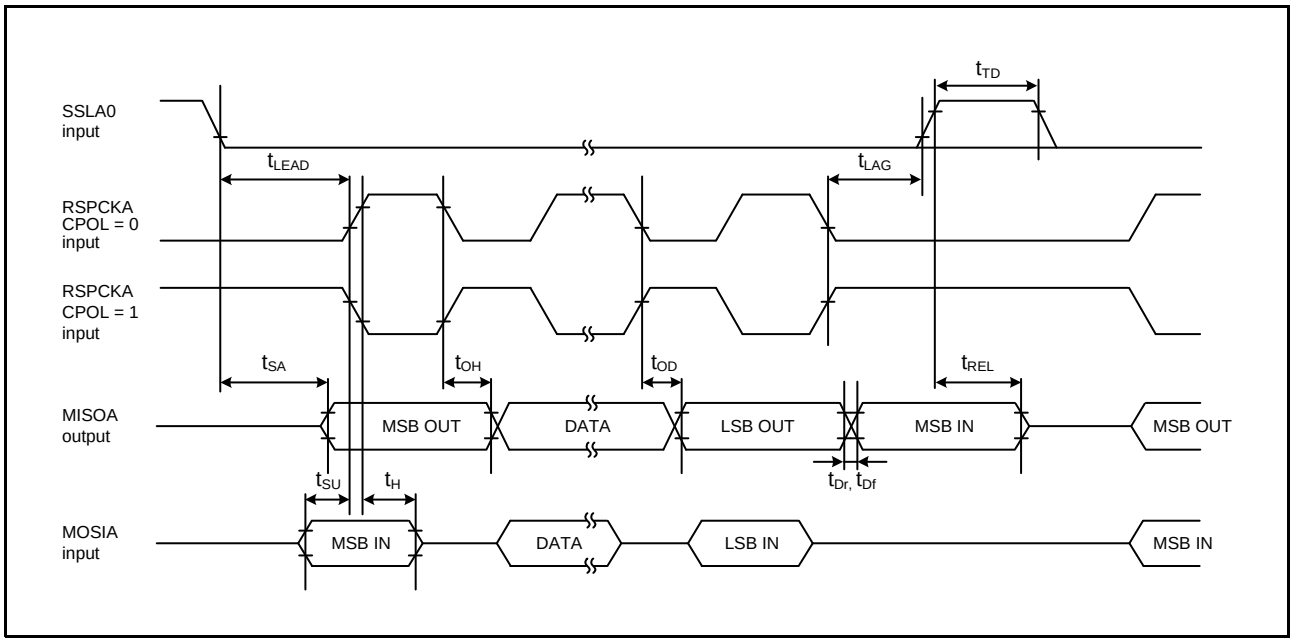


Figure 2.61 RSPI Timing (Slave, CPHA = 0)

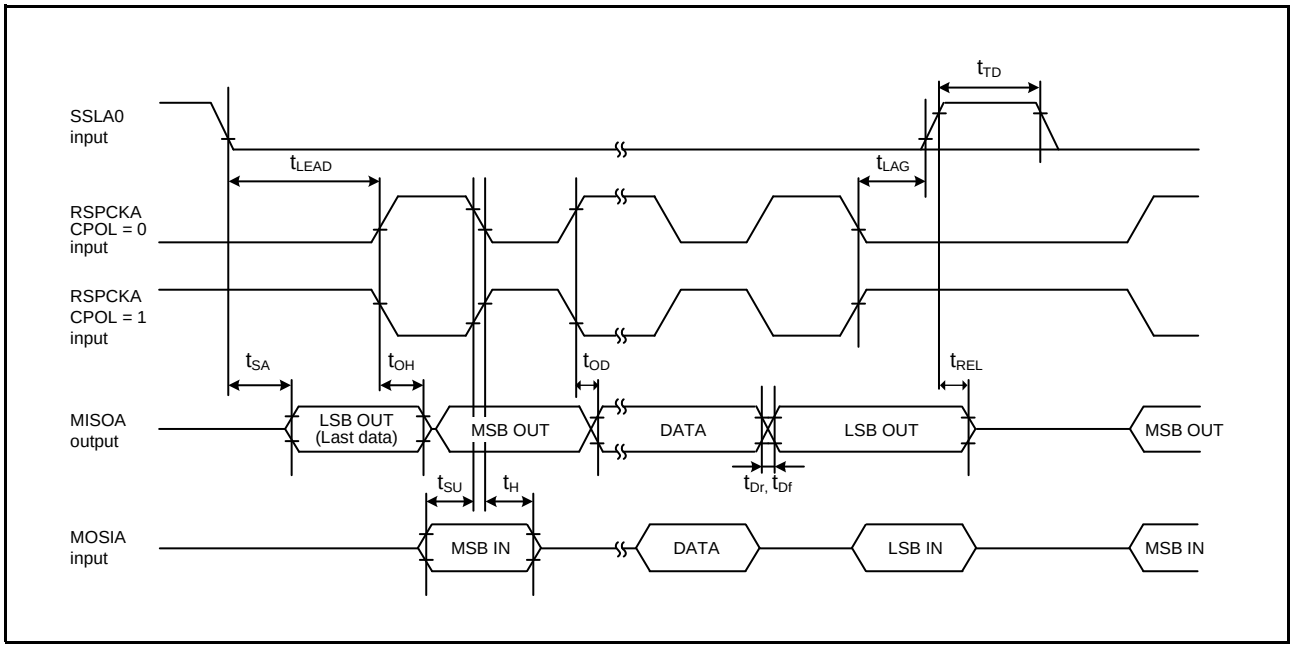


Figure 2.62 RSPI Timing (Slave, CPHA = 1)

2.3.7.11 QSPI

Table 2.37 QSPI Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF
High-drive output is selected by the driving ability control register.

Item		Symbol	Min.	Max.	Unit*1	Test Conditions*2
QSPI	QSPCLK clock cycle	t_{QScyc}	2	4080	t_{PBcyc}	Figure 2.63
	Data input setup time	t_{Su}	6.5	—	ns	Figure 2.64, Figure 2.65
	Data input hold time	t_{IH}	5	—	ns	
	SS setup time	t_{LEAD}	1.5	8.5	t_{QScyc}	
	SS hold time	t_{LAG}	1	8	t_{QScyc}	
	Data output delay time	t_{OD}	—	10.0	ns	
	Data output hold time	t_{OH}	–5	—	ns	
	Successive transmission delay time	t_{TD}	1	8	t_{QScyc}	

Note 1. t_{PBcyc}: PCLKB cycle
Note 2. We recommend that pins suffixed with the same letter such as -A and -B, indicating grouping of the pins, should be used as a set. The AC characteristics of the QSPI are measured using the pins from the same group.

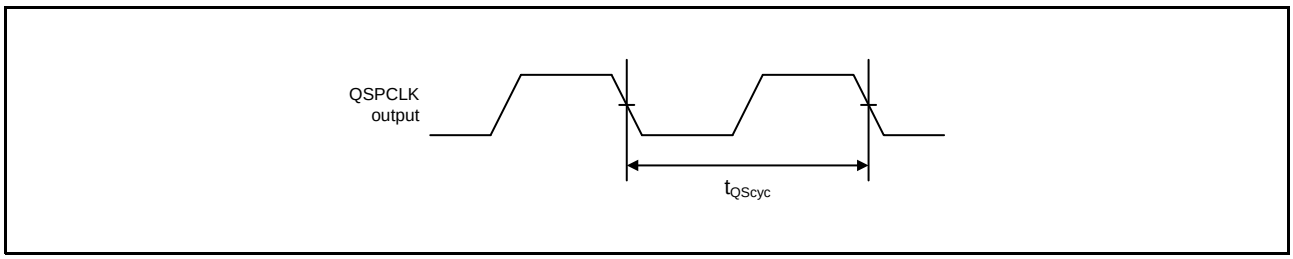


Figure 2.63 QSPI Clock Timing

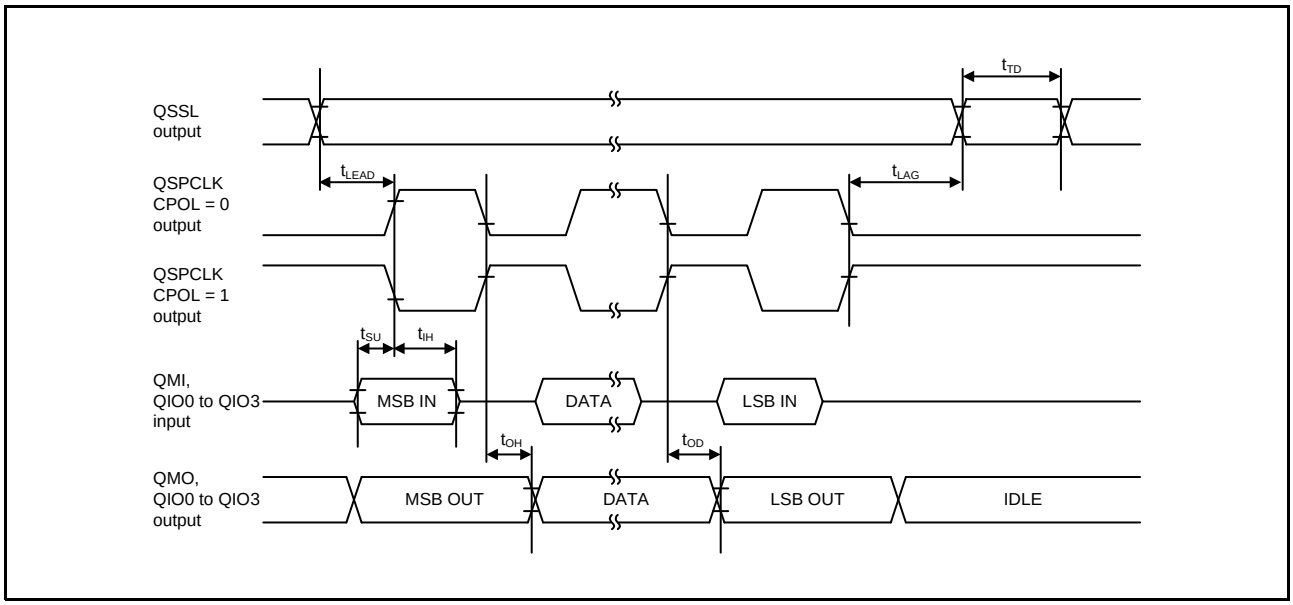


Figure 2.64 Transmit/Receive Timing (CPHA = 0)

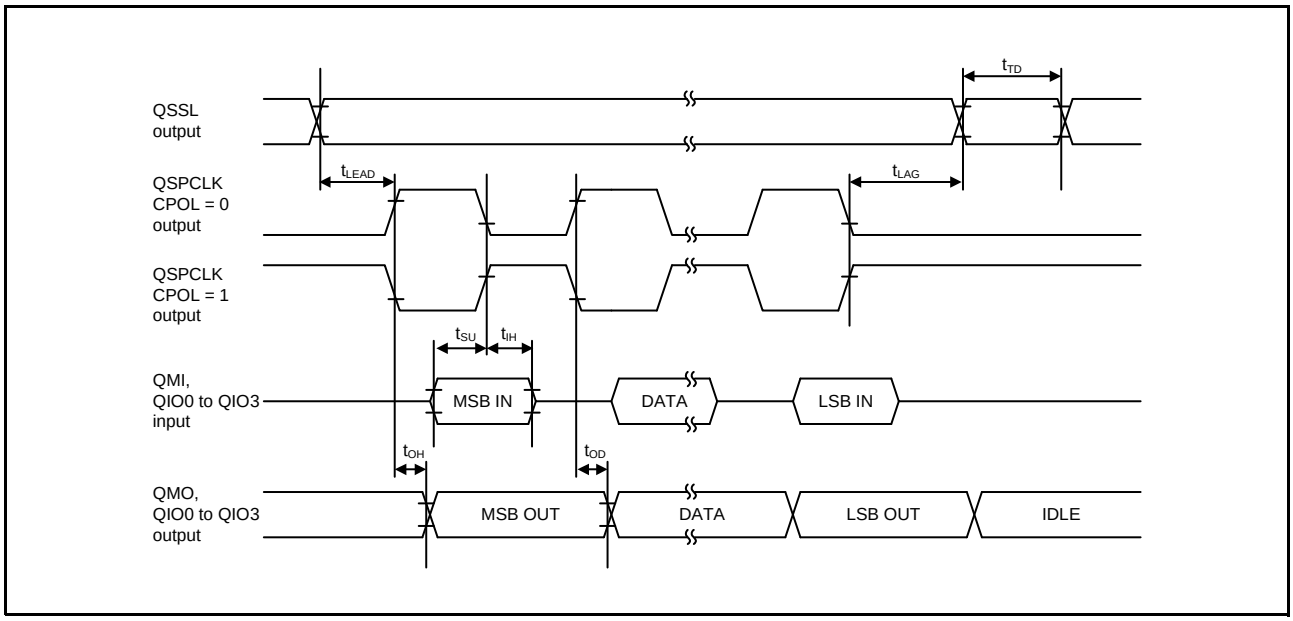


Figure 2.65 Transmit/Receive Timing (CPHA = 1)

2.3.7.12 SSI

Table 2.38 Serial Sound Interface Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF
High-drive output is selected by the driving ability control register.

Item		Symbol	Min.	Max.	Unit	Test Conditions
SSI	AUDIO_MCLK input frequency	t_{AUDIO}	—	50	MHz	
	Output clock cycle	t_O	150	64000	ns	Figure 2.66
	Input clock cycle	t_I	150	64000	ns	
	Clock high pulse width	t_{HC}	60	—	ns	
	Clock low pulse width	t_{LC}	60	—	ns	
	Clock rising time	t_{RC}	—	25	ns	
	Data delay time	t_{DTR}	–5	25	ns	Figure 2.67, Figure 2.68
	Setup time	t_{SR}	25	—	ns	
	Hold time	t_{HTR}	25	—	ns	
	WS change edge SSIDATA output delay	t_{DTRW}	—	25	ns	Figure 2.69

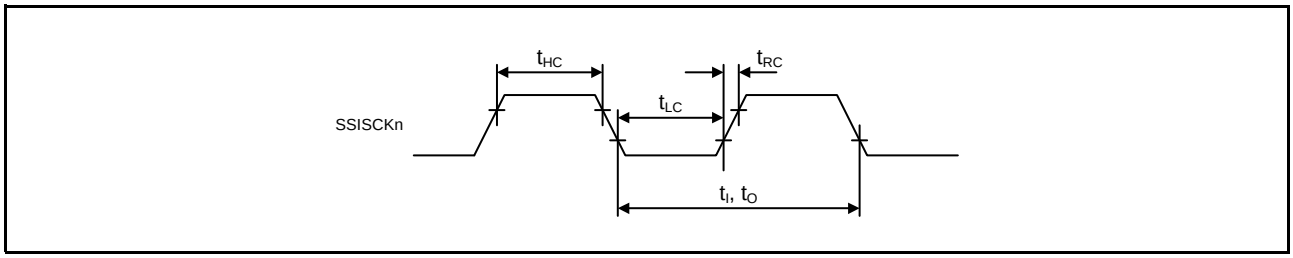


Figure 2.66 Clock Input/Output Timing

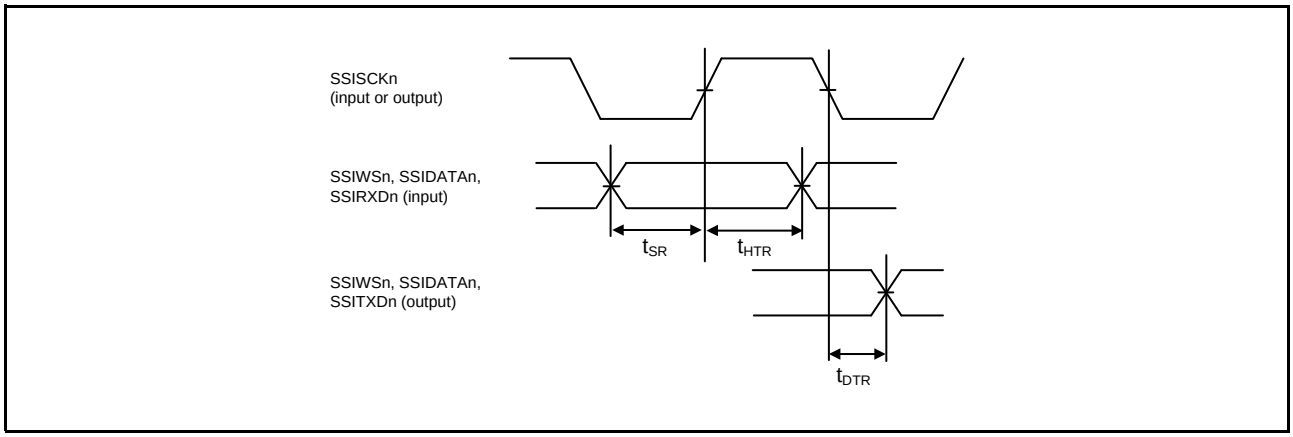


Figure 2.67 Transmit/Receive Timing (SSISCKn Rising Synchronous)

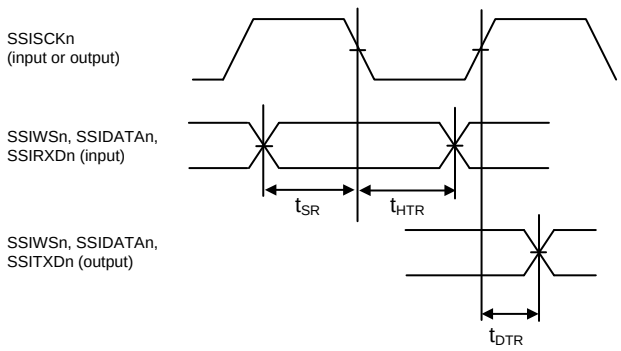
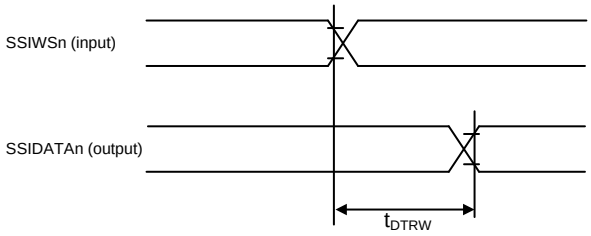


Figure 2.68 Transmit/Receive Timing (SSISCKn Falling Synchronous)



MSB bit output timing in slave transmission from SSIWSn with the settings of DEL = 1, SDTA = 0, or DEL = 1, SDTA = 1, SWL[2:0] = DWL[2:0]

Figure 2.69 SSIDATA Output Delay from SSIWSn Change Edge

2.3.7.13 MMC

Table 2.39 MMC Host Interface Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF
High-drive output is selected by the driving ability control register.

Item		Symbol	Min.*1	Max.	Unit	Test Conditions*2
MMCIF	MMC_CLK clock cycle	t_{MMCPP}	2 × t_{PBcyc}	—	ns	Figure 2.70
	MMC_CLK clock high level width	t_{MMCWH}	6.5	—	ns	
	MMC_CLK clock low level width	t_{MMCWL}	6.5	—	ns	
	MMC_CLK clock rising time	t_{MMCLH}	—	5	ns	
	MMC_CLK clock falling time	t_{MMCHL}	—	5	ns	
	MMC_CMD, MMC_D7 to MMC_D0 output data delay (data transfer mode)	$t_{MMCODLY}$	–6.5	6.5	ns	
	MMC_CMD, MMC_D7 to MMC_D0 input data setup	t_{MMCISU}	8	—	ns	
	MMC_CMD, MMC_D7 to MMC_D0 input data hold	t_{MMCIH}	2	—	ns	

Note 1. t_{PBcyc}: PCLKB cycle
Note 2. We recommend that pins suffixed with the same letter such as -A and -B, indicating grouping of the pins, should be used as a set. The AC characteristics of the MMC are measured using the pins from the same group.

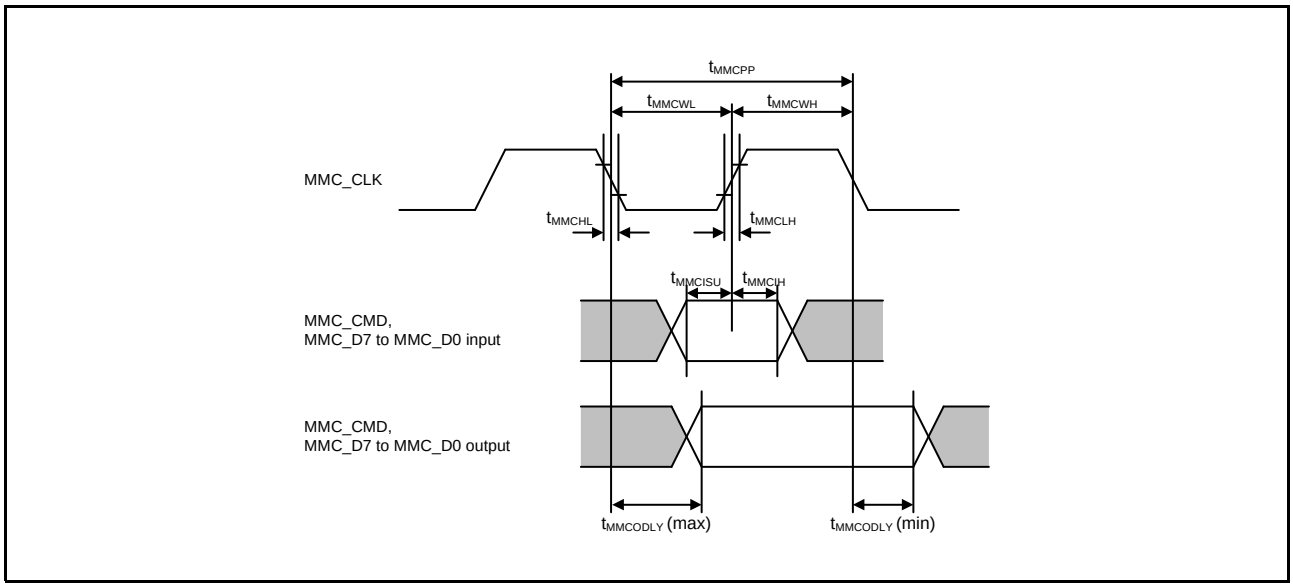


Figure 2.70 MMC Interface

2.3.7.14 SDHI

Table 2.40 SDHI Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item		Symbol	Min.	Max.	Unit	Test Conditions*1
SDHI	SDHI_CLK pin output cycle time	$t_{PP(SD)}$	2 × t_{PBcyc}*2	—	ns	Figure 2.71
	SDHI_CLK pin output high pulse width	$t_{WH(SD)}$	0.4 × $t_{PP(SD)}$	—	ns	
	SDHI_CLK pin output low pulse width	$t_{WL(SD)}$	0.4 × $t_{PP(SD)}$	—	ns	
	SDHI_CLK pin output rise time	$t_{TLH(SD)}$	—	5	ns	
	SDHI_CLK pin output fall time	$t_{THL(SD)}$	—	5	ns	
	Output data delay time (data transfer mode) for SDHI_CMD and SDHI_D0 to SDHI_D3 pins	$t_{ODLY(SD)}$	–6.5	4	ns	
	Input data setup time for SDHI_CMD and SDHI_D0 to SDHI_D3 pins	$t_{ISU(SD)}$	7	—	ns	
	Input data hold time for SDHI_CMD and SDHI_D0 to SDHI_D3 pins	$t_{IH(SD)}$	2	—	ns	

Note 1. When a letter “-A”, “-B”, etc. to indicate group membership is appended to the pin name, each pin is recommended to use in combination with the pins in the same group. All SDHI AC timings are measured in combination with the pins in the same group.
Note 2. t_{PBcyc}: PCLKB cycle

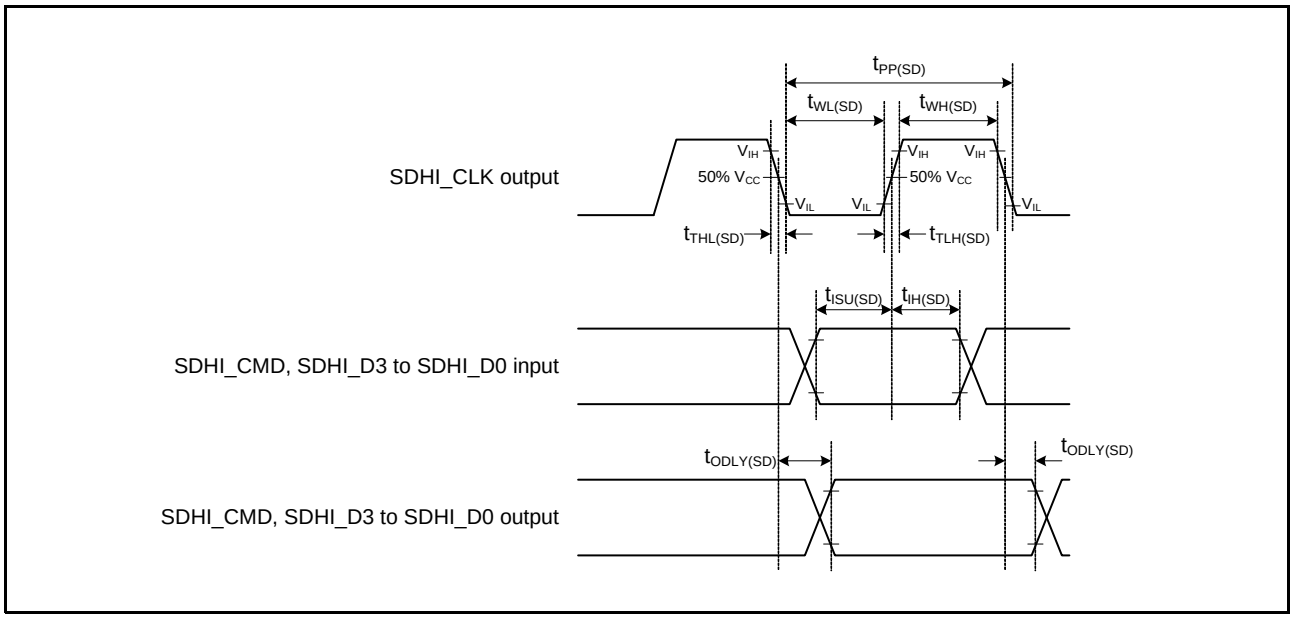


Figure 2.71 SD Host Interface Input/Output Signal Timing

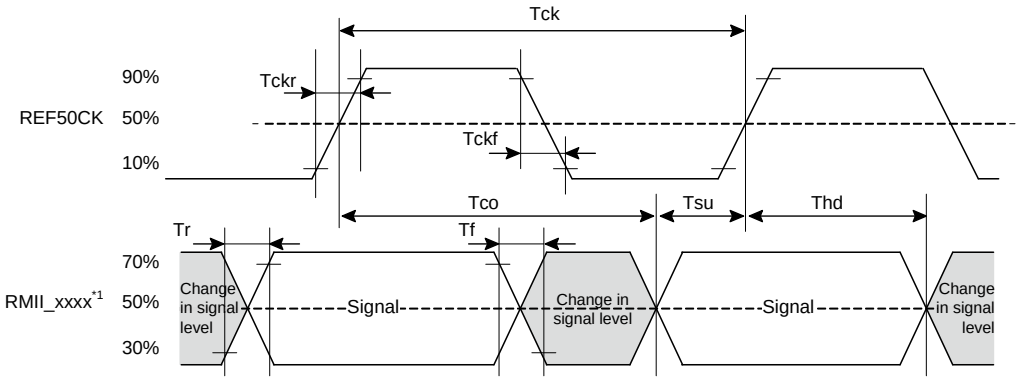
2.3.7.15 ETHERC

Table 2.41 ETHERC Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF
High-drive output is selected by the driving ability control register.

Item		Symbol	Min.	Max.	Unit	Test Conditions
ETHERC (RMII)	REF50CK cycle time	T_{ck}	20	—	ns	Figure 2.72 to Figure 2.74
	REF50CK frequency Typ. 50 MHz	—	—	50 + 100 ppm	MHz	
	REF50CK duty	—	35	65	%	
	REF50CK rise/fall time	$T_{ckr/ckf}$	0.5	3.5	ns	
	RMII_xxxx*1 output delay time	T_{co}	2.5	15.0	ns	
	RMII_xxxx*2 setup time	T_{su}	3	—	ns	
	RMII_xxxx*2 hold time	T_{hd}	1	—	ns	
	RMII_xxxx*1, *2 rise/fall time	T_r/T_f	0.5	5	ns	
	ET_WOL output delay time	t_{WOLd}	1	23.5	ns	Figure 2.76
ETHERC (MII)	ET_TX_CLK cycle time	t_{Tcyc}	40	—	ns	—
	ET_TX_EN output delay time	t_{TENd}	1	20	ns	Figure 2.77
	ET_ETXD0 to ET_ETXD3 output delay time	t_{MTDd}	1	20	ns	
	ET_CRS setup time	t_{CRSs}	10	—	ns	
	ET_CRS hold time	t_{CRSh}	10	—	ns	
	ET_COL setup time	t_{COLs}	10	—	ns	Figure 2.78
	ET_COL hold time	t_{COLh}	10	—	ns	
	ET_RX_CLK cycle time	t_{TRcyc}	40	—	ns	—
	ET_RX_DV setup time	t_{RDVs}	10	—	ns	Figure 2.79
	ET_RX_DV hold time	t_{RDVh}	10	—	ns	
	ET_ERXD0 to ET_ERXD3 setup time	t_{MRDs}	10	—	ns	
	ET_ERXD0 to ET_ERXD3 hold time	t_{MRDh}	10	—	ns	
	ET_RX_ER setup time	t_{RERs}	10	—	ns	Figure 2.80
	ET_RX_ER hold time	t_{RESh}	10	—	ns	
	ET_WOL output delay time	t_{WOLd}	1	23.5	ns	Figure 2.81

Note 1. RMII_TXD_EN, RMII_TXD1, RMII_TXD0
Note 2. RMII_CRS_DV, RMII_RXD1, RMII_RXD0, RMII_RX_ER



Note 1. RMII_TXD_EN, RMII_TXD1, RMII_TXD0, RMII_CRS_DV, RMII_RXD1, RMII_RXD0, RMII_RX_ER

Figure 2.72 Timing with the REF50CK and RMII Signals

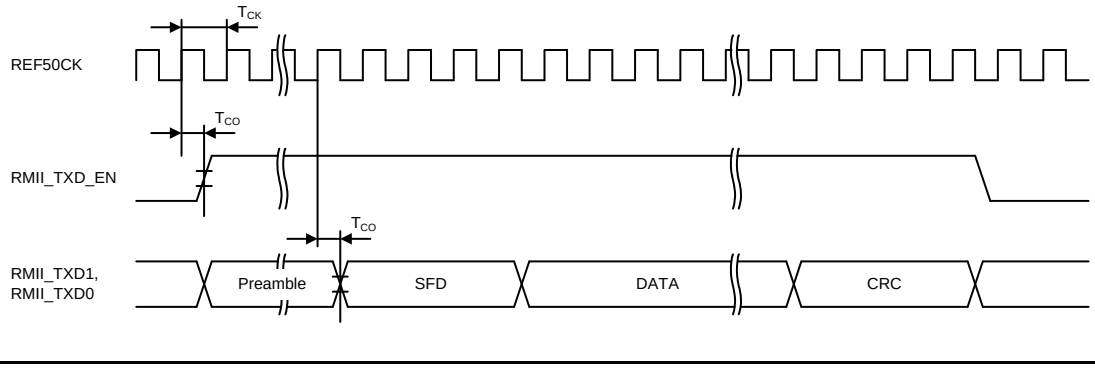


Figure 2.73 RMII Transmission Timing

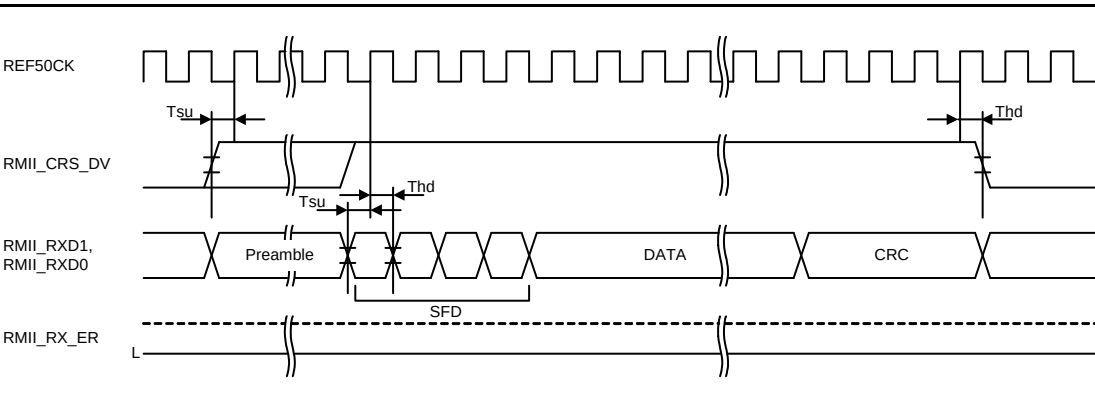


Figure 2.74 RMII Reception Timing (Normal Operation)

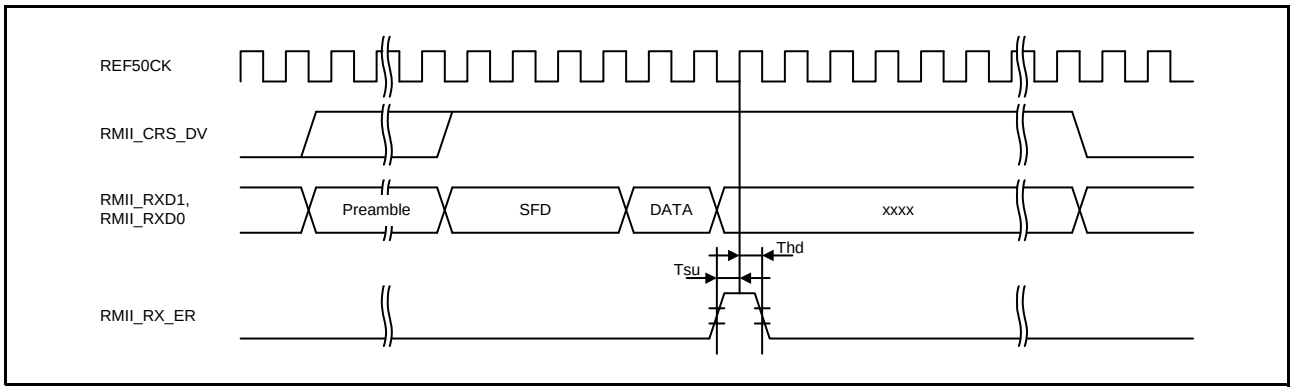


Figure 2.75 RMII Reception Timing (Error Occurrence)

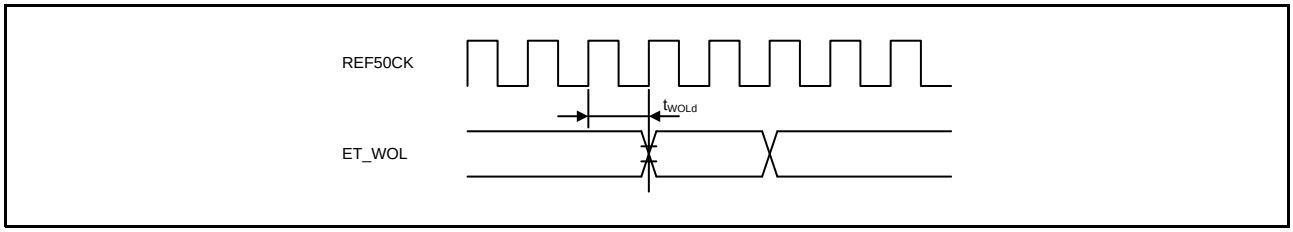


Figure 2.76 WOL Output Timing (RMII)

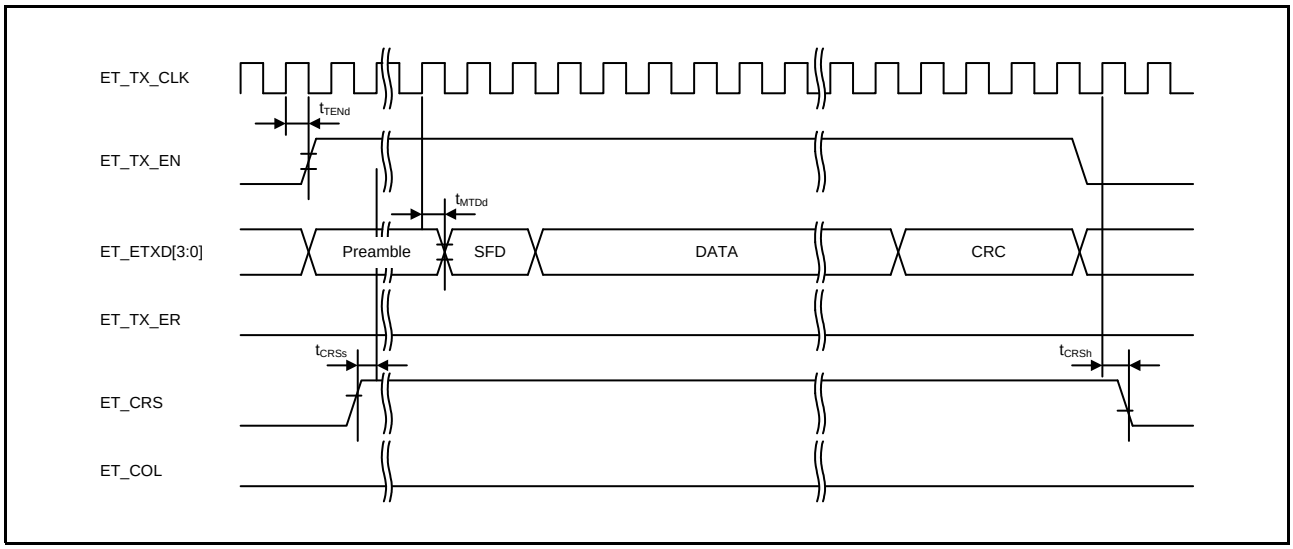


Figure 2.77 MII Transmission Timing (Normal Operation)

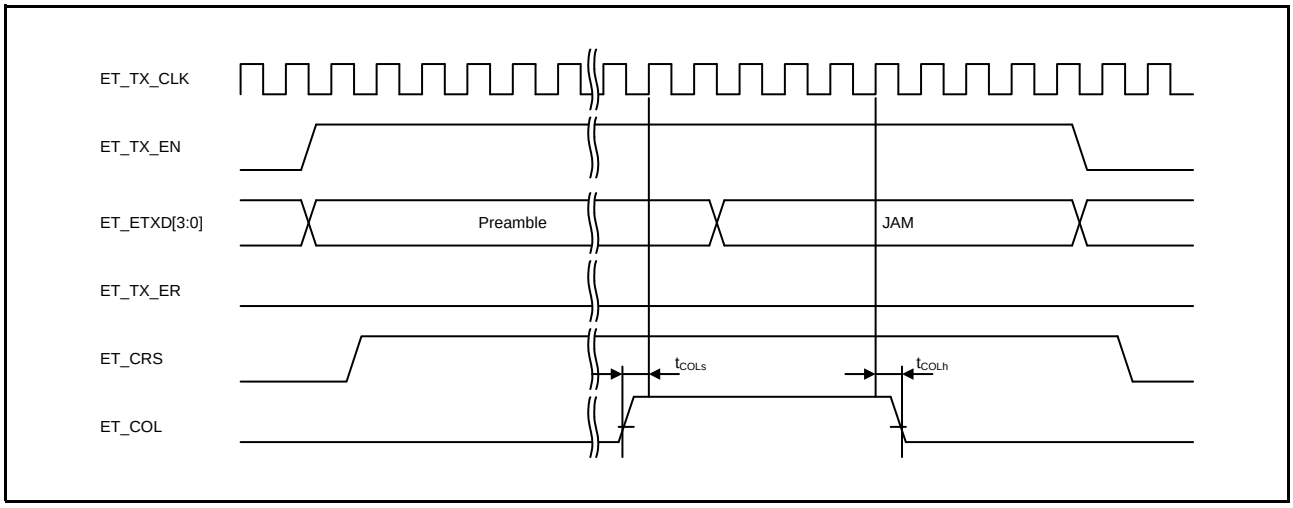


Figure 2.78 MII Transmission Timing (Conflict Occurrence)

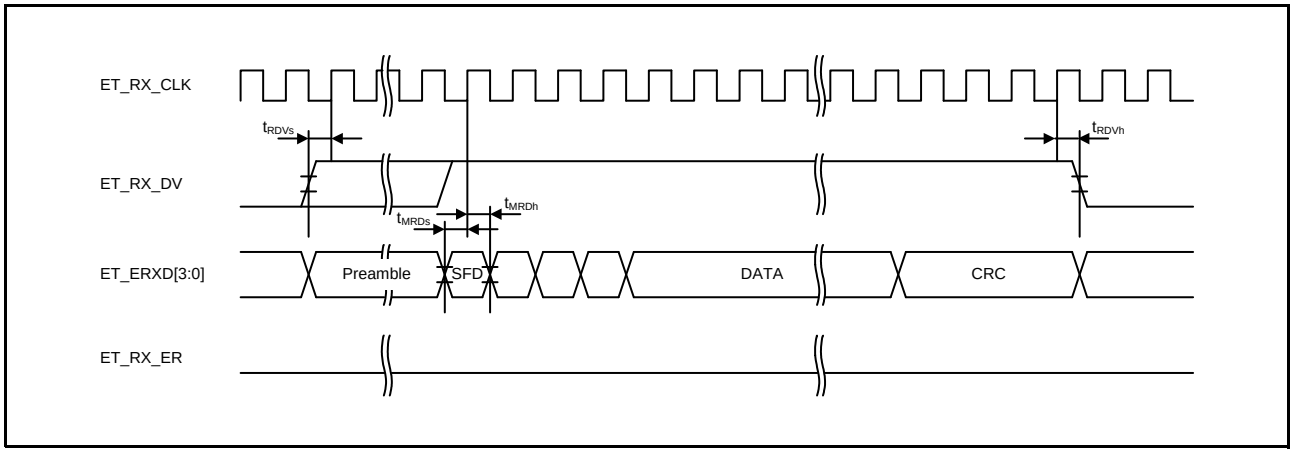


Figure 2.79 MII Reception Timing (Normal Operation)

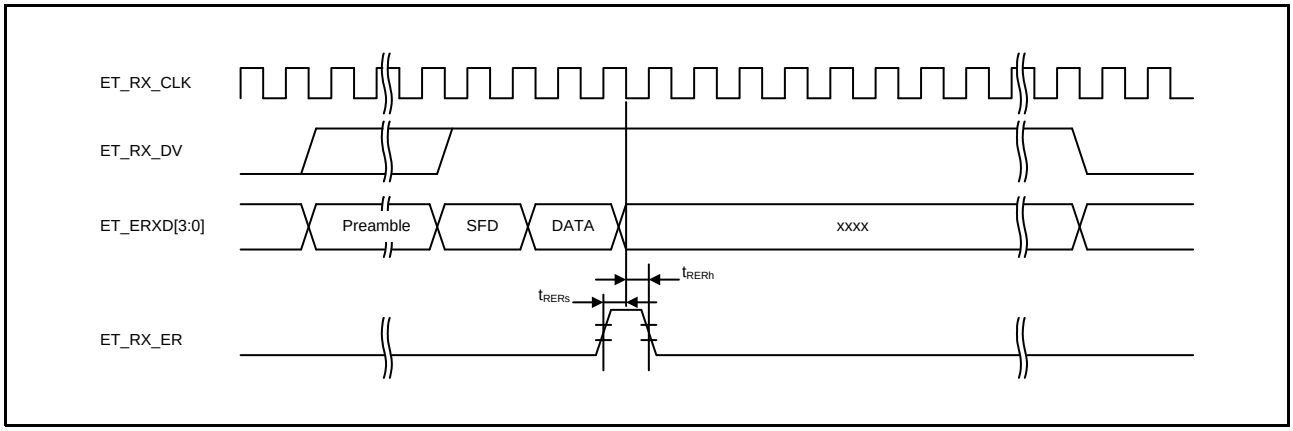


Figure 2.80 MII Reception Timing (Error Occurrence)

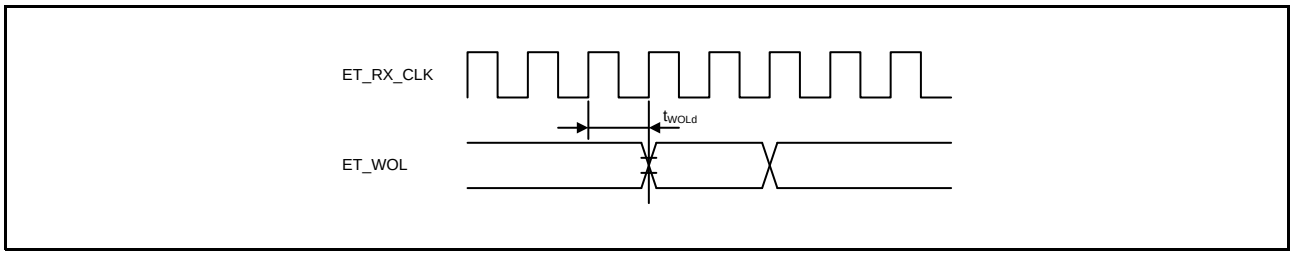


Figure 2.81 WOL Output Timing (MII)

2.3.7.16 PDC

Table 2.42 PDC Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF
High-drive output is selected by the driving ability control register.

Item		Symbol	Min.*1	Max.	Unit	Test Conditions
PDC	PIXCLK input cycle time	t_{PIXcyc}	37	—	ns	Figure 2.82
	PIXCLK input high pulse width	t_{PIXH}	10	—	ns	
	PIXCLK input low pulse width	t_{PIXL}	10	—	ns	
	PIXCLK rising time	t_{PIXr}	—	5	ns	
	PIXCLK falling time	t_{PIXf}	—	5	ns	
	PCKO output cycle time	t_{PCKcyc}	2 × t_{PBcyc}	—	ns	Figure 2.83
	PCKO output high pulse width	t_{PCKH}	(t_{PCKcyc} – t_{PCKr} – t_{PCKf})/2 – 3	—	ns	
	PCKO output low pulse width	t_{PCKL}	(t_{PCKcyc} – t_{PCKr} – t_{PCKf})/2 – 3	—	ns	
	PCKO rising time	t_{PCKr}	—	5	ns	
	PCKO falling time	t_{PCKf}	—	5	ns	
	VSYNV/HSYNC input setup time	t_{SYNCS}	10	—	ns	Figure 2.84
	VSYNV/HSYNC input hold time	t_{SYNCH}	5	—	ns	
	PIXD input setup time	t_{PIXDS}	10	—	ns	
	PIXD input hold time	t_{PIXDH}	5	—	ns	

Note 1. t_{PBcyc}: PCLKB cycle

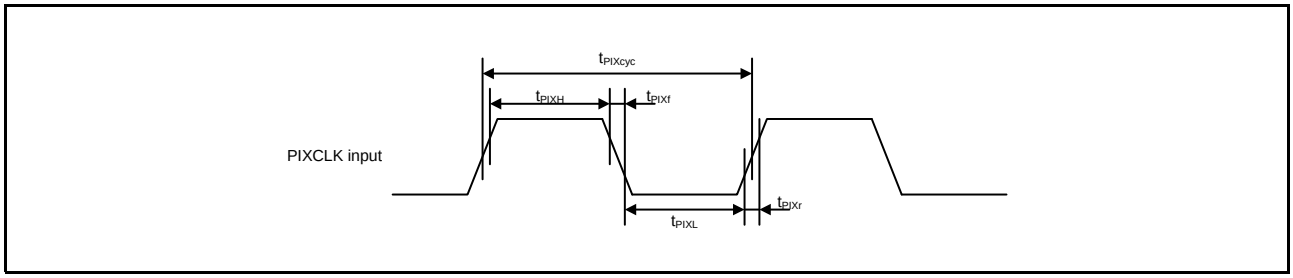


Figure 2.82 PDC Input Clock Timing

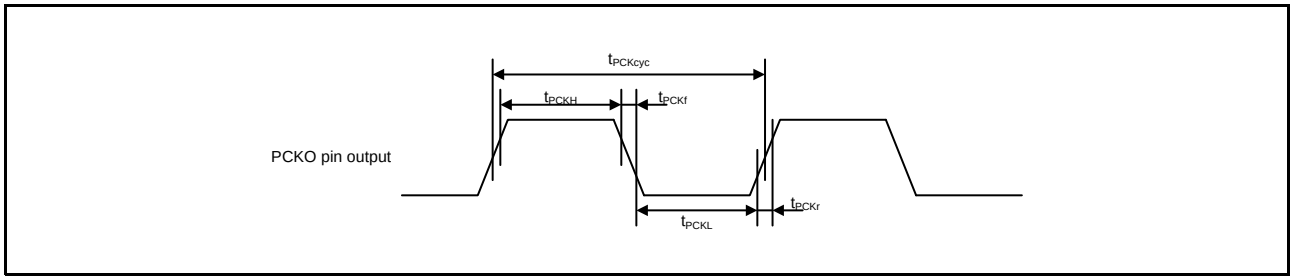


Figure 2.83 PDC Output Clock Timing

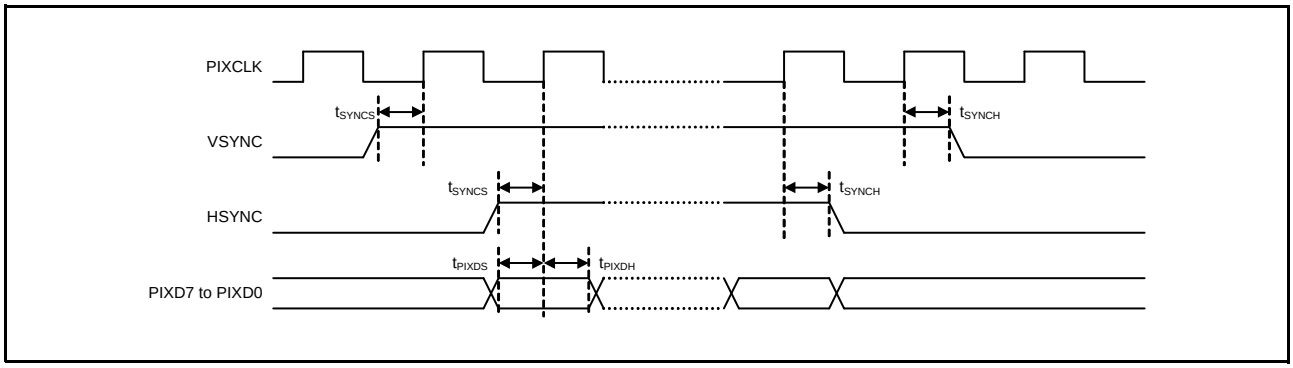


Figure 2.84 PDC AC Timing

2.3.7.17 A/D Converter Trigger

Table 2.43 A/D Converter Trigger Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF
High-drive output is selected by the driving ability control register.

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
A/D converter	A/D converter trigger input pulse width	t_{TRGW}	1.5	—	t_{PBcyc}	Figure 2.85

Note 1. t_{PBcyc}: PCLKB cycle

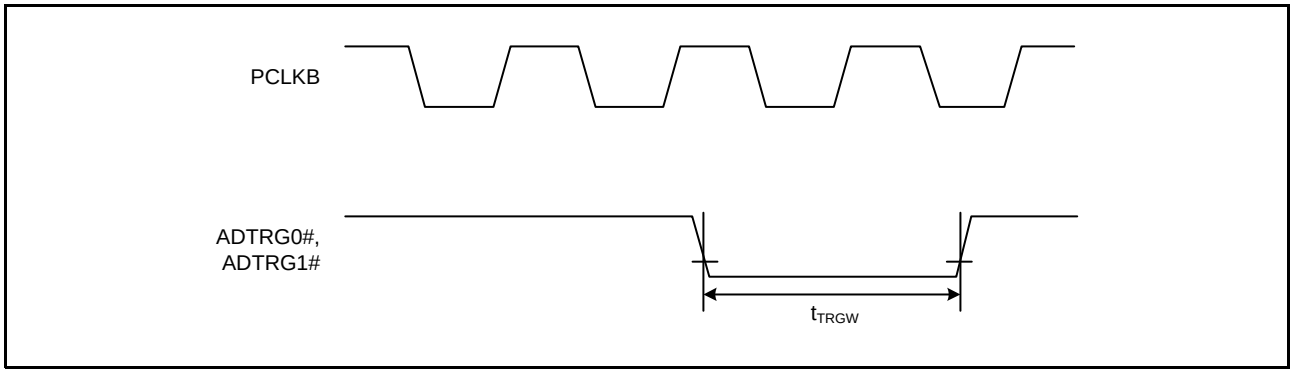


Figure 2.85 A/D Converter Trigger Input Timing

2.3.7.18 CAC

Table 2.44 CAC Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF
High-drive output is selected by the driving ability control register.

Item*1, *2			Symbol	Min.*1	Max.	Unit*1	Test Conditions
CAC	CACREF input pulse width	$t_{PBcyc} \leq t_{cac}$	t_{CACREF}	4.5 t_{cac} + 3 t_{PBcyc}	—	ns	
		$t_{PBcyc} > t_{cac}$		5 t_{cac} + 6.5 t_{PBcyc}	—		

Note 1. t_{PBcyc}: PCLKB cycle
Note 2. t_{CAC}: CAC count clock source cycle

2.4 USB Characteristics

Table 2.45 On-Chip USB Low Speed (Host Only) Characteristics (DP and DM Pin Characteristics)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 3.0 to 3.6 V, 3.0 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
USBA_RREF = 2.2 kΩ ±1%, USBMCLK = 20/24 MHz, UCLK = 48 MHz,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input characteristics	Input high level voltage	V_{IH}	2.0	—	—	V	
	Input low level voltage	V_{IL}	—	—	0.8	V	
	Differential input sensitivity	V_{DI}	0.2	—	—	V	| DP – DM |
	Differential common mode range	V_{CM}	0.8	—	2.5	V	
Output characteristics	Output high level voltage	V_{OH}	2.8	—	3.6	V	I_{OH} = –200 µA
	Output low level voltage	V_{OL}	0.0	—	0.3	V	I_{OL} = 2 mA
	Cross-over voltage	V_{CRS}	1.3	—	2.0	V	Figure 2.86
	Rise time	t_{LR}	75	—	300	ns	
	Fall time	t_{LF}	75	—	300	ns	
	Rise/fall time ratio	t_{LR} / t_{LF}	80	—	125	%	t_{LR}/ t_{LF}
Pull-up and pull-down characteristics	DP/DM pull-down resistance (when the host controller function is selected)	R_{pd}	14.25	—	24.80	kΩ	

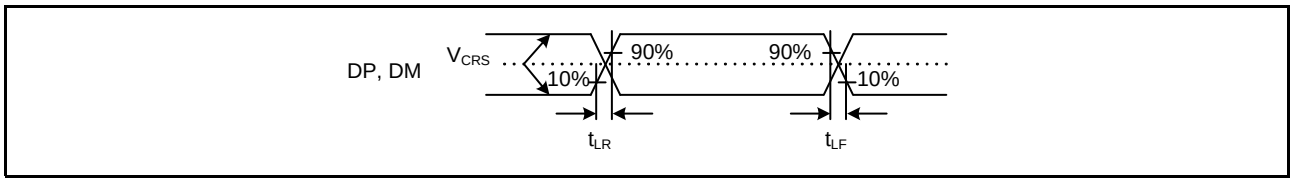


Figure 2.86 DP and DM Output Timing (Low Speed)

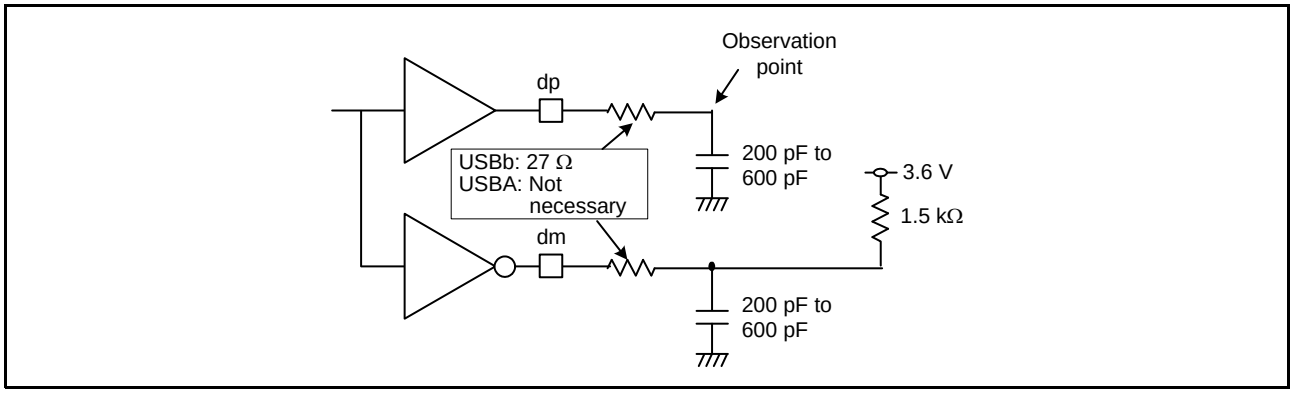


Figure 2.87 Test Circuit (Low Speed)

Table 2.46 On-Chip USB Full-Speed Characteristics (DP and DM Pin Characteristics)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 3.0 to 3.6 V, 3.0 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
USBA_RREF = 2.2 kΩ ±1%, USBMCLK = 20/24 MHz, UCLK = 48 MHz,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input characteristics	Input high level voltage	V_{IH}	2.0	—	—	V	
	Input low level voltage	V_{IL}	—	—	0.8	V	
	Differential input sensitivity	V_{DI}	0.2	—	—	V	| DP – DM |
	Differential common mode range	V_{CM}	0.8	—	2.5	V	
Output characteristics	Output high level voltage	V_{OH}	2.8	—	3.6	V	I_{OH} = –200 µA
	Output low level voltage	V_{OL}	0.0	—	0.3	V	I_{OL} = 2 mA
	Cross-over voltage	V_{CRS}	1.3	—	2.0	V	Figure 2.88
	Rise time	t_{FR}	4	—	20	ns	
	Fall time	t_{FF}	4	—	20	ns	
	Rise/fall time ratio	t_{FR} / t_{FF}	90	—	111.11	%	t_{FR}/ t_{FF}
	Output resistance	Z_{DRV}	28	—	44	Ω	USBb: Rs = 27 Ω included
			40.5	—	49.5	Ω	USBA: Rs not necessary (PHYSET.REPSEL[1:0] = 01b and PHYSET.HSEB = 0)
Pull-up and pull-down characteristics	DP pull-up resistance (when the function controller function is selected)	R_{pu}	0.900	—	1.575	kΩ	Idle state
			1.425	—	3.090	kΩ	At transmission and reception
	DP/DM pull-down resistance (when the host controller function is selected)	R_{pd}	14.25	—	24.80	kΩ	

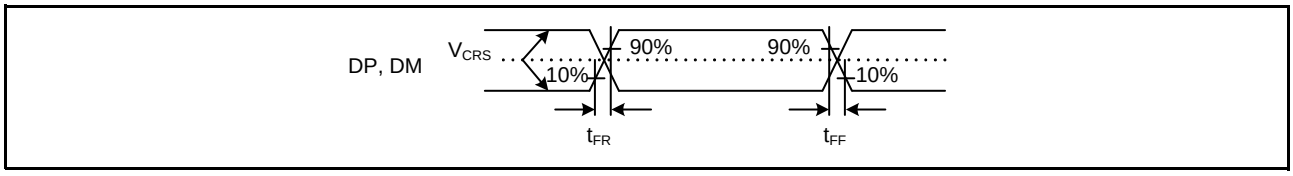


Figure 2.88 DP and DM Output Timing (Full-Speed)

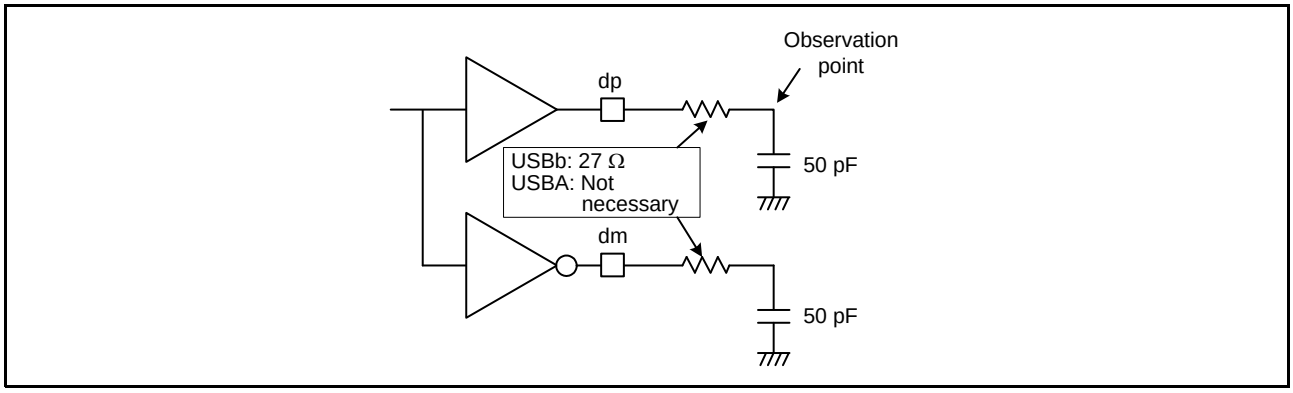


Figure 2.89 Test Circuit (Full-Speed)

Table 2.47 On-Chip USB High-Speed Characteristics (DP and DM Pin Characteristics)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 3.0 to 3.6 V, 3.0 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
USBA_RREF = 2.2 kΩ ±1%, USBMCLK = 20/24 MHz, PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input characteristics	Squelch detect sensitivity (Differential voltage)	V_{HSSQ}	100	—	150	mV	Figure 2.90
	Disconnect detect sensitivity	V_{HSDSC}	525	—	625	mV	Figure 2.91
	Common mode voltage	V_{HSCM}	–50	—	500	mV	
Output characteristics	Idle state	V_{HSOI}	–10	—	10	mV	
	Output high level voltage	V_{HSOH}	360	—	440	mV	
	Output low level voltage	V_{HSOL}	–10	—	10	mV	
	Chirp J output voltage (difference)	V_{CHIRPJ}	700	—	1100	mV	
	Chirp K output voltage (difference)	V_{CHIRPK}	–900	—	–500	mV	
AC characteristics	Rise time	t_{HSR}	500	—	—	ps	Figure 2.92
	Fall time	t_{HSF}	500	—	—	ps	
	Output resistance	Z_{HSDRV}	40.5	—	49.5	Ω	

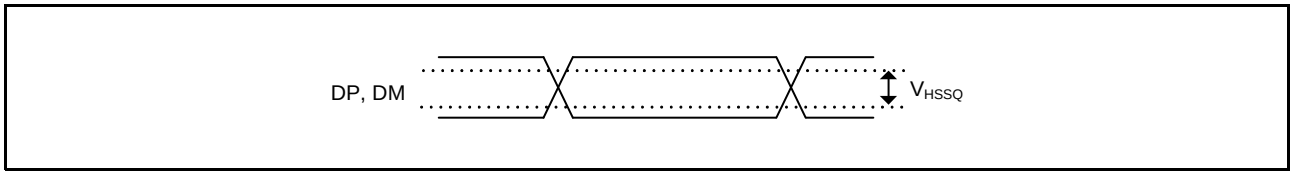


Figure 2.90 DP and DM Squelch detect sensitivity (High-Speed)

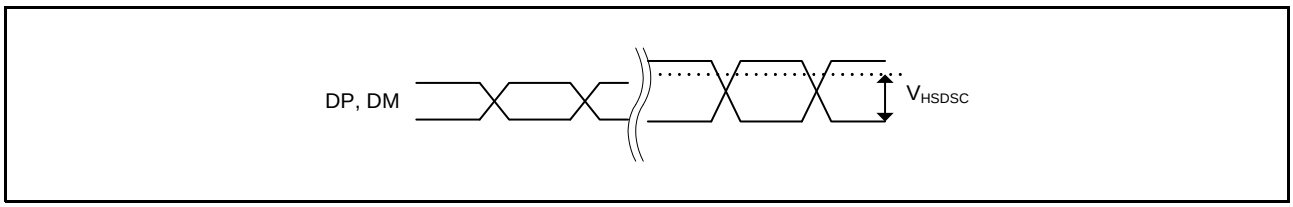


Figure 2.91 DP and DM Disconnect detect sensitivity (High-Speed)

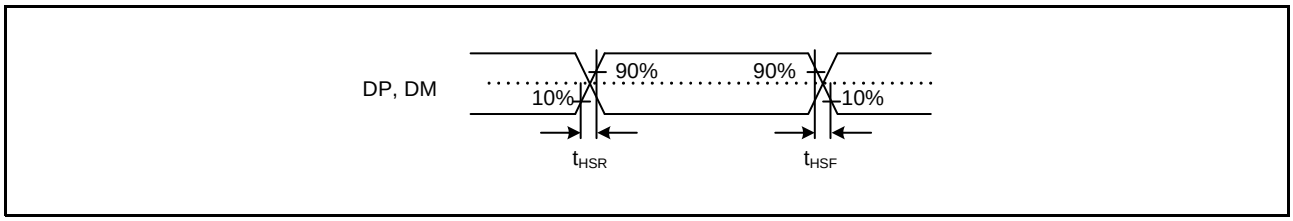


Figure 2.92 DP and DM Output Timing (High-Speed)

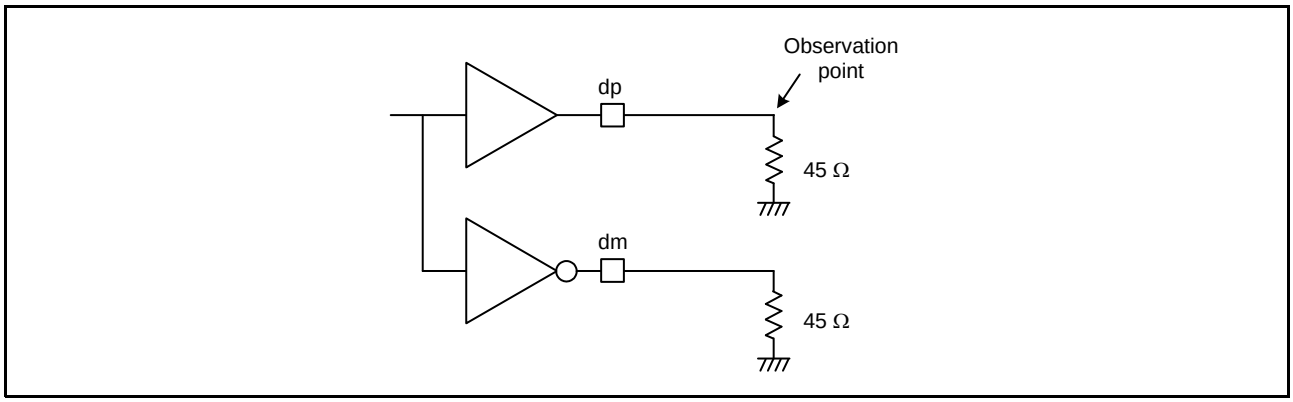


Figure 2.93 Test Circuit (High-Speed)

Table 2.48 Battery Charge Characteristics (USBA only)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA =
AVSS_USBA = 0 V, USBA_RREF = 2.2 kΩ ±1%, USBMCLK = 20/24 MHz, PCLKA = 8 to 120 MHz,
PCLKB = 8 to 60 MHz, $T_a = T_{opr}$

Item	Symbol	Min.	Max.	Unit	Test Conditions
D+ sink current	I_{DP_SINK}	25	175	µA	
D– sink current	I_{DM_SINK}	25	175	µA	
DCD source current	I_{DP_SRC}	7	13	µA	
Data detection voltage	V_{DAT_REF}	0.25	0.4	V	
D+ source voltage	V_{DP_SRC}	0.5	0.7	V	Output current = 250 µA
D– source voltage	V_{DM_SRC}	0.5	0.7	V	Output current = 250 µA

2.5 A/D Conversion Characteristics

Table 2.49 12-Bit A/D (Unit 0) Conversion Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
PCLKB = PCLKC = 1 MHz to 60 MHz, $T_a = T_{opr}$, source impedance = 1.0 kΩ

Item		Min.	Typ.	Max.	Unit	Test Conditions
Resolution		8	—	12	Bit	
Analog input capacitance		—	—	30	pF	
Channel-dedicated sample-and-hold circuits in use (AN000 to AN002)	Conversion time*1 (Operation at PCLK = 60 MHz)	1.06 (0.40 + 0.25)*2	—	—	µs	• Sampling of channel-dedicated sample-and-hold circuits in 24 states • Sampling in 15 states
	Offset error	—	±1.5	±3.5	LSB	AN000 to AN002 = 0.25 V
	Full-scale error	—	±1.5	±3.5	LSB	AN000 to AN002 = VREFH0 –0.25 V
	Quantization error	—	±0.5	—	LSB	
	Absolute accuracy	—	±2.5	±5.5	LSB	
	DNL differential nonlinearity error	—	±1.0	±2.0	LSB	
	INL integral nonlinearity error	—	±1.5	±3.0	LSB	
	Holding characteristics of sample-and-hold circuits	—	—	20	µs	
	Dynamic range	0.25	—	VREFH0 – 0.25	V	
Channel-dedicated sample-and-hold circuits not in use (AN000 to AN007)	Conversion time*1 (Operation at PCLK = 60 MHz)	0.48 (0.267)*2	—	—	µs	Sampling in 16 states
	Offset error	—	±1.0	±2.5	LSB	
	Full-scale error	—	±1.0	±2.5	LSB	
	Quantization error	—	±0.5	—	LSB	
	Absolute accuracy	—	±2.0	±4.5	LSB	
	DNL differential nonlinearity error	—	±0.5	±1.5	LSB	
	INL integral nonlinearity error	—	±1.0	±2.5	LSB	

Note: The above specification values apply when there is no access to the external bus during A/D conversion. If access proceeds during A/D conversion, values may not fall within the above ranges.
Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.
Note 2. The value in parentheses indicates the sampling time.

Table 2.50 12-Bit A/D (Unit 1) Conversion Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
PCLKB = PCLKD = 1 MHz to 60 MHz, $T_a = T_{opr}$, source impedance = 1.0 kΩ

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	8	—	12	Bit	
Conversion time*1 (Operation at PCLK = 60 MHz)	0.88 (0.667)*2	—	—	µs	Sampling in 40 states
Analog input capacitance	—	—	30	pF	
Offset error	—	±2.0	±3.5	LSB	
Full-scale error	—	±2.0	±3.5	LSB	
Quantization error	—	±0.5	—	LSB	
Absolute accuracy	—	±4.0	±6.0	LSB	
DNL differential nonlinearity error	—	±1.5	±2.5	LSB	
INL integral nonlinearity error	—	±2.0	±3.5	LSB	

Note: The above specification values apply when there is no access to the external bus during A/D conversion. If access proceeds during A/D conversion, values may not fall within the above ranges.
Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.
Note 2. The value in parentheses indicates the sampling time.

Table 2.51 A/D Internal Reference Voltage Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
PCLKB = PCLKD = 60 MHz, $T_a = T_{opr}$

Item	Min.	Typ.	Max.	Unit	Test Conditions
A/D internal reference voltage	1.20	1.25	1.30	V	

2.6 D/A Conversion Characteristics

Table 2.52 D/A Conversion Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V,
2.7 ≤ VREFH0 ≤ AVCC0, VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
$T_a = T_{opr}$

Item		Min.	Typ.	Max.	Unit	Test Conditions
Resolution		12	12	12	Bit	
Direct output	Absolute accuracy	—	—	±6.0	LSB	2-MΩ resistive load 10-bit conversion
	DNL differential nonlinearity error	—	±1.0	±2.0	LSB	2-MΩ resistive load
	RO output resistance	—	7.5	—	kΩ	
	Conversion time	—	—	3.0	µs	20-pF capacitive load
Amplifier output	Resistive load	5	—	—	kΩ	
	Capacitive load	—		50	pF	
	Output voltage range	0.2	—	AVCC1 – 0.2	V	
	DNL differential nonlinearity error	—	±1.0	±2.0	LSB	
	INL integral nonlinearity error	—	±2.0	±4.0	LSB	
	Conversion time	—	—	4.0	µs	

2.7 Temperature Sensor Characteristics

Table 2.53 Temperature Sensor Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
$T_a = T_{opr}$

Item	Min.	Typ.	Max.	Unit	Test Conditions
Relative accuracy	—	±1	—	°C	
Temperature slope	—	4.1	—	mV/°C	
Output voltage	—	1.24	—	V	Ta = 25°C
Temperature sensor start time	—	—	30	µs	
Sampling time*1	4.15	—	—	µs	

Note 1. Set the S12AD1.ADSSTRT register such that the sampling time of the 12-bit A/D converter satisfies this specification.

2.8 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

Table 2.54 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
$T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	Low power consumption function disabled*1	V_{POR}	2.5	2.6	2.7	V	Figure 2.94
		Low power consumption function enabled*2		2.0	2.35	2.7		
	Voltage detection circuit (LVD0)		V_{det0_1}	2.84	2.94	3.04		Figure 2.95
			V_{det0_2}	2.77	2.87	2.97		
			V_{det0_3}	2.70	2.80	2.90		
	Voltage detection circuit (LVD1)		V_{det1_1}	2.89	2.99	3.09		Figure 2.96
			V_{det1_2}	2.82	2.92	3.02		
			V_{det1_3}	2.75	2.85	2.95		
	Voltage detection circuit (LVD2)		V_{det2_1}	2.89	2.99	3.09		Figure 2.97
			V_{det2_2}	2.82	2.92	3.02		
			V_{det2_3}	2.75	2.85	2.95		
Internal reset time	Power-on reset time		t_{POR}	—	4.6	—	ms	Figure 2.94
	LVD0 reset time		t_{LVD0}	—	0.70	—		Figure 2.95
	LVD1 reset time		t_{LVD1}	—	0.57	—		Figure 2.96
	LVD2 reset time		t_{LVD2}	—	0.57	—		Figure 2.97
Minimum VCC down time			t_{VOFF}	200	—	—	µs	Figure 2.94, Figure 2.95
Response delay time			t_{det}	—	—	200	µs	Figure 2.94 to Figure 2.97
LVD operation stabilization time (after LVD is enabled)*3			$T_{d(E-A)}$	—	—	10	µs	Figure 2.96, Figure 2.97
Hysteresis width (LVD1 and LVD2)			V_{LVH}	—	80	—	mV	

Note: The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det1}, and V_{det2} for the POR/ LVD.

Note 1. The low power consumption function is disabled and DEEPCUT[1:0] = 00b or 01b.

Note 2. The low power consumption function is enabled and DEEPCUT[1:0] = 11b.

Note 3. The voltage of VCC = AVCC0 = AVCC1 when LVD1 is enabled must be set to at least 80 mV above the maximum value of the voltage detection 1 level ($V_{det1_1, 2, 3}$) selected by the LVDLVLR.LVD1LVL[3:0] bits. Similarly, the voltage of VCC = AVCC0 = AVCC1 when LVD2 is enabled must be set to at least 80 mV above the maximum value of the voltage detection 2 level ($V_{det2_1, 2, 3}$) selected by the LVDLVLR.LVD2LVL[3:0] bits.

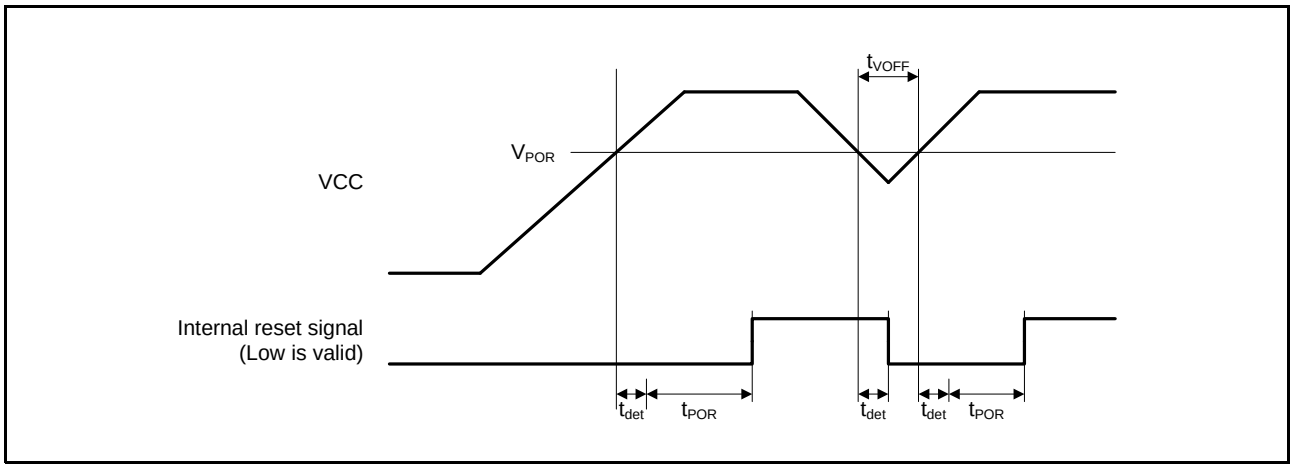


Figure 2.94 Power-on Reset Timing

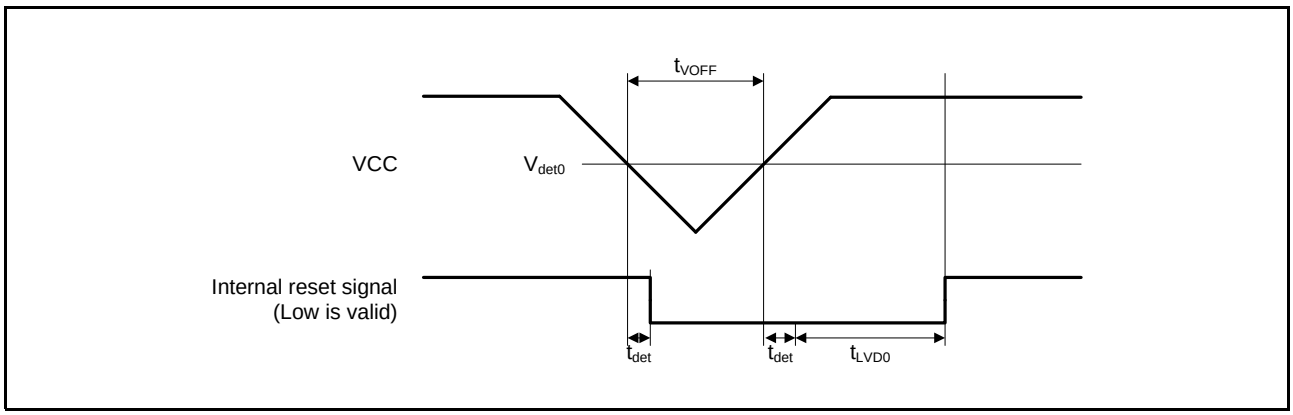


Figure 2.95 Voltage Detection Circuit Timing (V_{det0})

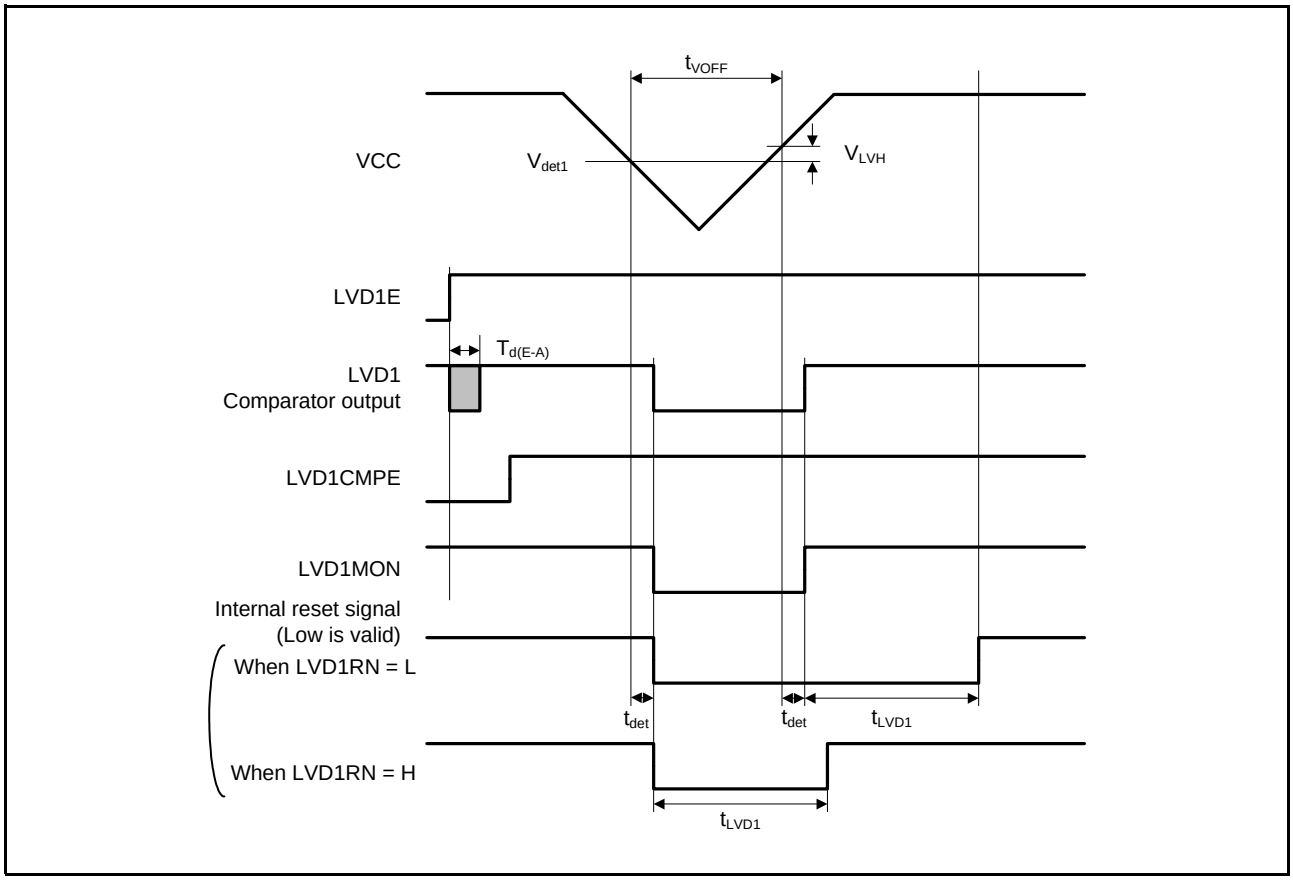


Figure 2.96 Voltage Detection Circuit Timing (V_{det1})

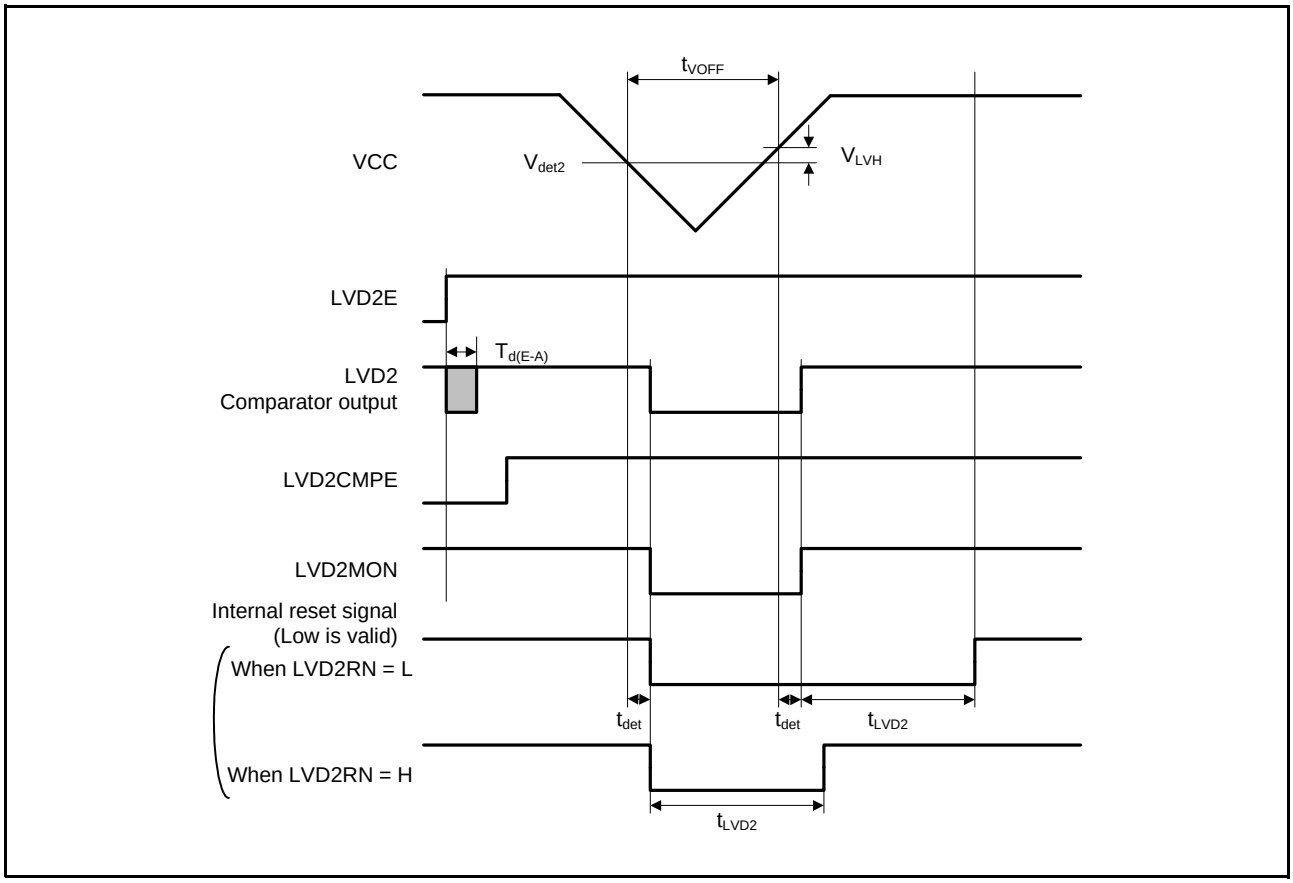


Figure 2.97 Voltage Detection Circuit Timing (V_{det2})

2.9 Oscillation Stop Detection Timing

Table 2.55 Oscillation Stop Detection Circuit Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t_{dr}	—	—	1	ms	Figure 2.98

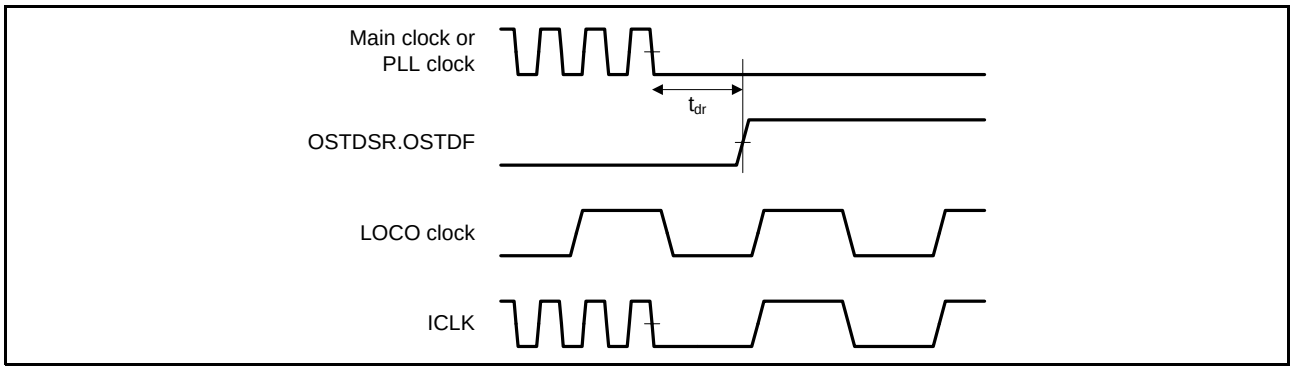


Figure 2.98 Oscillation Stop Detection Timing

2.10 Battery Backup Function Characteristics

Table 2.56 Battery Backup Function Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
V_{BATT} = 2.0 to 3.6 V, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage level for switching to battery backup	$V_{DETBATT}$	2.50	2.60	2.70	V	Figure 2.99
Lower-limit V_{BATT} voltage for power supply switching due to VCC voltage drop*1	V_{BATTSW}	2.70	—	—		
VCC-off period for starting power supply switching*1	$t_{VOFFBATT}$	200	—	—	µs	

Note 1. The VBATT voltage must not fall below its lower limit VBATTSW when the source of supply is switched to VBATT from VCC due to a drop in VCC.

Note 2. The VCC-off period in switching of the power supply indicates the period from VCC falling below the minimum value of the battery backup switching threshold voltage (VDETBATT) until the source of power is switched to VBATT. If VCC recovers within this period, the source may not be switched to VBATT and supply from VCC is continued instead.

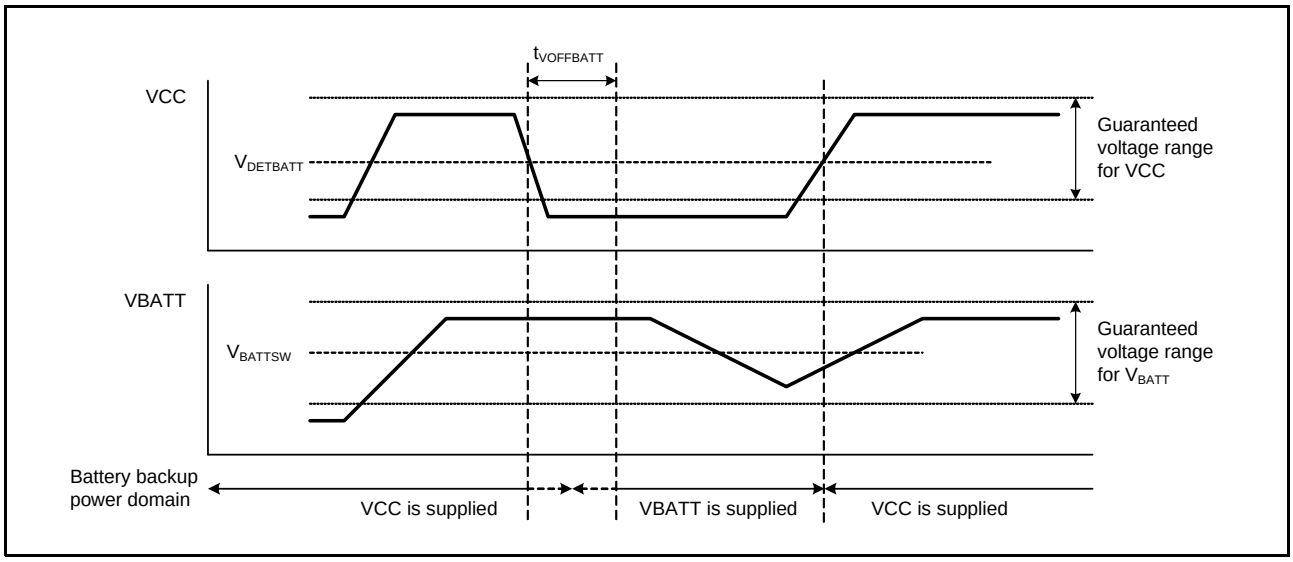


Figure 2.99 Battery Backup Function Characteristics

2.11 Flash Memory Characteristics

Table 2.57 Code Flash Memory Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V
Temperature range for programming/erasure: $T_a = T_{opr}$

Item		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	Test Conditions
			Min.	Typ.	Max.	Min.	Typ.	Max.		
Programming time N_{PEC} ≤ 100 times	256 bytes	t_{P256}	—	0.9	13.2	—	0.4	6	ms	
	8 Kbytes	t_{P8K}	—	29	176	—	13	80	ms	
	32 Kbytes	t_{P32K}	—	116	704	—	52	320	ms	
Programming time N_{PEC} > 100 times	256 bytes	t_{P256}	—	1.1	15.8	—	0.5	7.2	ms	
	8 Kbytes	t_{P8K}	—	35	212	—	16	96	ms	
	32 Kbytes	t_{P32K}	—	140	848	—	64	384	ms	
Erasure time N_{PEC} ≤ 100 times	8 Kbytes	t_{E8K}	—	71	216	—	39	120	ms	
	32 Kbytes	t_{E32K}	—	254	864	—	141	480	ms	
Erasure time N_{PEC} > 100 times	8 Kbytes	t_{E8K}	—	85	260	—	47	144	ms	
	32 Kbytes	t_{E32K}	—	304	1040	—	169	576	ms	
Reprogramming/erasure cycle*1		N_{PEC}	1000*2	—	—	1000*2	—	—	Times	
Suspend delay time during programming		t_{SPD}	—	—	264	—	—	120	µs	
First suspend delay time during erasing (in suspend priority mode)		t_{SESD1}	—	—	216	—	—	120	µs	
Second suspend delay time during erasure (in suspend priority mode)		t_{SESD2}	—	—	1.7	—	—	1.7	ms	
Suspend delay time during erasure (in erasure priority mode)		t_{SEED}	—	—	1.7	—	—	1.7	ms	
Forced stop command		t_{FD}	—	—	32	—	—	20	µs	
Data hold time*3, *4		t_{DRP}	20	—	—	20	—	—	Year	T_a ≤ 85°C
			10	—	—	10	—	—		T_a ≤ 105°C
FCU reset time		t_{FCUR}	35	—	—	35	—	—	µs	

Note 1. Definition of reprogram/erase cycle:
The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 256-byte programming is performed 32 times for different addresses in 8-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. This is the minimum number of times to guarantee all the characteristics after reprogramming (guaranteed range is from 1 to the value of the minimum value).

Note 3. This shows the characteristic when the flash memory writer or self-programming library from Renesas Electronics is in use, and the number of times programming and erasure proceed does not exceed the specified value.

Note 4. These values are based on the results of reliability testing.

Table 2.58 Data Flash Memory Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
Temperature range for programming/erasure: $T_a = T_{opr}$

Item		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	Test Conditions
			Min.	Typ.	Max.	Min.	Typ.	Max.		
Programming time	4 bytes	t_{DP4}	—	0.36	3.8	—	0.16	1.7	ms	
Erasure time	64 bytes	t_{DE64}	—	3.1	18	—	1.7	10	ms	
Blank check time	4 bytes	t_{DBC4}	—	—	84	—	—	30	µs	
	64 bytes	t_{DBC64}	—	—	280	—	—	100	µs	
	2 Kbytes	t_{DBC2K}	—	—	6169	—	—	2200	µs	
Reprogramming/erasure cycle*1		N_{DPEC}	100000 *2	—	—	100000 *2	—	—	Times	
Suspend delay time during programming		t_{DSPD}	—	—	264	—	—	120	µs	
First suspend delay time during erasure (in suspend priority mode)		t_{DSESD1}	—	—	216	—	—	120	µs	
Second suspend delay time during erasure (in suspend priority mode)		t_{DSESD2}	—	—	300	—	—	300	µs	
Suspend delay time during erasing (in erasure priority mode)		t_{DSEED}	—	—	300	—	—	300	µs	
Forced stop command		t_{FD}	—	—	32	—	—	20	µs	
Data hold time*3, *4		t_{DDRP}	20	—	—	20	—	—	Year	$T_a \leq 85°C$
			10	—	—	10	—	—		$T_a \leq 105°C$

Note 1. Definition of reprogram/erase cycle:
The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 100000), erasing can be performed n times for each block. For instance, when 4-byte programming is performed 512 times for different addresses in 2-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. This is the minimum number of times to guarantee all the characteristics after reprogramming (guaranteed range is from 1 to the value of the minimum value).

Note 3. This shows the characteristic when the flash memory writer or self-programming library from Renesas Electronics is in use, and the number of times programming and erasure proceed does not exceed the specified value.

Note 4. These values are based on the results of reliability testing.

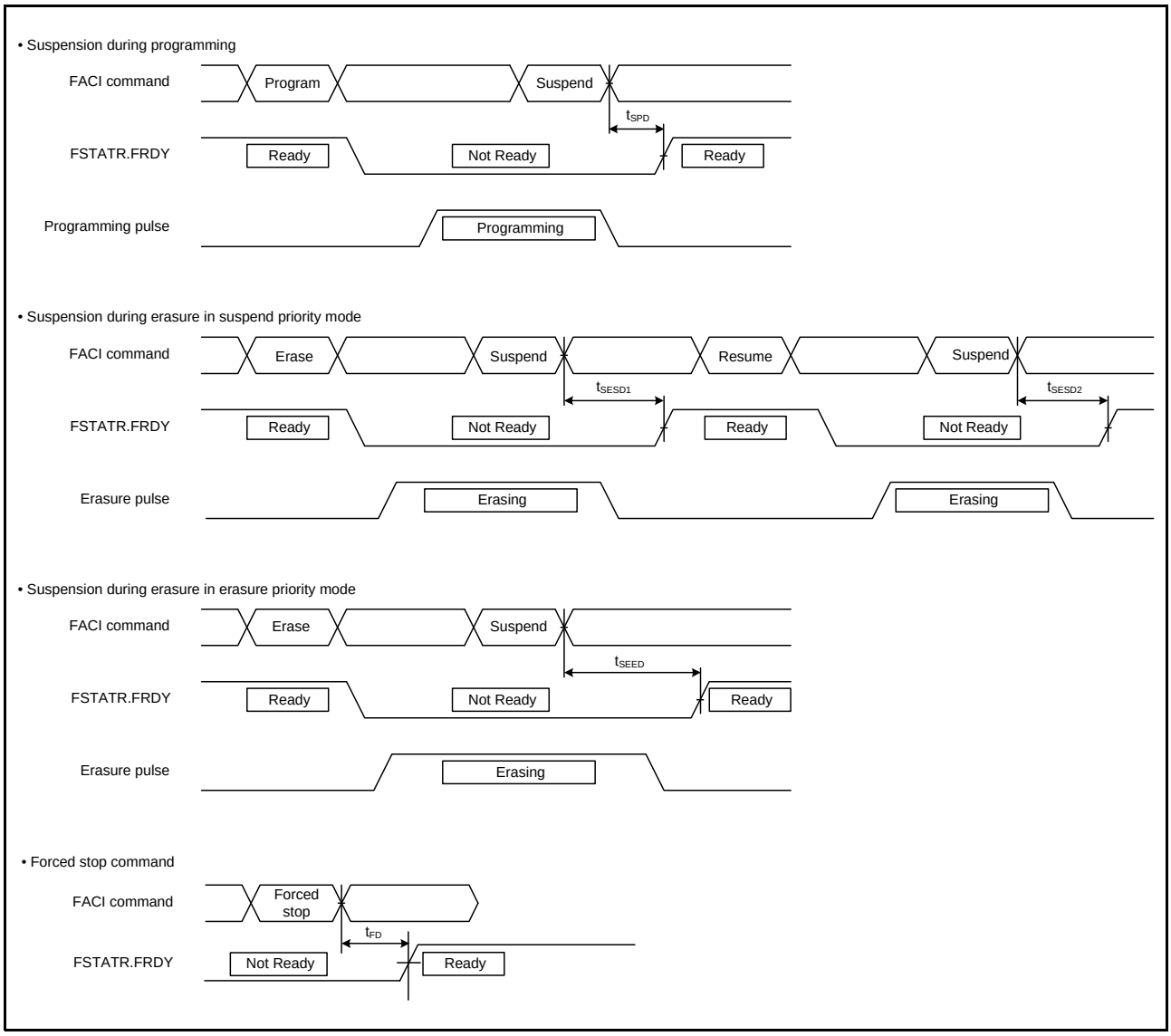


Figure 2.100 Flash Memory Programming/Erasure Suspension Timing

2.12 Boundary Scan

Table 2.59 Boundary Scan Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
$T_a = T_{opr}$
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF
High-drive output is selected by the driving ability control register.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
TCK clock cycle time	t_{TCKcyc}	100	—	—	ns	Figure 2.101
TCK clock high pulse width	t_{TCKH}	45	—	—	ns	
TCK clock low pulse width	t_{TCKL}	45	—	—	ns	
TCK clock rise time	t_{TCKr}	—	—	5	ns	
TCK clock fall time	t_{TCKf}	—	—	5	ns	
TRST# pulse width	t_{TRSTW}	20	—	—	t_{TCKcyc}	Figure 2.102
TMS setup time	t_{TMSS}	20	—	—	ns	Figure 2.103
TMS hold time	t_{TMSH}	20	—	—	ns	
TDI setup time	t_{TDIS}	20	—	—	ns	
TDI hold time	t_{TDIH}	20	—	—	ns	
TDO data delay time	t_{TDOD}	—	—	40	ns	

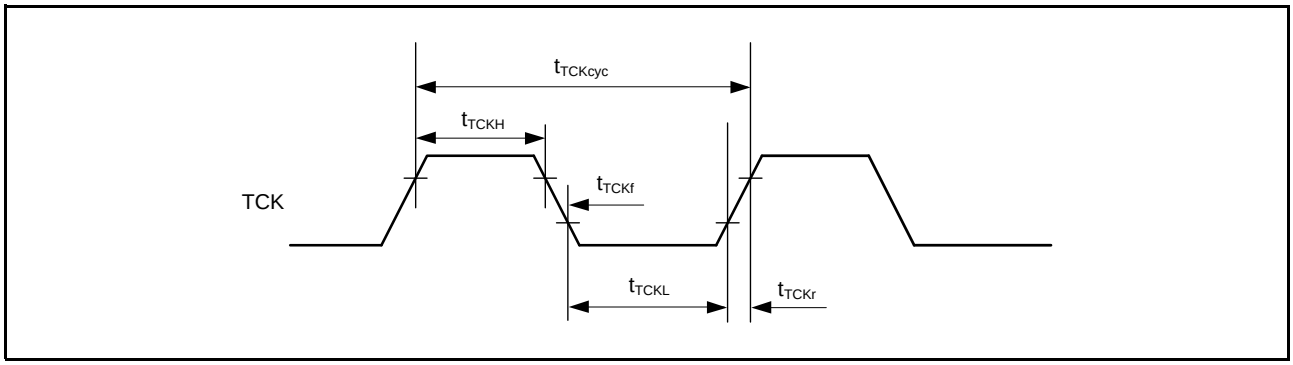


Figure 2.101 Boundary Scan TCK Timing

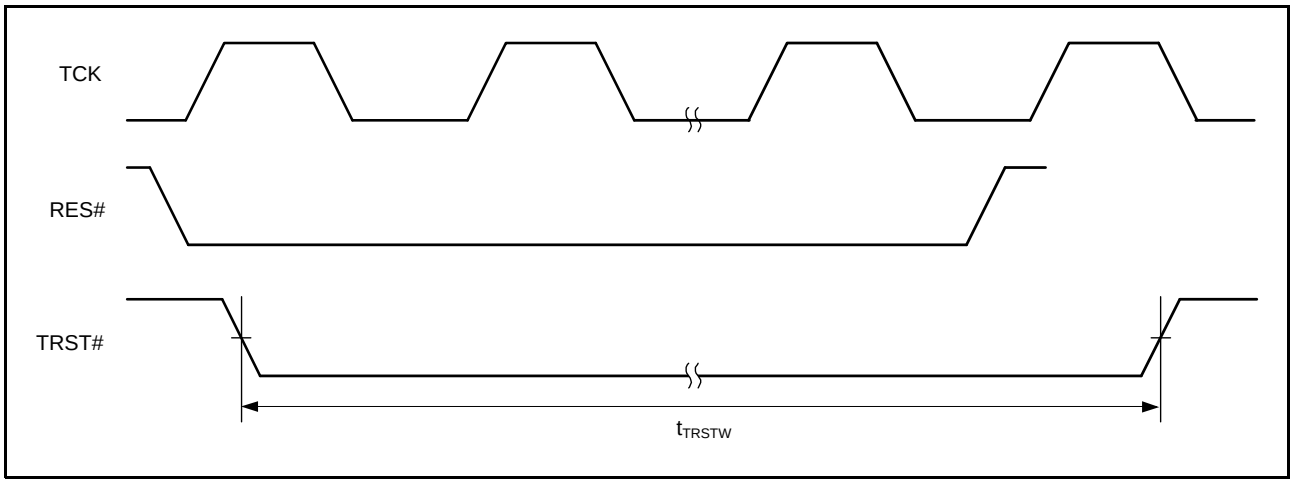


Figure 2.102 Boundary Scan TRST# Timing

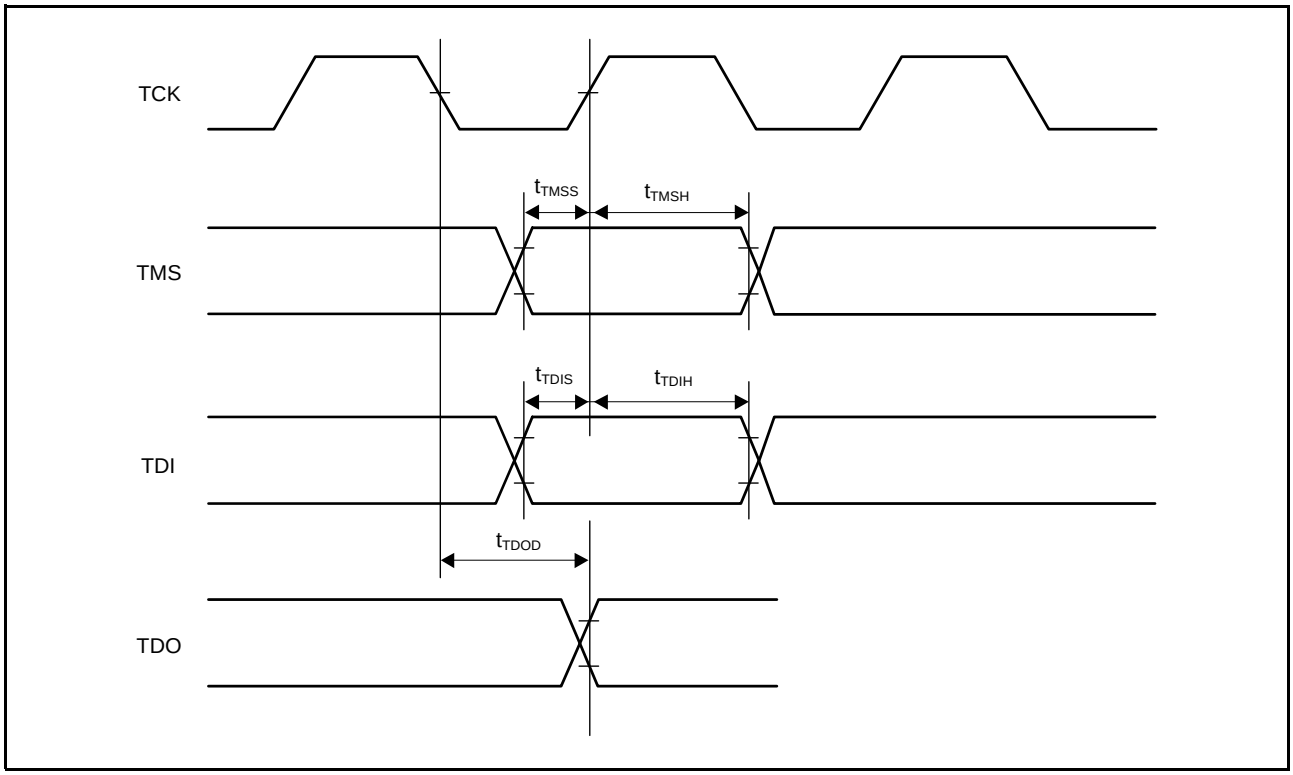
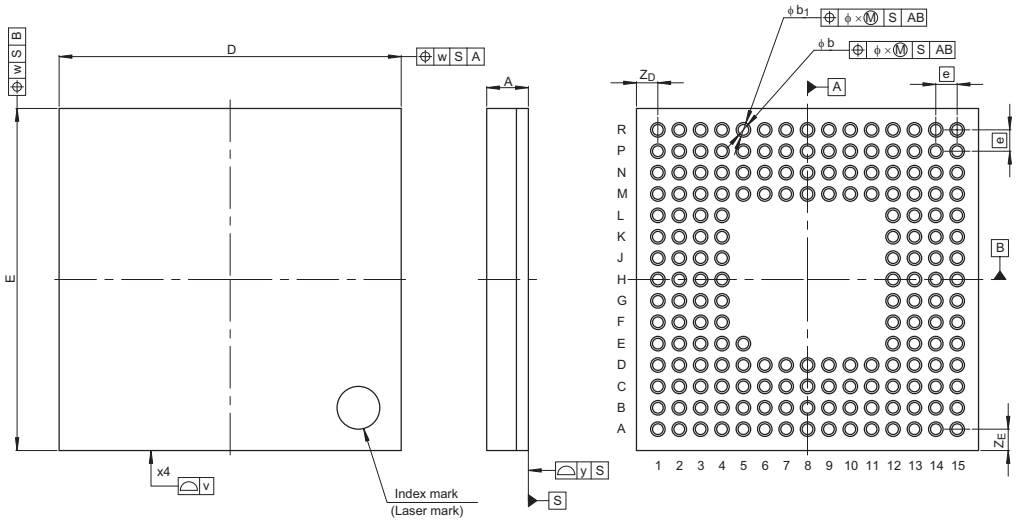


Figure 2.103 Boundary Scan Input/Output Timing

Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

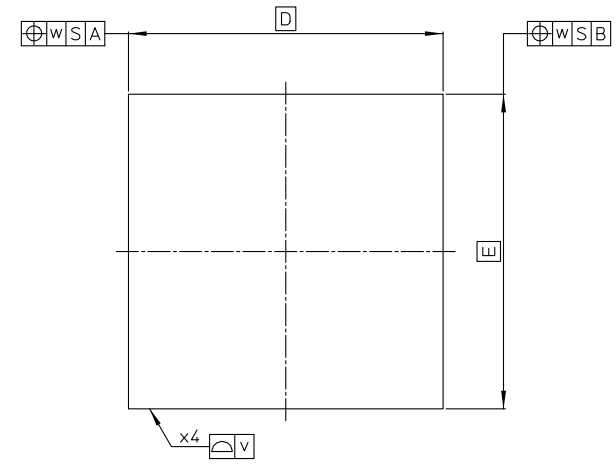
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TFLGA177-8x8-0.50	PTLG0177KA-A	177F0E-A	0.2g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	8.0	—
E	—	8.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.05
e	—	0.5	—
b	0.21	0.25	0.29
b_1	0.29	0.34	0.39
x	—	—	0.08
y	—	—	0.08
Z_D	—	0.5	—
Z_E	—	0.5	—

Figure A 177-Pin TFLGA (PTLG0177KA-A)

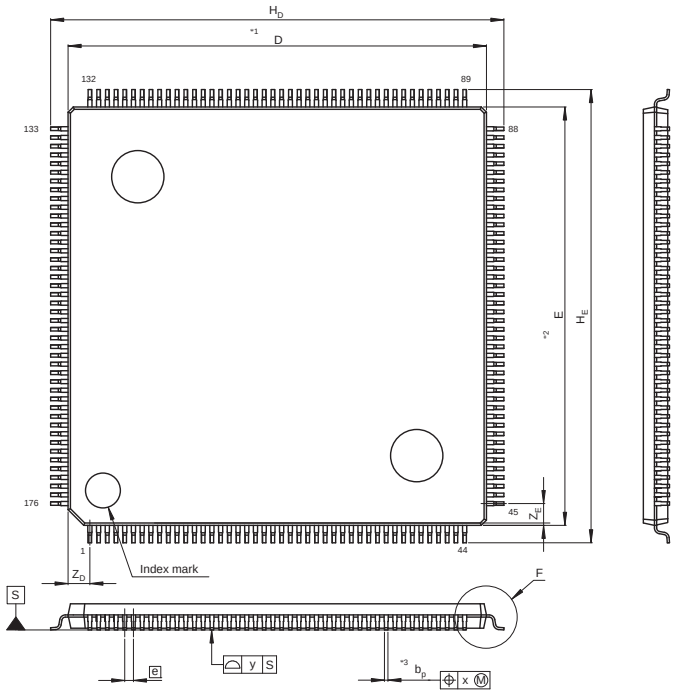
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFBGA176-13x13-0.80	PLBG0176GA-A	BP-176/BP-176V	0.45g

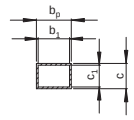


Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	13.0	—
E	—	13.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.40
A_1	0.35	0.40	0.45
e	—	0.80	—
b	0.45	0.50	0.55
x	—	—	0.08
y	—	—	0.10
y_1	—	—	0.2
S_D	—	—	—
S_E	—	—	—
Z_D	—	0.90	—
Z_E	—	0.90	—

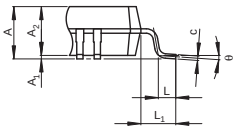
Figure B 176-Pin LFBGA (PLBG0176GA-A)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP176-24x24-0.50	PLQP0176KB-A	176P6Q-A/FP-176E/FP-176EV	1.8g





Terminal cross section



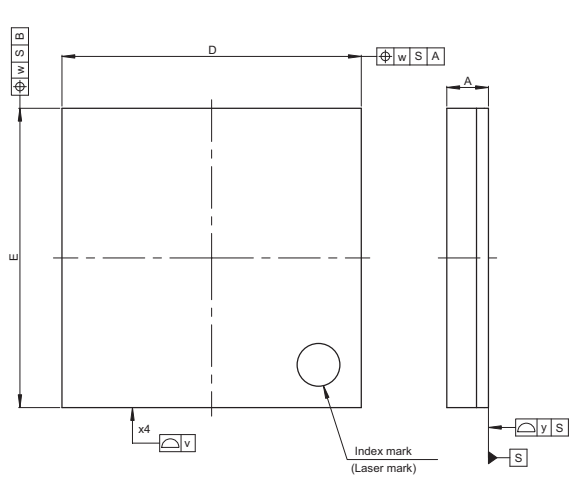
Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	23.9	24.0	24.1
E	23.9	24.0	24.1
A_2	—	1.4	—
H_D	25.8	26.0	26.2
H_E	25.8	26.0	26.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure C 176-Pin LFQFP (PLQP0176KB-A)

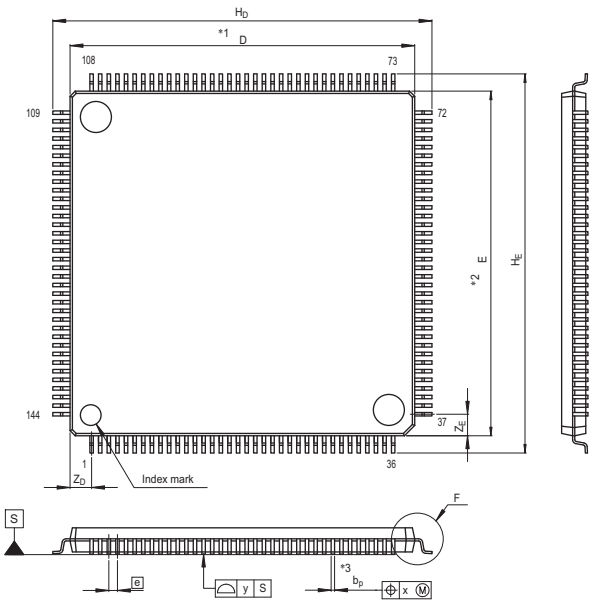
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TFLGA145-7x7-0.50	PTLG0145KA-A	145F0G	0.1g

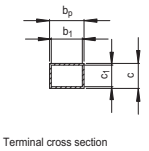


Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	7.0	—
E	—	7.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.05
e	—	0.5	—
b	0.21	0.25	0.29
b_1	0.29	0.34	0.39
x	—	—	0.08
y	—	—	0.08
Z_D	—	0.5	—
Z_E	—	0.5	—

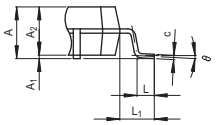
Figure D 145-Pin TFLGA (PTLG0145KA-A)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP144-20x20-0.50	PLQP0144KA-A	144P6Q-A / FP-144L / FP-144LV	1.2g





Terminal cross section



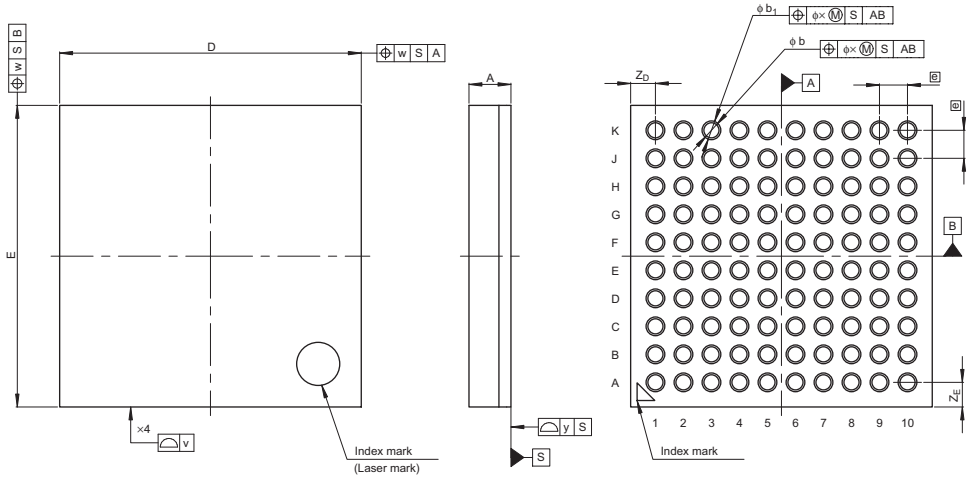
Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.9	20.0	20.1
E	19.9	20.0	20.1
A_2	—	1.4	—
H_D	21.8	22.0	22.2
H_E	21.8	22.0	22.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure E 144-Pin LFQFP (PLQP0144KA-A)

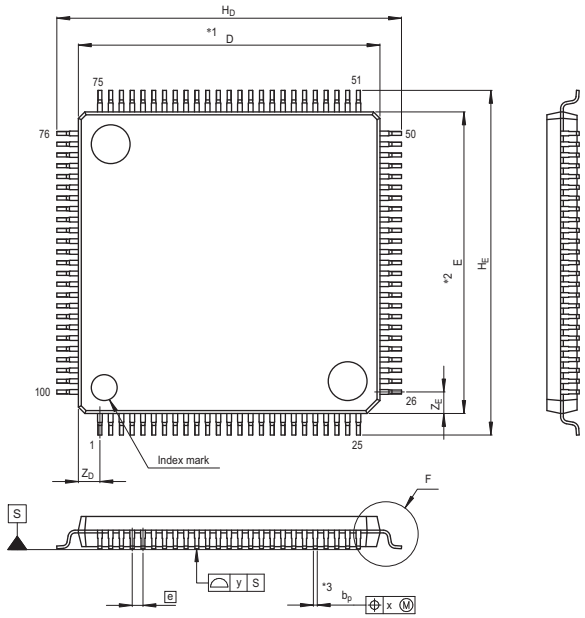
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TFLGA100-7x7-0.65	PTLG0100JA-A	100F0G	0.1g



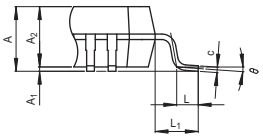
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	7.0	—
E	—	7.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.05
e	—	0.65	—
b	0.31	0.35	0.39
b_1	0.385	0.435	0.485
x	—	—	0.08
y	—	—	0.10
Z_D	—	0.575	—
Z_E	—	0.575	—

Figure F 100-Pin TFLGA (PTLG0100JA-A)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP100-14x14-0.50	PLQP0100KB-A	100P6Q-A / FP-100U / FP-100UV	0.6g



Terminal cross section



Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure G 100-Pin LFQFP (PLQP0100KB-A)

REVISION HISTORY	RX71M Group User's Manual: Datasheet

Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

Rev.	Date	Description		Classification
		Page	Summary	
1.00	Jan 15, 2015	—	First edition, issued	
1.10	Dec 28, 2017	All	Terms unified: GPTa → GPTA LQFP → LFQFP	
		Features		
		1	AES key lengths, changed	TN-RX*-A122A/E
		1. Overview		
		2	Table 1.1 Outline of Specifications (1/9), changed	TN-RX*-A127A/E
		5	Table 1.1 Outline of Specifications (4/9), changed	
		8	Table 1.1 Outline of Specifications (7/9), changed	
		9	Table 1.1 Outline of Specifications (8/9), changed	
		10	Table 1.1 Outline of Specifications (9/9), changed	TN-RX*-A122A/E
		23	Table 1.4 Pin Functions (6/8), changed	
		48	Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (2/5), changed	TN-RX*-A122A/E
		52	Table 1.8 List of Pin and Pin Functions (144-Pin LFQFP) (1/5), changed	
		55	Table 1.8 List of Pin and Pin Functions (144-Pin LFQFP) (4/5), changed	
		58	Table 1.9 List of Pin and Pin Functions (100-Pin TFLGA) (2/4), changed	
		63	Table 1.10 List of Pin and Pin Functions (100-Pin LFQFP) (3/4), changed	
		4. I/O Registers		
		108	Table 4.1 List of I/O Registers (Address Order) (37 / 70) 0008 C296h, added	
		110	Table 4.1 List of I/O Registers (Address Order) (39 / 70), changed	TN-RX*-A152A/E
		111	Table 4.1 List of I/O Registers (Address Order) (40 / 70), changed	
		112	Table 4.1 List of I/O Registers (Address Order) (41 / 70), changed	
		134, 135	Table 4.1 List of I/O Registers (Address Order) (63 / 70) (64 / 70), changed	
		142	Table 4.1 List of I/O Registers (Address Order), Note 6 added	TN-RX*-A152A/E
		5. Electrical Characteristics		
		143	Table 5.1 Absolute Maximum Rating, changed	TN-RX*-A160A/E TN-RX*-A178A/E
		143	Table 5.2 Recommended Operating Conditions, added	TN-RX*-A178A/E
		144	Table 5.3 DC Characteristics (1), changed	TN-RX*-A159A/E TN-RX*-A160A/E TN-RX*-A178A/E
		145	Table 5.4 DC Characteristics (2), changed	TN-RX*-A159A/E
		148	Table 5.7 Thermal Resistances (Reference), added	TN-RX*-A178A/E
		187	Figure 5.48 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKA Division Ratio Set to 1/2), changed	TN-RX*-A159A/E
		208	Figure 5.82 Test Circuit (High-Speed), changed	
		211	Table 5.52 Temperature Sensor Characteristics, changed	TN-RX*-A159A/E
		217	Figure 5.88 Battery Backup Function Characteristics, changed	
		218	Table 5.56 Code Flash Memory Characteristics, changed	TN-RX*-A146A/E
		219	Table 5.57 Data Flash Memory Characteristics, changed	
1.20	Oct 20, 2022	All	G-version products added	TN-RX*-A0203A/E
		Features		
		1	Operating temp. rangeh, changed	
		1. Overview		
		3	Table 1.1 Outline of Specifications (2/9), changed	
		10	Table 1.1 Outline of Specifications (9/9), changed	
		16	Table 1.3 List of Products (4/4), changed	
		17	Figure 1.1 How to Read the Product Part Number, changed	
		24	Table 1.4 Pin Functions (6/8), changed	

Rev.	Date	Description		Classification
		Page	Summary	
1.20	Oct 20, 2022	2.Electrical Characteristics		
		67	Table 2.1 Absolute Maximum Rating, changed	
		67	Table 2.2 Recommended Operating Conditions, changed	
		69	Table 2.4 DC Characteristics (2), changed	
		70, 71	Table 2.5 DC Characteristics (3), changed	
		72	Table 2.6 DC Characteristics (4), changed	
		73	Table 2.7 Thermal Resistances (Reference), changed	
		79	Table 2.16 LOCO and IWDT-Dedicated Low-Speed Clock Timing, changed	
		148	Table 2.56 Battery Backup Function Characteristics, changed	
		149	Table 2.57 Code Flash Memory Characteristics, changed	
		151	Figure 2.100 Flash Memory Programming/Erasure Suspension Timing, changed	

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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